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COVER SHEET FOR TECHNICAL MEMORANDUM

TITLE- Future Spaceborne Memories with 10^3-10^7 Bit Capacities

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ABSTRACT

Weight, volume and power consumption of small (10^3-10^7 bit capacity) digital storage units are estimated for the 1970-1972 period. Technologies considered in the study include laminated ferrites, planar thin films, plated wires, metal-oxide-silicon (MOS) integrated circuits, ferrite cores and tape recorders. All of these except MOS integrated circuits retain stored information if power is cut, i.e., they are nonvolatile.

It is found that future spaceborne memories will be available with the following characteristics as a first approximation:

Capacity(bits)	Weight(lbs)	Volume(in^3)	Power(watts)
10^3 - 10^4	<.03	<.2	<10
10^4 - 10^5	<.3	<2	<30
10^5 - 10^6	<3	<10	<50
10^6 - 10^7	<30	<100	<100

These figures are for memories with $\leq 2\mu$ sec. cycle time. Lower powers can be obtained at the expense of speed and the various other parameters. Curves are included in the memorandum that show the variations among volume, weight, capacity, power, speed, and choice of technology.

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SUBJECT: Future Spaceborne Memories with 10^3-10^7 Bit Capacities - Case 103

DATE: July 26, 1968

FROM: B. W. Kim
TM-68-1031-4

TECHNICAL MEMORANDUM

1.0 INTRODUCTION

The purpose of this memorandum is to estimate the weight, volume and power consumption of digital storage units which could be made available in 1970-1972 for spaceborne applications and which have storage capacities in the range 10^3-10^7 bits.* Other considerations important for space applications such as temperature, radiation, shock, vibration, pressure, linear acceleration and angular rate are not considered here.

Among many memory devices which will be available in 1970-1972, laminated ferrite, planar thin film, plated wire, and MOS integrated circuit technologies were selected for consideration here. Core memories and tape recorders have been predominantly used for space applications and were also selected for comparison with other technologies. Bipolar transistors are another strong contender for future storage applications but are omitted here because of their large power consumption and the resultant cooling problems. They would, however, be the best candidate for the applications in which high memory speed is desired.

Storage units based on these devices except tape recorders would have no moving parts. They could be used to satisfy the buffer or main storage requirements for unmanned satellites and probes as well as manned spacecrafts.

Most estimates here are based mainly on data or analysis of data found in the references cited at the end of this memorandum. Weight, volume, and power consumption of the storage units are plotted against storage capacity in Figures 1-3 for different storage technologies. The total weight of the storage units and their respective power supplies is plotted in Figure 4 in the same fashion using 500 lbs. per 1,000 watts of power supply as a reasonable estimate of the early 70's.(1) All the curves are generated

*For comparison, the largest IBM 4πEP spaceborne computer memory has 4.7×10^6 bits, the Gemini tape recorder 7×10^7 bits and the Apollo tape recorder $1 - 3 \times 10^8$ bits.

such that each represents its own reasonably typical constraints such as memory speed. Moreover, memory system organizations (such as the number of bits per word) and objectives of the units (such as low power consumption and speed) play such a large role in volume, weight, and power consumption that figures for particular memories may depart widely from these curves.

2.0 MEMORY TECHNOLOGIES

2.1 Tape Recorders

Current spaceborne digital tape recorders have single-reel capacities in the 10^4-10^8 bit range. They weigh 6-15 lbs., have volumes 200-300 $in.^3$, but consume very little power, 1-2 watts.[2] Not only have they large weight and volume but also moving parts. Recent developments in batch fabrication of solid state memory devices offer smaller and lighter memories with less or equal power consumption but with no moving parts. Even with improvements[3] of tape recorders expected in 1970-1972 such as higher storage density of the tapes (about twice current tape density), lower power consumption by utilizing brushless D.C. motors, and smaller volume and weight (very little improvement) by using integrated circuit electronics, they do not seem to measure up to the potential advantages of solid state storage units, as shown in Figures 1-3. The tape recorders weigh less than others, above 10^6 bit capacities, only when the weight of power supplies is considered.

2.2 Magnetic Cores

Magnetic cores have been the predominant technology in spaceborne random-access memories. They have enjoyed wide acceptance and may stay with us a little longer mainly because of their long established and well-understood technology. But they seem to be near the saturation point in improvements.

Current cores[4-6] have 20/12 mil sizes and about 1,600 bits/$in.^2$ packing densities. Because each core must be manually or semiautomatically threaded with conductors in the manufacturing process, there is an inherent limit in reducing the core sizes with a fixed number of conductors to thread. The core memories also suffer from the limitation of their destructive-read-out (DRO) operations, which require rewriting at each reading access. More sophisticated geometries are used to make them nondestructive-read-out (NDRO) operative such as the multiaperture devices (MAD) and Biax. But no significant improvements in materials or geometries are expected by 1970-1972.

An improvement of bit packing density by a factor of two is expected with faster memory speed (several hundred nanosecond cycle times) than current memory speeds (a few microsecond cycle times).

2.3 Laminated Ferrites

Storage units consisting of laminated ferrite planes, MOS drivers and selection logic, and bipolar transistor sense amplifiers have been developed by RCA Laboratories[7-9]. They are word-organized, random access, DRO, nonvolatile memories. Briefly, a laminated array is a sandwich of three ferrite sheets with an embedded matrix of conductors fabricated by a batch process. The embedded conductors form two sets of insulated, mutually orthogonal windings with 10 mil center spacings. One set of windings is used for read-write energization (word lines) and the other set for the sense-digit function (digit lines). Laminated memory planes with up to 1,024 x 200 crossovers have been built, but fabrication difficulty limits the practical size up to 512 x 200 crossovers.

A 4-plane assembly which has been built[7] has the following characteristics:

Memory capacity	65,536 bits
Number of words	1,024
Number of bits per word	64
Size	2.85 x 0.78 x 0.25 $in.^3$
Weight	0.04 lbs.

Word select circuits, address decoders, and digit sensors and drivers necessary to make this assembly a complete random access memory would, for example, require two slabs of alumina substrate with 84 chips of integrated circuits.[10] A little calculation shows that each slab with the chips has a size of 2.85 x 0.78 x 0.085 $in.^3$ and 0.025 lbs. The power consumption in each digit line (about one-third watt at 1 MHZ) accounts for almost all power consumption of the storage unit.[11] This results in about 21 watts of power consumption for the above 4-plane assembly with 2 microsecond access cycle. To complete the above table, we have, for 65,536 bit capacity:

Memory system volume	9.3×10^{-1} $in.^3$
Memory system weight	0.065 lbs.
Average power consumption for a 2 microsecond access cycle	21 watts

A preliminary estimate[6] shows that a memory could be built with the following characteristics:

Memory capacity	1.3×10^7 bits
Number of words	65,536
Number of bits per word	200
Memory system volume	130 $in.^3$
Memory system weight	15 lbs.
Average power consumption for:	
a 2 microsecond access cycle	100 watts
a 200 microsecond access cycle	10 watts

Faster cycle times can be achieved using shorter sense-digit lines and increased word currents. Currently, efforts are being made by RCA under a NASA contract to reduce the power consumption in the bipolar transistor sense amplifiers.

The curves corresponding to laminated ferrite memories in Figures 1-3 are simply straight line projections of the data of the two cases presented above. The effect of the power supply weight, as shown in Figure 3, on the uncompensated weight curve of Figure 2 is a much smaller slope and the shift of this weight curve from a lower (lighter) region to a higher (heavier) region among all the curves. This is due to the fact that most of the power in laminated memories is consumed in the digit lines whose number is not reduced in direct proportion to the reduction of storage capacity in our consideration of memory organizations, and that power consumption of laminated ferrite memories is one of the highest even though weight is one of the lowest.

2.4 MOS Integrated Circuits

Recent developments[12-17] in large scale integration (LSI) of semiconductor circuits have made the semiconductor memory extremely attractive and practical, since a memory system requires large numbers of identical devices or components connected in a regular pattern. The outstanding performance characteristics of the semiconductor memory are related to the electrical and physical compatibility of high-speed integrated circuit logic and memory elements. High-speed operation with NDRO operation is obtained at no extra cost. However, MOS memories are volatile, i.e., they lose stored information if power is cut off.

Because of its extremely low power (10 nw. per bit) and convenient static operation, complementary MOS was selected here for further study even though p-channel and n-channel MOS devices have their own advantages. This low power consideration is important not only because power is costly in terms of weight but also because in current aerospace computers the memory subsystem consumes approximately 40% to 60% of the total computer power.(18)

2.4.1 Random-access MOS Memory

Currently, a 16 x 16 bit read-write complementary MOS memory chip of size 32 x 10^3 $mils^2$ including address logic and line drivers has been made.(14) This size can be squeezed to 100 x 100 $mils^2$, and by 1970 the capacity of the chip is expected to be increased to 32 x 16 bits on this size.(19)

A feasibility study(10) showed that an alumina substrate with size 12 cm. x 8 cm. and 90 interconnection leads on 1.25 mm. centers on one 12 cm. edge could accommodate a 32K bit memory module with 256 2-$mm.^2$ p-channel MOS read-write memory chips and 84 peripheral electronics chips by making use of the beam-lead technology.(20) This module would have 1,024 words, 32 bits per word, with each memory chip having 16 words, 8 bits each. It would have 32 leads for input data, 32 for output, 20 for 10-bit address and 6 for power and timing. The peripheral electronics of this module consumes about 1.46 watts.

A total of 64 100 x 100 $mils^2$ complementary MOS memory chips, 32 x 16 bits each, can be placed on the same alumina substrate in place of 256 p-channel MOS memory chips to make the same 1,024 words x 32 bits memory module. This module would weigh 0.1 lb. with 1.25 $in.^3$ volume and would consume 0.064 watts operative (at 1 MHZ) and 3.2 x 10^{-4} watts standby powers in the 64 memory chips in addition to 1.46 watts in the 84 peripheral electronics chips.(10) Allowing about 3.3 watts for central timing and register circuits,(10) the total power consumption would be about 4.8 watts.

There seems to be little motivation for increasing the module size above the 32K bit level, since assembly, test, repair, and interconnection problems would become severe above 32K bits. The anticipated cost, reliability, power requirements, and physical size of the 32K bit module are such that it appears reasonable to consider assembling a larger memory from a number of these modules.

Address selection, parallel driving of data lines, interconnection, noise, and maintainability should be considered to determine a reasonable number of modules.

For example, 32 of these modules could be assembled to make a 10^6 bit memory with 32K words, 32 bits per word. A 15 bit binary address is required for word selection. The 10 least significant bits of the address are connected in parallel to the decoder inputs on all 32 modules. The five remaining address bits are centrally decoded and used to route power supply and/or timing pulses to one of 32 modules. Therefore, the digit circuits of only one of the 32 modules will be energized at any one time, resulting in tremendous power reduction. The digit output lines of 32 modules can be tied together and then connected to the output register drivers. The full cycle time is expected to be less than 220 ns.(10)

The 32 modules can be mounted in parallel on the back panel on about 1/3 cm. centers. The total volume would be 60 $in.^3$, and weight 3.2 lbs. Since only one module is activated at any time, the total power consumption would be the power consumption of a module plus central decoder timing and register circuits and the standby power of memory cells (10^{-2} watts). This would be about 5.6 watts.

2.4.2 Sequential-access MOS storage

A random-access MOS storage unit can be made into a sequential-access unit by adding a counter to the address register. In fact, this may be the solution for large capacity sequential-access MOS storage units. But MOS shift registers are also very suitable for sequential access units. There would be as many parallel shift registers as the desired number of bits per word or the total number of bits in the combined inputs.

At the present time, a 100 x 100 $mils^2$ chip can be made to hold a 100 bit complementary(13) or a 200 bit p-channel(16-21) MOS shift register. By 1970-1972, the same size chip is expected to hold a 200 bit complementary(19) or a 2,000 bit p-channel(16-21) MOS shift register. Evidently, the p-channel MOS shift register has far better density, but its standby power consumption is far greater than that of the complementary MOS shift register. Complementary MOS shift registers consume about 10^{-4} watts per bit at 1 MHZ assuming each bit drives 1 pf. load within a chip and the power supply is 10 volts. Because of the inherent nature of shift registers, total power consumption is directly proportional to the storage capacity. This restricts the capacity of MOS sequential memories to the low range.

The complementary MOS shift registers are selected here since they consume almost no standby power. With the same packaging technique as in section 2.4.1, a 12 x 8 cm.^{2} alumina board will contain about 1,260 100 x 100 mils^2 chips (2.52 x 10^5 bits), consume 25.2 watts (10^{-4} watts x 2.52 x 10^5) and weigh 0.1 lbs. A system of 40 boards will contain 50,400 chips (10^7 bits), consume 1,000 watts, weigh 4 lbs. and occupy 240 in.^{3} with 1 cm. spacings between boards. This larger spacing between boards may be reduced depending on the cooling system capabilities.

2.5 Planar Thin Film

Planar magnetic thin film memories represent one of the longer established approaches to batch fabrication of storage arrays. Most previous thin film developments used a smaller array of discrete elements fabricated by a vacuum deposition process on a substrate such as glass or aluminum.(6) Each element is typically about 1,000 angstroms thick and is approximately 25 x 25 mils^2 in area. Some more recent developments use either a continuous sheet or narrow strips of thin magnetic film vacuum deposited on the substrate. The x and y drive lines are either vacuum deposited on the same substrate with appropriate insulation between them or, in some cases, the drive lines and sense lines are fabricated on separate substrates which are then mechanically superimposed over the one containing the magnetic elements. Anisotropic material is used so that there is a preferred direction (easy axis) of magnetization. In a conventional planar thin film memory, the word lines are parallel to the easy axis of magnetization, creating a field pattern in the hard direction. The digit and sense lines run parallel to the hard axis of magnetization creating a field pattern in the easy direction. A word line pulse rotates all bit positions of a word in the hard direction, but they tend to flip back when released. A relatively small digit signal pushes them into the one state or back to the zero state as desired.

The flux path is not closed; hence, the sense signal is small because the flux is only rotated rather than switched. This results in a smaller sense signal and a tendency to creep or demagnetize along the outer edges of the bit spot. To alleviate the creep problem, the film is made thinner. The thicker the film, the greater the tendency to demagnetization and creep, but on the other hand, the thinner the film, the less the sense signal. Hence a compromise must be made between the desired sense signal and minimum creep in choosing the thickness of the film.

Currently, new developments are being carried out by a Univac group. The new film, called mated-film,(22) has a closed flux path, which requires low digit current and high output signals. It is claimed that this new technique puts the mated film memories in the price range of core memories.

It seems reasonable to expect that weight, volume and power consumption with this mated film technology will be improved by a factor of two over the current thin film memories.

2.6 Plated Wire

Plated wire is a type of magnetic thin film memory semibatch-fabricated by plating a magnetic film on a wire substrate. A cylindrical magnetic film of plated wire has advantages over planar film in having a closed flux path in the digit direction, and thus lower digit currents are required and a large sense signal is obtained. Generally, there are two basic geometries which have evolved: one method utilizes arrays consisting of beryllium copper wires, coated with a relatively thick magnetic metal and orthogonally linked by solenoid windings which may be in wire or strap form; the other method consists of woven planes with the wires in one direction being plated with magnetic metal and the wires in the other direction being nonmagnetic.

A representative plated wire storage plane of the solenoid type consists of 5 mil diameter wires on 15 mil centers, each plated with a 10,000 Å layer of 81% nickel, 19% iron alloy, and mounted in an array with 10 mil wide orthogonal straps on 45 mil centers. Each strip is a word line and the center conductor of each plated wire a bit line.

In the quiescent state, a "1" would be stored circumferentially in one sense and a "0" in the opposite sense at each bit position. To read, a current in a word strap would tilt the direction of magnetization from the rest position, which is at right angles to the plated wire axis, to a new position closer to the axial orientation. The change in the component of flux linking the digit line would result in an output voltage being induced on this line. If the word read current is maintained below a critical value, destructive read switching will not occur and each bit of information will return to its original rest state at the completion of the read process.

To write, the word strap is activated by the same amplitude and polarity current pulse as for reading and the bit lines are activated by appropriate polarity current pulses to write the "1" or "0". The word drive effectively narrows the hysteresis loop of the selected word sufficiently that the

bit write currents will switch the bits of the selected word but will not switch the bits of the unselected words.

For aerospace applications, Univac has reported engineering models and feasibility studies of random[24-25] and sequential[26-29] access plated wire memories. The plated wire curves in Figures 1-4 are "best fits" for these data.

3.0 SUMMARY AND CONCLUSIONS

It seems a little presumptuous to estimate the memory systems available in 1970-1972, since a period of merely six months can bring about radical developments in memory device technology. Weight, volume, and power consumption of digital memories estimated here for 1970-1972 consider typical memory organization and speed for each memory technology and hence their curves in Figures 1-4 show only crude approximations and should be taken as such. Depending on the objectives of each memory system, the figures of actual memories may depart widely from the curves.

On the other hand, there is also a strong likelihood that these estimations will be attained and probably surpassed because of the wealth of promising technologies.

Core memories not only weigh more but also consume more power than solid-state memories over the entire 10^3-10^7 bit range, as shown in Figures 2-3. Including the weight of power supplies makes the core memories even heavier, in fact, the heaviest among all random access memories as shown in Figure 4. Hence, one can conclude that the batch-fabricated memories will probably replace core memories in random access organizations.

Tape recorders are bulkier and heavier than other sequential access memories below about 10^6 bit capacities. Even with the weight of power supplies considered, this break-even point appears about the same. Hence, one can predict that batch-fabricated sequential access memories may replace tape recorders below the 10^6 bit capacity and perhaps even above this limit due to the inherent unreliability of the moving parts of tape recorders.

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1031-BWK-fcm

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Attachments
References
Figures 1-4

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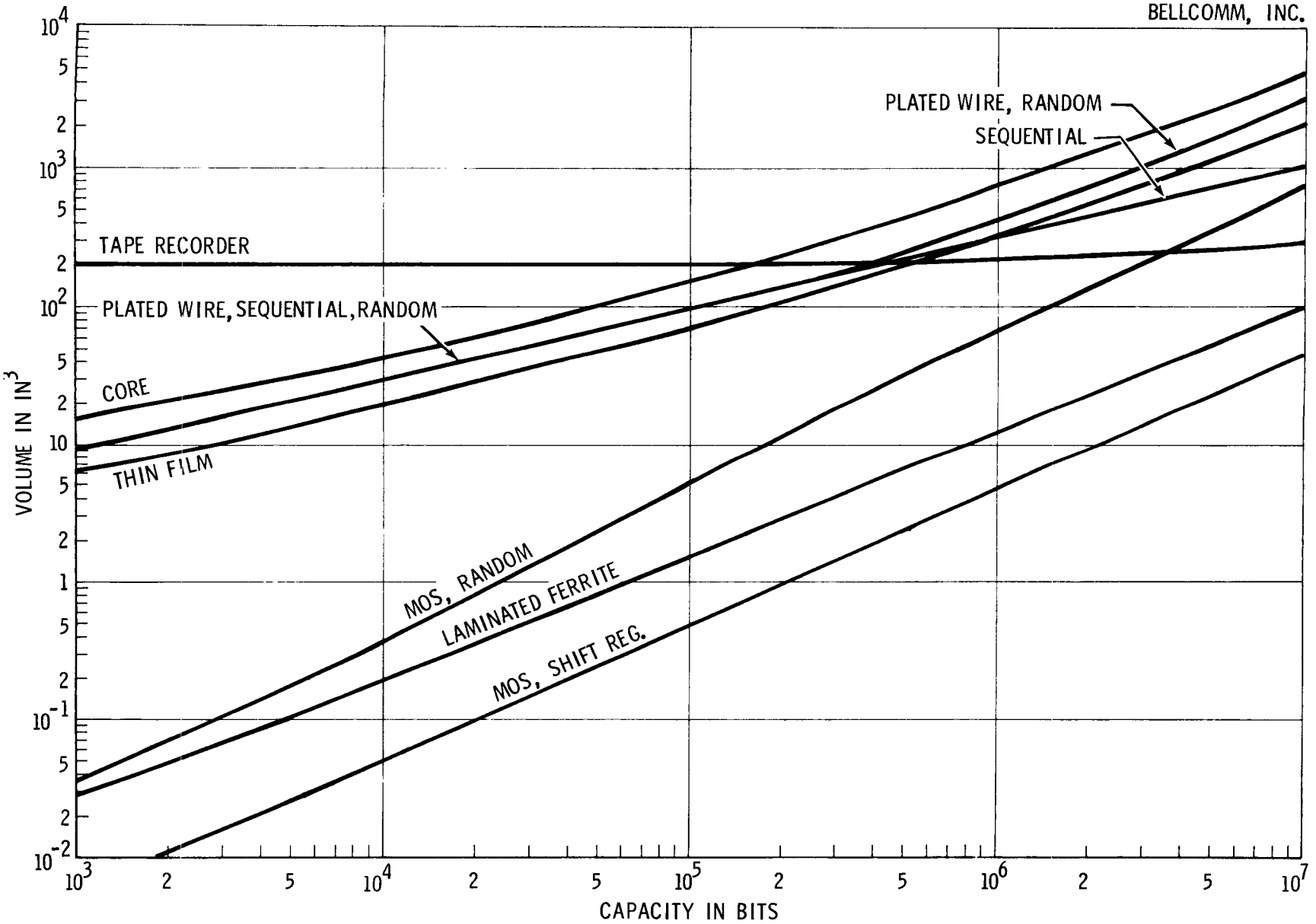

FIGURE 1 - MEMORY VOLUME vs. CAPACITY (1970 - 1972)

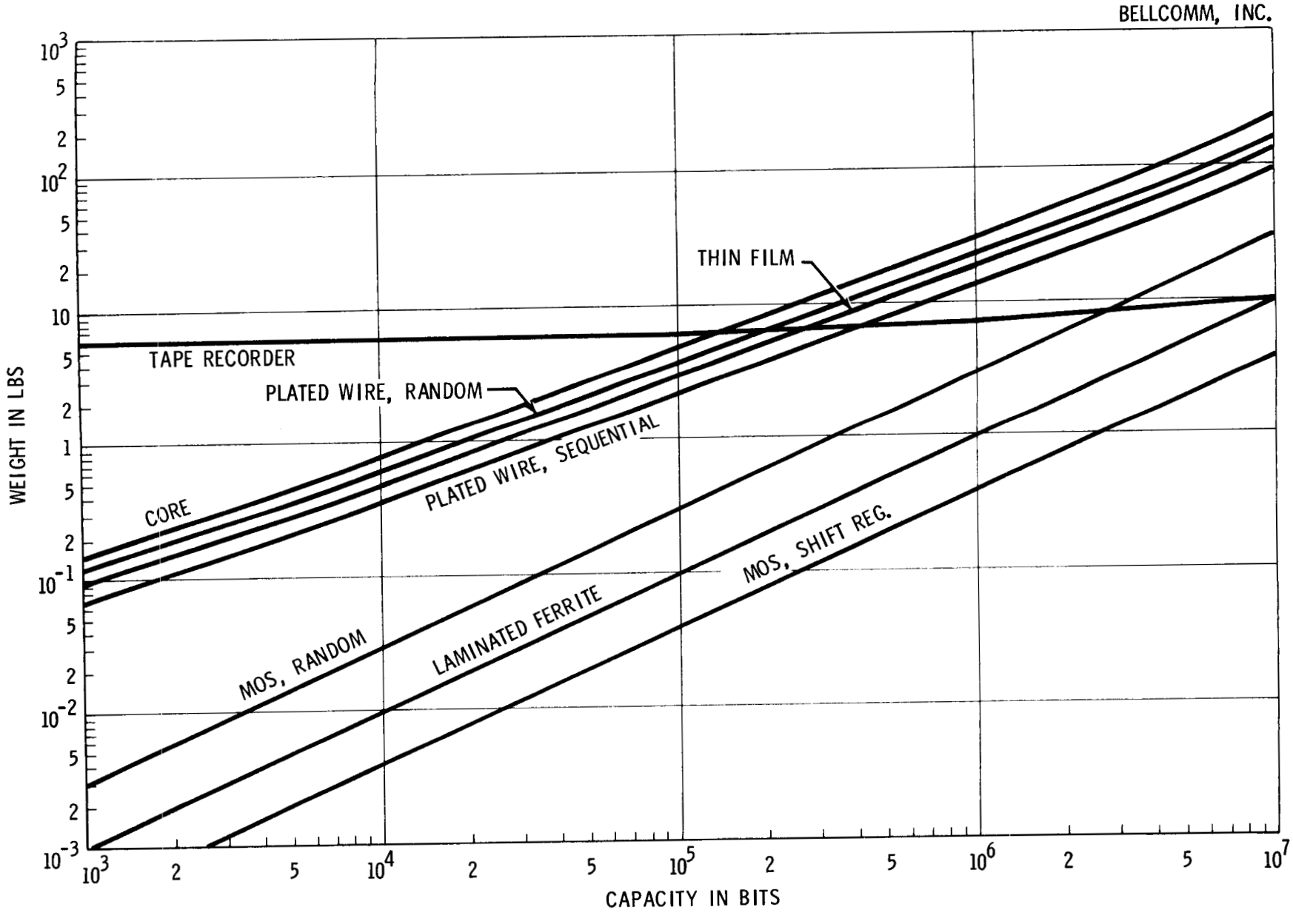

FIGURE 2 - MEMORY WEIGHT vs. CAPACITY (1970 - 1972)

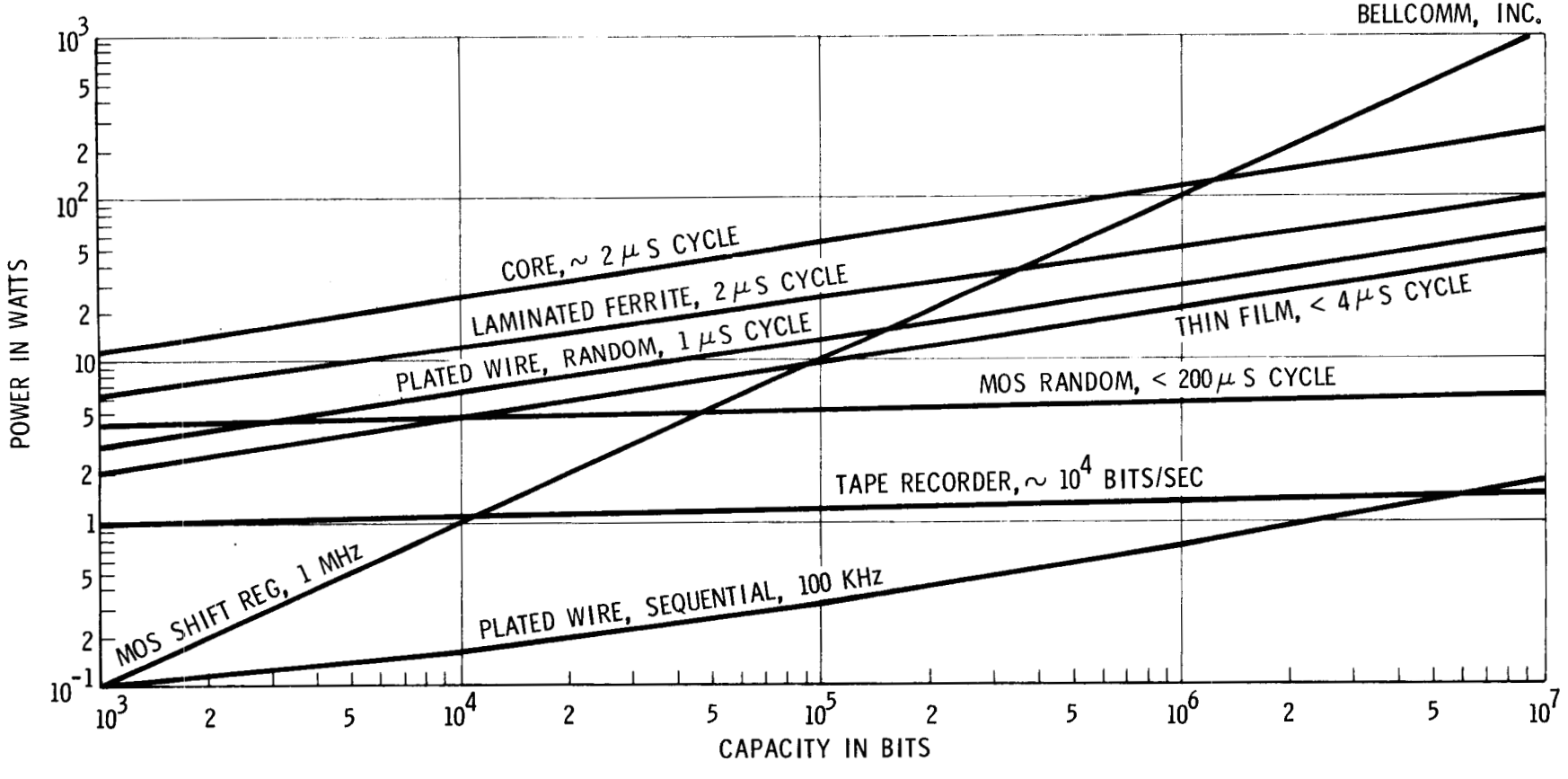

FIGURE 3 - MEMORY POWER vs. CAPACITY (1970 - 1972)

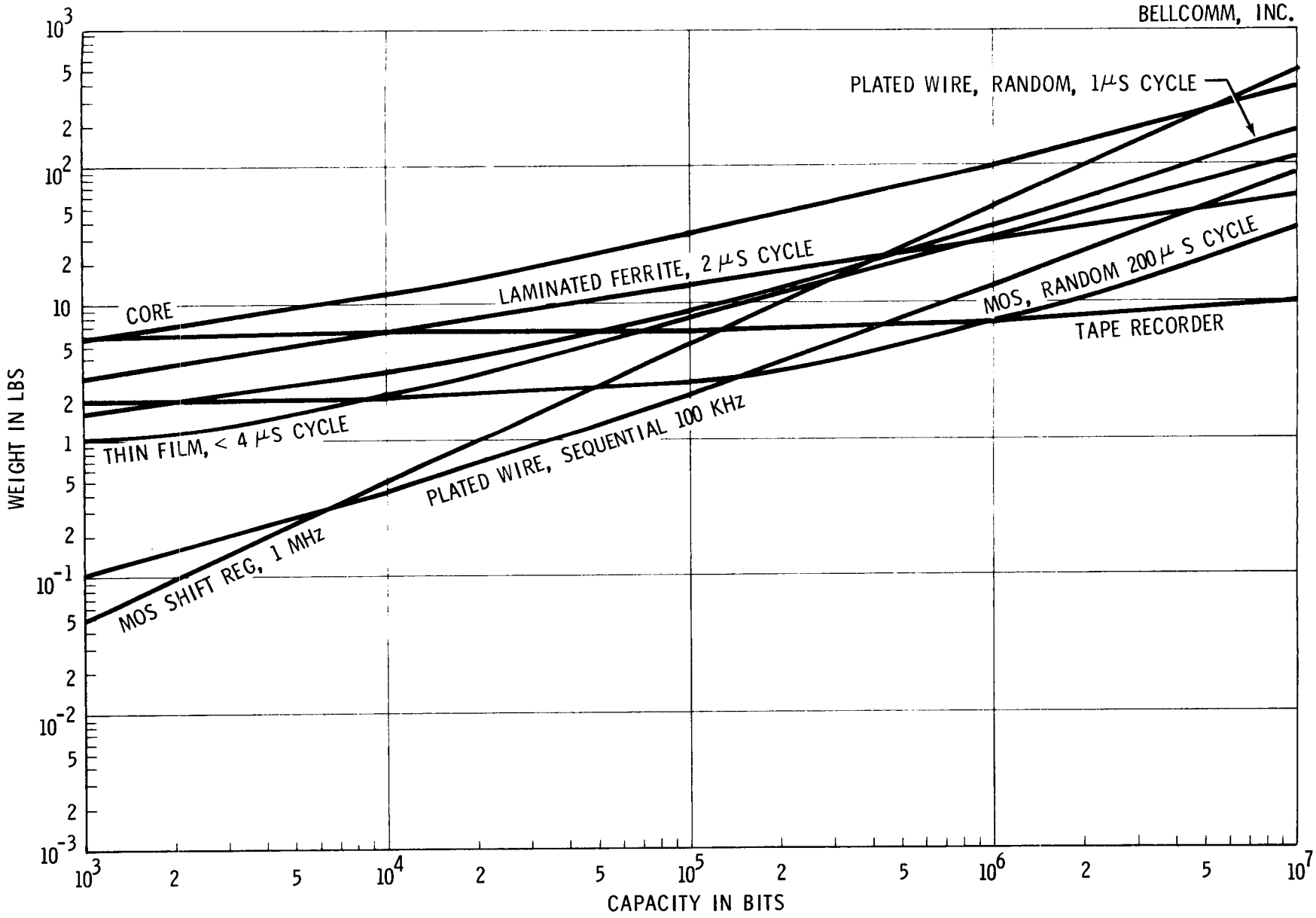

FIGURE 4 - MEMORY WEIGHT, POWER SUPPLY INCLUSIVE, vs. CAPACITY (1970 - 1972)