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# CONTENTS

3-37

| | PAGE NUMBER | ISSUE NUMBER AND DATE |
|---|---|---|
| | | 6-29-76 |
| | | 1 |
| PAGE INDEX<br>SUPPORTING INFORMATION | A1 | 1 |
| APPLICATION | B1 | 1 |
| | to | |
| | B4 | 1 |
| COMMANDS | C1 | 1 |
| | to | |
| | C32 | 1 |



## PAGE INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DOCUMENT ONLY THOSE PAGES AFFECTED WILL BE REISSUED.
2. THIS PAGE INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY PAGE OF THE DOCUMENT IS REISSUED, OR A NEW PAGE IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW PAGE WILL BE THE SAME ISSUE NUMBER AS THAT OF THE PAGE INDEX.
4. PAGES THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE PAGE INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DOCUMENT AS A WHOLE.

BELL LABORATORIES

## SUPPORTING INFORMATION

| CATEGORY | NUMBER |
|---|---|
| MAINTENANCE REFERENCE MANUAL | PK-1C900 |
| COMMON SYSTEMS<br>3A CC<br>COMMAND MANUAL | AT&TCo PROV<br>PK-1C901-01-A1<br>37 PAGES |

## 1. INTRODUCTION

1.01 THE SECTIONS OF THIS SPECIFICATION CONSTITUTE THE COMMAND MANUAL FOR THE 3ACC. ALL THE 3ACC COMMANDS ARE INCLUDED, TOGETHER WITH A DETAILED DISCRIPTION OF EACH, AND GENERAL INSTRUCTIONS FOR THEIR USE IN PROGRAMMING.

## 2. DESCRIPTION

2.01 THIS SPECIFICITION DESCRIBES ALL THE COMMANDS IN THE 3ACC INSTRUCTION SET SO THAT THE PROGRAMMER MAY SELECT THE INSTRUCTIONS BEST SUITED TO THE TASK BEING PROGRAMMED. THE MANUAL CONTAINS A DETAILED DESCRIPTION OF EACH INSTRUCTION, AND THE CONDITIONS THAT MUST BE SET UP PRIOR TO THEIR USE. THE APPROXIMATE TIME INTERVAL REQUIRED TO EXECUTE EACH COMMAND IS SUPPLIED FOR EACH.

## 4. GENERAL NOTES AND EXPLANATIONS

4.01 EACH COMMAND IS ILLUSTRATED AS IT APPEARS IN THE FULL PROGRAM STORE WORD. CERTAIN COMMANDS ARE DOUBLE WORD COMMANDS AND ARE SO DEPICTED.

4.02 IN THE ILLUSTRATION OF THE PROGRAM STORE WORD, PH AND PL STAND FOR THE PARITY HIGH AND PARITY LOW BITS RESPECTIVELY.

4.03 IN THE ILLUSTRATION OF THE PROGRAM STORE WORD, BA STANDS FOR BRANCH ALLOWED. IF A BRANCH IS MADE TO A PROGRAM STORE WORD, THAT WORD MUST HAVE THE BA BIT SET EQUAL TO ONE OR A BRANCH ERROR WILL BE GENERATED. EXTRACTION OF DATA IS NOT CONSIDERED TO BE A BRANCH.

4.04 A MICROSTORE CYCLE IS DEFINED AS 150 NSEC.

4.05 THE OPERATION CODES THAT ARE SHOWN IN THE PROGRAM STORE WORD ILLUSTRATIONS ARE IN HEXADECMIAL.

4.06 CP CODE MNEMONICS BEGINNING WITH:

| | | |
|---|---|---|
| A | INDICATES | ADD |
| B | INDICATES | BRANCH |
| C | INDICATES | COMPARE OR COMPLEMENT |
| EX | INDICATES | EXCHANGE |
| I | INDICATES | INSERT |
| I | INDICATES | LOAD |
| M | INDICATES | MAINTENANCE |
| N | INDICATES | AND |
| O | INDICATES | INCLUSIVE OR |
| PL | INDICATES | ROTATE LEFT |
| PP | INDICATES | ROTATE RIGHT |
| S | INDICATES | SET OR SUBTRACT |
| ST | INDICATES | STORE |
| T | INDICATES | TEST |
| X | INDICATES | EXCLUSIVE OR |
| Z | INDICATES | ZERO |

4.07 SYMBOLS USED IN COMMAND DESCRIPTIONS:

| | |
|---|---|
| * | AND |
| \| | OR |
| ¬ | NOT |
| WY | CONTENTS OF WORD IN MEMORY |
| CF | CONDITION FLIP-FLOP |

4.08 OPERAND SYMBOLS:

| | |
|---|---|
| Px OR Py | ANY OF THE 16 GENERAL REGISTERS (R15-R0) WITHIN THE 3ACC. SEE PAGE C1. |
| Ps | ANY OF THE 16 SPECIAL REGISTERS WITHIN THE 3ACC. SEE PAGE C11 AND TABLE BELOW. |

| | | |
|---|---|---|
| AI | ==> | ADDRESS INPUT REGISTER - ADDRESS MATCH FUNCTION |
| AK | ==> | ADDRESS MASK REGISTER - ADDRESS MATCH FUNCTION |
| DB | ==> | DISPLAY BUFFER - PANEL DISPLAY |
| DI | ==> | DATA INPUT REGISTER - DATA MATCH FUNCTION |
| DK | ==> | DATA MASK REGISTER - DATA MATCH FUNCTION |
| ER | ==> | ERROR REGISTER |
| IM | ==> | INTERRUPT MASK REGISTER |
| IS | ==> | INTERRUPT SET REGISTER (READ ONLY) |
| MCHB | ==> | MAINTENANCE CHANNEL BUFFER REGISTER |
| MCHTR | ==> | MAINTENANCE CHANNEL TRANSMIT/RECEIVE REGISTER (LOAD ONLY) |
| MMSR | ==> | MAIN MEMORY STATUS REGISTER |
| MS | ==> | MAINTENANCE STATES REGISTER |
| PA | ==> | PROGRAM ADDRESS REGISTER |
| SAR | ==> | STORE ADDRESS REGISTER |
| SS | ==> | SYSTEM STATUS REGISTER |
| TI | ==> | TIMER (READ ONLY) |

| | |
|---|---|
| PA= PA0 OR R12 | GENERAL REGISTER ADDRESS PAIR OF R12 AND R13 USED TO CONTAIN A 20-BIT ADDRESS (BITS 3-0 OF R12 AND BITS 15-0 OF R13) |
| PA= PA1 OR R14 | GENERAL REGISTER ADDRESS PAIR OF R14 AND R15 USED TO CONTAIN A 20-BIT ADDRESS (BITS 3-0 OF R14 AND BITS 15-0 OF R15) |
| B | BIT POSITION |
| I | IMMEDIATE DATA |
| M | MASK |
| N | 4-BIT NUMBER (IMMEDIATE DATA OR INDEX) |
| OFFSET | 8-BIT INDEX NUMBER |
| X | LOW 8 BITS OF AN ADDRESS |
| Y | MEMORY ADDRESS LOCATION |

DEFINITION OF ADDRESSABLE 16-BIT GENERAL PURPOSE REGISTERS

| | |
|---|---|
| 0 | REGISTER 0 |
| 1 | REGISTER 1 |
| 2 | REGISTER 2 |
| 3 | REGISTER 3 |
| 4 | REGISTER 4 |
| 5 | REGISTER 5 |
| 6 | REGISTER 6 |
| 7 | REGISTER 7 |
| 8 | REGISTER 8 |
| 9 | REGISTER 9 ALSO USED FOR INPUT/OUTPUT |
| 10 | REGISTER 10 ALSO USED FOR INPUT/OUTPUT |
| 11 | REGISTER 11 ALSO USED FOR INPUT/OUTPUT |
| 12 | REGISTER 12 ALSO USED FOR MEMORY ADDRESSING |
| 13 | REGISTER 13 ALSO USED FOR MEMORY ADDRESSING |
| 14 | REGISTER 14 ALSO USED FOR MEMORY ADDRESSING |
| 15 | REGISTER 15 ALSO USED FOR MEMORY ADDRESSING |

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

LL Rx,Y LOAD Rx WITH THE CONTENTS OF MEMORY AT LOCATION Y

| PH | PL | BA | OP CODE 31 | Rx | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y | | | |

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. LOAD Rx WITH THE CONTENTS OF MEMORY AT LOCATION Y.
2. MEMORY AT LOCATION Y IS UNCHANGED.

APPROXIMATE EXECUTION TIME 3.75 MICROSECONDS

LAL Px,Y,PA  LOAD Px WITH THE CONTENTS OF MEMORY AT LOCATION Y AND SET PA TO Y

| PH | PL | BA | OP CODES 32/33 | Px | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y | | | |

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. LOAD Px WITH THE CONTENTS OF MEMORY AT LOCATION Y AND SET PA TO Y.

2. Px SHOULD NOT BE EQUAL TO EITHER MEMBER OF THE PA REGISTER PAIR.

3. MEMORY AT LOCATION Y IS UNCHANGED.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF PA. IT IS 0 FOR PA=12 AND 1 FOR PA=14.
BITS(15-4) OF GENERAL REGISTER 12/14 ARE NOT CHANGED BY THIS INSTRUCTION.
SEE NOTE CONCERNING PA ON PAGE B2.

APPROXIMATE EXECUTION TIME 3.90 MICROSECONDS

L Rx,N(PA)  LOAD Rx WITH THE CONTENTS OF MEMORY AT LOCATION PA INDEXED BY N

| PH | PL | BA | OP CODES 40/41 | Rx | N |
|---|---|---|---|---|---|

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. LOAD Px WITH THE CONTENTS OF MEMORY AT LOCATION DETERMINED BY ADDING N TO RA.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
SEE NOTE CONCERNING PA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.55 MICROSECONDS

LA Rx,N(RA)  LOAD Rx FROM MEMORY AT LOCATION RA INDEXED BY N AND UPDATE RA

| PH | PL | BA | OP CODES 42/43 | Rx | N |
|---|---|---|---|---|---|

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. LOAD Rx WITH THE CONTENTS OF MEMORY AT LOCATION DETERMINED BY ADDING N TO RA AND UPDATE RA.

2. Rx SHOULD NOT BE EQUAL TO EITHER MEMBER OF THE RA REGISTER PAIR.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
BITS(15-4) OF GENERAL REGISTER 12/14 ARE NOT CHANGED BY THIS INSTRUCTION.
SEE NOTE CONCERNING PA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.55 MICROSECONDS

LX Rx,Ry(RA)  LOAD Rx WITH THE CONTENTS OF MEMORY AT LOCATION RA INDEXED BY Ry

| PH | PL | BA | OP CODES 44/45 | Px | Ry |
|---|---|---|---|---|---|

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. LOAD Rx WITH THE CONTENTS OF MEMORY AT LOCATION DETERMINED BY ADDING Ry TO RA.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.55 MICROSECONDS

LAX Rx,Ry(PA)  LOAD Px FROM MEMORY AT LOCATION RA INDEXED BY Ry AND UPDATE RA

| PH | PL | BA | OP CODES 46/47 | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. LOAD Px WITH THE CONTENTS OF MEMORY AT LOCATION DETERMINED BY ADDING Ry TO RA AND UPDATE RA.

2. Rx SHOULD NOT BE EQUAL TO EITHER MEMBER OF THE RA REGISTER PAIR.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
BITS(15-4) OF GENERAL REGISTER 12/14 ARE NOT CHANGED BY THIS INSTRUCTION.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.55 MICROSECONDS

LI Rx,I  LOAD Rx WITH 16 BITS OF IMMEDIATE DATA, I

| PH | PL | BA | OP CODE 07 | Rx | 1 |
|---|---|---|---|---|---|
| PH | PL | | | I | |
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. LOAD Rx WITH I.

APPROXIMATE EXECUTION TIME 2.40 MICROSECONDS

LN Rx,N  LOAD Rx WITH 4 BITS OF IMMEMEDIATE DATA, N

| PH | PL | BA | OP CODE 06 | Rx | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. ZERO BITS(15-4) OF Px.

2. LOAD Rx BITS(3-0) WITH N.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

REGISTER TO MEMORY OPERATIONS

STL Rx,Y  STORE RI IN MEMORY AT LOCATION Y

| PH | PL | BA | OP CODE 39 | Rx | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y | | | |

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. STORE Rx IN MEMORY AT LOCATION Y.

2. Rx IS UNCHANGED.

APPROXIMATE EXECUTION TIME 3.75 MICROSECONDS

STAL Rx,Y,RA  STORE Rx IN MEMORY AT LOCATION Y AND SET RA TO Y

| PH | PL | BA | OP CODES 3A/3B | Rx | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y | | | |

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. STORE Rx IN MEMORY AT LOCATION Y AND SET RA TO Y.

2. Rx SHOULD NOT BE EQUAL TO EITHER MEMBER OF THE RA REGISTER PAIR.

3. Rx IS UNCHANGED.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
BITS(15-4) OF GENERAL REGISTER 12/14 ARE NOT CHANGED BY THIS INSTRUCTION.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 4.05 MICROSECONDS

ST Rx,N(RA)  STORE Rx IN MEMORY AT LOCATION RA INDEXED BY N

| PH | PL | BA | OP CODES 48/49 | Rx | N |
|---|---|---|---|---|---|

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. STORE Rx AT LOCATION DETERMINED BY ADDING N TO RA.

2. Rx IS UNCHANGED.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.70 MICROSECONDS

STA Rx,N(RA)  STORE Rx IN MEMORY AT LOCATION RA INDEXED BY N AND UPDATE RA

| PH | PL | BA | OP CODES 4A/4B | Rx | N |
|---|---|---|---|---|---|

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. STORE Rx AT LOCATION DETERMINED BY ADDING N TO RA AND UPDATE RA.

2. Rx SHOULD NOT BE EQUAL TO EITHER MEMBER OF THE RA REGISTER PAIR.

3. Rx IS UNCHANGED.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
BITS(15-4) OF GENERAL REGISTER 12/14 ARE NOT CHANGED BY THIS INSTRUCTION.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.70 MICROSECONDS

STX Rx,Ry(RA)  STORE Rx IN MEMORY AT LOCATION RA INDEXED BY Ry

| PH | PL | RA | OP CODES 4C/4D | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. STORE Rx AT LOCATION DETERMINED BY ADDING Ry TO RA.

2. Rx IS UNCHANGED.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.70 MICROSECONDS

STAX Rx,Ry(RA)  STORE Rx IN MEMORY AT LOCATION RA INDEXED BY Ry AND UPDATE RA

| PH | PL | BA | OP CODES 4E/4F | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. STORE Rx AT LOCATION DETERMINED BY ADDING Ry TO RA.

2. Rx SHOULD NOT BE EQUAL TO EITHER MEMBER OF THE RA REGISTER PAIR.

3. Rx IS UNCHANGED.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
BITS(15-8) OF GENERAL REGISTER 12/14 ARE NOT CHANGED BY THIS INSTRUCTION.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.70 MICROSECONDS

STAF N(PA)  STORE ACCESS FUNCTION USING REGISTER 0 AT LOCATION RA INDEXED BY N

| PH | PL | BA | OP CODE 7C | 0/1 | N |
|---|---|---|---|---|---|
| PH | PL | BEC0 | CW0 | BDSR1 | BDSR0 | ISO1 | ISO0 | UPD1 | UPD0 | IDL1 | IDL0 | RW1 | RW0 | MM21 | MM20 | MM11 | MM10 |
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. COMPUTE THE EFFECTIVE ADDRESS FOR THIS INSTRUCTION BY ADDING N TO PA.

2. SAVE THE CONTENTS OF THE MAIN MEMORY STATUS REGISTER.

3. LOAD THE MAIN MEMORY STATUS REGISTER FROM THE SECOND WORD OF THIS INSTRUCTION.
THE ISOLATE BITS ARE LEFT AS THEY WERE ON ENTRY.

4. PERFORM THE INDICATED READ/WRITE OPERATION USING REGISTER 0 AS DESTINATION/SOURCE FOR THE DATA.

5. PARITY IS CORRECTED ON THE DATA RECEIVED FROM THE STORE BEFORE IT IS PLACED IN REGISTER 0.

6. ZERO THE CF.

7. IF A STORE ERROR C OCCURS:
A. THE CF IS SET EQUAL TO ONE.
B. THE ER IS CLEARED.

8. RESTORE THE PREVIOUSLY SAVED CONTENTS OF THE MAIN MEMORY STATUS REGISTER.

9. THIS INSTRUCTION KEEPS AN INTERNAL TIMER TO PREVENT THE CC FROM HANGING.
IF THE INSTRUCTION TIMES OUT, REGISTER 0 IS SET TO ALL ONES.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY SYSTEM MACROS.
REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

NOTE: BIT 4 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 9.45 MICROSECONDS.

STAFX Rx(PA)  STORE ACCESS FUNCTION USING REGISTER 0 AT LOCATION PA INDEXED BY Rx

| PH | PL | BA | OP CODE 7C | 2/3 | Rx |
|---|---|---|---|---|---|

| PH | PL | BEC0 | CW0 | BDSR1 | BDSF0 | ISO1 | ISO0 | UPD1 | UPD0 | IDL1 | IDL0 | RW1 | RW0 | MM21 | MM20 | MM11 | MM10 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. COMPUTE THE EFFECTIVE ADDRESS FOR THIS INSTRUCTION BY ADDING Rx TO RA.

2. SAVE THE CONTENTS OF THE MAIN MEMORY STATUS REGISTER.

3. LOAD THE MAIN MEMORY STATUS REGISTER FROM THE SECOND WORD OF THIS INSTRUCTION.
   THE ISOLATE BITS ARE LEFT AS THEY WERE ON ENTRY.

4. PERFORM THE INDICATED READ/WRITE OPERATION USING REGISTER 0 AS DESTINATION/SOURCE FOR THE DATA.

5. PARITY IS CORRECTED ON THE DATA RECEIVED FROM THE STORE BEFORE IT IS PLACED IN REGISTER 0.

6. ZERO THE CF.

7. IF A STORE ERROR C OCCURS:
   A. THE CF IS SET EQUAL TO ONE.
   B. THE ER IS CLEARED.

8. RESTORE THE PREVIOUSLY SAVED CONTENTS OF THE MAIN MEMORY STATUS REGISTER.

9. THIS INSTRUCTION KEEPS AN INTERNAL TIMER TO PREVENT THE CC FROM HANGING.
   IF THE INSTRUCTION TIMES OUT,REGISTER 0 IS SET TO ALL ONES.

   NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY,IT WILL BE SUPPLIED BY SYSTEM MACROS.
   REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.
   NOTE: BIT 4 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
   SEE NOTE CONCERNING RA ON PAGE B2.

   APPROXIMATE EXECUTION TIME 9.30 MICROSECONDS.

STM Rx,N(PA),M  INSERT Rx UNDER MASK INTO MEMORY AT LOCATION RA INDEXED BY N

| PH | PL | BA | OP CODES 04/05 | Rx | N |
|---|---|---|---|---|---|

| PH | PL | MASK |
|---|---|---|

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. ADD N TO PA TO DETERMINE LOCATION OF WORD WY.

2. LOAD GENERAL REGISTER 0 WITH THE CONTENTS OF WORD WY.

3. (WY • ¬MASK) | (Rx • MASK) ==> WY

   NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
   SEE NOTE CONCERNING PA ON PAGE B2.

   APPROXIMATE EXECUTION TIME 5.40 MICROSECONDS

STVM Rx,N(PA)  INSERT Rx UNDER VARIABLE MASK INTO MEMORY AT LOCATION RA INDEXED BY N

| PH | PL | BA | OP CODES 66/67 | Rx | N |
|---|---|---|---|---|---|

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. OBTAIN MASK FROM THE CONTENTS OF REGISTER 0.

2. ADD N TO PA TO DETERMINE LOCATION OF WORD WY.

3. LOAD GENERAL REGISTER 0 WITH THE CONTENTS OF WORD WY.

4. (WY • ¬MASK) | (Rx • MASK) ==> WY

   NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
   SEE NOTE CONCERNING PA ON PAGE B2.

   APPROXIMATE EXECUTION TIME 5.55 MICROSECONDS

LAYOUT OF 16 WORD HOLD-GET AREA

| PH | PL | OP | WORDS 0 AND 1 ARE RESERVED FOR RETURN ADDRESS | BITS (19-16) OF RA |
|---|---|---|---|---|
| PH | PL | | BITS(15-0) OF RETURN ADDRESS | |
| PH | PL | | WORD 2 RESERVED FOR REGISTER 2 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 3 RESERVED FOR REGISTER 3 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 4 RESERVED FOR REGISTER 4 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 5 RESERVED FOR REGISTER 5 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 6 RESERVED FOR REGISTER 6 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 7 RESERVED FOR REGISTER 7 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 8 RESERVED FOR REGISTER 8 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 9 RESERVED FOR REGISTER 9 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 10 RESERVED FOR REGISTER 10 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 11 RESERVED FOR REGISTER 11 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 12 RESERVED FOR REGISTER 12 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 13 RESERVED FOR REGISTER 13 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 14 RESERVED FOR REGISTER 14 WHEN HELD BY HOLD ALL INSTRUCTION | |
| PH | PL | | WORD 15 RESERVED FOR REGISTER 15 WHEN HELD BY HOLD ALL INSTRUCTION | |

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

NOTE: WORDS 0 AND 1 ARE HELD BY BSA INSTRUCTIONS AND INTERRUPTS.

HA HOLD REGISTERS 2 THROUGH 15 IN WORDS 2 THROUGH 15 OF HOLD-GET AREA

| PH | PL | BA | OP CODE 73 | 1 | 0 |
|---|---|---|---|---|---|

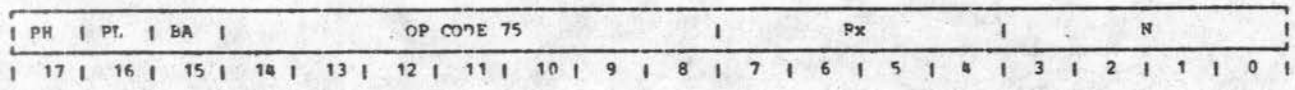
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1. STORE EACH REGISTER IN ITS ASSOCIATED WORD OF THE HOLD-GET AREA.
2. REGISTERS STORED ARE UNCHANGED.

   NOTE: WORDS 0 AND 1 OF THE HOLD-GET AREA ARE RESERVED FOR RETURN ADDRESS.

   APPROXIMATE EXECUTION TIME 28.55 MICROSECONDS

HN Px,N HOLD Px IN WORD N OF HOLD-GET AREA

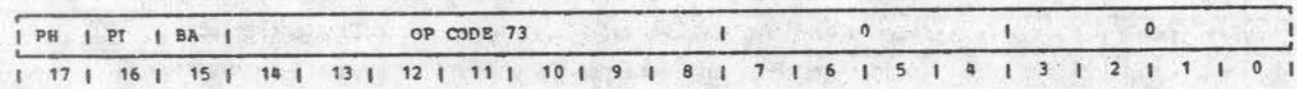



1. STORE Px IN WORD N OF HOLD-GET AREA.

2. Px IS UNCHANGED.

APPROXIMATE EXECUTION TIME 2.70 MICROSECONDS

GA GET REGISTERS 2 THROUGH 15 FROM WORDS 2 THROUGH 15 OF HOLD-GET AREA

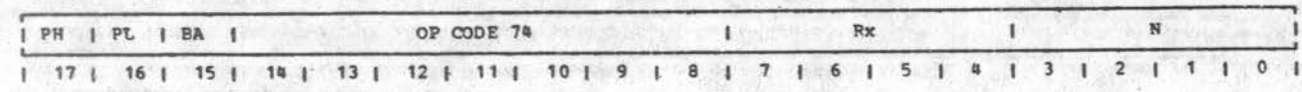



1. LOAD EACH REGISTER FROM THE ASSOCIATED WORD OF THE HOLD-GET AREA.

NOTE: WORDS 0 AND 1 OF THE HOLD-GET AREA ARE RESERVED FOR RETURN ADDRESS.

APPROXIMATE EXECUTION TIME 26.55 MICROSECONDS

GN Px,N GET Px FROM WORD N OF HOLD-GET AREA



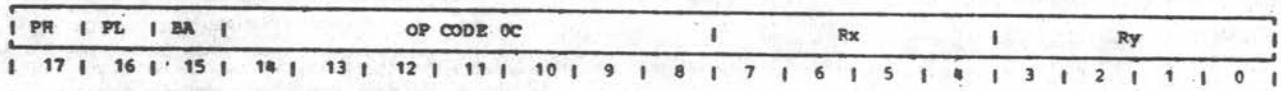

1. LOAD Rx FROM WORD N OF HOLD-GET AREA.

2. WORD N IS UNCHANGED.

APPROXIMATE EXECUTION TIME 2.55 MICROSECONDS

REGISTER TO REGISTER OPERATIONS

LR Rx,Ry  LOAD Rx WITH THE CONTENTS OF Ry

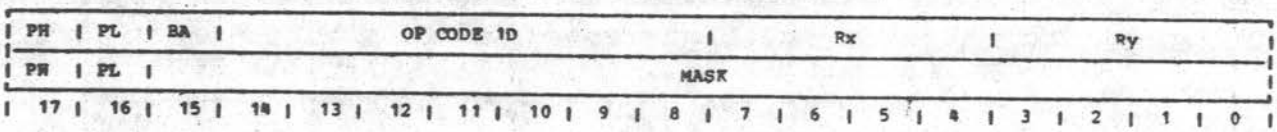



1. LOAD Rx WITH THE CONTENTS OF Ry.

2. Ry IS UNCHANGED.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

LRM Rx,Ry,M  LOAD Rx WITH THE CONTENTS OF Ry UNDER IMMEDIATE MASK, M

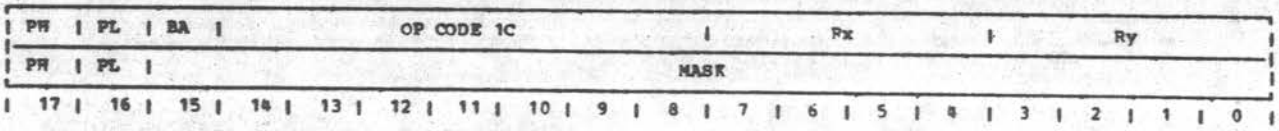



1. Ry • MASK ==> Rx

2. Ry IS UNCHANGED.

APPROXIMATE EXECUTION TIME 2.40 MICROSECONDS

IRM Rx,Ry,M  INSERT Ry INTO Rx UNDER IMMEDIATE MASK, M

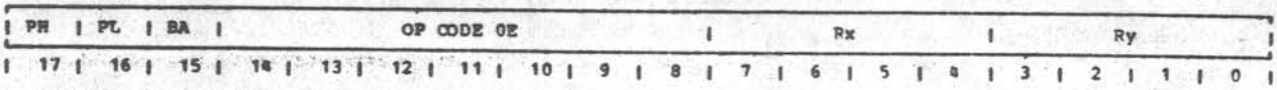



1. (Ry • MASK) | (Rx • ¬MASK) ==> Rx.

2. Ry IS UNCHANGED.

APPROXIMATE EXECUTION TIME 2.40 MICROSECONDS

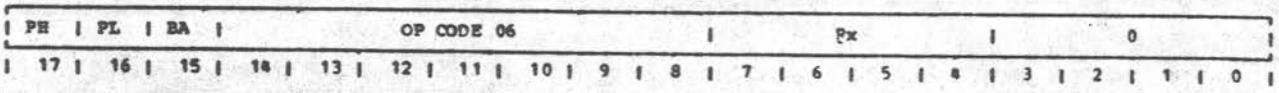
EXR Rx,Ry  EXCHANGE THE CONTENTS OF Rx WITH THE CONTENTS OF Ry




1. EXCHANGE THE CONTENTS OF Rx WITH THE CONTENTS OF Ry.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

ZP Rx  ZERO Rx




1. ZERO REGISTER Rx. THE CF IS UNCHANGED.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

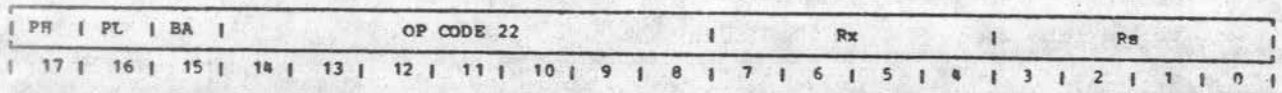
SPECIAL REGISTER OPERATIONS

THE FOLLOWING TABLE DEFINES THOSE REGISTERS WHICH ARE ACCESSED WITH THE SPECIAL REGISTER INSTRUCTIONS

| Rs | TO FIELD FUNCTION | FROM FIELD FUNCTION |
|---|---|---|
| 0 | GB ==> MCHTP 22 BIT PATH | TI ==> GB 18 BIT PATH PL=0,PH=0 |
| 1 | GB ==> SAP 22 BIT PATH | SAR ==> GB 22 BIT PATH |
| 2 | GB ==> PA 22 BIT PATH | PA ==> GB 22 BIT PATH |
| 3 | GB ==> MCHB 22 BIT PATH | MCHB ==> GB 22 BIT PATH |
| 4 | UNASSIGNED | MMSP ==> GB 20 BIT PATH PL=0,PH=1 |
| 5 | GB ==> AK 22 BIT PATH | AK ==> GB 22 BIT PATH |
| 6 | GB ==> AI 22 BIT PATH | AI ==> GB 22 BIT PATH |
| 7 | GB ==> DK 18 BIT PATH | DK ==> GB 18 BIT PATH |
| 8 | GB ==> DI 18 BIT PATH | DI ==> GB 18 BIT PATH |
| 9 | GB ==> DB 22 BIT PATH | DB ==> GB 22 BIT PATH |
| 10 | GB ==> ER 22 BIT PATH | ER ==> GB 22 BIT PATH |
| 11 | GB ==> DB 22 BIT PATH IF DISPLAY BIT IN SS IS 1 | UNASSIGNED |
| 12 | GB ==> IM 18 BIT PATH | IM ==> GB 18 BIT PATH |
| 13 | GB ==> SS_S A 1 SETS SS | IS ==> GB 18 BIT PATH |
| 14 | GB ==> MS 18 BIT PATH | MS ==> GB 18 BIT PATH |
| 15 | GB ==> SS_R A 1 RESETS SS | SS ==> GB 22 BIT PATH PL=-CC,PH=CC |

NOTE: THE 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-7&292 SHOULD BE CAREFULLY STUDIED BEFORE USING ANY OF THE SPECIAL INSTRUCTIONS.

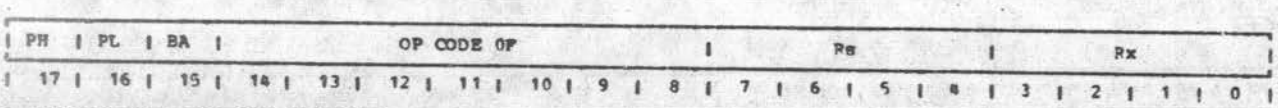
LRS Rx,Rs LOAD Rx WITH THE CONTENTS OF Rs




1. LOAD Rx WITH THE CONTENTS OF Rs
   WHERE Rx IS ONE OF THE GENERAL PURPOSE REGISTERS
   AND Rs IS ONE OF THE 16 BIT SPECIAL REGISTERS

   APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

LSR Rs,Rx LOAD Rs WITH THE CONTENTS OF Rx




1. LOAD Rs WITH THE CONTENTS OF Rx
   WHERE Rx IS ONE OF THE GENERAL PURPOSE REGISTERS
   AND Rs IS ONE OF THE 16 BIT SPECIAL REGISTERS

   APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

PACK Rs  PACKS GENERAL REGISTERS 2 AND 3 INTO 20 BIT SPECIAL REGISTER Rs

| PH | PL | BA | OP CODE 14 | Rs | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. GENERAL REGISTER 2 BITS(3-0) ==> Rs BITS(19-16)
2. GENERAL REGISTER 3 BITS(15-0) ==> Rs BITS(15-0)

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

UNPF Rs  UNPACKS 20 BIT SPECIAL REGISTER Rs TO GENERAL REGISTERS 2 AND 3

| PH | PL | BA | OP CODE 15 | 0 | Rs |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. Rs(19-16) ==> GENERAL REGISTER 2 BITS(3-0)
2. Rs(15-0) ==> GENERAL REGISTER 3 BITS(15-0)
3. GENERAL REGISTER 2 BITS(15-4) ARE SET TO ZERO BY THIS INSTRUCTION.

NOTE: IT IS NOT NECESSARY TO SUPPRESS THE GATING BUS PARITY CHECK WHEN USING THIS INSTRUCTION ON A SPECIAL REGISTER THAT MAY NOT HAVE CORRECT PARITY.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

BRANCH OPERATIONS

B Y  BRANCH TO LOCATION Y

| PH | PL | BA | CP CODES 56/57 | OFFSET |
|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0 |

1. BRANCH TO LOCATION Y WHICH IS DETERMINED BY ADDING OFFSET TO THE PA.

   NOTE: BIT 8 IS DETERMINED BY THE SIGN OF THE OFFSET. IT IS 0 FOR POSITIVE OFFSET AND 1 FOR NEGATIVE OFFSET.

   APPROXIMATE EXECUTION TIME 1.80 MICROSECONDS

BR N(PA)  BRANCH TO LOCATION PA INDEXED BY N

| PH | PL | BA | OP CODE 55 | 0/1 | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0 | |

1. BRANCH TO LOCATION Y WHICH IS DETERMINED BY ADDING N TO PA.
2. THIS INSTRUCTION IS ONLY CAPABLE OF FORWARD BRANCHES.

   NOTE: BIT 4 IS DETERMINED BY THE VALUE OF PA. IT IS 0 FOR PA=12 AND 1 FOR PA=14.
   SEE NOTE CONCERNING PA ON PAGE B2.

   APPROXIMATE EXECUTION TIME 2.70 MICROSECONDS

BL Y  BRANCH LONG TO LOCATION Y

| PH | PL | BA | OP CODE 3E | 0 | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y | | | |
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0 | |

1. BRANCH TO LOCATION Y.

   APPROXIMATE EXECUTION TIME 2.70 MICROSECONDS

BC Y  BRANCH ON CONDITION TO LOCATION Y

| PH | PL | BA | CP CODES 58/59 | OFFSET |
|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0 |

1. IF THE CF IS EQUAL TO:
   A. ZERO, DO NOT BRANCH AND EXECUTE THE NEXT SEQUENTIAL INSTRUCTION.
   B. ONE, BRANCH TO LOCATION Y WHICH IS DETERMINED BY ADDING OFFSET TO THE PA.

   NOTE: BIT 8 IS DETERMINED BY THE SIGN OF THE OFFSET. IT IS 0 FOR POSITIVE OFFSET AND 1 FOR NEGATIVE OFFSET.

   APPROXIMATE EXECUTION TIME 1.95 MICROSECONDS FOR CF=1 AND 1.50 MICROSECONDS FOR CF=0

BNC Y BRANCH ON NOT CONDITION TO LOCATION Y

| PH | PL | BA | OP CODES 5A/5B | OFFSET |
|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 4 3 2 1 0 |

1. IF THE CF IS EQUAL TO:
   A. ZERO, BRANCH TO LOCATION Y WHICH IS DETERMINED BY ADDING OFFSET TO THE PA.
   B. ONE, DO NOT BRANCH AND EXECUTE THE NEXT SEQUENTIAL INSTRUCTION.

   NOTE: BIT 8 IS DETERMINED BY THE SIGN OF THE OFFSET. IT IS 0 FOR POSITIVE OFFSET AND 1 FOR NEGATIVE OFFSET.

   APPROXIMATE EXECUTION TIME 1.50 MICROSECONDS FOR CF=1 AND 1.95 MICROSECONDS FOR CF=0

BCL Y BRANCH LONG ON CONDITION TO LOCATION Y

| PH | PL | BA | OP CODE 50 | 0 | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y | | | |
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 4 3 2 1 0 | |

1. IF THE CF IS EQUAL TO:
   A. ZERO, DO NOT BRANCH AND EXECUTE NEXT SEQUENTIAL INSTRUCTION.
   B. ONE, BRANCH TO LOCATION Y.

   APPROXIMATE EXECUTION TIME 2.70 MICROSECONDS FOR CF=1 AND 1.80 MICROSECONDS FOR CF=0

BNCL Y BRANCH LONG ON NOT CONDITION TO LOCATION Y

| PH | PL | BA | OP CODE 51 | 0 | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y | | | |
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 4 3 2 1 0 | |

1. IF THE CF IS EQUAL TO:
   A. ZERO, BRANCH TO LOCATION Y.
   B. ONE, DO NOT BRANCH AND EXECUTE THE NEXT SEQUENTIAL INSTRUCTION.

   APPROXIMATE EXECUTION TIME 1.80 MICROSECONDS FOR CF=1 AND 2.70 MICROSECONDS FOR CF=0

BX Rx,Y BRANCH ON INDEX NOT ZERO TO LOCATION Y

| PH | PL | BA | OP CODE 3C | Rx | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y | | | |
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 4 3 2 1 0 | |

1. IF THE CONTENTS OF Rx IS NOT EQUAL TO ZERO, DECREMENT Rx BY 1 AND BRANCH TO LOCATION Y.

2. IF THE CONTENTS OF Rx IS EQUAL TO ZERO, EXECUTE THE NEXT SEQUENTIAL INSTRUCTION.

   APPROXIMATE EXECUTION TIME 2.55 MICROSECONDS FOR Rx=0 AND 2.70 MICROSECONDS FOR Rx¬=0

BPX Px(PA)  BRANCH TO LOCATION PA INDEXED BY Rx

| PH | PL | BA | OP CODE 55 | 2/3 | Rx |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. BRANCH TO LOCATION Y, WHICH IS DETERMINED BY ADDING THE CONTENTS OF Rx TO PA.

2. THIS INSTRUCTION IS ONLY CAPABLE OF FORWARD INDEXING.

NOTE: BIT 4 IS DETERMINED BY THE VALUE OF PA. IT IS 0 FOR PA=12 AND 1 FOR PA=14.
SEE NOTE CONCERNING PA ON PAGE B2.

APPROXIMATE EXECUTION TIME 2.55 MICROSECONDS

BPAX Rx  BRANCH TO LOCATION PA INDEXED BY Rx

| PH | PL | BA | OP CODE 5C | 0 | Rx |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. BRANCH TO LOCATION Y, WHICH IS DETERMINED BY ADDING THE CONTENTS OF Rx TO PA+1 (PROGRAM ADDRESS REGISTER +1.)
2. THIS INSTRUCTION IS ONLY CAPABLE OF FORWARD INDEXING.

APPROXIMATE EXECUTION TIME 1.65 MICROSECONDS

BSA Y  BRANCH TO LOCATION Y AND SAVE ADDRESS

| PH | PL | BA | OP CODE 3F | 1 | BITS(19-16) OF Y |
|---|---|---|---|---|---|
| PH | PL | BITS(15-0) OF Y |
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. DECREMENT THE HOLD-GET COUNTER BY 16 AND STORE THE RETURN ADDRESS IN WORDS 0 AND 1 OF THE HOLD-GET AREA. BITS 4-15 OF HOLD-GET AREA WORD 0 ARE ZEROED.

2. TRANSFER TO LOCATION Y.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY A SYSTEM MACRO.
REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

APPROXIMATE EXECUTION TIME 6.15 MICROSECONDS

BSAI X  BRANCH AND SAVE ADDRESS INDIRECT

| PH | PL | BA | OP CODE 76 | X |
|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. DECREMENT THE HOLD-GET COUNTER BY 16 AND STORE THE RETURN ADDRESS IN WORDS 0 AND 1 OF THE HOLD-GET AREA. BITS 4-15 OF HOLD-GET AREA WORD 0 ARE ZEROED.

2. BRANCH TO LOCATION X+2.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY A SYSTEM MACRO.
REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

APPROXIMATE EXECUTION TIME 5.70 MICROSECONDS

BTSA BRANCH TO SAVED ADDRESS

| PH | PL | BA | OP CODE 5D | 0 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. SET THE CF EQUAL TO:
   A. ONE, IF REGISTER 0 IS ZERO.
   B. ZERO, IF REGISTER 0 IS NONZERO.

2. SET THE OP CODE FIL BIT EQUAL TO BIT 15 IN WORD 0 OF THE HOLD-GET AREA.

3. BRANCH TO THE RETURN ADDRESS WHICH IS STORED IN WORDS 0 AND 1 OF THE HOLD-GET AREA.

4. ADD 16 TO THE HOLD-GET COUNTER.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY A SYSTEM MACRO. REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

APPROXIMATE EXECUTION TIME 4.95 MICROSECONDS

BTSAN N LOAD RETURN CODE AND BRANCH TO SAVED ADDRESS

| PH | PL | BA | OP CODE 5D | 3 | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. LOAD THE RETURN CODE N INTO BITS (3-0) OF REGISTER 0.
   BITS (15-4) OF REGISTER 0 ARE SET TO ZERO BY THIS INSTRUCTION.

2. SET THE CF EQUAL TO:
   A. ONE, IF REGISTER 0 IS ZERO.
   B. ZERO, IF REGISTER 0 IS NONZERO.

3. SET THE OP CODE FIL BIT EQUAL TO BIT 15 IN WORD 0 OF THE HOLD-GET AREA.

4. BRANCH TO THE RETURN ADDRESS WHICH IS STORED IN WORDS 0 AND 1 OF THE HOLD-GET AREA.

5. ADD 16 TO THE HOLD-GET COUNTER.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY A SYSTEM MACRO. REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

APPROXIMATE EXECUTION TIME 5.10 MICROSECONDS

BTSAG GET REGISTERS 2 THROUGH 15 AND BRANCH TO SAVED ADDRESS

| PH | PL | BA | OP CODE 5D | 1 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. LOAD REGISTERS 2 THROUGH 15 FROM WORDS 2 THROUGH 15 OF THE HOLD-GET AREA.

2. SET THE CF EQUAL TO:
   A. ONE, IF REGISTER 0 IS ZERO.
   B. ZERO, IF REGISTER 0 IS NONZERO.

3. SET THE OP CODE FIL BIT EQUAL TO BIT 15 IN WORD 0 OF THE HOLD-GET AREA.

4. BRANCH TO THE RETURN ADDRESS WHICH IS STORED IN WORDS 0 AND 1 OF THE HOLD-GET AREA.

5. ADD 16 TO THE HOLD-GET COUNTER.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY A SYSTEM MACRO. REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

APPROXIMATE EXECUTION TIME 31.20 MICROSECONDS

PTSAGN N  GET REGISTERS, LOAD RETURN CODE, AND BRANCH TO SAVED ADDRESS

| PR | PL | BA | OP CODE 5D | 2 | N |

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. LOAD REGISTERS 2 THROUGH 15 FROM WORDS 2 THROUGH 15 OF THE HOLD-GET AREA.

2. LOAD THE RETURN CODE N INTO BITS (3-0) OF REGISTER 0.
   BITS (15-4) OF REGISTER 0 ARE SET TO ZERO BY THIS INSTRUCTION.

3. SET THE CF EQUAL TO:
   A. ONE, IF REGISTER 0 IS ZERO.
   B. ZERO, IF REGISTER 0 IS NONZERO.

4. SET THE OP CODE FIL BIT EQUAL TO BIT 15 IN WORD 0 OF THE HOLD-GET AREA.

5. BRANCH TO THE RETURN ADDRESS WHICH IS STORED IN WORDS 0 AND 1 OF THE HOLD-GET AREA.

6. ADD 16 TO THE HOLD-GET COUNTER.

   NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY A SYSTEM MACRO.
   REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

   APPROXIMATE EXECUTION TIME 31.35 MICROSECONDS

PIE  PROGRAM INTERRUPT END

| PR | PL | BA | OP CODE 5D | 4 | 0 |

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. ZERO THE BLOCK INTERRUPT (BIN) BIT IN THE SYSTEM STATUS REGISTER WHICH WILL ENABLE INTERRUPTS.

2. RESTORE THE OP CODE FILL BIT WHICH WAS SAVED IN BIT 15 OF WORD 0 OF THE HOLD-GET AREA.

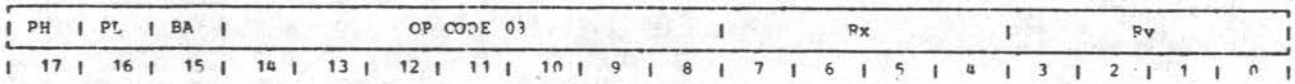
3. BRANCH TO THE RETURN ADDRESS WHICH IS STORED IN WORDS 0 AND 1 OF THE HOLD-GET AREA.

4. ADD 16 TO THE HOLD-GET COUNTER.

   APPROXIMATE EXECUTION TIME 4.20 MICROSECONDS

ARITHMETIC OPERATIONS

AP Rx,Ry  ADD Ry TO Rx AND STORE THE RESULT IN Rx



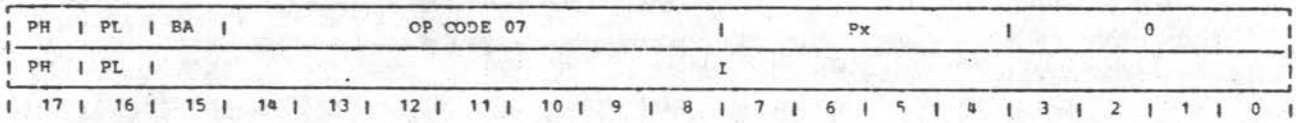

1. ADD THE CONTENTS OF Ry TO THE CONTENTS OF Rx AND PLACE THE RESULT IN Rx.

2. SET THE CF EQUAL TO:
   A. ONE, WHEN THIS INSTRUCTION CAUSES A CARRY BEYOND B(15).
   B. ZERO, WHEN THERE IS NO CARRY BEYOND B(15).

3. Ry IS UNCHANGED.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

AI Rx,I  ADD 16 BITS OF IMMEDIATE DATA, I, TO Rx

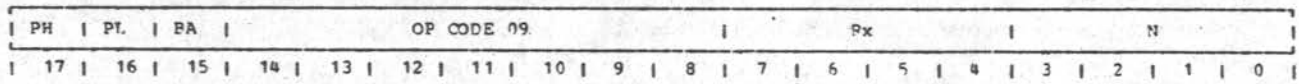



1. ADD I TO THE CONTENTS OF Rx AND STORE THE RESULTS IN Rx.

2. SET THE CF EQUAL TO:
   A. ONE, WHEN THIS INSTRUCTION CAUSES A CARRY BEYOND B(15).
   B. ZERO, WHEN THERE IS NO CARRY BEYOND B(15).

   APPROXIMATE EXECUTION TIME  2.40 MICROSECONDS

AN Rx,N  ADD 4 BITS OF IMMEDIATE DATA, N, TO Rx

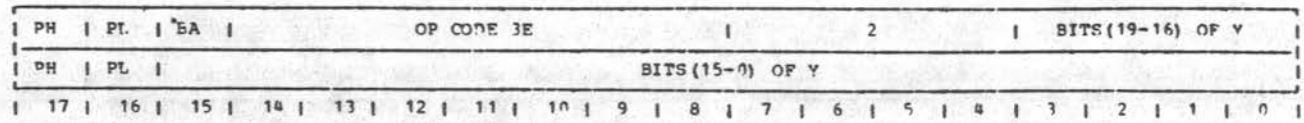



1. ADD N TO THE CONTENTS OF Rx AND STORE THE RESULTS IN Rx.

2. SET THE CF EQUAL TO:
   A. ONE, WHEN THIS INSTRUCTION CAUSES A CARRY BEYOND B(15).
   B. ZERO, WHEN THERE IS NO CARRY BEYOND B(15).

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

AIS Y  ADD 1 TO THE CONTENTS OF MEMORY AT LOCATION Y




1. ADD 1 TO THE CONTENTS OF MEMORY AT LOCATION Y.

2. SET THE CF EQUAL TO:
   A. ONE, WHEN THIS INSTRUCTION CAUSES A CARRY BEYOND B(15).
   B. ZERO, WHEN THERE IS NO CARRY BEYOND B(15).

3. PLACE THE SUM IN MEMORY AT LOCATION Y.

   APPROXIMATE EXECUTION TIME  5.40 MICROSECONDS

SN Rx,N  SUBTRACT 4 BITS OF IMMEDIATE DATA, N, FROM Rx

| PH | PL | BA | OP CODE 08 | Rx | 2s COMPLEMENT OF N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 | 4 3 2 1 0 |

1. SUBTRACT N FROM THE CONTENTS OF Rx AND STORE THE RESULT IN Rx.
   THE SUBTRACTION IS ACCOMPLISHED BY ADDING THE 2s COMPLEMENT OF N TO Rx.
   IF N IS EQUAL TO 0, 16 WILL BE SUBTRACTED FROM Rx.

2. SET THE CF EQUAL TO:
   A. ONE, WHEN Rx≥N IF N≠0.
   B. ZERO, WHEN Rx<N.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

SR Rx,Ry  SUBTRACT Ry FROM Rx AND STORE THE RESULT IN Rx

| PH | PL | BA | OP CODE 0A | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 | 4 3 2 1 0 |

1. SUBTRACT THE CONTENTS OF Ry FROM THE CONTENTS OF Rx AND STORE THE RESULT IN Rx.

2. SET THE CF EQUAL TO:
   A. ONE, WHEN Rx≥Ry.
   B. ZERO, WHEN Rx<Ry.

3. Ry IS UNCHANGED.

   APPROXIMATE EXECUTION TIME  1.35 MICROSECONDS

SI Rx,I  SUBTRACT 16 BITS OF IMMEDIATE DATA, I, FROM Rx

| PH | PL | BA | OP CODE 07 | Rx | 0 |
|---|---|---|---|---|---|
| PH | PL | 2s COMPLEMENT OF I | | | |
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 | 4 3 2 1 0 |

1. SUBTRACT I FROM THE CONTENTS OF Rx AND STORE THE RESULT IN Rx.
   THE SUBTRACTION IS ACCOMPLISHED BY ADDING THE 2s COMPLEMENT OF I TO Rx.

2. SET THE CF EQUAL TO:
   A. ONE, WHEN Rx≥I IF I≠0.
   B. ZERO, WHEN Rx<I.

   APPROXIMATE EXECUTION TIME  2.40 MICROSECONDS

LOGIC OPERATIONS

COM Rx[,Ry]  COMPLEMENT Rx[Ry] AND STORE IN Rx

| PH | PL | BA | OP CODE 1B | Rx | Rx[Ry] |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. IF Ry IS NOT SPECIFIED, COMPLEMENT Rx AND STORE IN Rx.

2. IF Ry IS SPECIFIED, COMPLEMENT Ry AND STORE IN Rx.

3. IF Rx IS EQUAL TO:
   A. ZERO, SET THE CF.
   B. NONZERO, CLEAR THE CF.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

NI Rx,I  AND 16 BITS OF IMMEDIATE DATA, I, TO Rx AND STORE IN Rx

| PH | PL | BA | OP CODE 07 | Rx | 2 |
|---|---|---|---|---|---|
| PH | PL | | I | | |
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. AND 16 BITS OF IMMEDIATE DATA, I, TO Rx AND STORE IN Rx.

2. IF Rx IS EQUAL TO:
   A. ZERO, SET THE CF.
   B. NONZERO, CLEAR THE CF.

   APPROXIMATE EXECUTION TIME  2.40 MICROSECONDS

NR Rx,Ry  AND Ry TO Rx AND STORE IN Rx

| PH | PL | BA | OP CODE 18 | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. AND Ry TO Rx AND STORE THE RESULT IN Rx.

2. Ry IS UNCHANGED.

3. IF Rx IS EQUAL TO:
   A. ZERO, SET THE CF.
   B. NONZERO, CLEAR THE CF.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

OI Rx,I  INCLUSIVE OR 16 BITS OF IMMEDIATE DATA, I, TO Rx AND STORE IN Rx

| PH | PL | BA | OP CODE 07 | Rx | 3 |
|---|---|---|---|---|---|
| PH | PL | | I | | |
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. INCLUSIVE OR 16 BITS OF IMMEDIATE DATA, I, TO Rx AND STORE IN Rx.

2. IF Rx IS EQUAL TO:
   A. ZERO, SET THE CF.
   B. NONZERO, CLEAR THE CF.

   APPROXIMATE EXECUTION TIME  2.40 MICROSECONDS

OR Rx,Ry  INCLUSIVE OR Ry TO Rx AND STORE IN Rx

| PH | PT | BA | OP CODE 19 | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. INCLUSIVE OR Ry TO Rx AND STORE THE RESULT IN Rx.

2. Ry IS UNCHANGED.

3. IF Rx IS EQUAL TO:
   A. ZERO, SET THE CF.
   B. NONZERO, CLEAR THE CF.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

XI Rx,I  EXCLUSIVE OR 16 BITS OF IMMEDIATE DATA, I, TO Rx AND STORE IN Rx

| PH | PT | BA | OP CODE 07 | Rx | 0 |
|---|---|---|---|---|---|
| PH | PT | | I | | |
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. EXCLUSIVE OR 16 BITS OF IMMEDIATE DATA, I, TO Rx AND STORE IN Rx.

2. IF Rx IS EQUAL TO:
   A. ZERO, SET THE CF.
   B. NONZERO, CLEAR THE CF.

   APPROXIMATE EXECUTION TIME  2.40 MICROSECONDS

XP Rx,Ry  EXCLUSIVE OR Ry TO Rx AND STORE IN Rx

| PH | PT | BA | OP CODE 1A | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. EXCLUSIVE OR Ry TO Rx AND STORE THE RESULT IN Rx.

2. Ry IS UNCHANGED.

3. IF Rx IS EQUAL TO:
   A. ZERO, SET THE CF.
   B. NONZERO, CLEAR THE CF.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

CR Rx,Ry  COMPARE Ry TO Rx

| PH | PT | BA | OP CODE 20 | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

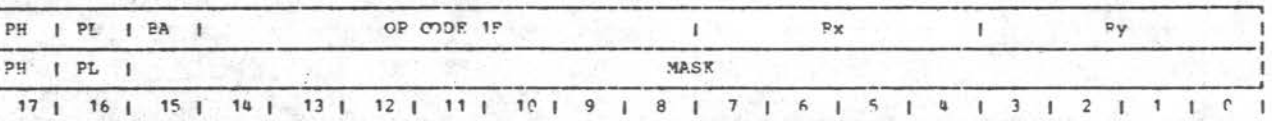
1. COMPARE Rx TO Ry BIT FOR BIT.

2. SET THE CF TO:
   A. ONE, IF ALL OF THE BITS MATCH.
   B. ZERO, IF ONE OR MORE OF THE BIT POSITIONS MISMATCH.

3. Rx AND Ry ARE NOT CHANGED BY THIS INSTRUCTION.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

CPM Rx,Ry,M  COMPARE Ry TO Rx UNDER 16 BIT IMMEDIATE MASK



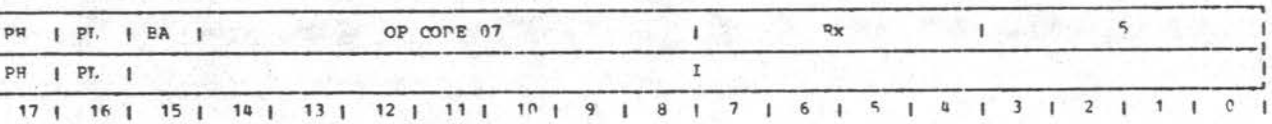

1. COMPARE Rx TO Ry BIT FOR BIT FOR EVERY BIT IN THE MASK THAT IS ONE.

2. SET THE CF TO:
   A. ONE, IF ALL OF THE BITS COMPARED MATCH.
   B. ZERO, IF ONE OR MORE OF THE COMPARED BIT POSITIONS MISMATCH.

3. Rx AND Ry ARE NOT CHANGED BY THIS INSTRUCTION.

   APPROXIMATE EXECUTION TIME  2.40 MICROSECONDS

CI Rx,I  COMPARE Rx TO 16-BITS OF IMMEDIATE DATA, I



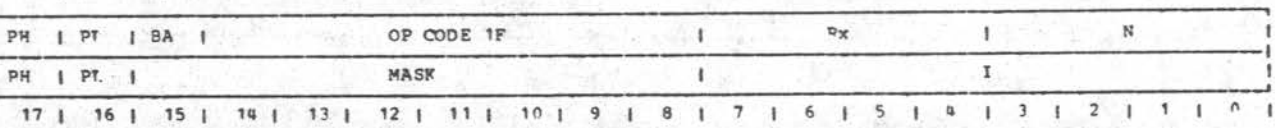

1. COMPARE Rx TO I BIT FOR BIT.

2. SET THE CF TO:
   A. ONE, IF ALL OF THE BITS MATCH.
   B. ZERO, IF ONE OR MORE OF THE BIT POSITIONS MISMATCH.

3. Rx IS NOT CHANGED BY THIS INSTRUCTION.

   APPROXIMATE EXECUTION TIME  2.40 MICROSECONDS

CIRM Rx,I,N,M  COMPARE 8 BITS OF Rx ROTATED BY N WITH IMMEDIATE DATA AND MASK




1. COMPARE Rx TO I BIT FOR BIT FOR EVERY BIT IN THE MASK THAT IS ONE.

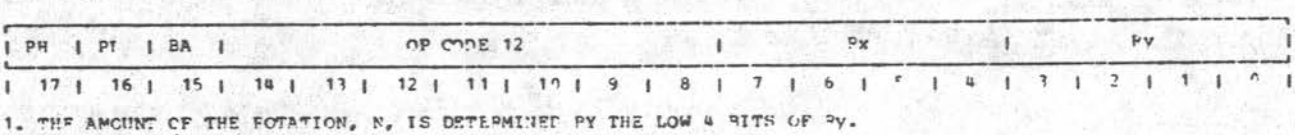
2. THE BITS IN Rx THAT ARE COMPARED ARE THE LOW 8 BITS AFTER THE CONTENTS OF Rx HAVE BEEN ROTATED RIGHT BY N.

3. SET THE CF TO:
   A. ONE, IF ALL OF THE BITS COMPARED MATCH.
   B. ZERO, IF ONE OR MORE OF THE COMPARED BIT POSITIONS MISMATCH.

4. Rx IS NOT CHANGED BY THIS INSTRUCTION.

   APPROXIMATE EXECUTION TIME  2.40 MICROSECONDS

RT Rx,Ry  ROTATE Rx LEFT AN AMOUNT DETERMINED BY THE LOW 4 BITS OF Ry




1. THE AMOUNT OF THE ROTATION, N, IS DETERMINED BY THE LOW 4 BITS OF Ry.

2. ROTATE Rx LEFT BY N BIT POSITIONS.

3. Ry IS UNCHANGED.

   APPROXIMATE EXECUTION TIME  2.70 MICROSECONDS

RLN Rx,N  ROTATE Rx LEFT BY N BIT POSITIONS

| PH | PL | BA | OP CODE 11 | Rx | 16-N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 | 4 3 2 1 0 |

1. ROTATE Rx LEFT BY N BIT POSITIONS.

   APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

RR Rx,Ry  ROTATE Rx RIGHT AN AMOUNT DETERMINED BY THE LOW 4 BITS OF Ry

| PH | PL | BA | OP CODE 13 | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 | 4 3 2 1 0 |

1. THE AMOUNT OF THE ROTATION, N, IS DETERMINED BY THE LOW 4 BITS OF Ry.

2. ROTATE Rx RIGHT BY N BIT POSITIONS.

3. Ry IS UNCHANGED.

   APPROXIMATE EXECUTION TIME 1.50 MICROSECONDS

RRN Rx,N  ROTATE Rx RIGHT BY N BIT POSITIONS

| PH | PL | BA | OP CODE 11 | Rx | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 | 4 3 2 1 0 |

1. ROTATE Rx RIGHT BY N BIT POSITIONS.

   APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

TZ Rx  TEST Rx FOR ALL ZEROS

| PH | PL | BA | OP CODE 18 | Rx | Rx |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 | 4 3 2 1 0 |

1. IF Rx IS EQUAL TO:
   A. ZERO, SET THE CF.
   B. NONZERO, ZERO THE CF.

   APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

FLZ Rx,Ry  FIND LOW ZERO IN Rx AND RECORD ITS POSITION IN Ry

| PH | PL | BA | OP CODE 21 | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 7 6 5 | 4 3 2 1 0 |

1. LOOK THROUGH Rx FOR THE FIRST ZERO FROM THE LOW END.

2. IF A ZERO IS FOUND:
   A. ITS LOCATION IS TRANSLATED TO A 4-BIT BINARY NUMBER WHICH IS PLACED INTO Ry.
   B. BITS(15-4) OF Ry ARE SET TO ZERO.
   C. THE CF IS SET TO 1.
   D. THE ZERO IN Rx IS SET TO 1.

3. IF A ZERO IS NOT FOUND.
   A. THE CF IS SET TO 0.
   B. Ry IS UNCHANGED.

   NOTE: Rx SHOULD NOT EQUAL Ry

   APPROXIMATE EXECUTION TIME 1.95 MICROSECONDS IF A ZERO IS FOUND AND 1.20 MICROSECONDS IF A ZERO IS NOT FOUND

SINGLE BIT OPERATIONS

SCF SET THE CONDITION-FLOP

| PH | PL | BA | OP CODE 20 | 0 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. SET THE CONDITION-FLOP.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

SOP SET OP CODE FIL BIT

| PH | PL | BA | OP CODE 0D | 0 | 1 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. SET OP CODE FIL BIT.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

SBN Px,B SET BIT B IN Px

| PH | PL | BA | OP CODE 2C | Rx | B |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. SET BIT B IN Px.
2. ALL OTHER BITS OF Px ARE UNCHANGED.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

SBR Rx,Ry SET BIT IN Px DETERMINED BY THE LOW 4 BITS OF Py

| PH | PL | BA | OP CODE 2D | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. THE BIT POSITION B IS DETERMINED BY THE LOW 4 BITS OF Ry.
2. SET BIT B IN Px.
3. ALL OTHER BITS OF Px ARE UNCHANGED.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

SBS N(PA),B SET BIT B IN MEMORY WORD AT LOCATION DETERMINED BY ADDING N TO PA

| PH | PL | BA | OP CODES 62/63 | B | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. THIS INSTRUCTION OPERATES ON WORD WY AT LOCATION DETERMINED BY ADDING N TO PA.
2. SET BIT B IN WORD WY.
3. ALL OTHER BITS OF WY ARE UNCHANGED.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF PA. IT IS 0 FOR PA=12 AND 1 FOR PA=14.
SEE NOTE CONCERNING PA ON PAGE B2.

APPROXIMATE EXECUTION TIME 4.35 MICROSECONDS

ZCF . ZERO THE CONDITION-FLOP

| PH | PL | BA | OP CODE 09 | 0 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. ZERO THE CONDITION-FLOP.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

ZBN Rx,B ZERO BIT B IN Rx

| PH | PL | BA | OP CODE 24 | Rx | B |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. ZERO BIT B IN Rx.
2. ALL OTHER BITS OF Rx ARE UNCHANGED.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

ZBR Rx,Ry ZERO BIT IN Rx DETERMINED BY THE LOW 4 BITS OF Ry

| PH | PL | BA | OP CODE 25 | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. THE BIT POSITION B IS DETERMINED BY THE LOW 4 BITS OF Ry.
2. ZERO BIT B IN Rx.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

ZBS N(RA),B ZERO BIT B IN MEMORY WORD AT LOCATION DETERMINED BY ADDING N TO RA

| PH | PL | BA | OP CODES 64/65 | B | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. THIS INSTRUCTION OPERATES ON WORD WY AT LOCATION DETERMINED BY ADDING N TO RA.
2. ZERO BIT B IN WORD WY.
3. ALL OTHER BITS OF WY ARE UNCHANGED.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 4.35 MICROSECONDS

ZOP ZERO OP CODE FIL BIT

| PH | PL | BA | OP CODE 0D | 0 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. ZERO OP CODE FIL BIT.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

ICF Px,N  INSERT CF IN BIT N OF Px

| PH | PL | BA | OP CODE 30 | Rx | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. IF THE CF IS EQUAL TO:
   A. ZERO, ZERO BIT N OF Px.
   B. ONE, SET BIT N OF Px.

2. ALL OTHER BITS OF Px ARE UNCHANGED.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

TPPL Rx  TEST GENERAL REGISTER PARITY LOW

| PH | PL | BA | OP CODE 5E | 0 | Rx |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. SET THE CF EQUAL TO PL OF Rx. PL IS THE PARITY BIT FOR DATA BITS(7-0).

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

TPPH Rx  TEST GENERAL REGISTER PARITY HIGH

| PH | PL | BA | OP CODE 5E | 1 | Rx |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. SET THE CF EQUAL TO PH OF Rx. PH IS THE PARITY BIT FOR DATA BITS(15-8).

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

TSRPL Rs  TEST SPECIAL REGISTER PARITY LOW

| PH | PL | BA | OP CODE 5F | 0 | Rs |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. SET THE CF EQUAL TO PL OF Rs. PL IS THE PARITY BIT FOR DATA BITS(7-0).

   NOTE: IT IS NOT NECESSARY TO SUPPRESS THE GATING BUS PARITY CHECK WHEN USING THIS INSTRUCTION ON A SPECIAL REGISTER THAT MAY NOT HAVE CORRECT PARITY.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

TSRPH Rs  TEST SPECIAL REGISTER PARITY HIGH

| PH | PL | BA | OP CODE 5F | 1 | Rs |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. SET THE CF EQUAL TO PH OF Rs. PH IS THE PARITY BIT FOR DATA BITS(19-8).

   NOTE: IT IS NOT NECESSARY TO SUPPRESS THE GATING BUS PARITY CHECK WHEN USING THIS INSTRUCTION ON A SPECIAL REGISTER THAT MAY NOT HAVE CORRECT PARITY.

   APPROXIMATE EXECUTION TIME  1.20 MICROSECONDS

TBN Px,B  TEST BIT B IN Px

| PH | PL | BA | OP CODE 28 | Rx | B |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. SET THE CF EQUAL TO BIT B OF Px.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

TBR Rx,Ry  TEST BIT IN Px DETERMINED BY LOW 4 BITS OF Ry

| PH | PL | BA | OP CODE 29 | Rx | Ry |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. THE BIT POSITION B IS DETERMINED BY THE LOW 4 BITS OF Ry.
2. SET THE CF EQUAL TO BIT B OF Px.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

TBS N(RA),B  TEST BIT B IN MEMORY WORD AT LOCATION DETERMINED BY ADDING N TO RA

| PH | PL | BA | OP CODES 52/53 | B | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. THIS INSTRUCTION OPERATES ON WORD WY AT LOCATION DETERMINED BY ADDING N TO RA.
2. SET THE CF EQUAL TO BIT B IN WORD WY.

NOTE: BIT 8 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 3.30 MICROSECONDS

TCC1  TEST CENTRAL CONTROL 1

| PH | PL | BA | OP CODE 5F | 1 | F |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 6 5 4 | 3 2 1 0 |

1. SET THE CF EQUAL TO:
   A. ZERO, IF THIS INSTRUCTION IS EXECUTED IN CC 0.
   B. ONE, IF THIS INSTRUCTION IS EXECUTED IN CC 1.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

SIO SEND I/O MESSAGE OVER CHANNEL AND SUBCHANNEL DEFINED IN R9

| PH | PL | BA | OP CODE 27 | 0 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. IDLE THE MAIN I/O CHANNEL DEFINED IN BITS(15-10) OF REGISTER 9.
2. LOAD THE I/O STATUS REGISTER WITH THE SUBCHANNEL SELECT FIELD DEFINED IN BITS(9-4) OF REGISTER 9 AND JAM THE TRANSMIT NORMAL CONTROL STATE.
3. LOAD THE I/O DATA REGISTER FROM REGISTER 10.
4. LOAD REGISTER 11 FROM THE I/O DATA REGISTER AND PERFORM A MATCH TEST.
5. INITIATE MESSAGE TRANSMISSION.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

SMIO SEND MAINTENANCE I/O MESSAGE OVER CHANNEL AND SUBCHANNEL DEFINED IN R9

| PH | PL | BA | OP CODE 27 | 2 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. IDLE THE MAIN I/O CHANNEL DEFINED IN BITS(15-10) OF REGISTER 9.
2. LOAD THE I/O STATUS REGISTER WITH THE SUBCHANNEL SELECT FIELD DEFINED IN BITS(9-4) OF REGISTER 9 AND JAM THE TRANSMIT MAINTENANCE CONTROL STATE.
3. LOAD THE I/O DATA REGISTER FROM REGISTER 10.
4. LOAD REGISTER 11 FROM THE I/O DATA REGISTER AND PERFORM A MATCH TEST.
5. INITIATE MESSAGE TRANSMISSION.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

TIO TEST FOR I/O MESSAGE IN CHANNEL DEFINED IN R9

| PH | PL | BA | OP CODE 27 | 4 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | |

1. IF A MESSAGE IS PRESENT IN THE MAIN I/O CHANNEL DEFINED IN BITS(15-10) OF REGISTER 9:
   A. THE CF IS SET TO 1.
   B. REGISTER 11 IS LOADED WITH THE MESSAGE AND CHECKED FOR PARITY.
   C. THE MAIN CHANNEL IS PUT IN THE IDLE STATE.
2. IF A MESSAGE IS NOT PRESENT IN THE MAIN I/O CHANNEL DEFINED IN BITS(15-10) OF REGISTER 9:
   A. THE CF IS SET TO 0.
   B. REGISTER 11 IS UNCHANGED.
3. REGISTER 10 IS NOT CHANGED BY THIS INSTRUCTION.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

TMIO TEST FOR MAINTENANCE I/O MESSAGE IN CHANNEL DEFINED IN R9

| PH | PL | PA | OP CODE 27 | 5 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. IF A MAINTENANCE MESSAGE IS PRESENT IN THE MAIN I/O CHANNEL DEFINED IN BITS(15-10) OF REGISTER 9:
   A. THE CF IS SET TO 1.
   B. REGISTER 11 IS LOADED WITH THE MESSAGE AND CHECKED FOR PARITY.
   C. THE MAIN CHANNEL IS PUT IN THE IDLE STATE.
2. IF A MAINTENANCE MESSAGE IS NOT PRESENT IN THE MAIN I/O CHANNEL DEFINED IN BITS(15-10) OF REGISTER 9:
   A. THE CF IS SET TO 0.
   B. REGISTER 11 IS UNCHANGED.
3. REGISTER 10 IS NOT CHANGED BY THIS INSTRUCTION.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

TCH TEST THE MAIN I/O CHANNEL DEFINED IN R9 FOR THE IDLE STATE

| PH | PL | BA | OP CODE 27 | 6 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. IF THE MAIN I/O CHANNEL DEFINED IN BITS(15-10) OF REGISTER 9 IS:
   A. IDLE, SET THE CF TO 1.
   B. NOT IDLE, SET THE CF TO 0.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

TIO IDLE THE MAIN I/O CHANNEL DEFINED IN R9

| PH | PL | BA | OP CODE 27 | 7 | 0 |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. IDLE THE MAIN I/O CHANNEL DEFINED IN BITS (15-10) OF REGISTER 9.

NOTE: BITS(9-4) OF REGISTER 9 MUST CONTAIN A 3-OUT-OF-6 CODE TO PREVENT AN I/O ERROR.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

CONL N(RA) COMPLEMENT WRITE THE ON-LINE STORE AT LOCATION RA INDEXED BY N

| PH | PL | BA | OP CODE 7A | 0/1 | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 | 6 5 4 3 2 1 0 |

1. COMPUTE THE EFFECTIVE ADDRESS FOR THIS INSTRUCTION BY ADDING N TO RA.
2. SAVE THE CONTENTS OF THE MAIN MEMORY STATUS REGISTER.
3. READ THE ON-LINE STORE WITHOUT STORE ERROR CORRECTION OR PROCESSOR ERROR CORRECTION.
4. WRITE THE COMPLEMENT OF THE RECEIVED DATA INTO THE ON-LINE STORE.
5. RESTORE THE PREVIOUSLY SAVED CONTENTS OF THE MAIN MEMORY STATUS REGISTER.
6. ZERO THE CONDITION FLIP FLOP.
7. THIS INSTRUCTION KEEPS AN INTERNAL TIMER TO PREVENT THE CC FROM HANGING. IF THE INSTRUCTION TIMES OUT, REGISTER 0 IS SET TO ALL ONES.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY SYSTEM MACROS. REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

NOTE: BIT 4 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14. SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 9.90 MICROSECONDS.

CONLX Rx(RA) COMPLEMENT WRITE THE ON-LINE STORE AT LOCATION RA INDEXED BY Rx

| PH | PL | BA | OP CODE 7A | 2/3 | Rx |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 9 8 | 7 | 6 5 4 3 2 1 0 |

1. COMPUTE THE EFFECTIVE ADDRESS FOR THIS INSTRUCTION BY ADDING Rx TO RA.
2. SAVE THE CONTENTS OF THE MAIN MEMORY STATUS REGISTER.
3. READ THE ON-LINE STORE WITHOUT STORE ERROR CORRECTION OR PROCESSOR ERROR CORRECTION.
4. WRITE THE COMPLEMENT OF THE RECEIVED DATA INTO THE ON-LINE STORE.
5. RESTORE THE PREVIOUSLY SAVED CONTENTS OF THE MAIN MEMORY STATUS REGISTER.
6. ZERO THE CONDITION FLIP FLOP.
7. THIS INSTRUCTION KEEPS AN INTERNAL TIMER TO PREVENT THE CC FROM HANGING. IF THE INSTRUCTION TIMES OUT, REGISTER 0 IS SET TO ALL ONES.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY SYSTEM MACROS. REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

NOTE: BIT 4 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14. SEE NOTE CONCERNING RA ON PAGE B2.

APPROXIMATE EXECUTION TIME 9.75 MICROSECONDS.

COFI. N(PA)  COMPLEMENT WRITE THE OFF-LINE STORE AT LOCATION PA INDEXED BY N

| PH | PL | BA | OP CODE 7B | 0/1 | N |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 | 9 | 8 7 6 5 4 3 2 1 0 |

1. COMPUTE THE EFFECTIVE ADDRESS FOR THIS INSTRUCTION BY ADDING N TO RA.
2. SAVE THE CONTENTS OF THE MAIN MEMORY STATUS REGISTER.
3. READ THE OFF-LINE STORE WITHOUT STORE ERROR CORRECTION OR PROCESSOR ERROR CORRECTION.
4. WRITE THE COMPLEMENT OF THE RECEIVED DATA INTO THE OFF-LINE STORE.
5. RESTORE THE PREVIOUSLY SAVED CONTENTS OF THE MAIN MEMORY STATUS REGISTER.
6. ZERO THE CONDITION FLIP FLOP.
7. THIS INSTRUCTION KEEPS AN INTERNAL TIMER TO PREVENT THE CC FROM HANGING.
   IF THE INSTRUCTION TIMES OUT,REGISTER 0 IS SET TO ALL ONES.

   NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY,IT WILL BE SUPPLIED BY SYSTEM MACROS.
   REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

   NOTE: BIT 4 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
   SEE NOTE CONCERNING PA ON PAGE B2.

   APPROXIMATE EXECUTION TIME 10.20 MICROSECONDS.

COFLX Rx(PA)  COMPLEMENT WRITE THE OFF-LINE STORE AT LOCATION PA INDEXED BY Rx

| PH | PL | BA | OP CODE 7B | 2/3 | Rx |
|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 13 12 11 10 | 9 8 | 7 6 5 4 3 2 1 0 |

1. COMPUTE THE EFFECTIVE ADDRESS FOR THIS INSTRUCTION BY ADDING Rx TO RA.
2. SAVE THE CONTENTS OF THE MAIN MEMORY STATUS REGISTER.
3. READ THE OFF-LINE STORE WITHOUT STORE ERROR CORRECTION OR PROCESSOR ERROR CORRECTION.
4. WRITE THE COMPLEMENT OF THE RECEIVED DATA INTO THE OFF-LINE STORE.
5. RESTORE THE PREVIOUSLY SAVED CONTENTS OF THE MAIN MEMORY STATUS REGISTER.
6. ZERO THE CONDITION FLIP FLOP.
7. THIS INSTRUCTION KEEPS AN INTERNAL TIMER TO PREVENT THE CC FROM HANGING.
   IF THE INSTRUCTION TIMES OUT,REGISTER 0 IS SET TO ALL ONES.

   NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY,IT WILL BE SUPPLIED BY SYSTEM MACROS.
   REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

   NOTE: BIT 4 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
   SEE NOTE CONCERNING RA ON PAGE B2.

   APPROXIMATE EXECUTION TIME 10.05 MICROSECONDS.

MSTF N(PA)  MAINTENANCE STORE FUNCTION USING REGISTER 0 AT LOCATION RA INDEXED BY N

| PH | PL | PA | OP CODE 01 | 0/1 | N |
|---|---|---|---|---|---|

| PH | PL | BEC0 | CW0 | BDSR1 | BDSR0 | ISO1 | ISO0 | UPD1 | UPD0 | IDL1 | IDL0 | RW1 | RW0 | MM21 | MM20 | MM11 | MM10 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. COMPUTE THE EFFECTIVE ADDRESS FOR THIS INSTRUCTION BY ADDING N TO RA.

2. SAVE THE CONTENTS OF THE MAIN MEMORY STATUS REGISTER.

3. LOAD THE MAIN MEMORY STATUS REGISTER FROM THE SECOND WORD OF THIS INSTRUCTION.
   THE ISOLATE BITS ARE LEFT AS THEY WERE ON ENTRY.

4. PERFORM THE INDICATED READ/WRITE OPERATION USING REGISTER 0 AS DESTINATION/SOURCE FOR THE DATA.

5. RESTORE THE PREVIOUSLY SAVED CONTENTS OF THE MAIN MEMORY STATUS REGISTER.

6. ZERO THE CONDITION-FLOP.

7. THIS INSTRUCTION KEEPS AN INTERNAL TIMER TO PREVENT THE CC FROM HANGING.
   IF THE INSTRUCTION TIMES OUT, REGISTER 0 IS SET TO ALL ONES.

8. CAUTION: THE STORE OPERATION DEFINED BY THE MAIN MEMORY STATUS CONSTANT IN WORD 2 MAY ALLOW THIS INSTRUCTION TO GATE STORE DATA WITH BAD PARITY ONTO THE PROCESSOR GATING BUS. IF HARDWARE CHECKS ARE NOT INHIBITED THIS WILL CAUSE A PROCESSOR SWITCH.

   NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY SYSTEM MACROS.
   REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

   NOTE: BIT 4 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
   SEE NOTE CONCERNING RA ON PAGE B2.

   APPROXIMATE EXECUTION TIME 7.20 MICROSECONDS

MSTFX Rx(RA)  MAINTENANCE STORE FUNCTION USING REGISTER 0 AT LOCATION RA INDEXED BY Rx

| PH | PL | BA | OP CODE 01 | 2/3 | Rx |
|---|---|---|---|---|---|

| PH | PL | BEC0 | CW0 | BDSR1 | BDSR0 | ISO1 | ISO0 | UPD1 | UPD0 | IDL1 | IDL0 | RW1 | RW0 | MM21 | MM20 | MM11 | MM10 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. COMPUTE THE EFFECTIVE ADDRESS FOR THIS INSTRUCTION BY ADDING Rx TO RA.

2. SAVE THE CONTENTS OF THE MAIN MEMORY STATUS REGISTER.

3. LOAD THE MAIN MEMORY STATUS REGISTER FROM THE SECOND WORD OF THIS INSTRUCTION.
   THE ISOLATE BITS ARE LEFT AS THEY WERE ON ENTRY.

4. PERFORM THE INDICATED READ/WRITE OPERATION USING REGISTER 0 AS DESTINATION/SOURCE FOR THE DATA.

5. RESTORE THE PREVIOUSLY SAVED CONTENTS OF THE MAIN MEMORY STATUS REGISTER.

6. ZERO THE CONDITION-FLOP.

7. THIS INSTRUCTION KEEPS AN INTERNAL TIMER TO PREVENT THE CC FROM HANGING.
   IF THE INSTRUCTION TIMES OUT, REGISTER 0 IS SET TO ALL ONES.

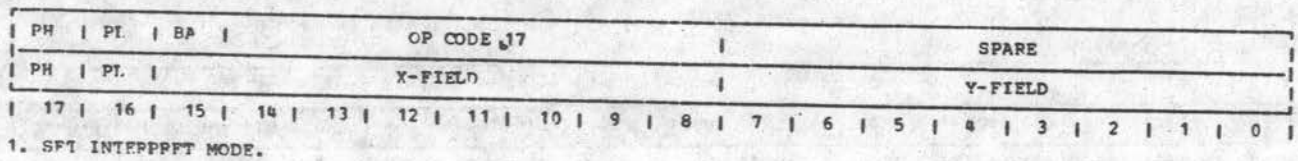
8. CAUTION: THE STORE OPERATION DEFINED BY THE MAIN MEMORY STATUS CONSTANT IN WORD 2 MAY ALLOW THIS INSTRUCTION TO GATE STORE DATA WITH BAD PARITY ONTO THE PROCESSOR GATING BUS. IF HARDWARE CHECKS ARE NOT INHIBITED THIS WILL CAUSE A PROCESSOR SWITCH.

   NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY SYSTEM MACROS.
   REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

   NOTE: BIT 4 IS DETERMINED BY THE VALUE OF RA. IT IS 0 FOR RA=12 AND 1 FOR RA=14.
   SEE NOTE CONCERNING RA ON PAGE B2.

   APPROXIMATE EXECUTION TIME 7.05 MICROSECONDS

MI MICRO INTERPRET

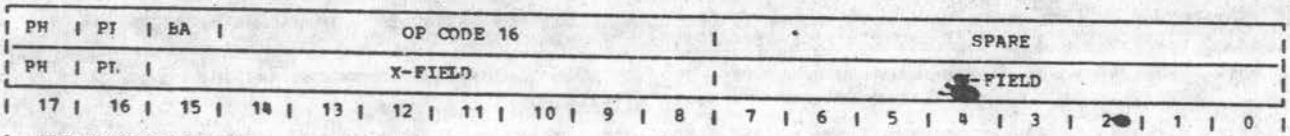



1. SET INTERPRET MODE.
2. GATE X-FIELD TO THE MIR TO FIELD AND Y-FIELD TO THE MIR FROM FIELD.
3. PERFORM THE INDICATED MICRO OPERATION.
4. REPEAT FOR THE NEXT STORAGE WORD UNTIL MICRO OPERATION WHICH TURNS OFF INTERPRET MODE IS GIVEN.
5. INTERRUPTS ARE NOT PROCESSED WHEN THE CC IS IN INTERPRET MODE.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY A SYSTEM MACRO. REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS PER MAIN MEMORY ACCESS

MIS SINGLE CYCLE MICRO INTERPRET

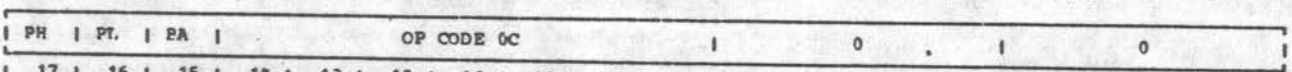



1. SET INTERPRET MODE.
2. GATE X-FIELD TO THE MIR TO FIELD AND Y-FIELD TO THE MIR FROM FIELD.
3. PERFORM THE INDICATED MICRO OPERATION.
4. CLEAR INTERPRET MODE AND EXECUTE THE NEXT SEQUENTIAL INSTRUCTION.
5. INTERRUPTS ARE NOT PROCESSED WHEN THE CC IS IN INTERPRET MODE.

NOTE: THIS INSTRUCTION SHOULD NOT BE CODED DIRECTLY, IT WILL BE SUPPLIED BY A SYSTEM MACRO. REFER TO 3ACC COMMON SYSTEM PROGRAMMERs GUIDE X-74292.

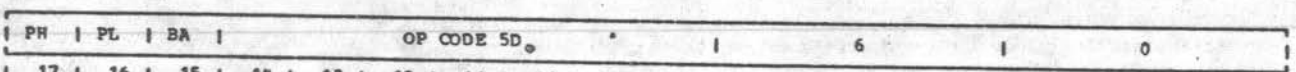
APPROXIMATE EXECUTION TIME 2.40 MICROSECONDS

NOP NO OPERATION




APPROXIMATE EXECUTION TIME 1.20 MICROSECONDS

HALT HALT THE CENTRAL CONTROL




1. THIS INSTRUCTION CAUSES THE CC TO LOOP UNTIL IT IS INITIALIZED OR INTERRUPTED. IF THE CC IS INTERRUPTED THE INTERRUPT WILL RETURN TO THE HALT INSTRUCTION.

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**********************************************************************
*  CAUTION: NO CHECK IS MADE TO DETERMINE THE ONLINE/OFFLINE STATUS  *
*           OF THE PROCESSOR PRIOR TO EXECUTION OF THIS INSTRUCTION  *
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