SHEET INDEX

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RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

NOTES:

1. ⏚ GROUND RETURN.

2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS. CAPACITANCE VALUES ARE IN MICROFARADS. VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.

3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS:

IC CODE	BAT TERM +5	GRD TERM
25LS2521	20	10
54S32	14	7
54S38	14	7
LS00	14	7
LS240	20	10
LS244	20	10
LS138	16	8
54LS280	14	7
93S48	16	8
54LS373	20	10
21288,LS	14	7
DS7837J	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

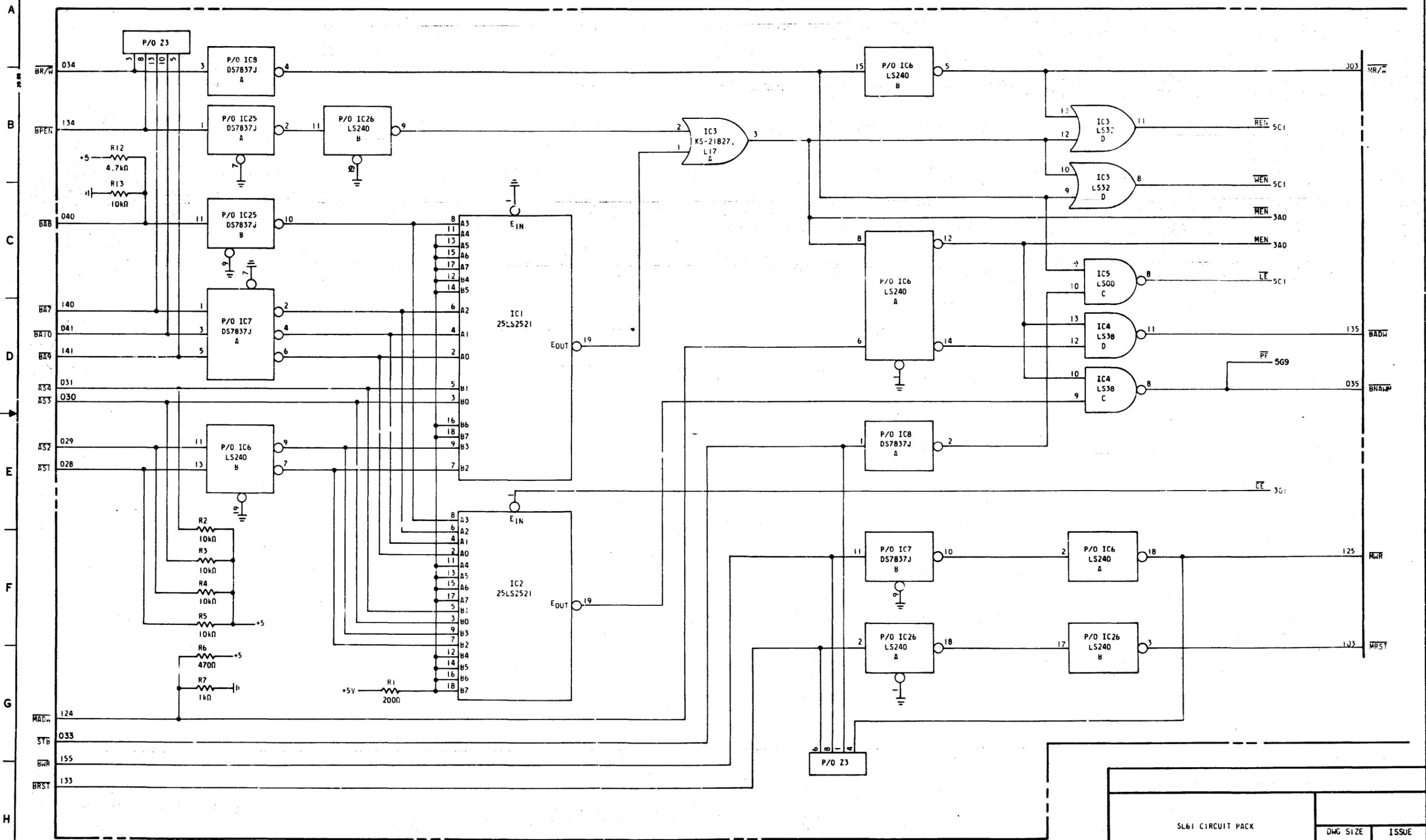| FUNCTION	TERMINALS
+5	000,001,002, 100,101,102
GRD	024,027,032,043,044, 045,055,056,122,123, 126,127,128,129,130, 131,132,143,144,145, 156

5. ALL RESISTORS ARE KS-20616,LIA.

6. A "B" PREFIX INDICATES THAT A SIGNAL APPEARS ONLY ON THE I/O BUS.

7. AN "M" PREFIX INDICATES THAT A SIGNAL APPEARS ONLY ON THE DAS (DISTRIBUTE AND SCAN) BUS.
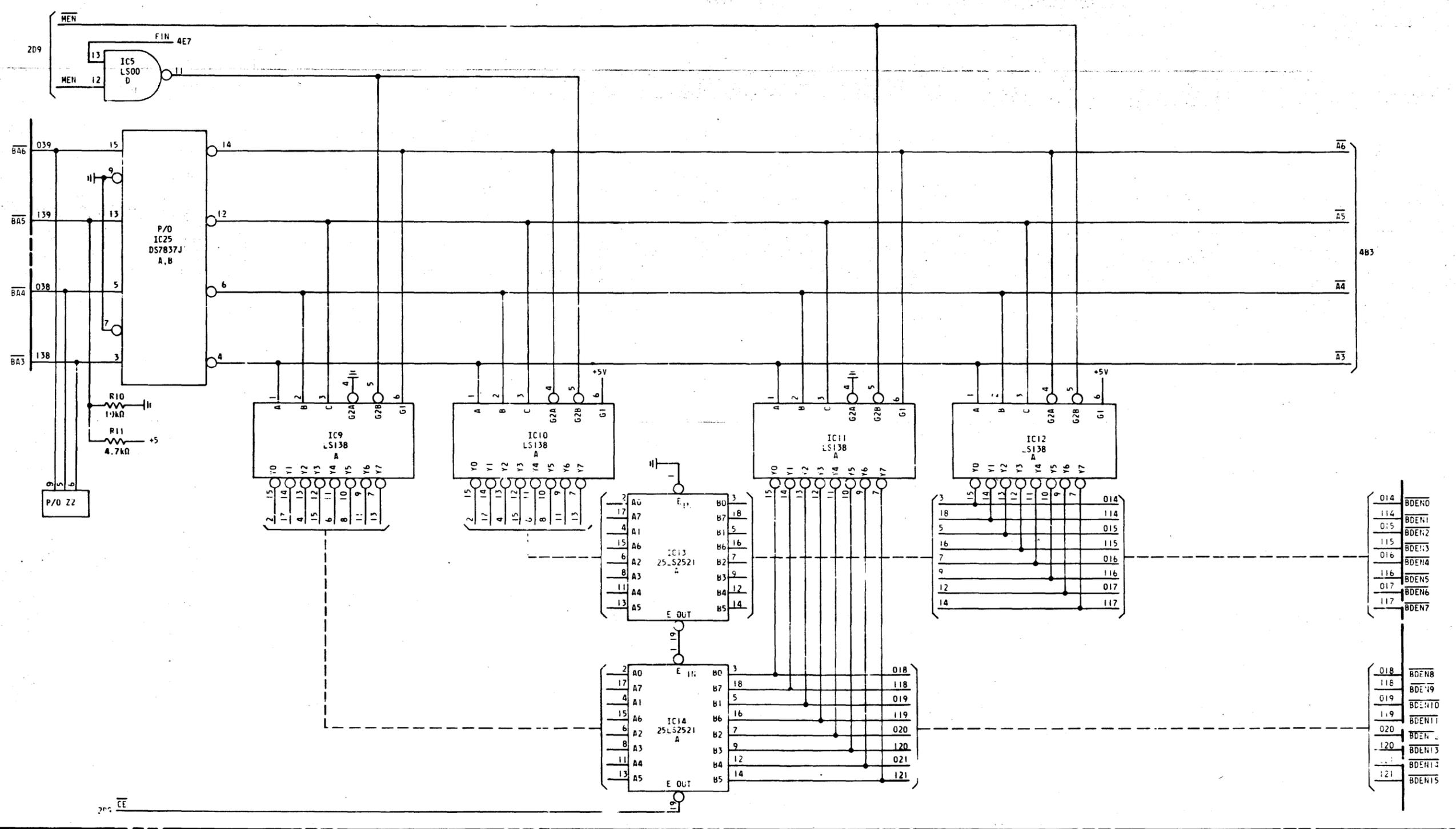
SYMBOL

SYSTEM USED ON	DESIGN CONTROL
COMMON	CB

SUPPORTING INFORMATION

CATEGORY	NO.

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.

2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.

3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

1N99

SL61 CIRCUIT PACK

MATRIX INTERFACE CIRCUIT

AT&TCO STANDARD

DWG SIZE 6S	ISSUE 2

BELL LABORATORIES	CPS-SL61	6 SHEETS

PART OF CPS SL6I

MATRIX INTERFACE

SL6I CIRCUIT PACK

	DWG SIZE	ISSUE
	6S	2

BELL LABORATORIES | CPS-SL6I | SHEET 2

BELL LABORATORIES	CPS-SL61		
SL6. CIRCUIT PACK	DWG SIZE 6S	ISSUE 2	
		SHEET 3	

PART OF CPS SL61
MATRIX INTERFACE
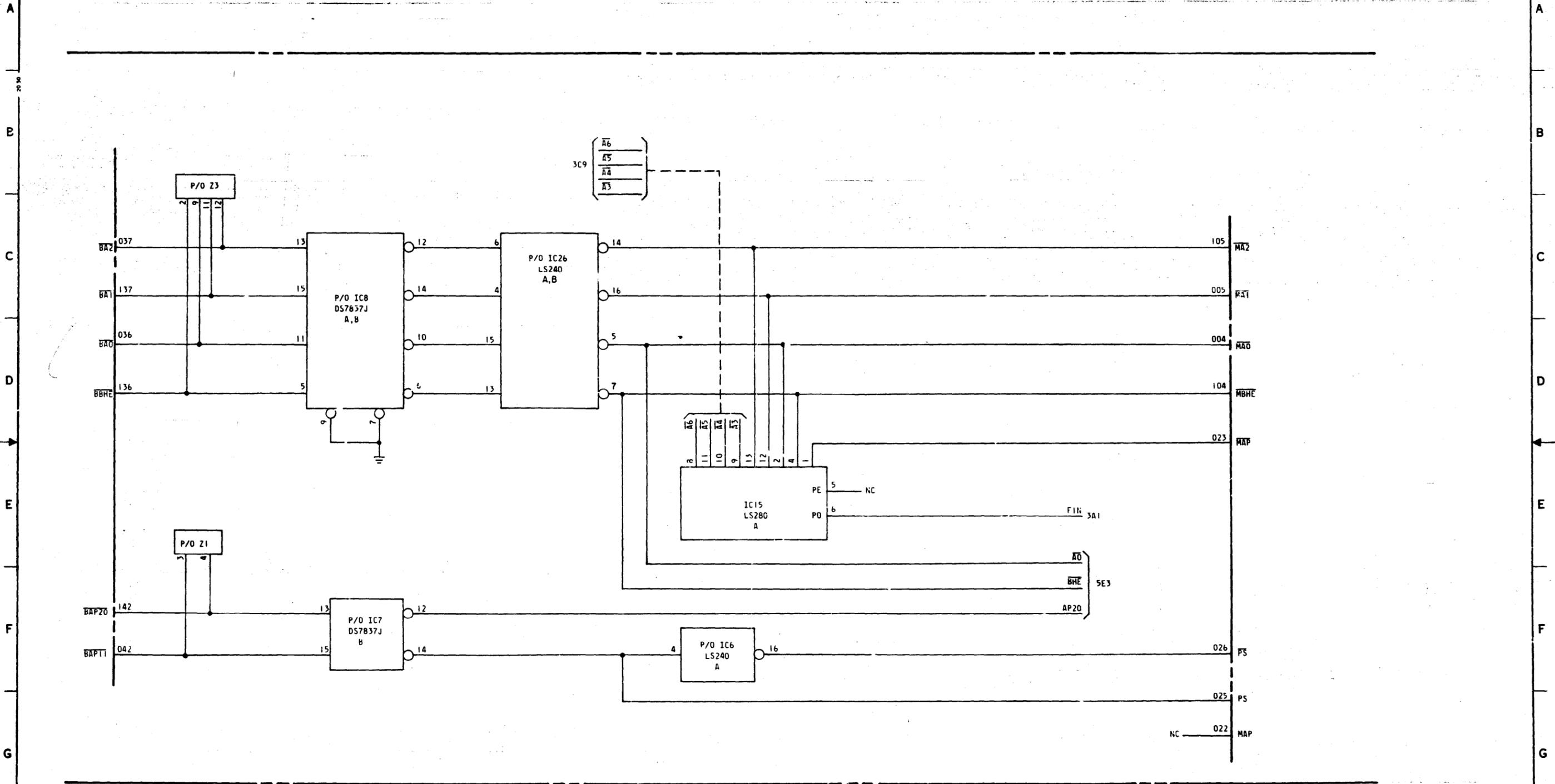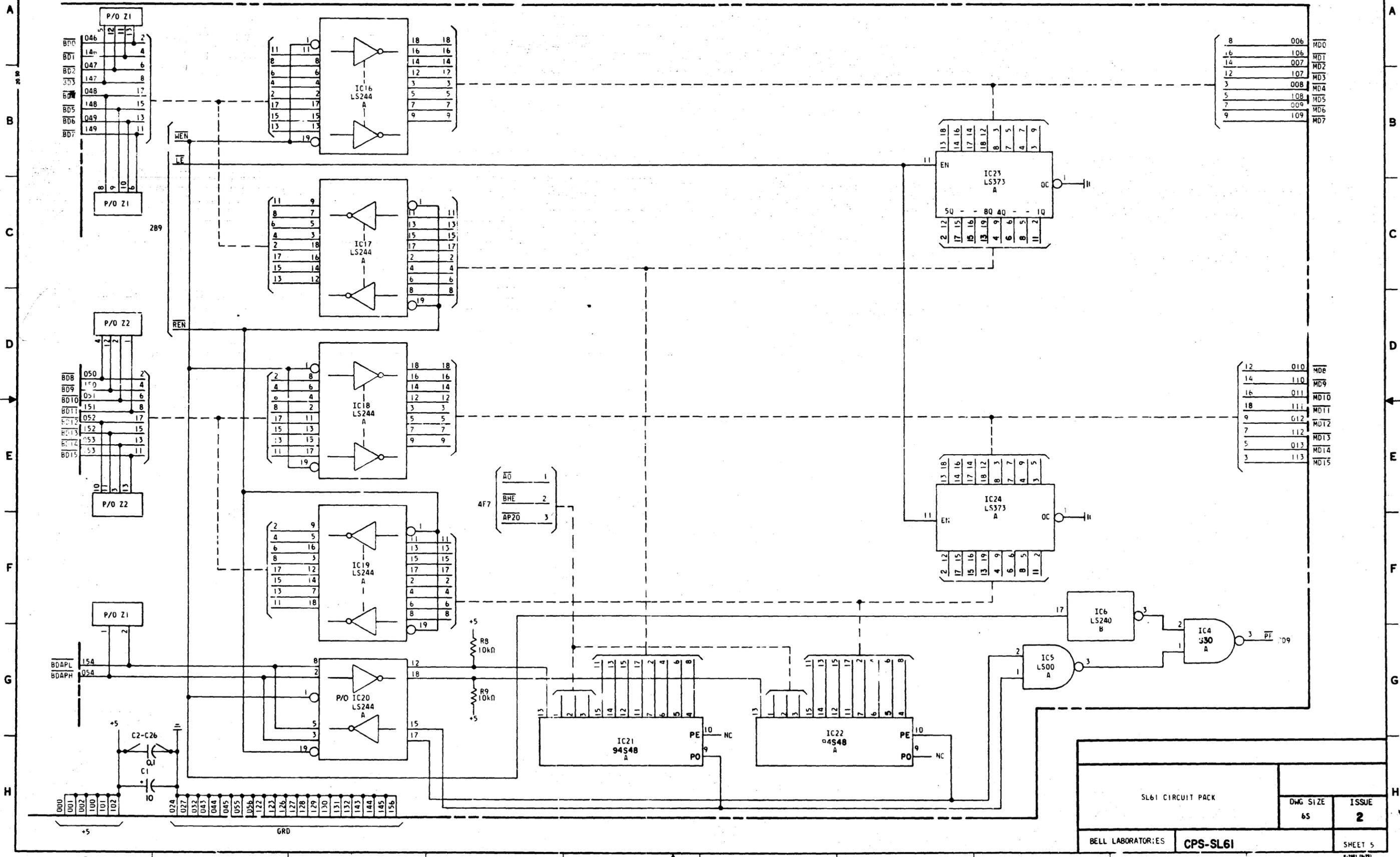
SL61 CIRCUIT PACK

DWG SIZE	ISSUE
6S	2

BELL LABORATORIES CPS-SL61

SHEET 4

SL61 CIRCUIT PACK

| BELL LABORATORIES | CPS-SL61 | DWG SIZE 6S | ISSUE 2 | SHEET 5 |

COMPONENT LIST

CIRCUIT, INTEGRATED

CP LOC	IC1		IC2		IC3		IC4		IC5		IC6		IC7		IC8	
CODE	AM25LS2521DM**		AM25LS2521DM**		SN54 S32J-00* OR KS-28127, L17		SN54S38J-00*		WA-LS00 OR SN54LS00J-00*		WA-LS240 OR SN54LS240J-00*		DS7837JX***		DS7837JX***	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		2D3		2F3		2B4		5G8		5G7	ELEM A	2C0, 2F7, 4F4	ELEM A	2D1	ELEM A	2B1, 2E6, 4D1
B						SPARE		SPARE		SPARE						
C						2B7		2D7		2C7						
D						2B7		2D7		3B1						
E																
F																
G																
H											ELEM B	2E1, 2B6, 5F7	ELEM B	2F6, 4F2	ELEM B	4D1
I																
J																

CP LOC	IC9		IC10		IC11		IC12		IC13		IC14		IC15		IC16	
CODE	WA-LS138 OR SN54LS138J-00*		WA-LS138 OR SN54LS138J-00*		WA-LS138 OR SN54LS138J-00*		WA-LS138 OR SN54LS138J-00*		AM25LS2521DM**		AM25LS2521DM**		SN54LS280J-00* OR KS-21285, L45		WA-LS244 OP SN54LS244J-00*	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		3D2		3D3		3D5		3D6		3E4		3G4		4E4		5B2
B																
C																
D																
E																
F																
G																
H																
I																
J																

CP LOC	IC17		IC18		IC19		IC20		IC21		IC22		IC23		IC24	
CODE	WA-LS244 OR SN54LS244J-00*		WA-LS244 OR SN54LS244J-00*		WA-LS244 OR SN54LS244J-00*		WA-LS244 OR SN54LS244J-00*		AM93S48DM**		AM93S48DM**		SN54LS373J-00*		SN54LS373J-00*	
ELEMEN	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		5C2		5E2		5F2		5G2		5G4		5G5		5C7		5F7
B																
C																
D																
E																
F																
G																
H																
I																
J																

CP LOC	IC25		IC26													
CODE	DS7837JX***		WA-LS240 OR SN54LS240J-00*													
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A																
B	ELEM A	2C1, 3C1	ELEM A	4C3												
C																
D																
E																
F																
G	ELEM B	2C1, 3C1	ELEM B	2B2, 2F7, 4C3												
H																
I																
J																

* TEXAS INSTRUMENTS
** ADVANCED MICRO DEVICES
*** NATIONAL SEMICONDUCTOR

CAPACITOR		NETWORK		RESISTOR	
DESIG	CODE	DESIG	CODE	DESIG	CODE
C1	601B,10	[3]Z1-Z3	KS-21288,L5	R1	KS-20616,L1A,200
[25]C2-C26	KS-21901,L1,0.1			[4]R2-R5	KS-20616,L1A,10kΩ
				R6	KS-20616,L1A,470
				R7	KS-20616,L1A,1kΩ
				R8-R10	KS-20616,L1A,10kΩ
				R11,R12	KS-20616,L1A,4.7kΩ
				R13	KS-20616,L1A,10kΩ

INPUT/OUTPUT INFORMATION

INPUT/OUTPUT LEADS

LEADS	DEFINITION
AS1-AS4	ADDRESS STRAPS
BA0-BA10	ADDRESS LEADS
BADW	ALL DECODE WELL
BAP11	ADDRESS PARITY OVER A0-A10
BAP20	ADDRESS PARITY OVER A0-A19 AND BHE
BBHE	BUS HIGH ENABLE
BD00-BD15	DATA LEADS
BDAPH	DATA ADDRESS PARITY OVER THE HIGH BYTE OF DATA
BDAPL	DATA ADDRESS PARITY OVER THE LOW BYTE OF DATA
BNAWN	NOT ALL WELL MATRIX
BPEN	PERIPHERAL ENABLE
B.ST	RESET
BR/W	READ/WRITE LEAD
BWR	WRITE STROBE
STB	STROBE LEAD

OUTPUTS

LEADS	DEFINITION
BDEN0-BDEN15	BOARD ENABLES
MA0-MA2	ADDRESS LEADS
MADW	ALL DECODE WELL
MAP,MAP	ADDRESS PARITY
MBHE	BUS HIGH ENABLE
MD00-MD15	DATA LEADS
MRST	RESET
MR/W	READ/WRITE LEAD
MWR	WRITE STROBE
PS,PS	PARITY STRAPS TO BE CONNECTED TO MAP AND MAP

LEADS ON BOARD

LEADS	DEFINITION
CE	CHIP ENABLE
FIN	FAULT INSERTION
LE	LATCH ENABLE
MEN,MEN	MATRIX ENABLE
PF	PARITY FAILURE
REN	READ ENABLE
WEN	WRITE ENABLE
GND	GROUND RETURN
NC	NO CONNECTION
+5V	BATTERY

CIRCUIT DESCRIPTION

SL61 IS THE MATRIX INTERFACE BOARD (MIF) FOR THE DISTRIBUTE AND SCAN (DAS) CIRCUITS OF THE CDT SYSTEM. ITS PURPOSE IS TO BUFFER AND ISOLATE THE I/O BUS FROM THE DAS BUS. THE CIRCUIT CAN BE DIVIDED INTO THREE PARTS: A BOARD ENABLE-DECODER WHICH IS PROGRAMMABLE TO ONE OF 16 ADDRESSES (IC'S 1,2,3), AN ADDRESS PARITY DECODER AND ONE OUT OF SIXTEEN DECODER (IC'S 9,10,11,12,13,14) TO GENERATE INDIVIDUAL BOARD ENABLE SIGNALS FOR THE SCAN OR DISTRIBUTE BOARDS, AND A BIDIRECTIONAL DATA BUS BUFFER AND DATA PARITY GENERATOR/ CHECKER WITH LATCH (IC'S 16,17,18,19,20,21,22,23,24).

EACH PART HAS ERROR DETECTING FEATURES WHICH GENERATE THE NOT ALL WELL MATRIX (NAWM) SIGNAL. A TEST OF THE ERROR DETECTION IS PERFORMED BY SENDING FALSE PARITY FROM THE CPU VIA THE I/O BUS. FALSE ADDRESS PARITY IS DETECTED BY IC15 WHICH IN TURN DISABLES ONE HALF OF THE DUPLICATED ONE OUT OF SIXTEEN DECODERS (IC'S 9,10). THIS IS DETECTED BY ITS ASSOCIATED MATCHER, IC13 AND IC14, WHICH IN TURN DISABLES ONE HALF OF THE DUPLICATED BOARD ENABLE DECODER IC2. THE OUTPUT OF IC2 GENERATES THE NAWM SIGNAL VIA IC4.

FALSE DATA PARITY IS DETECTED BY IC21 AND IC22 AND GENERATES A NAWM VIA IC5 AND COLLECTOR ORED IC4.