SHEET INDEX

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SYMBOL

BUFFER A

ELEMENT IDENT

A

TERM. MOD	FUNCT	TERM.	LOC	TERM. MOD	FUNCT	TERM.	LOC
ACKIO	I	308	2A7	INF120	Ø	213	3H7
BLK.CBRI	I	005	3A8	INF130	Ø	306	3H9
BRFLO	I	207	3A9	INF140	Ø	206	3H9
BRO	I	004	2A8	INF150	Ø	300	3H2
BUSYO	I	302	2A1	INTPO	Ø	017	2H8
CLK	I	305	2A7	LDITR1	Ø	203	3H5
GPRO	I	C19	2A6	LØADO	Ø	215	3H7
IACTO	I	208	3A9	MRSTA1	Ø	204	3H0
INF000	I	013	2A1	RDYO	Ø	205	2H0
INF010	I	113	2A1	RT.ADRA0	Ø	003	2H5
INF020	I	014	2A1	RT.ADRB0	Ø	100	2H6
INF030	I	114	2A1	RT.ADRC0	Ø	002	2H6
INF040	I	012	2A1	ST.CLK0	Ø	108	2H1
INF050	I	112	2A0	STUFF0	Ø	212	3H6
INF090	I	217	3A7	SWB1	Ø	009	3H4
INF100	I	216	3A7	SYNC0	Ø	103	2H2
INF110	I	011	3A6	TG.SEQ1	Ø	010	3H5
INF120	I	313	3A6	UNLØADO	Ø	209	3H6
INF130	I	007	3A0	WAIT0	Ø	015	2H4
INF140	I	106	3A0	+5	P	000,119	2H2
INF150	I	006	3A0	GRD	G	200,319	2H4
INITO	I	107	2A1				
LDPCKD0	I	318	2A6				
PE1	I	001	2A0				
RC0	I	118	2A2				
RD0	I	115	2A3				
SD0	I	018	2A2				
SL.0	I	116	2A3				
STFILL0	I	104	3A2				
C.BRT	Ø	105	3H9				
CLC01	Ø	309	3H1				
CLC11	Ø	008	3H1				
CSTC1	Ø	111	3H4				
DV.FILL1	Ø	110	3H0				
ENDT0	Ø	109	3H5				
ER0	Ø	304	2H0				
GP0	Ø	117	2H6				
IDEN0	Ø	016	2H8				
INF060	Ø	101	3H3				
INF070	Ø	102	3H3				
INF080	Ø	201	3H2				
INF090	Ø	315	3H8				
INF100	Ø	314	3H8				
INF110	Ø	214	3H8				

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEMS USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN: 340mA

NOTES:

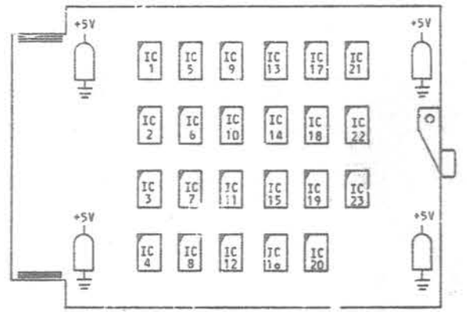
1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
41AE	16	7,8
41BP	16	8
41BR	16	7,8
41CA	16	8
41CD	16	8
41CF	16	7,8
41CK	16	8
41EG	16	7,8
41EH	16	7,8
41U	16	8
41W	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.
6. INTEGRATED CIRCUIT LOCATION GUIDE: (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

DWG ISSUE	ICE OR CD ISSUED	DATE ISSUE	DRAWN	APPD
1	—	10-8-74	L.R.E. LRE	RNF MTS RFG
2D1	—	12-9-75	P/S LRE	CE LEG RFG

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK10
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE.	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

ISSUE 2D1

1N98

JK10 CIRCUIT PACK

BUFFER A CIRCUIT

(2)

AT&TCO STANDARD

CPS-JK10

4 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

6S

PART OF CPS JKIO

BUFFER A

PE1 001 · INFO50 112 · INFO40 012 · INFO30 114 · INFO20 014 · INFO10 113 · INFO00 013 · INITO 107 · RCO 118 · SDO 018 · RDO 115 · SSTO 116 · BUSYO 302 · GPRO 019 · LDPCK00 318 · CLK 305 · ACKIO 308 · BRO 004

PE0 IC12 41BP E · INFO51 IC21 41EG D · INFO41 IC21 41EG A · R1 1.4KΩ · +5

0.36CD1 IC17 41CK A (STROBE, D1 D0 D2 D3 D4 D5 D6 D7)

CLEARO IC20 41EH D · CLEARC 3C · RC1 IC5 41BP B · SD1 IC5 41BP F · RD1 IC5 41BP E · SST1 IC5 41BP C · BUSY1 IC11 41BP E · BUSY1 3F4

E.SST1 IC5 41BP D · GPR1 IC5 41BP A · GP.RSO IC5 41BP G · EDCLK1 IC21 41EG B · STP.WTO IC9 41U A · R4 1.4K · CLKO IC7 41BP C · ACKI1 IC7 41BP F · BR1 IC12 41BP G · BR1 3F3

3E8 H1 · ADDRO IC23 41AE B · NC · E.RCO IC13 41U D · E.SDO IC13 41U C · E.RDO IC13 41U A · E.SSTO IC9 41U C · BF.WTO IC13 41U B · READY1 IC11 41BP D · GP.WTO IC9 41U C · DLYCLK1A IC19 41AE B · CLK1 IC7 41BP E · DLYCLK1B IC19 41AE A · R3 1KΩ · +5

BF.RDYO IC12 41BP F · 3F7 · ITP.#FF1 · INTP1 IC22 41BR B

PARITY1 IC12 41BP D · PARITY1 3F3

ER1 IC14 41U C · RDY1 IC20 41EH A · E.RCO 3B1 · SYNC1 IC18 41W A · E.SDO 3F5 · E.RDO 3F5 · WAIT1 IC9 41U B · READY1 3D2 · STATUS1B IC7 41BP A · STATUS1A IC7 41BP G · IDEN1 IC21 41EG C · R2 1.4KΩ · BK.XTPO 3F6

3E0 BLK.WTO · STATUS1B 3E9 · WAITO 3C0

ERO IC3 41CA C · RDYO IC3 41CA B · SYNCO IC8 41CA A · WAITO IC1 41CA C · RT.ADRAO IC8 41CA D · RT.ADRBO IC8 41CA C · RT.ADRCO IC8 41CA B · GPO IC1 41CA A · IDENO IC1 41CA B · INTPO IC1 41CA D

C1 5 · C2 5 · C3 5 · C4 5

C5 0.1 · C6 0.1 · C7 0.1 · (C8-C26) 0.1 · C27 0.1

STATUS1A 3F3

ERO 304 · RDYO 205 · S*.CLKO 108 · SYNCO 103 · 000, 119 · +5 · GRD 300, 314 · WAITO 015 · RT.ADRAO 003 · RT.ADRBO 100 · RT.ADRCO 002 · GPO 117 · IDENO 016 · INTPO 017

ISSUE 2D1

JK10 CIRCUIT PACK (2)

BELL TELEPHONE LABORATORIES INCORPORATED

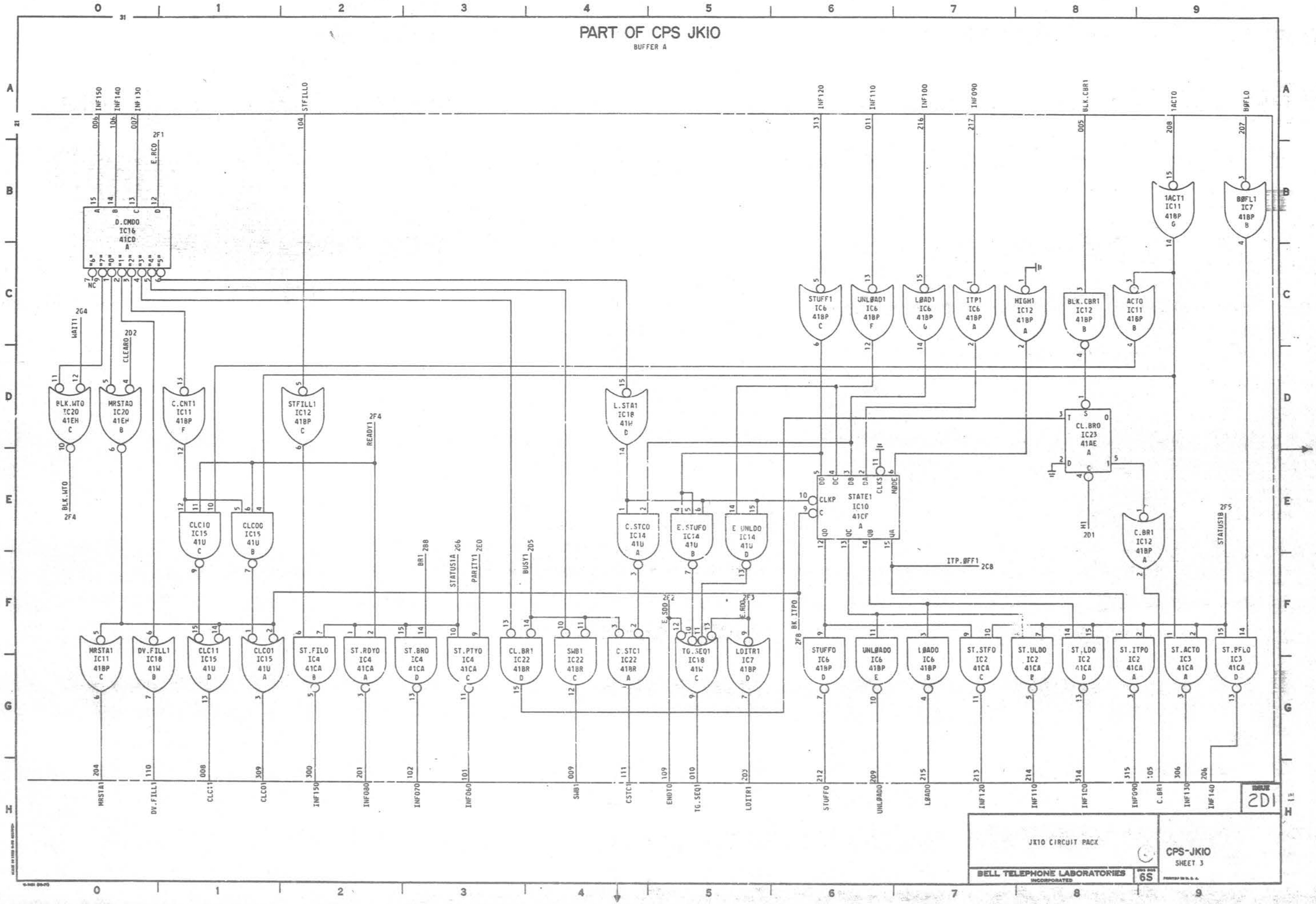
CPS-JK10 SHEET 2

SIZE 6S

CPS-JK10

PART OF CPS JK10

BUFFER A



JK10 CIRCUIT PACK	CPS-JK10 SHEET 3
BELL TELEPHONE LABORATORIES INCORPORATED	6S

CPS-JK10

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41CA DESIG	SH LOC	IC2 41CA DESIG	SH LOC	IC3 41CA DESIG	SH LOC	IC4 41CA DESIG	SH LOC	IC5 41BP DESIG	SH LOC	IC6 41BP DESIG	SH LOC	IC7 41BP DESIG	SH LOC	IC8 41CA DESIG	SH LOC	IC9 41U DESIG	SH LOC	IC10 41CF DESIG	SH LOC	IC11 41BP DESIG	SH LOC	IC12 41BP DESIG	SH LOC
A	GPO	2G6	ST.ITPO	3G8	ST.ACTO	3G9	ST.RDYO	3G2	GPR1	2B6	ITP1	3C7	STATUS1B	2F5	SYNCO	2G2	STP.WTO	2C6	STATE1	3E6	HIGH1	3C8	C.BR1	3E9
B	IDENO	2G8	ST.STFO	3G7	ERO	2G0	ST.PTYO	3G3	RC1	2C2	L@AD0	3G7	B@FL1	3B9	RT.ADRCO	2G6	WAIT1	2F4			ACT0	3C9	BLK.CBR1	3C8
C	WAITO	2G4	ST.LDO	3G8	ERO	2G0	ST.BRO	3G3	SST1	2C3	STUFF1	3C6	CLKO	2C7	RT.ADRBO	2G6	E.SST0	2D3			MRSTA1	3G0	STFILL1	3C2
D	INTPO	2G8	ST.BFLO	3G9	ST.BRO	3G3			E.SST1	2C5	STUFF0	3G6	LDITR1	3G5	RT.ADRAO	2G5	GP.WTO	2D5			READY1	2D4	PARITY	2D0
E									RD1	2C3	UNL@AD0	3G6	CLK1	2D7							BUSY1	2C4	PEO	2B0
F									SD1	2C2	UNL@AD1	3C6	ACKI1	2B7							C.CNT1	3D1	BF.RDYO	2C8
G									GP.RSO	2C6	L@AD1	3C7	STATUS1A	2F5							1ACT1	3B9	BR1	2B8

LOC CODE ELEM ID	IC13 41U DESIG	SH LOC	IC14 41U DESIG	SH LOC	IC15 41U DESIG	SH LOC	IC16 41CD DESIG	SH LOC	IC17 41CK DESIG	SH LOC	IC18 41W DESIG	SH LOC	IC19 41AE DESIG	SH LOC	IC20 41EH DESIG	SH LOC	IC21 41EG DESIG	SH LOC	IC22 41BR DESIG	SH LOC	IC23 41AE DESIG	SH LOC
A	E.RDO	2G3	C.STCO	3E4	CLCO1	3G1	D.CMDO	3B0	D.36CD1	2C1	SYNC1	2F2	DLYCLK1B	2E6	RD@1	2F0	INFO4:	2B1	C.STC1	3G4	CL.BRO	3B3
B	BF.WTO	2D4	E.STUFO	3E5	CLCO0	3E1					DV.FILL1	3G0	DLYCLK1A	2D6	MRSTA0	3D0	EDCLK1	2B6	INTP1	2D8	ADDRO	2D1
C	E.SDO	2D3	ER1	2F0	CLC10	3G1					TG.SEQ1	3G5			BLK WTO	3D0	TDEN1	2F8	SWB1	3G4		
D	E.RCO	2G2	E.UNLDO	3E5	CLC11	3G1					L.STA1	3D4			CLEARO	2C2	INFO51	2B0	CL.BR1	3G3		
E																						
F																						
G																						

CAPACITOR

DESIG	CODE
[4] C1-C4	6014,5
[23] C5-C27	KS-19774 L5,0.1

RESISTOR

DESIG	CODE
[2] R1,R2	KS-20616 L1A,1.4KΩ
R3	KS-20616 L1A,1KΩ
R4	KS-20616 L1A,1.4KΩ

CIRCUIT DESCRIPTION

CIRCUIT PACK JK10 HANDLES THE BUFFER ADDRESS AND COMMAND DECODING AND HANDSHAKING ON THE COMMON PARALLEL BUS. BUFFER ADDRESS 00T011 APPEARING ON BUS LEADS INF000-INF050 IS DECODED BY D.36CD1 CAUSING THE ADDRESS F/F ADDRO TO BE CLEARED ON THE LEADING EDGE OF RCO, SELECTING THE BUFFER AND ENABLING COMMAND INPUTS SDO, RDO AND SSTO AS WELL AS THE ERO OUTPUT. THE BUFFER IS DESELECTED (ADDRO IS SET) EITHER BY INITO OR BY AN RC ACCOMPANYING A NONBUFFER DEVICE CODE. AN ADDRESSED CIRCUIT RETURNS SYNCO IN RESPONSE TO RCO, SDO, RDO, OR SSTO AND NEGATES SYNCO FOLLOWING THE REMOVAL OF THE COMMAND SIGNAL. ERO IS ASSERTED BY RCO AND IS HELD TRUE BY A PARITY ERROR INDICATION (PE1 TRUE).

THE RECEPTION OF AN SSTO (ITES STATUS INFORMATION ONTO THE BUS AND ASSERTS WAITO AND PARITY GENERATE REQUEST GPO IN ADDITION TO SYNCO. THE NEXT FALLING EDGE OF CLK SETS DLYCLK1A AND THE FOLLOWING RISING EDGE SETS DLYCLK1B, CUTTING OFF GPO. THE PARITY GENERATION CIRCUITS IN THE BUS TERMINATOR RESPOND BY ASSERTING GPRO WHICH REMOVES STATUS INFORMATION FROM THE BUS AND INHIBITS THE BUFFER WAITO. THE DELAY CHAIN IS CLEARED WHEN SSTO IS REMOVED.

RDO CLOCKS INFORMATION ON THE PARALLEL BUS INTO THE INTERMEDIATE TRANSFER REGISTER, ITR, ON JK12 VIA LEAD LDITR1. SDO GATES THE ITR ONTO THE BUS VIA LEAD ENDTO.

WAITO IS ASSERTED WHEN BUSYO IS ACTIVE AND THE BUFFER IS SELECTED BUT MAY BE BLOCKED AT GATE BLK.WTO BY COMMAND DECODER (D.CMDO) OUTPUT 7. INTPO IS ASSERTED WHEN BRO IS ACTIVE AND THE STATE REGISTER ITP.@FF BIT IS NOT SET. AN INTERRUPT CONDITION ENABLES BUFFER INTERRUPT IDENTIFICATION GATE IDENO IN RESPONSE TO AN ACK10 COMMAND.

D.CMDO DECODES THE INFORMATION ON INF130-INF150 WHEN RCO IS ON TO ACTIVATE 1 OUT OF 8 DECODER OUTPUTS. OUTPUT 7 PREVIOUSLY MENTIONED IS USED IN CONNECTION WITH A MOP COMMAND.

OUTPUT 5 CLOCKS THE BIT PATTERN ON LEADS INF090-INF120 INTO THE 4-BIT STATE REGISTER STATE1. THE STATE REGISTER CONTROLS THE STATES OF LEADS STUFF0, UNL@AD0, L@AD0, INT.@FF1 WHICH INDICATE THE TYPE OF OPERATION TO BE PERFORMED ON THE OFF-LINE BUFFER. OUTPUT 4 ASSERTS SWB1, TOGGLING THE ACT F/F ON JK11 AND EFFECTING A BUFFER SWITCH. OUTPUT 3 CLOCKS THE CL.BR0 F/F WHICH ASSERTS C.BR1, CLEARING THE BR FLAG ON JK11. CL.BR0 F/F MAY BE HELD SET BY AN ACTIVE LEVEL ON BLK.CBR1. OUTPUT 2 ASSERTS EITHER CLC11 OR CLC01 TO CLEAR THE BUFFER COUNTER INDICATED BY THE STATE OF 1ACT0. OUTPUT 1 ASSERTS DV.FILL1 RESULTING IN A CC-INITIATED ON-LINE BUFFER FILL OPERATION. OUTPUT 0 PERFORMS BUFFER INITIALIZATION (AS DOES LEAD INITO) BY RESETTING STATE1, CLEARING BOTH ON-LINE AND OFF-LINE BUFFER COUNTERS VIA CLC01 AND CLC11, AND ASSERTING MRSTA1. OUTPUT 6 OF D.CMDO IS NOT USED.

CSTC1 CLEARS THE STUFF SEQUENCE COUNTER IN JK11 WHILE THE L@AD BIT IN THE STATE REGISTER IS BEING SET. TG.SEQ1 STARTS OFF-LINE SEQUENCING ON JK11 IF EITHER THE STATE REGISTER STUFF OR UNLOAD BIT IS BEING SET OR IF RDO OR SDO IS ACTIVE.

D.CMDO TRUTH TABLE
(ASSUME E.RCO ACTIVE)

INF150	INF140	INF130	ASSERTED DECODER OUTPUT
0	0	0	7
0	0	1	3
0	1	0	5
0	1	1	1
1	0	0	6
1	0	1	2
1	1	0	4
1	1	1	0

2D1

JK10 CIRCUIT PACK (2)

CPS-JK10
SHEET 4

BELL TELEPHONE LABORATORIES INCORPORATED 6S

CPS-JK10