5ESS® SWITCHING SYSTEMS
DIGITAL SERVICE UNIT
MODEL 3
CIRCUIT

Description of Changes

1. This Change is being written to correct errors in SD-5D197-01 Sheets G6, G7, G10, G13, and G16. This change is a documentation change only and does not affect the manufactured product.

2. The slot identification labeling which references each circuit pack slot is identified incorrectly on Sheet G6. It reads "(SLOTB1)CP", it should read "(SLOTB2)CP".

3. The PICB and PIDB cable termination points (if required) for each circuit pack are determined by each installation. Sheets G7, G10, G13, and G16 depict actual termination points in the SMPU or TSIU. These points are being relabeled to depict generic termination.

AT&T

DEPT NA53503000-FJS-CEJ

5ESS® SWITCHING SYSTEMS
DIGITAL SERVICE UNIT
MODEL 3
CIRCUIT

CONTENTS

LIST OF FIGURES

1. GENERAL DESCRIPTION

1.1 PURPOSE OF CIRCUIT

The Digital Service Unit, Model 3 (DSU3) houses the Digital Service Circuit 3 (DSC3). Up to eighteen DSC3s can be installed into the DSU3 shelf. (See *Figure 1.*) The DSU3 provides switching services such as tone generation and touch-tone decoding, which have been traditionally performed by analog circuits. However, the DSU3 operates in a digital environment, as did the DSU1 and DSU2. The new shelf, in future development, will also house the new memory boards for Recorded Announcements and other functions for the 5ESS Switching Module 2000 (SM-2000). Presently, in the 5EE6 generic, the DSU3 will only house the DSC3 circuit pack (UN363).

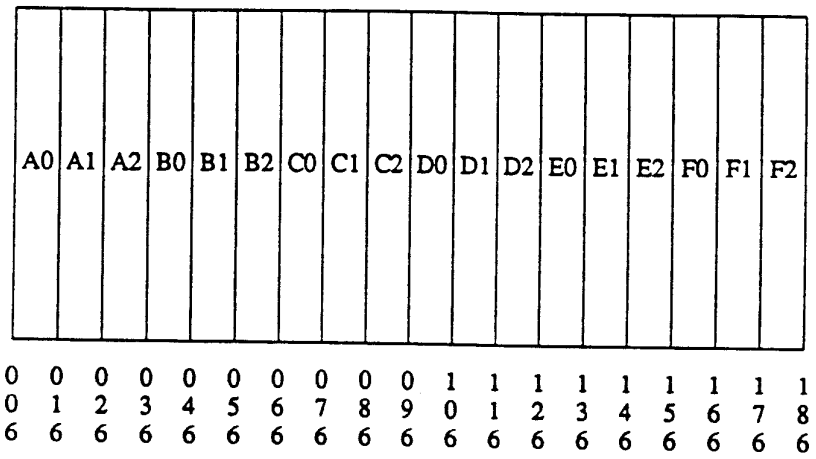


Figure 1. Digital Service Unit, Model 3 (DSU3).

1.2 GENERAL DESCRIPTION OF OPERATION

The DSU3 can have several variations of DSC3s and memory boards installed within the shelf. When a multi-DSC3 configuration is desired, only the primary DSC3 will be equipped with Peripheral Interface Data Buses (PIDBs). When a DSC3 memory board configuration is desired, each slot will have the parallel bus for memory boards daisy-chained to the next slot. Therefore, memory boards are always grown to the right of a DSC3.

The DSC3 will be used in the SM-2000 Release 1 to provide the Local Digital Service Functions (LDSF). The DSC3 has an Intel 80C186 for local control, ten DSP32C-M4s for high speed processing of input Pulse Code Modulation (PCM) data, Rate Adapt for PIDB data conversions, Unified Control Interface (UCI) for control interface, and a DSN16 for the Digital Signal Processor (DSP) network. See the DSC3 circuit description and/or Hardware/Software Interface (HSI) document for general description of operation of the DSC3.

Note: Inter-DSC3 Communication, Memory boards, and several variations of DSC3s and memory boards is being done as a platform for future features.

2. DETAILED DESCRIPTION

2.1 INTERCONNECTIONS

The interconnections of the DSU3 are such that when multi-DSC3 configurations are desired, the primary DSC3 will supply the secondary DSC3(s) with a differential 16 MHz clock, frame sync signal, and PCM data. Also, as shown in *Figure 2*, the common memory data bus and control signals are interconnected from one slot to the next adjacent slot for DSC3 memory board desired configurations.

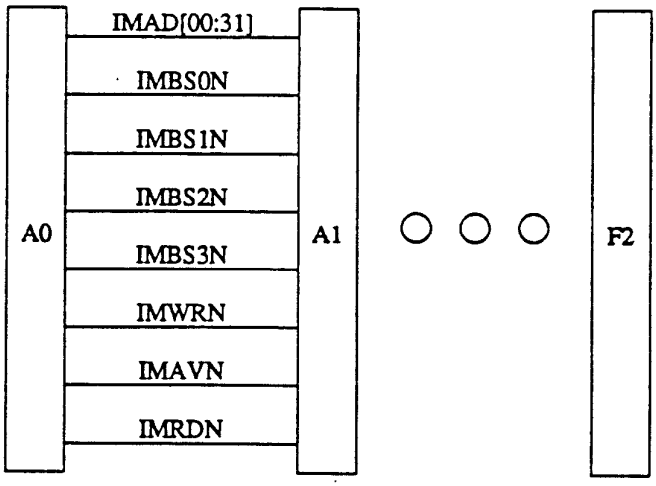


Figure 2. DSU3 Backplane Interconnections For Common Memory.

Note: In an effort to clear up any confusion about the serial PCM data paths (SDIN and SDOUT), *Figure 3* illustrates that SDOUT goes to SDIN of another slot within that fuse group, but the schematic (B-Sheets) only shows SDIN from one slot to SDIN of another slot in the same fuse group. This was done in the schematic for routing and connectivity purposes in order to connect the slots. The DSC3 has SDIN and SDOUT signals.

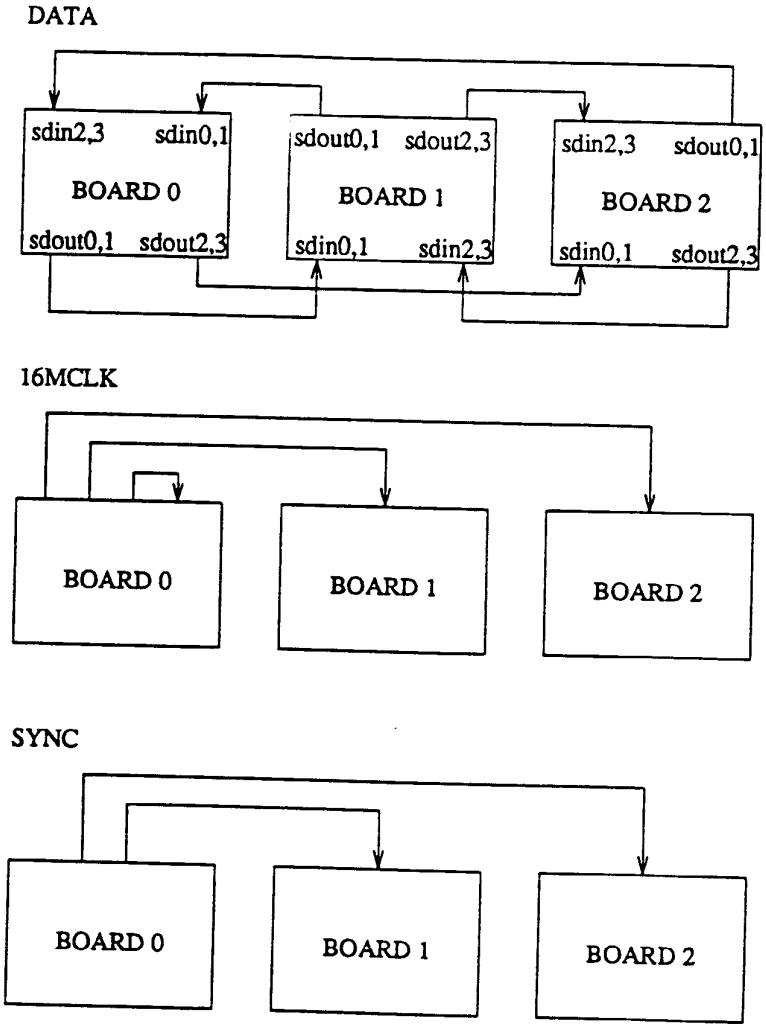
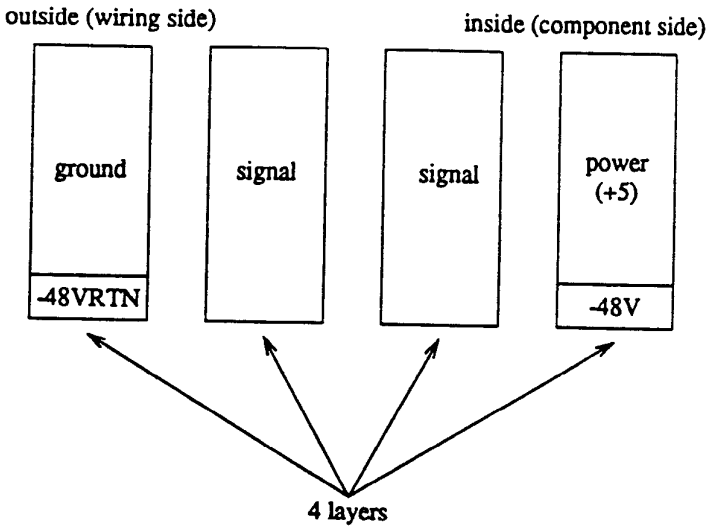


Figure 3. DSU3 Backplane Interconnections.

2.2 BACKPLANE

The backplane has four layers [ground, signal, signal, power (+5)], as illustrated in *Figure 4*. The power layer is inside for heat dissipation reasons, and the ground layer is outside for ElectroMagnetic Compatibility (EMC) reasons. The backplane is divided into six fuse groups; each fuse has three slots. The backplane is segmented such that the lower section of each fuse group contains two power lugs, which supply the incoming power: -48V and -48VRTN. The DSC3 uses the incoming power (-48V and -48VRTN), and the on-board power module converts it to an outgoing +5 voltage. The power layer is supplied a +5 voltage from the on-board power module. All pins in the backplane are gold tipped on both ends. On the component side (or pack side) the power and power return pins are elongated to provide power sequencing.



Notes:
1. Pins 101, 201, 301, 401 on component side are .750" in length (-48VRTN).
2. Pin 100 on component side is .700" in length (-48V).
3. All other pins on component side are .650" in length.
4. All pins on wiring side are .700" in legnth.
5. All pins will be gold tipped on both ends.
6. The power layer is inside for heat dissipation reasons.

Figure 4. DSU3 Backplane Layers.

3. REFERENCE DATA

3.1 CONNECTING CIRCUITS

As illustrated in *Figure 5*, the DSU3 is connected to the following units:

- Switch Module Processor Unit (SMPU), connected via PICBs to the CI pack in the SMPU for the purpose of sending control messages from the SMP to the DSC3, and
- Time Slot Interchange Unit (TSIU), connected via PIDBs to the DX pack in the TSIU for the purpose of sending and receiving serial data, and for sending a 4.096 MHz clock and 8 KHz frame sync signal from the TSI to the DSC3.

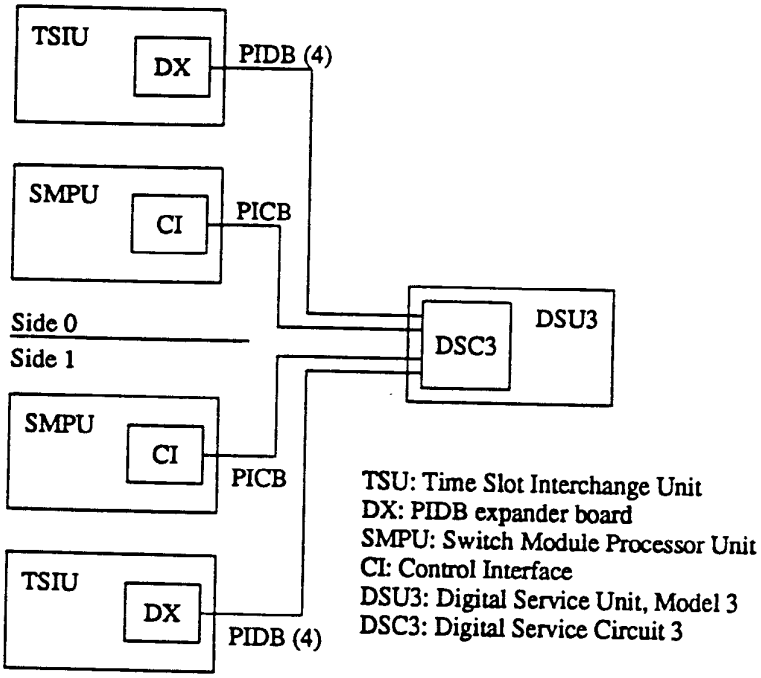


Figure 5. Unit Connections.

3.2 WORKING LIMITS

Voltage:

- Static voltage: -42.75v to -52.5v
- Transient voltage: -39.5 to -60.0v

Current:

- Static and Transient current: The total current draw for a fuse group shall not exceed the specifications for a 10 Amp - fast acting fuse (Comcode: 406559324, WP-91768-L11).

Temperature:

- 0° C to 50° C (office aisle ambient)
- 0° C to 70° C (at circuit pack)

3.3 ACRONYMS

C	Celsius
CI	Control Interface
DSC3	Digital Service Circuit 3
DSN16	Digital Signal Processor Switching Network 16
DSP	Digital Signal Processor
DSU1	Digital Service Unit, Model 1
DSU2	Digital Service Unit, Model 2
DSU3	Digital Service Unit, Model 3
DX	PIDB expander board
EMC	ElectroMagnetic Compatibility
FPGA	Field Programmable Gate Array
HSI	Hardware/Software Interface
KHz	Kilohertz
LDSF	Local Digital Service Function
MHz	Megahertz
PCM	Pulse Code Modulation
PICB	Peripheral Interface Control Bus
PIDB	Peripheral Interface Data Bus
SMP	Switch Module Processor
TSI	Time Slot Interchange
UCI	Unified Control Interface

AT&T BELL LABORATORIES

DEPT 55535-FS-CEJ