5ESS® SWITCHING EQUIPMENT
MESSAGE SWITCH PERIPHERAL UNIT
CIRCUIT

CHANGES

D. Description of Changes

Added TN1800 (N option) which provides the communication module processor (CMP) with 20 Mbyte of memory to be used in software release 5E9 or later.

AT&T BELL LABORATORIES

DEPT NA5301700-HVT-SDS

5ESS® SWITCHING EQUIPMENT
MESSAGE SWITCH PERIPHERAL UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Added Circuit Note 104 to specify current rating of MSPU fuse.

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DEPT NFNW260570-HVT-SDS

5ESS® SWITCHING EQUIPMENT
MESSAGE SWITCH PERIPHERAL UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Incorporate new feature - Communication Module Processor (CMP). The Communication Module Processor (CMP) consists of a core board and a memory board. The CMP resides in Message Switch Peripheral Unit (MSPU) Community 1 along with the Pump Peripheral Controller (PPC) and Foundation Peripheral Controller (FPC). The Message Switch Control Unit (MSCU) accesses the CMP, via the Input / Output Microprocessor Interface (IOMI), through dual access memory located in the CMP. The function of the CMP is to provide Recent Change response time and Administrative Module (AM) memory relief by migrating the Recent Change and associated data base functions from the AM to the CMP.

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DEPT 55423-SJL-PEW

5ESS™ SWITCHING EQUIPMENT
MESSAGE SWITCH PERIPHERAL UNIT
CIRCUIT

CHANGES

D. Description of Changes

D.1 Added MC5D066A1B (R option) which is generically equivalent to MC5D066A1 (S option). Offices which are running on the MC5D066A1 need not replace them with the MC5D066A1B. These two microcodes can be mixed within a system or unit.

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DEPT 55612-CJW-SJL

5ESS™ SWITCHING EQUIPMENT
MESSAGE SWITCH PERIPHERAL UNIT
CIRCUIT

SECTION I - DETAILED DESCRIPTION

1. MESSAGE SWITCH PERIPHERAL PROCESSOR (MSPP) HARDWARE DESCRIPTION

1.01 The MSPP (TN856) is the common controlling circuit pack for all Message Switch (MSG) Peripheral Controller (PC) applications (MMP, FPC, and PPC). This circuit board is a single board processor which interfaces to other application boards for particular PC functions. The MSPP interfaces to the MSCU via an IOMI bus. The MSPP has a 16-bit microprocessor with 128K bytes of Dynamic Random Access Memory (RAM), 8K bytes of static RAM, 16K bytes of Erasable Programmable Read Only Memory (EPROM), error detection circuits, and clock circuits to ensure its own sanity as well as to provide timing to other application boards. The interface to the application boards supports either 8- or 16-bit peripherals. Across this bus, the MSPP performs parity generation and checking functions for both the data bus and the address bus. Direct Memory Access (DMA) operations are supported across this bus, allowing efficient data transfers without processor involvement.

2. MODULE MESSAGE PROCESSOR (MMP) HARDWARE DESCRIPTION

2.01 An MMP consists of up to four boards. These circuit boards are the MSPP (TN856) as described in Section 1.01, the Module Message Processor 1 circuit board (UN170) and one or two Module Message Processor 2 (A,B) circuit boards (TN858A and TN858B). The MMPs function is to process control messages between the IMs (via the MICU and TMS) and the MSCU.

Data transmission between the MICU and the MMPs is bidirectional and full duplex. Transmission is done over the Message Interface Buses (MIB). These MIBs are cross-coupled for reliability. This cross-couple is implemented by running MIBs from both of the duplicated MICUs to each MMP. Which MIB each MMP selects is a programmable option.

Each MMP supports up to eight fixed control time slots. An MSPU

holds a community of four MMPs supporting up to 32 control time slots per community. For reliability, each control time slot in a community is allocated to a different IM. Because each IM uses 2 control time slots per simplex MSG, the two MSPU communities (MSPU community 2 and MSPU community 3) can service a combination of up to 32 IMs and RSMs. Of the 32 control time slots on the MIB, the MMP will then select eight for processing. Data between the MMPs and the Interface Module Processors (IMPs) in the IMs have a protocol (BX.25 level 2) appended to the control messages. This protocol ensures data integrity over the transmission. At the IMPs and the MMPs are circuits designed to remove or append this protocol.

2.02 MMP1 H/W Description

2.03 The MMP1 (UN170) is the MIB interface board for the MMPs. The MMP1 circuit board contains three interrupt controllers, a master DMA controller, six registers, and parity generation circuitry. This board performs the following basic functions:

1. Generation of timing signals which control serial data transfer between MMP1 and the MICU via the MIB. Other timing signals control serial data parity checking and generation.

2. Generation of interrupt control vectors to the MSPP microprocessor following interrupt requests generated by MMP1 and MMP2.

3. Control of MSPP microprocessor bus access to enable DMA data transfer between MMP2 and memory.

4. Selection of active MIB.

5. Selection of time slots from either MIB.

6. Parity checking of serial data, parallel data, and address signals.

2.04 In offices that are being equipped with Remote Switching Modules (RSMs), the MMPs must utilize the UN170B circuit board. Otherwise, RSM capability will not be achieved for the system. The UN170B can also be used with local IMs.

2.05 MMP2 H/W Description

2.06 The MMP2 (TN858) is the High-Level Data Link Controller (HDLC) board for the MMPs. Each MMP2 circuit pack handles 4 control time slots which allows an MMP with 2 TN858s to handle 8 control time slots. The MMP2 board has two slave DMA controllers, four HDLCs, three registers and parity circuitry in order to perform the following functions:

1. Demultiplexing of four time slots received from MMP1.

2. Disassembly and error checking of the received time-slot frames.

3. Transfer of the information field of the received time-slot frame to MSPP dynamic RAM, under DMA control.

4. Transfer of data from MSPP dynamic RAM to the information field of the transmitted time slot under DMA control.

5. Assembly of the transmitted time-slot frames.

6. Multiplexing of four time slots and transmission to MMP1.

7. Parity checking of serial data, parallel data, and address signals.

3. FOUNDATION PERIPHERAL CONTROLLER (FPC) HARDWARE DESCRIPTION

3.01 The FPC consists of an MSPP (TN856) circuit pack as described in Section 1.01 and a FPC4 (UN173) circuit pack. FPC4 consists of an interrupt controller, Control and Diagnostic Access Circuit (CDAC), and parity generation circuit to perform the following functions:

1. Generation of interrupt control vectors to the MSPP microprocessor.

2. Selection of active CDAL.

3. Transmission and reception of control and status information over the CDAL to/from the MICU.

The FPC is used to control the configuration of the MICU as well as to control the Time Multiplexed Switch (TMS). These messages are initiated by the CP through the MSCU and are sent to the FPC. From there, via the CDAL, the MICU and TMS are controlled. The FPC also interfaces to the MSCU via an IOMI bus.

The FPCs are cross-coupled to both MICUs for reliability. The FPC under direction of CP software controls the configuration of the hardware in the MICUs, including the Message Interface (MI) boards, the Link Interface (LI) boards, and the Network Clock (NCLK) boards.

The FPC also issues time-slot path setup requests to the TMS on command from the CP. Diagnostics on most of the MICU hardware are executed directly in the FPC. Some of the NCLK diagnostic is executed in the NCLK. The FPC sends the requests to execute this diagnostic. Diagnostic requests are sent to the TMS from the FPC to activate the execution of TMS diagnostics.

4. PUMP PERIPHERAL CONTROLLER (PPC) HARDWARE DESCRIPTION

4.01 The PPC consists of an MSPP (TN856) circuit pack as described in Section 1.01 and a PPC1 (TN886) circuit pack. The PPC1 performs the following basic functions:

1. A pair of 4K byte RAM buffers temporarily store blocks of data written by the MSPP.

2. An 11-bit word counter generates the RAM buffer address during reads (transmissions to the interface module). An address multiplexer switches the source of the RAM buffers address from the address counter to the processors address bus.

3. A data formatting circuit converts the 16-bit words read from the RAM buffer to 8-bit time slots. Each time slot contains six data bits, a framing bit, and a parity bit.

4. An 8-bit time-slot counter has two functions: the counting of the 8 bits per time slot and the counting of the 32 time slots per frame.

5. The output data circuit contains a multiplexer that switches idle code or data to the output. A shift register converts the parallel data to serial data which is outputted on the MIB at 2 MHz rate.

6. Time slot selection is accomplished by a 32-by-1-bit RAM. Each bit corresponds to one of the 32 time slots and is used to determine which of the time slots will be used for data transmission during IM pump.

7. Diagnostic circuits check data parity, address parity, data formatting, and the time slot select RAM.

The PPC interfaces to the MICU via an MIB. Although the MIB provides a serial path for data transmission in both directions, the PPC transmits only towards the IMs. The return path is used for diagnostic loop-around capabilities. The PPC also interfaces to the MSCU via the IOMI bus.

The PPC is used to quickly initialize the IM memory. PPC uses 6 bits each of up to 32 control time slots to deliver data to an IM at a rate of 1.536 Mb/s. Also this data is pumped to the IMs through the MSCU to the PPC in 2K byte blocks. The PPC then sends the data through the MICU via an MIB bus to the TMS where it is distributed to the destination IM.

The PPC are cross-coupled to both MICUs over separate MIBs. Data can be sent to the IMs from either PPC through either TMS half. Duplication of the PPC is for reliability.

4.02 MSPU Power and Control/Display

4.03 Each MSPU is provided with a separate power converter (495FB) and a Control and Display (C/D) circuit pack (SN412). This allows the flexibility of powering down the MSPU without affecting the other units. The status of the power supply is reported to the CP by the MSCU. Also the control and display pack reports the power status via duplicated scan points in the Input Output Processor (IOP). The C/D duplicated scan and distribute cables are cross-coupled to ensure reliability.

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