

COMMON SYSTEMS  
3B20D MODEL 2 AND 3 PROCESSOR  
PROCESSOR SYSTEM CABINET  
FOR 5ESS®

CHANGES

*D. Description of Changes*

For the model 2 and 3 processors:

Added apparatus figure 107 which adds UN33C scanner signal distributor (SCSD).

Added apparatus figure 108 which adds MC4C052A1C (TN82B) BX.25 high speed data link controller.

Added apparatus figure 109 which adds MC4C052A1D (TN82B) BX.25 high speed data link controller.

Added apparatus figure 110 which adds UN33D SCSD.

Added apparatus figure 111 which adds UN52B 1600 BPI high speed tape.

Added apparatus figure 112 which adds MC4C052A1E (TN82B) BX.25 high speed data link controller.

Added apparatus figure 114 which adds TN1839 two channel synchronous link (for Network Systems International [NSI] applications only).

Added apparatus figure 115 which adds TN1420 BX.25 high speed (64KBPS) data link controller.

*E. Reason for Changes*

Added apparatus figures 107, 108, 109, 110, and 111 to the "Apparatus Figure Summary" to bring the schematic drawing (SD) into agreement with J4C176B-1.

Added apparatus figures 112, 113, and 114 to the "Apparatus Figure Summary" for three new circuit packs (CPs).

AT&T BELL LABORATORIES

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

This circuit provides processor system configurations for the 3B20D Model 2 and 3B Processor for the 5ESS® Switch. Various fixed floor plans are provided depending on 3B20D Model and the disk

drive cabinet required in the application requirements.

Graphic information and cable interconnection information is presented in the schematic diagram (SD).

2. GENERAL DESCRIPTION OF OPERATION

The processor system is made up of a processor control cabinet and a tape/disk cabinet connected together to form the 3B20D for the 5ESS® Switch.

The description of the processor control cabinet is contained in CD-4C119-01.

The description of the tape/disk cabinet circuit is contained in CD-4C126-01.

SECTION II - DETAILED DESCRIPTION OF OPERATION

FS1 through FS6 provides a plan view of the fixed floor plan and an interconnection and flow diagram for each Model 2 or 3 3B20D Processor and the particular disk drive configuration required. Floor plans are provided for 300 Mb, 314 Mb disk drive, tape drive and Peripheral Interface Cabinet.

The following configurations are provided in FS1 through FS6.

FS1 - 3B20D Model 2 Processor (300Mb Disk Drive).

FS2 - 3B20D Model 2 Processor arranged to Retrofit Tape/Disk Cabinet (T/DC) (340 Mb Disk Drive 00-07).

FS3 - 3B20D Model 3 Processor Arranged with 340 Mb Disk Drive (00-03) and Tape Unit 0.

FS4 - 3B20D Model 3 Processor Arranged with 340 Mb Disk Drives (04-15) and Tape Unit 1.

FS5 - 3B20D Model 3 Processor Arranged with 340 Mb disk Drives (04-15).

FS6 - 3B20D Model 3 Processor Arranged with Peripheral Interface Cabinet (PIC).

### SECTION III - REFERENCE DATA

#### 1. WORKING LIMITS

None.

#### 2. FUNCTIONAL DESIGNATIONS

All symbols are identified by functional name and equipment Jcode (J1CXXX-1).

#### 3. FUNCTIONS

Provides the fixed floor plan configurations and cabling information for the 3B20D Model 2 and Model 3 processors with the various tape/disk and disk cabinets available.

#### 4. CONNECTING CIRCUITS

When this circuit is listed on a keysheet, connecting information thereon is to be followed.

All connecting information is provided in the SD-4C122-01.

### 5. MANUFACTURING TEST REQUIREMENTS

X-79516 Manufacturing Test Requirements for 3B20D Processor (Model 1, 2 and 3) covers the test requirements for the 3B20D Processor System.

### SECTION IV - REASONS FOR REISSUE

#### D.1 - Changes in Functional Schematics or Apparatus Figures

This reissue provides a new circuit description, and provides the information required to implement the Very Large Memory Module (VLMM). Apparatus Figures 501 - 519 and Notes 110, 111, 316, 317, 318, 319 were added to provide this information.

Apparatus Figures 224-229 were added to reflect the latest Tape Unit configurations available.

Notes 313-315 were changed and App. Fig. 451-454 were added to include the J1C215B-1 Peripheral Interface Cabinet (PIC).

Notes 306 and 306.3 were changed to reflect UN145B - MC4C160A1B, Note 104.4 was added to include the utilization of one UN145B controlling multiple tape drives.

Notes were changed to change KS22875,L14 disk designation to KS22875,L18 E/W L51 to reflect the vanilla disk drive ordering scheme.

D.2 - Description of Changes

Note: This reissue also covers information authorized by the following appendixes to Issue 9B of this CD:

APPX 1B	DWG ISS 2B
APPX 2B	DWG ISS 3B
APPX 3B	DWG ISS 4B
APPX 4A	DWG ISS 5A
APPX 5A	DWG ISS 6A
APPX 6AC	DWG ISS 7AC
APP 7B	DWG ISS 8B

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