

COMMON SYSTEMS  
 3B20D MODEL 2 & 3 PROCESSOR  
 I/O PROCESSOR BASIC UNIT  
 CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The 3B20D Input/Output Processor (IOP) provides a standardized peripheral and data link input/output interface for the 3B20D Processor.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The 3B20D IOP basic unit consists of a common 3B20D dual serial bus interface controller and two communities of single-board peripheral interfaces called Peripheral Controllers (PCs). Each community consists of four PCs, a common nine-bit data bus, and a sixteen-bit address bus. Eight control leads per community, for Direct Memory Access (DMA) operations, are also used. There are five signals, covering requests, errors, interrupts, selection, and acknowledgement for each PC.

SECTION II - DETAILED DESCRIPTION

1. IOP CONTROL INTERCONNECTION AND FLOW DIAGRAM - FS1

1.01 FS1 shows the interconnection of the Dual Duplex Serial Bus Selector (DDSBS) circuit pack with the Bus Interface Controller (BIC), the Trace Control Unit (TN60), the Micro Control Store (TN84), the Peripheral Controller Interface (PIC), and the

Input/Output Microprocessor Interface (IOMI). The DDSBS provides a duplex interface between the peripheral unit BIC and the Dual Serial Channel of the Central Control in units 0 and 1. The BIC buffers processor data and commands to the PIC, as well as data and status information from the PIC. It also performs the mandatory "handshaking" to communicate with the DDSBS. The PIC (TN61 and TN84) transfers data between internal registers and the various registers on the BIC and IOMI over a sixteen-bit data bus. The IOMI links the PIC to a maximum of four PC communities, with four PCs per community. Each community interface with IOMI has a sixteen-bit dual port memory address, an 8+1 parity bit bidirectional data bus, and eight control pulses. Also included are the Bus Terminating Resistor Assemblies (BTR1 and BTR2).

2. PERIPHERAL CONTROLLERS - COMMUNITY 0 AND 1 - FS2

2.01 FS2 contains the interconnection and flow information for the Peripheral Controllers. Community 0 contains the Maintenance TTY Controller (TN83B or TN983 circuit pack), and three UN33D circuit packs. Community 1 consists of four UN33D circuit packs.

3. POWER AND POWER CONTROL INTERCONNECTION AND FLOW DIAGRAM - FS3

3.01 The schematic for the IOP power is provided in FS3, which includes two 495FA converters, a 494GA power unit, a TN6 control unit, and two TN9 converters. The 495FA converter supplies +5 volts to the controller and the PCs, while the TN9s supply the EIA voltages +/-12 and +5 volts to the PCs. The 495FA converter is designed to be inserted or removed with -48 volts applied to the circuit.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The 3B20D IOP basic unit requires -48 volts (+/-10%) at approximately 9 amps. The +5 volt logic, supplied by a 495 power converter to the controller and the PC 0 communities, must be within +/-10%. Similarly, the +5 volt logic, supplied by the 494 power converter to the PC 1 communities, must be within +/-10%. The +12 and -5 memory voltages, supplied by TN9, must also be within +/-10%.

EIA voltages (+/-12 volts) from TN9 are monitored and must be greater than 4.5 volts in magnitude. A PC community will not power up without its associated TN9.

2. FUNCTIONAL DESIGNATION

2.01 Circuit Packs and Converters:

- (1) Power Switch
- (1) Dual Duplex Serial Bus Selector - TN69
- (1) Bus Interface Controller - TN70
- (2) Microcontrol Store - TN84
- (1) Peripheral Interface Controller - TN61
- (1) I/O Microprocessor Interface - UN25
- (3) Power Converters - 495 and 494
- (2) Power Converter/Monitor - TN9
- (1) Power Controller - TN6
- (8) Peripheral Controller (per Office requirements)

3. CONNECTING CIRCUITS

- (a) Power Distribution Frame
- (b) 3B20D Processor Control Store
- (c) 3B20D Growth Unit

4. MANUFACTURING TEST REQUIREMENTS

The Manufacturing Test Requirements for the IOP Basic Unit Circuit are included in the Manufacturing Test Requirements for 3B20D Processor (Model I, II and III), X-79516.

SECTION IV - REASONS FOR REISSUE

1. CHANGES IN APPARATUS

1.01 This reissue is made to allow the latest versions of circuit packs to be used when desired (UN33D, UN70C, and MC4C132A1C of TN983), and to correct a net name (IPWRCLRO was IPWRCLAO).

Note: This reissue also covers information authorized by the following appendixes up to Issue 2 of this CD:

APPX 1A - DWG ISS 2A  
APPX 2D - DWG ISS 3D  
APPX 3A - DWG ISS 4B  
APPX 4AC - DWG ISS 5AC  
APPX 5B - DWG ISS 6B  
APPX 6B - DWG ISS 7B  
APPX 7B - DWG ISS 8B  
APPX 8B - DWG ISS 9B  
APPX 9B - DWG ISS 10B

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