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6

COMMON SYSTEMS

PROCESSOR FRAME POWER
CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The processor frame power circuit (PFPC) provides for the control and distribution of the various operating voltages required for the circuits that comprise the system processor.

2. GENERAL DESCRIPTION OF OPERATION

2.01 Central office -48 volt and +24 volt potentials connect from the power distribution frame (PDF) to the PFPC where local fusing and further distribution to processor circuits are provided. Power modules (dc-to-dc converters) in the PFPC derive the +3 volt and +5 volt potentials required by the 3A central control (3A CC). Other processor units (ie, the main store controller and memory [MASC&M], the main store memory [M&SM], and the input/output control [I/O control]) contain the power converters required to provide their operating potentials. These converters, as well as those in the PFPC, are activated via the PFPC in conjunction with the 3A CC control panel POWER key.

2.02 The power modules are activated by the application of a +24 volt start (+24 ST) signal. These signals are provided via contacts on PFPC relays STA0 and STB0 through STB2. A 2-step (A and B) power-on sequence is provided. Relay STA0 operates when the POWER key is in the ON position. The operation of relays STB0 through STB2 is delayed long enough to ensure that the output of converters activated by relay STA0 is settled at the proper level. Thus, circuits powered from A converters should be stable while B power is coming up. A control signal from the

PFPC holds 3A CC circuits powered from A converters in an initialized state for a time sufficient for the output of B converters to stabilize. This allows the 3A CC to start from a known point and prevents extraneous I/O orders while power is coming up.

2.03 Note that, while circuit operating potentials are controlled via the 3A CC control panel POWER key, -48 volts and +24 volts associated with power (ie, the input to power modules, reference circuits, and indicators) are not. Thus, these potentials will be present in the various processor frame units when the POWER key/lamp indicates power is off. Also, an interlock exists to prevent accidental removal of power from the active (on-line) processor. A control signal from the 3A CC can prevent power shutdown independent of the POWER key when the processor is active.

2.04 Each power module provides an out-of-limit power alarm (PA) signal and an out-of-control fuse alarm (FA) signal. The FA signal can be due to a converter supplying excessive output current or having an output voltage that is grossly out of limits. The converter will shut itself down for an FA condition and will maintain the FA signal until the trouble is cleared and the alarm reset. An illuminated LED on the responsible converter accompanies either the PA or FA. The LED is extinguished after clearing the alarm condition via the POWER RESET key on the PFPC.

2.05 The PA signal for all converters (except the 5-volt converters associated with the MASC6M and MASM units) is collected by the PFPC, where it is latched and converted to a minor alarm signal. The minor alarm is reported to the on-line processor via the scanner circuit and to the office alarm circuit. The minor alarm is reset via the POWER RESET key in the PFPC.

2.06 The FA signal for all converters along with the MASC6M and MASM 5-volt converter PA signals and the blown fuse signals are combined and detected by the PFPC. The combined signal is latched and converted to a major alarm. The major alarm is reported to the on-line processor via the scanner circuit and to the office alarm circuit. Since a portion of the processor can be without power when a major alarm occurs (due to a blown fuse or a converter shutdown), the PFPC removes processor power. Power may be restored when the trouble is cleared by operating the POWER RESET key in the PFPC.

2.07 The ability of each converter to respond to a PA condition can be tested by the PFPC. A PA test can be initiated manually by the 3A CC control panel LAMP & POWER TEST key. The LED on each converter

successfully responding to the PA test will light while the key is held and go out when the key is released. This test can also be performed automatically by operating a decoder point and monitoring the minor alarm scan point.

SECTION II - DETAILED DESCRIPTION

1. GENEFAI

1.01 In the following description, leads with mnemonics that end in 1 are generally high when active or in the one state. Those that end in 0 are generally low when active or in the one state.

2. POWER CONTROL - FS 1

NORMAL POWER OFF-TO-ON SEQUENCE

2.01 The 3A CC control panel POWER key is shown in the power-off state. When power is off, relays STA0 and STB0 through STB2 are released. Leads STA001 through STA031, STB001 through STB021, STB101 through STB131, and STB201 through STB221 are disconnected from +24 volts and do not supply the power-on signal to their associated circuits. Lead PWROFF0 is low, which signals the 3A CC to hold in the initialized state when power comes on. Relay MJ0 is operated in the absence of a major alarm.

2.02 Operating the POWER key to the power-on state returns the ground, PWRKAM3, via lead PWRKAM, and the operated MJ0 relay contact to relay STA0, causing STA0 to operate. Leads STA001 through STA031 close to +24 volts as a power-on signal to their associated circuits. Input APO00 to the CONTROL element of circuit pack (CP) FC210 is grounded by the operated STA0 and MJ0 relays.

2.03 This triggers a delay circuit which, after 800 ms (nominal, 500 ms to 2 seconds allowing for tolerances), grounds lead DBP001. Lead OBRLY0 follows DBP001 to ground and operates relay STB0. Leads STB001 through STB021 close to +24 volts as a power-on signal to their associated circuits. An STFC contact also grounds OSTB1.2C to operate relays STB1 and STB2. Leads STB101 through STB131 (and STB201 through STB221) close to +24 volts as a power-on signal to their associated circuits. Lead PWF10 is also grounded to light the PWF lamp on the 3A CC control panel.

2.04 Input PPO00 to the CP FC210 CONTROL element is grounded when relays STB0, STB1, and STB2 operate. This triggers another delay circuit (800 ms nominal, 500 ms to 2 seconds allowing for circuit tolerances) that, when the time period is exceeded, allows lead PWROFF0 to go high. All circuit power should be stable by this time, and the 3A CC is no longer held in the initialized state.

NORMAL POWER ON-TO-OFF SEQUENCE

2.05 Relays MJ0, STA0, STB0, STB1, and STB2 are all in the operated state when power is on. Note that the STA0 relay is held operated via the POWER key and via an STB0 contact. Lead LOFF1 must be high for power to be turned off via the POWER key. Lead LOFF1 is high when the 3A CC is locked off line and in the manual mode or when the 3A CC is in the test and manual modes.

2.06 When the POWER key is operated to the power-off position, lead PWRKAM is open-circuited, but relay STA0 is held operated through the STB0 contact. Lead PWRKAB is grounded in the power-off state. With PWRKAB at ground and LOFF1 high, lead CBRLY0 goes high and relay STB0 releases. Contact 11 of STB0 is an early break-make and should open before contact 9, which is an early make-break. Thus, relays STB1 and STB2 should have their operate path (via contact 11) opened before relay STA0 (via contact 9). This delay removes B power before A power. Input APON0 opens when relay STA0 releases, causing lead PWROFF0 to go low. This is the state which holds the 3A CC initialized when power is turned on.

2.07 Note that with lead LOFF1 low, lead CBRYL0 remains low independent of the POWER key. Relay STB0 remains operated and holds STA0 operated. The POWER key in the off position with power on is an abnormal condition and is reported to the scanner via the power alarm circuitry.

POWER DOWN DUE TO MAJOR ALARM

2.08 A blown fuse or a power module FA signal causes relay MJ0 to release. CONTROL input APON0 and the POWER key operate path to relay STA0 are thus opened by contacts 1 and 3 of MJ0. Relay STA0 remains operated via STB0 contact 9 for the moment. Lead DBPON1 follows APON0 high, causing relay STB0 to release and power to shut down in the manner described in 2.05 through 2.07, with the exception that the POWER key remains in the operated position and lead LOFF1 has no effect.

POWER RESTORATION FROM A MAJOR ALARM

2.09 When the source of the alarm is cleared, power is restored by operating the major alarm relay (assuming that the POWER key remains in the power-on state). The major alarm relay is operated via the POWER RESET key, as will be described for FS 2. Relay STA0 is operated via PWRKAM and MJ0 contact 1, APON0 is grounded via MJ0 contact 3 and STA0 contact 9, and the power is sequenced up as described in 2.01 through 2.04.

3. POWER ALARM - FS 2

POWER ALARM DETECTION

3.01 Relays MJ0, MN, and NPA are normally held in the operated state. Relay MJ0 is released to indicate a major alarm. A minor alarm is generated when relay MN or NPA releases. Relay MJ0 is controlled by a flip-flop contained in the ALARMS element of CP FC210. Output ORLY00 is at ground to operate relay MJ0. The alarm bus for +24 volt fuses connects to input +FA1. The alarm bus for -48 volt fuses connects to input -FAC. The FA signal from all power modules and the FA signal (via a buffer circuit) from MASC&M and MASM +5 volt power modules connect to the CVFA1 input. Any of these inputs active (nominally +20 volts for +FA1 and CVFA1 and -40 volts for -FA0) sets the flip-flop, which releases relay MJ0. Leads MJ0 and MJRC comprise a normally-closed loop to the system scanner and MJ1 or MJ1A can be paired with lead MJ1R to provide a normally-closed or normally-open loop to the office alarm circuit to monitor the major alarm. An alarm indication is also given at the frame by illuminating the PWRES lamp via MJ0 contact 2.

3.02 The FA signal from all power modules except those associated with the MASC&M and MASM units are connected to the PAI1 input to the ALARMS element of CP FC210. When input PAI1 is active (nominally +20 volts) a flip-flop is set that causes lead ORLY10 to go high and release relay MN. Leads MN0 and MNR0 comprise a normally closed loop to the system scanner, and lead MN1 or MN1A can be paired with MN1R to provide a normally closed or normally open loop to the office alarm circuit to report the minor alarm. Contact 9 of the MN relay lights the PWRES lamp when a minor alarm is present.

3.03 Either alarm is retired by clearing the cause and operating the PWRES key. This grounds the NPA0 net, which clears both alarm flip-flops to the state where outputs OPIY00 and ORLY10 are at ground to operate relays MN and MJ0. The NPA0 lead at ground also extinguishes all power module IEDS that may have been illuminated in conjunction with the alarm condition.

POWER ALARM TEST

3.04 The ability of each power module to generate a PA signal, and the detection of this signal by the PFPC, can be tested. Much of the converter circuitry for the FA signal is common to the PA signal; thus, all but a portion of the FA signal path is also exercised in the PA test. The test can be initiated manually, via the 3A CC control panel IAMP & POWER TEST key, or automatically via a software-controlled decoder point. A manual test is evaluated

by observing the appropriate illumination and extinguishing of power module and CP FB152 and FC262 alarm LEDs. An automatic test is evaluated by monitoring the minor alarm scan point. Except for the means of initiation and evaluation, the test is similar in both the automatic and manual versions.

3.05 A power module generates complementary power alarm signals. The PA signal is normally low and goes high for the alarm state. The NPA signal is normally high and goes low (less than +4 volts) as an alarm. The PA terminal of each power module and CPs FB152 and FC262 position is wired serially so that the PA net will not be continuous if any position is not connected. The minor alarm flip-flop is connected at one end of the PA net (lead PAI1). A voltage source is connected to the opposite end of the net during a PA test (lead PAO1). If the net is continuous, the MN relay will release and a PAT signal will be generated to put each power module and CPs FB152 and FC262 into the PA state. If all units enter the PA state, the PA condition will be cleared at the end of the test by a ground on the NPAO net.

MANUAL POWER ALARM TEST

3.06 The manual PA test is invoked by operating (and holding operated) the LAMP & POWER TEST key on the 3A CC control panel. This removes the ground input OPATR1 to the CP FC210 TEST element. Lead POPAT is grounded by the TEST element to operate the PAT relay. Contact 12 of the PAT relay closes lead OSPAT0 to ground as a signal to the MASC&M circuit to:

- (a) Switch the PA terminal of the 5-volt converters associated with the memory into the frame PA net
- (b) Inhibit the PA signal otherwise generated by a +5 volt memory PA
- (c) Light the alarm LED on the FC262.

3.07 Contact 9 of the PAT relay closes to connect lead PAO1, which is at one end of the frame PA net, to +24 volts through a current-limiting resistor.

3.08 If the frame PA net is continuous, this +24 volts appears at input PAI1 of CP FC210 element alarms and sets the minor alarm flip-flop. This causes lead ORIY10 to go high and release relay MN. A LAMP & POWER TEST key contact bridges the minor alarm loop to the scanner to prevent an alarm indication when MN releases during the manual PA test. The office alarm connections, MN1, MN1A, and MN1R are not blocked. With relay MN released and relay PAT operated, lead PAT0 is grounded to put all power modules and the FB152 CP in the PA state. The alarm LED will light on the

FB152 CP and all power modules that enter the PA state and may be observed. If all units enter the PA state, lead NPA0 will fall below +4 volts. This is detected by the FC210 TEST element, and (via leads NPO0, FNPAFOC, and RNPARI0) ONPAR0 is opened to allow the NPA relay to release.

3.09 The test is ended by releasing the LAMP & POWER TEST key, which releases the PAT relay. Lead NPA0 is grounded, while relays PAT and NPA are released. The NPA0 signal extinguishes all IEDs and clears the minor alarm flip-flop to operate relay MN. Contact 9 of relay PAT opens to operate relay NPA when PAT is released. Capacitor C1 slows the operation of relay NPA to generate an NPA0 signal sufficient to perform the clearing function.

3.10 The PA test would have failed if the PA net was not continuous. In this event, the MN relay would not have released, and no PAT0 signal would have been generated to light the converter LEDs. A failure would also result if each converter failed to go into the PA state. In this case, the NPA0 signal would not have been generated. A faulty converter would not have the associated IED lit.

3.11 Note that if the NPA relay fails in the released state, a continuous NPA0 signal is generated while the PAT relay is not operated. This inhibits the power alarms. Contact 5 of relay NPA is in the minor alarm loop, so that it will open in this event and call attention to the trouble.

AUTOMATIC POWER ALARM TEST

3.12 The automatic PA test is identical with the manual PA test with the following exceptions:

- (a) The PAT relay is controlled by a ground on lead POPAT from a peripheral decoder, rather than the LAMP & POWER TEST key on the 3A CC control panel.
- (b) The minor alarm scan point is not inhibited. (It was bridged by the LAMP & POWER TEST key for the manual test.)
- (c) Success or failure of the operation is determined by monitoring the minor alarm scan point (rather than observing the lighting and extinguishing of LEDs). The PAT relay is operated, and after a delay in excess of one second, the minor alarm scan point should be present. The PAT relay is released and, after a delay, the minor alarm scan point should not be present.

4. POWER MODULES - FS 3+3 VOLT POWER DISTRIBUTION

4.01 The J87389F and J87389P power modules equipped in the PFPC supply +3 volts required by the 3A CC logic. Regulation to within ± 0.1 volts is achieved by sensing and filtering at the load. An FB152 CP equipped in the 3A CC derives a +12 volt reference from +24 volts for the 3-volt converters in the PFPC and for those equipped in other units in the processor frame. An element of an FC21 CP equipped in the 3A CC provides local filtering, monitors the +3 volts at the load, and derives a +3 volt reference from the +12 volt reference.

4.02 Each FC21 CP contains two elements. One FC21 element is associated with each J87389F power module. Two FC21 elements are associated with each J87389P power module. Each J87389F power module can supply up to 5 amperes. Each J87389P power module can supply up to 8 amperes.

+5 VOLT POWER DISTRIBUTION

4.03 The J87389J power modules equipped in the PFPC supply +5 volts to the 3A CC microprogram store, control panel LEDs, and MASM termination circuits. Local sensing and filtering (ie, at the power module rather than at the load) and an internal reference are employed with these converters. This is sufficient to maintain the potential at the load within ± 0.5 volts with the distribution techniques employed. Each +5 volt power module can supply up to 4 amperes. Power module PM039A supplies the control panel LEDs and the MASM terminations. Power module PM061A powers the first one thousand words of microstore in the 3A CC. These are always equipped. Power modules PM061B through D supply the second, third, and fourth one thousand words of microstore, respectively, in the 3A CC and are equipped on an optional basis as shown in Circuit Note 102.

POWER MODULE OPERATION

4.04 Except for the output potential and the location of reference, filter, and sensing, the +3 volt and +5 volt modules operate the same in the PFPC. Minus 48 volts is converted to the output potential by switching regulator action. Plus 24 volts is required to power the module converter and alarm circuits. The -48 volt return lead is not grounded at the processor frame, to avoid coupling noise into the ground plane to which the frame logic circuits connect. Four modules share a -48 volt fuse. This allows the use of a 3-ampere fuse and provides fault isolation. Plus 24 volts is connected directly to the +24 V terminal to power the alarm LED.

4.05 The module is activated by connecting +24 volts to the +24ST terminal, which supplies the conversion and detection circuitry. This connection is controlled via relays STAC through STR1 as described in FS 1. No more than four converters share a start lead to provide fault isolation, to allow the use of a 3/4-ampere fuse, and to limit the current through the start relay contact to less than 1/2 ampere so as to provide long-term reliable operation of the relay. The converter PA is active to indicate an out-of-range output. The PAs are connected together to control the minor alarm as described in FS 2. Note that since PM039A supplies some +5 volt memory power, the associated PA signal is connected to other memory +5 volt converters to cause an FA signal via CP FC262 in the MASC&M unit. This also is described in FS 2.

4.06 The power module FA signal indicates an overvoltage or excess current. These signals control the major alarm relay as described in FS 2. A power converter should shut itself down when it generates an FA signal. The FA signal will continue while the converter is shut down as long as the +24VST connection is made. This connection is removed to all converters when the major alarm relay releases (the MJ0 relay is released for the alarm condition). The module alarm LED is lit while the module is in the PA or the FA state. The PA signal follows the PA condition, delayed by a few milliseconds. Thus, if the converter goes in and out of the PA state, the PA signal will come and go. The LED will light with the first occurrence of the PA condition and will remain lit until it is cleared via the NPA lead. (The NPA leads for all converters are connected together.) This lead is grounded to extinguish the converter LED. It is also used as an indicator in the power alarm test as described in FS 2.

4.07 The converter designation and output mnemonic indicate the frame level to which it delivers power. Thus, PM058B with output 3V058F supplies +3 volts to frame level 058, which is part of the 3A CC.

5. FUSES - FS 4

5.01 All units in the processor frame are fused via the PFPC. Plus 24 volts is supplied via 3/4-ampere alarming-type fuses (70H) except to the I/O control circuit. These fuses are limited to 3/4 ampere to ensure that they will be blown by a fault in the circuit that they feed before the main fuse in the PDF blows. A blown 70H fuse puts +24 volts on the alarm bus via the operated alarm contact. This connects to the FA1 net, where it causes a major alarm.

5.02 All -48 volt fuses and +24 volt ABC fuses are 3-ampere Russman GRR type.

These will also be blown by a local fault before the PDF main fuse blows. These are nonalarming fuses, however, and are paralleled by a 1/2-ampere 70G fuse which provides the alarming function. Thus, an overcurrent in a circuit fed by this combination blows both fuses. Caution must be exercised to avoid having the 1/2-ampere pilot fuse in place without the load-carrying GBB fuse in place or else the normal load current, if in excess of 1/2 ampere will blow the pilot fuse. The alarm contact of a blown pilot fuse puts -48 volts on the -FA0 net through the limiting resistor. This results in a major alarm via the power alarm circuitry.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 None.

2. FUNCTIONAL DESIGNATION

2.01 Circuit Packs

<u>Designation</u>	<u>Meaning</u>
Alarms	Major and minor alarm Flip-flops
Control	Power sequencing control
Test	Power Alarm Test Circuits

2.02 Power Converters

<u>Designation</u>	<u>Meaning</u>
PMXXX	Power Module Supplying Frame Level XXX, Power Net Y (eg, PM058B Supplies Frame Level 058, Power Net B)

2.03 Relays

<u>Designation</u>	<u>Meaning</u>
STA0	+24 VST Control for A Power
STB0-B2	+24 VST Control for B Power
MN	Minor Alarm
MJ	Major Alarm
NPA	Reset Power Alarm
PAT	Power Alarm Test

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3. FUNCTIONS

3.01 The processor frame power unit provides the following functions for circuits equipped on the processor frame.

- (a) Fuses for +24 volt and -48 volt potentials.
- (b) A sequenced (2-step) on/off power control under control of the 3A CC control panel POWER Key.
- (c) A signal to hold the 3A CC in a reset state for a duration sufficient for all logic power to reach its operating potential when power is turned on.
- (d) Collection and reporting of power and fuse alarms.
- (e) Testing of the power alarm circuit.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a key sheet, the connecting information thereon shall be followed.

4.02 The following circuits are (may be) equipped on the processor frame and are included as connecting circuits:

- (a) 3A Central Control Circuit - SD-1C900-01.
- (b) 3A Central Control, Control Panel Circuit - SF-1C901-01.
- (c) Main Store Controller and Memory Circuit - SF-1C902-01.
- (d) Main Store Memory Circuit - SD-1C903-01.
- (e) Processor Frame Circuit - SD-1C910-01.
- (f) 2B ESS I/O Control Circuit - SD-2H099-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 Manufacturing testing requirements for this common systems circuit are determined by the using system. X-78890 specifies the manufacturing testing requirements for the No. 2B ESS control complex, which includes this circuit.