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COMMON SYSTEMS

MAIN STORE MEMORY CIRCUIT

CHANGES

D. Description of Changes

D.1 Reduced cost of the main store memory circuit by removing all unused connectors and wiring when the circuit is incorporated in a system using a word size of 16 bits. This change does not apply to the memory circuit for the No. 2B ESS.

D.2 Further reduced the cost of this circuit by replacing the existing memory unit backplane with a cost-reduced version.

D.3 Added Option Z, which allows the main store memory circuit to be used in a system with a 16-bit word size.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5515-MM-LEG

COMMON SYSTEMS

MAIN STORE MEMORY CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The main store memory (MASM) circuit is the means of storage for the program instructions and data used by the 3A central control (3A CC). The main store controller and memory (MASCM) circuit can write information into the MASM, or read information from the MASM, in response to commands from the 3A CC. The MASCM together with up to three MASMs comprise a main store (MAS) of the 3A CC.

2. GENERAL DESCRIPTION OF OPERATION

BASIC MEMORY ORGANIZATION

2.01 Program and data words stored in the MAS may be of different lengths for different applications (either 26 bits or 18 bits) but, for illustrative purposes in this document, will be considered to be 26 bits in length, as in the 2B Processor application. Each bit of information is stored as the presence or absence of electrical charge on the parasitic capacitance of an insulated gate field-effect transistor (IGFET) memory cell.

2.02 A matrix of these IGFET cells, 64 columns wide by 64 rows deep, is contained on one silicon integrated circuit (SIC) chip. One chip stores 4K (K=1024) bits of information.

2.03 Data is stored in the MASM in a bit-sliced arrangement, where all of the equivalently weighted bits of 32K words are stored in one subunit of the MASM, eg, all 32K bit 0s are stored together, all 32K bit 1s are stored together, and so on for each of the 26 bits of the 32K words. Since 4K bits are contained in one memory DIP, eight DIPs can contain 32K bits of equivalent binary weight. Two arrays of eight DIPs each are assembled onto one printed circuit board, along with necessary memory access circuitry, to form one memory plane (MP). Each MP is then an array of 32K by two bits.

2.04 Thirteen MPs, storing a total of 32K by 26 bits, are grouped together in one apparatus mounting, along with one fanout board (FOB), to form one MAS memory module. One MASM may contain either one or two

memory modules and the necessary power supplies, depending on the storage requirements of a particular application.

2.05 One MAS may include up to three MASM circuits. These six memory modules plus the two memory modules incorporated as part of the MASCM define a maximum-size MAS of eight modules, containing a total of 256K words.

2.06 The MASM is a dynamic, volatile, random-access memory. A dynamic memory is one in which stored information degenerates with time, and must be periodically regenerated. A volatile memory is a memory whose stored information is lost if the power supply of the memory is interrupted. A random-access memory is one in which any single word-storage location may be accessed in any single operational cycle, and consecutive operational cycles need not access consecutive word-storage locations. Functions performed by the MASM fall into one of four categories:

(a) Data storage

(b) Data retrieval

(c) Data refresh

(d) Operating checks.

2.07 Data storage, the act of writing information into the IGFET memory, is accomplished by presenting the address of the desired storage location, the data to be stored, and appropriate control signals to the MASM. Circuitry on the FOB buffers and regenerates the address and control signals to each MP in the module, where the address bits are decoded and the data is written into the proper IGFET cells.

2.08 Similarly, data retrieval, or reading from memory, is accomplished by presenting the desired address and appropriate control signals to the MASM. In this case, however, the control signals indicate that a read operation is in progress, and data bits are gated out from the addressed IGFET cells. The data bits, in addition to being transmitted to the main store controller (MASC), are rewritten into their respective storage locations, giving the MASM the attribute of nondestructive data readout.

2.09 Since data is stored as a charge on the parasitic capacitance of the IGFET cell, the data in each cell must be regenerated, or refreshed, at regular intervals; otherwise, the charge could leak off and the data would be lost. Data regeneration occurs as part of every normal read operation. In a refresh operation, 64 cells (one row) on each chip in the MAS are read simultaneously, refreshing 1/64 of the MAS per cycle. Refresh cycles occur approximately every 34.3 microseconds, refreshing the entire MAS in approximately 2.2 milliseconds. The timing and sequencing necessary for refresh is performed by the MASC.

2.10 The MASM contributes to two operational checks within the MAS. Parity-check circuitry on the FOB checks address parity and issues an error indication to the MASC if the check fails. In addition, certain FOB control-signal outputs are fed back to the MASCM as check points for FOB diagnostic-input exercises and normal operation monitoring.

EQUIPMENT ARRANGEMENT

2.11 In the 2B Processor, a typical application, the MAS is housed in the double-bay processor frame. The MAS may contain as many as three MASM units. One MASM apparatus mounting contains one or two memory modules plus power supplies for two modules. If a No. 2B ESS is to be equipped with more storage capacity than the 256K words of one MAS, a supplementary MAS frame containing up to two additional MAS units (an additional 512K words) is added.

SECTION II - DETAILED DESCRIPTION

1. MEMORY (FS 1)

GENERAL

1.01 The memory portion of the MASM is made up of the circuitry which actually stores information and circuitry which accesses the stored information. There are five functional considerations involved in the access and maintenance of the stored data. Each of these areas will be discussed in detail in this section:

(a) Addressing

(b) Control and timing

(c) Data input/output characteristics

(d) Refresh considerations

(e) Maintenance and diagnostic access.

1.02 The MASM is a relatively asynchronous circuit, that is, it requires no critically synchronized input-timing signals. Additionally, the required input-signal voltage levels are transistor-transistor-logic (TTL) levels, and the outputs are open-collector transistors. These characteristics allow the MASM to operate properly over a wide range of input/output (I/O) conditions. For this reason, precise I/O characteristics at the MASM are primarily determined by the specific system application. Therefore, this description will focus on the functional operations and constraints of the MASM, rather than on precise terminal I/O requirements.

ADDRESSING

1.03 The MASM contains either 32K words (if one module is equipped) or 64K words (two modules equipped). Fifteen address bits are necessary to uniquely define every word in a module, and three additional address bits specify which one of eight possible modules in an MAS is to be selected. These 18 address inputs to each FOB in an MAS appear as leads A001A through A171A for the A module, and A001B through A171B for the B module.

1.04 Two parity bits must accompany the address. Parity over the parity bit AP7.01 and address bits A001 through A071 must be odd. Parity over the parity bit AP17.81 and address bits A081 through A171 must also be odd. All of these inputs are buffered onto the FOB and fed into a parity checker. If a parity error occurs, output APERC will go active (low).

1.05 Address bits A151 through A171 define which module is to be accessed. These three bits generate select outputs MSEL0 (0,1) through MSEL2 (0,1), which are wired to select inputs SEL01 through SEL21 to provide appropriate module address identity (see Circuit Note 104). Bits A001 through A141 generate address signals on the FOB which are passed out to the MPs to specify the actual storage location to be accessed.

CONTROL AND TIMING

1.06 There are two timing/control inputs to the MASM: chip select (CS0), which commands the access of the addressed memory device; and read/write (RW0), which controls the direction of access (ie, read from or write into). Both signals are buffered and gated by the FOB, then distributed to the MPs.

DATA I/O CHARACTERISTICS

1.07 Since the MASM is a read/write memory, there are two data paths to consider: data-in, or write data (WRTD000 through WRTD230, WRTDPH0, WRTDPL0); and data-out or read data (RDD000 through RDD230, RDDPH0, RDDPL0).

REFRESH CONSIDERATIONS

1.08 Each storage location in the MASM must be accessed at least once every 2.2 ms to ensure data retention. Since the memory device employed in the MASM has an "automatic refresh" type of architecture, this objective can be met by accessing each of the 64 rows on each memory chip at least once every 2.2 ms. There are two basic refresh strategies that can be used: burst refresh, in which read/write operations are suspended while 64 consecutive refresh cycles occur every 2.2 ms; and distributed refresh, in which the 64 refresh cycles are evenly distributed over the 2.2-ms interval, "stealing" a cycle from read/write operations approximately every 34.3 USEC. The MASM is operated in a distributed refresh mode when used with the MASCM.

1.09 Address bits A061 through A111 are the six row address bits. Each of the 64 possible states of these leads must be accessed during the 64 refresh cycles within a given 2.2-ms interval. Address parity must be correct, or an address parity error will be indicated.

MAINTENANCE AND DIAGNOSTIC ACCESS

1.10 There are six status outputs from the MASM which provide maintenance information to the MASCM. When low, MSEL(0,1)0 indicates that A151 through A171 have selected the associated module (0 or 1 within the MASM). When low, SELCS0 indicates that the associated module is selected and CS0 is active. SELRW0 combines module selection and RWC status. Output RSEL0 is low when REFMD0 is controlling the module selection and REF0 is active to the memory planes during a refresh cycle. Output APER0 indicates a parity error when low, that is, the parity over the address calculated at the FOB does not match the parity transmitted with the address. Output UNSLER0 is low if GCS0 is being sent to the MPs, but the module is not selected.

1.11 The MASM has one diagnostic access-force input, FOBMT1. When this line goes high, it causes maintenance output UNSLER0 to go active for any occurrence of CS0. This permits diagnosing faults in the UNSLER0 maintenance check circuit.

2. MEMORY POWER (FS 2)

DISTRIBUTION

2.01 The memory power circuitry consists of two dc-dc converters which provide power to the MASM, plus associated wiring. The power input to the converters is -48 volts, and the control voltage input is +24 volts. One power converter, the +5 volt power module, J87421A-1, provides regulated +5 volts to the TTL circuits on the FOBs and MPs. The other converter, the J87422B-1 power module, provides +12 volts and -5 volts to the memory devices and drivers on the MPs. In addition, wiring is provided to connect an external +5 volt supply (5V039A) and return (5T039A) to power the vertical bus terminations used in the 2B Processor application.

CONTROL

2.02 The two power modules are turned on or off by independent start leads. When +24 V is applied to a start lead, that converter is on; when the start lead is

open, the converter is off. The J87421A-1 start lead, STA011, must go active at least 0.5 second before the J87422B-1 start lead, STB01, when powering the MASM; and must go inactive more than 0.5 second after STB01 goes inactive when depowering the MASM.

2.03 In the event of power system malfunctions, the power converters provide alarm outputs. The PAI1 lead goes high if the output voltage of J87421A-1 is above or below its normal operating region, and the PA1 lead goes high if either output of the J87422B-1 is out of limits. The CVPA1 lead will go high if either converter is supplying too much current or is providing an output voltage level which could damage memory circuitry.

2.04 The power modules incorporate diagnostic features to check the integrity of the power alarm circuits. If PAT0 is forced high, PA1 and PAI1 should go high, simulating a power alarm. To provide further diagnostic resolution in cases where the PA1 and PAI1 leads for each MASM are tied into a common power alarm bus (as is the case in the 2B Processor application), the NPA0 lead will be low if all power alarm circuits are properly functioning but high if one or both converters within an MASM are malfunctioning. The power alarm test circuits are reset by applying ground to NPA0.

2.05 Since the load presented to the J87422B-1 is essentially capacitive, the +12 volt bus will remain at a high voltage level for several seconds after the converter is turned off unless provision is made to discharge these outputs. In the 2B Processor application, a discharge circuit on the J87422B-1 converter in the MASM takes these outputs to 0 volts within approximately 2 seconds in the event of power shutdown or converter failure. Other applications should provide a similar feature to avoid possible damage to the memory planes during power shutdown, diagnostic checks, or converter failure. Only the +12 volt output need be discharged.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Voltage Range

-48 V (-52 V to -42 V)
+24 V (20.7 V to 26.2 V)

1.02 Temperature Range

0°C to 50°C

1.03 Relative Humidity Range

0 percent to 90 percent

2. FUNCTIONAL DESIGNATIONS

2.01 None.

3. FUNCTIONS

3.01 The MASM provides a means of storing 32K words or 64K words of program or data information for the 3A CC.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

(a) Main Store Controller and Memory Circuit - SD-1C902-02.

(b) Processor Frame Power Circuit - SD-1C911-01.

5. MANUFACTURING TESTING REQUIREMENTS

Intermediate Requirements

5.01 None.

End Requirements

5.02 This circuit should be tested to verify that it is wired in accordance with the schematic and wiring drawings, that the requirements of the circuit requirements table are met, and that the circuit is capable of performing all functions stated in this circuit description.

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