ATIS-1000640.2001(R2011)

BROADBAND ISDN NETWORK NODE INTERFACES AND INTER-NETWORK INTERFACES – RATES AND FORMATS SPECIFICATIONS

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American National Standard for Telecommunications

Broadband ISDN Network Node Interfaces and Inter-Network Interfaces – Rates and Formats Specifications

Secretariat

Alliance for Telecommunications Industry Solutions

Approved August 21, 2001

American National Standards Institute, Inc.

Abstract

This standard provides specifications of the rates and formats of signals for use at Network Node Interfaces (NNIs) and Inter-Network Interfaces (INIs) in a Broadband Integrated Services Digital Network (B-ISDN).

Foreword

The information contained in this Foreword is not part of this American National Standard (ANS) and has not been processed in accordance with ANSI's requirements for an ANS. As such, this Foreword may contain material that has not been subjected to public review or a consensus process. In addition, it does not contain requirements necessary for conformance to the standard.

Accredited Standards Committee T1, Telecommunications serves the public through improved understanding between carriers, customers, and manufacturers. Technical Subcommittee T1S1 of Committee T1 develops telecommunications standards and technical reports related to services, architectures, and signaling, in addition to related subjects under consideration in other North American and international standards bodies.

ANSI guidelines specify two categories of requirements: mandatory and recommendation. The mandatory requirements are designated by the word *shall* and recommendations by the word *should*. Where both a mandatory requirement and a recommendation are specified for the same criterion, the recommendation represents a goal currently identifiable as having distinct compatibility or performance advantages.

Suggestions for improvement of this standard are welcome. They should be sent to the Alliance for Telecommunications Industry Solutions, T1 Secretariat, 1200 G Street NW, Suite 500, Washington, DC 20005.

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Broadband ISDN Network Node Interfaces and Inter-Network Interfaces – Rates and Formats Specifications

1 Scope

This standard provides specifications of the rates and formats of signals for use at Network Node Interfaces (NNIs) and Inter-Network Interfaces (INIs) in a Broadband Integrated Services Digital Network (B-ISDN). The term, *NNI,* was originally used in ITU-T (formerly CCITT) for the description of SDH-based systems, and its use has been carried over to SONET-based systems. The meaning of NNI is further expanded in these B-ISDN specifications to include non-SONET interfaces such as DS3. INI applies to interfaces between network nodes in different networks, and has been previously established in American National Standards for other applications.

NNI and INI specifications will facilitate both intra-network and inter-network connections for B-ISDN, result in increased interoperability, and promote early availability of network interconnections and ubiquitous service offerings. This standard specifically addresses NNI and INI reference architectures and physical realizations, physical layer specifications at five bit rates (51.840 Mbit/s, 155.520 Mbit/s, 622.080 Mbit/s, 2.48832 Gbit/s, and 44.736 Mbit/s), transmission overhead characteristics, and a brief overview of Operations and Maintenance (OAM) functionality.

This standard provides fundamental definitions of the NNI and the INI and is to be used in conjunction with other standards on Physical Media Dependent (PMD) and higher layer (i.e., ATM layer, AAL layer) specifications for providing a complete technical description of the B-ISDN NNI and INI. This standard is based on a B-ISDN as described in the ITU-T Recommendations of the I-series.

There is much commonality between NNI/INI and UNI specifications at the physical layer due to the use of common underlying transport structures. The intent of this document is to be consistent with relevant American National Standards and other relevant standards and specifications.

This revision of T1.640-1996 clarifies the use of the C1 (now J1 and Z0) bytes in Table 1 as well as corrects errors related to the cell delineation states for the cell payload scrambler. In addition, several references have been updated to reflect the latest versions.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this American National Standard. At the time of publication, the editions indicated were valid. All standards and publications are subject to revision, and parties to agreements based on this American National Standard are encouraged to investigate the possibility of applying the most recent editions of the standards and publications indicated below.

T1.101-1999, *Synchronization interface standard.*[1]

T1.102-1993 (R1999), *Digital hierarchy – Electrical interfaces.*[1]

T1.105-2001, *Synchronous optical network (SONET) – Basic description including multiplex structure, rates, and formats.*[1]

T1.105.03-1994, *Synchronous optical network (SONET): Jitter at network interfaces.*[1]

T1.107-2002, *Digital hierarchy – Formats specifications.*[1]

T1.231-1997, *Layer 1 in-service digital transmission performance monitoring.*[1]

T1.404-1994, *Network-to-customer installation – DS3 metallic interface specification.*[1]

T1.627-1993 (R1999), *Broadband ISDN – ATM layer functionality and specification.*[1]

T1.646-1995, *Telecommunications – Broadband ISDN – Physical layer specification for user-network interfaces including DS1/ATM.*[1]

T1.654-1996, *Broadband ISDN – Operations and maintenance principles and functions.*[1]

A bibliography of related standards and publications appears in Annex C for information.

3 Abbreviations & Acronyms

The following acronyms are used throughout this document.

AAL	ATM Adaptation Layer
AIC	Application Identification Channel
AIS	Alarm Indication Signal
ANSI	American National Standards Institute
ATM	Asynchronous Transfer Mode
B-ICI	B-ISDN Inter-Carrier Interface
BIP-8	Bit Interleaved Parity – 8 Bits
B-ISDN	Broadband ISDN
CCITT	International Telegraph and Telephone Consultative Committee
CES	Circuit Emulation Service
CI	Customer Installation
CRS	Cell Relay Service
DCC	Data Communications Channel
dpANS	draft proposed American National Standard

[1] This document is available from the Alliance for Telecommunications Industry Solutions, 1200 G Street N.W., Suite 500, Washington, DC 20005. <http://www.atis.org>

DS1	Digital Signal Level 1
DS3	Digital Signal Level 3?
FEAC	Far End Alarm and Control
FEBE	Far End Block Error
FRS	Frame Relay Service
HEC	Header Error Check
IEEE	Institute of Electrical and Electronics Engineers?
INI	Inter-Network Interface
ISDN	Integrated Services Digital Network
ITU	International Telecommunication Union
ITU-T	ITU-Telecommunication Standardization Sector
LCD	Loss of Cell Delineation
LCD-FE	Loss of Cell Delineation – Far-End?
LTE	Line Terminating Equipment
NI	Network Interface
NN	Network Node
NNI	Network Node Interface
OAM	Operations and Maintenance
OC-1	Optical Carrier Level 1
OCD	Out of Cell Delineation
PLCP	Physical Layer Convergence Protocol
PMD	Physical Media Dependent
POH	Path Overhead
PRS	Primary Reference Source
RDI	Remote Defect Indication
RFI	Remote Failure Indication
SDH	Synchronous Digital Hierarchy
SMDS	Switched Multi-megabit Data Service
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope
STE	Section Terminating Equipment
STS	Synchronous Transport Signal
STSX-1	STS level 1 cross-connect
TMN	Telecommunications Management Network?
UNI	User-Network Interface
VCI	Virtual Channel Identifier
VPI	Virtual Path Identifier

4 Definitions

4.1 ATM network: A public or private B-ISDN network consisting of one or more Network Nodes, covering a certain geographical area, which uses a high-speed multiplexing and switching method utilizing fixed-length cells of 53 octets to support multiple types of traffic.

4.2 B-ISDN Inter-Carrier Interface (B-ICI): The Inter-Network Interface (INI) between two ATM Networks that belong to different network providers or carriers.

4.3 Customer Installation (CI): Equipment and wiring at the customer's location on the customer side of the Network Interface.

4.4 Inter-Network Interface (INI): The interface between two Network Nodes in different Networks.

4.5 Network: A collection of transmission and switching facilities used to establish communication channels.

4.6 Network Interface (NI): The point of interconnection between one network and another network.

4.7 Network Node (NN): A grouping of one or more Network Elements (at one or more sites) which provides network related functions, and is administered as a single entity. A single site may contain more than one Network Node. For the purpose of this document, a Network Node is considered synonymous with a Network Element, and is usually at a single site. This restriction simplifies the definition of the NNI and INI, which would not apply between Network Elements.

4.8 Network Node Interface (NNI): The interface between two Network Nodes within a single Network.

4.9 User-Network Interface (UNI): The term used to refer to the Network Interface (NI) as well as to interfaces within the Customer Installation (CI).

5 Interface reference architectures

The interface reference architectures for B-ISDN cover two types of interconnections, inter-network connections, and intra-network connections, as described in the following:

1. *Inter-network connections* can be found between different ATM Networks; for example, between different network providers or carriers. Inter-Network connections can also be found between different ATM Networks belonging to a single carrier. Figure 1 illustrates the reference architecture for inter-network connections and relates the Inter-Network Interface (INI) to the Network Interface (NI), which is one of the User-Network Interfaces (UNI). The INI connects two ATM Networks, either directly or via one or multiple tandem ATM Networks. The NI is the type of UNI that provides customer access to the network; such access may be service specific, e.g., for Cell Relay Service (CRS), Frame Relay Service (FRS), Switched Multi-megabit Data Service (SMDS), or Circuit Emulation Service (CES). If the INI for B-ISDN connects two networks belonging to two different carriers, it is also known as B-ISDN Inter-Carrier Interface (B-ICI).

2. *Intra-network connections* can be found within a single ATM Network between two Network Nodes, usually between two sites, as shown in Figure 2. This interface is termed Network Node Interface (NNI) and is also referred to as SONET (or other transport system) mid-span meet.

   Annex B shows a diagram that relates ATM Networks and customer installations and the various interfaces involved.

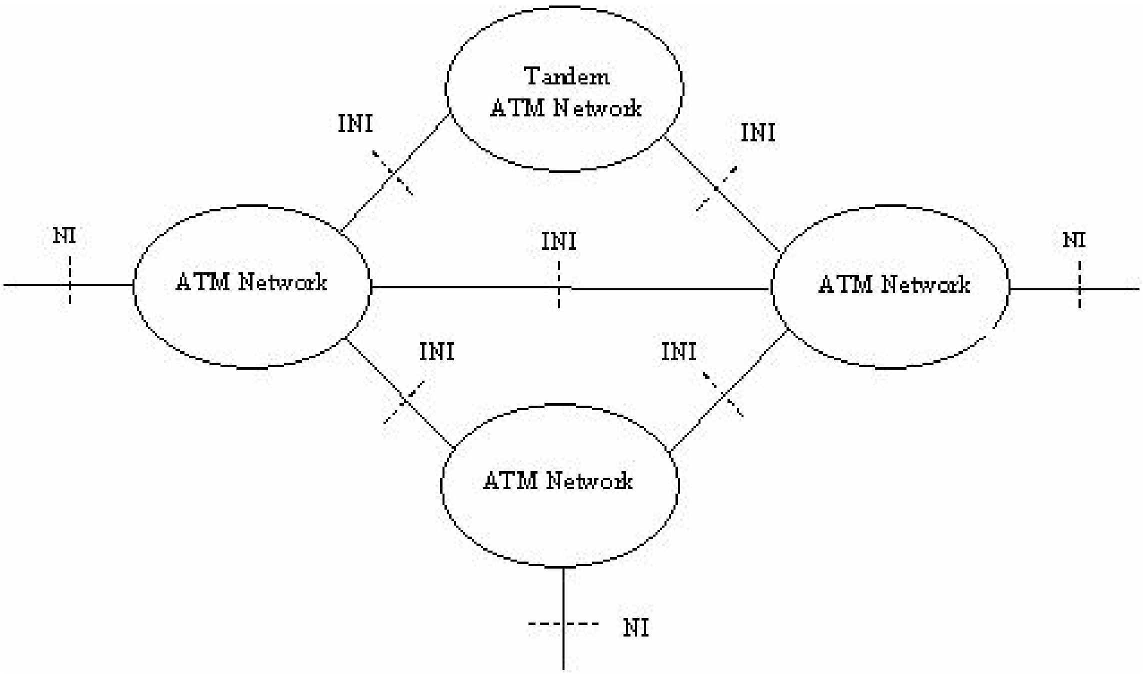

Figure 1 - Inter-network reference architecture

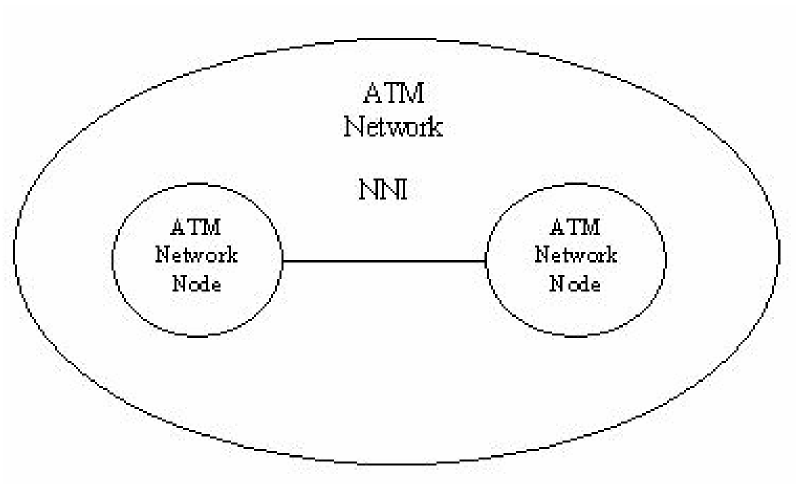

Figure 2 - Intra-network reference architecture

6 Interface physical realizations

Two basically different interface physical realizations can be distinguished:

1. The first one, labeled NNI/INI and shown in Figure 3, is a direct interoffice interconnection between two ATM Units. Thus, the NNI/INI may correspond to a transport interface such as a SONET mid-span meet. The interconnection may be between two Network Nodes within the same network (NNI), or between two Network Nodes in different networks (INI).

2. The second one, labeled NNI'/INI' and shown in Figure 4, is a multiplexed interoffice interconnection between two SONET Transport Systems, where ATM represents a logical channel or tributary that is only part of the overall transported payload that traverses the NNI'/INI'. SONET Transport Systems may be multiplexes or cross-connect systems capable of aggregating individual circuits (or channels, or tributaries) for transport over a higher capacity transport system. As in Figure 3, the interconnection may be between two Network Nodes within the same network (NNI') or between two Network Nodes in different networks (INI').[2)]

The above definitions apply just as well for non-SONET Transport Systems. In particular, ATM on either DS1 or DS3 may be transported over non-SONET systems.

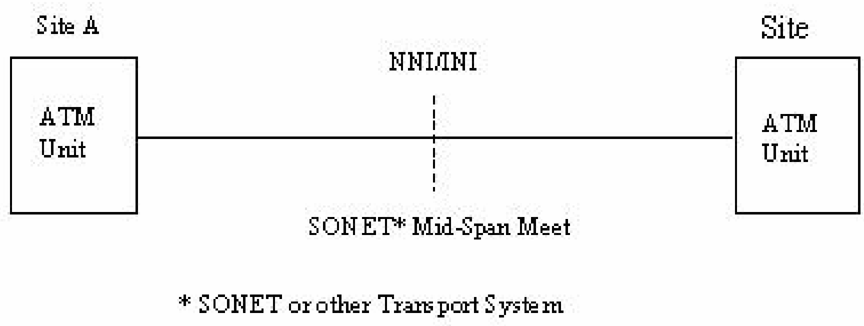

Figure 3 - Physical realization example of the NNI and INI

[2] The above definitions for the NNI/INI and NNI'/INI' interfaces are consistent with the definitions introduced in the B-ICI Specifications (see Annex C for reference) for the B-ICI and B-ICI' interfaces, respectively. Thus, the INI and INI' between networks belonging to different carriers correspond to the B-ICI and B-ICI', respectively.

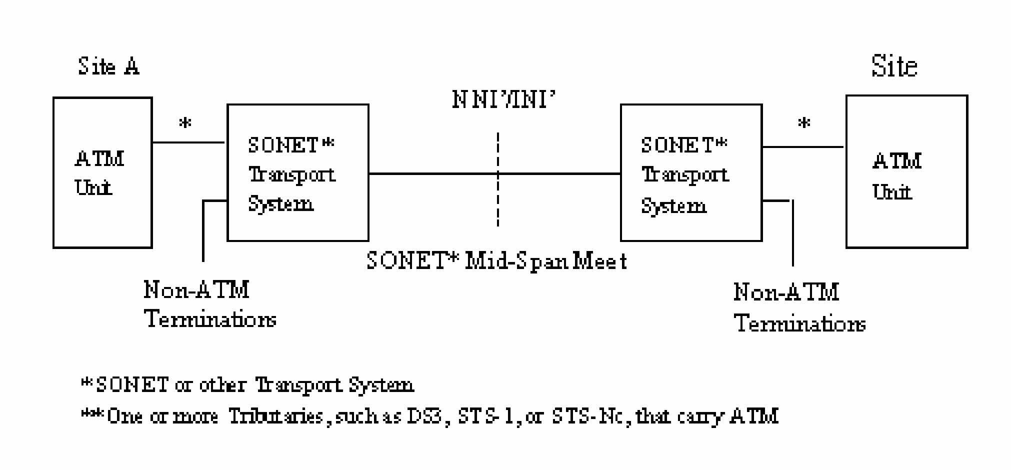

Figure 4 - Physical realization example of the NNI' and INI'

7 Physical layer specifications at 51.840 Mbit/s

The B-ISDN interface at 51.840 Mbit/s is SONET-based and utilizes the STS-1 payload structure. This interface, if implemented, shall comply with the specifications in this clause.

7.1 Bit rate

At the physical layer, the nominal bit rate shall be 51.840 Mbit/s. The bit rate available for user information cells, signaling cells, and ATM layer OAM cells, excluding physical layer related maintenance information transported in SONET overhead bytes, shall be nominally 48.384 Mbit/s. This rate is equivalent to the STS-1 Synchronous Payload Envelope (SPE) payload capacity (i.e., the total STS-1 SPE capacity minus the portion allocated to POH and fixed stuff bytes in columns 30 and 59).

7.2 Interface symmetry

The 51.840 Mbit/s interface shall be symmetric (i.e., the same bit rate shall be transmitted in both directions).

7.3 Signal format

The 51.840 Mbit/s interface is based on SONET as specified in T1.105-2001 and shall utilize the SONET STS-1 frame structure as specified in T1.646-1995 for the UNI. This frame structure contains fixed stuff bytes in columns 30 and 59.

7.3.1 Overhead bytes active across the interface

The active overhead bytes within the SONET frame depend on implementation details of the physical circuit connection. The following overhead specifications are intended to maintain flexibility, while still allowing specific requirements on overhead activation and functionality for the physical realizations described in 6 that distinguish between two types of interfaces, the NNI/INI and the NNI'/INI'.

In all these realizations, the following requirement applies: The overhead bytes active across the two types of interfaces shall be consistent with the specifications given in T1.105-2001.

A summary of the SONET overhead bytes and their requirement status is provided in Table 1.[3] Note that, consistent with the discussion in 6, only the Path Overhead is specified for NNI'/INI' in Table 1, while the Section and Line Overheads for NNI'/INI' are dictated by the multiplex/transport system. The table's notes are considered an integral part of the overhead specification.

The following definitions apply to Table 1, as well as to Table 2:

– *Required (R)* – These signals at the interface shall contain valid information as defined by this standard.

– *Optional (O)* – Valid information may or may not be present in these signals. Use of these functions is a local matter.

– *Not Active (NA)* – This function is not defined at the interface.

[3] Table 1 applies to all SONET rates, not just to 51.840 Mbit/s.

Table 1 - SONET overhead requirements for the interfaces

Overhead byte	Function	NNI INI	NNI' INI'
Section overhead			
A1, A2	Framing	R[1]	&
B1	Section error monitoring, BIP-8	R[1,2]	&
J0/Z0 (C1 in older implementations)	Section Trace / Section Growth	R[1,9]	&
D1, D2, D3	Section data communications channel	O[1,3]	&
E1	Section orderwire	O[1]	&
F1	Section user channel	O[1,8]	&
Line overhead			
B2	Line error monitoring, BIP-8N	R	&
D4 - D12	Line data communications channel	O[3]	&
E2	Line orderwire	O	&
H1, H2, H3	STS pointer	R	&
H1*, H2*	Concatenation indication[4] (for STS-3c, -12c, -48c)	R	&
H1, H2, H1*, H2*	STS path AIS	R	&
K1, K2	Automatic protection switch	O[5]	&
K2 (bits 6-8)	Line AIS, Line RDI	R	&
Z1 (bits 5-8)	Synchronization message	O	&
Z2 (bits 5-8)	Line FEBE (for STS-1 only)	R[6]	&
Z2 (in 3rd STS-1)	Line FEBE (for STS-3c, STS-12c, STS-48c)	R[6]	&
Path overhead			
B3	STS path error monitoring, BIP-8	R	R
C2	STS path signal label	R	R
G1 (bits 1-4)	STS path FEBE	R	R
G1 (bit 5)	STS path RDI	R	R
G1 (bit 6)	STS path RDI qualifier[7]		
F2	Path user channel	O[8]	O[8]
H4	Indicator	NA	NA
J1	STS path trace	O	O
Z3, Z4, Z5	Growth	NA	NA

R = Required, except where noted   NA = Not Active

O = Optional   & = As dictated by the multiplex/transport system

NOTES

1 Not required or applicable for physical layer regenerators.

2 Not required or applicable for interconnection without regenerators.

3 Section DCC required for STEs and LTEs in an application requiring communications over the SONET interface. Not required or applicable where carriers have decided to de-activate the DCC across a B-ICI .

4 H1 and H2 are the first H1 and H2 bytes of N H1, H2 bytes. H1* and H2* are the 2nd through Nth H1 and H2 bytes of N H1, H2 bytes of an STS-Nc. The asterisk indicates concatenation.

5 Only for the protection line. The suggested method of protecting interfaces is via a 1+1 protection switch architecture.

6 Initially specified only for B-ISDN UNI applications. However, standards bodies recently adopted Line-FEBE for NNIs and INIs as well.

7 The use of bit 6 of G1 is currently under study for use as an RDI qualifier to denote terminal-related versus transmission-related defects.

8 Not applicable at INIs between carriers.

9 In older implementations, the C1 bytes are set by default to the binary numbers corresponding to their order of appearance in the STS-Nc frame. Implementations based on T1.105-2001 use these bytes (C1 bytes) for section trace J0 and section growth Z0 functions. Receivers should not assume that the C1 bytes are available for frame alignment of STS-1 identification.

7.3.2 ATM cell mapping

The ATM cell stream shall be directly mapped into the STS-1 SPE payload capacity by aligning the byte structure of every cell with the byte structure of the SONET frame. The entire payload capacity is filled with cells, row by row. Because the payload capacity is not an integer multiple of the cell length, a cell may cross the SPE boundary.

7.3.3 Framing

Framing information shall be contained in the A1 and A2 bytes, as defined in T1.105-2001.

7.4 Cell rate decoupling

The physical layer shall expect cells to arrive from the ATM layer at a rate equal to the payload capacity of the SONET frame. This implies communication of the exact payload capacity to the ATM layer from the physical layer. The ATM layer inserts unassigned cells when assigned cells are not available to fill the payload capacity. Further information and detailed specification of unassigned and assigned ATM cells can be found in T1.627-1993 (R1999). An alternate method, where cell rate decoupling is performed at the physical layer by inserting idle cells when assigned and unassigned cells are not available from the ATM layer, is described in T1.646-1995.

7.5 Powering arrangements

Power shall not be provided across the 51.840 Mbit/s interface.

7.6 HEC generation and HEC check

The HEC generation and error checking functions specified in 12 shall be implemented for the 51.840 Mbit/s SONET STS-1-based interface.

7.7 Cell payload scrambler

The cell payload (self-synchronous) scrambler specified in 12.3 shall be implemented for the 51.840 Mbit/s SONET STS-1-based interface.

7.8 Cell delineation

The cell delineation functions specified in 12.4 shall be implemented for the 51.840 Mbit/s interface.

NOTE - Subclauses 7.9 and 7.10 are provided for information only; they do not represent requirements set by this standard.

7.9 PMD characteristics

Information about the PMD characteristics can be found in T1.646-1995 for the short-reach, intermediate-reach, and long-reach optical OC-1 and the electrical STSX-1 applications.[4] The choice of interface parameter set is application specific.

7.10 Synchronization, timing, and jitter

In normal operation, the signal at the interface is synchronized by a source traceable to a Primary Reference Source (PRS) as described in T1.101-1999. This source may be a Stratum 3 (or better) quality clock that is traceable to a Stratum 1 clock. When the signal at the interface is not synchronized (e.g., when in the free-running mode), a failure condition exists that needs corrective action.

Information about the network interface jitter limits can be found in T1.105.03-1994.

8 Physical layer specifications at 155.520 Mbit/s

The B-ISDN interface at 155.520 Mbit/s is SONET-based and utilizes the STS-3c concatenated payload structure. This interface, if implemented, shall comply with the specifications in this clause.

8.1 Bit rate

At the physical layer, the nominal bit rate shall be 155.520 Mbit/s. The bit rate available for user information cells, signaling cells, and ATM layer OAM cells, excluding physical layer related maintenance information transported in SONET overhead bytes, shall be nominally 149.760 Mbit/s. This rate is equivalent to the STS-3c SPE payload capacity (i.e., the total STS-3c SPE capacity minus the portion allocated to POH).

8.2 Interface symmetry

The 155.520 Mbit/s interface shall be symmetric (i.e., the same bit rate shall be transmitted in both directions).

8.3 Signal format

The 155.520 Mbit/s interface is based on SONET as specified in T1.105-2001 and shall utilize the SONET STS-3c frame structure as specified in T1.646-1995 for the UNI.

[4] Telcordia (former known as Bellcore) GR-253-CORE may also be useful; see Annex C for reference.

8.3.1 Overhead bytes active across the interface

The overhead bytes active across the two types of interfaces described in 6 and further discussed in 7.3.1 shall be consistent with the specifications given in T1.105-2001. A summary of the SONET overhead bytes and their requirement status is provided in Table 1 for the two types of interfaces.

8.3.2 ATM cell mapping

The ATM cell stream shall be directly mapped into the STS-3c SPE payload capacity by aligning the byte structure of every cell with the byte structure of the SONET frame, as specified in T1.105-2001. The entire payload capacity is filled with cells, row by row. Because the payload capacity is not an integer multiple of the cell length, a cell may cross the SPE boundary.

8.3.3 Framing

Framing information shall be contained in the A1 and A2 bytes as defined in T1.105-2001.

8.4 Cell rate decoupling

The physical layer shall expect cells to arrive from the ATM layer at a rate equal to the payload capacity of the SONET frame. This implies communication of the exact payload capacity to the ATM layer from the physical layer. The ATM layer inserts unassigned cells when assigned cells are not available to fill the payload capacity. Further information and detailed specification of unassigned and assigned ATM cells can be found in T1.627-1993 (R1999). An alternate method, where cell rate decoupling is performed at the physical layer by inserting idle cells when assigned and unassigned cells are not available from the ATM layer, is described in T1.646-1995.

8.5 Powering arrangements

Power shall not be provided across the 155.520 Mbit/s interface.

8.6 HEC generation and HEC check

The HEC generation and error checking functions specified in 12 shall be implemented for the 155.520 Mbit/s SONET STS-3c-based interface.

8.7 Cell payload scrambler

The cell payload (self-synchronous) scrambler specified in 12.3 shall be implemented for the 155.520 Mbit/s SONET STS-3c-based interface.

8.8 Cell delineation

The cell delineation functions specified in 12.4 shall be implemented for the 155.520 Mbit/s interface.

NOTE – Subclauses 8.9 and 8.10 are provided for information only; they do not represent requirements set by this standard.

8.9 PMD characteristics

Information about the PMD characteristics can be found in ITU-T Recommendation G.957 (see Annex C) and in T1.646-1995 for the short-reach, intermediate-reach, and long-reach optical OC-3 and the electrical STSX-3 applications.[4] The choice of interface parameter set is application specific.

8.10 Synchronization, timing, and jitter

In normal operation, the signal at the interface is synchronized by a source traceable to a PRS, as described in T1.101-1999. This source may be a Stratum 3 (or better) quality clock that is traceable to a Stratum 1 clock. When the signal at the interface is not synchronized (e.g., when in the free-running mode), a failure condition exists that needs corrective action.

Information about the network interface jitter limits can be found in T1.105.03-1994.

9 Physical layer specifications at 622.080 Mbit/s

The B-ISDN interface at 622.080 Mbit/s is SONET-based and utilizes the STS-12c concatenated payload structure. This interface, if implemented, shall comply with the specifications in this clause.

9.1 Bit rate

At the physical layer, the nominal bit rate shall be 622.080 Mbit/s. The bit rate available for user information cells, signaling cells, and ATM layer OAM cells, excluding physical layer related maintenance information transported in SONET overhead bytes, shall be nominally 599.040 Mbit/s. This rate is equivalent to the STS-12c SPE payload capacity (i.e., the total STS-12c SPE capacity minus the portion allocated to POH and fixed stuff bytes).

9.2 Interface symmetry

The 622.080 Mbit/s interface shall be symmetric (i.e., the same bit rate shall be transmitted in both directions).

9.3 Signal format

The 622.080 Mbit/s interface is based on SONET, as specified in T1.105-2001, and shall utilize the SONET STS-12c frame structure, as specified in T1.646-1995 for the UNI. This frame structure contains three columns of fixed stuff bytes immediately following the POH.

9.3.1 Overhead bytes active across the interface

The overhead bytes active across the two types of interfaces described in 6 and further discussed in 7.3.1 shall be consistent with the specifications given in T1.105-2001. A summary of the SONET overhead bytes and their requirement status is provided in Table 1 for the two types of interfaces.

9.3.2 ATM cell mapping

The ATM cell stream shall be directly mapped into the STS-12c SPE payload capacity by aligning the byte structure of every cell with the byte structure of the SONET frame. The entire payload capacity is filled with cells, row by row. Because the payload capacity is not an integer multiple of the cell length, a cell may cross the SPE boundary.

9.3.3 Framing

Framing information shall be contained in the A1 and A2 bytes, as defined in T1.105-2001.

9.4 Cell rate decoupling

The physical layer shall expect cells to arrive from the ATM layer at a rate equal to the payload capacity of the SONET frame. This implies communication of the exact payload capacity to the ATM layer from the physical layer. The ATM layer inserts unassigned cells when assigned cells are not available to fill the payload capacity. Further information and detailed specification of unassigned and assigned ATM cells can be found in T1.627-1993 (R1999). An alternate method, where cell rate decoupling is performed at the physical layer by inserting idle cells when assigned and unassigned cells are not available from the ATM layer, is described in T1.646-1995.

9.5 Powering arrangements

Power shall not be provided across the 622.080 Mbit/s interface.

9.6 HEC generation and HEC check

The HEC generation and error checking functions specified in 12 shall be implemented for the 622.080 Mbit/s SONET STS-12c-based interface.

9.7 Cell payload scrambler

The cell payload (self-synchronous) scrambler specified in 12.3 shall be implemented for the 622.080 Mbit/s SONET STS-12c-based interface.

9.8 Cell delineation

The cell delineation functions specified in 12.4 shall be implemented for the 622.080 Mbit/s interface.

NOTE – Subclauses 9.9 and 9.10 are provided for information only; they do not represent requirements set by this standard.

9.9 PMD characteristics

Information about the PMD characteristics can be found in ITU-T Recommendation G.957 (see Annex C) and in T1.646-1995 for the short-reach, intermediate-reach, and long-reach optical OC-12 applications.[4] The choice of interface parameter set is application specific.

9.10 Synchronization, timing, and jitter

In normal operation, the signal at the interface is synchronized by a source traceable to a PRS, as described in T1.101-1999. This source may be a Stratum 3 (or better) quality clock that is traceable to a Stratum 1 clock. When the signal at the interface is not synchronized (e.g., when in the free-running mode), a failure condition exists that needs corrective action.

Information about the network interface jitter limits can be found in T1.105.03-1994.

10 Physical layer specifications at 2.48832 Gbit/s

The B-ISDN interface at 2.48832 Gbit/s is SONET-based and utilizes the STS-48c concatenated payload structure. This interface, if implemented, shall comply with the specifications in this clause.

10.1 Bit rate

At the physical layer, the nominal bit rate shall be 2.48832 Gbit/s. The bit rate available for user information cells, signaling cells, and ATM layer OAM cells, excluding physical layer related maintenance information transported in SONET overhead bytes, shall be nominally 2.39616 Gbit/s. This rate is equivalent to the STS-48c SPE payload capacity (i.e., the total STS-48c SPE capacity minus the portion allocated to POH and fixed stuff bytes).

10.2 Interface symmetry

The 2.48832-Gbit/s interface shall be symmetric (i.e., the same bit rate shall be transmitted in both directions).

10.3 Signal format

The 2.48832-Gbit/s interface is based on SONET as specified in T1.105-2001 and shall utilize the SONET STS-48c frame structure. The structure of the frame is shown in Figure 5. It consists of 9 rows and 4320 columns. The first 144 columns constitute Transport Overhead, which consists of Section Overhead and Line Overhead. The Section Overhead is contained in rows 1-3 and the Line Overhead in rows 4-9. The H1 and H2 Pointer Bytes in row 4 indicate the offset in bytes between the pointer and the first byte of the STS-48c SPE (i.e., the first byte of the Path Overhead, J1). The H3 Pointer Action Byte is used for frequency justification of the SPE. The STS-48c SPE consists of 4176 columns and is the path structure that carries the ATM cells. The first column within this structure is the Path Overhead, followed immediately by 15 columns of fixed stuff bytes. The remaining 4160 columns represent the payload capacity available for ATM cells.

10.3.1 Overhead bytes active across the interface

The overhead bytes active across the two types of interfaces described in 6 and further discussed in 7.3.1 shall be consistent with the specifications given in T1.105-2001. A summary of the SONET overhead bytes and their requirement status is provided in Table 1 for the two types of interfaces.

10.3.2 ATM cell mapping

The ATM cell stream shall be directly mapped into the STS-48c SPE payload capacity by aligning the byte structure of every cell with the byte structure of the SONET frame. The entire payload capacity is filled with cells, row by row. Because the payload capacity is not an integer multiple of the cell length, a cell may cross the SPE boundary.

10.3.3 Framing

Framing information shall be contained in the A1 and A2 bytes as defined in T1.105-2001.

10.4 Cell rate decoupling

The physical layer shall expect cells to arrive from the ATM layer at a rate equal to the payload capacity of the SONET frame. This implies communication of the exact payload capacity to the ATM layer from the physical layer. The ATM layer inserts unassigned cells when assigned cells are not available to fill the payload capacity. Further information and detailed specification of unassigned and assigned ATM cells can be found in T1.627-1993 (R1999). An alternate method, where cell rate decoupling is performed at the physical layer by inserting idle cells when assigned and unassigned cells are not available from the ATM layer, is described in T1.646-1995.

10.5 Powering arrangements

Power shall not be provided across the 2.48832-Gbit/s interface.

10.6 HEC generation and HEC check

The HEC generation and error checking functions specified in 12 shall be implemented for the 2.48832-Gbit/s SONET STS-48c-based interface.

10.7 Cell payload scrambler

The cell payload (self-synchronous) scrambler specified in 12.3 shall be implemented for the 2.48832-Gbit/s SONET STS-48c-based interface.

10.8 Cell delineation

The cell delineation functions specified in 12.4 shall be implemented for the 2.48832-Gbit/s interface.

NOTE – Subclauses 10.9 and 10.10 are provided for information only; they do not represent requirements set by this standard.

10.9 PMD characteristics

Information about the PMD characteristics can be found in ITU-T Recommendation G.957 for the short-reach, intermediate-reach, and long-reach optical OC-48 applications.[4] The choice of interface parameter set is application specific.

10.10 Synchronization, timing, and jitter

In normal operation, the signal at the interface is synchronized by a source traceable to a PRS, as described in T1.101-1999. This source may be a Stratum 3 (or better) quality clock that is traceable to a Stratum 1 clock. When the signal at the interface is not synchronized (e.g., when in the free-running mode), a failure condition exists that needs corrective action.

Information about the network interface jitter limits can be found in T1.105.03-1994. This document also addresses the two types of regenerators that are allowed by current standards for OC-48, Type A and Type B. Related with this are two levels of input jitter tolerance (i.e., normal and reduced tolerance) at all OC-48 receivers. Consequently, two interface jitter limits have been established and joint engineering is required to determine which limit shall be used at the interface.

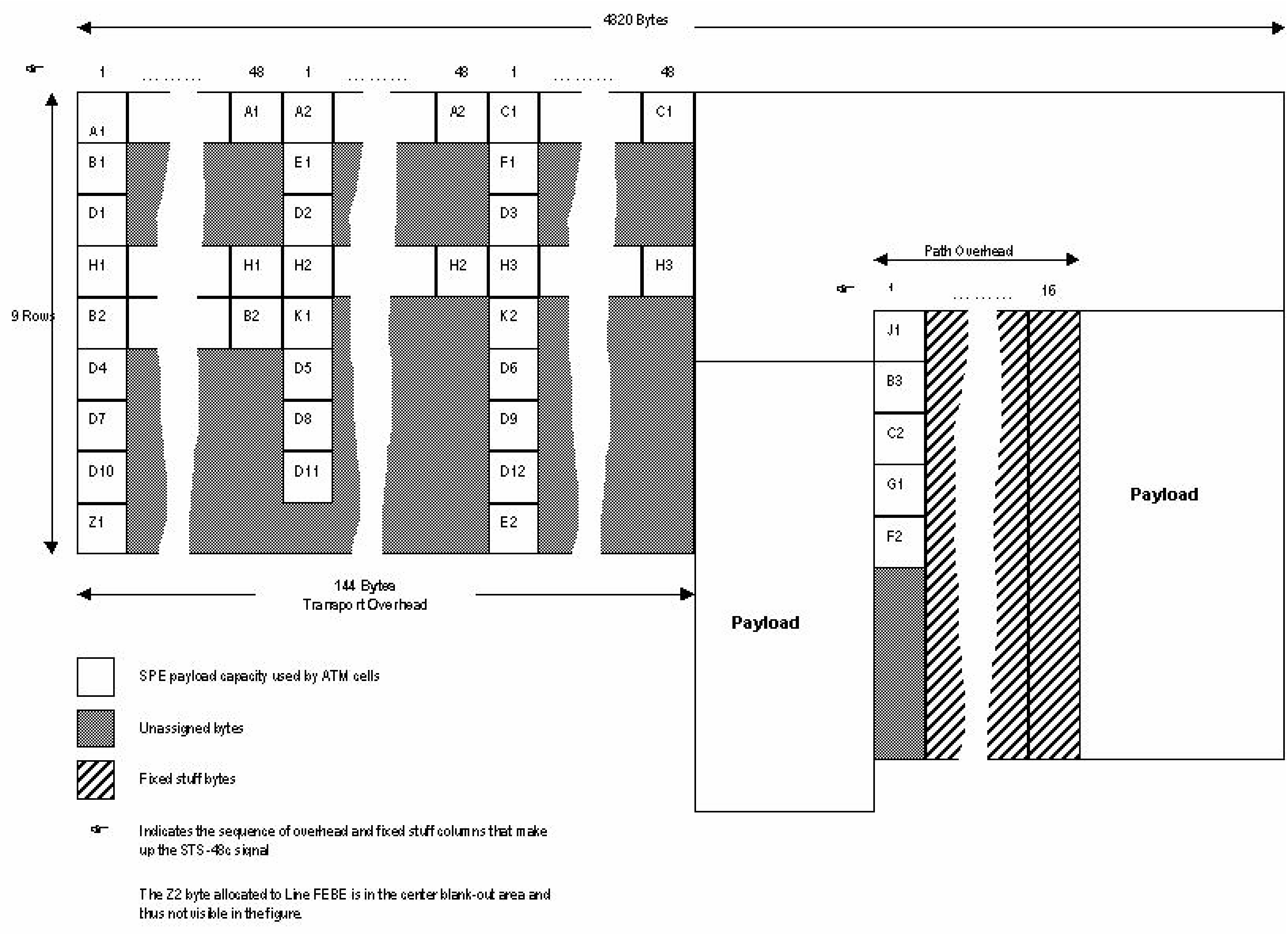

Figure 5 - SONET STS-48c transporting ATM cells

11 Physical layer specifications at 44.736 Mbit/s

The B-ISDN interface at 44.736 Mbit/s is a non-SONET interface. Mapping of ATM cells into the payload of the DS3 may be accomplished in one of two mutually incompatible ways:

1) Direct mapping; and

2) Physical Layer Convergence Protocol (PLCP)-based mapping.

Either method maps ATM cells into the DS3 multiframe structure with C-Bit Parity application. This interface, if implemented, shall comply with either the direct mapping specified in this clause or the PLCP-based mapping specified in Annex A.

For new implementations, the direct mapping is preferred. However, the need to support existing implementations that use the PLCP-based mapping should be taken into account by network operators and manufacturers. The direct mapping is viewed as the long-term target mapping for the following reasons:

– The ATM capacity of the direct mapping method is approximately 9% greater than that of the PLCP-based method; and

– The C-Bit Parity functionality that applies to both mapping methods is sufficient to support the interface. Therefore, the PLCP functionality is redundant.

11.1 Bit rate

At the physical layer, the nominal bit rate shall be 44.736 Mbit/s and the signal shall be synchronized as described in 11.10. When the interface is not synchronized, the bit rate shall be 44.736 Mbit/s ± 20 ppm.

The bit rate available for user information cells, signaling cells, and ATM layer OAM cells, excluding physical layer related maintenance information transported in DS3 or PLCP overhead bytes, shall be nominally 44.210 Mbit/s in the DS3 direct mapped format and 40.704 Mbit/s in the DS3 PLCP-based format.

11.2 Interface symmetry

The 44.736 Mbit/s DS3 interface shall be symmetric (i.e., the same bit rate shall be transmitted in both directions).

11.3 Signal format

The interface format at the physical layer shall be based on asynchronous DS3 with C-Bit Parity format for the Full Payload Rate application as defined in T1.404-1994, T1.107-2002, and ITU Recommendation G.703.[5] T1.404-1994 introduces the concept of the Full Payload Rate application, which requires that all

[5] Telcordia (former known as Bellcore) GR-499-CORE may also be useful; see Annex C for reference.

seven stuffing bit locations of a DS3 frame shall be used as data bits; whereas T1.107-2002 addresses the Modified M23 application, which requires that all stuffing bit locations shall always be stuffed. The use of the Full Payload Rate application is necessary to allow either the directly mapped ATM cells or the PLCP frame to be nibble-aligned[6] when mapped onto the DS3.

The DS3 frame structure is shown on Figure 6. It consists of an M-Frame of 4760 bits that is divided into seven M-Subframes of 680 bits each. Every M-Subframe is further divided into eight blocks of 85 bits, consisting of one overhead bit and 84 information bits. The information bits are reserved to carry the payload.

11.3.1 Overhead bits active across the interface

The 56 overhead bits in the M-Frame are assigned various functions as listed in Figure 6. The C1, C2, and C3 bits constitute the 21 C-bits of the C-Bit Parity application that are used for various maintenance and operations functions, including parity. The DS3 C-bit usage and requirements are defined in Table 2.

Table 2 - DS3 C-Bit channel requirements

Bits	M-Subframe	Function	NNI INI	NNI' INI'
C1	1	Application Identification Channel (AIC)	R	R
C2	1	Network requirement bit*	R	R
C3	1	Far End Alarm and Control Channel (FEAC)	R	R
C1, C2, C3	2	Reserved for future use	NA	NA
C1, C2, C3	3	Calculated Parity-bits, path parity indicator	R	R
C1, C2, C3	4	FEBE function	R	R
C1, C2, C3	5	Terminal-to-terminal path maintenance data link	O	O
C1, C2, C3	6, 7	Reserved for future use	NA	NA

R = Required

O = Optional

NA = Not Active, Set to “1”

* The value of this bit is set as specified in T1.646-1995.

11.3.2 ATM cell mapping for the direct mapping format

Direct mapping of ATM cells into the DS3 payload is accomplished by directly inserting the 53-byte ATM cells into the DS3 information payload within the DS3 frame shown in Figure 6. The byte structure of the ATM cells is aligned with the nibble structure of the DS3 M-Frame. The M-Frame is organized such that 84 information bits follow every overhead bit. The 84 bits can be assumed to be organized into 21 consecutive nibbles. The ATM cell is placed such that the start of a cell always coincides with the start of a nibble. ATM cells may cross M-Frame boundaries.

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[6] A nibble is 4 bits.

11.4 Cell rate decoupling

The physical layer shall expect cells to arrive from the ATM layer at a rate equal to the payload capacity of the DS3 frame. This implies communication of the exact payload capacity to the ATM layer from the physical layer. The ATM layer inserts unassigned cells when assigned cells are not available to fill the payload capacity. Further information and detailed specification of unassigned and assigned ATM cells can be found in T1.627-1993 (R1999). An alternate method, where cell rate decoupling is performed at the physical layer by inserting idle cells when assigned and unassigned cells are not available from the ATM layer, is described in T1.646-1995.

11.5 Powering arrangements

Power shall not be provided across the 44.736 Mbit/s interface.

11.6 HEC generation and HEC check

The HEC generation and error checking functions specified in 12 shall be implemented for the 44.736 Mbit/s DS3-based interface.

11.7 Cell payload scrambler

The cell payload (self-synchronous) scrambler specified in 12.3 shall always be implemented for 44.736 Mbit/s DS3-based interfaces.

11.8 Cell delineation

For the direct mapped method, cell delineation shall be performed using the HEC method as described in 12.4.

For the PLCP-based method, the cells are in predetermined locations within the PLCP frame (see Annex A). Framing on the DS3 frame and then on the PLCP frame is sufficient to delineate cells.

NOTE – Subclauses 11.9 and 11.10 are provided for information only; they do not represent requirements set by this standard.

11.9 PMD characteristics

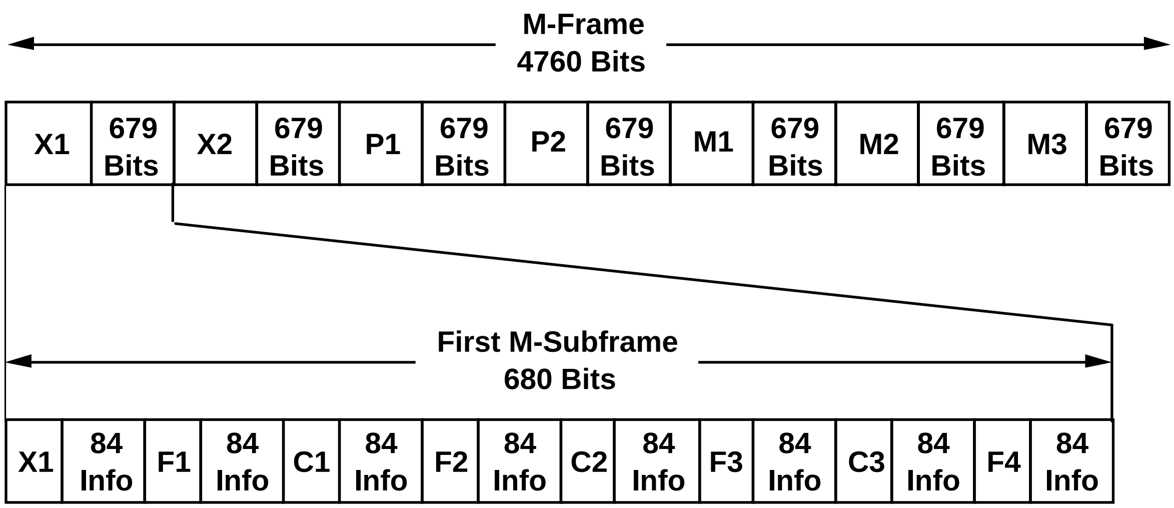
Information about the PMD characteristics at the 44.736 Mbit/s DS3-based electrical interface can be found in T1.102-1993 (R1999).

11.10 Synchronization, timing, and jitter

In normal operation for the PLCP-based method, the PLCP frame at the interface is synchronized by a source traceable to a PRS, as described in T1.101-1999. This source may be a Stratum 3 (or better) quality clock that is traceable to a Stratum 1 clock.

In normal operation for the direct mapped method, timing shall be provided by the DS3 signal. The timing of the 44.736-Mbit/s signal shall be traceable to a PRS as described in T1.101-1999. This source may be a Stratum 3 (or better) quality clock that is traceable to a Stratum 1 clock. The 8-kbit/s timing can be derived from the 44.736-Mbit/s signal by dividing by 5592.

Information about the network interface jitter limits at the 44.736-Mbit/s B-ISDN interface can be found in T1.102-1993 (R1999).



M-Frame overhead bit sequence

56 overhead bits occupy sequential overhead bit positions as follows:

M-Subframe 1	X1	F1	C1	F2	C2	F3	C3	F4
M-Subframe 2	X2	F1	C1	F2	C2	F3	C3	F4
M-Subframe 3	P1	F1	C1	F2	C2	F3	C3	F4
M-Subframe 4	P2	F1	C1	F2	C2	F3	C3	F4
M-Subframe 5	M1	F1	C1	F2	C2	F3	C3	F4
M-Subframe 6	M2	F1	C1	F2	C2	F3	C3	F4
M-Subframe 7	M3	F1	C1	F2	C2	F3	C3	F4

NOTES

1 See T1.107-1995 for description of X1 and X2 bits.

2 See T1.107-1995 for description of P1 and P2 bits.

3 The M-Frame alignment signal is M1=0, M2=1, and M3=0.

4 The M-Subframe alignment signal is F1=1, F2=0, F3=0, F4=1.

5 C1, C1 and C3 bits are assigned for the C-Bit Parity application; see T1.107-2002.

Figure 6 - DS3 frame structure (106.4 μs)

12 HEC functionality, scrambling, and cell delineation

12.1 HEC generation

The following procedure shall be performed to generate the HEC (Header Error Check) sequence by each cell originator.[7] The following polynomials are used to specify the HEC value:

$$\mathbf{G}(x) = x^8 + x^2 + x + 1$$

$$\mathbf{C}(x) = x^6 + x^4 + x^2 + 1$$

Where:

G(*x*) is the generating polynomial, and

C(*x*) is the coset polynomial.

The HEC value corresponding to a given header shall be obtained by the following procedures:

- The 32 bits of bytes 1, 2, 3, and 4 of the header shall be the coefficients of a polynomial M(x) of degree 31 (bit 1 of byte 1 of the header corresponds to the x^{31} term, and bit 8 of byte 4 of the header corresponds to the x^0 term);
- M(x) shall be multiplied by x^8 and divided (modulo 2) by G(x). C(x) shall be added modulo 2 (exclusive OR) to the remainder of this division producing a polynomial R(x) of degree < 8; and
- The coefficients of R(x) are considered to be an 8-bit sequence. This 8-bit sequence shall be the HEC. The 8 bits of the HEC shall be placed in the HEC field so that the coefficient of the x^7 term is bit 1 and the coefficient of the x^0 term is bit 8.

12.2 HEC check

The HEC function of the receiver on either side of the interface has two states: Correction state and Detection state.

- In Correction state, cells received with an apparent single-bit error in the header shall be corrected and the HEC function shall go into Detection state.
- In Correction state, when a multi-bit error in the cell header is detected[8], the cell shall be discarded and the HEC function shall go into Detection state.

---

[7] Note that in the HEC generation procedure given here, the most significant bit (and first to be transmitted) is number 1. In the ATM layer specifications and standards, the bit numbering order is different.

[8] When in Correction state, the HEC error detection capability is reduced. Test results of ATM switches show that when the header is corrupted with three or more bit errors, for some error patterns the HEC fails to detect multiple bit errors, and the HEC treats such headers as containing only a single bit error and attempts to correct them. This usually results in a nondiscarded cell with bit errors in the header.

- In Detection state, all the cells with detected header errors shall be discarded.
- In Detection state, when a cell with no error in the header is received, the HEC function shall go into Correction state.[9]

Figure 7 shows the state diagram of these bistate operational requirements. As an option, the single-bit error correction capability may be disabled (or not provided), and in this case all cells with detected errored headers shall be discarded. The default mode provides for single-bit error correction. The header error analysis process performed by the receiving physical layer equipment is illustrated in Figure 8.

12.3 Cell payload scrambler

The following specifications apply to SONET-based and DS3-based interfaces.

A cell payload (self-synchronizing) scrambler, with polynomial $1 + X^{43}$ shall be used to scramble/descramble the 48-byte information field of ATM cells.

The scrambler shall operate continuously through the stream of ATM cells, bypassing ATM cell headers. Hence, ATM cell headers are not scrambled.

The scrambler state at the beginning of a cell payload shall be the state at the end of the previous cell payload.

Descrambling shall be disabled during the cell delineation Hunt state (described below).

During the cell delineation Presynch and Synch states (described below), the scrambler shall be enabled for a number of bits equal to the length of the information field and disabled for the following assumed header.

12.4 Cell delineation

Cell delineation is performed using the HEC byte of the ATM cell header; however, for the DS3 interface using the PLCP method, the ATM cells are explicitly delineated upon PLCP framing (see 11.8 and Annex A).

For the SONET B-ISDN interfaces, the location of cell boundaries within the byte stream shall be obtained by determining the location at which the HEC coding rule is obeyed. For the DS3 interface using the direct mapping method, the location of cell boundaries within the nibble stream shall be obtained by determining the location at which the HEC coding rule is obeyed. This cell delineation process is described by the state diagram shown in Figure 9. This process has three states of operation: Sync state, Hunt state, and Presync state. The details of the state diagram are described below:

> NOTE – The "correct HEC" means the header has no bit error (syndrome is zero) and has not been corrected.

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[9] It may be desirable in some applications to delay (e.g., in the range of one to two seconds) the return to the Correction state. The referenced delay would help avoid the potential situation where multi-bit errors go undetected during burst activity while in Correction state.

a) In the *Sync state* (cell boundaries are assumed correct), correct HECs are verified on a cell-by-cell basis. The process moves to the Hunt state when ALPHA consecutive incorrect HECs are obtained.

b) In the *Hunt state,* the delineation process is performed by checking bit-by-bit for the correct HEC for the assumed header field. Once such an agreement is found, it is assumed that one header has been found and the process enters the Presync state. When byte or nibble boundaries are available within the receiving physical layer prior to cell delineation (as with SONET or DS3-based interfaces), the cell delineation process may be performed byte-by-byte or nibble-by-nibble.

c) In the *Presync state,* correct HECs are sought on a cell-by-cell basis. If DELTA consecutive correct HECs are obtained while in this state, the process returns to the Sync state. If one incorrect HEC is detected, the process returns to the Hunt state.

The parameters ALPHA and DELTA are to be chosen to make the cell delineation process as robust and secure as possible. Robustness against false misalignments due to bit errors depends on the value of ALPHA. Robustness against false delineation in the resynchronization process depends on the value of DELTA. Values of ALPHA = 7 and DELTA = 6 are suggested.

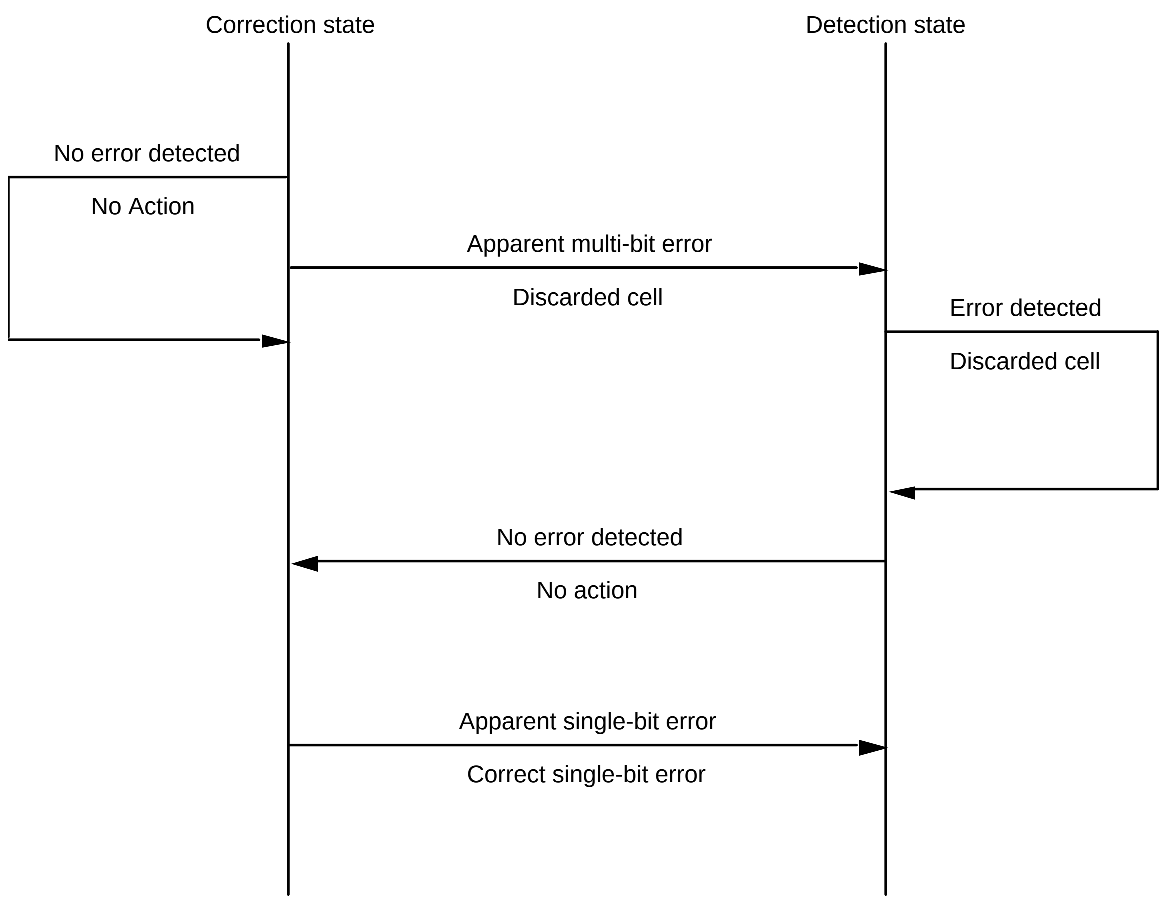
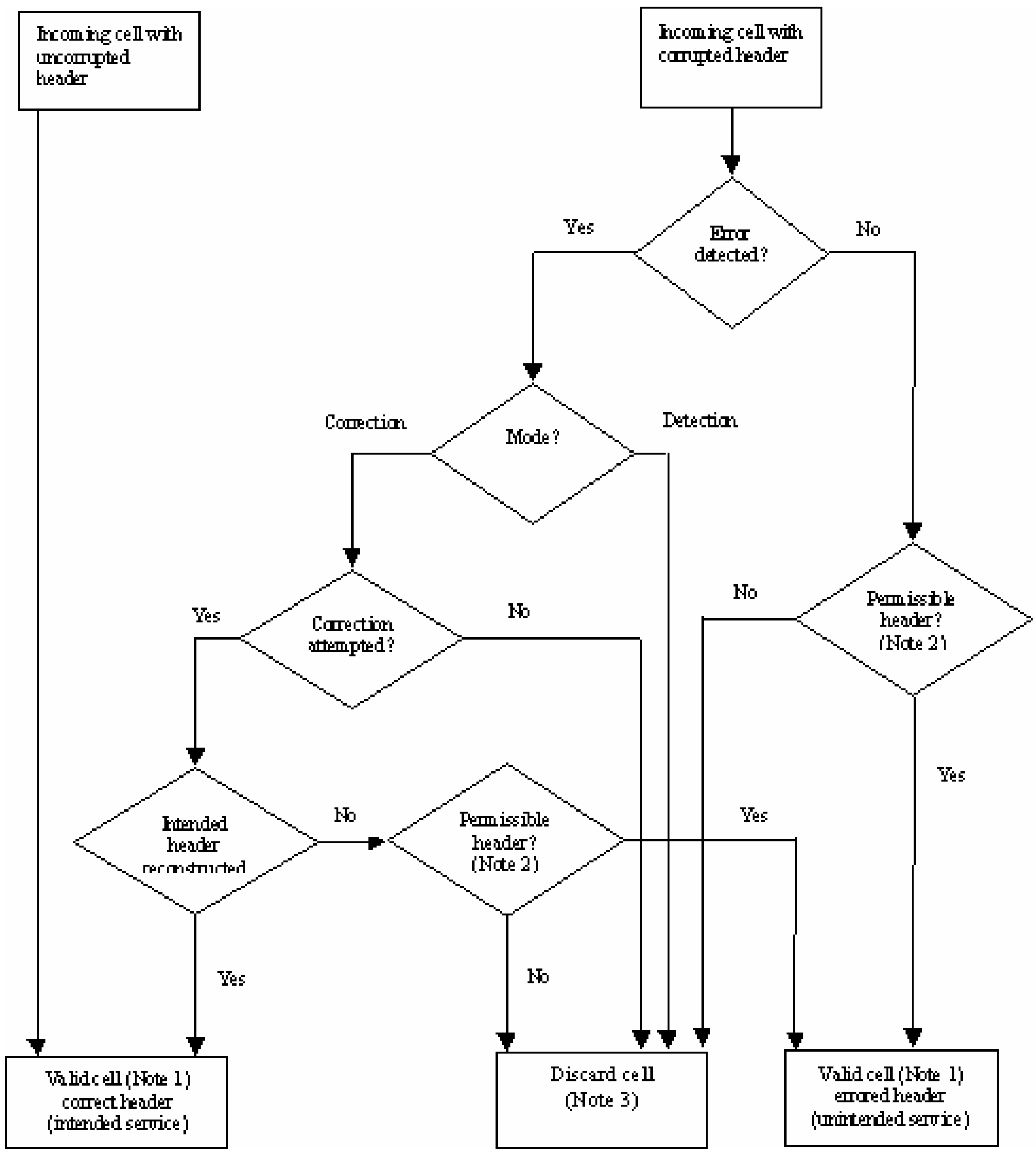


Figure 7 - Receiver HEC bistate operation



NOTES

1 Definition of "valid cell": A cell where the header is declared by the header error control process to be free of errors (ITU-T Recommendation I.113).

2 An example of an impermissible header is a header whose VPI/VCI is neither allocated to a connection nor preassigned to a particular function (idle cell, OAM cell, etc.). In many instances the ATM layer will decide if the cell header is permissible -- see T1.627-1993 (R1999).

3 A cell is discarded if its header is declared to be invalid, or if the header is declared to be valid and the resulting header is impermissible.

Figure 8 - Cell header error analysis

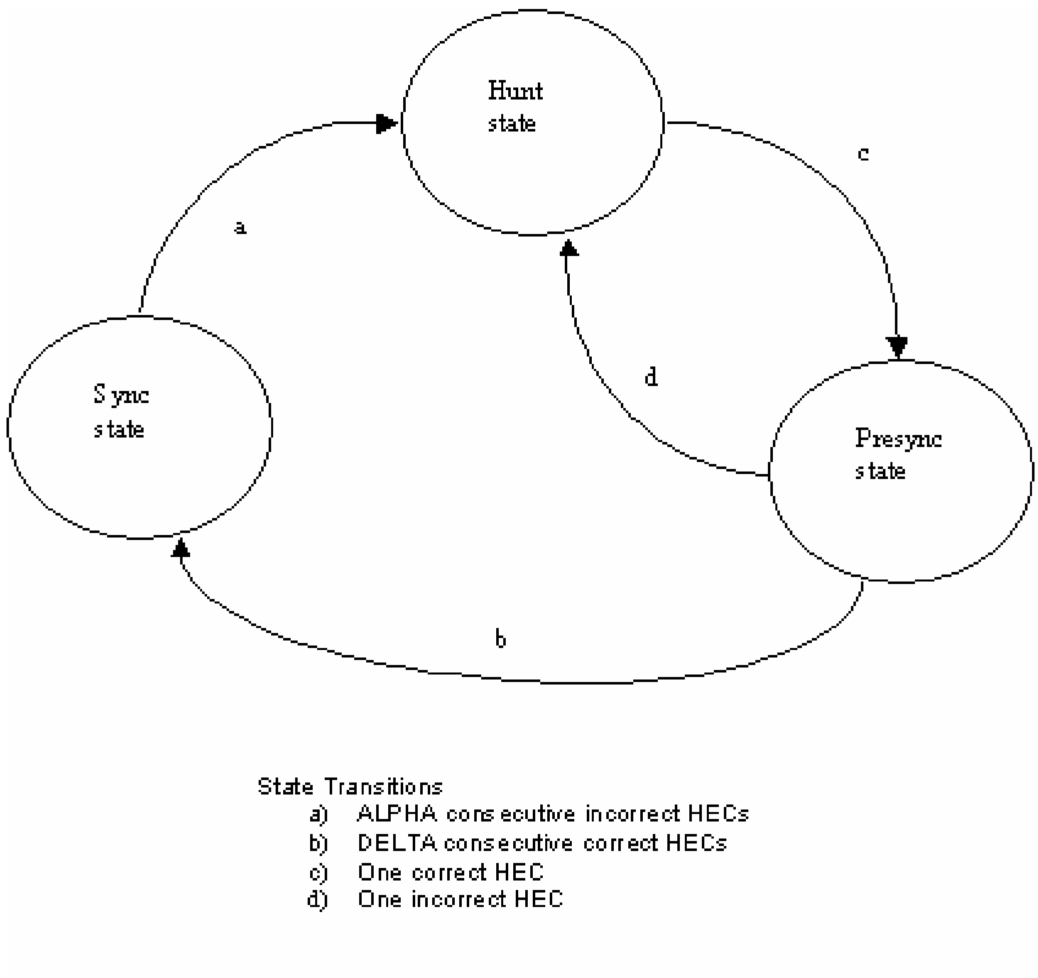


Figure 9 - Cell delineation state diagram

13 Physical layer operations and maintenance

Operations and Maintenance (OAM) are based on Telecommunications Management Network (TMN) principles, as described in ITU-T Recommendation M.3010, which covers, among others, Performance Management and Fault Management. Performance and Fault Management strategies for the physical layer rely upon three fundamental operations tools, as described in T1.231-1997, *Surveillance, Testing, and Restoration*.

13.1 Surveillance

Surveillance has two distinct, but related, functional aspects. These are Performance Monitoring and Alarm/Status Monitoring:

- *Performance Monitoring* is the process of continuous, in-service, nonintrusive collection of performance data associated with a transmission entity to allow timely detection of performance degradations or related troubles, preferably before the end user is adversely affected.
- *Alarm/Status Monitoring* is the process that tracks failure events, via alarm/status indications, to contribute to an understanding of the overall transmission performance of an entity.

Standardized monitoring is important in light of a multi-vendor and a multi-carrier environment, and the need to resolve responsibilities for end-to-end performance degradations at interfaces between different networks.

T1.231-1997 presents a set of requirements to provide for uniform and consistent Performance Monitoring and Alarm/Status Monitoring for DS3 and SONET digital rates. It provides standard definitions for performance primitives, performance parameters, and performance failures. However, it does not establish any requirements or guidelines for levels of performance. T1.231-1997 covers all sublayers of the physical layer except the ATM Specific Functions.

13.2 ATM Specific Functions

The ATM Specific Functions of the physical layer, as well as ATM layer Performance Management and Fault Management, are covered in T1.654-1996. In this document, Performance Management includes Performance Monitoring, and Fault Management includes Alarm/Status Monitoring.

Maintenance states and functions directly related to ATM cell delineation on either side of an NNI/INI are defined and discussed below.

13.2.1 Cell delineation maintenance states

Near-end and far-end reports related to cell delineation are based on maintenance state transitions for cell delineation events. The three maintenance states currently considered in this standard are:

1) Working State;
2) OCD Anomaly; and
3) LCD Defect.

These states are summarized in Figure 10 and are defined in the following:

- *Out of Cell Delineation (OCD)*: An OCD Anomaly occurs when transition *a* of the cell delineation process (refer to 12.4 and Figure 9) occurs while in the working state. An OCD Anomaly terminates when the cell delineation state transition *b* occurs (refer to 12.4 and Figure 9) or when the LCD Defect maintenance state is entered.

- *Loss of Cell Delineation (LCD)*: An LCD Defect occurs when an OCD Anomaly persists for *x* ms. An LCD Defect terminates when the cell delineation process (refer to 12.4 and Figure 9) enters and remains in the Synch state for *x* continuous milliseconds.

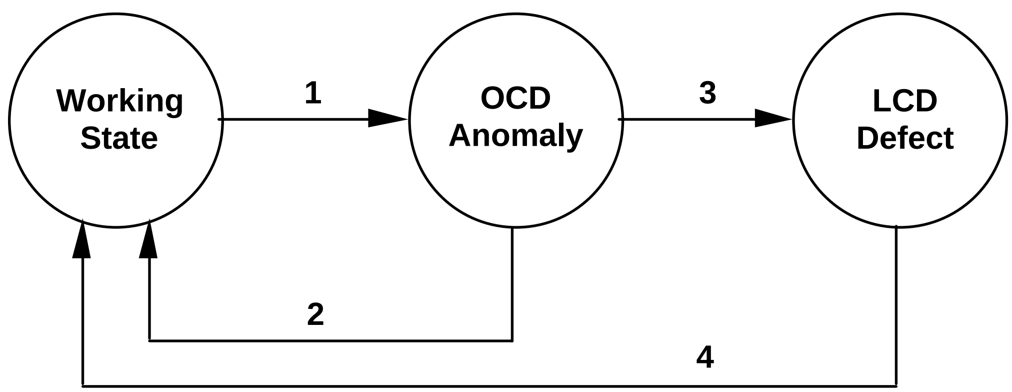
– *Loss of Cell Delineation – Far-End (LCD-FE)*: An LCD Defect results in an RDI-P FE report. This is discussed in detail in T1.646-1995*.*

The value of *x* is 4 ms for all SONET-based interfaces and 2.5 ms for the DS3 interface.

13.3 Physical Layer Functions

Physical layer maintenance functions for SONET-based as well as DS3-based interfaces are described in T1.646-1995*.* For the DS3-based interfaces, that document addresses both, the DS3 level and the PLCP level maintenance functions. Maintenance functions and framing formats required for the DS3 layer are also described in T1.404-1994.[10]

For the DS3 PLCP mapping, a duplicate maintenance functionality exists for the path level error monitoring. This functionality is provided by the DS3 C-Bit Parity application as well as by the PLCP format. It should be noted that both functions, the C-Bit Parity (Calculated Parity-bits) and the PLCP BIP-8 (B1-byte), must be activated by the transmitting side. The receiver may be configured to utilize only one of these functions to monitor the path level performance.



<u>Maintenance State Transitions</u>

1) Triggered by state transition *a* of the cell delineation process (see cell delineation state diagram, Figure 9).

2) Triggered by state transition *b* of the cell delineation process (see cell delineation state diagram, Figure 9).

3) Triggered by *x* continuous milliseconds (see 13.2.1 for the value of *x*) in the OCD Anomaly maintenance state.

4) Triggered by x continuous milliseconds (see 13.2.1 for the value of x) in the Sync state of the cell delineation process (see cell delineation state diagram, Figure 9).

Figure 10 - Maintenance state transition diagram for cell delineation events

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[10] Maintenance functions for the PLCP layer can also be found in Telcordia (formerly known as Bellcore) TR-TSV-000773; see Annex C for reference.

Annex A

(normative)

A ATM cell mapping for the PLCP-based format at 44.736 Mbit/s

This annex describes an alternate mapping of ATM cells into DS3 from the direct mapping method described in 11.3.2. This alternate mapping supports existing implementations that use the PLCP-based mapping.

PLCP-based mapping of ATM cells into the DS3 payload is accomplished in two steps. First, the 53-byte ATM cells are inserted into the PLCP frame as shown in Figure A.1. This PLCP is a subset of the PLCP defined in IEEE P802.6[11], and is the same as that used at the NI. Second, the overall PLCP frame is then mapped into the DS3 information payload within the DS3 frame shown in Figure 6. Note that the 125-µs PLCP frame is longer than the 106.4-µs DS3 frame.

A.1 PLCP format

The DS3 PLCP consists of a 125-µs frame within a standard DS3 payload. There is no fixed relationship between the start of the PLCP frame and the DS3 frame (i.e., the DS3 PLCP may begin anywhere inside the DS3 payload). As can be seen from Figure A.1, the DS3 PLCP frame consists of 12 rows of ATM cells, each preceded by four overhead bytes. Nibble stuffing is required after the twelfth ATM cell to fill the 125-µs PLCP frame. Although the PLCP is not aligned to the DS3 framing bits, the bytes in the PLCP frame are nibble aligned to the DS3 payload envelope. Nibbles begin after the overhead bits (X, F, C, P, or M) of the DS3 frame.

A.2 PLCP overhead bytes/nibbles active across the interface

The following PLCP overhead bytes/nibbles are required to be active across the interface (refer to Figure A.1):

A1 - Frame alignment
A2 - Frame alignment
B1 - Bit interleaved parity
C1 - Cycle/stuff counter
G1 - PLCP path status
Px - Path Overhead Identifier
Zx - Growth bytes
Trailer nibbles

[11] Telcordia (formerly known as Bellcore) TR-TSV-000773 may also be useful; see Annex C for reference.

A.2.1 Frame alignment (A1, A2)

The PLCP framing bytes shall use the same framing pattern used in SONET. These bytes are A1=11110110, A2=00101000.

A.2.2 Bit interleaved parity (B1)

The BIP-8 (B1) byte supports PLCP path error monitoring, and shall be calculated over a 12 x 54 byte structure consisting of both the POH field and the ATM cells (a total of 648 bytes) of the previous PLCP frame.

A.2.3 Cycle/stuff counter (C1)

The cycle/stuff counter provides a nibble stuffing opportunity and Trailer length indicator for the PLCP frame.

A stuffing opportunity shall occur every third frame of a 3-frame (375 µs) stuffing cycle. The value of the C1 code shall be used as an indication of the phase of the 375-µs stuffing opportunity cycle (see Table A.1).

Table A.1 shows that a trailer containing 13 nibbles is used in the first frame of the 375-µs stuffing opportunity cycle. A trailer of 14 nibbles is used in the second frame. The third frame provides a nibble stuffing opportunity. A trailer containing 14 nibbles is used in the third frame if a stuff occurs. If not, the trailer contains 13 nibbles.

Table A.1 - DS3 PLCP cycle/stuff counter definition

C1 Code	Frame phase of cycle	Trailer length
11111111	1	13
00000000	2	14
01100110	3 (no stuff)	13
10011001	3 (stuff)	14

A.2.4 PLCP path status (G1)

The PLCP path status byte shall convey the received PLCP status and performance to the transmitting far-end. This byte permits the status of the full receive/transmit PLCP path to be monitored at either end of the path. The G1 byte is divided into three subfields as follows: a 4-bit Far End Block Error (FEBE) in bits 1 to 4 of G1, a 1-bit Remote Failure Indication (RFI or Yellow) in bit 5 of G1, and three X-bits in bits 6 to 8 of G1 (receivers shall be capable of ignoring the value of the X-bits).

The specification of a DS3 PLCP path RDI signal in addition to or in replacement of the path RFI signal is for further study.

A.2.5 Path Overhead Identifier (P0–P11)

The Path Overhead Identifier bytes shall index the adjacent POH byte of the DS3 PLCP. Table A.2 provides the coding for each of the Path Overhead Identifier bytes.

Table A.2 - DS3 PLCP Path Overhead Identifier code definitions

Path Overhead Identifier	Path Overhead Identifier code	Associated POH
P11	00101100	Z6
P10	00101001	Z5
P9	00100101	Z4
P8	00100000	Z3
P7	00011100	Z2
P6	00011001	Z1
P5	00010101	X
P4	00010000	B1
P3	00001101	G1
P2	00001000	X
P1	00000100	X
P0	00000001	C1

X - Receiver required to ignore

A.2.6 Growth bytes (Z1–Z6)

The growth bytes shall be reserved for future use. These bytes shall be set to Z*i*=00000000, by the transmitter (*i*=1, 2..., 6). The receiver shall be capable of ignoring the value contained in these fields.

A.2.7 Trailer nibbles

The contents of each of the 13/14 trailer nibbles shall be 1100.

PLCP framing		POI	POH	PLCP payload	
A1	A2	P11	Z6	First ATM cell	
A1	A2	P10	Z5	ATM cell	
A1	A2	P9	Z4	ATM cell	
A1	A2	P8	Z3	ATM cell	
A1	A2	P7	Z2	ATM cell	
A1	A2	P6	Z1	ATM cell	
A1	A2	P5	X	ATM cell	
A1	A2	P4	B1	ATM cell	
A1	A2	P3	G1	ATM cell	
A1	A2	P2	X	ATM cell	
A1	A2	P1	X	ATM cell	
A1	A2	P0	C1	Twelfth ATM cell	Trailer
1	1	1	1	53 Octets	13 or 14
Octet	Octet	Octet	Octet		Nibbles
			Object of BIP-8 calculation		

POI = Path Overhead Indicator

POH = Path Overhead

BIP-8 = Bit Interleaved Parity - 8

X = Unassigned - Receiver required to ignore

Figure A.1 - PLCP frame structure (125 μs)

Annex B

(informative)

B Examples of interfaces

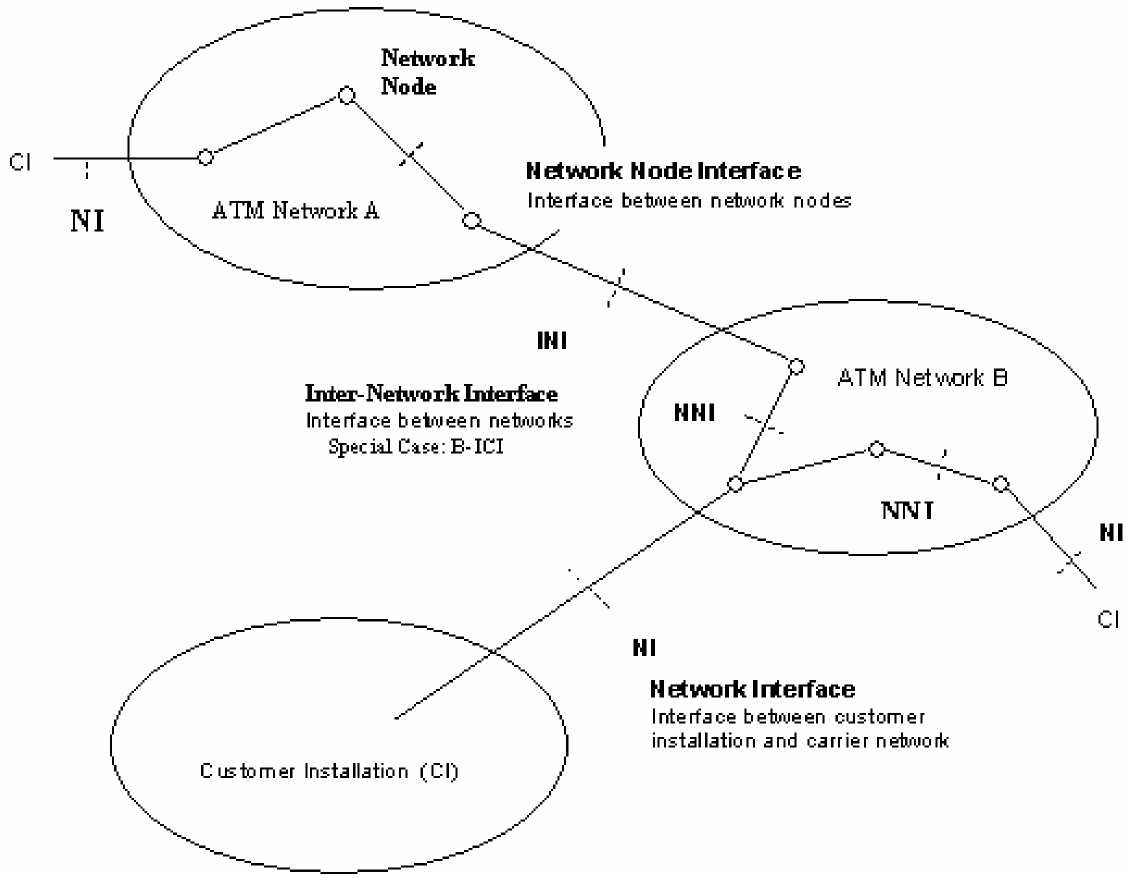

Figure B. 1 - Example of Interfaces

Annex C

(informative)

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