TELETYPE CORPORATION
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MASTER AND SUPPLEMENTARY HIGH SPEED TAPE SENDER WITH RADIO FREQUENCY INTERFERENCE (RFI) SUPPRESSION FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

DESCRIPTION AND THEORY OF OPERATION

CONTENTS PAGE

1. GENERAL

1.01 This section provides a general description and theory of operation of radio frequency interference (RFI) suppression on the master and supplementary high speed tape senders. It is used with ref- to the standard literature as additional information relating to certain modules and components. There are also certain added new features used only on later ~~models, such as~~ external stop-send, bid retention, and **models, such as** sequence. Functional operation of the high speed tape senders is unchanged (Figures 1 and 2).

1.02 The basic function of RF1 suppression as applied to t&typewriter equipment is to provide shielding to suppress electrical field radiation from 1 kilo hertz to 1 giga hertz. Signal, clock, and electrical power inputs and outputs are the same as described in the standard MAPS sections.

2. DESCRIPTION

2.01 The new parts added to the tape senders consist of a conduit plate, function box assembly, capacitors, ground straps, latches and contacts.

2.02 The conduit plate has three 3/4 inch knockouts for clock and signal input and output cables. and one 1/2 inch opening for an ac power input circuit connector. The conduit plate is mounted in the cable opening at the bottom rear of the cabinet.

2.03 The junction box consists of a three terminal board, two 0.47 microfarad bypass capacitors, and wires to connect -with an existing ac input terminal hoard. Adjustable pawl fasteners are grounded and secure the front panel to the cabinet frame.

DX TAPE READER

2.04 Signal shielding for the DX tape reader consists of two 0.001 microfarad capacitors, two contact shorting assemblies, and a ground strap. The two capacitors are connected across the -28 volt dc and common of the code reading and verifying contacts.

2.05 The contact shorting assembly is connected to the code reading and verify contact mounting screws in such a manner that they are grounded to the reader top plate.

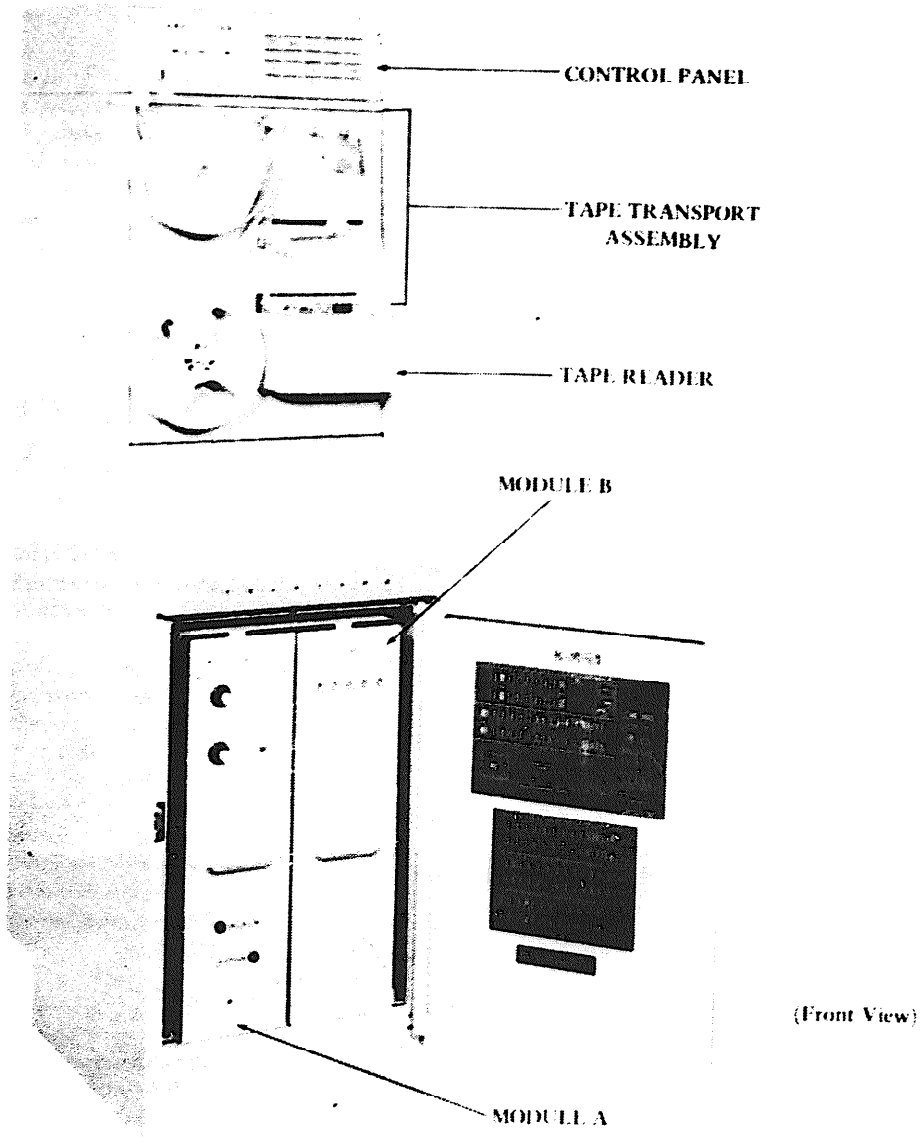
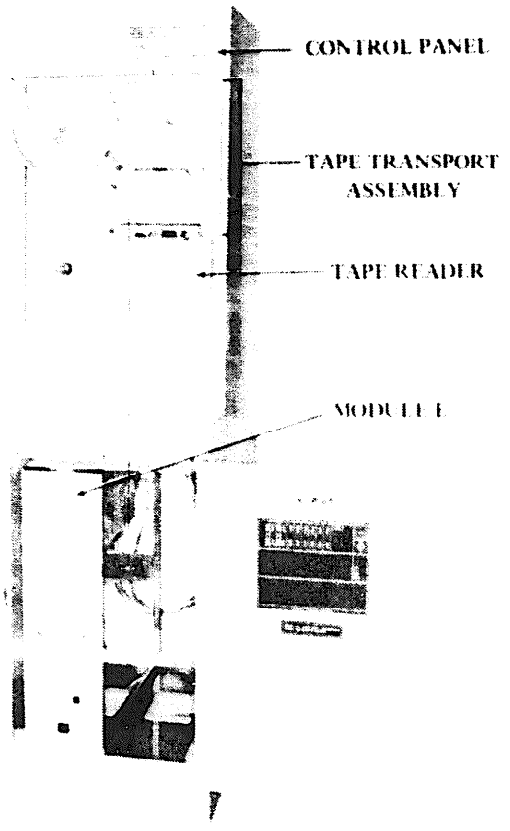


Figure 1. Master High Speed Tape Sender



(Front View)

Figure 2. Supplementary High Spread Tape Sender

Figure 2 Supplementary High Speed Tape Sender

The ground strap is connected to the base of the reader and its mounting bracket, providing a path to ground, bypassing the reader shock mounts.

EXTERNAL STOP SEND

2.06 The external stop-send capability provides the system with an external means of stopping the reader on the character after the one being read. The reader stops when a +6 volts is received at the input lead which is at -6 volts level under normal operating conditions. The reader continues transmitting in correct character frame when a -6 volt signal is received on this input lead.

BID RETENTION

2.07 A bid retention feature on the supplementary and master transmitters automatically retains the line after the manual STOP switch is operated, and the tape lid is lifted with the reader in the on-line condition. This allows the operator the option of stopping the reader during transmission, lifting the tape lid and removing the tape for possible editing. The tape may be replaced in the reader, the STOP switch released and transmission resumed without losing the on-line condition.

SOM CHARACTER SEQUENCE

2.08 The SOM sequence feature adds an additional letter V character at the beginning of the sequence. Each reader transmission is preceded by fourteen characters consisting of eight programmed identifying characters, one operator programmed character, one figure character, three numeric characters, and a letter character in that order (example: VZCZCABCX↑999↓).

2.09 The three numeric characters increase one count after each transmission. The counter can be manually reset to any count, including zero. The operator has the option of deleting a complete sequence by using the NUMBERS DELETE indicator switch. The message rate is limited to the maximum recycling rate of the counter (five times per second).

3. THEORY OF OPERATION

CONTROLS AND INDICATORS

3.01 Operator controls and indicators art located on the control panel at the top of each cabinet. The master and supplementary control panels are identical except for the message numbering indicator on the left ride of the master control panel. Additional controls are located on the front panels **of** the electronic modules in, the tower half of each cabinet behind protective doors. Parallel to serial **con**verter programming facilities arc located wthin the master transmitter logic module (Figures 3. 4. and 51

3.02 The VERIFIER/TAPE FEED (Figures 3 and 4) split alarm and pushbutton switch indicates an alarm in red, with the reset switch common to both alarms. External equipment alarms are accepted through a relay common to both alarms, providing the alarm transfer contacts.

3.03 The ABNORMAL TRAFFIC indicator lights when an abnormal traffic input signal is received from the external equipment.

3.04 When the reader is in the STOP condition. the STEP READ switch can be used to step the reader through a tape message, one character length (0.1 inch) for each operation of **the** switch. **The operator may use the** STEP **switch to manually** step the **reader at tunes** when there is no normally supplied step pulses.

3.05 Operating **the** STOP switch. illuminates **the switch indicator and stops the reader during transmission.** No other associated reader may **send at this** time. Operating the switch a second time, puts out the switch light, **and** restarts the **reader** and tape reading system.

3.06 **When** the POWER switch is operated, the switch indicator is illuminated and the switch activates electric power to the tape transport motor, tape re___ motor, and electronic modules.

3.07 When a bid to transmit has not been mitiated, operate the MOTORS switch. which illuminates the inductor and permits manual operation of the reader and tape winder motors.

3.08 The ON LINE indicator is illuminated when the reader has authorization to transmit.

3.09 The BID switch indicator is illuminated when operated and generates a bid to transmit when tape is in the reader.

3.10 When the NUMBER DELETE switch is operated and illuminated. the start of message sequence is not transmitted ahead of each transmission. At the end of each transmission the switch automatically resets to the normal (send number) mode and the indicator light is turned off.

3.11 **Circuit breakers are provided on the front** panel **of** the power supply module for overload protection. Should a circuit breaker trip to its off position, the normal procedure of turning off cabinet power before resetting the breaker should be observed

3.12 **The additional controls found on the front** panels **of the** electronic **modules in** the lower half of the cabinet are as follows:`

(1) Module A - CODE LEVEL selector switch 15. **6.** 7. **and** 8 levels); UNITS PER CHARACTER INTREVAL selector switch indicates synchronous or [illegible] **indicates synchronous or**

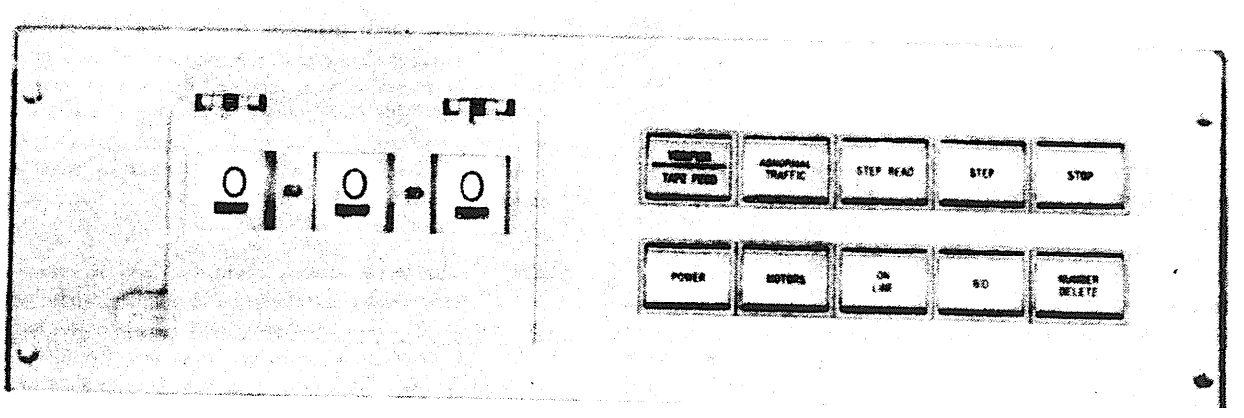


Figure 3 Master Control Panel

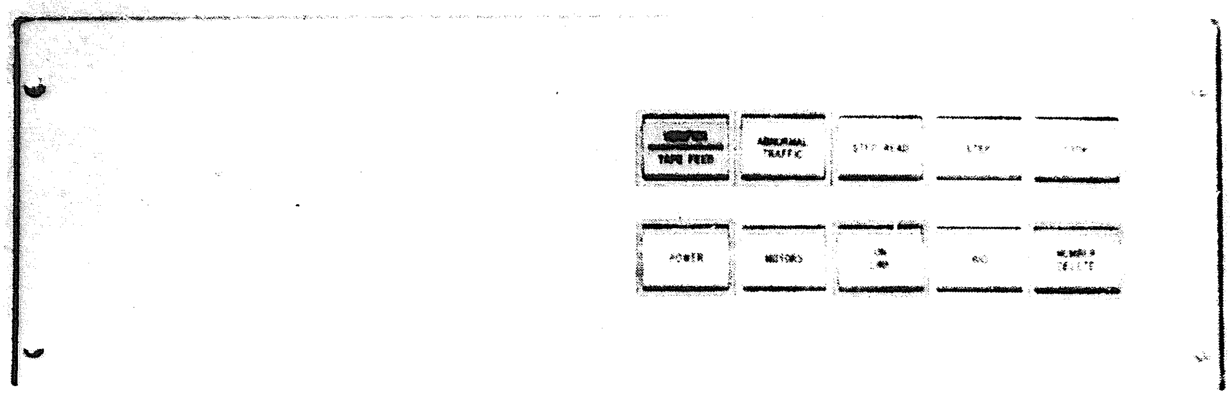


Figure [illegible] — Supplementary Control Panel

start stop level numerals. SIGNAL MODE toggle switch indicates either START STOP or SYNCHRONOUS operation.

(2) Module B — The SOM CHARACTER toggle switches (2, 3, 4, 5, and 6, one for each character bit, are operated in MARK or SPACE position to determine the [illegible] character in the start of message sequence.

(3) Module E — The module control panel contains some logic circuitry and [illegible] voltage circuit breakers; all other controls are contained in modules A and B in the master cabinet.

CIRCUIT DESCRIPTION

3.13 The 0 volt and -5 volts on [illegible] internal leads are identified by a shaded corner in the logic symbol from which they originate. The [illegible] coupled inputs to logic elements are shown as half arrow heads. Half arrow heads indicate ac coupled pulse input.

3.14 The commonly used NOR logic element is identified by the designation [illegible] within the [illegible] symbol. The output of the element is negative when [illegible] input is 0 volt. The output is 0 volt only if all inputs are negative. A special input, identified by an arrow entering a corner of the symbol, allows the addition of extra logic inputs to the element or connecting two or more elements together to obtain more inputs and greater load driving capability.

3.15 The flip-flop element is designated by a rectangular box with a diagonal line across [illegible]. The priming voltage inputs are shown as half arrow heads and the setting voltage inputs by tail arrows. Prime [illegible] inputs are [illegible] enter the upper [illegible] of the symbol and prime 0 volt and set 0 signals enter the lower half of the symbol. An arrow entering the center of the symbol designates the set 1 and set 0 inputs are connected together.

3.16 If no priming inputs are shown, the prime 1 input is connected to the inverted output (lower half of the symbol) and prime 0 input is connected to the normal output (upper half of symbol). Each input pulse reverses the condition of the voltages on the normal and inverted outputs.

3.17 The pulse amplifier element is identified by a square box with the letters PA in the symbol. A half arrow head indicates the input. This element produces a pulse approximately two microseconds in duration whenever the input goes negative. When both inputs are used, a pulse is produced only when both inputs go negative.

[illegible] A trapezoid with the letters PA within the symbol represents the power amplifier element. This element has two inputs and can perform the NOR element function with approximately three times the load driving capability of [illegible] NOR [illegible] element.

[illegible] element can be used either as a one shot [illegible] and is identified by a [illegible] box with the letters DY within the symbol. Delay [illegible] pulse duration indicated [illegible] the frequency is [illegible].

[illegible] input polar signals +6 [illegible] volts [illegible] signals 0 volt and -6 [illegible] by a rectangular box [illegible]

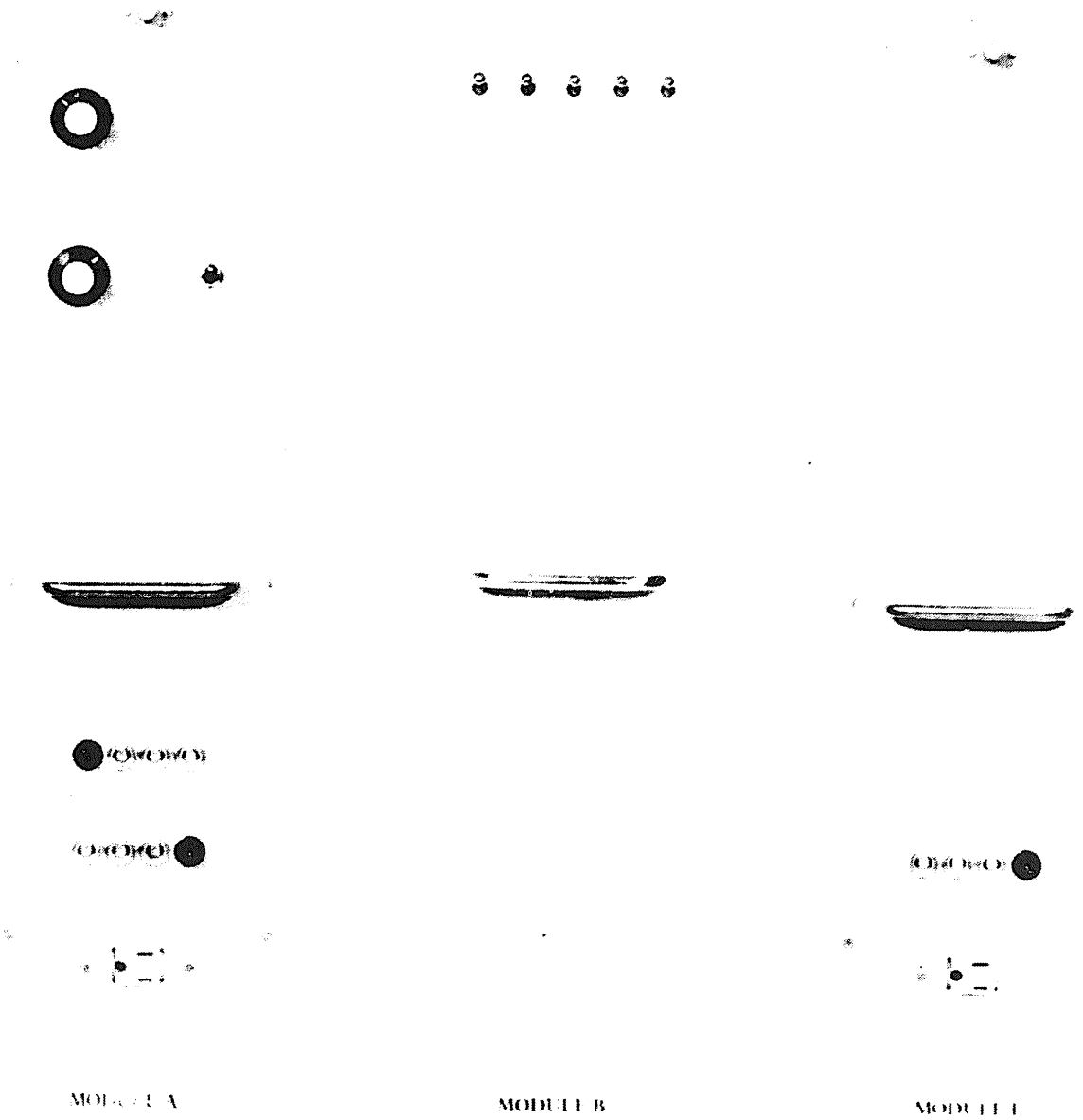


Figure 5 Master and Supplementary Modules

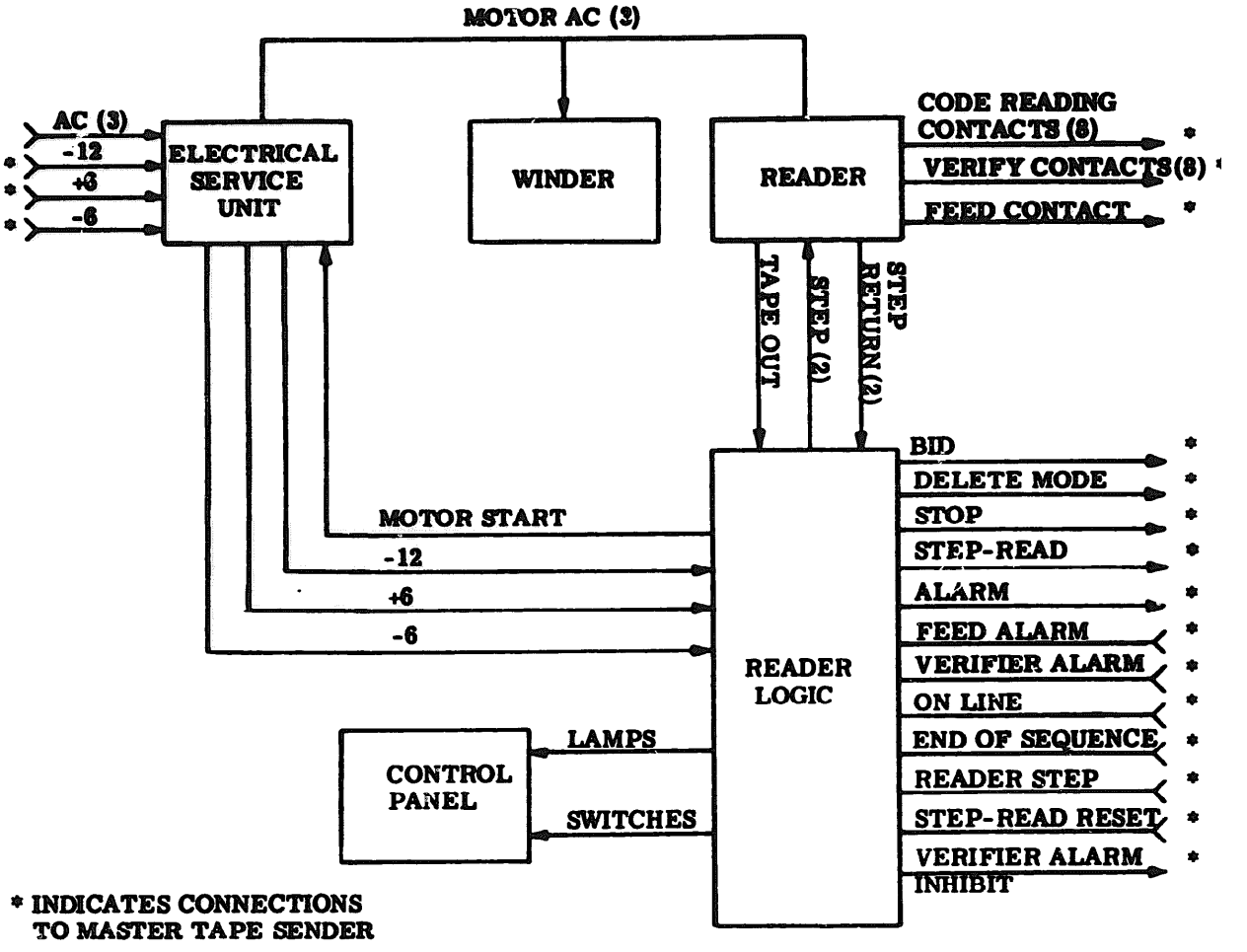


Figure 6 - Block Diagram for Supplementary High Speed Tape Sender

3.21 An output element translates neutral signal (0 volt and -6 volts) to output polar signals (+6 volts and -6 volts). It is identified by a rectangular box with OUTPUT printed within the symbol.

SUPPLEMENTARY READER LOGIC

3.22 The electronic logic circuits contained in module E are divided into the following four functional : bid circuitry, start of mo th delete circuitry, step circuitry, and alarm circ t of

A. Bid Circuitry

3.23 Insert the punched paper tape in the reading head. The normally closed tape-out contact moves to its ng head. open Position which is connected to pin C8 of JE128. This es to its action- initiates the bid circuitry of the reader logic Refer to 28. This 7742WD, Sheet 2, Figure 6. Refer to

3.24 Pin C8 of JE128 assumes a negative voltage allowing the inverter ZE102 to saturate. The 0 volt voltage output at the inverter (pin 9) is applied to the input pin B30 he 0 volt pin B30,

LA-2D ZE103, **and pin B4 of LA-2A,** ZE118. At LA-2D it is inverted, **and** applied to pin A32, LA-1D, ZE103 together with the input at pin B32. When both inputs are negative, the output on pin B34 is **driven** to 0 volt which acts as a prime voltage **for setting the flip-flop** D-B **of** ZE110 into the set one state. (Pin B33 is at 0 volt and pin B34 at a minus voltage.)

3.25 The BID indicator switch may now be operated to **provide** a transition **at** the **input, pins A36, and** B36 of flip-flop D-B of ZE110. The voltage transition switches the flip-flop to the set one state. The **two** LA networks connected between the BID switch and the complementary input are connected **as** a dc (direct current) flip-flop, to prevent switch contact bounce from affecting the set input of the flipflop.

3.26 With flip-flop D-B of ZE110 in the set one state, **pin** B34 is driven negative and pin B33 is driven to 0 volt. The 0 volt is inverted by PA-1C of **ZE108** and applied to PA-1D of ZE108. The output, pin B1 **of** PA-1D of ZE108 is driven to 0 volt, energizing relay K2 **and the motor start** relay K1 through an isolating diode CR-B of ZE110.

3.27 The diode prevents relay **K2** from being energized when the MOTORS indicator switch (SF107) located on the control panel, is operated. Refer to 7742WD. Sheet 6 for the motor circuit. When energized, the **motor** start relay K1 starts the reader and tape winder **motors.** Energizing relay K2 lights the bid indicator lamp and motor indicator lamp. The diode connected between the bid lamp and motor lamp prevents the bid lamp from lighting when the MOTORS switch is activated.

3.28 The negative voltage at pin B34 on flip-flop D-B of ZE110 is inverted to 0 volt by PA-2C of ZE108 and applied to the input pin A32 on DY-A of ZE108 for a 500 millisecond one shot. The output pin A34 is driven to 0 **volt and remains there for** a period of 500 milliseconds, at this time it returns to a negative voltage. This negative transition is applied at the input pin A31 on PA-E of ZE108 and provides a positive puke at the output, pin A27.

3.29 This puke is again delayed by an identical delay - pulse amplifier network. The results are a total delay of one second from the time a negative transition was obtained at pin B34 on flip-flop D-B of ZE110 until a pulse is provided at pin 824 on flip-flop D-C of ZE110. The associated prime input pin A24 on flip-flop D-C of ZE110 was driven to 0 volt at the time flip-flop Q-B of ZE110 was initially switched by the BID indicator switch. The flip-flop D-C of ZE110 is switched, driving the inverted output pin B26, negative. This output is applied to the input, pin B25 on LA-1C of ZE114.

3.30 **The second input of** this element, pin A24, **is supplied** by the output on PA-1C **of** ZE108 which **-samples** the normal output pin B33 **on** flip-flop D-B of ZE110. The normal output of flip-flop D-B, having been driven to 0 volt at the time the BID switch was activated, allows PA-1C section of ZE108 to provide a -5 volts to pin A24 in LA-1C of ZE114. With both inputs on LA-1C of ZE114 at a negative voltage, the output pin A27 is driven to 0 volt. This 0 volt is supplied as a BID request signal to sequence control logic in the master transmitter cabinet.

3.31 The effect of inserting tape in the reader and operating the BID switch is to immediately start the reader and winder motors, and one second later provide a BID request signal.

3.32 After operating the BID indicator switch, the operator may cancel the bid request provided action is taken prior to the receipt of the on-line signal from the sequence control logic. This reset action is accomplished by operating the BID indicator switch a second time to obtain a positive transition at the complementary input pin A36 and B36 on flip-flop D-B **of** ZE110. The prime 0 volt input at pin B35 of ZE110 is at 0 volt due to the input pins B22 and B23 on LA-2C of ZE114, both being negative. The input pin B23 was driven negative through PA-1C of ZE108 at the time flip-flop D-B was first set.

3.33 The second input to LA-2C of ZE114 samples the on-line signal from the sequence control logic. As long as the on-line signal remains negative the flip-flop D-B of ZE110 is primed to be reset. When the on-line signal goes to 0 volt, the prime 0 volt input, pin B35 is driven negative and the option for resetting the flip-flop D-B with the BID indicator switch is removed.

3.34 Flip-flop D-B can now be reset only by a tape-out indication from the reader. This tape-out indication is a positive transition at the input pin 12 of inverter ZE102 where it is inverted and applied to pin B4 on LA-2A, ZE118. If pin B3 and pin B5 on LA-2A is negative at this time a positive transition will be applied at pin B32 and pin B27 on supplementary gates of ZE110, resetting flip-flops D-B and DC of ZE110. When these fiip-flops are reset the reader and winder motors are turned off and the bid request to the sequence control logic is removed.

3.35 The negative input at pin B5 on ZE118 is a result of LA-2B on ZE118 sampling either an off-line condition or an end of sequence. If neither of these conditions exist the input at pin B5 will be at 0 volt and the tape-out indication will be prevented from resetting the above mentioned flip-flops. This logic prevents an incomplete start of message sequence to be transmitted when the tape lid is released during the sequence. The negative input at pin B3 of ZE118 is a result of LA-2A of ZE116 (refer to 7742WD, Sheet 4) STOP switch not being activated. Pressing the STOP switch while the reader is on-line and reading tape. allows the output pin A9, of ZE116 to be driven to 0 volt and applied to pin A27, CRC on ZE112. The input pin B3, LA-2A on ZE118 is driven to 0 volt, preventing output pin A9 from being driven to 0 volt and resetting flip-flops D-B and D-C on ZE110.

3.36 The power on reset circuit at Position ZE202 is used to provide a collector set pulse to flipflops D-B and DC of ZE110, a predetermined time after power is turned on. This action insures that the bid circuitry is not bidding for the line when the equipment is initially turned on. The 150 ohm, 1 watt resistors shown across the various relay contacts driving indicator lamps, are used to keep a small amount of voltage across the filament of the lamp. This reduces the initial current surge and extends the life of the lamp.

B. Start of Message Delete Circuitry

3.37 The number delete circuitry provides the operator with the option of deleting the number sequence which normally precedes each message tape. Prior to operating the BID indicator switch, the operator determixes if the message tape requires a number sequence. If the number sequence is not necessary the NUMBER DELETE indicator switch is operated. This switch provides a positive transition at the input pin A36 and B36 on flip-flop D-B. ZE112, provided the on-line signal applied at pin B14 on LA-1B, ZE114 is negative. If this on-line signal is at 0 volt, indicating the associated transmitter is on-line, the indication from the NUMBER DELETE indicator switch is held at LA-1B of ZE114 and does not switch flip-flop D-B of ZE112. Refer to 7742WD. Sheet 3.

3.38 Assume the on-line signal applied at pin B14 on LA-1B of ZE114 is negative and the signal from the NUMBER DELETE indicator switch is presented to input pin A36 and B36 on flip-flop D-B of ZE112. This flip-flop will be switched to the one state. driving the output pin B34. negative. The signal is applied to input pin A4, PA-2D of ZE108, driving the output pin Al to 0 volt, which energizes relay K4 and lights the number delete lamp through the K4 relay contact.

3.39 The negative voltage at pin B34 of flip-flop ZE112-B is also applied to pin B26 on LA-1F of ZE103. This element is held at this time due to 0 volt being supplied to pin A21 from the output B6 on PA-1C of ZE108 (refer to 7742WD. Sheet 2). When the BID indicator switch is operated, flip-flop D-B of ZE110 is switched as described in 3.25. A 0 to -5 volt transition is applied to pin A24 on LA-PC and pin A21 on LA-IF of ZE103.

3.40 The output pin A27 of LA-1C, ZE103 is held at -5 volts due to the 0 volt present at input pin B25 and output pin B28 on LA-1F of ZE103 goes to 0 volt. The resulting positive transition at the output of LA-IF is used to set flip-flop D-C of ZE112 into the one state. driving the output pin B26, negative. This voltage level is inverted by LA-ID of ZE114 and applied to the sequence control logic in the master cabinet as a delete mode signal.

3.41 At the completion of the message tape. a tape-out indication is received from the tape-out contact at the reader. This indication resets the bid circuitry as described in 3.34, and provides a negative to 0 volt transition at pin B6 on PA-1C of ZE108, (refer to 7742WD. Sheet 2). This transition is applied to pin A30 of supplementary gate ZE112, resetting flip-flop D-B of ZE112. With the reset of flip-flop D-B. the NUMBER DELETE indicator lamp is extinguished.

3.42 During normal operation (not in the delete mode) the output pin B33. on flip-flop D-B of ZE112, is at -5 volts. This is applied to the input pin B25 on LA-1C of ZE103, and permits the negative bid signal transition at pin A24 as described in 3.40. The inverted signal is passed to flip-flop DC of ZE112 as a set zero signal. This provides a -5 volt indication at the delete mode output pin F7 of JE128.

3.43 At the completion of the start of message sequence a negative going transition is received from the master logic at JE128, pin E7. The signal is inverted by LA-2E, of ZE118, and applied to pin B31 of the supplementary gate ZE112 as a reset signal for flip-flop D-C of ZE112. This reset signal is allowed to pass, provided an on-line signal is present at the prime input pin A31 of the supplementary gate. When flip-flop D-C of ZE112 is reset. the delete mode indication to the master logic is changed to 0

volt. This permits the step pulses in the master logic to be diverted from the start of message generator to the associated reader.

C. Step and Read Circuitry

3.44 During reader operation, the operator has the option of stopping the reader and stepping it manually with the STEP READ indicator switch. When the STOP switch is operated, the associated STOP indicator lamp is lit and a voltage level change from 0 to -5 volts is obtained at pin B4 on LA-2A, ZE103. The switch output is fed through a dc flip-flop configuration, similar to the circuit described in 3.25 to remove contact bounce. (Refer to 7742WD, Sheet 4.)

3.45 When the reader is operating, the on-line signal input at pin B5 of LA-2A, ZE103 is -5 volts. As a result of the negative level being applied to pin B5 of LA-2A, ZE103 and the level change from 0 volt to -5 volts at pin B4 due to the STOP switch, the output pin A9 is driven to 0 volt. The 0 volt is used as a reader stop signal to the master logic and as a prime voltage to flip-flop D-F of ZE110.

3.46 In the master logic this signal is used to inhibit the stop pulses to the start of message (SOM) generator or the reader, thereby stopping operation. The prime voltage applied at pin A2 of flip-flop D-F permits the positive transition appearing at the set input pin A1, to switch the or the reader, thereby stopping operation. The prime voltage applied at pin A2 of flip-flop D-F permits the positive transition appearing at the set input pin Al, to switch the flip-flop, driving the output pin B3, to -5 volts. The positive transition at the input, pin **Al, is a** result of operating the STEP READ switch.

3.47 The output pin B3 of flip-flop D-F on ZE110 is inverted by LA-2E on ZE116 and supplied to the master logic as a step-read pulse. This pulse allows the reader to k stepped one character, and read by the reader to k transmitted on line, provided the stop switch is in-the stop position. When the **STOP** switch is operated again, returning it to its normal position, the reader is stepped automatically by the incoming step pulse rate.

3.48 The reader may be manually stepped (off-line) during periods when the reader is not normally being stepped by the incoming step puke rate. The STEP indicator switch output is fed to a dc connected flip-flop configuration, consisting of **LA-lB,** and LA-2B on ZE116. When the **STEP** switch is operated, a positive transition is obtained at the output pin **All** of this flip-flop and applied **to LA-1B,** ZE103 for inversion prior to king applied to the input pin B13 of LA-2B, ZE103.

3.49 If the second input pin B12 of LA-2B is negative at this tune, the input at pin B13 will be inverted and appear at the output pin **All.** The input level at pin B12 is 0 volt only when the STOP switch is in its normal position and at the time the on-line signal input at pin B23 of LA-2C, ZE103 is -5 volts. When this condition is met it is assumed the reader is normally king stepped by incoming step pulses and the manuai step indications are held.

3.50 The result is, the STEP switch is available for manually stepping the reader at times when it is not reading tape and being stepped by pulses received at pin D10 on JE128. Assuming the input pin B12 of LA-2B, ZE103 is at -5 volts, the manual step pulses at pin B13 appear inverted at the output pin A11. Then the pulses are inverted twice by LA-2F, ZE103 and LA-2F on ZE116.

3.51 At the output, manual step pulses appear as positive transitions which are applied to the driver assembly. The driver assembly, located in the tape transport assembly, functions to change the low-level stepping pulses to a power level adequate for energizing the reader stepping Coils. Th pulses are delivered **to** the driver assembly from two sources, one from the STEP switch described in 3.50, and **the** other from the sequence control circuitry in the master logic. They are applied to pin D10 an **JEl28.**

3.52 The LA-IA of ZE118 performs the function of preventing an alarm indication from occuring when the reader is restarted after it has been stopped and manually stepped with the STEP switch. This is required due to the characteristics of the verify logic explained in the following paragraphs.

3.53 Input pin **A7** of **LA-lA, ZE118** samples the condition of the STOP switch. When the STOP switch is in the stop condition, the input is -5 volts. **Pin B7 of LA-1A, ZE118 sa-ples** the on-line signal, -5 volts, which is on at this point. The third input pin, **A6** of **LA-1A, ZE118** samples the STEP switch output at pin **Al7** of **LA-1B. ZE103.** When the switch **is** operated, pin **A6** of **LA-1A, ZEll8 is** driven negative, with **all** three inputs of LA-1A, **ZE118** at -5 volts. The output pin **A10 is** driven **to** 0 volt. This positive transition is applied to the master cabinet logic where it is used to prevent an alarm on reader start-up when the contacts are sampled again.

3.54 When power is turned off at the supplementary cabinet, relays **Kl** and K2 provide an open circuit at the stop signal output, pin **Cl0 of JE128,** and the step-read signal output, pin C9 of JE128. When power is turned on, the relays are prevented from energizing for a period of 80 milliseconds, after being energized, the contacts close. At this time the two outputs have had time to stabilize at -5 volts and any transitions are prevented from being applied to the master logic.

D. Alarm Circuitry

3.55 Two types of alarms are contained in the reader logic circuitry: A verify error alarm and a reader feed error alarm. When either one of these errors occur, an indication is received at pin A8 or B8 of JE128. setting an associated flip-flop **D-D** or **D-E** of **ZE110.** The flip-flops are primed by the presence of an on-line indication from the master logic. When either of the two flip-flops is set, an

associated alarm lamp is lighted and a 0 volt indication is applied at pin A1 or B1 of LA-2E, ZE103. The output pin B9 of LA-2E, ZE103 is inverted by LA-1E, ZE116 and supplied to the verifier in the master logic as a 0 volt alarm signal. (Refer to 7742WD, Sheet 5.)

3.56 **If the alarm flip-flops were to come up in the alarm condition when power is turned on, an output of the alarm circuit is required at LA-1C, ZE116. This prevents an alarm indication to the master logic. Since an alarm at any one sender prevents operation at any other sender, this condition could interrupt the step pulses to an operating sender.**

3.57 Press the VERIFIER/TAPE FEED indictor switch **(ALARM RESET on schematic) to reset alarm flip-flops and extinguish the alarm lamp or lamps. An ON-LINE indicator lamp is lighted when the on-line signal is received. The indicator lamp is a signal to the operator when a particular reader is allowed to transmit after a line bid has been entered. Relay K3 performs the same function at the output of the alarm circuitry as relays K1 and K2 performed in the step and read circuitry described in 3.54.**

MASTER TRANSMITTER LOGIC

3.58 The master transmitter cabinet contains one DX type reader with the necessary tape handling equipment. The electronic **logic** and power supply is contained in two removable modules located in the lower part of the cabinet.

3.59 The electronic logic circuits in modules A and B are similar to the reader logic in module E except for the use of relays to open intercabinet signal lines when power is off. The controlling logic circuits contained in modules A and B are divided into five functional logic systems. They are arranged for controlling up to five external supplementary tape senders plus the associated master transmitter. Refer to Figure 7 for a block diagram. The logic circuitry consists of the following logic systems: reader logic, parallel to serial converter, sequence control, verifier, and start of message generator (SOM).

A. Reader Logic

Bid Circuitry

3.60 Insert the punched paper tape in the reading head. The normally closed tape-out contact moves to its open position which is connected to pin C8 of JA128. This action initiates the bid circuitry of the reader logic. Refer to Figure 7 and 7744WD. Sheet 2.

3.69 Pin C8 of JA128 assumes a negative voltage allowing the inverter ZA301 to saturate. The 0 volt output at the inverter (pin 9) isapplied to the input pin B30 of LA-2D, ZA103 and pin A5 of LA-IA, ZA303. At LA-2D it is inverted, and applied at pin A32 of LA-ID, ZA103 Text with the input at pin B32. When both inputs are Text the output on pin B34 is driven to 0 volt which acts as a prime for the inputs at pins A36, and B36 for setting flip-flop DB of ZA110.

3.62 The BID indicator switch may now be operated to provide a transition at the input pins A36, and B36, of flip-flop D-B, switching to the set one state. The two LA elements connected between the BID switch and the flip-flop set input are connected as a dc (direct current) flip-flop to eliminate contact bounce.

3.63 With flip-flop D-B in the set state, pin B34 is driven negative and pin B33 is at 0 volt. This 0 volt is inverted by PA-1C of ZA108 and applied to PA-1D of ZA108. The output pin B1, of ZA108 is driven to 0 volt energizing relay K2, and the motor start relay K1 through an isolating diode, ZA110. This diode prevents relay K2 from being energized when the MOTORS indicator switch is operated. With the motor start relay K1 energized the reader and tape winder motors start. When relay K2 is energized the BID and MOTORS lamps are lighted. The diode (CRG101) connected between the BID and MOTORS lamps prevents the BID lamp from being energized when the MOTORS indicator switch is operated.

3.64 The negative voltage transition at pin B34 on flip-flop D-B, of ZA110 is inverted by PA-2C of ZA108 and applied at the input pin A32 of delay DY-A of ZA108. The output pin A34 is driven to 0 volt and remains at 0 volt for a period of 500 milliseconds. when it returns to a negative voltage. This negative transition is applied at the input pin A31, of PA-E on ZA108, and provides a positive pulse at the output pin A27. This pulse is again delayed by an identical delay circuit, the ‘pulse amplifier network. This results in a total delay of one second from the time a negative transition was obtained at pin B34. on D-B of ZA110 until a pulse is provided at the set input pin B24. on D-C of ZA110.

3.65 The associated prime input pin A24, was driven to 0 volt at the time flip-flop D-B was initially set by the BID indicator switch. The D-C Rip-flop is switched driving the inverted output pin B26. to -5 volts. This output is applied to the input pin B25, of LA-1C. ZA114.

3.66 The second input of LA 1C, pin A24 is supplied by the output of PA-1C on ZA108 which samples the normal output of D-B. The normal output pin B33, of D-B is driven to 0 volt at the time the BID switch is activated and allows PA-1C of ZA108 to provide -5 volts to the input pin A24 of LA-1C on ZA114. With both inputs of LA-K, ZA114 negative, the output pi A27 is driven to 0 volt. This 0 volt is supplied to the sequence control logic as a bid request.

3.67 The effect of inserting tape in the reader and operating the BID switch. is to immediately start the reader and winder motors and one second later provide a bid request to the sequence control logic.

3.68 **After operating the BID switch, the operator may cancel the bid request by operating the BID switch a second time before receipt of the on-line signal from the sequence control logic. This reset action obtains a positive transition at the complementary input pins, A36 and B36 of flip-flop D-B on ZA110. At this time the prime one input pin, A35, is at -5 volts because the output pin, B33 on D-B, is at 0 volt. This 0 voltage is applied to the input pin, B32 of LA-1D, ZA103 driving the output of this element to -5 volts.**

3.69 **At the same time, the prime 0 input pin, B35, is at 0 volt because the input pins, B22 and B23 of LA-2C, ZA114 are both negative. The input pin, B23 was driven to -5 volts through PA-1C of ZA108 at the time flip-flop D-B was first switched to the bid condition. The second input to LA-2C, ZA114 is the on-line signal from the sequence control logic. As long as the on-line signal remains negative, D-B is primed to reset. When the on-line signal goes to 0 volt the prime 0 input pin B35 is driven to -5 volts and** the ability to reset D-B with the BID switch is removed.

3.70 Flip-flop D-B can now be reset only by a reader tape-out indication in the form of a positive transition at the input pin 12, **of** inverter ZA301 where it is inverted and applied to pin **AS** of LA-1A, ZA305. If pin B7 of LA-1A is negative, at this time a positive transition will be applied at pins B32 and B27 of supplementary gates in ZA110 resetting flip-flop D-B and D-C. When D-B and D-C are reset the reader and winder motors are turned off and the bid request to the sequence control logic is removed.

3.71 The negative input at pin B7 of ZA305 is a result of LA-1C, ZA321 sampling either an off-line condition or an end of sequence. If neither of these conditions exist, the input at pin B7 will be at 0 volt and the tape-out indication will be prevented from resetting flipflops D-B and D-C. This logic prevents an incomplete start of message sequence to be transmitted when the tape lid is released during the sequence. The negative input at A6 of ZA305 is a result of LA-2A, ZA116 (refer to 7742WD, Sheet 4) STOP switch not being activated. Operating the STOP switch while the reader is on-line and reading tape, allows the output pin A10 of ZA116 to be driven negative. The resulting negative voltage is inverted by LA-2A of ZA116 and the output of 0 volt is applied to the input pin A6 of ZA305. This 0 volt at pin A6 prevents the tape-out contact from resetting flip-flops D-B and D-C of ZA110.

3.72 The power on, reset circuit at ZA401, is used to provide a collector set pulse to flip-flop D-B and D-C, a predetermined time after power is turned on. This action insures that the bid circuitry is not biding for the line when the equipment is turned on.

Start of Message Delete Circuitry

3.73 The number delete circuitry provides the operator with the option of deleting the number sequence which normally precedes each message tape. Prior to operating the BID switch the operator determines if the message tape requires a number sequence. If not, **the operator presses** the NUMBER DELETE switch, providing **a positive transition** at the input pins A36 and B36 **of flip-flop D-B on** ZA112, if the on line signal applied at **pin B14 of LA-1B,** ZA114 is negative. If this on-line signal is at **0 volt, indicating** the associated transmitter is on-line, the signal from the NUMBER DELETE switch is held at LA-1B, ZA114 and **does** not switch D-B of ZA112. Refer to 7744WD. Sheet 3.

3.74 With the -5 volts on-line **signal applied to pin B14** of LA-1B, ZA114 th**e indication from the** NUMBER DELETE switch is presented to pins A36 and **B36** of flip-flop D-B on ZA112. The D-B will be switched to the one state driving the output pin B34 negative. This -5 volts is applied to the input pin A4 of PA-2D on ZA108, driving the output pin Al to 0 volt, which energizes relay K4 and fights the NUMBER DELETE lamp through K4 contacts.

3.75 The negative voltage at pin B34 of flip-flop D-B is also applied as a prime at pin B26 of LA-1F, ZA103. The LA-1C. ZA103 is inhibited at this time due to the 0 volt supplied at pin B25 from pin B33 on D-B. **When** the BID switch is operated and D-B of ZA110 is switched as described in 3.62, a 0 to -5 volt transition is applied to pin A24 of LA-1C and pin A21 of LA-IF. ZA103. The output pin A27, of LA-1C. ZA103 is held at -5 volts due to the 0 volt present at input pin B25.

3.76 The output pin B28 of LA-1F, ZA103 is allowed to go to 0 volt due to -5 volts present at its other **input pin, B26. The resulting positive transition at the output of LA-1F, ZA103 is used to set flip-flop D-C of ZA112 into the one state driving pin B26 to -5 volts. This level is inverted by LA-1D, ZA114 and applied to the sequence control logic** as **a number delete signal.**

3.77 At the completion of a message the tape-out indication is received from the tape-out contact at the reader. This signal resets the bid circuitry as described in 3.70 and provides a -5 volt to 0 volt transition at pin B6 of PA-1C, on ZA108. This transition is applied to pin A30 of supplementary gate ZA112 providing a reset signal for flip-flop D-B of ZA112. With the reset of D-B, ZA112 the NUMBER DELETE lamp is extinguished. Refer to 7**744WD,** Sheet 2.

3.78 During normal operation (not in the delete mo**de)** pint B33 of flip-flop D-B is at -5 volts. This is applied to the pin B25 of LA-1C, ZA103 and permits a negative transition at pin A24 (3.75) to be inverted and passed to the flip-flop **D-C** as a reset signal. This pro**vides -5** volts indication at the **dele**te mode output, pin F7 of **JA128.**

3.79 A negative going transition, is received from the **start of message (referred to as SOM – module B panel) sequence generator at pin E7 on JA128, upon completion of the SOM sequence. The signal is inverted by** LA-2C, ZA305 and **applied to pin B31 of supplementary gate**

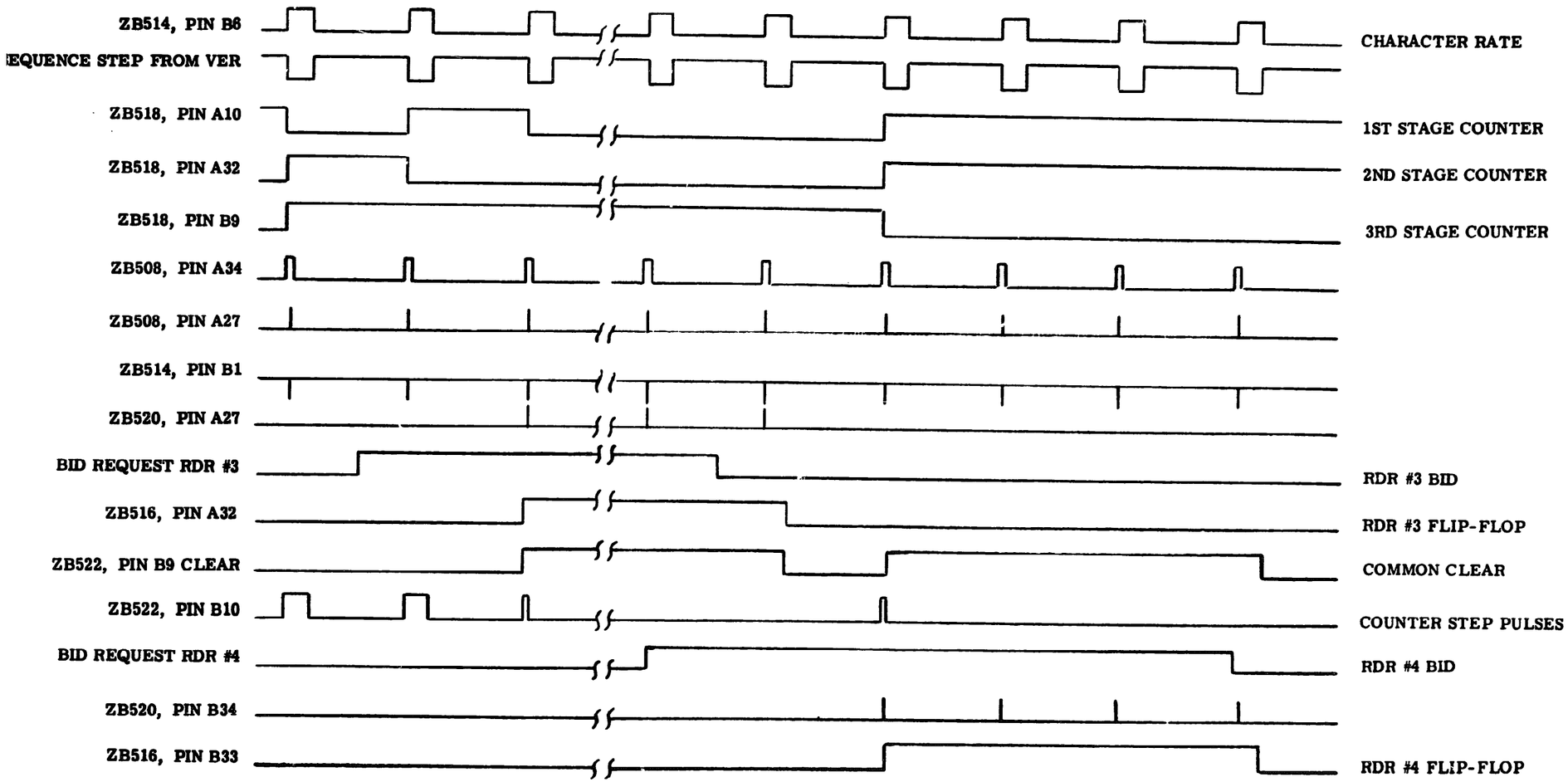


Figure 9 - Timing Diagram For Sequence Control

Figure 7 - Block Diagram for Master High Speed Tape Sender

ZA112 as a reset signal for flip-flop D-C. This reset signal is allowed to pass provided an on-line signal is present at the prime input pin A31, of supplementary D gate. When D-C is reset, the delete mode indication to the sequence control circuitry is changed to 0 volt. This permits the step pulses in the sequence control to be diverted from the SOM generator to the associated reader.

Step and Read Circuitry

3.80 During the reading operation, the operator has the option of stopping the reader and stepping it manually with the STEP READ switch. This circuit starts functioning when the STOP switch is operated and the associated STOP lamp is lighted. A level change from 0 to -5 volts is obtained at pin B4 of LA-2A, ZA103. Here again the output of a switch is fed through a dc (direct current) flip-flop configuration to remove contact bounce. Refer to

3.81 When the reader is operating, the on-line signal input at pin B5 of LA-2A, ZA103 is -5 volts. As a result of the negative level being applied to pin B5 of LA-2A, ZA103 and the level change from 0 to -5 volts at pin B4, due to the STOP switch output, pin A9 is driven to 0 volt. This 0 volt is used as a reader stop signal and as a prime to flip-flop D-F of ZA110. The signal is used to inhibit the step pulses to the SOM generator or the reader, thereby stopping operation.

3.82 The prime voltage applied at pin A2 of flip-flop D-F permits the positive transition, appearing at the set input, pin A1, to switch the flip-flop, driving the output pin, B3 to -5 volts. The positive transition at the input pin A1 is a result of operating the STEP READ switch. The output pin B3, of flip-flop D-F on ZA110, is inverted by LA-2E, ZA116 and supplied as a step read pulse. This pulse allows the reader to be stepped one character, and the character read by the reader to be transmitted on-line. To allow the reader to be stepped automatically by the incoming step pulse rate again, the operator presses the STOP switch returning it to the normal condition.

3.83 The reader may also be manually stepped off-line during periods when the reader is nor normally being stepped by the incoming pulse rate. The STEP switch output is fed to a dc connected flip-flop configuration consisting of LA-1B. and LA-2B on ZA116. When the STEP switch is operated. a positive transition is obtained at the output pin **A11,** on the dc flip-flop. This transition is applied to **LA-1B, ZA103,** for inversion prior to being applied to the nput pin B13, of **LA-2B. ZA103.**

3.84 If the second input pin, **B12** of LA-2B is negative at this time, the input at pin **B13** will be inverted and appear at the output pin, A11. The input level at pin **B12** is 0 volt only when the STOP switch is in its normal position **and** at **the** time the on-line signal input is at pin B23 of **LA-**2c. **ZA**103 -5 volts. When this condition is met it is assumed the reader is normally being stepped by the incoming pulse rate, the manual step indications must be held.

3.85 switch is available for **stepping the** reader manually except when the **reader is normally** reading tape and stepped by the into**ming step pulse** rate received at pin D10 of JA128.

3.86 **Assuming the input pin B12 of LA-2B, ZA103 is at -5 volts, the manual step indications at input pin B13 appear inverted at the output pin, A11. Then they are inverted twice by LA-2F, ZA103 and LA-1F, ZA116. At the output the manual step indications appear as positive transitions which are applied to the driver assembly.**

3.87 The driver assembly is located in the tape transport **assembly and functions to change the low-level stepping pulses to a power level adequate for energizing the reader stepping coils. The stepping pulses delivered to the driver assembly come from two sources, one is the STEP** switch described in 3.83, and the other is the sequence control circuitry in the master logic, which are applied to pin D10, JA128.

3.88 The LA-1A of ZA321 perform the function of preventing an alum indication from occuring when the reader is restarted after it has been stopped and manually stepped by means of the STEP switch. This circuit is required due to the characteristics of the verify logic.

3.89 The description of the following circuit is the same as described in 3.88. Input pin A7 of LA-1A, ZA321 samples the condition of the STOP switch. With the **STOP** switch in the stop condition, this input is -5 volts. Pin B7 of LA-1A, ZA321 samples the on-line signal which is -5 volts and on at rhis point. The third input pin, A6 of LA-1A. **ZA321** samples the **STEP** switch output at pin A17 of **LA-1B,** ZA103. When the STOP switch is operated again, pin A6 of LA-IA, ZA321 is at -5 volts. and the output pin A10 is driven to 0 volt. This positive transition is applied to the verifier logic where it is used to prevent an alarm on reader start-up when the contacts are again sampled.

Alarm Circuitry

3.90 There arc two types of alarms provided in the reader logic. a **VERIFIER** alarm and a TAPE FEED alarm. If either of these two errors occurs, an indication is received at pin **A8 or B8** of **JA128,** setting an associated flip-flop D-D **or D-E** of ZA110. These flip-flops arc primed by the presence of an on-line indication. When either of the two flip-flops is set, an associated alarm lamp is lighted and a 0 volt indication is applied at either pin Al or **B1** of LA-2E, ZA103. The output pin **B9** of **LA-2E.** ZA103 is inverted by **LA-1E.** ZA116 and supplied to the verifier as a 0 volt alarm signal. Refer to 7744WD, Sheer 5.

3.91 To reset the alarm flip-flops and extinguish the alarm indicator lamp or lamps. the operator presses the affected alarm switch An on-lilac indicator lamp is lighted when the on-line signal is received. This indicator lamp informs the operator when a particular reader is allowed to transmit after a bid for the line has been entered.

3.92 **The primary fur.ctions of the parallel to serial converter are as follows: (Refer to 7744WD, Sheets 6 and 7, and Figure 8 for block diagram).**

(a) Accepts an eight-level parallel signal, 0 volt for mark and -5 volts for a space, and converts this signal into a serialized signal output, +6 volts for mark, and -6 volts for space.

(b) Accepts a clock pulse input at the bit rate which determines the speed of operation.

(c) Provides a reader step pulse output at the character rate.

(d) Capability of working five through eight-level operation, start-stop or synchronous.

(e) Optional parallel signal output is provided.

3.93 **The parallel to serial** converter, hereafter referred to as converter. inclu**des** a four stage binary counter which is capable of a maximum count of 16. It is also capable of being reset at a specific count by the UNITS PER CHARACTER INTERVAL switch. hereafter referred to as UPC1 switch (module A). which will be explained laocr.

3.94 The counter is reset by a positive pulse coupled through diodes to the 1 side of flip-flops D-B. DC. DE, and D-F of ZA307. The positive pulse coupled to flip-flop D-B is first fed through the SIGNAL MODE switch (module A). When the SIGNAL MODE switch is in the START-STOP position. the 1 side of flip-flop D-B is reset to 0 volt by the reset pulse. When the SIGNAL MODE switch is in the SYNCHRONOUS position. the 0 side of flip-flop D-B is set to 0 volt by the reset pulse.

3.95 Clock pulses. +6 volts to -6 volts. arc fed to input circuit ZA302-A. pin 34. The input circuit converts the polar clock from 0 to -6 volts signal. 0 volt corresponding to a +6 volt input. while -6 volts corresponds to a -6 volt input. This neutral clock is inverted by LA-2D). ZA305 and fed to the input of the binary counter. The output of LA-2D on ZA305 also feeds LA-2B on ZA305. Since the clock has been inverted by LA-2D, ZA305 the counter counts at the negative going clock transitions. The outputs of all stages in the binary counter arc fed to power amplifiers which in turn feed the UPC1 switch. Refer to 7744WD, Sheet 10.

3.96 NOR gates LA-1A. LA-1B, LA-K, LA-1D, LA-1E, and LA-1F of ZA314 and LA-1B, LA-1D, and LA-1E of ZA305 and their associated OR gates ZA313-22, 21, 28, 19, 18, 17, 16, 15, and 14 detect the count in the counter. When the counter is reset in the start-stop mode, pins A32. B33 of LA 1D on ZA305, and pins A13 and B13 of OR gate ZA313-1 arc at -6 volts. The output of LA-1D, ZA2X305 is then dependent upon the other input pin B32.

3.97 **LA-1D, ZA305 samples the contents of flip-flop D-E of ZA319 when the counter is at the reset state. When there is a count of one in the counter, the output of LA-1E, ZA305 is dependent upon the input at pin B6 which samples flip-flop D-D of ZA319. Flip-flops D-F of ZA319, D-C, D-F, D-E, and D-D of ZA317; D-B, D-C, D-D, and D-E of ZA319 are sequentially sampled, each for the duration of the bit clock period. When the SIGNAL MODE switch is in the SYNCHRONOUS position, flip-flop D-E of ZA319 is not sampled.**

3.98 **The flip-flops mentioned in 3.97 stores information supplied from the verifier. If the one prime is at 0 volts, the flip-flop will store a mark when a complementary input is supplied a positive pulse. If the 0 prime is at 0 volt, the flip-flop will store a space. The primes for the storage flip-flops determine whether a mark or space is stored in a particular level. At the time a positive pulse is applied to the converter for reset, a character shift pulse is also applied to the complementary inputs of the storage flip-flops.**

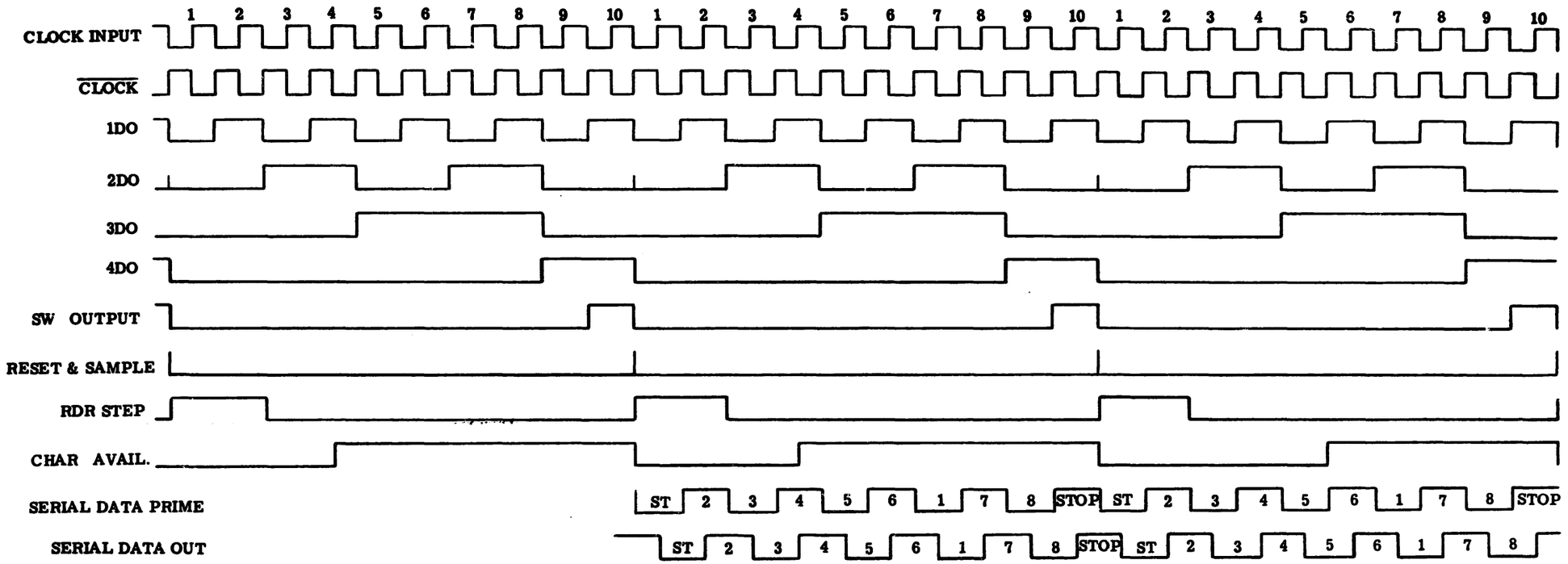
3.99 **The output of the storage flip-flops are fed to program board ZA316 where the customer has the option of either sampling the 1 or 0 sides of the flip-flops. When the 1 side is sampled, a mark at the input will be sampled as a mark at the output. If the 0 side is sampled, a** mark at the input will be sampled as a space.

3.100 The output of NOR gates LA**-1A, LA-1B, LA-1C,** LA-1D, LA-1E and LA-1F of **ZA314, and LA-1B,** and LA-1E of ZA305 are fed to LA-1F**, ZA305. The output** of LA-1D. ZA305 is fed to NOR gate **LA-1F, ZA305 only** when the **SIGNAL MODE switch is in the START-STOP** position. The output of **LA-1F**, ZA305 is the serial out**put. A** 0 volt output of LA**-1F, ZA305 represents a mark while a -6** volt level represents a space.

3.101 The counter can accept up to sixteen clock pulses before recycling. The number is dependent upon the position of the UPC1 switch. If the switch is positioned so the counter counts above eight, each subsequent clock pulse will generate a mark or stop condition, until the counter is reset and again samples the storage flipflops.

3.102 Levels eight, seven, and one from the verifier are fed through NOR gates 1-F. 1-D. and 2-D of ZA321, respectively. The outputs of these gates are fed to the converter. revels six, five, four, three and two from the verifier are fed directly to the converter. The character available signal from the verifier also feeds the converter.

3.103 The CODE LEVEL switch (module A), determines the number of code levels that arc transmitted. When the switch is in the five-level position a 0 volt level is fed to NOR gate 1-F, 1-D. and 2-D of ZA321 which inhibits these gates. When the switch is in the six-level position. NOR



SWITCH SET FOR 10 UPCI

Figure 8 - Timing Diagram for Parallel to Serial Converter

gates 1-F and 1-D are held and so on through seven and eight levels. When a level is held in this manner, a mark is generated when the storage flip-flop which stores that particular level is sampled.

3.104 The parallel signal output from the verifier is also passed through output circuits ZA323-S, ZA324-B, ZA325-A, ZA325-B, ZA324-A, ZA325-C, ZA324-C, and ZA323C. The output circuit converts its neutral input, 0 to -6 volts to a polar output +6 to -6 volts respectively. The output circuits drive integrators, and time constants are determined by the customer. The outputs of the integrators are optional parallel signal outputs.

3.105 The character available signal from the verifier is also fed to the set input two millisecond delay ZA311-A whose prime is permanently grounded. The normal output is fed to output circuit ZA326-A, and the auxiliary character available output is a two millisecond wide positive pulse.

3.106 The UPC1 switch is a four section switch which samples the outputs of the binary counter. The four poles of this switch are fed to NOR gate 1A of ZA303. Pin A8 of this gate is fed from OR gates ZA313-13 and 12 which sample the send number lead from the SOM generator. The send number is strapped to either JA128-G4, H4, G3, or H3. During the SOM sequence, the send number lead is a 0 volt which inhibits LA-IA of ZA303, and disables the UPC1 switch.

3.107 The output of LA-IA, ZA303 primes pin B4 of LA-2A, ZA303 for its other input pin ES. The latter gate thus samples the combined outputs of NOR gates 1-F, 1-D, 1-B and 1-C, of ZA303. Depending upon where the send number lead is strapped. one of the above named NOR gates will k primed while the others will be inhibited during the SDM sequence. The other inputs of these gates sample the outputs of the binary counter.

3.108 If the send number lead were strapped to JA-128H3. a count of nine in the counter will place a -6 volts at all the inputs of LA-1C. ZA303 which drives the output to 0 volt. This 0 volt level is fed to already primed LA-2A on ZA303 which inverts the signal and feeds -6 volts to the converter. This -6 volt level is then inverted again by NOR gate LA-2A and LA-2C of ZA314 and appears as a 0 volt level for a count of nine in the counter.

3.109 The outputs of NOR gates LA-2A and LA-2C of ZA314 are fed to PA-I' and PA-E of ZA311. When the next clock pulse steps the counter. the output of LA-1C of ZA303 drops to -6 volts. Consequently a negative transition appears at the input of PA-F. and PA-E of ZA311. The positive pulse resulting from the negative transition resets the counter to either 0000 or 0001 depending upon mode of operation.

3.110 The positive pulse at the output of PA-E, ZA311 is fed to the complementary inputs of the storage flip-flops. It is at this time that the information from the verifier is fed into storage and becomes the next character to be transmitted. The positive pulse is also fed to the set one input of flip-flop D-B of ZA317. Refer to 7744WD. Sheet 10.

3.111 At the end of the SOM sequence, the send number lead goes to -6 volts and holds LA-1C of ZA303 placing a -6 volt level at pin A8 of ZA303. NOR gate LA-IA, of ZA303 now samples the UPC1 switch. Depending on the position of this switch the counter is either reset on the sixth through sixteenth clock pulse (START-STOP) or fifth through sixteenth (SYNCHRONOUS).

3.112 Flip-flop D-B, ZA317 is reset when the counter steps to a count of two. The normal output of flip flop D-B is fed to LA-2E of ZA303. At the output of this gate there are negative pulses whose duration is either one or two clock pulses, depending upon the mode of operation. The interval between leading edges is determined by the UPC1 switch or send number strap connections (during the SOM sequence). This is the character interval. The output of NOR gate LA-2E of ZA303, the reader step lead, is fed to the verifier where it is used to generate various timing sequences.

3.113 The serial data output from LA-1F of ZA305 primes flip-flop D-D of ZA307. LA-1E of ZA303 inverts the serial data input applied to the prime 0 of the flip-flop in such a way that if the 0 side is primed, the one side prime is at -6 volts or the sequence may be reversed. The bit sample from the converter (which is at clock pulse time) is fed to the complementary input of flip-flop D-D, ZA307.

3.114 Previously it was stated that the counter was stepped by the inverted clock, with the bit sample at clock pulse time. Thus, flip-flop D-D is primed a half of a bit time before bit sample occurs. The output of flip-flop D-D is fed to output circuit ZA323-B where a +6 volt output represents a mark while -6 volt output represents a space.

3.115 A polar (+6 volts) abnormal traffic indication signal on input connector JA128 pin C4 is fed by external equipment to input circuit card ZA302. The output of this input card is fed to PA-1C of ZB1315. input pin A9. The output load of this power amplifier is from the coil of relay KB501-B.

3.116 With the abnormal traffic input positive, relay KB501-B is de-energized and the associated contacts arc open. Driving the abnormal traffic input negative energizes relay KB501-B. The relay contacts close providing a ground return for the abnormal traffic indicator lamp on the master and supplememtary reader cabinets.

C. Sequence Control

3.117 The sequence control logic assures that only one reader out of the six is capable of supplying signals to the verifier at any one time. (Refer to 7744WD, Sheets 13 and 14.) The circuitry shown on Sheet 13 provides for bid request inputs from up to six readers. Since the logic for each reader is identical, the sequence of operation will be described for reader number three only.

3.118 When a bid request (0 volt) is received at pin G2 of JB128 it is inverted twice by LA-X, ZB520 and LA-2F, ZB505. An inverted signal is taken from pin A26 of ZB520 to k applied to pin B25 of the flip-flop ZB516, D-C as a reset prime. The bid request input therefore primes the flip-flop at pin A24 in preparation for a set one input at pin B24. This pin receives a zero transition from the output of LA-1C, ZB520 at a time when all inputs of this gate go to a -5 volt level. Three of the inputs to this gate sample the output collectors of a three stage counter composed of flip-flops D-F, D-C and D-E, ZB518.

3.119 The one side of the first stage is sampled at pin B24, the one side of the second stage is sampled at pin B25, and the zero side of the third stage is sampled at pin A24. The fourth gate input is a character clock signal. The third step pulse input to the counter, along with the character clock input at pin A32 of LA-1C on ZB520, results in an output at pin A27 of ZB520 as shown in Figure 10. The bid signal input primes pin A24 of flip-flop DC. ZB516 at this time, as shown on Figure 10. The output of ZB520, pin A27 when applied to pin B24 of flip-flop DC, causes it to go to the set condition (Figure 10).

3.120 The resulting 0 volt at pin A32 of flip-flop D-C is also applied to NOR gate LA-1E. ZB522 where it is used as an inhibit signal for subsequent step pulses arriving at pin A2 of this gate. (Figure 9, shows these step pulses being inhibited.) The inverted output of flip-flop D-D, pin B26, which was driven to -5 volts when the flip-flop was set, drives PA-K, ZB508 into saturation.

3.121 The output pin B16 of the power amplifier provides a 0 volt on line signal to the reader logic. This signal is also applied to pin B5 of PA-2C, ZB508 driving the output pin B4 to -12 volts, de-energizing relay K-3. This opens the associated contacts and removes the ground normally supplied to the verifier logic, permitting the contacts of the associated reader to be sampled.

3.122 The inverted output side of flip-flop D-C. ZB516 also supplies a negative on-line signal to the sequence control logic. The timing diagram, Figure 9. shows the sequence of operation when reader three is given the on-line signal as described in the preceding **paragraphs. When** transmission for reader three is completed. reader four is given the on-line signal. The step clock gating circuitry. shown on 7744WD, Sheet 15, performs the function of directing the step pulses to the start of message generator or to any one of six readers. The gate network for all readers are identical so the operation for only reader one will be described.

3.123 Whether the step pulses are to be initially directed toward the start of message generator (normal condition) or the reader drive circuitry (delete mode) is dependent upon the delete prime input voltage from the reader logic. When in the normal condition (a start of message sequence is to proceed the message tape) this input voltage is negative. The negative voltage is applied at pin A7 of LA-IA, ZB524 and acts as a prime. It is inverted by LA-2E, ZB524 and applied as an inhibit signal to pin B14 of LA-1B, ZB524.

3.124 A second input to LA-IA, ZB524 is the negative on-lint signal (assuming reader one has the clear line to send) which is applied at pin B7 and also to pin B15 of NOR gate LA-1B, ZB524 as a prime voltage. Two of the three inputs to LA-IA, ZB524 are now primed. The third input, pin A6 receives negative read pulses from the output of LA-2B, ZB524, and LA-1B, ZB524 receives negative step pulses at pin A13. Since one input of LA-1B, ZB524 is at 0 volt, the output pin A17, remains at a negative voltage while the output pin A10 of LA-1A, ZB524 supplies positive pulses to the input pin B31 of LA-2D, ZB526.

3.125 The result is a negative pulse output at pin A28 which is supplied as a step pulse to the start of message generator. At the end of the fourteenth character start of message sequence the delete prime input from the reader logic changes to 0 volt. This drives the output of LA-1A. ZB524 to -5 volts and primes LA-1B, ZB524. The negative pulses appearing at pin A13 of this gate are inverted and appear at the output pin A17. as positive step pulses to reader one. These pulses are also fed to the verifier for alarm purposes.

D. Verifier

3.126 This logic accepts a step pulse from the parallel to serial converter at the character rate. The functions performed are listed in the three following groups:

(a) Inhibiting the step pulse in alarm conditions, and in the stop mode.

(b) Allow a step pulse to be passed when manually stepping the reader.

(c) Generate time slots within the character period, and reference the step pulse for reader contact sampling and verifying.

(d) Stopping the reader externally.

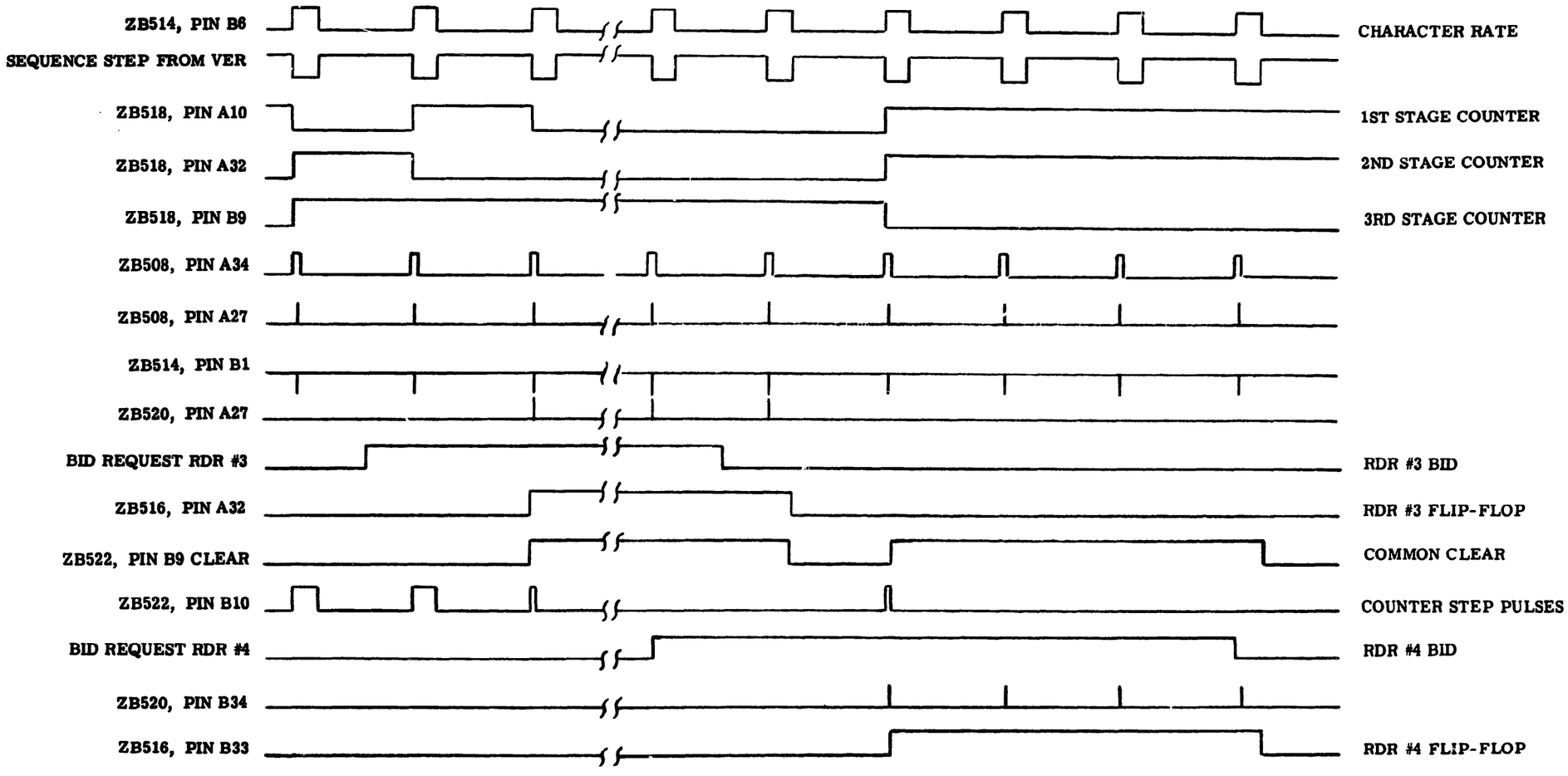


Figure 9 - Thing Diagram For Sequence Control

3.127 The **reader step** input is applied **at pin C2** of **JBl28** as a negative pulse (Figure 10). **This** pulse is **inverted by PA-2D). ZB514** and is **used to trigger a 50 microsecond delay (DY-A, ZB319).** The 50 microsecond delay is used **to delay** the application **of the step pulse** at the input, pin **A3 of PA-2D). ZB319** until after a reader stop **an** has had time to be applied to one of the **seven inputs to LA-1C, ZB324.** The reader **stop signal may be applied at** any time during reader operation or at the time a reader is given one on-line signal.

3.128 In the latter case **the** on-line to the reader logic occurs at reader step time. Therefore the reader stop signal from the master reader control or from any one of the five supplementary reader controls will be applied at one of the seven inputs to LA-1C, ZB324 at the reader step time, causing the input pin A4 of PA-2D, ZB319 to be driven to zero. disabling the input at pin A3. Fifty microseconds later the delayed step pulse will be applied at pin A3. This action permits **the** operator to bid for the line with the reader logic in the stop mode. Then manually step through the start-of-message sequence or the message tape when in the number delete mode. The seventh input to LA-1C, ZB324 pin B25, inhibits step pulses when an alarm condition is present. The eighth input to LA-1C, ZB324 pin A25, is applied through pol/neut converter ZA302 and **CR-B,** ZB108. This input is the remote stop-send signal which permits stopping the reader from a remote location.

3.129 Pulse amplifier PA-E, ZB319 provides a positive pulse at the trailing edge (negative transition) of the 50 microsecond delay (Figure **10).** The pulse is inverted by LA-X, ZB324 and applied to pin A3 of PA-2D, 28319. If a 0 volt (reader stop), signal is not present at any one of the eight inputs of LA-1C, ZB324 a positive level will appear at the output pin, A27. This level under normal conditions will be inverted by **LA-2B,** ZB522 and applied as a negative input at pin A4 of PA-2D, ZB319. The pulse appearing at pin A3 is **then** allowed to **pass** to the output pin A1, **as** a positive pulse.

3.130 If a 0 volt (reader stop) signal is present at one of the inputs to OR gate LA-1C, ZB324 (Figure 10) the output pin A27, is driven negative. This prevents the passage of step pulses at PA-2D, ZB319, pin **A3** by the presence of 0 volt at pin A4. The following paragraphs explain how a single step pulse is developed after a reader stop signal has been received.

3.131 A positive manual step signal is applied at one of the six inputs to LA-1A. ZB324 (Figure 10). It is inverted twice and used as a prime one pulse at pin **B14** of flip-flop D-D, ZB322 which is then set by the next step pulse. Flip-flop D-D and D-C, are normally in the reset state (pins B22 at 0 volt and A32 at -5 volts). When power is turned on, the flip-flops do not assume this state, the normal flow of step pulses at pins A22 and A25 will cause the flip-flops to be **driven into** this state.

3.132 When flip-flop D-D is set the output pin A22, is driven to -5 volts. Both inputs to LA-2C, ZB522 are now at -5 volts, allowing the output pin A26 to go to 0 volt which is used as a prime one input, for **flip-flop D-C, ZB322,** pin A24. On arrival of the next step pulse at pin **A25 this** flip-flop is driven to the set one state, allowing the output pin A32 to go to 0 volt [Figure **10). This** 0 **volt is** applied at pin **B12** of LA-2B, ZB522 and drives the output pin **A11,** negative.

3.133 The negative voltage at pin **A11 is** used as a **prime at** pin **A4 of PA-2D, ZB319. Fifty microseconds later** a negative pulse is applied at the second input pin **A3 of this gate** causing a positive pulse output at **pin A1 (Figure 10).** This pulse has the same time reference and is **used to perform** the same functions as the normal step pulse stream, but only one pulse is generated for each application of a manual step pulse.

3.134 After flip-flop D-C of ZB322 has **been set, it** primes itself and flip-flop D-D, ZB322 for **reset. The** output pin A32, is. 0 volt at this time. This 0 volt is applied at pin B22 of LA-2C, ZE522 and removes the prime one voltage at pin **A24** of ZB322. Pin B23 of flip-flop D-D and pin B25 of flip-flop D-C are primed for the following reader step pulse which resets both flip-flops.

3.135 The step pulses are passed through PA-2D, ZB319. The second input pin A4, of this element is -5 volts at this time. If there is no alarm indication from any one of the six readers as sampled by NOR gate LA-1E, ZB324 (7744WD, Sheet 19), and no voltage supplied to pin B25 of LA-1C, ZB324 or no external stop-send signal at pin 24 of JG106, the voltage at pin A4 of **PA-2D will** remain at -5 volts.

3.136 When an alarm indication is received. the voltage at pin A4 of the power amplifier is driven to 0 volt. This prevents step pulses appearing at pin **A3** to be passed to the output pin A1, thereby stopping reader operation. This 0 volt is **also** applied at the input pin B3. of PA-1D. **ZB319** (Sheet **19)** which de-energizces the alarm relay KB-501-A. When KB-501-A de-energizes. the transfer contact at pins **B1. C1,** and D1 of JB328 **changes** state. This indication of an alarm is supplied to external equipment.

3.137 During normal operating conditions reader step pulses are present at the output of **PA-2D). ZB319,** pin **A1.** From here the pulses are fed to the sequence control logic for stepping either the start of message generator or the reader. The step pulses arc also applied to the input pin A22 of the 800 microsecond delay DY-B. **ZB317.** The output is taken from the normal side, B27 and is au 800 microsecond positive pulse. At the trailing edge of this pulse. a positive pulse is developed by PA-F, ZB512. pin B11 (Figure 10), where it is inverted by PA-2C, ZB319 and applied as **a** negative reset pulse to the verifier logic.

3.138 **This reset pulse** the first of four time **slots** which are referenced to the step pulse and are developed within each character period. These time slots are used for reading and verifying the reader contact information. The reset pulse is used to reset the contact sampling circuit prior to reading a new character.

3.139 The second time slot is developed by 1.6 millisecond **delay,** DY-A, **ZB317** and **PA-F, ZB317.** The output pin B11 of ZB317 is inverted by **PA-2D,** 2B317 and is applied as a negative verifier sample pulse to the verifier logic. This pulse is used to sample the reader verifying contacts, and occurs 1.6 milliseconds after the reset pulse or 2.4 milliseconds after the step pulse (Figure 10).

3.140 The third time slot is developed by 110 microsecond delay **DY-B, ZB315** and **PA-E. ZB317.** This pulse is used to set the verifier alarm flip-flop D-B, ZB322 if a verifier error indication is present. The positive pulse output of pin **A27, ZB317 (Figure 10) is** inverted by LA-2D, ZB324 and applied to pin B5 of NOR gate LA-2A, ZB324. If the second input of this gate is -5 volts at this time, the pulse will be applied at the set one input pin A36, of flip-flop D-B, sampling the prime at pin A35 (refer to 7744WD, Sheet 19).

3.141 Pin B4 of LA-2A, ZB324 receives its voltage from the inverted output, Pin B10 of flip-flop DE, ZE322 (refer to 7744WD, Sheet 18). This flip-flop is normally reset, making the output 0 volt, due to the reset pulse being fed to the 50 microsecond delay, DY-B, ZB319. A pulse is also generated by PA-E, ZB512 and applied to the reset input pin **B12** of ZB322. The output pin B10, is not driven to -5 volts until an on-line and not send number signal is present at the prime one input pin A12, and a set pulse is applied at pin All.

3.142 This set pulse on pin All is developed by the 110 microsecond delay DY-A, ZB315, and PA-E, ZB315. It is the fourth and last time slot developed during the character period, and determines the time that the character being read by the reader contacts is placed in the verifier storage. This is the pulse that sets flip-flop D-E, driving pin B10 to -5 volts. Pin B4 of LA-2A, ZB324 (refer to 7744WD, Sheet 19) will not be primed until the first read pulse has occurred after an on-line is present. Therefore, the first verifier alarm sample pulse is inhibited.

3.143 The prime for the verifier alarm flip-flop D-B, ZB322 is applied at pin A35 and is supplied by the output of NOR gate LA-1B, ZB324. If all inputs of this gate are -5 volts the output is 0 volt (error condition). Input B15 is supplied by the start of message generator and is driven to 0 volt when this circuit is generating a sequence. This input inhibits a verifier alarm during the start of message sequence.

3.144 During normal reader stepping B15 of LA-1B, is at -5 volts and the second input pin A14, is at 0 volts until an error is detected. When an error is detected, input A14 is driven **negative** causing the output pin A17 to go to 0 volts, priming flip-flop D-B for the next alarm sample pulse.

3.145 When the verifier alarm flip-flop D-B is set, pin B33 goes from -5 volts to 0 volt, which is inverted by **PA-1C,** ZB319 and supplied as a negative alarm indcation to the reader logic. The alarm flip-flop is reset by the following reader step pulse applied it pin B36.

3.146 flip-flop D-F, ZB322 (refer to 7744WD, Sheet 18) is used to provide a character available signal to the parallel to serial converter and the signal gating. The flip-flop is normally reset by the delayed alarm sample pulse input at pin B1. When on on-line signal is received at the prime input pin A2, the next read pulse applied at pin A1 will set the flip-flop and provide a character available signal. It remains in this state until the next step pulse at pin B1, causes the flip-flop to reset.

3.147 If an on-line signal is still present for the next character, the following read pulse will again set the flip-flop to the character available state. This action continues until the on-line is removed or an alarm condition inhibits the read pulses causing the flip-flop to remain in the reset state.

3.148 To prevent generating a character on the line when in the external stop-send mode, a signal is received from a remote source on pin 24 of JG106 (which is normally at -6 volts). The output pin 9 of ZA302 is driven from -6 volts to 0 volt. This 0 volt is placed at input pin A25 of LA-1C and input pin Al2 of LA-2B, ZB324 through isolating diodes CR-E and CR-B of ZB108 respectively. The output pin 27 of LA-1C, ZB324 is driven negative. This puts 0 volt at input pin A4 of PA-2D, ZB319 and prevents the passage of step pulses at pin A3 of PA-2D, ZB319. The presence of 0 volt at input pin Al2 of LA-2B, ZB324 inhibits the step-read pulse at pin B12 of LA-2B, ZB324 to Pass to the output pin A11, thus preventing transmission.

3.149 The verifier logic performs the function of sampling the code reading and verifier contacts of the operating reader, placing the code reading information in storage and later clearing the storage with the verifier information. The outputs of the storage register, supply an alarm condition at the alarm sample time. if all levels of the registerare not properly cleared by the verifier information prior to this sample time.

3.150 Input provisions are made for 6 readers with 17 contacts per reader; 8 reading, 8 verify and 1 feed. Since the logic for all Ievels is identical, only level number one will be described.

3.151 Assuming reader number one is operating, the code reading contact indication is applied at pin A10 of JB228 (refer to 7744WD, Sheet 16). The verifier contact indication is applied at pin C10 of JE228, The contact

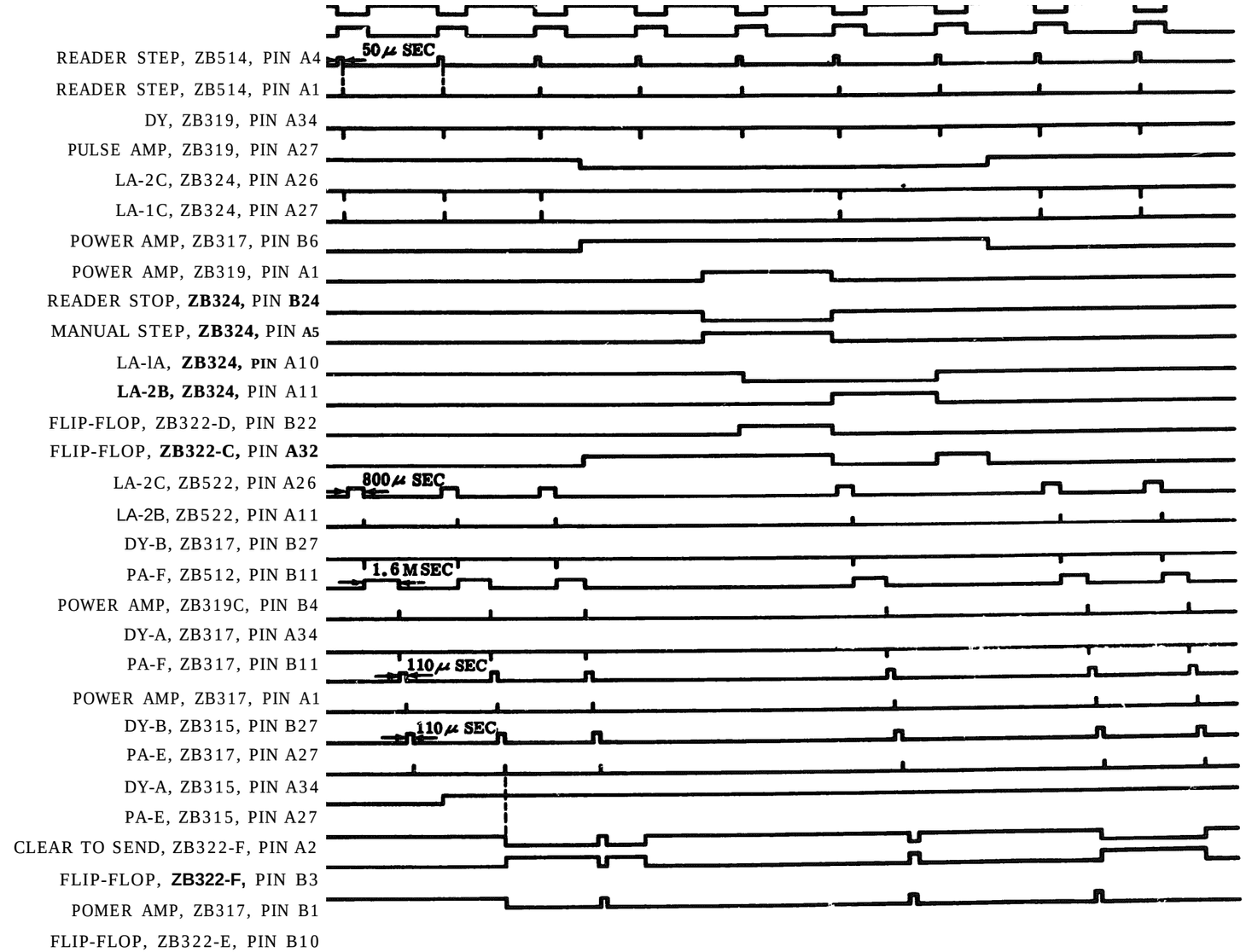


Figure 10 - Timing Diagram for Verifier

configuration for each input is as shown in the reference block. When the contact is detecting a hole (mark) it is closed to ground. When the contact is detecting no hole (space) it is open.

3.152 The code reading contact signal at pin **A10** of JB228 is applied to pin B26 of NAND **gate.** has been It will be permitted to pass to the output pin **A29,** sequence the inhibited input appearing at pin B6 of the **gate** only the opened. The other five inhibit inputs from the sequence control are held at ground at this time permitting only the contact signals from reader number one to be capable of supplying an output at pin A29.

3.153 When the contact detects a hole (mark) the output pin A29 of the gate goes to -5 volts. When a no hole (space) is detected the output is driven to 0 volt. These levels are inverted by LA-1D. ZB118 resulting in 0 volt for a mark and -5 volts for a space at the output pin B34. This output is applied to LA-2D, ZB118 which is connected in conjunction with LA-IF. ZB118 to function as a dc flip-flop.

3.154 With a mark being read by the contact, 0 volt is applied at pin B31 of LA-2D driving pin A28 to -5 volts. This -5 volts is applied to pin B36, of LA-1F. With the second input of this gate at -5 volts the output pin B28 is driven to 0 volts which is fed back to LA-2D at pin B30 clamping the network into the mark condition. The 0 volt present at the output of LA-1F is also applied to pin A29 of supplementary D gate ZB108 where it is used as a prime for the read sample pulse applied to pin B30.

3.155 The output of LA-2D which is -5 volts this time is applied at pin A30 of supplementary flip-flop ZB108 inhibiting the read sample pulse applied to pin B32. Flip-flop D-B, ZB108 is now primed to be set on the arrival of a read sample pulse, which will drive pin B33 to 0 volt. This mark condition will remain in storage until the next character.

3.156 At the beginning of the next character period, the reader is supplied a step pulse, 800 microseconds later a reset pulse is generated and supplied as a positive pulse to pin A34 of LA-1F, ZB118. At this time the reader has stepped and is now reading the next character due to the step command of the previous character. Assuming the character now being read is a space, the voltage applied at pin B31 of LA-2D is -5 volts.

3.157 When the reset pulse is applied to LA-1F. pin B28 is driven to -5 volts which is fed back to pin B30 of LA-2D. This results in pin A28 going to 0 volt and holding the output of LA-IF at -5 volts. The dc flip-flop has thereby been reset by the application of the reset pulse and is reset because the reader output is spacing.

3.158 The next pulse occurring after the reset pulse is the verify sample pulse. This negative pulse is applied at pin A7 of LA-1A, **ZB110 and is used to** sample **the output of the dc flip-flop network consisting of LA-2C and LD-2D,** 118. This output is applied to pin A6 of LA-IA.

3.159 **The gated NAND, ZB124-B is now sampling the readers verify contact, which at this time should be reading the bit previously under the read contact. Since that bit was a mark, the voltage at the gated output pin A31, is -5 volts. This -5 volts is inverted by LA-1C, ZB118 and applied to the input pin B23, of LA-2C, ZB118 driving the output to -5 volts. This voltage is sampled by the verify sample pulse.**

3.160 When it is -5 volts, **a** positive pulse is developed **at** the **output pin** A10, LA-1A of ZB110 which is applied to complimentary input pin **A36,** of flip-flop D-B. This pulse resets the flip-flop (which was set previously) driving pin B33 to -5 volts to remove the alarm indication.

3.161 The next time slot in the character period is the alarm sample pulse. This occurs 110 microseconds after the verify sample pulse. If the 0 volt at pin B33 of flip-flop D-B has not been removed by the verify sample pulse. the alarm sample pulse causes an alarm. If the code reading contact had supplied a space indication instead of a mark, flip-flop D-B would have been reset at the time of **the** read sample pulse.

3.162 One character after the read sample pulse, the verify contact would have indicated a space. which would have resulted in the inhibit voltage at the input of LA-1 A. This prevents the verify sample pulse from reaching the complementary input pin A36. of flip-flop D-B. The flip-flop remains in the reset state (pin B33 at -5 volts) and no alarm condition is detected by the alarm sample pulse which occurs 110 microseconds later.

3.163 All eight levels are treated in the same manner. When a mark is detected by the code reading contact. the storage flip-flop is set at the read sample time. If a space is detected the storage flip-flop is not set. One character later, if **a** mark is detected by the verify contact, a complementing input pulse is applied to the flip-flop. If a space is detected the complementing input pulse is inhibited and the flip-flop is not switched.

3.164 Logic identical to that described in the preceding paragraph pertaining to levels 5,6,7, and 8 appears on Sheet 17 (7744WD). The logic appearing on Sheet 20 is used for sampling and detecting a reader feed error. Gated NAND ZB120-A, samples the feed contact from up to six readers and supplies an output at pin A29. The six inhibit inputs from the sequence control logic determine which feed contact input will control the output. Only one is permitted to do so at any one time.

3.165 If any one of the six readers is receiving step pulses these step pulses will be gated and inverted at NOR 1F, ZB522. A step pulse will be developed by PA-F, ZB510 and applied as a step pulse to the four stage counter. The state of the four flip-flops is sampled by LA-1D, ZB324. If the counter is reset and then allowed to receive 15 step pulses, LA-1D, ZB324 will supply a 0 volt output at pin B34. This 0 volt level will be inverted by LA-1F, ZB324 and pubes, LA-ID, ZB324 will supply a 0 volt output at pin B34. This 0 volt level will be inverted by LA-1F, ZB324 and PA-2C, ZB514 and be supplied as a 0 volt feed **alarm** indication to the reader logic.

3.166 Normally pin A29 of ZB120-A is at -5 volts (feed contact closed). When the reader steps, the paper tape will move forcing the feed contact to open until the next feed hole is sensed by the contact. and will close again. The contact remains closed until the reader is stepped again and the contact will be forced open as before.

3.167 As a result of stepping the reader, a transition is obtained at pin A29 of ZB120-A. This positive transition is inverted by LA-21, ZB110 and applied to PA-1, ZB514. The positive pulse output of **PA-F** is applied as a reset pulse to the four stage counter.

3.168 The alarm indication is inhibited if the feed indication has been received prior to **15** step pulses, Had a feed indication not been received, the counter would not have been reset and an alarm indication would have been generated.

Signal Gating

3.169 The logic appearing on Sheet 12 (7744WD) performs the function of presenting to the Parallel to serial converter one of the three following signals:

(a) The output from the reader via the verifier register.

(b) The output of the start of message generator (SOM).

(c) The no character available signal (all levels marking).

3.170 In the no character available condition, -5 volts is applied to pin A8 of PA-X, ZB317. The output pin B4 is driven to 0 volt which is applied to eight second-level gates, driving the outputs to -5 volts. These -5 volt outputs arc inverted by eight inverters and supplied to the parallel to serial converter as 0 volt mark signals.

3.171 When the SDM generator is operating. the send number indication from the SOM generator is 0 volt. This is applied to all eight first level gates driving the outputs to -5 volts. This inhibits the reader information which is king sampled at the verifier storage.

3.172 The -5 volt outputs from the first level gates to applied to the inputs of the second level each second act **as** primes **at each** gate. A second input to each second level gate is a character available indication which is -5 volts at this time.

3.173 The two inputs of each second level NOR gate **servicing code levels 1, a** and 8 have all been supplied with -5 volts resulting in **a** 0 volt output from each gate. This is inverted and supplied as **a** -5 volt space indication to the parallel to serial comer. Since the start of message generator sequence is 5-level code only, the space indications on these remaining three levels are required to inhibit perforating these levels at the receiving set.

3.174 The output from the start of message generator is supplied to each of the five, three input second level gates, associated with code levels 2, 3, 4, 5, and 6. The 0 volt designates a mark and -5 volts designates a space. with the other two inputs primed as explained in the previous paragraph, the mark-space indication is inverted at the output of the NOR gates and again at the inverters resulting in 0 volt for a mark and -5 volts for a space. This information is supplied to the parallel to serial converter.

3.175 In the case where the reader is supplying information to the parallel to serial converter, this information is supplied at one of the inputs to each of the first level gates (0 volt is a space, -5 volts is a mark). The second input to the gates is supplied by the send number signal from the SOM generator which is -5 volts at this time. The data input is therefore inverted by the first level gates, and applied to the input of each of the second level gates.

3.176 A second input to each second level gate is the character available signal which is -5 volts at this time, as in the SOM generator output. At the output of the second level gates the reader information is 0 volt for space and -5 volts for mark. This is inverted by the inverters and applied to the parallel to serial converter as a 0 volt for mark and a -5 volts for space.

E. Start of Message Generator (SOM)

3.177 The start of message generator, referred to as the SOM generator, is explained in 2.28. The 14 character sequence is capable of being distributed at 2400 WPM, utilizing the five level Baudot code. The number display assembly (master control panel), gives a visual indication of the next number to be generated.

3.178 The SOM generator uses a four stage counter made up of flip-flops D-B, DC, D-E. and D-F, ZB307 (7744WD), Sheet 22). A detect network consisting of NOR gates LA-1 A. LA-1B, LA-1C, LA-1D, LA-1E, LA-1F, of ZB311, LA-1A, LA-1B. LA-1C, LA-1D, LA-1E, LA-1F, of ZB309 and LA-1A, LA-1D of ZB305 and LA-18 of ZB522,

which detects the count in the counter as the counter s
The outputs of the above named gates are numbered
through fourteen corresponding to the count which each
detects. The num

3.179 '44WD, Sheet gate LA-1D, ZB305 **detects the reset**
79 **The N**of the counter. The collectors of the
condition of the counter. The collectors of
flip-flops in the counter, feed NOR gates. which in turn
is **to** reduce the loading on each flip-flop in the counter.

3.180 When the counter leaves the reset condition there is at least one input of NOR gate LA-1D, ZB305 that is at 0 volt (7744WD, Sheet 23). For the duration of the SOM sequence the output of this gate is a -6 volts, this negative level is fed **to** PA-1D and PA-2D, ZB313 (7744WD, Sheet 22). Power amplifier PA-2D energizes relay KB501-C which energizes the stepping magnets located in the number display.

3.181 Relay KB501-C stays energized for the entire SOM sequence. When the counter resets, PA-2D de-energizes KB501-C and the stepping magnets. The number display steps one character. Therefore at reset, the number display steps and indicates the next message number to be sent.

3.182 The -6 volt level at pin B3 of PA-ID, ZB313 during the SOM sequence is inverted by this power amplifier, and fed to LA-1B of ZB324 (7744WD, Sheet 19) where it inhibits the verifier alarm during the SOM sequence. The output of PA-ID on ZB313 is also fed to the verifier, (7744WD, Sheet 12). During the SOM sequence, this output also inhibits the gates that sample the output of the reader.

3.183 The output of PA-1C, ZB313 (7744WD, Sheet 22), feeds three points:

(1) NOR gate LA-2F, ZB302 (7744WD. Sheet 25).

(2) Set input of DY-B, ZB512.

(3) Power amplifier PA-2C, ZB313.

During the SOM sequence. the -6 volt level appearing at the input of NOR gate LA-2F. ZB302 (7744WD, Sheet 25) is inverted and fed to the parallel to serial converter (Sheet 10) where it inhibits the UPCI switch (module A) for the duration of the SOM sequence.

3.184 The output of NOR gate LA-2F also feeds PA-ID, ZB315. During the SOM sequence, the -6 volt level at the output of this power amplifier primes the output gates of the SOM generator. At the end of the SOM sequence, the output of NOR gate LA-2F, drops to -6 volts, which enables the UPCI switch to perform its function. The output of PA-ID then inhibits the output gates of the SOM generator.

3.185 Upon reset of the SOM counter, a **positive transition appears** at **tbe output of PA-1C, ZA313, (7744WD, Sheet 22). This triggers DY-B, ZB512 since its** prime is permanently at 0 volt. The normal output is **fed to** NOR **gate LA-lC, ZB305 where it acts as an inhibiting factor for the SOM pulses which originate in the sequence control. When triggered, the delay times out** for 225 **milliseconds, inhibiting** NOR gate LA-1C.

3.186 **The purpose of applying 0 volt at pin A24, of** this **gate during this-period, is to prevent the counter from being re[illegible]. The delay is required due to the stepping mechanism which drives the number display. Since it takes a positive transition to trigger the delay, the delay will only be triggered when the counter reaches reset.**

3.187 The output of NOR gate LA-1C, ZB305 is **fed** through diode CR-C of ZB108 to the direct base input of NOR gate LA-1D, ZB305 (7744WD, Sheet 23). The positive SOM step pulses at this point prevent possible unwanted switching transients to appear at the output of NOR gate LA-ID, ZB305.

3.188 Upon receipt of the first SOM step pulse the counter steps off reset. The first gate in the detect network, LA-1A, ZB311 (7744WD, Sheet 23) detects the first count (all of its inputs are negative) and drives its output to 0 volt. During the first character interval, the other NOR gates in the detect network all have at least one 0 volt input, therefore the outputs of these gates are negative at this time.

3.189 For the first character it has been shown that the output of NOR gate LA-1A, ZB311 is 0 volt. This output is fed to NOR gates LA-IA, LA-1B, LA-1C, and LA-1D, ZB302 (7744WD, Sheet 25), where it is inverted and applied to the already primed gates LA-2E, LA-2B, LA-2C, and LA-2D, ZB302 producing a 0 volt level at the output of these gates, levels six, five, four and three respectively.

3.190 Since the input of gate LA-1E, ZB302 is at -6 volts during the first character, the output of this gate is at 0 volt. This level is inverted by output gate LA-2A, ZB302 producing -6 volts at the output of this gate. For the first character, level two is spacing while levels three, four, five and six arc marking, representing the letter V.

3.191 The second SOM step pulse steps the counter which drives the outputs of LA-IA, ZB311 to -6 volts and LA-1B, ZB311 to 0 volt (7744WD, Sheet 23), indicating a count of two in the counter. The 0 volt level at the output of LA-1B, ZB311 is fed to LA-1E, and LA-1A, ZB302 (7744WD, Sheet 25). Therefore the second character levels, three, four and five are spacing while levels two, and six are marking, generating the letter Z for the second character in the SOM (refer to 7744WD, Sheets 23 and 25).

3.192 The thid **through** eighth step pukes generate the appropriate characters. The ninth step pulse drives the output of **LA-1C,** ZB309 **to** 0 volt. which is inverted by **LA-1F,** ZB302 (7744WD, Sheet 25) and reinverted by PA-2C, ZB315. The five switches on the front panel of module **B permit** the operator to feed this 0 volt level at the output of PA-2C, ZB315 to OR gates **ZB304-22. 16, 7, 3,** and **10** for levels six, five, four, three and two respectively. This 0 volt level applied to these OR gates supplies a mark signal to these particular levels.

3.193 The tenth SOM generator step puke generates a figures character. During the eleventh step period the output of NOR gate LA-1E, ZB309 is 0 volt which is inverted by NOR gates LA-1E and LA-2E, ZB503 (7744WD, Sheet 24). The -6 volt level appearing at the outputs of the gates mentioned above, primes NOR gates LA-IA. LA-2A, LA-1B, LA-2B, and LA-1C, of ZB503. The outputs of these gates are therefore dependent upon their other inputs on pins A6, B4, B15, B12, and B25.

3.194 The inputs for the above named gates are supplied by the Baudot coded switch assembly located in the number display assembly. The outputs of these gates are fed to their number identifying inputs of OR gates ZB304-22, 11, 17, 20, and 21, and NOR gates LA-IA, LA-1B, LA-1C, LA-ID. and LA-1E of ZB302. Therefore, a -6 volt level at an input of NOR gates LA-IA, LA-2A, LA-1B, LA-2B, and LA-1C of ZB503 generates a mark in their respective level.

3.195 The next two numerical characters are generated by the same means, utilizing different levels of the Baudot coded switch. The fourteenth SOM step pulse generates a letters character during that interval. At this time the output of **PA-2C, ZB313 (7744WD.** Sheet 22) goes to -6 volts. The output of this power amplifier is fed to the reader logic (7744WD, Sheet 3). This -6 volt step is inverted and sets flip-flop DC of ZA112. The output of this flip-flop is fed to step clock gating (module B 7744WD, Sheet 15) where it prevents subsequent SOM step pulses from reaching the SOM counter and now permits the next reader step pulse to be fed to the reader logic on Sheet 4.

3.196 The fifteenth SOM step pulse causes the output of **NOR** gate **LA-lB, ZB522** to go to -6 volts. This negative transition is fed to PA-E, ZB313 (7744WD, Sheet 22) causing a positive pulse at its output. This pulse is coupled through diodes to the normal outputs of the flip-flops in the SOM counter, driving them to 0 volt, or the reset condition.

Master Transmitter Po

3.197 Alternating current (ac) **is connected at** TBG102(7744WD, Sheet7),and 0.47 microfarad bypass capacitors (for shielding purposes). The ac line is protected by circuit breaker **CRG101 (15** ampere). From this circuit breaker **(C6C101) power is** distributed to various components and assemblies throughout the **cabinet.** Power receptacle JA1 is provided and protected by its own 5 ampere circuit breaker. The POWER indicator switch controls power to all equipment in the cabinet by operating a silicon bidirectional switch SWG102. This switch provides power to the reader driver assembly (protected by its own 1-1/2 ampere circuit breaker). the power supply (protected by a 3 ampere circuit breaker). and to silicon bidirectional switch SWG 101.

3.198 The SWG101 switch is controlled by relay K1 and controls power to the reader and winder motors. Relay K1 is controlled by the MOTORS indicator switch, which controls the indicator lamp. Power amplifier PA-ID, ZA108 ca. turn on the motors even if the MOTORS switch is off by energizing K1 through CR-B. ZA110. This power amplifier also operates relay K2 which energizes the **BID** lamp and, through a diode. the MOTORS lamp. The diodes prevent a bid from being indicated when the MOTORS switch is turned on. The power amplifier input is shown on 7744WD, Sheet 2.

Supplementary Transmitter Power Distribution

3.199 The ac portions of this circuit (7744WD. Sheet 6) are exactly the same as those described in 3.197 and 3.198 except for a 10 ampere ac circuit breaker instead of 15 ampere, component designations and the addition of relay KF101. This relay operates when power is applied to the silicon bidirectional switch controlling the motors through the 4 ampere circuit breaker CBF102. When KF101 operates it connects the supplementary station equipment to the -12 volt, -6 volt, and +6 volt power supply leads. Each of these voltages is individually protected by a circuit breaker. PA-1D, ZE108 drives bid relay K2 as shown on Sheet 2.

Power Supply

3.200 The power supply (7744WD. Sheet 6) produces outputs of 28 volts. 48 volts, -12 volts. -6 volts, and +6 volts. Each of these outputs is associated with a separate winding on transformer VR1, and each output circuit has its own full-wave rectifier. filter capacitor. and bleeder resistor. VR1 is a ferroresonent transformer which compensates for power line voltage variations. The -6 volt and +6 volt outputs are electronically regulated. In the -6 volt regulator, transistors Q5 and Q6 are in parallel and connected

3.201 Transistor Q2 receives base current through R6 from the -12 volt supply. Some of this base current is diverted to ground through Q1 and CR11. Resistor R7 provides a drain for the leakage currents of Q5 and Q6. The CR11 maintains a constant voltage of -4.7 at the emitter of Q1 regardless of the current through Q1. Base current to Q1 is supplied from the output terminal through the voltage divider composed of R11, R10, and R9. If the output of the supply should go more negative the base of Q1 would go

3.202 The negative change would increase the base current of Q1, therefore increasing the collector current. This would make less current available for the base of Q2, causing a reduced current into the bases of Q5 and Q6 reducing the load voltage, correcting for the change. Similarly, if the load voltage should go less negative the base current of Q1 would be reduced, making more base current available for Q2. This would allow more current to flow through Q5 and Q6 returning the output voltage to its correct value. The +6 volt regulator operation is exactly the same as that of the -6 volt regulator except that only one series pass transistor is used.