

**DATA SET 201-TYPE
TRANSMITTER-RECEIVER
THEORY OF OPERATION
AND
SUPPLEMENTARY INFORMATION**

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B. New Sync	9	of Data Sets 201A and 201B. The information	
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G. Automatic Answer	10	required for installation, maintenance, or servicing	
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		1.02 Data Sets 201-type (Fig. 1) are fixed-rate	
		synchronous transmitter-receivers which are	
		designed to operate over voiceband facilities. Data	
		Sets 201A-type have a speed capability of 2000 bits	
		per second (bps) and are intended for DATA-PHONE®	
		service on the switched message network but may	
		also be used with private line arrangements. Data	
		Sets 201B-type have a speed capability of 2400 bps	

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and are for private line use although they may be used on the switched message network as backup for private line service.

1.03 For information on other Bell System Practices pertaining to Data Sets 201-type, refer to

Part 7 (REFERENCES). For specific information pertaining to features and options of Data Set 201-type, refer to the section entitled Data Set 201-Type, Reference Guide (590-002-100).



Fig. 1—Data Set 201—Front View

2. BASIC THEORY OF OPERATION

2.01 This is an introduction to the operation of the data transmitter, data receiver, and control circuits. This description does not contain information pertaining to interface leads. Refer to Part 4 (EQUIPMENT CHARACTERISTICS). For a more detailed study of the modulation and demodulation used in Data Sets 201-type, refer to Part 5 (DETAILED THEORY OF OPERATION).

2.02 Data Sets 201-type are transmitter-receivers which will accept serial binary data from a business machine. This input data must be in the form of positive and negative pulses as follows:

VOLTAGE	BINARY STATE	SIGNAL
Positive	Zero	Space
Negative	One	Mark

Direct transmission would require an infinite bandwidth and these pulses are therefore unsuitable for transmission over voiceband facilities having a usable bandwidth of approximately 250 to 3200 Hz. The purpose of the data transmitter is to convert these pulses to a form which can be transmitted with minimum distortion over voiceband facilities. The purpose of the data receiver is to convert the line signal back to serial positive and negative pulses.

2.03 Data Sets 201-type must operate synchronously. Data from the customer's data source must be clocked in at the bit rate (2000 bps for 201A; 2400 bps for 201B) and will be returned from the receiver at that same rate. In Data Set 201-type transmission, the timing information is contained in the line signal. The transmitting Data Set 201-type can be ordered in a version which will provide the necessary clock signals to the customer's data source (internally timed), or the data set can be obtained in a form that will accept the clocking

signal from the transmitting business machine (externally timed).

TRANSMITTER

2.04 Refer to Fig. 2 for a basic block diagram of a Data Set 201 (internally timed). The data from the business machine is clocked into the data set at a precise rate determined by the sample clock. The sample clock is a square wave at the bit rate. The data from the customer is allowed into the data set during the positive transition of the sample clock, and this data is examined during the negative transition. The data sampler examines the incoming bit to determine whether it is a one or a zero and then converts this data to a form suitable for use in Data Set 201.

Note: The detailed functioning of the data transmitter, data receiver, and control circuits will be provided in Part 5 (DETAILED THEORY OF OPERATION).

2.05 From the data sampler, the data goes to the phase modulator. The phase modulator uses the data provided by the data sampler to change the phase of the carrier frequency (the method of phase modulation will be explained later). The carrier frequency is 1750 Hz for Data Set 201A and 1800 Hz for Data Set 201B.

2.06 The process of modulating the carrier frequency with data produces undesirable frequencies. The purpose of the line-shaping circuits is to filter out the undesirable frequencies and to allow only the line signal to pass. When the transmit-receive switch is conditioned for transmitting, the data will appear on the telephone line to be sent to the distant receiver.

RECEIVER

2.07 The overall function of the receiver is to recover the data from the receiving line and to generate the necessary timing signals. Refer to Fig. 2 for a block diagram of Data Set 201. The right half of the drawing shows the data receiver.

2.08 The data received from the line is amplified and regulated in the automatic gain control (AGC) circuits. This maintains the receive signal at a constant level suitable for use by the receiver circuits.

2.09 Coming out of the AGC circuits, the line signal is split into two paths. One path is for recovering data and the other path is for recovering timing information. The demodulator extracts the data information from the line signal; however, the data must be combined with the timing information before being sent to the customer.

2.10 The line signal is fed to a high-pass filter and a low-pass filter in the sync recovery circuits. As will be explained later, part of the timing recovery information lies in the upper sideband and part is in the lower sideband. The filters obtain these signals and combine them in the filter and timing recovery circuits. The output of the timing recovery circuits is a square wave at the bit rate. The sample and data deconverter circuits demodulate the data to positive and negative pulses and combine data and timing information. The data is then clocked to the customer at the same rate at which the data was clocked into the data set at the distant transmitting end.

CONTROL CIRCUITS

2.11 The operation described so far is for a data transmitter sending data to a distant data receiver. This type of one-way transmission is known as half-duplex. Other types of private line and DATA-PHONE applications will be discussed in Part 3 (APPLICATIONS).

2.12 The control circuits described in this section are presented in Fig. 3. The two main parts are the control circuits which interface with the customer and the transmit-receive (TR) switch.

2.13 As shown in Fig. 3, when the data set is connected to a 2-wire line, only half-duplex operation is possible; that is, the data set must be either transmitting or receiving. Data Set 201-type cannot transmit and receive simultaneously over a single 2-wire line. However, if a 4-wire line is used, full-duplex operation is possible; that is, the data set can transmit over one pair and receive over the other pair. The business machine determines when the data set will transmit or receive by controlling the transmit-receive (TR) switch through voltages applied to the control circuits.

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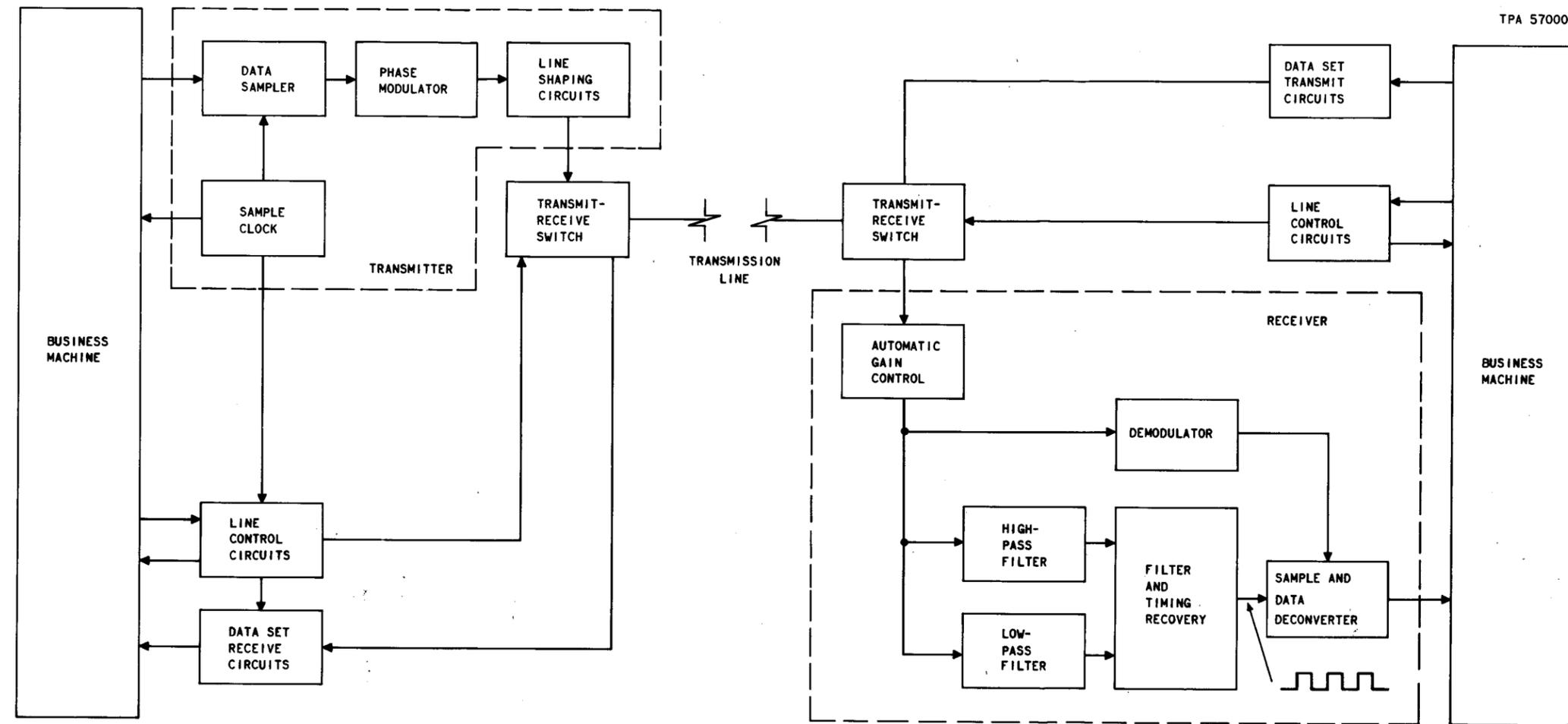


Fig. 2—Data Set 201, Block Diagram

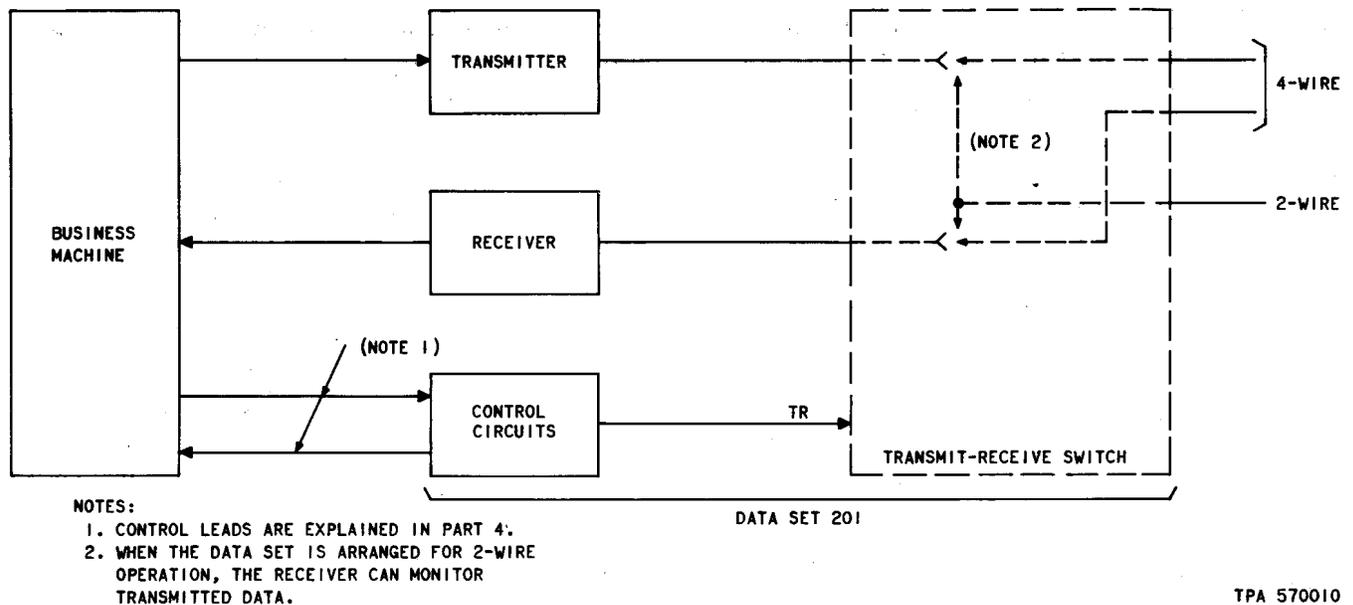


Fig. 3—Data Set 201, Control Circuits

3. APPLICATIONS

3.01 The following is a description of the various applications in which a Data Set 201 can be used. The connection diagrams for these applications are contained in Section 592-011-200, 592-011-201, or 592-011-202.

3.02 Data Set 201A is intended for DATA-PHONE service on the switched message network (DDD) but may also be used on private line arrangements. Data Set 201B is for private line use although it may be used on the switched message network as backup for private line service. In both cases, basic 3002 channels can be used. However, Data Set 201B will provide better error performance with 3002 channels with C2 conditioning.

3.03 When Data Set 201-type is arranged for 2-wire operation, the receiver is normally on line and the transmitter is idle. When the transmitter is turned on, the transmitted data is monitored by the local receiver. When the data set is arranged for 4-wire operation, the transmitted data is not monitored by the local receiver; the transmitter and receiver are independent and can be operated at the same time.

3.04 Data Sets 201-type arranged for full-duplex operation can be used in a continuous carrier mode or switched carrier mode. In both cases,

the receiver is on line at all times, and it is necessary to apply a positive voltage to the request-to-send (RS) lead while transmitting data. In the switched carrier mode, the transmitter is off when a negative voltage is applied to RS. In the continuous carrier mode, the transmitter sends an idle code of steady marks (binary 1) when RS is negative.

Note: A detailed description of all interface leads is provided in 4.18 through 4.37.

SWITCHED MESSAGE NETWORK SERVICE

3.05 DATA-PHONE service is part of the switched message network which provides, on the request of the user, point-to-point communications between terminals. DATA-PHONE service provides for the transmission of data between telephone stations, using normal dialing techniques to address the calls. The connections so established may be used alternately for voice and data communications. The voice mode may be used to coordinate the manual operation of the data terminal equipment at each end.

3.06 Switched network DATA-PHONE operation is available with all Data Sets 201-type and always includes alternate voice capability. Because switched network lines are 2-wire, normal operation is half-duplex and is usually furnished with unattended

answering capability. Data Set 201A can be used full-duplex on the switched message network if two 2-wire DATA-PHONE lines are used. However, manual calling and manual answering must be used.

3.07 Data Sets 201-type use either a 569NB telephone or Data Auxiliary Set (DAS) 804A for signaling, alternate voice, and unattended answering. Data sets equipped for contact closure interface (201A1, A2, B1, B2) use the 569NB telephone. Data sets equipped for EIA voltage interface (201A3, A4, B3, B4) use the DAS 804A. Unattended answering can be selective, under control of the AUTO button, or permanent, whereby the AUTO button is bypassed. An optional DAS 801 can be used to provide automatic calling under control of the business machine. Use of the automatic calling unit and the unattended answer capability makes possible fully automated "machine-to-machine" calls.

PRIVATE LINE SERVICE

3.08 The private line services provide 2-wire or 4-wire channels for connecting two or more terminals. The channels can be used with or without alternate voice and with or without switching arrangements. Alternate voice can be provided with a telephone or DAS 804A (as explained in 3.07). When alternate voice is provided, unattended answer may be used where applicable. The unattended answer feature operates by detecting ringing on the line and requires specially engineered private line arrangements to provide the necessary signaling.

3.09 Data Sets 201-type are compatible for use with Data Auxiliary Set (DAS) 828A and 828C. DAS 828A and 828C provide standard, prewired, tested station arrangements for terminating 4-wire private line voiceband data channels. DAS 828A can be used with or without alternate voice. DAS 828C is for use on 4-wire private line systems which have two DDD lines for backup. For more information on DAS 828A and 828C, refer to Part 7 (REFERENCES).

3.10 It is possible to provide a Data Set 201-type normally operating on a private line basis with the ability to use a DATA-PHONE line for backup. Such backup operation may be valuable in the event of temporary heavy traffic overload of the private line channels. It may also provide for the occasional transmission of data to points

which cannot economically be included in the user's private line network.

POLLING SYSTEMS

3.11 The applications discussed previously have all been of the point-to-point type; that is, one data station has access to only one other data station. Polling systems are multipoint private lines allowing a data terminal to access or to be accessed by any number of remote data terminals. The centrally located data terminal or hub can transmit data to or receive data from the remote data stations by accessing each station individually, setting up synchronization (handshaking), and either transmitting or receiving.

3.12 Polling arrangements can be used as either 2-wire or 4-wire. Because 2-wire arrangements transmit and receive on the same line (but not simultaneously), there are echo problems involved which can make the turnaround time up to 200 msec. Therefore, when messages are short and turnaround time is important, 4-wire polling is used. The hub data station can address the remote data stations on one line and can receive data on the other line. With 4-wire polling, turnaround time can be as short as 7-1/2 msec.

3.13 For transmission to the computer, several terminals may wish to transmit simultaneously. However, only one terminal can transmit and the others must wait their turn. There are two popular methods which the centrally located terminal may use to select which remote terminal will transmit next: roll-call polling and hub polling.

3.14 With hub polling, the centrally located data station works down a list of remote terminals and addresses each in turn. Some terminals may be polled more than others to give them a better response time or priority sequencing may be used. With roll-call polling, the central data station addresses only the terminal at the end of the line and the remote terminals pass the polling message down the line until all the remote terminals have been interrogated.

3.15 Turnaround time is the time necessary for the data set to switch from transmitting to receiving or from receiving to transmitting. On 4-wire private line systems where echo suppressors are not used, the turnaround time is limited by the data set and is usually about 7-1/2 milliseconds.

If the data set were being used on 2-wire lines with echo suppressors, the turnaround time would be limited by the time needed to turn around the echo suppressors. Because this time is much greater than the start-up time of the data set, an option (long clear-to-send) is provided to ensure that the data set does not begin to send data until the echo suppressors have been turned around.

Note: For more information on RS and CS, refer to the description of interface leads given in 4.21 and 4.22.

4. EQUIPMENT CHARACTERISTICS

4.01 The following is a description of the options available for Data Set 201 and a description of the interface leads.

OPTIONS

4.02 Data Sets 201-type are provided with a number of features or options which may be requested by the user. Some of these features are available as customer options; others are available as Telco engineering options. All options are added and removed by straps on the circuit boards in locations L1, L2, L4, and T10. Refer to Table A in Section 592-011-200 for information on adding or removing options on Data Sets 201A1, A2, B1, or B2. Refer to Table A in Section 592-011-201 for information on adding or removing options on Data Sets 201A3, A4, B3, or B4.

A. Terminal Impedance

4.03 The data set can be provided with either a 600-ohm or 900-ohm terminal impedance. The 600-ohm terminal impedance is used for private line service. The 900-ohm terminal impedance is used for service on the switched network and on 900-ohm private line facilities.

B. New Sync

4.04 This option may be used at the hub station in multistation arrangements, such as polling, to assure rapid synchronization between messages. Receiver clock holdover after the end of a message may interfere with the start of synchronization on receipt of the following message. A positive pulse (one millisecond or longer) is applied to the new sync interface lead (terminal 14) at the receiving station to quench the existing clock. The new

sync option is not usually used on switched service and point-to-point private lines. When the new sync option is not used, a strap is available (on circuit board L1) to ground the new sync interface lead.

C. Echo Delay

4.05 *Echo Delay Used:* When this option is provided, there is approximately 150 milliseconds of delay between request-to-send and clear-to-send. This delay allows time for the echo suppressors to turn around and for the distant receiver to establish synchronization. In addition, this option clamps the receiver for approximately 100 milliseconds after the transmitter is turned off to permit line echoes to decay before the transmitter is turned on. Generally, this option is used on 2-wire lines.

4.06 *Echo Delay Not Used. Short Clear-to-Send Interval:* When this option is used, the delay between request-to-send and clear-to-send is reduced to approximately 7-1/2 milliseconds and the receiver clamp is removed to allow fast turnaround time. Generally, this option is used on 4-wire lines where echo is not a problem.

4.07 *Echo Delay Not Used. Long Clear-to-Send Interval:* With this option, the interval between request-to-send and clear-to-send is approximately 150 milliseconds. However, the 100-millisecond receiver squelch is not provided (as it is for the *Echo Delay Used* option). This option is used on 4-wire lines when the customer requires a longer start-up time for synchronization of equipment.

D. 2-Wire or 4-Wire

4.08 *2-Wire:* With this option, half-duplex (alternate one-way-at-a-time) operation is required. When the data set is transmitting, the transmitted data appears on the received data lead (interface pin 3) to provide a local copy.

4.09 *4-Wire:* This option makes full-duplex operation possible. The data set can transmit and receive simultaneously and independently. With the carrier controlled by request-to-send, the data set can transmit (carrier is *on*) when the request-to-send lead is *on*. The data set transmitter is off when request-to-send is *off*. With the continuous carrier option, the data set can transmit

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when request-to-send is on; however, when request-to-send is off, the data transmitter sends an idle code of steady marks (binary 1).

E. Transmitter Output Level

4.10 Data Sets 201-type have options to provide a transmitter output level of 0, -2, -4, -6, or -8 dBm. In this way, a specified signal level as low as -8 dBm can be provided by the data set. However, present tariffs specify that the data power level reaching the serving central office shall be no greater than -12 dBm. Therefore, on loops where the loss is less than 4 dB, an external pad must be added to the line as specified in Section 592-011-201.

Note: Data Sets 201A and 201B list type do not require an external pad.

F. Receiver Signal Level

4.11 This option allows selection of the range of received signal level. By adding attenuation in 6-dB steps, the receiver may be changed from its most sensitive range to its least sensitive range. This sensitivity range is also affected by the compromise equalizer. With the compromise equalizer out, the receiver sensitivity is variable from -50 to -2 dB, depending on the option used. With the compromise equalizer in, the sensitivity is variable from -42 to +10 dB, depending on the option used.

4.12 The compromise equalizer is required for switched network (DDD) applications. This equalizer is an amplitude and delay equalizer and is a compromise equalizer in that it is designed to correct for the average slope distortion and envelope delay distortion encountered on switched facilities.

G. Automatic Answer

4.13 Data Sets 201A1, A2, B1, and B2 are equipped with an electromechanical automatic answer unit. This automatic answer unit provides a 0 volt or +6 volt indication on the interlock (IT) lead and responds to contact closures on the remote release (RR) lead, the remote control (RC) lead, and the ring indicator (RG1 and RG2) leads. All other interface leads conform to EIA specification RS-232-B. This automatic answer unit is used with the 569-type telephone set, which also provides an alternate voice capability.

4.14 Data Sets 201A3, A4, B3, and B4 (and all Data Sets 201 list type) are compatible with Data Auxiliary Set (DAS) 804A and will respond to both contact and voltage signals on the remote control (RC) lead and the ring indicator leads. If desired, these sets can be provided with an interface which conforms to EIA specification RS-232-B. The DAS 804A provides automatic answering and alternate voice capability.

4.15 Data Sets 201-type can be equipped with either selective or permanent automatic answer. With selective automatic answer, the AUTO ANS button on the DAS 804A or key telephone set must be depressed to enable the data station to answer automatically an incoming call. With permanent automatic answer, the AUTO ANS button is bypassed.

H. Control Lead Interface

4.16 The control leads affected by this option are the interlock (IT) lead, the remote control (RC) lead, the remote release (RR) lead, the ready (RDY) lead, and the ring indicator (RG1 and RG2) leads. When the EIA voltage interface lead is provided, the interlock lead, the remote control lead, and the ring indicator 1 lead conform to EIA specification RS-232-B. The remote release lead, the ready lead, and the ring indicator 2 lead are not used.

4.17 When the contact closure interface is provided, the interlock lead provides a 0 voltage for an *off* condition and +6 volts for an *on* condition. The remote control lead, the ready lead, the remote release lead, and the ring indicator leads respond to contact closures as specified in 4.32 through 4.36.

INTERFACE LEADS

4.18 The following is a description of the interface leads between Data Set 201 and the business machine. For a summary of the interface leads and their designations, refer to Table A. Table A also shows the pin numbers to which the various interface leads are connected.

4.19 **Send Data:** The business machine transmits positive and negative voltages to the data set on the send data (SD) lead. Positive voltages of +5 volts or greater are interpreted by the data set as a "space" or binary 0. Negative voltages of -5 volts or more are interpreted as a "mark"

TABLE A
CUSTOMER INTERFACE CONNECTIONS

J2 PIN NO.	EIA STANDARD NOMENCLATURE	DATA SET 201A AND 201B DESIGNATIONS
1	Protective Ground (AA)	Frame Ground (FG)
2	Transmitted Data (BA)	Send Data (SD)
3	Received Data (BB)	Received Data (RD)
4	Request to Send (CA)	Request to Send (RS)
5	Clear to Send (CB)	Clear to Send (CS)
6	Data Set Ready (CC)	Interlock (IT)
7	Signal Ground (AB)	Signal Ground (SG)
8	Data Carrier Detector (CF)	Carrier On (CO)
9	Reserved For Data Set Testing	Positive Battery (+12V)
10	Reserved For Data Set Testing	Negative Battery (-12V)
11	Unassigned	Not used
12	Unassigned	Not used
13	Unassigned	Not used
14	Unassigned	New Sync (NS)
15	Transmitter Signal Element Timing (DB)	Serial Clock Transmitter (SCT)
16	Unassigned	Dibit Clock Transmitter (DCT)
17	Receiver Signal Element Timing (DD)	Serial Clock Receiver (SCR)
18	Unassigned	Dibit Clock Receiver (DCR)
19	Unassigned	Remote Release (RR)*
20	Data Terminal Ready (CD)	Remote Control (RC)*
21	Unassigned	Ready (RDY)*
22	Ring Indicator (CE)	Ring Indicator 1 (RG1) †
23	Unassigned	Ring Indicator 2 (RG2) †
24	Transmitter Signal Element Timing (DA)	Serial Clock-Transmitter-External (SCTE)

* When contact interface is used, these leads are for unattended answering and are used for terminating dialed calls. When voltage interface is used, the Remote Control (RC) lead performs this function, and leads 19 and 21 are not used.

† When contact interface is used, these leads indicate to the customer when a ringing signal is present on the line. When voltage interface is used, the Ring Indicator 1 (RG1) lead performs this function, and lead 23 is not used.

or binary 1. The data set receives data from the business machine on this lead at the time of the positive transition of the serial clock transmitter (SCT) signal on pin 15 and samples the bit at the time of the negative transition.

4.20 Receive Data: Data received from the line is converted to positive and negative voltages which are clocked out on the receive data (RD) lead to the business machine. The polarities on this lead agree with those on the SD lead. Data should be sampled by the business machine on the negative transition of serial clock receive (SCR), pin 17.

4.21 Request to Send: When the business machine is ready to transmit data, a positive voltage is applied to this lead; otherwise, the voltage should be negative. After applying the positive voltage, the business machine should then look for a positive voltage on the clear to send (CS), pin 5. For minimum delay between RS and CS, the positive-going RS pulse should be coincident with the positive-going dibit clock transmitter (DCT) pulse, pin 16. (DCT cannot be used on externally timed data sets.) RS should remain positive until at least 100 microseconds (μ sec) after the last data bit is sampled on the negative transition of SCT, pin 15. When RS is made negative at the end of a message, the carrier remains on for about 2 milliseconds (msec) to clear the transmitter.

4.22 Clear to Send: The voltage on this lead is negative when RS is negative and positive when RS is positive. The CS signal responds with some built-in delay, depending on the configuration. During this delay, the data set transmits a steady mark (binary 1s) to synchronize the distant receiver. The turn-on delay between RS and CS for 2-wire applications is about 150 to 200 msec to allow time to disable line echo suppressors and to synchronize with the distant receiver (echo delay used option). For 2-wire applications, the receiver is held off for about 100 msec after RS is made negative to allow echoes on the line to decay. The turn-on delay between RS and CS for 4-wire applications is approximately 8-1/2 to 9-1/2 msec for Data Set 201A and 7 to 8 msec for Data Set 201B. For minimum delay, RS should be made positive on a positive transition of DCT.

4.23 Interlock: The interlock (IT) lead provides an indication to the business machine when

the data set is in the data mode, that is, transmitting or receiving. If the data set is arranged for data-only operation, the indication on the IT lead will be in a steady *on* state. If the data set is equipped for contact closure interface, an *on* indication is +6 volts and an *off* indication is zero to +0.5 volts. If the data set is equipped for EIA voltage interface, an *on* indication is +6 volts and an *off* indication is -6 volts.

4.24 Signal Ground: This is a reference point for all voltages. Signal ground (SG) is common with frame ground (FG), pin 1.

4.25 Carrier On: The carrier on (CO) lead provides an indication to the business machine that data signals are being received by the data set. The voltage on this lead is positive when line signals are present at the receiver and negative at other times. If CO is negative, RD (pin 2) will be clamped negative and the receive clocks (serial and dibit) will be clamped positive. In 2-wire operation, the CO indication will be positive when the data set is transmitting. This allows the transmitted data to be monitored by the receiver. The turn-on delay of CO is 2 to 9 msec and the turn-off delay is about 10 msec.

Note: The CO indication is an energy detector and will respond to high noise levels on the line.

4.26 Positive and Negative Battery: These are +12 and -12 volts present at the interface. These voltages are to be used only for data set testing.

4.27 New Sync: This lead may be used at the hub station of multistation arrangements, such as polling, to assure rapid synchronization between messages. This is necessary because of receiver clock holdover after the end of a message which may interfere with the start of synchronization on receipt of the following message. A positive one msec pulse (or greater) is applied (by the business machine) to this lead at the receiver to quench the existing clock. At all other times, the applied voltage must be negative and supplied from a low-impedance source. Use of new sync (NS) is recommended when the time between messages is less than 100 msec. When the new sync option is not used, an internal strap on the L1 circuit pack is provided to bypass it.

4.28 Serial Clock Transmitter: A square wave bit rate clock signal appears on this lead for internally timed data sets. This signal may be used to time up to eight externally timed data sets. The leading edge of the signal on SD, pin 2, should be presented by the business machine on the first positive transition of SCT after CS, pin 5, has gone positive. The SCT lead is common with the serial clock transmitter external (SCTE) lead, pin 24.

4.29 Dibit Clock Transmitter: In data sets using internal timing, a square wave clock signal at one-half the bit rate appears on this lead. Transitions in DCT coincide with the positive-going signal on SCT. The DCT clock signal is not available for use by the business machine on externally timed data sets.

4.30 Serial Clock Receiver: This lead provides a square wave timing signal derived from dibit clock receiver (DCR), pin 18. The business machine should sample the received data on the negative transition of SCR. This signal contains jitter and is not suitable for providing external timing to another data set.

4.31 Dibit Clock Receiver: This lead provides the recovered received clock at one-half the bit rate. Positive-going changes in SCR, pin 17, coincide with transitions in DCR.

4.32 Remote Release: On data sets equipped for contact closure interface, this lead is used in conjunction with the remote control (RC) lead as explained in 4.33. If the data set is equipped for EIA voltage interface, the RR lead is not used.

4.33 Remote Control: On data sets equipped with the unattended answer feature, this lead is used to control the status of the data set. If the data set is equipped for contact closure interface, the business machine must furnish a contact closure between the RC lead and the ready (RDY) lead. This can be a permanent strap if desired. When the business machine detects an incoming call by the status of the ring indicator (RG1 and RG2) leads, it must provide a contact between RC and the remote release (RR) lead or the data set will not answer the call. This closure must be maintained for the duration of the call. If the data set is equipped for EIA voltage interface, the business machine detects ringing by the status of the RG1 lead, and the data set will not answer

the incoming call until the RC lead goes positive. This positive voltage must be held for the duration of the call.

4.34 Ready: If the data set is equipped for contact closure interface, this lead is used in conjunction with the RC lead as explained in 4.33. If the data set is equipped for EIA voltage interface, the ready (RDY) lead is not used.

4.35 Ring Indicator 1: On data sets equipped with the unattended answer feature, this lead is used to signal the business machine during the ringing cycle of an incoming call. This function is accomplished in two different ways, depending upon the data set interface.

(a) If the data set is equipped for contact closure interface, this lead is connected to ring indicator 2 (RG2) during the ringing cycle of an incoming call.

(b) If the data set is equipped for EIA voltage interface, a positive voltage appears on this lead during ringing and a negative voltage appears at all other times.

4.36 Ring Indicator 2: This lead is used in conjunction with the RG1 lead as explained in 4.35 (a). If the data set is equipped for EIA voltage interface, this lead is not used.

4.37 Serial Clock Transmitter External: On externally timed data sets, this lead is used by the business machine to furnish bit rate timing to the transmitter. The timing signal must have a frequency of 2000 Hz \pm 0.01 percent for Data Set 201A or 2400 Hz \pm 0.01 percent for Data Set 201B. This timing signal must have a 49.5 percent to 50.5 percent duty cycle. This terminal is common with SCT, pin 15.

5. DETAILED THEORY OF OPERATION

5.01 There are three methods of modulating a sinusoidal carrier: amplitude, frequency, and phase modulation. All three find use in digital data transmission. Amplitude modulation (AM) systems suffer from sensitivity to level changes and noise. Frequency modulation (FM) systems require excessive bandwidth to gain noise advantage over AM. Phase modulation systems (as used for digital data transmission) are designed to detect phase changes and are therefore rather insensitive to level changes and noise.

5.02 Using phase modulation, it is practical to encode in multiple-phase positions and thus attain a higher data rate at no increase in line signaling rate. For these reasons, phase modulation has found favor as a practical method of high-speed data transmission in limited bandwidths. These desirable characteristics are achieved at some expense in data set complexity.

5.03 Data Sets 201-type use 4-phase modulation to encode data on the carrier wave. The data is encoded on the carrier wave as a succession of signal element phase shifts, each of which is an odd multiple of 45° with respect to the previous signal element phase. In order to encode by means of these four phase shifts, the serial data as received by the transmitter is examined as pairs of binary digits called dibits. Since there are four possible dibit combinations (00, 01, 11, 10), each of the four phase shifts may be associated with one of the dibit codes. This means that the phase of the carrier for a particular dibit is shifted by some predetermined amount with respect to the phase just transmitted for the previous dibit. This is to be contrasted to phase-modulation systems where the phase shift is in reference to a fixed phase. This scheme makes it unnecessary to transmit absolute phase information.

5.04 The way that data is encoded provides a phase shift for each new dibit regardless of what dibits or succession of dibits are received. The fact that the signal element phase is continually shifted enables the receiver to recover the necessary synchronization information. The operation of the bit synchronization recovery circuit which accomplishes this recovery will be explained in detail in the text.

5.05 The data is recovered by measuring the relative phase angle between the received signal element and the previous signal element delivered by a delay line (stored reference). The transmitter coding is such that one bit is determined by comparison to the delayed output, while the other bit is determined by comparison to a delayed output, the phase of which is shifted by 90° . Pairs of bits are identified simultaneously but delivered serially to the receiver data output circuit under control of the recovered timing synchronization signal. This clock signal also is supplied to the customer.

TRANSMITTER

5.06 While there are several ways in which data can be encoded into relative phase positions, Data Sets 201A and 201B use the same basic method, differing only in details. As shown in Fig. 4, the transmitter has two separate sources of carrier called Channel A and Channel B. These channels alternate in supplying the line signal, with the transfer from one channel to the other taking place gradually once each dibit. In other words, the signal from Channel A will be "on-line" for one dibit, Channel B the next, and so on. During the time the Channel A is supplying the line signal, its phase is held constant, and it is during this time that the phase of Channel B (which is "off-line") is changed to the value that it will have during the next dibit interval.

5.07 The necessary phase changes, therefore, are made at a time when the channel being changed is not supplying the line signal. This technique produces a line signal which changes phase gradually as the signal from one channel takes over from the other. Abrupt phase changes, which would "splatter" energy over a wide frequency spectrum, are avoided.

5.08 As will be discussed later, the data will be recovered in the receiver by comparing the phase of the line signal corresponding to one dibit with the phase that existed during the previous dibit. This is called a "stored reference" system. This relative phase we will call the "epoch angle," and the relationship between it and the incoming data is shown in Fig. 5. It is important not to confuse the epoch angle (change of carrier phase) with the absolute phase of the carrier. These are different parameters although they are closely related.

5.09 Another parameter which is easy to confuse with the epoch angle is the shift in line signal phase that accompanies the transfer from one channel to the other. This shift is the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next and is known as the "tail-to-head" or "transition" angle. The epoch angle is the difference in phase between the line signals at the beginning of two successive dibit periods or "head-to-head" angle. These are not the same because there is not an integral number of carrier cycles per dibit.

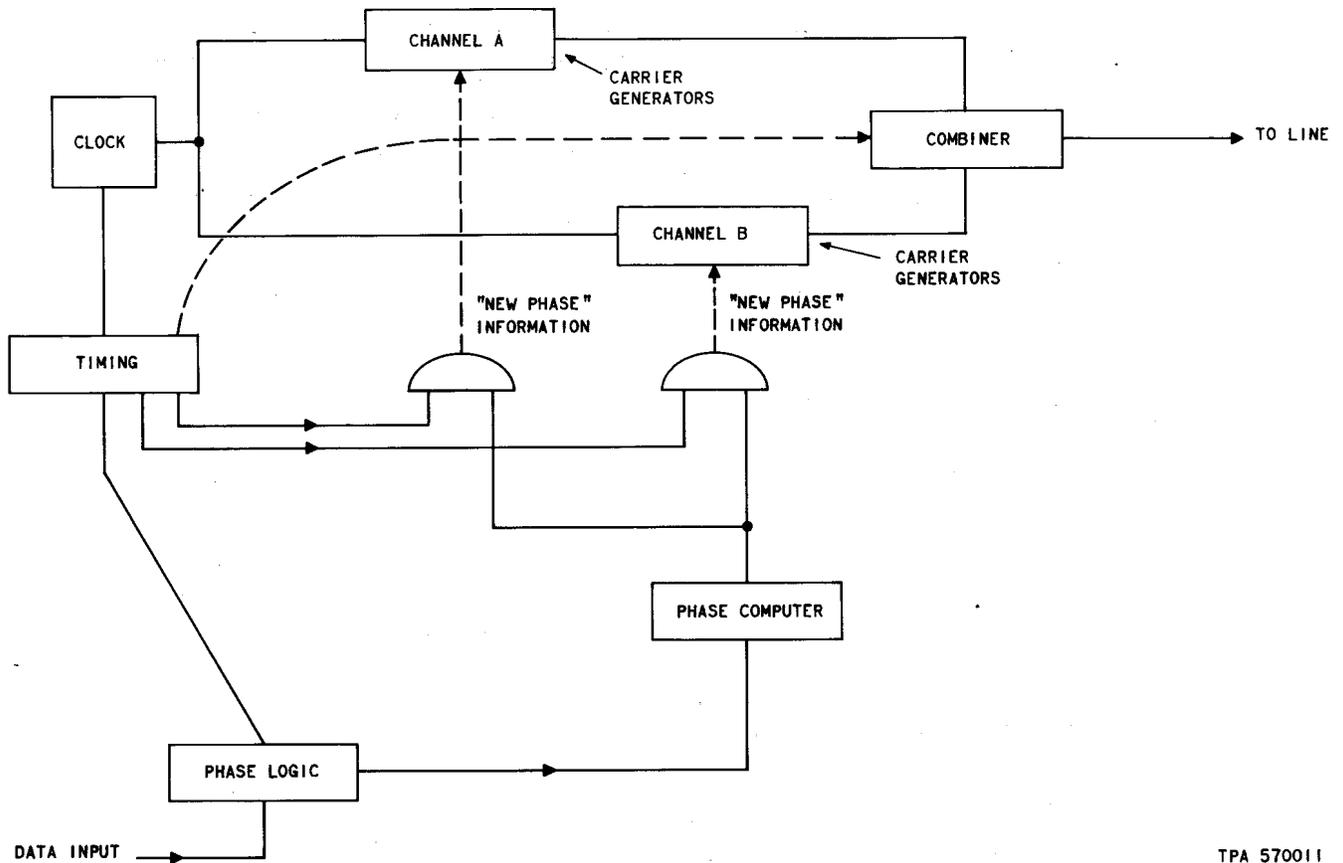


Fig. 4—Block Diagram of Transmitter

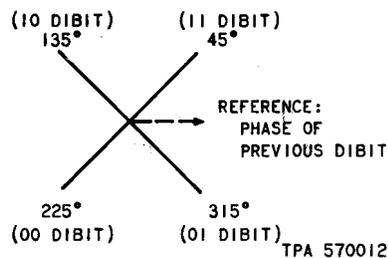


Fig. 5—Epoch Angles

5.10 The circuit description in this section will be confined to Data Set 201A with the internal timing option. While the basic principles of operation with external timing or of the other data sets in the 4-phase family are the same, there are many differences in details.

5.11 As just discussed, the receiver compares the phase of the line signal with its phase

one millisecond earlier in time (one dibit interval). This difference in phase is defined as the "epoch angle." The transmitter circuits produce the proper epoch angles in the line signal by controlling the initial phase of the carrier generated for each dibit, ie, the phase of the carrier at the beginning of the dibit interval.

5.12 With the "2-channel" technique and epoch angles that are odd multiples of 45°, it can be shown that there are only eight possible phases of line signal. Furthermore, these phases are divided into two families of four orthogonal phases, one for each channel, which are spaced 45° apart. This is shown in Fig. 6.

5.13 For each dibit in the incoming data, the transmitter circuits create the proper epoch angle in the line signal by (1) computing the new carrier phase to be transmitted, (2) setting the "off-line" channel to produce that phase of carrier until instructed further, and (3) switching channels.

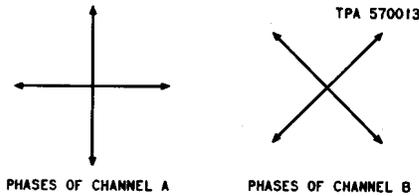


Fig. 6—Eight Possible Carrier Phases

5.14 In the 201A, all of these transmitter operations are locked to a crystal oscillator clock running at 14,000 Hz or eight times the carrier frequency. As shown in Fig. 7A, the carrier frequency F_c is generated by binary counters that divide the clock signal by eight. Details of these carrier generators are covered later and are shown on another figure.

5.15 Another output from the clock is passed through successive stages of frequency division to produce the many timing signals used within the set and by the customer's equipment. The first stage is a division by seven, which produces the SCT signal or "bit clock." This is a square wave at 2,000 Hz and is furnished to the customer for clocking his source of data at the precise rate required by the 201A. The next stage divides this signal by two and produces the DCT signal or "dibit clock." DCT is a square wave at the dibit rate of 1,000 Hz and is used only for internal timing purposes, although it is present on the interface. The last stage again divides by two producing the E signal, a 500-Hz square wave also used for internal timing. The E signal produces two pairs of pulses (EP and EN, E'P and E'N) that control the flow of information within the data set. The interrelation of the SCT, DCT, and E signals and these control pulses is shown in Fig. 7B.

5.16 These two chains of frequency dividers fix the ratio of F_c to DCT at 1-3/4 to 1 for the 201A. The 201B generates similar timing signals but by different circuit arrangements. For this set, the ratio of F_c to DCT is 1-1/2 to 1.

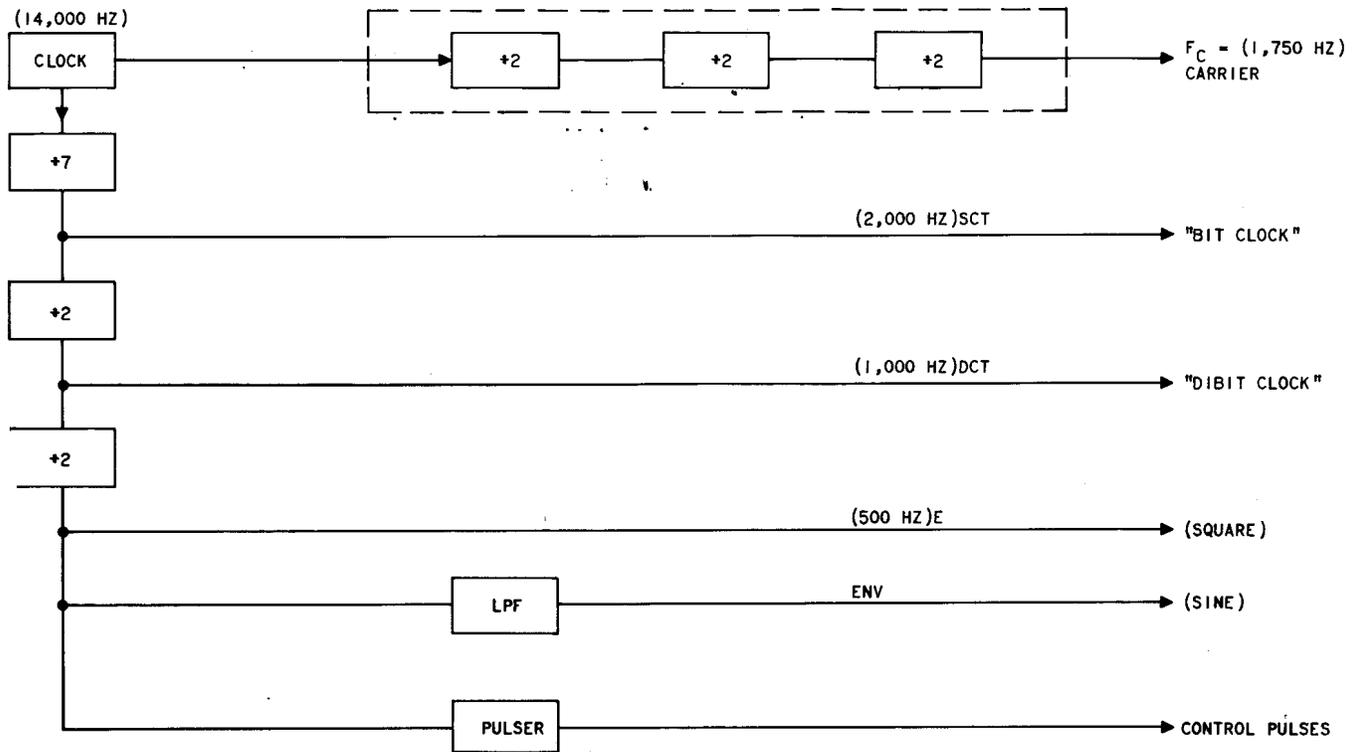
5.17 Another major function of the E signal is controlling the gradual transfer from one channel to the other. The E signal passes through a filter that removes its higher components, leaving only a 500-Hz sine wave known as the ENV signal. The output of the Channel A carrier generator is then amplitude-modulated by this ENV signal as

shown in Fig. 8A. The inverted E signal (called E') is also stripped of its harmonics to produce the ENV' signal, a 500-Hz sine wave opposite in polarity to the ENV signal. The ENV' signal amplitude-modulates the Channel B carrier so that it is at minimum level when Channel A is at its maximum.

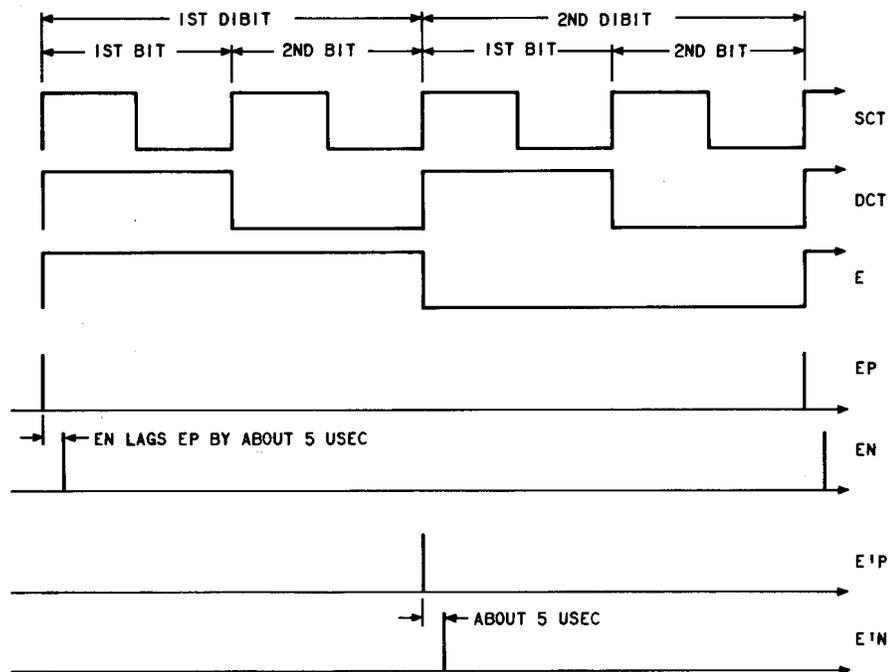
5.18 After the carrier signals (which are square waves) are amplitude-modulated, each is passed through a low-pass filter to eliminate its out-of-band components (harmonics of 1,750 Hz). These two signals are then added together to make up the line signal. As Fig 8B shows, the line signal changes phase gradually as one channel decreases in level and the other increases. Figure 8C shows in another way how the phase changes occur. Proceeding from left to right, we see how at first the line signal L is dominated by Channel A. Then as A decreases in amplitude and B increases, the phase of the line signal swings smoothly around until it becomes that of Channel B.

5.19 As mentioned earlier, the carrier signals are generated by dividing the clock signal by eight in a chain of three binary counters. The first stage of division (see Fig. 9) is known as the "common binary." After this stage, the circuit splits into Channel A and Channel B branches. The second and last stages of division in each channel are known as the "channel binaries." Note that the Channel A binaries are fed from the "1" output of the common binary, while the Channel B binaries are fed from the "0" output. As is evident from the waveform diagrams, this results in a 45° difference between the phase diagrams for the two channels. (In connection with Fig. 6, this was shown to be necessary.)

5.20 The channel binaries in each channel make up a 2-digit binary counter whose input is the signal from the common binary. At any instant, the state of each counter can be expressed as a 2-digit binary number, referring to the state of the Channel A binary as "A" and to that of the Channel B binary as "B." Note, however, that the state of the last counter stage is the "most significant" digit in the number describing the channel binary state. Note also that the "carry" signal to the last counter stage is taken from the "1" output of the first. This makes each counter a "downcounter," following the sequence A (or B) = 11, 10, 01, 00, 11, 10, 01, 00, etc.



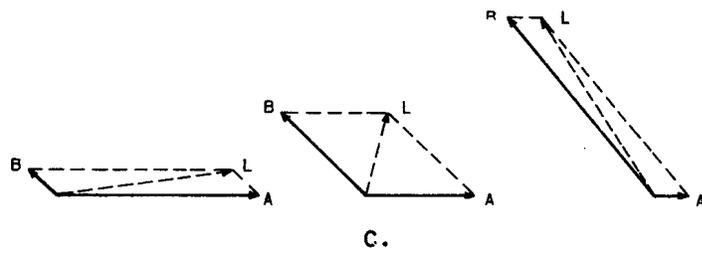
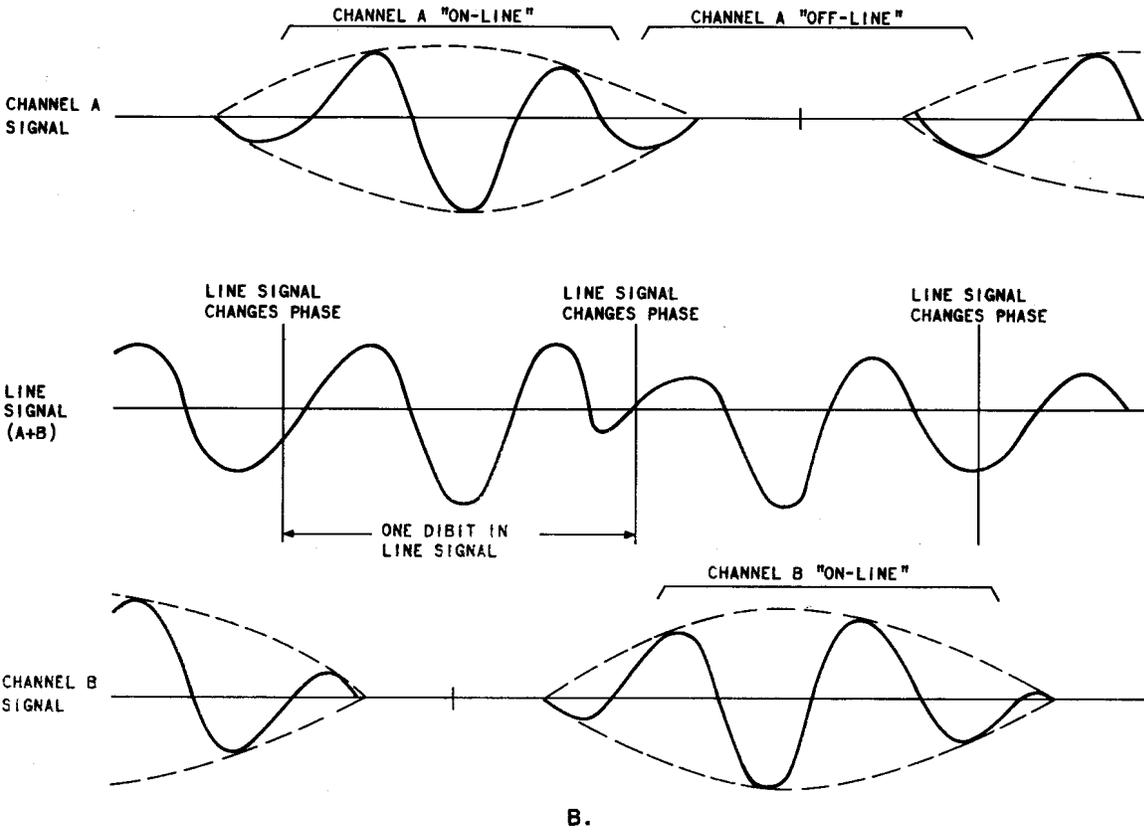
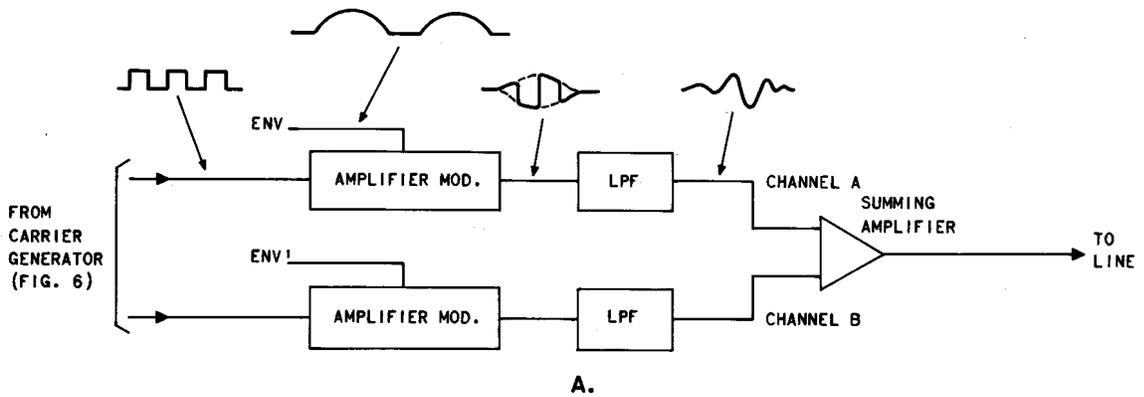
A.



B.

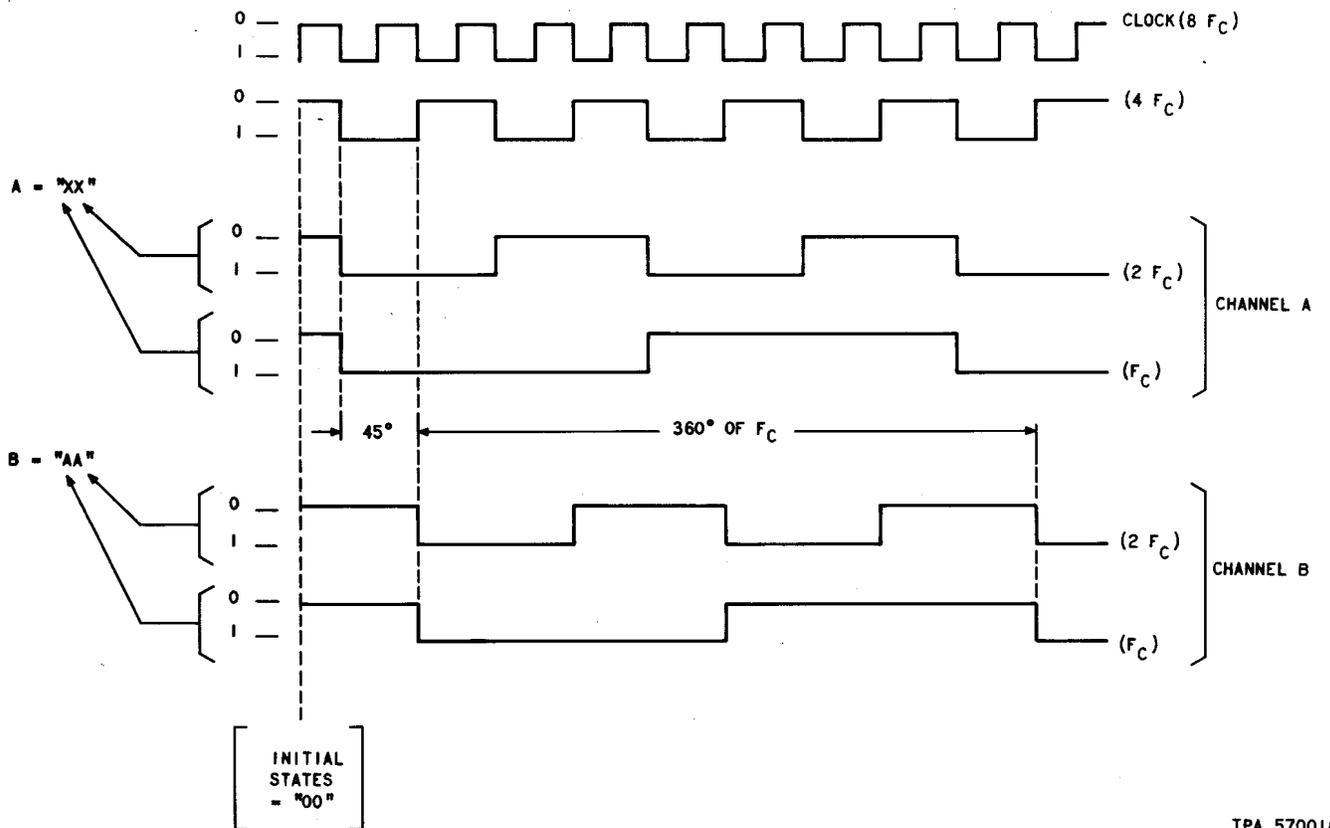
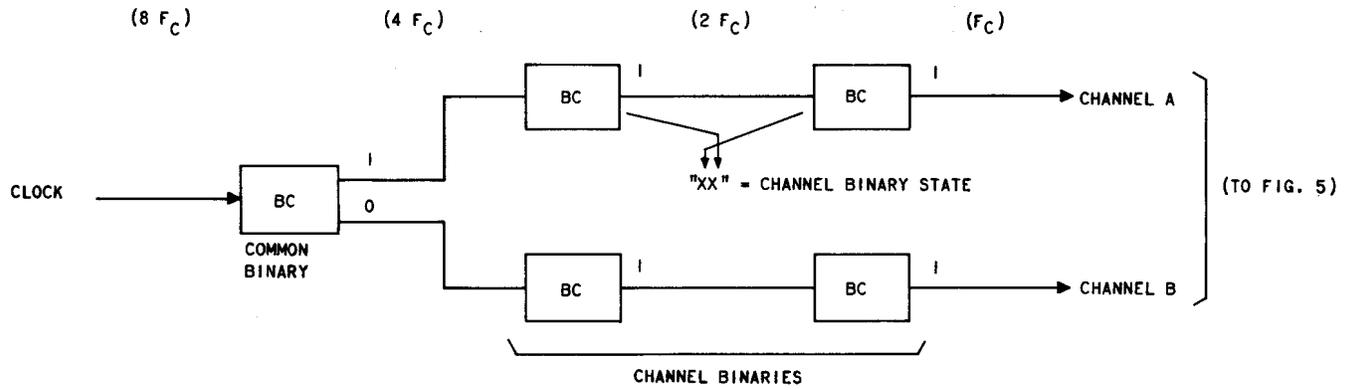
TPA 570014

Fig. 7—Timing Signals



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Fig. 8—Production of Line Signal



TPA 570016

Fig. 9—45° Difference Between Channels A and B

5.21 The waveforms in Fig. 9 assume that the channel binaries of each channel start counting in the "00" state. Figure 10 shows the effect of starting the Channel A binaries in each of the four possible states. It is evident that one out of four carrier phases can be selected by setting the channel binaries into the correct initial starting condition. The dividers are then allowed to run freely (generating carrier) until the next change of phase is to be made. A similar set of waveforms could be drawn for Channel B.

5.22 Figure 11A shows a summary of the carrier phases produced by each channel if the various initial conditions are put into the binaries of that channel. Comparison with Fig. 6 shows that the necessary carrier phases can all be produced. From this, it follows that any epoch angle can be

generated in the line signal by starting the off-line channel binaries in the proper state. Figure 11B illustrates this point.

5.23 Figure 12 shows how the channel binaries are set into the proper starting condition or "initialized." The incoming data is first processed by the "phase logic" circuits which produce pulses on a pair of leads connecting to the "phase register," whose contents at any instant we will call "C" (a 2-digit binary number). This register acts as a subtractor. A pulse on one input lead causes 10 to be subtracted from the contents of the register and the remainder left in the register. A pulse on the other input lead subtracts 01. These pulses may be considered as a (binary) number " ΔC ," which is subtracted from the number "C" in the register.

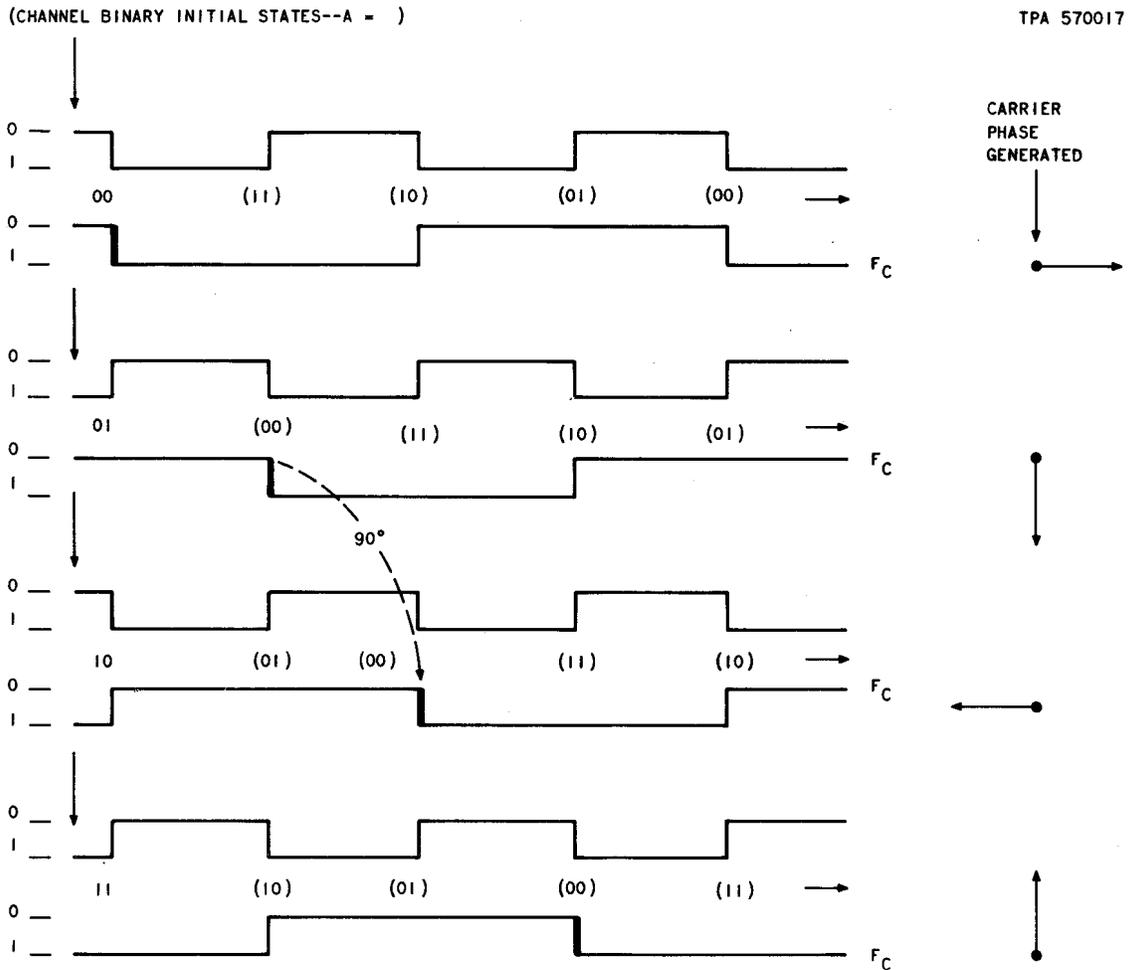


Fig. 10—Carrier Phase vs. Channel Binary Initial Conditions

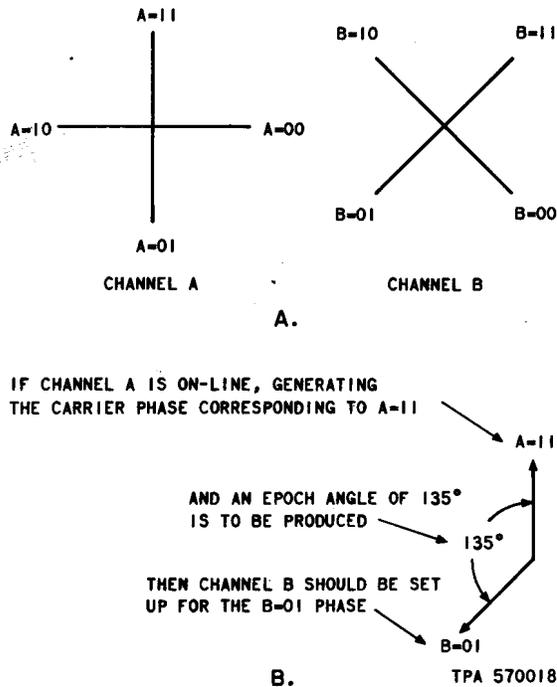


Fig. 11—Carrier Phase vs. Channel Binary Initial Conditions

5.24 Once each millisecond (at the end of each dibit in the incoming data) control pulses open the gates between the register and the off-line pair of channel binaries, and those channel binaries are set into a new initial condition. If Channel B is being initialized, the number contained in the register will be transferred to its channel binaries. That is, after the transfer is complete, the state of the Channel B binaries will be the same as the number contained in the register, or $B = C$. When Channel A is being initialized, the process is similar, but the "most significant" digit is inverted in the transfer ("1" becomes "0," and vice versa) or $A = C + 10$. The register contents are not affected by these transfers.

5.25 In Fig. 13, the carrier phases are marked with the corresponding register contents rather than with the channel binary state. This figure is the same as Fig. 11 except that it reflects the inversion that occurs in Channel A during the transfer.

5.26 We can find from Fig. 13A what pulses must reach the register (ΔC) to produce each epoch angle. For example, if Channel B is

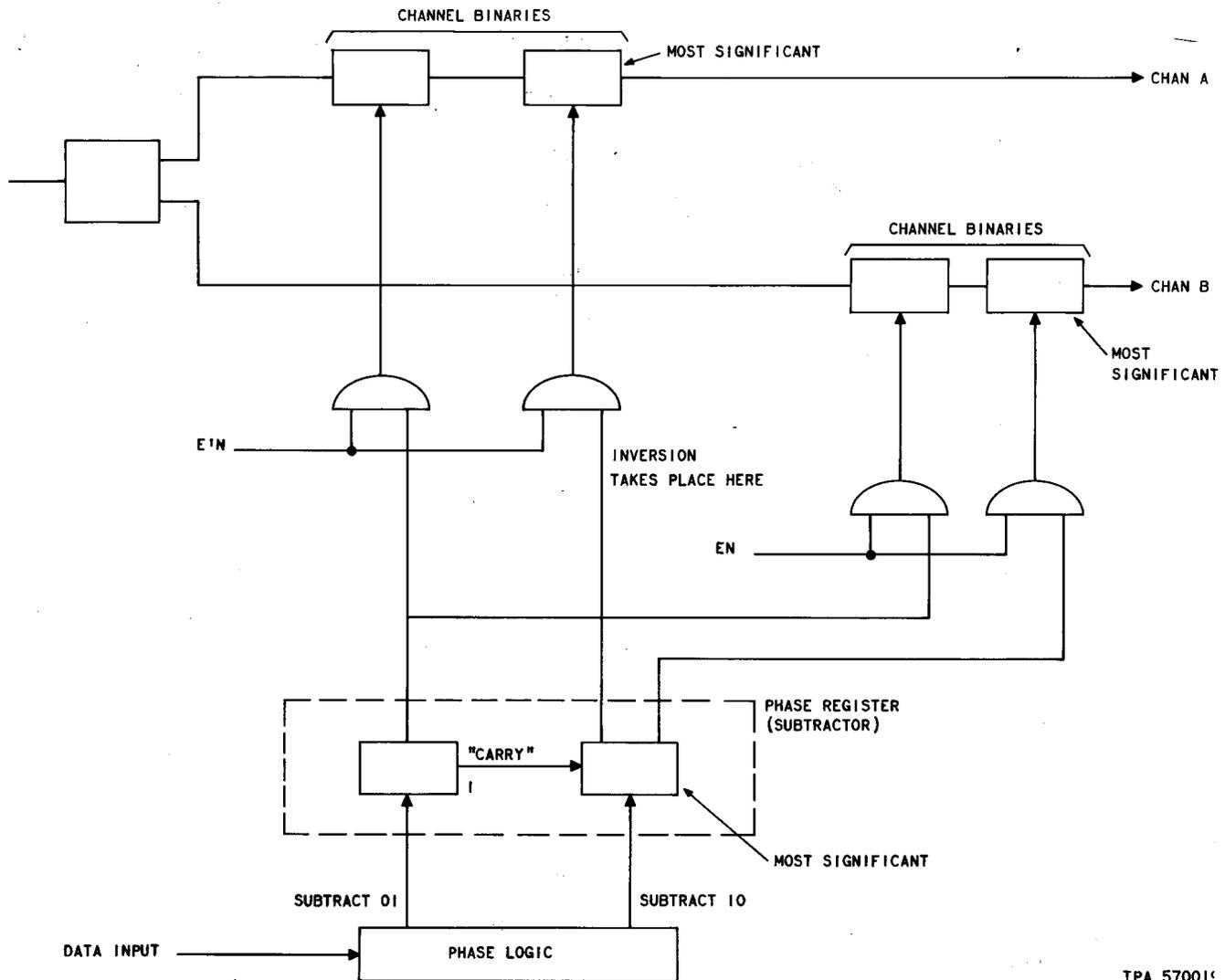
"on-line" with the carrier phase corresponding to "00" in the register at the time it was set up one millisecond ago and if the data requires that an epoch angle of 135° be generated, then we must somehow change the register to "01" before initializing Channel A. This is because inspection of Fig. 13 shows that the phase this will produce corresponds to a change of 135° from the current "on-line" phase. Thus, we must subtract "11" from the "00" left in the register when Channel B was initialized ($00 - 11 = 01$ in binary) requiring a pulse on each input lead, or $\Delta C = 11$. This is illustrated in Fig. 13B.

5.27 Figure 13B illustrates only one way of producing a 135° epoch angle; all told there are eight ways, corresponding to the eight possible reference carrier phases. If we inspect all eight ways, two facts emerge: (1) as long as the reference is a Channel B phase as illustrated, we get a uniform answer of $\Delta C = 11$, but (2) using a Channel A phase as reference produces a different answer, $\Delta C = 00$.

5.28 The results of this process for each epoch angle are tabulated in Fig. 14. As shown, the results depend on which channel is being initialized. However, inspection shows that the difference between channels is a constant one. Each time we go to Channel B, we must subtract an additional "01." This, of course, takes place every other dibit.

5.29 Figure 15 shows how the ΔC pulses are computed. The data logic circuits develop directly from the incoming data what might be called the basic ΔC (ie, the one needed when going to Channel A) in the form of pulses called "D180" and "D90." The data logic is such that a D180 pulse is generated if the first bit in the dibit is a "1" (dibits 10 and 11) and a D90 pulse is generated if the two bits in the dibit are different (dibits 01 and 10). Then an additional pulse on the "01" lead is generated every other dibit (by the "EP" signal) to subtract the extra "01" needed when Channel B is being set up.

5.30 These pulses are not coincident; they are spread over the dibit interval as diagrammed in Fig. 16. As shown, the D180 pulse occurs when the first bit is sampled (if the data is a "1") and the D90 pulse when the second bit is sampled (if it is unlike the first). Then two things happen in quick succession, at the end of the dibit. First,



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Fig. 12—Operation of Phase Register

the EP (or E'P) pulse sets the channel binaries to the "11" state. With the circuit arrangements used, this is a necessary prelude to transferring the information in the register to the channel binaries. This pulse also subtracts "01" from the contents of the register if Channel B is the one being initialized. Then about 5 microseconds later the EN (or E'N) pulse opens the gates between the register and the channel binaries to complete the transfer.

5.31 Let us now follow the transmitter through its operations for a few dibits referring to Fig. 17. The assumed starting conditions are (1) the phase register contains the number $C = 00$, and (2) the Channel B binaries have just been set

to the corresponding phase. This, of course, means that Channel A is "on-line."

5.32 When the first data bit is sampled, it turns out to be a "1," and a D180 pulse is generated. This subtracts 10 from the 00 in the register leaving 10 as shown. Next, the second bit is sampled, and since it is unlike the first bit, a D90 pulse is generated. This subtracts 01 from the 10 in the register leaving $C = 01$.

5.33 At the end of the dibit, the 01 is transferred to the Channel A binaries. Consulting Fig. 13 (reproduced at the right of Fig. 17), we find that the resulting new Channel A phase leads the Channel B phase by the desired epoch angle, 135° .

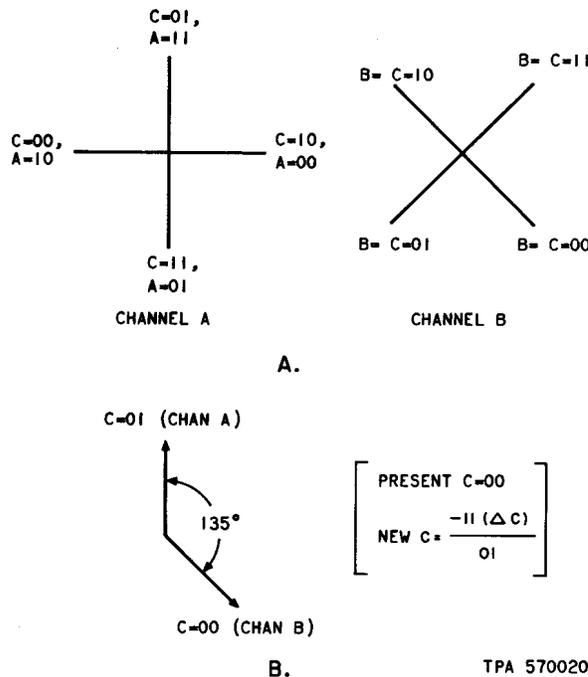


Fig. 13—Carrier Phase vs. Register Contents

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	ΔC SUMMARY			
DIBIT:	11	10	00	01
EPOCH ANGLE:	45°	135°	225°	315°
CHANNEL B ON-LINE, SETTING UP CHAN A	10 ←	11	00	01
CHANNEL A ON-LINE, SETTING UP CHAN B	11 ←	00	01	10
THE DIFFERENCE IS CONSTANT---=01	11 -10 01	00 -11 01	01 -00 01	10 -01 01

Fig. 14—Summary of Required "ΔC" Pulses

Note that at this time Channel B is "on-line"; the 135° epoch angle will not appear in the line signal until the channels switch again at the time labeled "T."

5.34 As dibit #2 appears, it also produces a D180 and a D90 pulse, causing the indicated arithmetic operations in the phase register. At

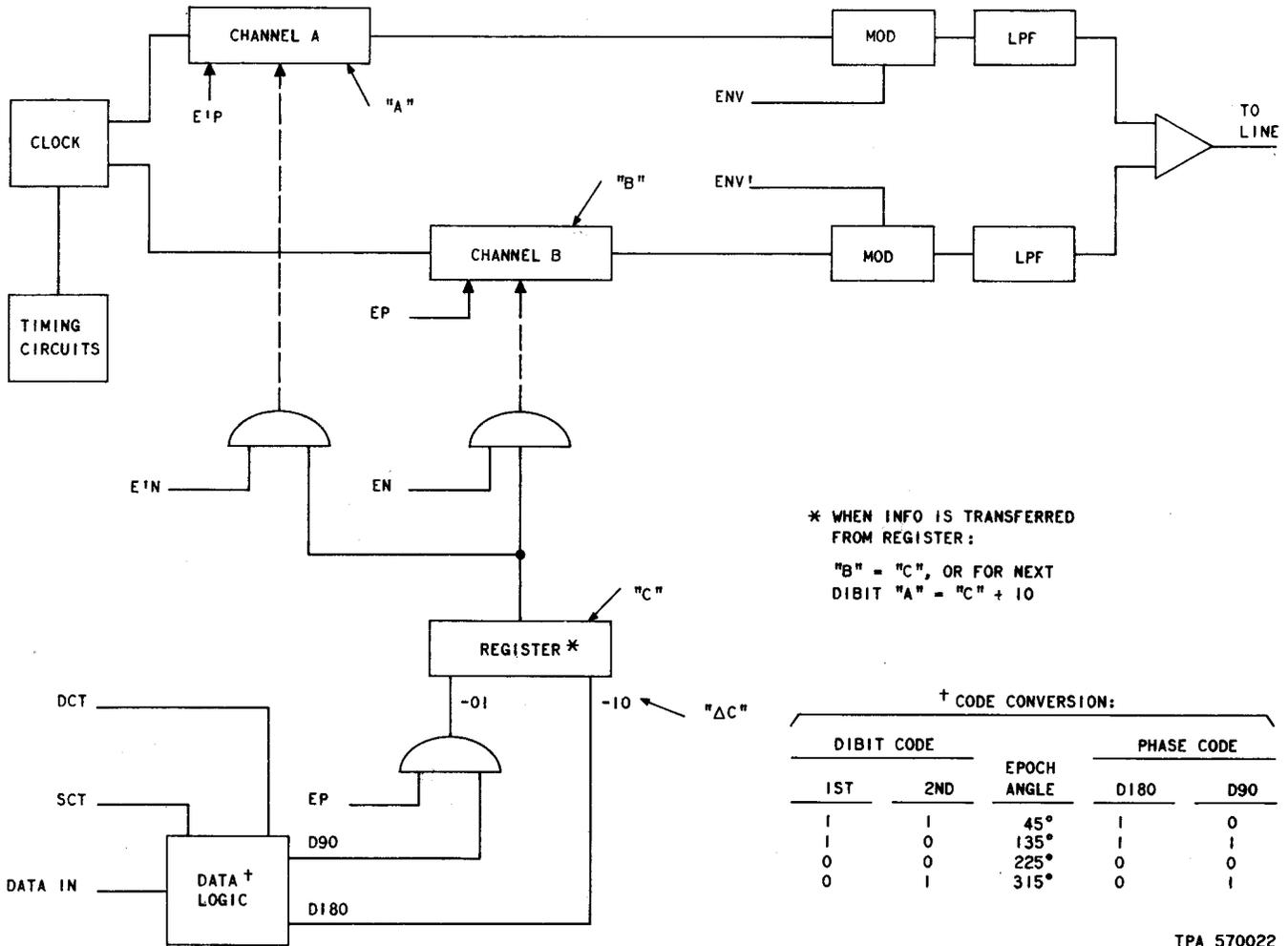
the end of the dibit, however, the EP pulse subtracts an additional 01, leaving C = 01 to be transferred to the Channel B binaries. As shown, this produces another epoch angle of 135°. For dibit #3, the only pulse produced is D180 (since the bits are alike) and the resulting epoch angle is 45°.

5.35 Completion of the chart in Fig. 17 for dibits 4, 5, and 6 is left to the reader. As a check, however, the register contents at the end of dibit #6 are C = 11. Also, the epoch angles produced can be checked against Fig. 5 to see that they correspond to the assumed data.

LINE SIGNAL SPECTRUM

5.36 As discussed earlier, the signal consists of a phase-shifted carrier containing an integral number of quarter cycles of carrier per dibit. The reason for this restriction will be discussed later. For random data, the waveform is nonperiodic in time and cannot be analyzed simply. However, for repeated dibits, the signals become periodic and will produce line spectra. It will be shown that the frequencies of the lines produced will depend upon the dibit code and the number of quarter cycles of carrier per dibit. These factors will determine the tail-to-head or transition angle between successive digits which in turn control the spectrum of the phase-shifted line signal.

5.37 As an example, consider the repeated dibit 11. For the 201A, each dibit interval contains 1-3/4 cycles of the 1750-Hz carrier. The transmitter circuits add +45° to the initial phase angle of the 1750-Hz carrier for each succeeding dibit on the line, producing an epoch angle of +45°. If it is assumed that this is done abruptly (rather than gradually, as is actually the case), the resulting line signal would appear as in Fig. 18. This signal has a period of 8 ms or a fundamental frequency of 125 Hz, a frequency too low to appear as a significant component in the spectrum. The transition angle for this example is either +135° or -225°. This corresponds to the angle between the tail of the previous dibit and the head of the present dibit and is illustrated in Fig. 19. Averaged over a long period of time, this is equivalent to adding 3/8 cycle (or subtracting 5/8 cycle) of a 1750-Hz waveform to the carrier frequency each



TPA 570022

Fig. 15—Block Diagram of Transmitter

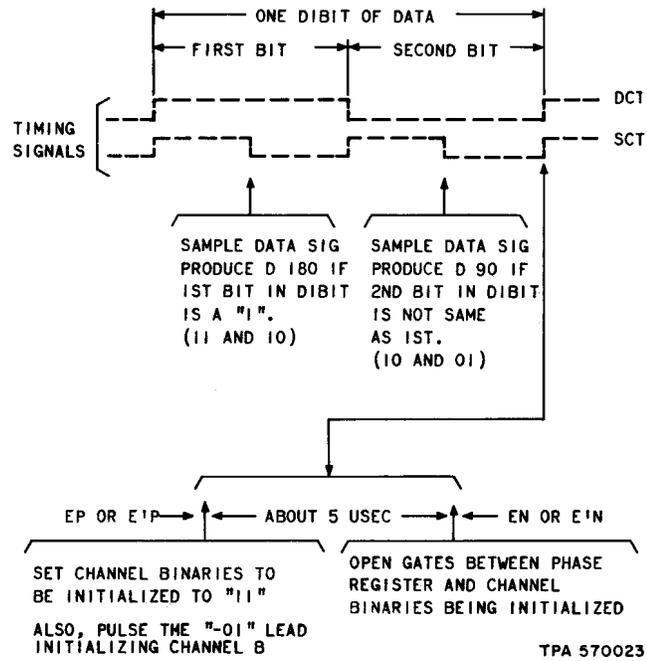


Fig. 16—Timing Chart

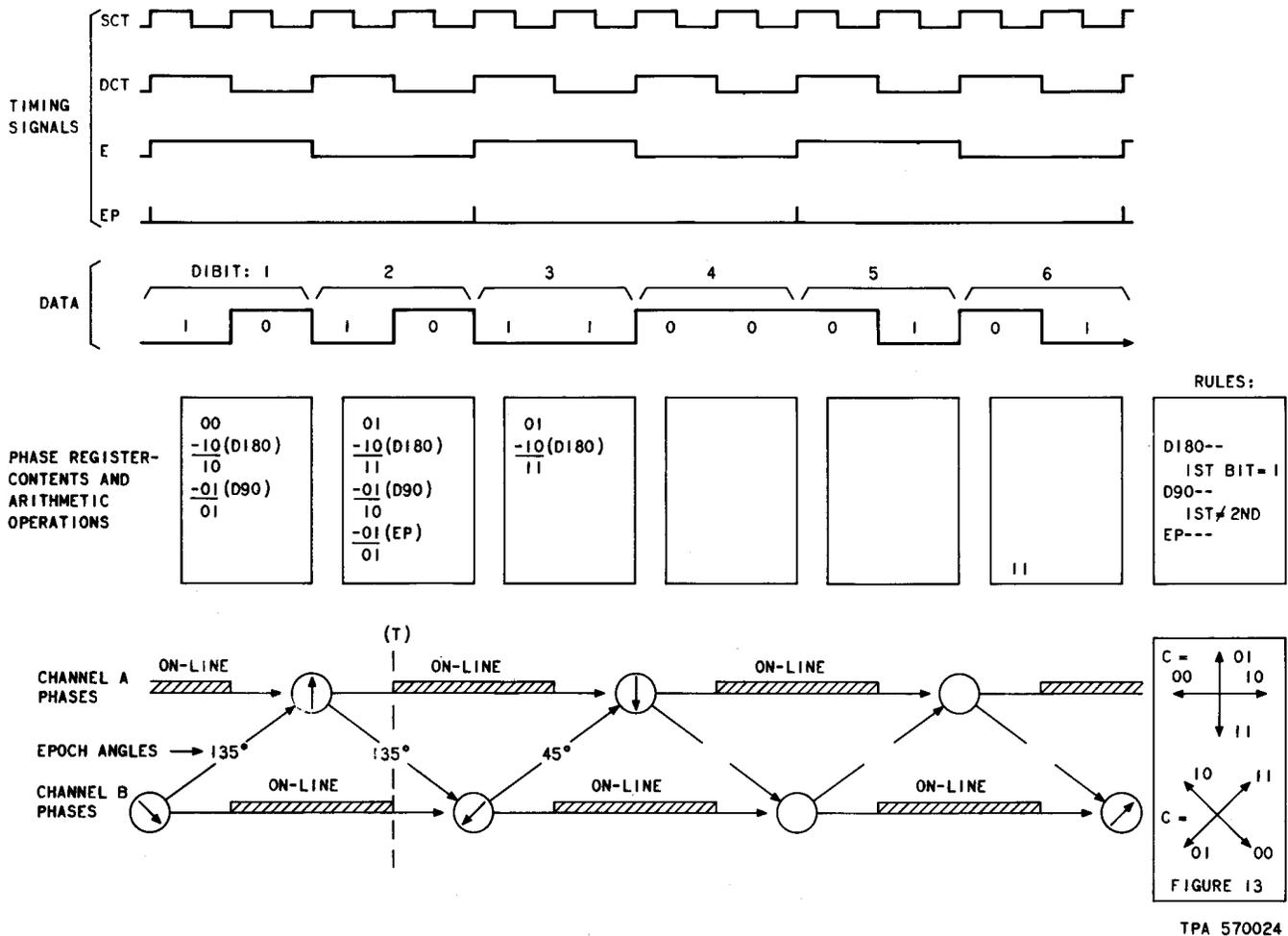


Fig. 17—Sequence Chart, Data Set 201A

millisecond. Expressed another way, the average frequency is shifted upward by an amount:

$$\text{upward shift} = \frac{3/8 \text{ cycle}}{1/1000 \text{ second}} = \frac{3000}{8} = 375 \text{ Hz}$$

The shifted carrier becomes:

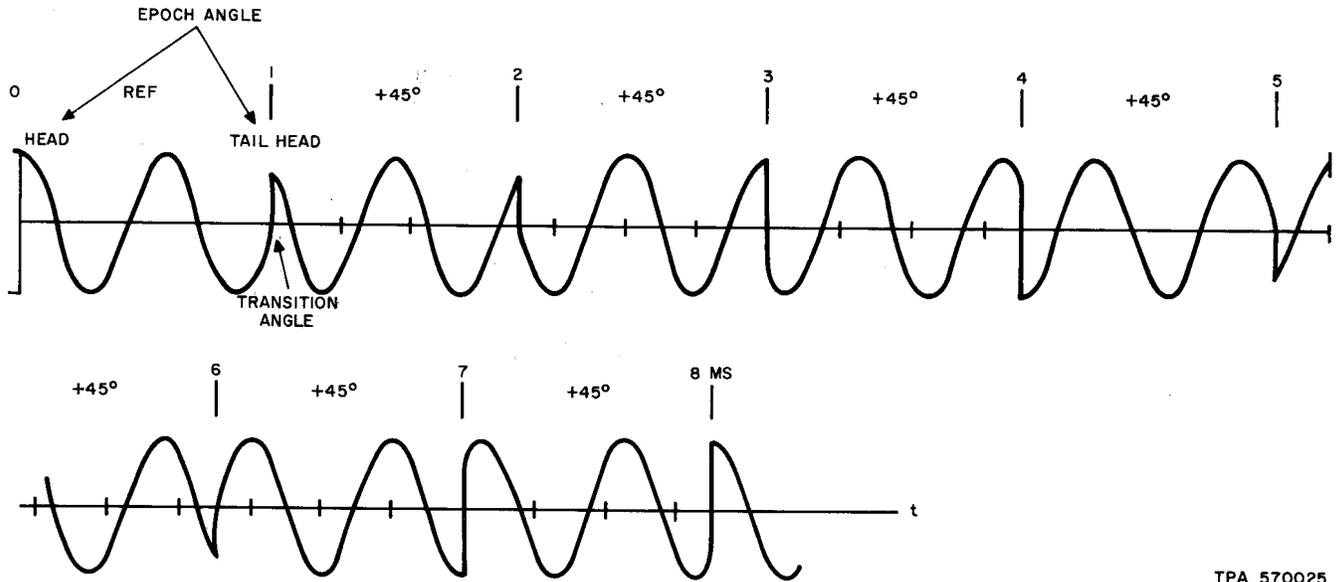
$$1750 + 375 = 2125 \text{ Hz}$$

5.38 Since this happens at the dibit frequency of 1000 Hz, there will be significant sideband

components of $2125 - 1000 = 1125 \text{ Hz}$ and $2125 + 1000 = 3125 \text{ Hz}$. The 3125-Hz component is very weak and is usually ignored. Averaged over a long period of time, the 1750-Hz carrier is suppressed as a result of this phase-shift modulation. Therefore, the significant frequency components in the repeated 11 dibit are 1125 Hz and 2125 Hz. The same result can be obtained by counting the number of zero crossings for the phase-shifted signal in Fig. 18. There are 34 zero crossings in 8 ms for an average frequency of:

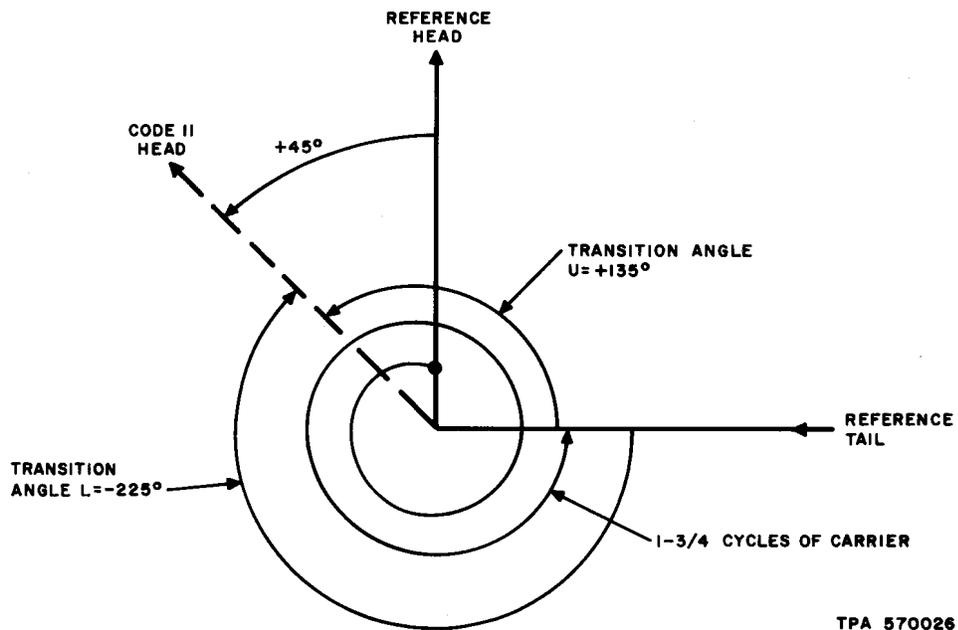
$$\frac{34 \text{ zero crossings}}{.008 \text{ sec.}} \times \frac{1 \text{ cycle}}{2 \text{ zero crossings}} = 2125 \text{ Hz}$$

201A DATA SET REPEATED 11 DIBITS



TPA 570025

Fig. 18—Simplified Line Signal for Repeated Dibits



TPA 570026

Fig. 19—Determining Transition Angle

5.39 In 4-phase modulation, where the coding is restricted to odd multiples of 45° for the epoch angle, the choice of an integral number of 1/4 cycle of carrier per dibit will assure a transition angle which is also some odd multiple of 1/8 cycle (45°) of the carrier waveform. This means that for repeated dibits, the carrier frequency shift will be restricted to odd multiples of a unit amount designated Δf corresponding to 1/8 cycle of the carrier per dibit interval. The unit amount becomes:

$$f = \frac{1/8 \text{ cycle}}{1/\text{dibit freq. sec.}} = \frac{\text{dibit freq.}}{8} \text{ Hz}$$

5.40 Figure 20 shows how the line spectra for repeated dibits of all four codes are developed for a choice of 1-3/4 cycles of carrier per dibit (for the 201A). Figure 21 is a summary of the line spectra for repeated dibits for Data Sets 201A and 201B. The 201B uses 1-1/2 cycles per dibit and, as a result, the line spectra differ for the two sets even though they use the same epoch angle coding. The result of the coding and carrier frequency restrictions noted above is a line signal spectrum which contains pairs of frequencies separated by exactly the dibit frequency regardless of the data input. This fact will be used in the receiver sync recovery circuits which are discussed later.

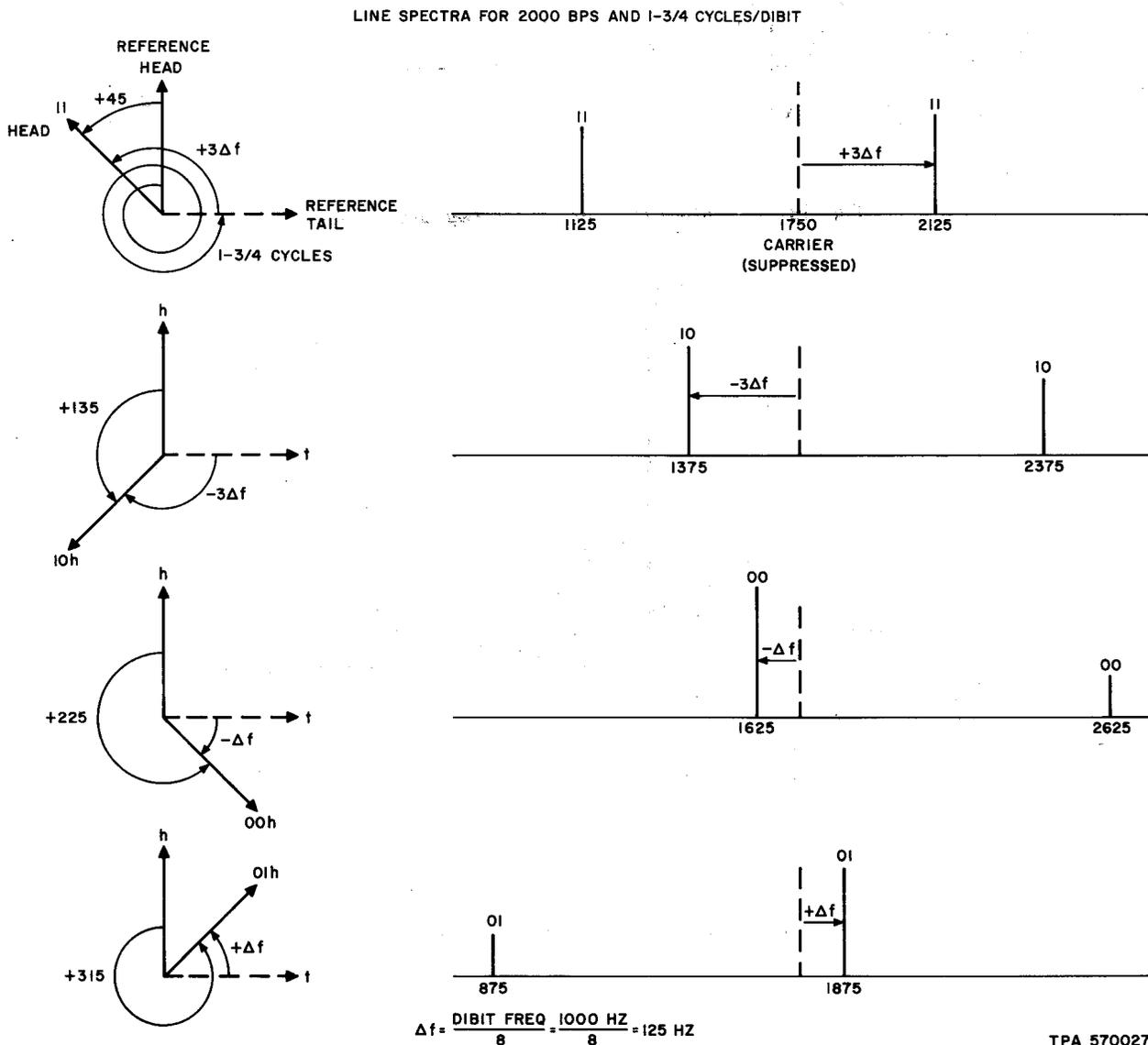


Fig. 20—Line Spectra for Repeated Dibits

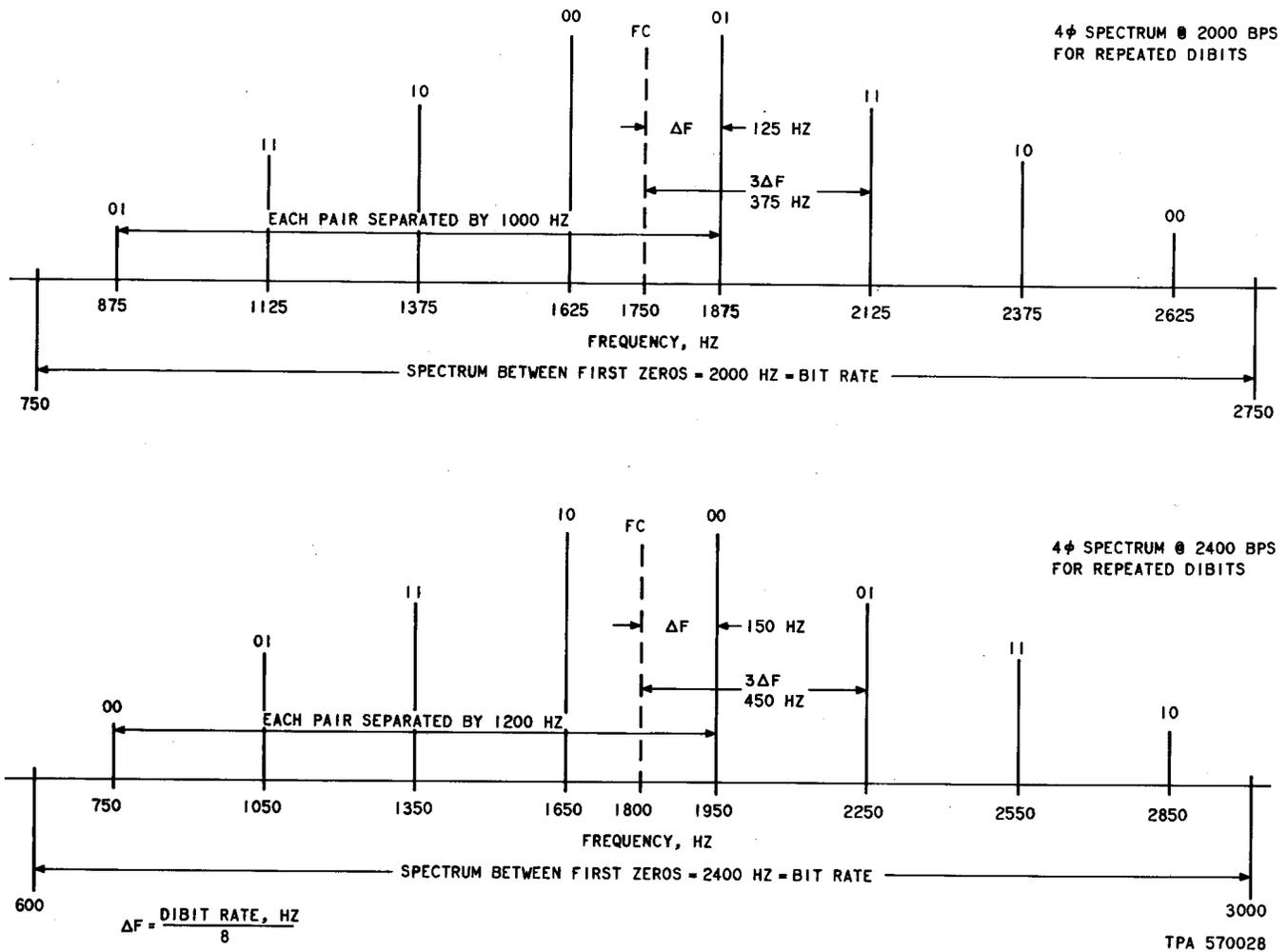


Fig. 21—Summary of Line Spectra for Repeated Dibits

5.41 The shape of the spectrum for random data can be determined by analyzing 4-phase modulation as two double sideband AM suppressed carrier channels operating in quadrature. A single DSAMSC (DSB) system corresponds to 200 percent AM and for binary digital data becomes a phase-reversal system. Two phase-reversal systems in quadrature become a fixed reference 4-phase system. For example, refer to Fig. 5 and note that the dibit pair 11 and 00 form one phase-reversal channel and the pair 10 and 01 form the second channel in phase quadrature to the first. Each channel becomes a suppressed carrier AM system operating at the dibit frequency and will exhibit a continuous frequency spectrum corresponding to the impulse response of the transmitter shaping circuits. With true raised cosine-shaping, the spectrum would have zeros corresponding to the

carrier frequency plus or minus a frequency F corresponding to $1/T$ where T is the dibit interval. For the 201A:

$$T = 1\text{ms (dibit interval)}$$

$$\text{and } f = \frac{1}{1\text{ms}} = 1000 \text{ Hz}$$

5.42 Then the spectrum to the first zeros will be $1750 - 1000 = 750 \text{ Hz}$ to $1750 + 1000 = 2750 \text{ Hz}$. The envelope modulators in Data Sets 201A use a modified raised cosine-shaping with a more abrupt cutoff as illustrated in Fig. 8. As a result, the actual spectrum for the 201A contains zeros at 2850 Hz and 650 Hz.

RECEIVER

5.43 The receiver has two main circuit functions:

(1) data recovery and (2) sync recovery.

An overall block diagram of the 201A receiver is shown in Fig. 22; the 201B is similar. After compromise equalization (optional), amplification, and AVC, the line signal is simultaneously presented to the data and sync recovery circuits. The operation of each will be discussed separately.

A. Data Recovery

5.44 As discussed earlier, data recovery depends upon the epoch phase angle between the present and the previous dibit. The present dibit is applied simultaneously to one input of each of two product modulators (or demodulators in this usage). The other input to one of the modulators is the previous dibit or 0° reference obtained through a 1 ms broadband delay line. The second input to the other product demodulator is the delay line output shifted -90° in phase. The product modulator with the -90° phase-shifted reference input recovers the first (A) bit of the dibit. The product modulator with the 0° reference input recovers the second (B) bit of the dibit. Data recovery of both bits is done simultaneously (in parallel) and the second bit is delayed in a shift register (B DATA REGISTER) by one bit interval before being transferred to the A DATA REGISTER which produces the output serial data. It is important to note that A and B as used here have nothing to do with Channels A and B in the transmitter.

5.45 Figure 23 shows the 201A data recovery circuits in more detail. The line signal is amplified and stabilized in amplitude before being applied to the recovery circuits as the line signal input LSI. This signal is then delayed one dibit interval by delay line R4 and R5. The 201A and 201B delay lines are shown schematically in Fig. 24. There are two outputs labeled 0° and -90°; these provide the reference or previous dibit signals for the two data recovery modulators on cards R6 and R8.

5.46 The demodulation process is shown in more detail in Fig. 25. Consider the case where the input dibit v can be represented by the function:

$v = \cos wt$. Here w is the carrier frequency in radians per second and t is time. In Fig. 25, the delay line 0° output (v_0) is the line signal from the previous dibit [$v_0 = \cos (wt + \theta)$] where t is the phase shift between the two dibits (this phase shift contains the information). The delay line 90° output v_{90} is the same signal as the 0° output except it is shifted an additional 90°; therefore:

$$v_{90} = \cos (wt + \theta + \pi/2)$$

$$\pi/2 \text{ radians} = 90^\circ.$$

As indicated in Fig. 25, the A product modulator multiplies v_{90} and v to produce A out. The B product modulator multiplies v_0 and v to produce B out.

$$A \text{ out} = v \cdot v_{90} = \cos (wt) \cos (wt + \theta + \pi/2)$$

$$B \text{ out} = v \cdot v_0 = \cos (wt) \cos (wt + \theta).$$

These expressions can be rewritten by using the trigonometric identity:

$$\cos(x) \cos(y) = 1/2 \cos (x+y) + 1/2 \cos (x-y).$$

The outputs of the product modulators are rewritten as follows:

$$A \text{ out} = 1/2 \cos (2 wt + \theta + \pi/2) + 1/2 \cos (\theta + \pi/2)$$

$$B \text{ out} = 1/2 \cos (2 wt + \theta) + 1/2 \cos (\theta).$$

5.47 The signals A out and B out are fed to low-pass filters which remove the double frequency components:

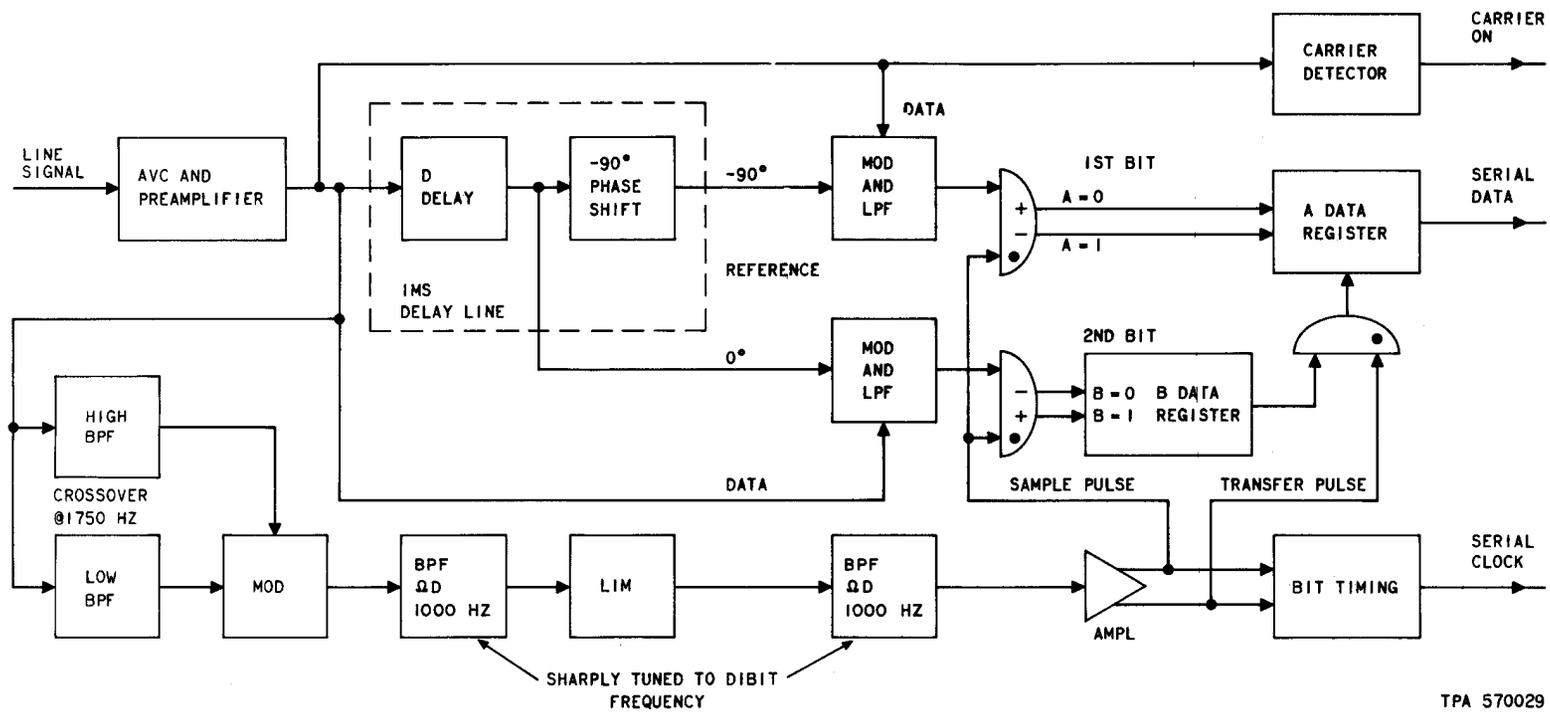
$$1/2 \cos (2 wt + \theta + \pi/2)$$

$$1/2 \cos (2 wt + \theta)$$

Our signal becomes the following:

$$1/2 \cos (\theta + \pi/2) \text{ and}$$

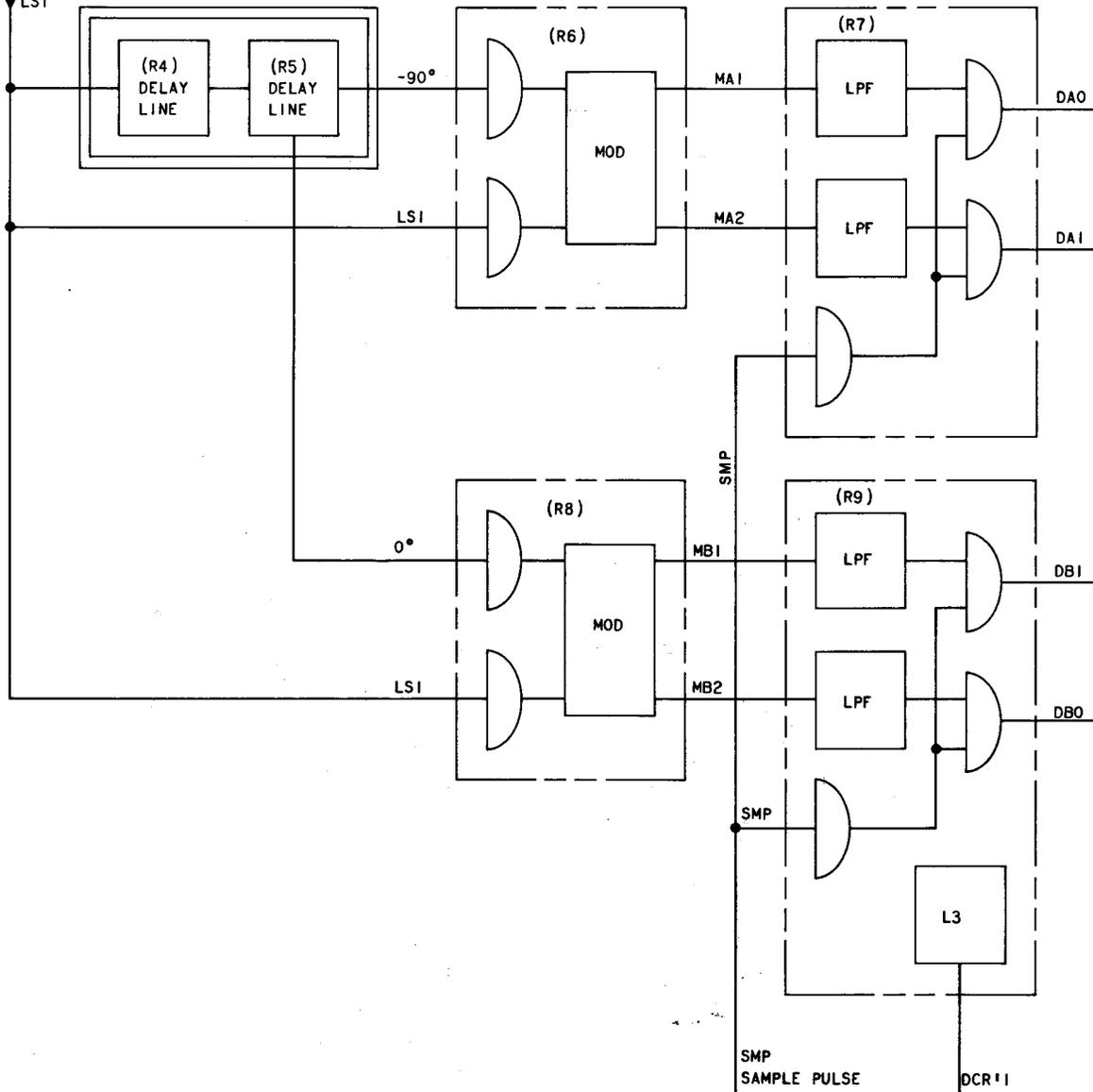
$$1/2 \cos (\theta).$$



TPA 570029

Fig. 22—201A Receiver Block Diagram

LSI = LINE SIGNAL INPUT
FROM AVC CIRCUITS



TPA 570030

Fig. 23—201A Data Recovery Circuits

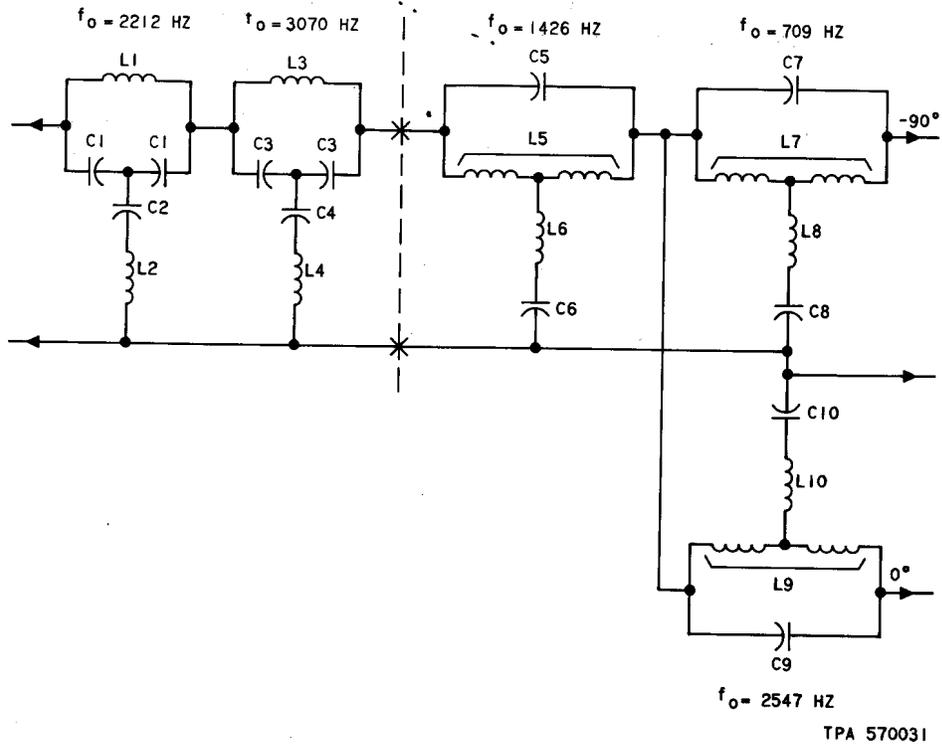


Fig. 24—Sketch of R4 and R5 Circuit, 844A and 844B Delay Lines

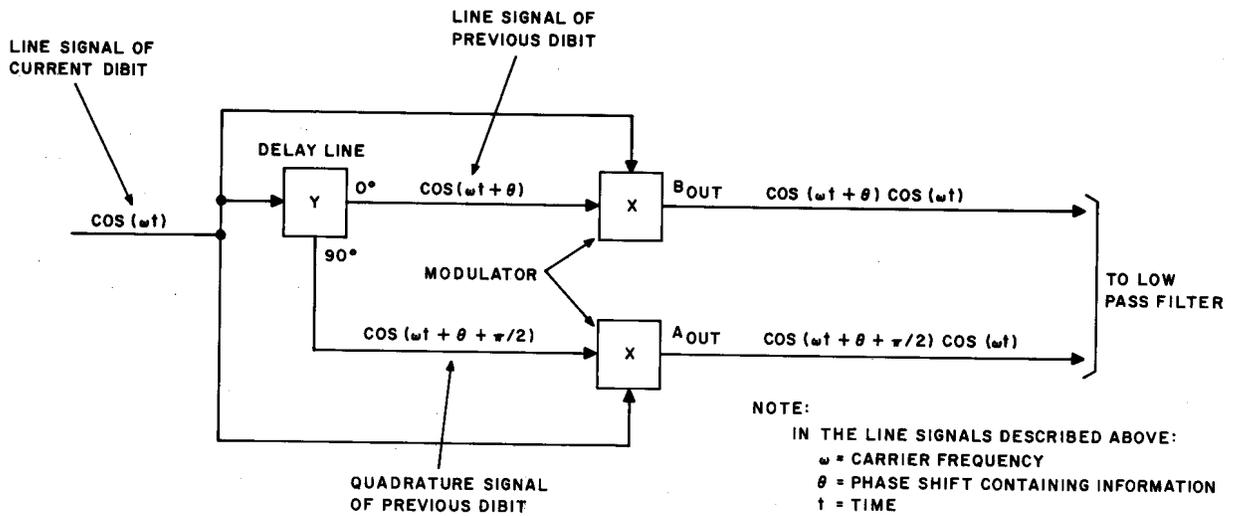


Fig. 25—Method of Operation for Balanced Product Modulator

These terms involve only the phase shift between dibits θ and are used to determine the two bits

of the dibit by taking their algebraic sign as shown in the table below:

DIBIT	θ	ALGEBRAIC SIGN OF $\frac{1}{2} \cos (\theta + \pi/2)$	ALGEBRAIC SIGN OF $\frac{1}{2} \cos (\theta)$
11	0 to 90	-	+
10	90 to 180	-	-
01	180 to 270	+	-
00	270 to 360	+	+

5.48 As an example, consider the recovery of the dibit 11 in the 201A 4-phase receiver. At the transmitter, the carrier phase was advanced $+45^\circ$ relative to its phase 1 ms earlier. We can write an expression to represent the previous dibit as

$$\text{previous dibit} = \cos [wt + \theta]$$

where θ is an arbitrary phase angle. Then the expression representing dibit 11 becomes

$$\text{dibit 11} = \cos [(wt + \theta) + 45^\circ].$$

5.49 Both signals are presented simultaneously to the input of the 0° product modulator. The DC term in the output becomes

$$\text{DC term} = 1/2 \cos 45^\circ.$$

The output polarity then is positive.

5.50 The previous dibit signal at the input to the -90° product modulator is

$$\text{previous dibit (shifted } -90^\circ) = \cos [(wt + \theta) - 90^\circ].$$

Then the DC term in the output becomes

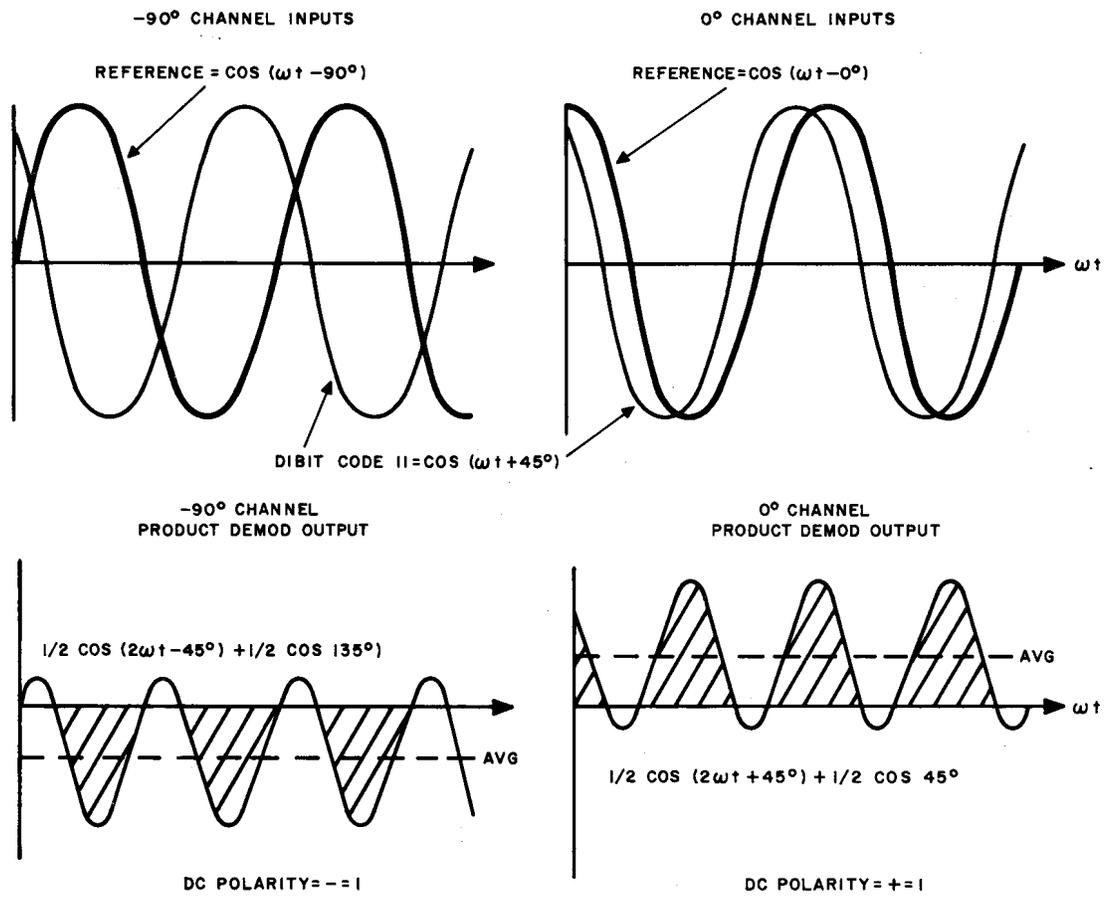
$$\text{DC term} = 1/2 \cos [45^\circ - (-90^\circ)] = 1/2 \cos 135^\circ.$$

5.51 The output polarity of the -90° channel is negative. This is illustrated with waveforms in Fig. 26. Again, abrupt phase transitions are assumed for simplicity. The DC output of the -90° modulator will be negative for epoch phase

angles between 0° and $+180^\circ$. The DC output of the 0° modulator will be positive for epoch angles between $\pm 90^\circ$. Figure 27 contains a summary of these results. Note that data recovery is independent of the number of carrier cycles per dibit.

5.52 Figure 28 shows the circuit details of the data sample amplifiers. There is one data sample amplifier for each of the two demodulators. The output signal from the demodulators is coupled (balanced to ground) to the input of the data sample amplifiers through low-pass filters. These filters effectively eliminate the double-frequency product output of the demodulators. The resultant voltage on the base of transistors Q2 and Q3 represents the DC term of Fig. 27 according to the dibit being detected. The voltage difference between the bases of Q2 and Q3 represents the recovered data signal before regeneration and serves as a point to observe the received "eye pattern." At the proper instant in the received dibit (approximately the middle of the eye pattern), this voltage difference is a maximum and a gate pulse on the SMP lead causes either Q2 or Q3 to conduct.

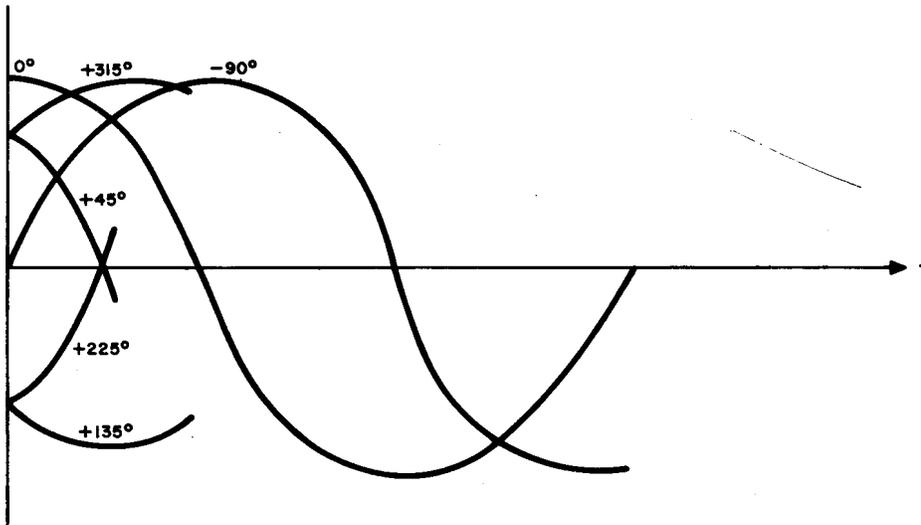
5.53 This results in a code pulse on either pin 14 or 5 in 2-rail logic representing the properly associated code for bit A (-90° Demod) and bit B (0° Demod). The A bit pulse sets the state of the A register whose output appears as the Received Data or RD on the interface. The code pulse for the B bit is delayed a one-half dibit interval in the B register before a readout pulse transfers it to the A register as the second bit of the bit pair. The output data is then in serial form for use by the customer. At this point the RD signal has been retimed and shaped so that it is essentially distortion-free.



RECOVERED DATA = 11

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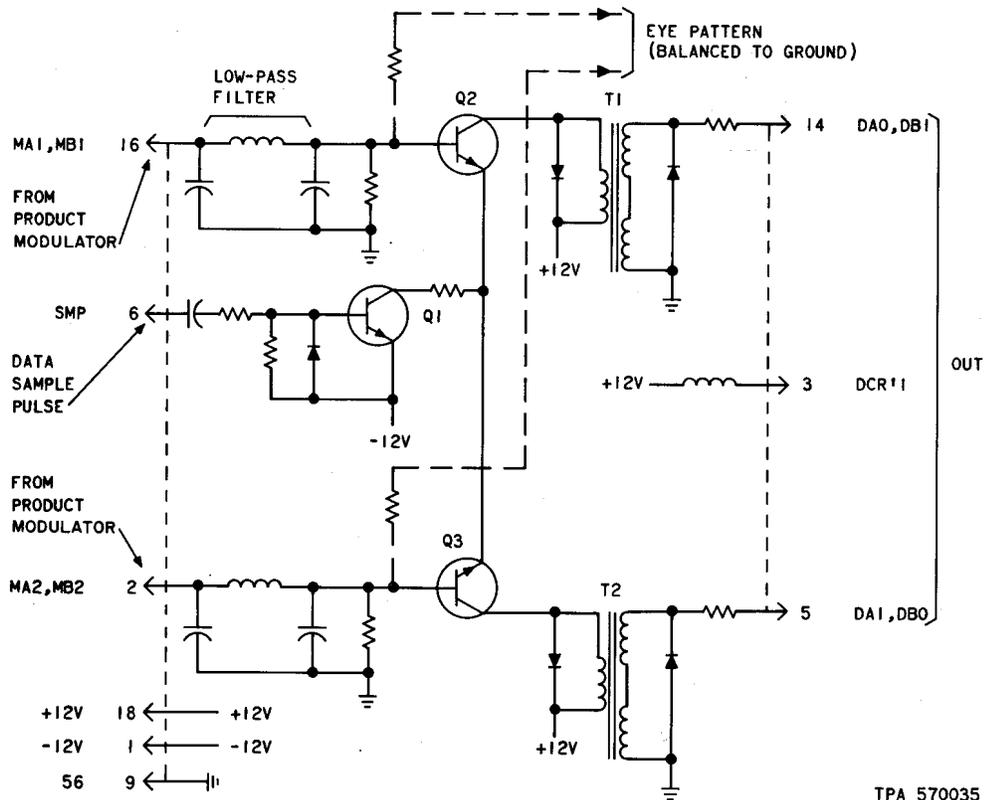
Fig. 26—Data Recovery in a Four-Phase Data Set Using Product Demodulators



EPOCH ANGLE	-90°		0°	
	POLARITY	CODE	POLARITY	CODE
+45	-	1	+	1
+135	-	1	-	0
+225	+	0	-	0
+315	+	0	+	1

TPA 570034

Fig. 27—Relationship Between Epoch Angles and DC Polarity for Product Modulators



TPA 570035

Fig. 28—Data Sample Circuit Details

B. Sync Recovery

5.54 Operation of the receiver logic and data sample circuits depends on an accurate clock signal. This clock signal can be extracted from the sidebands associated with each dibit code in the modulation spectrum. In the special case of repeated dibits as shown in Fig. 20 and 21, each dibit code generates a line spectrum pair with a constant separation corresponding to the dibit frequency. A detailed analysis can be used to show that these spectra pairs at the transmitter are also invariant in phase. Thus, by proper recovery technique, sync can be made available for all code combinations.

5.55 Figure 29 shows how this is accomplished.

The frequencies shown are for Data Set 201A and repeated dibits. The amplified and stabilized line signal is applied simultaneously to a pair of high- and low-pass splitting filters which cut off at the nominal carrier frequency. Since

each dibit code contains a prominent frequency above and below the carrier frequency, these are now separated and applied simultaneously to the two inputs of a balanced product demodulator. The difference frequency output of the product demodulator is the separation frequency. As shown in Fig. 29, this is the dibit frequency. This frequency is selected from the other modulation products by sharply tuned band-pass filters. The recovered dibit frequency is shaped to provide clock and timing signals for the receiver circuits, and it also is made available after conversion to bit frequency as SCR or Serial Clock Receive.

5.56 The stability of the sync recovery circuit is affected by delay distortion and, to some extent, by amplitude distortion at the edges of the signal spectrum. Repeated dibit codes which produce a weak or delayed outer sideband, eg, dibit 00 or 01 for the 201A, produce excessive jitter in the recovered sync signal and can cause data errors. For this reason, 4-phase data sets are designed to

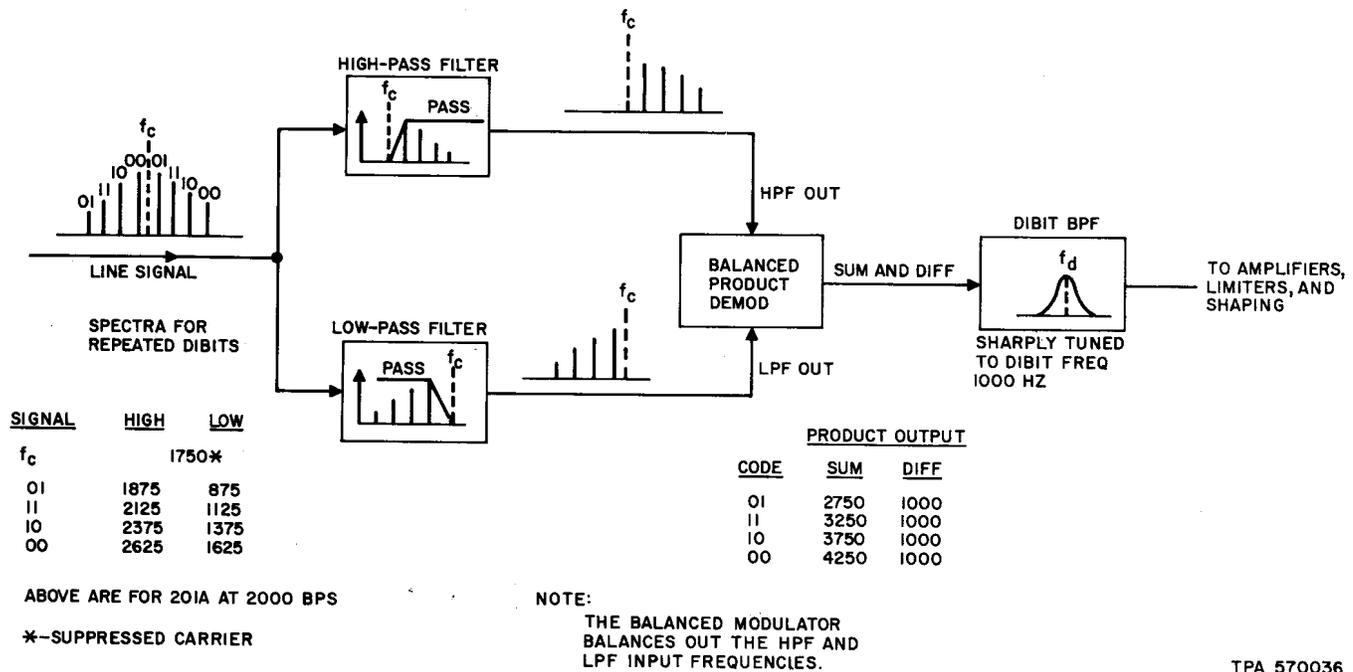


Fig. 29—Principle of Dibit Sync Recovery

“idle” with a code combination which produces a favorable line spectrum. This code is repeated dibit 11 for Data Sets 201A and 201B.

6. TESTING AND ALIGNMENT

6.01 The following tests supplement the test procedures contained in Sections 592-011-500, 592-011-501, and 592-011-502. If the data set passes the requirements of Sections 592-011-500, 592-011-501, or 592-011-502 and fails to operate with the business machine, the oscillator test should be performed. Data Sets 201-type contain circuit boards which are matched groups. If any board of the BT group must be replaced, the entire group must be tested and aligned. Refer to Section 592-011-151 for test and alignment of the BT-group codes.

Oscillator Test of Internally Timed Data Sets

6.02 The internally timed data sets contain a crystal oscillator from which all timing and clock signals are derived. This oscillator generates a 14.0 kHz signal for Data Set 201A-type or 14.4 kHz for Data Set 201B-type. This frequency is divided internally to produce the serial clock transmit (SCT) signal at 2000 Hz for Data Set 201A or 2400

Hz for 201B. The purpose of this test is to measure the SCT frequency and, if this frequency does not meet specifications, to replace the oscillator or frequency divider circuits.

6.03 The equipment required to perform this test is as follows:

- 1—Hewlett Packard counter, type 5321B or equivalent.

Note: Any equivalent counter must be capable of counting to five digits.

- 1—914B Data Test Set (DTS).

6.04 The test is performed as follows:

- (a) Disconnect power to the data set.
- (b) Connect the customer interface jack (J2) to the A connector on the 914B DTS. On the 914B DTS, all A interface selector switches must be pushed in.
- (c) Connect the counter to terminal 15 (SCT) at the interface selector switch panel on the 914B DTS.

(d) Measure the frequency on the SCT signal.

592-011-202

Date Sets 201A- and 201B-List Type, Transmitter-Receiver, Installation and Connections

Requirement: 2000 (± 1.0) Hz for 201A; 2400 (± 1.0) Hz for 201B

592-011-300

Data Sets 201A1, A2 and 201B1, B 2, Transmitter-Receiver, Maintenance

(e) If the frequency is not within limits, replace the T1 card and retest. If the frequency is still not within limits, replace the T2 and T3 cards and retest. If the SCT frequency cannot be brought within the required limits, return the data set to the distributing house.

592-011-301

Data Sets 201A3, A4 and 201B3, B 4, Transmitter-Receiver, Maintenance

7. REFERENCES

592-011-302

Data Sets 201A and 201B List Type, Transmitter-Receiver, Maintenance

7.01 For further information concerning Data Sets 201A and 201B, refer to the following Bell System Practices:

592-011-500

Data Sets 201A1, A2 and 201B1, B2, Transmitter-Receiver, Test Procedures

SECTION

TITLE

590-002-100

Data Set 201-Type, Reference Guide

592-011-501

Data Sets 201A3, A4 and 201B3, B4, Transmitter-Receiver, Test Procedures

592-011-100

Data Sets 201A1, A2 and 201B1, B 2, Transmitter-Receiver, Description and Operation

592-011-502

Data Sets 201A and 201B List Type, Transmitter-Receiver, Test Procedures

592-011-101

Data Sets 201A3, A4 and 201B3, B 4, Transmitter-Receiver, Description and Operation

598-080-100

Data Auxiliary Set 828A, Data Service Unit, Description and Operation

592-011-102

Data Sets 201A- and 201B-List Type, Transmitter-Receiver, Description and Operation

598-080-101

Data Auxiliary Set 828C, Description and Operation

592-011-151

Data Sets 201A3, A4 and 201B3, B 4, Transmitter-Receiver, Supplementary Information

598-080-200

Data Auxiliary Set 828A, Data Service Unit, Installation and Connections

592-011-200

Data Sets 201A1, A2 and 201B1, B 2, Transmitter-Receiver, Installation and Connections

598-080-201

Data Auxiliary Set 828C, Installation and Connections

592-011-201

Data Sets 201A3, A4 and 201B3, B 4, Transmitter-Receiver, Installation and Connections

598-080-300

Data Auxiliary Set 828A, Data Service Unit, Maintenance and Test Procedures

598-080-301

Data Auxiliary Set 828C, Maintenance and Test Procedures.