

37 KEYBOARD SEND-RECEIVE (KSR) TELETYPEWRITER SET

FOR SWITCHED NETWORK SERVICE

WIRING DIAGRAM AND CIRCUIT DESCRIPTIONS

CONTENTS	PAGE
1. GENERAL.....	1
2. WIRING DIAGRAM INDEX (ATTACHMENTS).....	1

which are not a part of a basic set or logic card WDP are listed separately in the index in numerical order.

1. GENERAL

1.01 This section is issued to provide actual and schematic wiring diagrams and detailed circuit description information for the 37 Keyboard Send-Receive (KSR) Teletypewriter Set (Figure 1).

1.02 Notes are included on the diagrams and explain the symbols used or point out certain special conditions that should be observed.

1.03 Most wiring diagrams (WDs) and circuit descriptions (CDs) in this section are a part of one or more wiring diagram packages (WDPs). A complete listing of these WDs and CDs is found on the attached WDP control sheets, and a numerical summary is included in the wiring diagram index. Other WDs and CDs

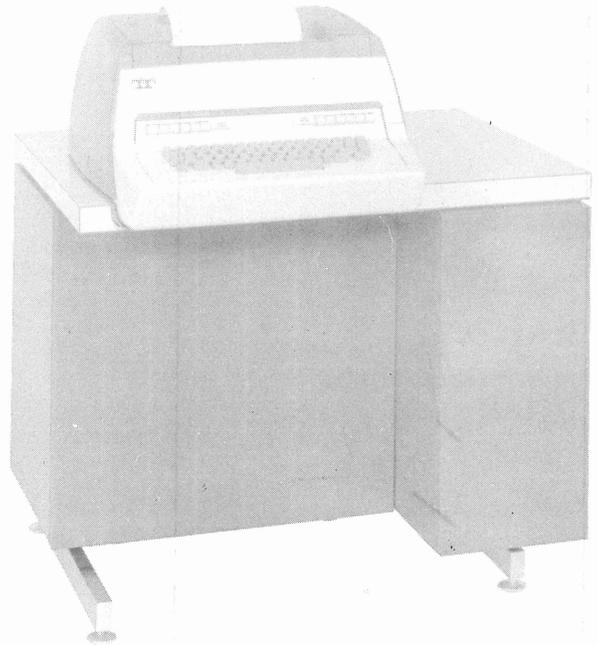


Figure 1 - 37 KSR Teletypewriter Set

2. WIRING DIAGRAM INDEX (ATTACHMENTS)

DRAWING NUMBER	ISSUE NUMBER	TITLE
Wiring Diagram Packages		
WDP0118	10	Basic Wiring Diagram Package for 37 RO, KSR, and ASR Sets. It includes the following WDs and CDs: 8352WD 8360WD 8353WD 8361WD 8358WD 8365WD 8358CD 303150 8359WD

WIRING DIAGRAM INDEX (continued)

DRAWING NUMBER	ISSUE NUMBER	TITLE																																		
Wiring Diagram Packages																																				
WDP0126	11	<p>Wiring Diagram Package for Circuit Card Set TP332595 (KSR). It includes the following WDs and CDs:</p> <table> <tbody> <tr><td>7856WD</td><td>8388CD</td></tr> <tr><td>8369WD</td><td>8389WD</td></tr> <tr><td>8370WD</td><td>8389CD</td></tr> <tr><td>8370CD</td><td>8399WD</td></tr> <tr><td>8371WD</td><td>8773WD</td></tr> <tr><td>8371CD</td><td>8773CD</td></tr> <tr><td>8374WD</td><td>303149</td></tr> <tr><td>8374CD</td><td>322044</td></tr> <tr><td>8376WD</td><td>322047</td></tr> <tr><td>8376CD</td><td>322050</td></tr> <tr><td>8377WD</td><td>322059</td></tr> <tr><td>8377CD</td><td>322062</td></tr> <tr><td>8383WD</td><td>322067</td></tr> <tr><td>8383CD</td><td>322068</td></tr> <tr><td>8387WD</td><td>322070</td></tr> <tr><td>8387CD</td><td>322304</td></tr> <tr><td>8388WD</td><td></td></tr> </tbody> </table>	7856WD	8388CD	8369WD	8389WD	8370WD	8389CD	8370CD	8399WD	8371WD	8773WD	8371CD	8773CD	8374WD	303149	8374CD	322044	8376WD	322047	8376CD	322050	8377WD	322059	8377CD	322062	8383WD	322067	8383CD	322068	8387WD	322070	8387CD	322304	8388WD	
7856WD	8388CD																																			
8369WD	8389WD																																			
8370WD	8389CD																																			
8370CD	8399WD																																			
8371WD	8773WD																																			
8371CD	8773CD																																			
8374WD	303149																																			
8374CD	322044																																			
8376WD	322047																																			
8376CD	322050																																			
8377WD	322059																																			
8377CD	322062																																			
8383WD	322067																																			
8383CD	322068																																			
8387WD	322070																																			
8387CD	322304																																			
8388WD																																				
Other Wiring Diagrams and Circuit Descriptions																																				
7828WD	7	Motor Unit — Actual																																		
7874WD	7	Base — Actual																																		
8362WD	3	Typing Unit (37P001/001/AA and 37P001/001/AB) — Actual																																		
8363WD	2	Function Box (TP319655, TP319776, TP319875) — Actual																																		
8364WD	3	Typing Unit (37P001/001/AD) — Actual																																		
8500WD	1	Keyboard — Actual and Schematic																																		

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER																																	
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30				
8353WD	4X	ACTUAL-YESU 805, 807, 809					2	2	2	2	2																									
8359WD	1	Actual-Power Supply (327803)	2	2	2	2	2	2	2	2	2	2																								
8361WD	1	Actual-Utility Strip	1	1	1	2	2	2	2	2	2	2																								
8365WD	TCR	Analysis Chart-Control Panels	1	1	1	1	1	4	4	4	4	5																								
8365WD	1	Analysis Chart-Control Panels	1	1	2	3	3	4	4	4	4	4																								
8365WD	2	Analysis Chart-Control Panels	1	1	1	2	2	3	3	3	3	3																								
8365WD	3	Analysis Chart-Control Panels	1	1	2	3	3	4	4	4	4	4																								
8365WD	4	Analysis Chart-Control Panels	1	1	1	2	2	3	3	3	3	4																								
8365WD	5	Analysis Chart-Control Panels	1	1	2	2	2	3	3	3	3	4																								
303150	1	Circuit Card-Power Supply Regulator	3	3	3	3	3	3	3	3	3	4																								
8358WD	CDO-CD7	Circuit Description-Power Supply (327803)	1	1	1	1	1	1	1	1	1	1																								

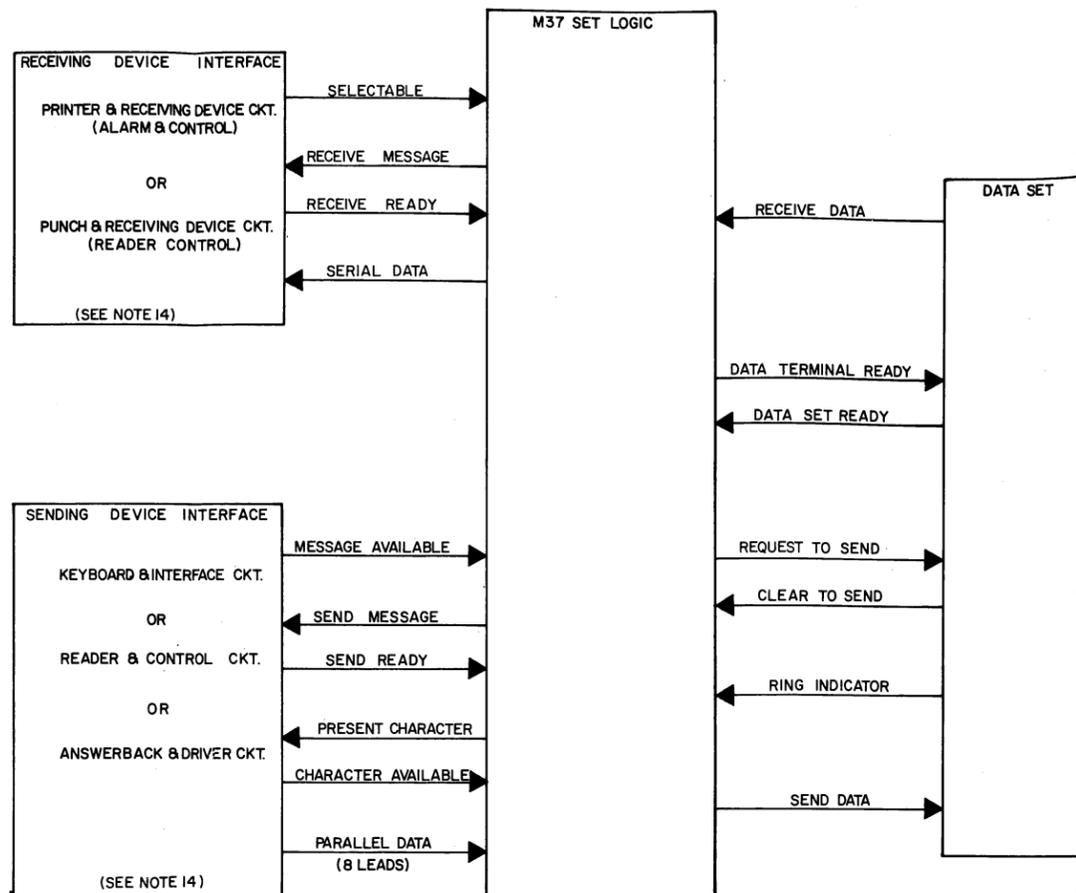
SEE SHEET 3 FOR NOTES.

8352WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-3-68	19717-R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC WIRING DIAGRAM FOR MODEL 37 KSR/ASR (YESU 805, 7)

APPROVALS

D AND R <i>LDM</i>	E OF M <i>[Signature]</i>
-----------------------	------------------------------

E-NUMBER

PROD. NO. 8352 WD.

DATE 8-16-68

P.D. FILE NO. G-A354AA.

DRAWN W.P.B.	CHKD. <i>[Signature]</i>
ENGD. R.E.L.	APPD. <i>[Signature]</i>

TELETYPE CORPORATION

8352WD

8352WD

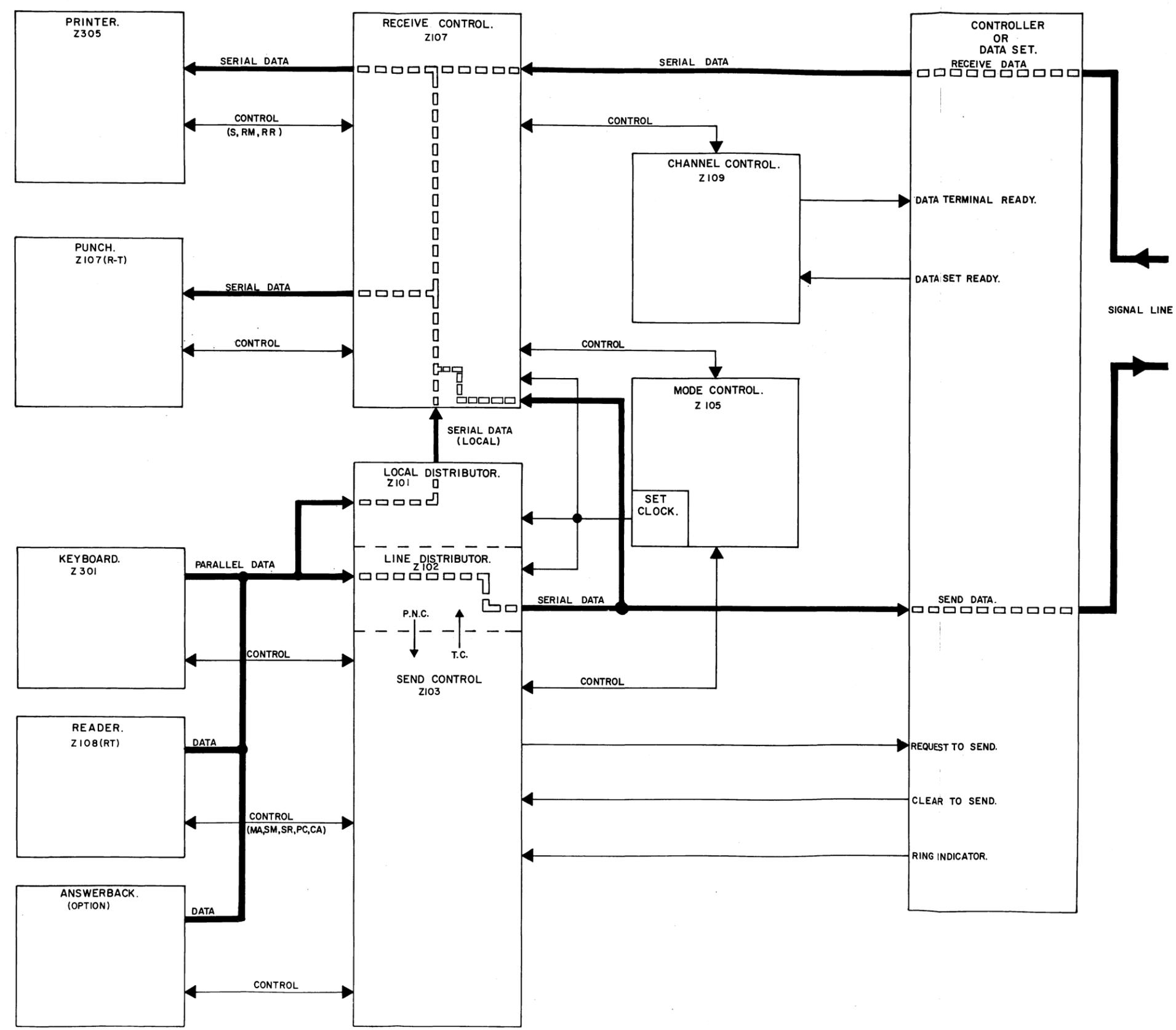
REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-3-68	19717-R
2	6-26-69	99304

NOTE:
REVISION INFORMATION MUST ALSO BE
REFLECTED ON THE ISSUE CONTROL REC-
ORD. WHICH IS A PART OF THIS DRAWING.

RECEIVE CIRCUITS.

SEND CIRCUITS.



SEE ISSUE CONTROL RECORD FOR COM-
PLETE LIST OF SHEETS COMPRISING THIS
W.D.

SHEET 2

SCHEMATIC
WIRING DIAGRAM
FOR
MODEL 37 KSR/ASR
(YESU 805,7)

APPROVALS

D AND R <i>LDM</i>	E OF M <i>[Signature]</i>
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E-NUMBER

PROD. NO. 8352 WD.

DATE 8-16-68

P.D. FILE NO. G-A354AA.

DRAWN W.P.B.	CHKD. <i>[Signature]</i>
ENG. R.E.L.	APPD. <i>[Signature]</i>

TELETYPE
CORPORATION

8352WD

8352WD

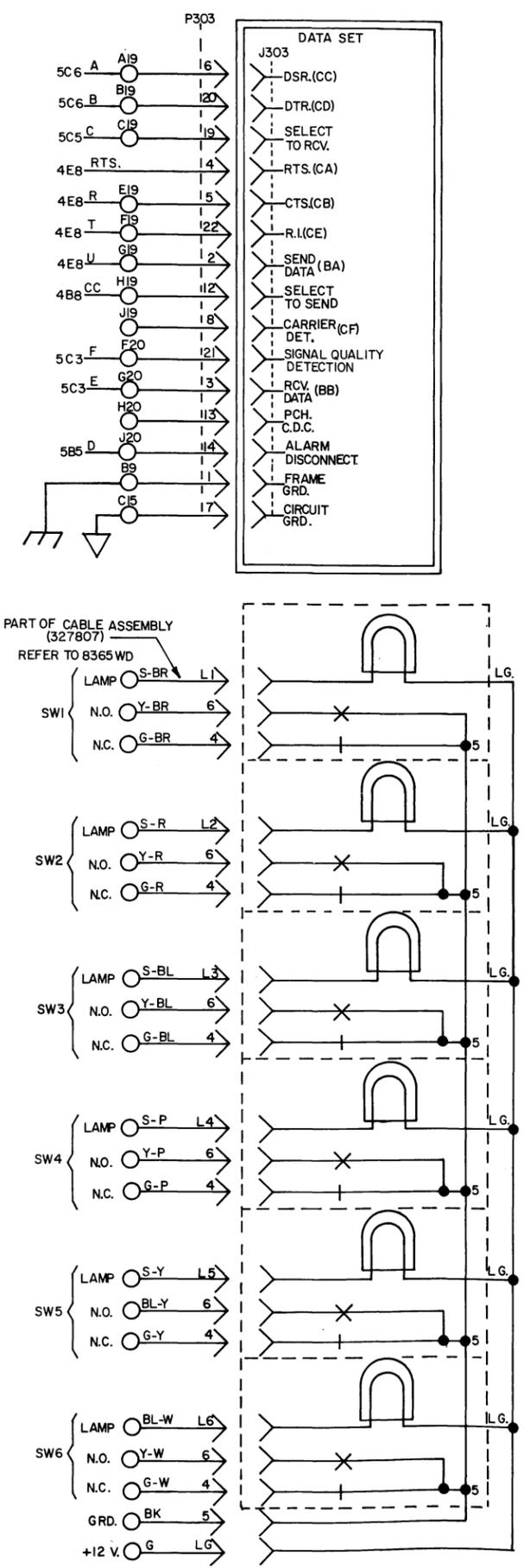
REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-3-68	19717-R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

1. ALL VOLTAGE DC UNLESS OTHERWISE SPECIFIED.
2. TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY, AND ARE NOT MARKED ON COMPONENT.
3. INDICATES FEMALE TERMINAL.
 INDICATES MALE TERMINAL.
4. ALL WIRES 24 AWG. UNLESS OTHERWISE SPECIFIED.
5. TWISTED PAIR:
6. ABBREVIATIONS USED:
 KBD. - KEYBOARD. MA. - MESSAGE AVAILABLE
 PTR. - PRINTER. S.M. - SEND MESSAGE.
 RDR. - READER. S.R. - SEND READY.
 PCH. - PUNCH. PC. - PRESENT CHARACTER.
 FWD. - FORWARD. CA. - CHARACTER AVAILABLE.
 REV. - REVERSE. S.C.S. - SHIFT CONTROL
 AUX. - AUXILIARY. SAMPLE.
 NORM. - NORMALIZE. P.N.C. - PRESENT NEXT
 RCV. - RECEIVE. CHARACTER.
 MESS. - MESSAGE. T.C. - TAKE CHARACTER.
 N.C. - NORMALLY CLOSED. R.S. - REGISTER SAMPLE.
 C.C. - CONTROL CHARACTER.
 N.O. - NORMALLY OPEN. L.C.L. - LOCAL.
 R.T.S. - REQUEST TO SEND.
 F X32 - FREQUENCY TIMES 32. C.T.S.(CB) - CLEAR TO SEND.
 R.I.(CE) - RING INDICATOR.
 SEND INT. - SEND. FDX. - FULL DUPLEX.
 INTERRUPT. HDX. - HALF DUPLEX.
 MAG. - MAGNET. NAK. - NEGATIVE
 SEL. - SELECTOR. ACKNOWLEDGE.
 ENQ. - ENQUIRE. ACK. - ACKNOWLEDGE.
 E.O.T. - END OF TRANSMISSION. D.S.R.(CC) - DATA SET READY.
 SW. - SWITCH. D.T.R.(CD) - DATA TERMINAL READY.
 L. - LAMP. C.D.C. - CALL DIRECTING CODE.
7. S NUMBERS:
8. SEE ASSOCIATED STUNT BOX SCHEMATIC FOR APPROPRIATE FUNCTIONS.
9. ALL CIRCUIT CONNECTIONS ARE SHOWN, BUT MIGHT NOT BE USED ON ALL CIRCUIT CARD ASSEMBLIES
10. DENOTES CIRCUIT GROUND.
 DENOTES FRAME GROUND.
 INDICATES TERMINALS ON TB III WIRING FIELD UNLESS OTHERWISE SPECIFIED.
11. COMMON VOLTAGE INPUTS TO ALL CIRCUIT CARDS.
 VCC - PIN 1
 GRD - PIN 2
 +12V. - PIN 35
 -12V. - PIN 36
12. FOR AC WIRING SEE 8360WD.
13. COLOR CODE
 BR - BROWN Y - YELLOW
 R - RED S - SLATE
 G - GREEN P - PURPLE
 BL - BLUE W - WHITE
 BK - BLACK
14. LINE DIST. - CIRCUIT CARD NAME.
 Z102 - CARD LOCATION IN ELECTRICAL SERVICE UNIT.
 SEE CIRCUIT CARD WDP FOR ASSOCIATED SCHEMATICS
 CIRCUIT CARD PIN NUMBERS ARE THE SAME AS CONNECTOR NUMBERS SHOWN

15. CROSS REFERENCE NOTATION.
 4 B2 COLUMN. ROW SHEET
16. REFERENCE SCHEMATIC DIAGRAMS:
 DATA SET 103G - SD100961.
 DATA SET 103H - SD10121



TYPICAL CONTROL SWITCH (TO BE WIRED PER 8365WD.)

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 3

SCHMATIC WIRING DIAGRAM FOR MODEL 37 KSR/ASR (YESU 805,7)

APPROVALS
 D AND R *LDM* E OF M *[Signature]*

E-NUMBER
 PROD. NO. 8352 WD.

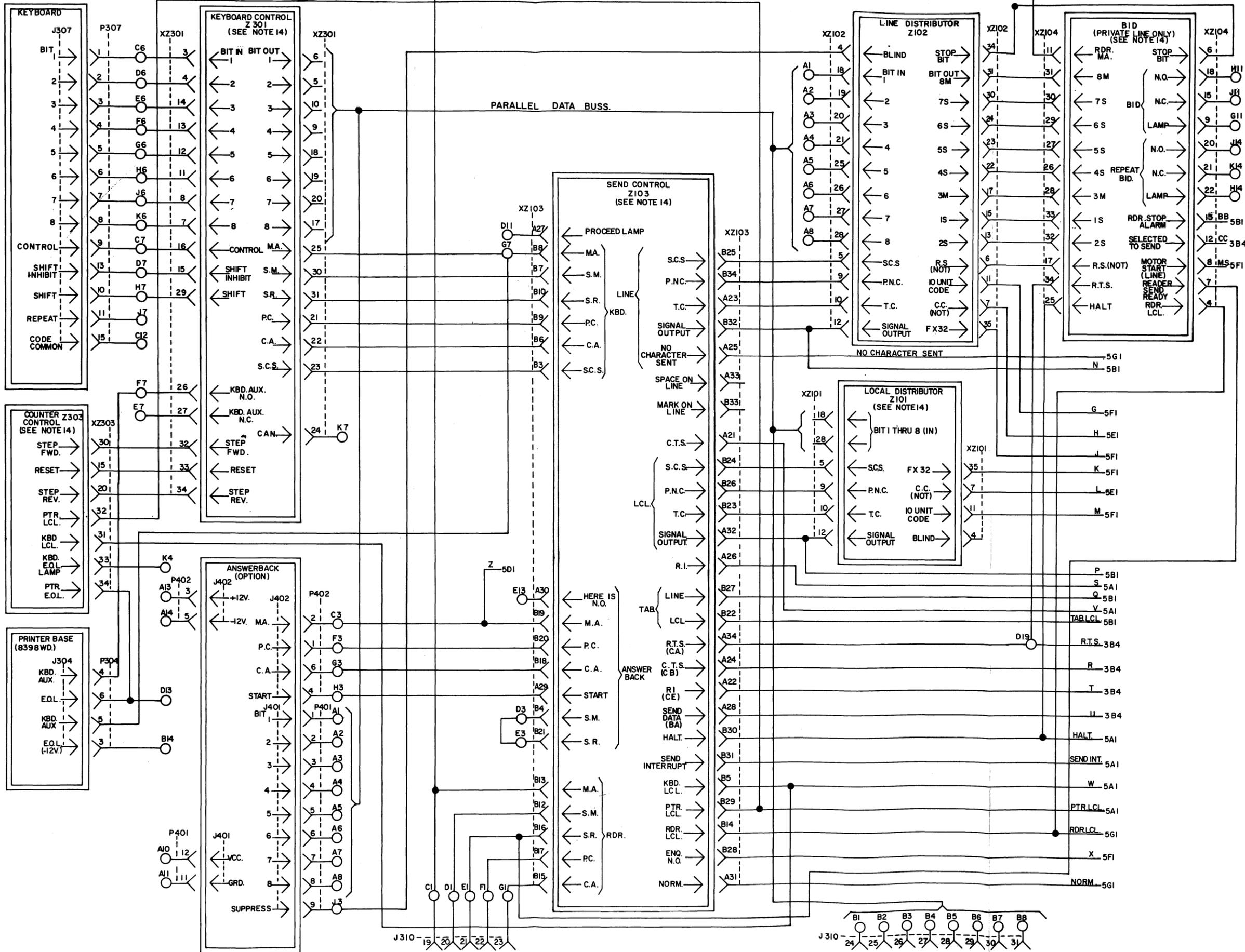
DATE 8-15-68
 P.D. FILE NO. G-A354AA

DRAWN W.P.B. CHKD *[Signature]*
 ENGD. C.A.Y. APPD. *[Signature]*

TELETYPE CORPORATION

8352WD

SEE SHEET 3 FOR NOTES.



8352 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-3-68	19717-R.
2	6-25-69	99304

SHEET 4

SCHEMATIC WIRING DIAGRAM FOR MODEL 37 KSR/ASR (YESU 805,7)

APPROVALS

D AND R E OF M

E-NUMBER

PROD. NO. 8352 WD.

DATE 6-20-68

P.D. FILE NO. G-A354AA

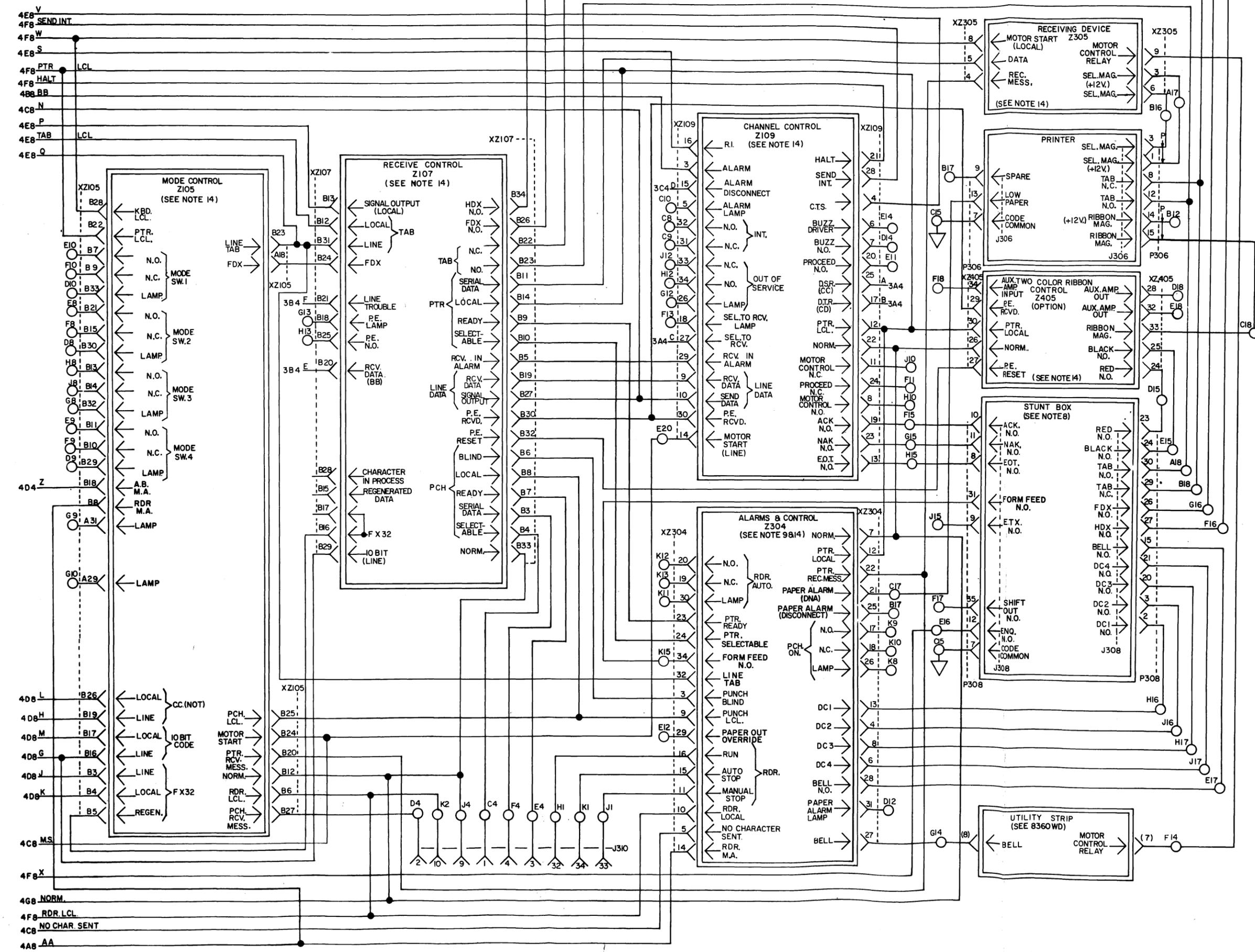
DRAWN W.R.B. CHKD.

ENGD. CAY./R.F.W. APPD.

TELETYPE CORPORATION

8352 WD

SEE SHEET 3 FOR NOTES.



8352WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-3-68	19717-R
2	6-25-69	99304

NOTE:
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SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 5 WDP

SCHEMATIC WIRING DIAGRAM FOR MODEL 37 KSR/ASP (YESU 805,7)

APPROVALS

D AND R	E OF M
<i>[Signature]</i>	<i>[Signature]</i>

E-NUMBER
 PROD. NO. 8352WD
 DATE 6-20-68
 P.D. FILE NO. G-A354AA
 DRAWN W.P.B. CHKD. *[Signature]*
 ENGD. C.A.Y. APPD. *[Signature]*

TELETYPE CORPORATION

8352WD

ISSUE CONTROL RECORD

8353WD

SHEET NO.	ISSUE																		
	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
1C	X	X																	
2C																			
3C	X																		
4C																			
5C	X																		
6C	X																		
7C	X																		
1X	X	X																	
2X	X	X																	
3X	X	X																	
4X	X	X																	
1	X	X																	
2	X	X																	
3	X	X																	
4	X	X																	
5	X	X																	
6	X	X																	
7	X	X																	

REVISIONS		
ISSUE	DATE	AUTH. NO.
- 1	12-6-68	19717-R
2	5-9-69	99130
3	5-20-69	99131
- 4	6-3-69	99130-2

WDP

ISSUE CONTROL SHEET 1 OF 1

ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805, 7,9

APPROVALS

D AND R	E OF M
<i>LDM</i>	<i>[Signature]</i>

E-NUMBER
PROD. NO. 8353WD

DATE:
P.D. FILE NO.
DRAWN. *[Signature]* CHKD. *[Signature]*
ENGD. *[Signature]* APPD. *[Signature]*

TELETYPE CORPORATION

8353WD

ACTUAL WIRING DIAGRAM
FOR ELECTRICAL SERVICE UNITS YESU 805, 7, 9
USED ON MODEL 37

8353WD
Issue
Page 1C of 7C

SEE ISSUE CONTROL
RECORD FOR COM-
PLETE LIST OF SHEETS
COMPRISING THIS
W.D.

1. PAGE NUMBERING

This WD consists of three sections: the issue control (and notes), the network listing index pages, and the network listing pages.

Page 3 of 4 means the third page of 4 issue control sheets.

Page 2X of 11X/30 is the 2nd page of 11 index pages in a WD having 30 total pages.

Page 10 of 15/30 is the 10th of 15 network pages in a WD having 30 total pages.

2. ISSUE CONTROL SHEETS

The issue control sheets contain the release information and notes pertaining to the WD.

3. NETWORK LISTING INDEX

The index pages list components and pin designations in alphanumeric, alphabetical and numerical order and indicate the number of the network (net) in which each appears.

4. NETWORK LISTING

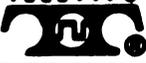
All pins with the same network listing number are electrically common. Any pin is connected to the pin listed immediately below (see sample net 0001). Where a pin is connected to two succeeding pins, one of the following pin designations will be indented, thereby indicating that the original is connected to the pin below it and to the indented pin (see sample net 0002). Where a pin is connected to more than two succeeding pins, additional indented columns will be used. The original pin is connected to all the pins at the end of the columns of dots and to the indented pin immediately below, (see sample net 0003). There is no direct connection between a pin and one listed below and in a column to its left.

5. Issue 2 added the following wires:

<u>FROM</u>	<u>TO</u>	<u>FROM</u>	<u>TO</u>
XZ304-34	TB111-K15	XZ104-8	XZ105-B24
XZ304-32	Z103-B27	XZ303-31	XZ103-B5
XZ304-29	TB111-E12	XZ303-32	XZ103-B29
XZ104-4	XZ103-B14	XZ303-34	TB111-D13
XZ104-6	XZ102-34	XZ405-34	TB111-F18
XZ104-7	XZ103-B16	XZ109-14	TB111-E20

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

WDP



NETWORK LISTING (TABULAR WIRING DIAGRAM)

ISSUE CONTROL

TITLE
ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805, 7, 9

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
8353 WD	1	MODEL 37	6/30/68	20	70

SAMPLE NETWORK (ARROWS SHOW CONNECTIONS)

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

Net	Component	Pin
0001	TB5001	A 1
	↓	
0001	TB5009	H 9
	↓	
0001	TB5011	A 1
0002	TB5001	B 5
	↓	
0002	BB5001	C 1
	↓	
0002	• TB5002	B 6
	↓	
0002	• PS5002	J 3
	↓	
0002	• • TB5001	D 2
	↓	
0002	• • TB5002	C 6
	↓	
0002	• • TB5002	A 10
	↓	
0002	• TB5001	K 5
	↓	
0002	TB5011	B 5
0003	TB5011	B 6
	↓	
0003	TB5012	B 5
	↓	
0003	• • • • TB5014	A 8
	↓	
0003	• • • • TB5014	A 2
	↓	
0003	• • • • TB5014	B 5
	↓	
0003	• • • • TB5014	B 6
	↓	
0003	• • • • TB5014	D 3
	↓	
0003	• • • • TB5014	E 9
	↓	
0003	TB5009	E 10

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

WDP

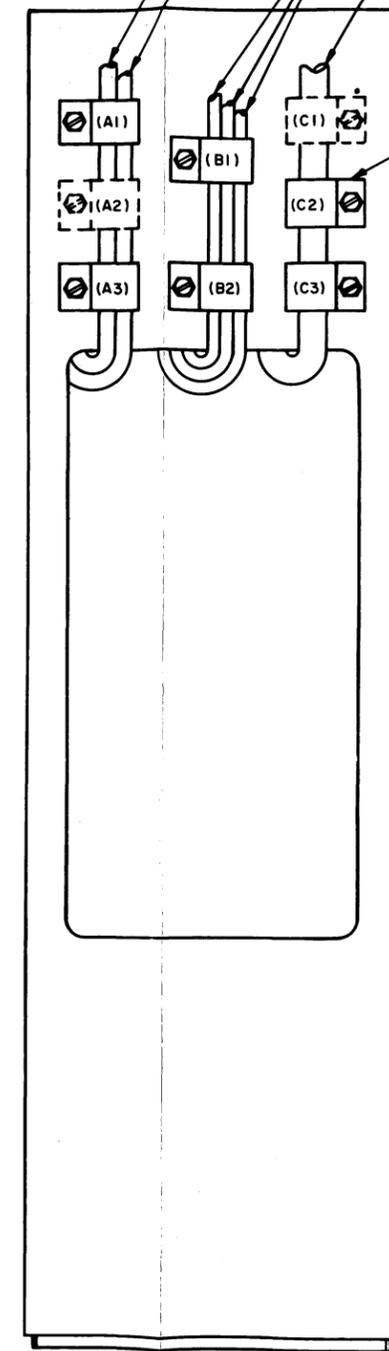
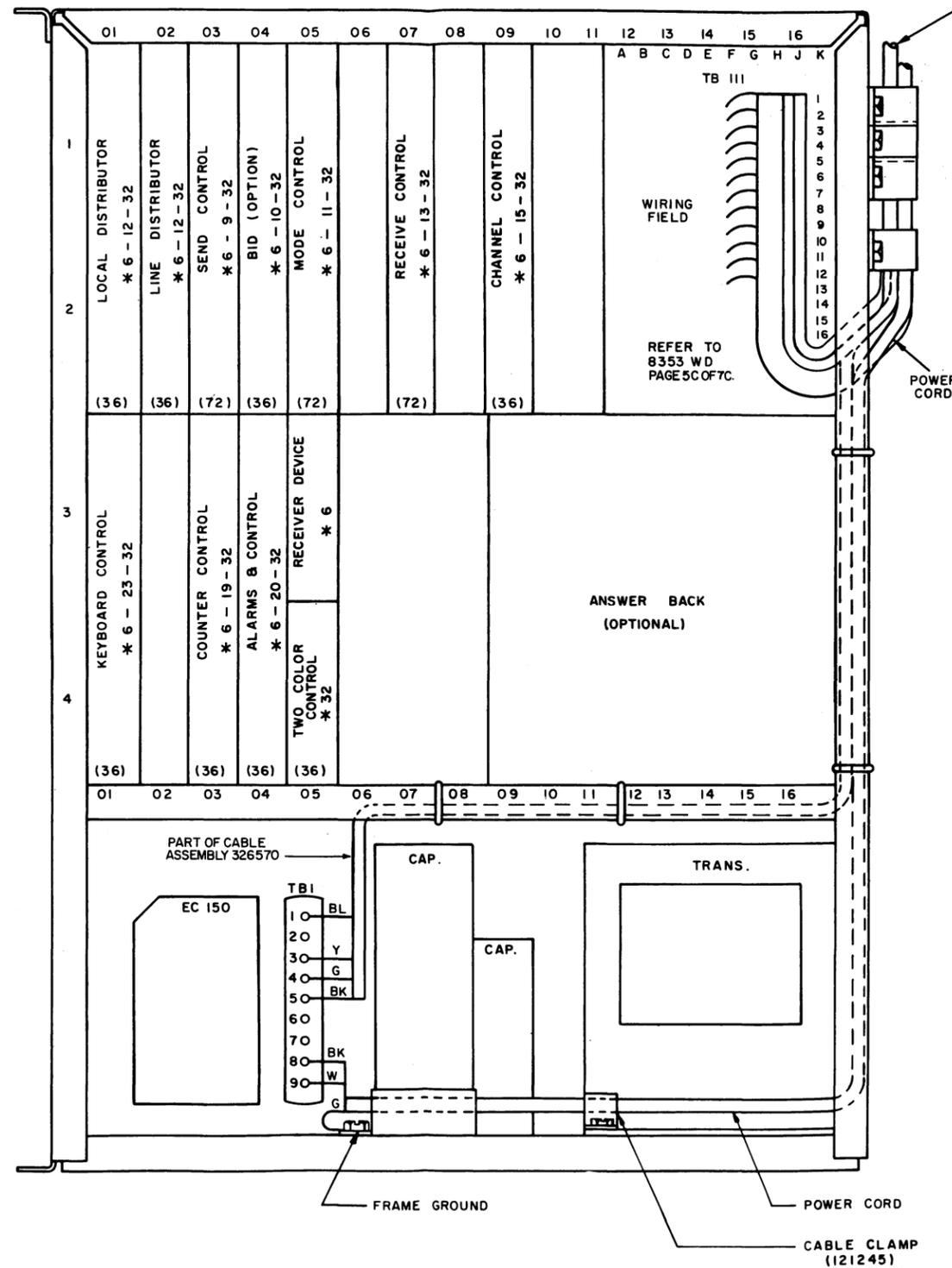
8353WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19717-R
2	5-20-69	99131

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

COMPONENT LOCATION



VIEWED FROM CARD SIDE

VIEWED FROM REAR

- NOTES
1. TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY AND ARE NOT MARKED ON THE COMPONENTS.
 2. NAMES SHOWN IN CIRCUIT CARD CONNECTOR LOCATIONS INDICATES THE FAMILY OF CARDS TO BE USED IN THOSE POSITIONS.
 3. THE NUMBER IN PARENTHESES () SHOWN IN CIRCUIT CARD CONNECTOR LOCATIONS INDICATES THE NUMBER OF CONNECTOR PINS.
(36) - 148440 CONNECTOR
(72) - 193263 CONNECTOR
 4. * - INDICATES LOCATION OF POLARIZING TABS, 148459. (THAT IS - SLOT 6 IS BETWEEN PINS 6 & 7).
 5. CABLE CLAMPS A & C (POSITIONS 1 & 2) ARE INSTALLED DEPENDENT UPON CABLE ROUTING.
FOR INSTALLATIONS WHERE CABLES ARE ROUTED TO THE LEFT OF THE MODULE, POSITIONS A2 & C1 SHOULD BE USED.
FOR INSTALLATIONS WHERE CABLES ARE ROUTED TO THE RIGHT OF THE MODULE, POSITIONS A1 & C2 SHOULD BE USED.
 6. THE NUMBER OF 327807 CABLE ASSEMBLIES USED DEPENDS UPON THE CONTROL PANEL ARRANGEMENT.
 7. COLOR CODE:
BK - BLACK BR - BROWN
BL - BLUE R - RED
G - GREEN O - ORANGE
Y - YELLOW P - PURPLE
W - WHITE S - SLATE
 8. N.O. - NORMALLY OPEN.
N.C. - NORMALLY CLOSE.
 9. CABLE ASSEMBLY 327808 IS USED TO ADD A KEYBOARD TO AN R.O.
 10. CABLE ASSEMBLY 326570 IS PART OF THE YESU 807.
 11. FOR 327803 POWER SUPPLY, SEE 8358WD AND 8359WD, SCHEMATIC AND ACTUAL WIRING DIAGRAMS.
 12. FOR 326593 UTILITY STRIP, SEE 8360WD AND 8361WD, SCHEMATIC AND ACTUAL WIRING DIAGRAMS.
 13. SEE 8352WD FOR ASSOCIATED SCHEMATIC WIRING DIAGRAM.

NDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.
PAGE 3C OF 7C

ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU 805, 7, 9

APPROVALS

D AND R E OF M
LDM

E-NUMBER
PROD. NO. 8353WD

DATE 4-23-68
P.D. FILE NO. 43-A254AA

DRAWN R.W.D. CHKD. [Signature]
ENGD. M.J.R. APPD. [Signature]

TELETYPE CORPORATION

8353WD

REFER TO PAGE 3C FOR NOTES
 326565 CABLE ASSEMBLY, ALL
 WIRE 18AWG.
 ▲-DENOTES 2 WIRES.

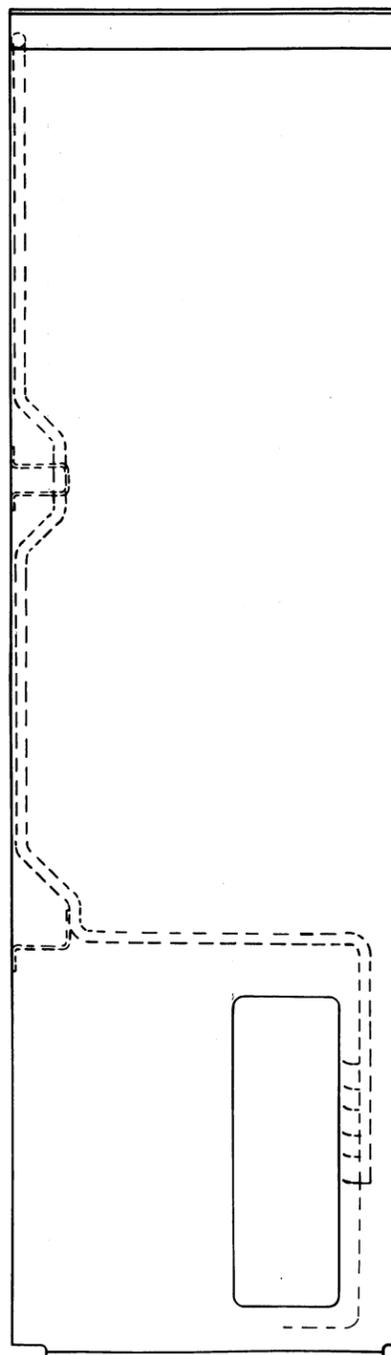
POWER SUPPLY CONNECTIONS

NOTE:
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 ORD, WHICH IS A PART OF THIS DRAWING.

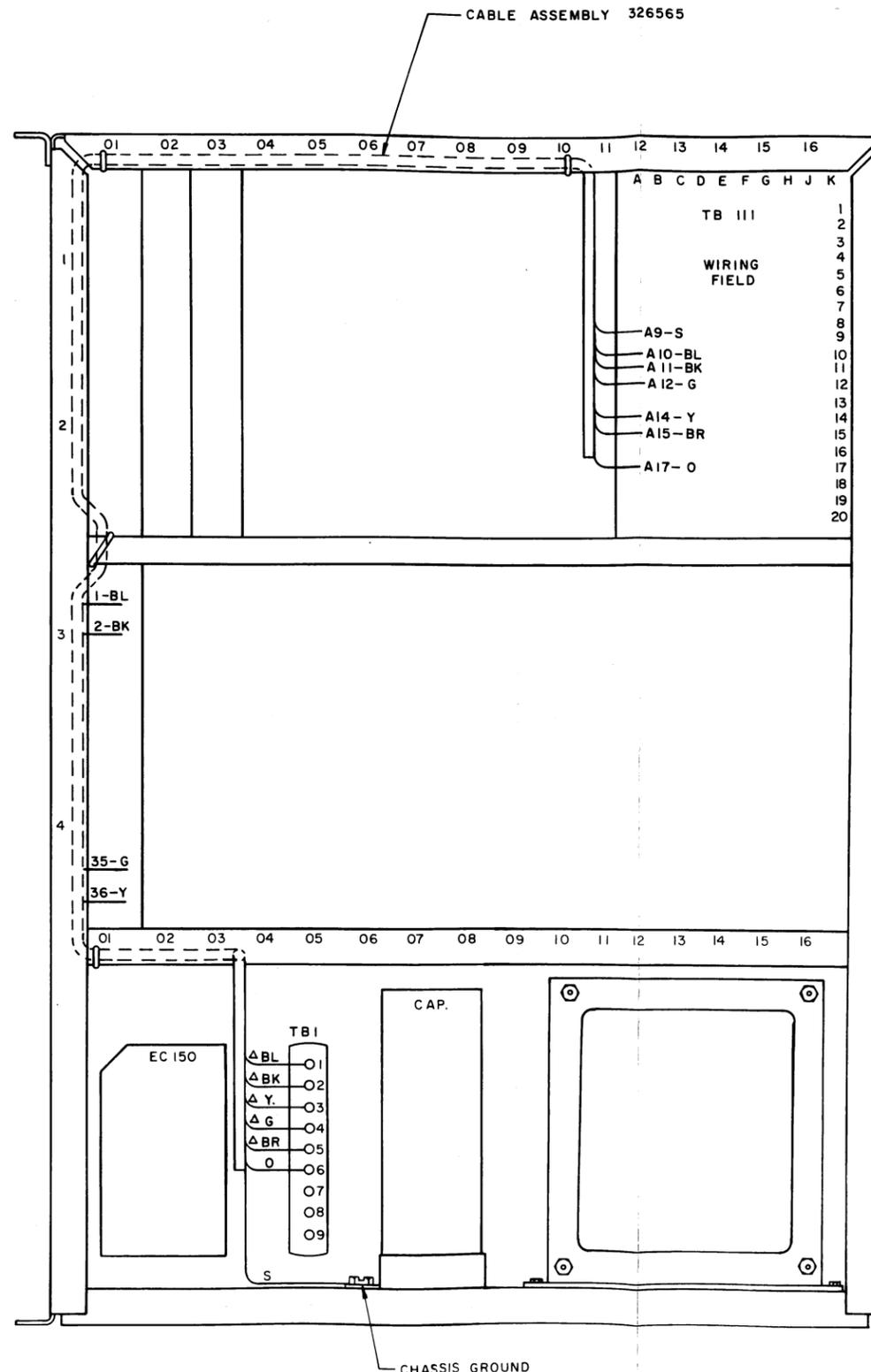
8353WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19717-R



VIEWED FROM FRONT SIDE



VIEWED FROM CARD SIDE

SEE ISSUE CONTROL RECORD FOR COM-
 PLETE LIST OF SHEETS COMPRISING THIS
 W.D.

PAGE 4C OF 7C

ACTUAL
 WIRING DIAGRAM
 FOR
 ELECTRICAL SERVICE
 UNITS
 YESU 805,7,9

APPROVALS

D AND R *[Signature]* E OF M *[Signature]*

E-NUMBER

PROD. NO. 8353WD

DATE 4-24-68

P.D. FILE NO. 43-A254AA

DRAWN RWD CHKD. *[Signature]*

ENGD. M.J.R. APPD. *[Signature]*

TELETYPE
 CORPORATION

8353WD

REFER TO PAGE 3C FOR NOTES

TB III SIGNAL LOCATION

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8353WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	12-6-68	19717-R
2	5-20-69	99131

	A	B	C	D	E	F	G	H	J	K
1	I	P D	MESSAGE AVAILABLE (MA)	SEND MESSAGE (SM)	READY (R) READER NO.1	PRESENT CHARACTER (PC)	CHARACTER AVAILABLE (CA)	RUN	MANUAL STOP	AUTOMATIC STOP
2	2	A A								READER LOCAL
3	3	R T	MESSAGE AVAILABLE (MA)	SEND MESSAGE (SM)	READY (R) ANSWER BACK	PRESENT CHARACTER (PC)	CHARACTER AVAILABLE (CA)	START	BLIND	
4	4	A A	SELECTABLE	RECEIVE MESSAGE	READY (R) PUNCH NO.1	DATA (D)	EOT	FEEDOUT	NORMALIZE	KEYBOARD END OF LINE LAMP
5	5	L B								
6	6	L I	BIT 1 N.C.	BIT 2 N.C.	BIT 3 N.C.	BIT 4 N.C.	BIT 5 N.C.	BIT 6 N.C.	BIT 7 N.C.	BIT 8 N.C.
7	7	E T	CONTROL CHARACTER	SHIFT INHIBIT	AUXILIARY CONTACT N.C. KEYBOARD	AUXILIARY CONTACT N.O.	AUXILIARY CONTACT (MESS.AVAIL.)	SHIFT	KEYBOARD REPEAT	
8	8	L S								
9		FRAME GROUND	FRAME GROUND							
10		+ 5 VOLTS.	+ 5 VOLTS.							
11		GROUND	GROUND	GROUND						
12		+ 12 VOLTS.	+ 12 VOLTS.	GROUND						
13		+ 12 VOLTS.	+ 12 VOLTS.	GROUND						
14		- 12 VOLTS.	- 12 VOLTS.	GROUND			MOTOR RELAY BASE	BELL (COIL)		
15		HIGH CURRENT GROUND	HIGH CURRENT GROUND	GROUND	ESC 3	ESC 4	ACK	NAK	EOT	ETX
16		CHARACTER DETECTED	SELECTOR MAGNET			ENQ	HDX NO.	FDX NO.	DC1	DC2
17		SELECTOR MAGNET RETURN	PAPER OUT (PO)	LOW PAPER (LP)		BELL	SO		DC3	DC4
18		TAB N.O.	TAB N.C. PRINTER	RIBBON MAGNET	AUXILIARY AMPLIFIER MAGNET DRIVER	AUXILIARY AMPLIFIER LAMP DRIVER OUTPUT STUNT BOX	AUXILIARY AMPLIFIER INPUT			
19		DATA SET READY (CC)	DATA TERMINAL READY (CD)	SELECTED TO RECEIVE	REQUEST TO SEND (CA)	CLEAR TO SEND (CB)	RING INDICATOR (CE)	TRANSMITTED DATA (BA)	SELECTED TO SEND	DATA CARRIER DETECTED (CF)
20						MOTOR START	DATA SET MODULATION FAILURE	RECEIVE DATA (BB)	ALARM DISCONNECT	

DATA SET

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

PAGE 5C OF 7 C

ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU 805, 7, 9

APPROVALS	
D AND R <i>L & M</i>	E OF M ---
E-NUMBER	
PROD. NO. 8353 WD	
DATE 4-30-68	
P.D. FILE NO. G-A354AA	
DRAWN W.P.B.	CHKD. <i>JS</i>
ENGD. M.J.R.	APPD. <i>JS</i>

TELETYPE CORPORATION
8353WD

8353WD

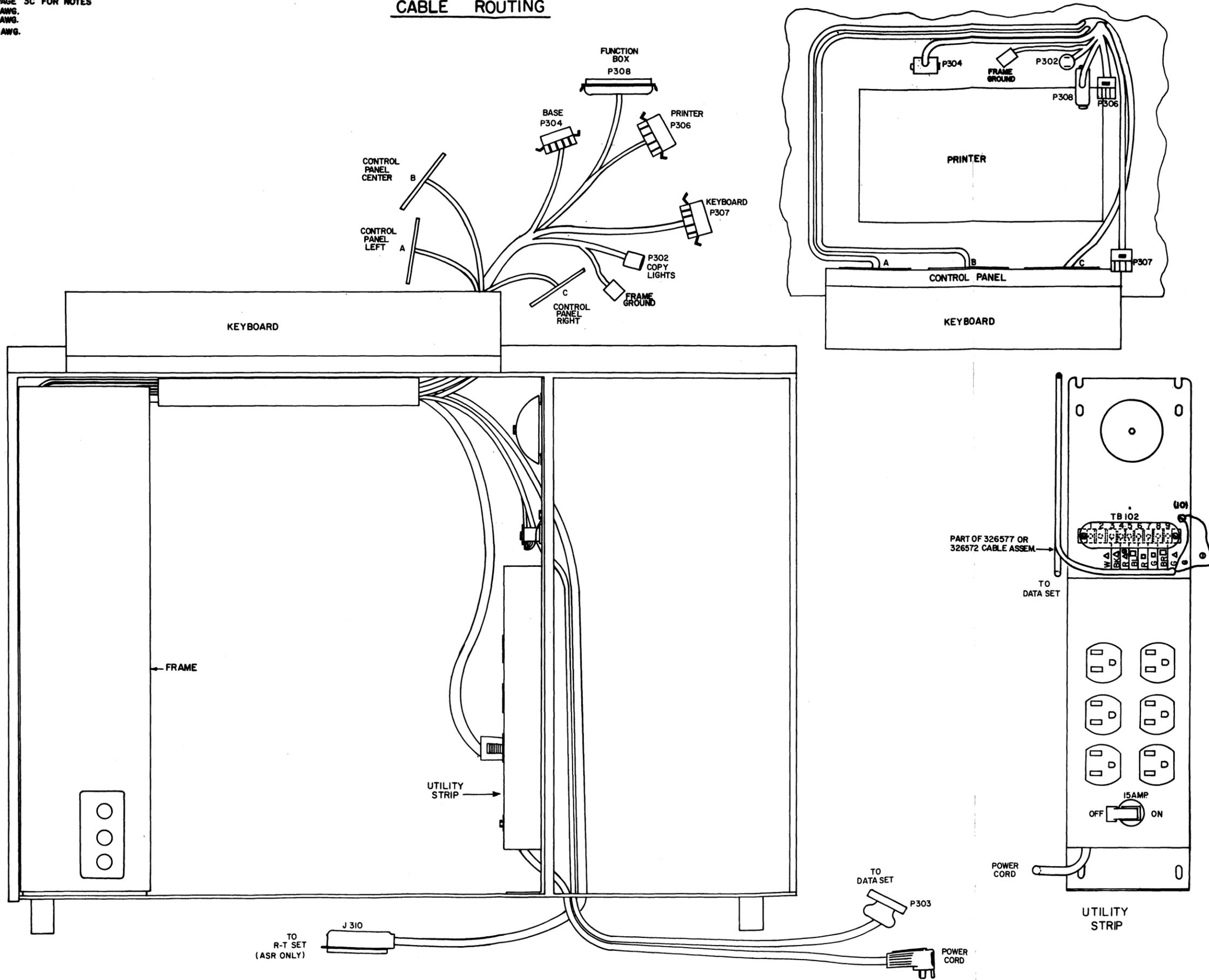
REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-6-68	19717-R
2	5-20-69	99131

NOTE:
 REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

CABLE ROUTING

REFER TO PAGE 3C FOR NOTES
 ▲ - DENOTES 18 AWG.
 □ - DENOTES 24 AWG.
 ● - DENOTES 20 AWG.



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

PAGE 6C OF 7C

ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU 805,7,9

APPROVALS

D AND R <i>LDM</i>	E OF M <i>[Signature]</i>
-----------------------	------------------------------

E-NUMBER
 PROD. NO. 8353 WD
 DATE 6-14-68
 R.D. FILE NO. G-A354AA
 DRAWN W.P.B. CHKD. *[Signature]*
 ENGD. R.E.L. APPD. *[Signature]*

TELETYPE CORPORATION

8353WD



NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

WDP

TITLE ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805.7.9			
WIRING DIAGRAM 8353WD	ISSUE 23	USED ON MODEL 37	DATE 05/01/69 6-3-69
		PAGE 1X	OF

COMPONENT	PIN	NET
TB111	A 1	0001
TB111	A 2	0002
TB111	A 3	0003
TB111	A 4	0004
TB111	A 5	0005
TB111	A 6	0006
TB111	A 7	0007
TB111	A 8	0008
TB111	A 9	0009
TB111	A10	0010
TB111	A11	0011
TB111	A12	0012
TB111	A13	0012
TB111	A14	0013
TB111	A15	0014
TB111	A17	0015
TB111	A18	0016
TB111	A19	0017
TB111	B 1	0001
TB111	B 2	0002
TB111	B 3	0003
TB111	B 4	0004
TB111	B 5	0005
TB111	B 6	0006
TB111	B 7	0007
TB111	B 8	0008
TB111	B 9	0009
TB111	B10	0010
TB111	B11	0011
TB111	B12	0012
TB111	B13	0012
TB111	B14	0013
TB111	B15	0014
TB111	B16	0018
TB111	B17	0019
TB111	B18	0020
TB111	B19	0021
TB111	C 1	0022
TB111	C 3	0023
TB111	C 4	0024
TB111	C 6	0025
TB111	C 7	0026
TB111	C 8	0027
TB111	C 9	0028
TB111	C10	0029
TB111	C11	0011
TB111	C12	0011
TB111	C13	0011
TB111	C14	0011
TB111	C15	0011
TB111	C17	0030
TB111	C18	0031
TB111	C19	0032

COMPONENT	PIN	NET
TB111	D 1	0033
TB111	D 3	0034
TB111	D 4	0035
TB111	D 6	0036
TB111	D 7	0037
TB111	D 8	0038
TB111	D 9	0039
TB111	D10	0040
TB111	D11	0041
TB111	D12	0042
TB111	D13	0043
TB111	D14	0044
TB111	D15	0045
TB111	D18	0046
TB111	D19	0047
TB111	E 1	0048
TB111	E 3	0049
TB111	E 4	0050
TB111	E 6	0051
TB111	E 7	0052
TB111	E 8	0053
TB111	E 9	0054
TB111	E10	0055
TB111	E11	0056
TB111	E12	0057
TB111	E13	0058
TB111	E14	0059
TB111	E15	0060
TB111	E16	0061
TB111	E17	0062
TB111	E18	0063
TB111	E19	0064
TB111	E20	0065
TB111	F 1	0066
TB111	F 3	0067
TB111	F 4	0068
TB111	F 6	0069
TB111	F 7	0070
TB111	F 8	0071
TB111	F 9	0072
TB111	F10	0073
TB111	F11	0074
TB111	F13	0075
TB111	F14	0076
TB111	F15	0077
TB111	F16	0078
TB111	F18	0079
TB111	F19	0080
TB111	F20	0081
TB111	G 1	0082
TB111	G 3	0083
TB111	G 6	0084
TB111	G 7	0085

COMPONENT	PIN	NET
TB111	G 8	0086
TB111	G 9	0087
TB111	G10	0088
TB111	G11	0089
TB111	G12	0090
TB111	G13	0091
TB111	G14	0092
TB111	G15	0093
TB111	G16	0094
TB111	G19	0095
TB111	G20	0096
TB111	H 1	0097
TB111	H 3	0098
TB111	H 6	0099
TB111	H 7	0100
TB111	H 8	0101
TB111	H10	0102
TB111	H11	0103
TB111	H12	0104
TB111	H13	0105
TB111	H14	0106
TB111	H15	0107
TB111	H16	0108
TB111	H17	0109
TB111	H19	0110
TB111	J 1	0111
TB111	J 3	0112
TB111	J 4	0113
TB111	J 6	0114
TB111	J 8	0115
TB111	J10	0116
TB111	J11	0117
TB111	J12	0118
TB111	J14	0119
TB111	J16	0120
TB111	J17	0121
TB111	J20	0122
TB111	K 1	0123
TB111	K 2	0124
TB111	K 4	0125
TB111	K 6	0126
TB111	K 7	0127
TB111	K 8	0128
TB111	K 9	0129
TB111	K10	0130
TB111	K11	0131
TB111	K12	0132
TB111	K13	0133
TB111	K14	0134
TB111	K15	0135
XZ101	1	0136
XZ101	2	0137
XZ101	5	0138

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.



NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

TITLE ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805.7.9			
WIRING DIAGRAM B353WD	ISSUE 23	USED ON MODEL 37	DATE 05101169 6-3-69
		PAGE 2X	OF

COMPONENT	PIN	NET
XZ101	7	0139
XZ101	9	0140
XZ101	10	0141
XZ101	11	0142
XZ101	12	0143
XZ101	18	0001
XZ101	19	0002
XZ101	20	0003
XZ101	21	0004
XZ101	25	0005
XZ101	26	0006
XZ101	27	0007
XZ101	28	0008
XZ101	35	0144
XZ101	36	0145
XZ102	1	0136
XZ102	2	0137
XZ102	4	0112
XZ102	5	0146
XZ102	6	0147
XZ102	7	0148
XZ102	9	0149
XZ102	10	0150
XZ102	11	0151
XZ102	12	0152
XZ102	13	0153
XZ102	15	0154
XZ102	17	0155
XZ102	18	0001
XZ102	19	0002
XZ102	20	0003
XZ102	21	0004
XZ102	22	0156
XZ102	23	0157
XZ102	24	0158
XZ102	25	0005
XZ102	26	0006
XZ102	27	0007
XZ102	28	0008
XZ102	30	0159
XZ102	31	0160
XZ102	35	0161
XZ102	36	0145
XZ103	A21	0162
XZ103	A22	0080
XZ103	A23	0150
XZ103	A24	0064
XZ103	A25	0163
XZ103	A26	0164
XZ103	A27	0041
XZ103	A28	0095
XZ103	A29	0098
XZ103	A30	0058

COMPONENT	PIN	NET
XZ103	A31	0113
XZ103	A32	0143
XZ103	A34	0047
XZ103	B 1	0136
XZ103	B 2	0137
XZ103	B 3	0165
XZ103	B 4	0034
XZ103	B 5	0166
XZ103	B 6	0167
XZ103	B 7	0168
XZ103	B 8	0085
XZ103	B 9	0169
XZ103	B10	0170
XZ103	B12	0033
XZ103	B13	0022
XZ103	B14	0124
XZ103	B15	0082
XZ103	B16	0048
XZ103	B17	0066
XZ103	B18	0083
XZ103	B19	0023
XZ103	B20	0067
XZ103	B21	0049
XZ103	B22	0171
XZ103	B23	0141
XZ103	B24	0138
XZ103	B25	0146
XZ103	B26	0140
XZ103	B27	0172
XZ103	B28	0061
XZ103	B29	0173
XZ103	B30	0174
XZ103	B31	0175
XZ103	B32	0152
XZ103	B34	0149
XZ103	B35	0176
XZ103	B36	0145
XZ104	1	0136
XZ104	2	0137
XZ104	4	0124
XZ104	6	0149 0143
XZ104	7	0048
XZ104	8	0065
XZ104	9	0089
XZ104	11	0022
XZ104	12	0110
XZ104	13	0177
XZ104	15	0117
XZ104	17	0147
XZ104	18	0103
XZ104	20	0119
XZ104	21	0134
XZ104	22	0106

COMPONENT	PIN	NET
XZ104	25	0174
XZ104	26	0156
XZ104	27	0157
XZ104	28	0155
XZ104	29	0158
XZ104	30	0159
XZ104	31	0160
XZ104	32	0153
XZ104	33	0154
XZ104	34	0047
XZ104	35	0176
XZ104	36	0145
XZ105	A18	0178
XZ105	A29	0088
XZ105	A31	0087
XZ105	B 1	0136
XZ105	B 2	0137
XZ105	B 3	0161
XZ105	B 4	0144
XZ105	B 5	0179
XZ105	B 6	0124
XZ105	B 7	0055
XZ105	B 8	0022
XZ105	B 9	0073
XZ105	B10	0072
XZ105	B11	0054
XZ105	B12	0113
XZ105	B13	0101
XZ105	B14	0115
XZ105	B15	0071
XZ105	B16	0151
XZ105	B17	0142
XZ105	B18	0023
XZ105	B19	0148
XZ105	B20	0180
XZ105	B21	0053
XZ105	B22	0173
XZ105	B23	0172
XZ105	B24	0065
XZ105	B25	0181
XZ105	B26	0139
XZ105	B27	0035
XZ105	B28	0166
XZ105	B29	0039
XZ105	B30	0038
XZ105	B32	0086
XZ105	B33	0040
XZ105	B35	0176
XZ105	B36	0145
XZ107	B 1	0136
XZ107	B 2	0137
XZ107	B 3	0068
XZ107	B 4	0024

XZ102 34 0193



NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

TITLE ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805.7.9			
WIRING DIAGRAM 8353WD	ISSUE 3	USED ON MODEL 37	DATE 05/01/69 6-3-69
		PAGE 3X	OF

COMPONENT	PIN	NET
XZ107	B 5	0182
XZ107	B 6	0183
XZ107	B 7	0050
XZ107	B 8	0181
XZ107	B 9	0184
XZ107	B 10	0185
XZ107	B 11	0186
XZ107	B 12	0171
XZ107	B 13	0143
XZ107	B 14	0173
XZ107	B 16	0179
XZ107	B 18	0091
XZ107	B 19	0187
XZ107	B 20	0096
XZ107	B 21	0081
XZ107	B 22	0020
XZ107	B 23	0016
XZ107	B 24	0178
XZ107	B 25	0105
XZ107	B 26	0094
XZ107	B 27	0152
XZ107	B 29	0151
XZ107	B 30	0188
XZ107	B 31	0172
XZ107	B 32	0189
XZ107	B 33	0113
XZ107	B 34	0078
XZ107	B 36	0145
XZ109	1	0136
XZ109	2	0137
XZ109	3	0177
XZ109	4	0162
XZ109	5	0029
XZ109	6	0059
XZ109	7	0044
XZ109	8	0102
XZ109	9	0187
XZ109	10	0152
XZ109	11	0116
XZ109	12	0173
XZ109	13	0107
XZ109	14	0065
XZ109	15	0122
XZ109	16	0164
XZ109	17	0021
XZ109	18	0075
XZ109	19	0077
XZ109	20	0056
XZ109	21	0174
XZ109	22	0113
XZ109	23	0093
XZ109	24	0074
XZ109	25	0017

COMPONENT	PIN	NET
XZ109	26	0090
XZ109	27	0032
XZ109	28	0175
XZ109	29	0182
XZ109	30	0188
XZ109	31	0028
XZ109	32	0027
XZ109	33	0118
XZ109	34	0104
XZ109	35	0176
XZ109	36	0145
XZ301	1	0136
XZ301	2	0137
XZ301	3	0025
XZ301	4	0036
XZ301	5	0002
XZ301	6	0001
XZ301	7	0126
XZ301	8	0114
XZ301	9	0004
XZ301	10	0003
XZ301	11	0099
XZ301	12	0084
XZ301	13	0069
XZ301	14	0051
XZ301	15	0037
XZ301	16	0026
XZ301	17	0008
XZ301	18	0005
XZ301	19	0006
XZ301	20	0007
XZ301	21	0169
XZ301	22	0167
XZ301	23	0165
XZ301	24	0127
XZ301	25	0085
XZ301	26	0070
XZ301	27	0052
XZ301	29	0100
XZ301	30	0168
XZ301	31	0170
XZ301	32	0190
XZ301	33	0191
XZ301	34	0192
XZ301	35	0176
XZ301	36	0145
XZ303	1	0136
XZ303	2	0137
XZ303	15	0191
XZ303	20	0192
XZ303	30	0190
XZ303	31	0166
XZ303	32	0173

COMPONENT	PIN	NET
XZ303	33	0125
XZ303	34	0043
XZ303	35	0176
XZ303	36	0145
XZ304	1	0136
XZ304	2	0137
XZ304	3	0183
XZ304	4	0120
XZ304	5	0163
XZ304	6	0121
XZ304	7	0113
XZ304	8	0109
XZ304	9	0181
XZ304	10	0124
XZ304	11	0111
XZ304	12	0173
XZ304	13	0108
XZ304	14	0022
XZ304	15	0123
XZ304	16	0097
XZ304	17	0129
XZ304	18	0130
XZ304	19	0133
XZ304	20	0132
XZ304	21	0030
XZ304	22	0180
XZ304	23	0184
XZ304	24	0185
XZ304	25	0019
XZ304	26	0128
XZ304	27	0092
XZ304	28	0062
XZ304	29	0057
XZ304	30	0131
XZ304	31	0042
XZ304	32	0172
XZ304	34	0135
XZ304	35	0176
XZ304	36	0145
XZ305	1	0136
XZ305	2	0137
XZ305	3	0015
XZ305	4	0180
XZ305	5	0186
XZ305	6	0018
XZ305	8	0166
XZ305	9	0076
XZ305	14	0176
XZ305	15	0145
XZ405	22	0136
XZ405	23	0137
XZ405	24	0045
XZ405	25	0060



NETWORK LISTING (TABULAR WIRING DIAGRAM)

WDP

TITLE: ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805.7.9

WIRING DIAGRAM 8353WD	ISSUE 23	USED ON MODEL 37	DATE 05/01/69 6-3-69	PAGE 1 OF
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SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

NET	COMPONENT	PIN
0001	TB111	B 1
0001	TB111	A 1
0001	XZ102	18
0001	XZ101	18
0001	XZ301	6
0002	TB111	B 2
0002	TB111	A 2
0002	XZ102	19
0002	XZ101	19
0002	XZ301	5
0003	TB111	B 3
0003	TB111	A 3
0003	XZ102	20
0003	XZ101	20
0003	XZ301	10
0004	TB111	B 4
0004	TB111	A 4
0004	XZ102	21
0004	XZ101	21
0004	XZ301	9
0005	TB111	B 5
0005	TB111	A 5
0005	XZ102	25
0005	XZ101	25
0005	XZ301	18
0006	TB111	B 6
0006	TB111	A 6
0006	XZ102	26
0006	XZ101	26
0006	XZ301	19
0007	TB111	B 7
0007	TB111	A 7
0007	XZ102	27
0007	XZ101	27
0007	XZ301	20
0008	TB111	B 8
0008	TB111	A 8
0008	XZ102	28
0008	XZ101	28
0008	XZ301	17
0009	TB111	A 9
0009	TB111	B 9
0010	TB111	A10

NET	COMPONENT	PIN
0010	TB111	B10
0011	TB111	A11
0011	TB111	B11
0011	TB111	C11
0011	TB111	C12
0011	TB111	C13
0011	TB111	C14
0011	TB111	C15
0012	TB111	B12
0012	TB111	A12
0012	TB111	A13
0012	TB111	B13
0013	TB111	A14
0013	TB111	B14
0014	TB111	A15
0014	TB111	B15
0015	TB111	A17
0015	XZ305	3
0016	TB111	A18
0016	XZ107	B23
0017	TB111	A19
0017	XZ109	25
0018	TB111	B16
0018	XZ305	6
0019	TB111	B17
0019	XZ304	25
0020	TB111	B18
0020	XZ107	B22
0021	TB111	B19
0021	XZ109	17
0022	XZ104	11
0022	XZ103	B13
0022	XZ105	B 8
0022	TB111	C 1
0022	XZ304	14
0023	TB111	C 3
0023	XZ103	B19
0023	XZ105	B18
0024	TB111	C 4



NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805.7.9

WIRING DIAGRAM 8353WD	ISSUE 43	USED ON MODEL 37	DATE 05/01/69 6-3-69	PAGE 2 OF
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NET	COMPONENT	PIN
0024	XZ107	B 4
0025	TB111	C 6
0025	XZ301	3
0026	TB111	C 7
0026	XZ301	16
0027	TB111	C 8
0027	XZ109	32
0028	TB111	C 9
0028	XZ109	31
0029	TB111	C10
0029	XZ109	5
0030	TB111	C17
0030	XZ304	21
0031	TB111	C18
0031	XZ405	33
0032	TB111	C19
0032	XZ109	27
0033	TB111	D 1
0033	XZ103	B12
0034	TB111	D 3
0034	XZ103	B 4
0035	TB111	D 4
0035	XZ105	B27
0036	TB111	D 6
0036	XZ301	4
0037	TB111	D 7
0037	XZ301	15
0038	TB111	D 8
0038	XZ105	B30
0039	TB111	D 9
0039	XZ105	B29
0040	TB111	D10
0040	XZ105	B33
0041	TB111	D11
0041	XZ103	A27

NET	COMPONENT	PIN
0042	TB111	D12
0042	XZ304	31
0043	TB111	D13
0043	XZ303	34
0044	TB111	D14
0044	XZ109	7
0045	TB111	D15
0045	XZ405	24
0046	TB111	D18
0046	XZ405	28
0047	XZ103	A34
0047	TB111	D19
0047	XZ104	34
0048	TB111	E 1
0048	XZ103	B16
0048	XZ104	7
0049	TB111	E 3
0049	XZ103	B21
0050	TB111	E 4
0050	XZ107	B 7
0051	TB111	E 6
0051	XZ301	14
0052	TB111	E 7
0052	XZ301	27
0053	TB111	E 8
0053	XZ105	B21
0054	TB111	E 9
0054	XZ105	B11
0055	TB111	E10
0055	XZ105	B 7
0056	TB111	E11
0056	XZ109	20
0057	TB111	E12
0057	XZ304	29
0058	TB111	E13
0058	XZ103	A30



NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805.7.9			
WIRING DIAGRAM 8353WD	ISSUE 23	USED ON MODEL 37	DATE 05/01/69 6-3-69
		PAGE 3	OF

NET	COMPONENT	PIN
0059	TB111	E14
0059	XZ109	6
0060	TB111	E15
0060	XZ405	25
0061	TB111	E16
0061	XZ103	B28
0062	TB111	E17
0062	XZ304	28
0063	TB111	E18
0063	XZ405	32
0064	TB111	E19
0064	XZ103	A24
0065	TB111	E20
0065	XZ109	14
0065	XZ105	B24
0065	XZ104	8
0066	TB111	F 1
0066	XZ103	B17
0067	TB111	F 3
0067	XZ103	B20
0068	TB111	F 4
0068	XZ107	B 3
0069	TB111	F 6
0069	XZ301	13
0070	TB111	F 7
0070	XZ301	26
0071	TB111	F 8
0071	XZ105	B15
0072	TB111	F 9
0072	XZ105	B10
0073	TB111	F10
0073	XZ105	B 9
0074	TB111	F11
0074	XZ109	24
0075	TB111	F13
0075	XZ109	18

NET	COMPONENT	PIN
0076	TB111	F14
0076	XZ305	9
0077	TB111	F15
0077	XZ109	19
0078	TB111	F16
0078	XZ107	B34
0079	TB111	F18
0079	XZ405	34
0080	TB111	F19
0080	XZ103	A22
0081	TB111	F20
0081	XZ107	B21
0082	TB111	G 1
0082	XZ103	B15
0083	TB111	G 3
0083	XZ103	B18
0084	TB111	G 6
0084	XZ301	12
0085	TB111	G 7
0085	XZ301	25
0085	XZ103	B 8
0086	TB111	G 8
0086	XZ105	B32
0087	TB111	G 9
0087	XZ105	A31
0088	TB111	G10
0088	XZ105	A29
0089	TB111	G11
0089	XZ104	9
0090	TB111	G12
0090	XZ109	26
0091	TB111	G13
0091	XZ107	B18
0092	TB111	G14
0092	XZ304	27
0093	TB111	G15



NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805.7.9

WIRING DIAGRAM 8353WD	ISSUE 23	USED ON MODEL 37	DATE 05/01/69 6-3-69	PAGE 4 OF
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NET	COMPONENT	PIN
0093	XZ109	23
0094	TB111	G16
0094	XZ107	B26
0095	TB111	G19
0095	XZ103	A28
0096	TB111	G20
0096	XZ107	B20
0097	TB111	H 1
0097	XZ304	16
0098	TB111	H 3
0098	XZ103	A29
0099	TB111	H 6
0099	XZ301	11
0100	TB111	H 7
0100	XZ301	29
0101	TB111	H 8
0101	XZ105	B13
0102	TB111	H10
0102	XZ109	8
0103	TB111	H11
0103	XZ104	18
0104	TB111	H12
0104	XZ109	34
0105	TB111	H13
0105	XZ107	B25
0106	TB111	H14
0106	XZ104	22
0107	TB111	H15
0107	XZ109	13
0108	TB111	H16
0108	XZ304	13
0109	TB111	H17
0109	XZ304	8
0110	TB111	H19
0110	XZ104	12

NET	COMPONENT	PIN
0111	TB111	J 1
0111	XZ304	11
0112	TB111	J 3
0112	XZ102	4
0113	TB111	J 4
0113	XZ109	22
0113	XZ107	B33
0113	XZ105	B12
0113	. XZ304	7
0113	. XZ405	26
0113	XZ103	A31
0114	TB111	J 6
0114	XZ301	8
0115	TB111	J 8
0115	XZ105	B14
0116	TB111	J10
0116	XZ109	11
0117	TB111	J11
0117	XZ104	15
0118	TB111	J12
0118	XZ109	33
0119	TB111	J14
0119	XZ104	20
0120	TB111	J16
0120	XZ304	4
0121	TB111	J17
0121	XZ304	6
0122	TB111	J20
0122	XZ109	15
0123	TB111	K 1
0123	XZ304	15
0124	TB111	K 2
0124	XZ105	B 6
0124	. XZ304	10
0124	XZ103	B14
0124	XZ104	4
0125	TB111	K 4
0125	XZ303	33



NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805.7.9

WIRING DIAGRAM 8353WD	ISSUE 23	USED ON MODEL 37	DATE 05/01/69 6-3-69	PAGE 5 OF
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NET	COMPONENT	PIN
0126	TB111	K 6
0126	XZ301	7
0127	TB111	K 7
0127	XZ301	24
0128	TB111	K 8
0128	XZ304	26
0129	TB111	K 9
0129	XZ304	17
0130	TB111	K10
0130	XZ304	18
0131	TB111	K11
0131	XZ304	30
0132	TB111	K12
0132	XZ304	20
0133	TB111	K13
0133	XZ304	19
0134	TB111	K14
0134	XZ104	21
0135	TB111	K15
0135	XZ304	34
0136	XZ109	1
0136	XZ107	B 1
0136	XZ105	B 1
0136	XZ104	1
0136	XZ103	B 1
0136	XZ102	1
0136	XZ101	1
0136	XZ301	1
0136	XZ303	1
0136	XZ304	1
0136	XZ305	1
0136	XZ405	22
0137	XZ109	2
0137	XZ107	B 2
0137	XZ105	B 2
0137	XZ104	2
0137	XZ103	B 2
0137	XZ102	2
0137	XZ101	2
0137	XZ301	2
0137	XZ303	2
0137	XZ304	2

NET	COMPONENT	PIN
0137	XZ305	2
0137	XZ405	23
0138	XZ101	5
0138	XZ103	B24
0139	XZ101	7
0139	XZ105	B26
0140	XZ101	9
0140	XZ103	B26
0141	XZ101	10
0141	XZ103	B23
0142	XZ101	11
0142	XZ105	B17
0143	XZ103	A32
0143	XZ101	12
0143	XZ107	B13
0144	XZ101	35
0144	XZ105	B 4
0145	XZ101	36
0145	XZ102	36
0145	XZ103	B36
0145	• XZ301	36
0145	• XZ303	36
0145	• XZ304	36
0145	• XZ405	36
0145	• XZ305	15
0145	XZ104	36
0145	XZ105	B36
0145	XZ107	B36
0145	XZ109	36
0146	XZ102	5
0146	XZ103	B25
0147	XZ102	6
0147	XZ104	17
0148	XZ102	7
0148	XZ105	B19
0149	XZ103	B34
0149	XZ102	9
0149	XZ104	6
0150	XZ102	10
0150	XZ103	A23

99130-2



NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE ACTUAL WIRING DIAGRAM FOR ELECTRICAL SERVICE UNITS YESU805,7,9				
WIRING DIAGRAM 8353WD	ISSUE J 13	USED ON MODEL 37	DATE 05/01/69 6-3-69	PAGE 6 OF

NET	COMPONENT	PIN
0151	XZ102	11
0151	XZ105	B16
0151	XZ107	B29
0152	XZ103	B32
0152	XZ102	12
0152	• XZ109	10
0152	XZ107	B27
0153	XZ102	13
0153	XZ104	32
0154	XZ102	15
0154	XZ104	33
0155	XZ102	17
0155	XZ104	28
0156	XZ102	22
0156	XZ104	26
0157	XZ102	23
0157	XZ104	27
0158	XZ102	24
0158	XZ104	29
0159	XZ102	30
0159	XZ104	30
0160	XZ102	31
0160	XZ104	31
0161	XZ102	35
0161	XZ105	B 3
0162	XZ103	A21
0162	XZ109	4
0163	XZ103	A25
0163	XZ304	5
0164	XZ103	A26
0164	XZ109	16
0165	XZ103	B 3
0165	XZ301	23
0166	XZ303	31
0166	XZ103	B 5
0166	XZ105	B28
0166	XZ305	8

NET	COMPONENT	PIN
0167	XZ103	B 6
0167	XZ301	22
0168	XZ103	B 7
0168	XZ301	30
0169	XZ103	B 9
0169	XZ301	21
0170	XZ103	B10
0170	XZ301	31
0171	XZ103	B22
0171	XZ107	B12
0172	XZ107	B31
0172	XZ105	B23
0172	XZ103	B27
0172	XZ304	32
0173	XZ109	12
0173	XZ107	B14
0173	XZ105	B22
0173	• XZ304	12
0173	• XZ405	30
0173	XZ103	B29
0173	XZ303	32
0174	XZ104	25
0174	XZ103	B30
0174	XZ109	21
0175	XZ103	B31
0175	XZ109	28
0176	XZ109	35
0176	XZ105	B35
0176	XZ104	35
0176	XZ103	B35
0176	XZ301	35
0176	XZ303	35
0176	XZ304	35
0176	XZ405	35
0176	XZ305	14
0177	XZ104	13
0177	XZ109	3
0178	XZ105	A18
0178	XZ107	B24
0179	XZ105	B 5

8358 WD

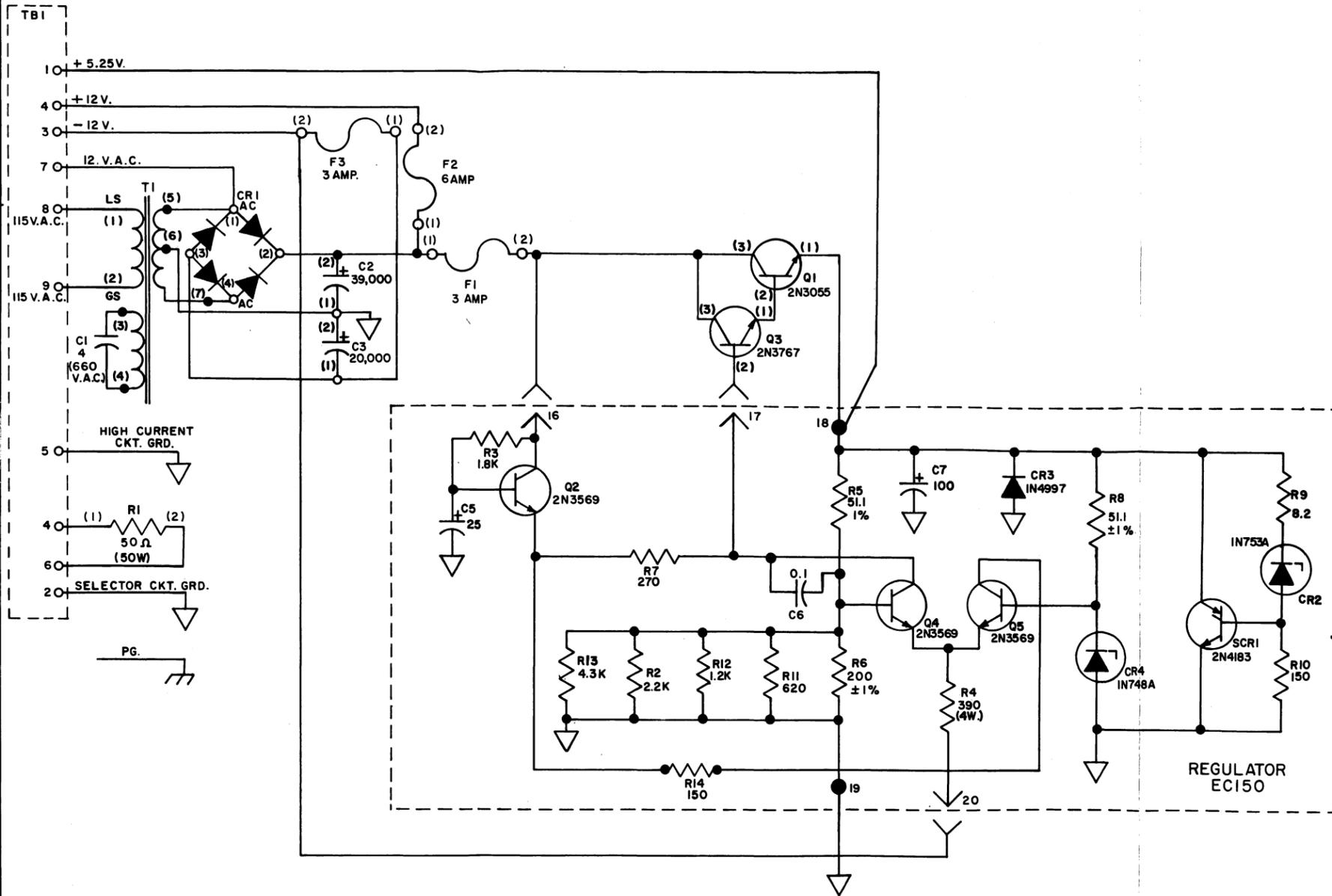
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REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-11-68	19371-R
2	6-28-68	95937
3	8-29-68	95998

- NO. NOTES
- REFER TO 8359WD FOR ACTUAL WIRING DIAGRAM.
 - REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY
 - ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
 - ALL RESISTORS 1/2 WATT AND RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED.
 - ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
 - ⊘ INDICATES FEMALE TERMINAL AND
→ INDICATES MALE TERMINAL
 - TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESIS ARE FOR REFERENCE ONLY AND ARE NOT MARKED ON COMPONENTS.
 - RESISTANCE VALUES OF TRANSFORMER WINDINGS:

BETWEEN TERMINALS	RESISTANCE
1 & 2	1.19 OHMS
3 & 4	5.5 OHMS
5 & 6	.022 OHMS
6 & 7	.022 OHMS



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SCHEMATIC WIRING DIAGRAM FOR POWER SUPPLY (327803)

APPROVALS

D AND R	E OF M
<i>MJR</i>	<i>[Signature]</i>

E-NUMBER

PROD. NO. 8358 WD

DATE 2-9-68

P.D. FILE NO. G-A384AA

DRAWN WPB CHKD *[Signature]*

ENG. MJR APPD. *[Signature]*

TELETYPE CORPORATION

8358 WD

CIRCUIT DESCRIPTION OF THE POWER SUPPLY AND REGULATOR
(ASSEMBLY NUMBER 327803)

TABLE OF CONTENTS

<u>SECTION</u>	<u>DESCRIPTION</u>	<u>TOTAL PAGES IN SECTION</u>
I	General Technical Information	3
II	Detailed Description and Theory of Operation	4

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE POWER SUPPLY AND REGULATOR
(ASSEMBLY NUMBER 327803)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 327803 multi-voltage power supply converts A.C. power to D.C. power appropriate for the operation of integrated circuits, discrete semi-conductor circuits, solenoids, and other devices.

1.2 The design of this unit provides economically and reliably the properties herein specified.

1.3 This unit is classified as basic equipment for the Teletype Model 37 KSR and ASR sets, is factory assembled, and is not construed as accessory equipment. No accessory mechanisms or parts are required after final production assembly.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

2.1.1 Primary Power

Primary power must be supplied by a 117 volt $\pm 10\%$, 60 $\pm 1\%$ Hz source capable of supplying approximately 270 volt amps. of power.

2.2 Output Characteristics

2.2.1 Nominal +12.5 Volt Output

The nominal +12.5 volt output exhibits a low output impedance due to ferro-resonant transformer action. The maximum worst case ripple voltage is approximately one volt peak to peak with all windings fully loaded and the worst case combination of line voltage and line frequency. This output does not exceed +13.75 volts ($I_L = 0.5$ amps., $I_L = 3$ amps.) with respect to ground, with the worst case combination of line voltage and line frequency and does not fall below +11.65 volts, all windings fully loaded with the worst possible combination of line voltage and line frequency. This output is capable of supplying 7.0 amps. at voltages within the limits specified at temperatures ranging from 0°C to +70°C.

2.2.2 Nominal - 12.5 Volt Output

The nominal -12.5 volt output exhibits a low output impedance due to ferro-resonant transformer action. The maximum worst case ripple voltage is approximately 800 millivolts peak to peak with all windings loaded and the

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worst case combination of line voltage and line frequency. This output does not exceed -13.88 volts with respect to ground ($I_L = 3.0$ amps., $I_L = 0.75$ amps.) with the worst case combination of line voltage and line frequency and does not become more positive than -11.13 volts, all windings fully loaded and the worst case combination of line voltage and line frequency. This output is capable of supplying 3.0 amps. at voltages within the limits specified at temperatures ranging from 0°C to 70°C.

2.2.3 Nominal +5.25 Volt Output

The nominal +5.25 volt output has an output impedance of approximately 12 milliohms. The maximum worst-case ripple voltage is approximately 15 millivolts at full load. This output is capable of being adjusted to within $\pm 1\%$ of the nominal value by means of a resistor clipping scheme. At elevated temperature (70°C) the output voltage must be equal to or greater than +5.0 volts ($I_L = 3.0$ amps.). The maximum current capability of this output is 3.0 amps.

2.3 Additional Features

2.3.1 An additional high current ground is provided for electrical noise producing circuits to reduce coupling into integrated circuitry.

2.3.2 A 12 volt AC output is available (wave form approximates a square wave).

2.4 Temperature Range

The power supply will operate continuously fully loaded in ambient temperatures ranging from 0°C to 70°C. Non-operating storage temperatures range from -40°C to +70°C.

2.5 Mounting, Marking, and Finishing Requirements

2.5.1 The power supply base is constructed of steel. All aluminum parts are anodized.

2.5.2 The power supply unit is appropriately mounted in a steel frame which houses the electrical service unit.

2.5.3 Circuit identification symbols are stamped on the base plate or mounting bracket adjacent to the designated apparatus.

2.5.4 All areas exceeding 160°F are stamped "HOT". The maximum temperatures are based on the worst-case conditions resulting from operation with line voltage $\pm 10\%$ of nominal, line frequency $\pm 1\%$ of nominal, and an ambient temperature of 110°F.

2.5.5 All areas containing high voltage terminals are stamped "DANGER, HIGH VOLTAGE".

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OUTPUT VOLTAGE	MAXIMUM AVERAGE LOAD CURRENT	*OVERALL LOAD/LINE REGULATION	RIPPLE (MAX.)
+12.5V (Nom.) @I ₋ = 3A	7.0 Amps	+10%, -7% (0.5A to 3A) ± 7% (3A to 10A)	1 Volt (p-p)
-12.5V (Nom.) @I ₊ = 3A	3.0 Amps	± 5% (0.75A to 3A)	800 mv. (p-p)
5.25V ± 1% RL = 4Ω	3.0 Amps	± 5% (0A to 3A)	15 mv. (p-p)

- * - Overall load/line regulation defines the maximum deviation from the specified nominal output voltage due to the worst case combinations of primary frequency, primary voltage, load current, ** winding interaction, and temperature.
- # - Winding interaction is defined as the variation of one voltage due to a load change on any other from no load to full load.

Temperature Range - 0°C - 70°C
 Frequency Range - 60 ± 1% HZ
 Line Voltage Range - 117V_{AC} ± 10%

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SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Regulator card assembly drawing and power supply schematic, 303150 (EC150) and 8358 WD, respectively.

2. DETAILED DESCRIPTION

2.1 A ferro-resonant transformer T_1 , steps down primary voltage. The secondary center-tap is grounded so that full-wave rectification can be obtained and secondary waveform is rectangular (due to transformer saturation). A rectifier bridge assembly, CR_1 , rectifies the secondary waveform and capacitors C_2 and C_3 provide the required filtering action.

The nominal ± 12.5 volt DC outputs obtain their regulations from T_1 . These outputs provide power for the regulator, solenoids, and lamp driver amplifiers. The + 12.5 volt DC output is fused at 7.0 amps by f_1 and the - 12.5 volt DC output is fused at 3.0 amps.

2.2 The + 5.25 volt output is regulated by a series-type negative feedback regulator. A regulator of this type can be broken down into a functional block diagram which describes the circuit. (See Section II-3)

The comparing element detects an error signal due to input and/or load variations, compares this signal to a fixed reference voltage, amplifies this signal, and in proper phase supplies a correction signal to the series control element. The series control element adjusts its voltage drop to compensate for output voltage variations. The pre-regulator supplies proper bias current for the control and comparing elements and decreases the per cent regulation.

3. THEORY OF OPERATION

3.1 A differential pair of transistors, Q_4 and Q_5 , function together as a comparing element. A darlington pair of transistors, Q_1 and Q_3 function as a composite series pass element. Transistor Q_2 acts as a constant current source which provides base drive for Q_3 , collector current for Q_4 , and collector current for Q_5 . The output voltage is adjustable by properly clipping the resistors shunting R_6 . (See Section II-3)

Upon application of power, the regulator is held off until C_5 charges adequately to turn on Q_2 . With Q_2 on, adequate Q_3 base current allows the output voltage to stabilize. The base of Q_5 is referenced to CR_1 . Because of differential amplifier operation, V_{R_6} approximately equals V_{CR_4} . If the output voltage tends to increase, a portion of this output voltage change ($B V_o$) appears across R_6 . As a result, Q_4 collector current increases and the overall base drive of the composite pass element decreases, causing an increase of Q_1 collector-emitter voltage. Conversely, decreases in output voltage tend to decrease Q_4

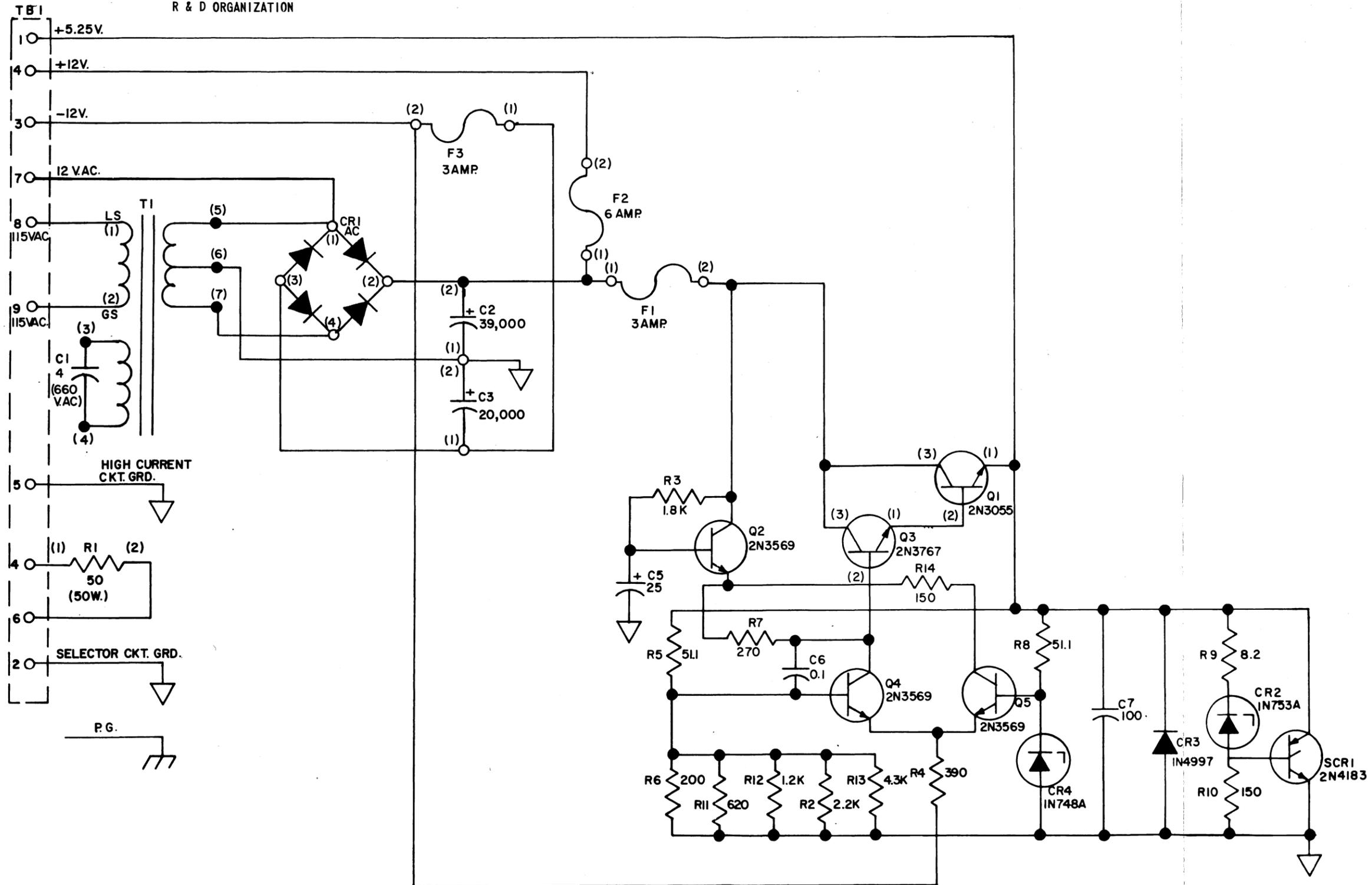
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collector current and increase the overall base drive current to the composite pass-element, causing a decrease of Q1 collector-emitter voltage. The push-pull operation of Q4 and Q5 tends to keep the emitter current of Q2 relatively constant. C6 stabilizes the comparing amplifiers and prevents high frequency oscillation. The resistor clipping network R11 through R13, effectively changes the base drive current of Q4. This action changes the collector current and the overall base drive to the series pass element. The clipping scheme sets the collector-emitter voltage of Q1 so that the output voltage is within the desired range.

All integrated circuitry is protected from over-voltage by a crowbar trigger circuit.

Application of negative voltages to logic circuitry is prevented by CR3. If the regulated output decreases to approximately -0.7V with respect to ground, CR3 will be forward biased. As a result, f1 and f3 blow.

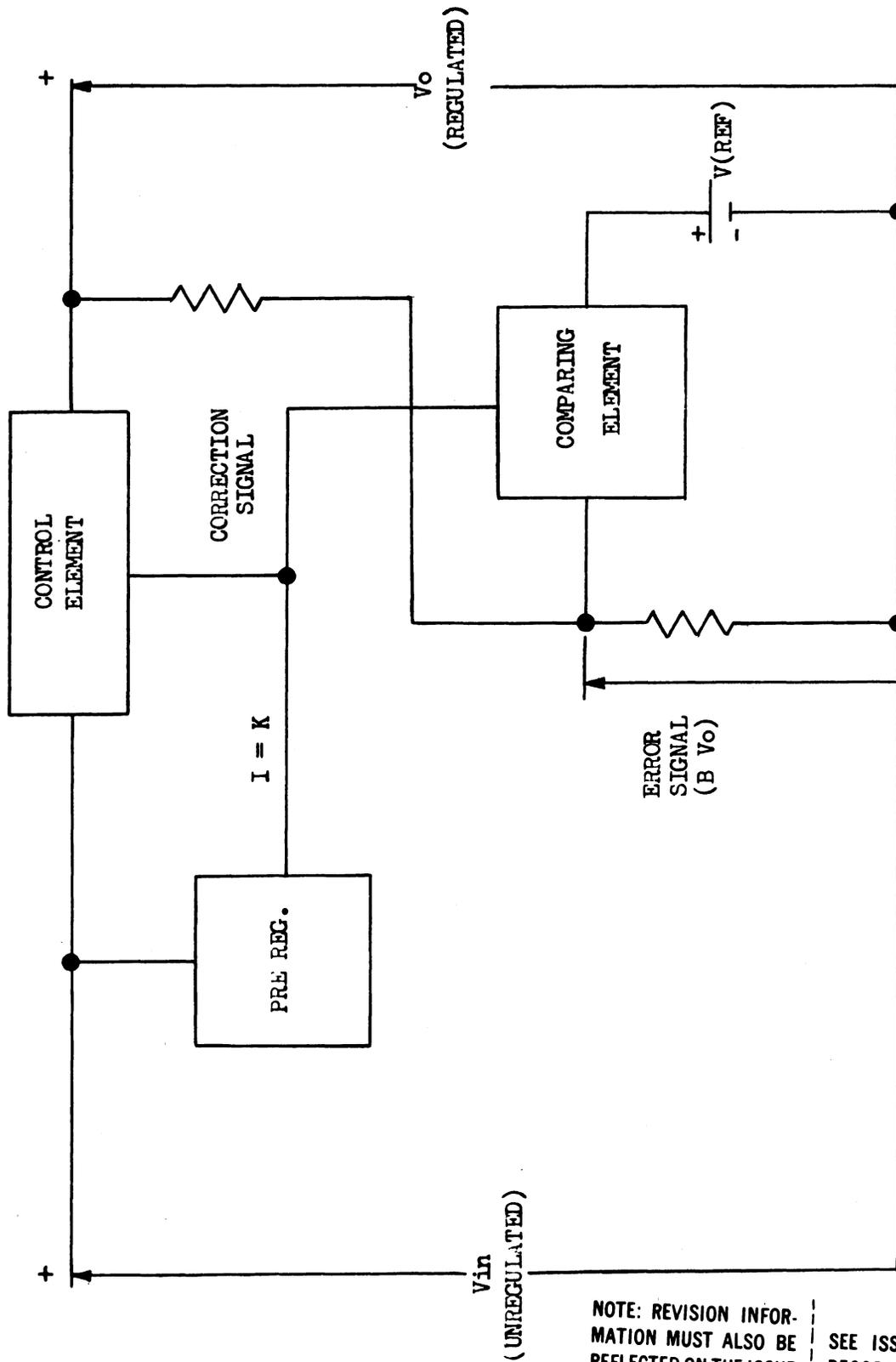
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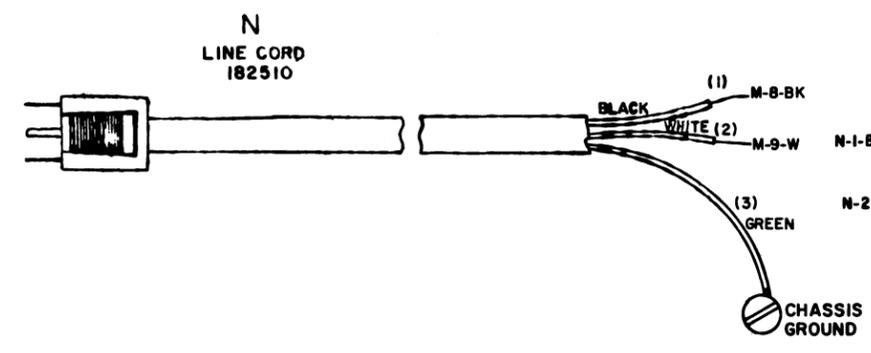
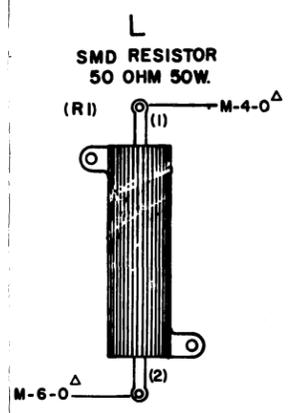
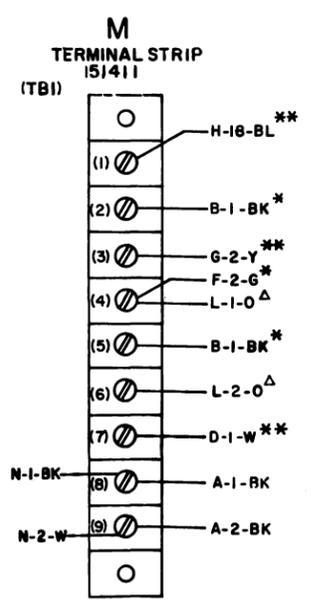
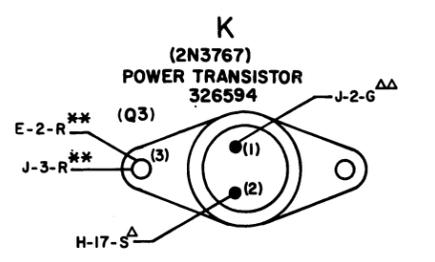
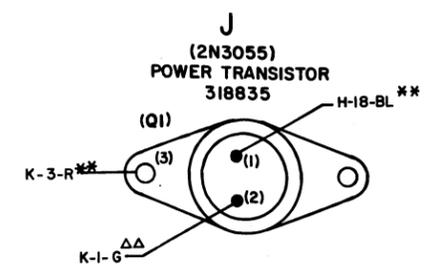
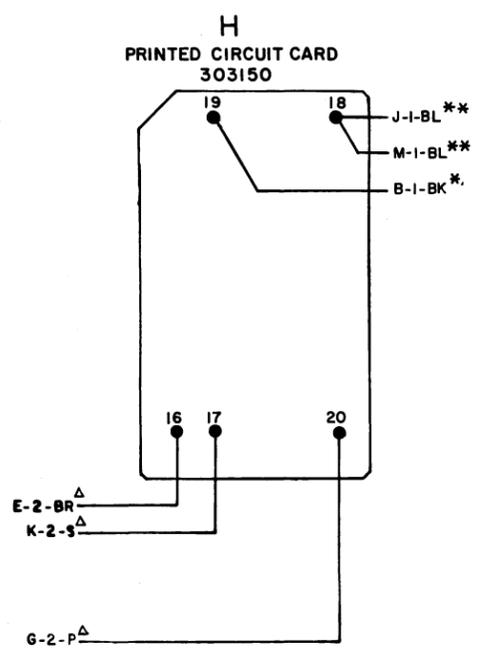
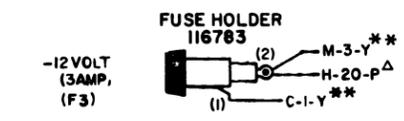
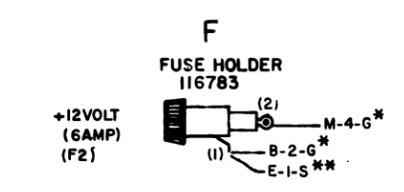
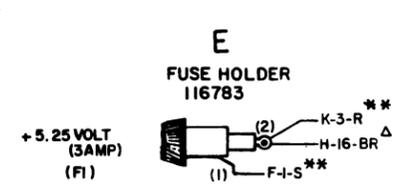
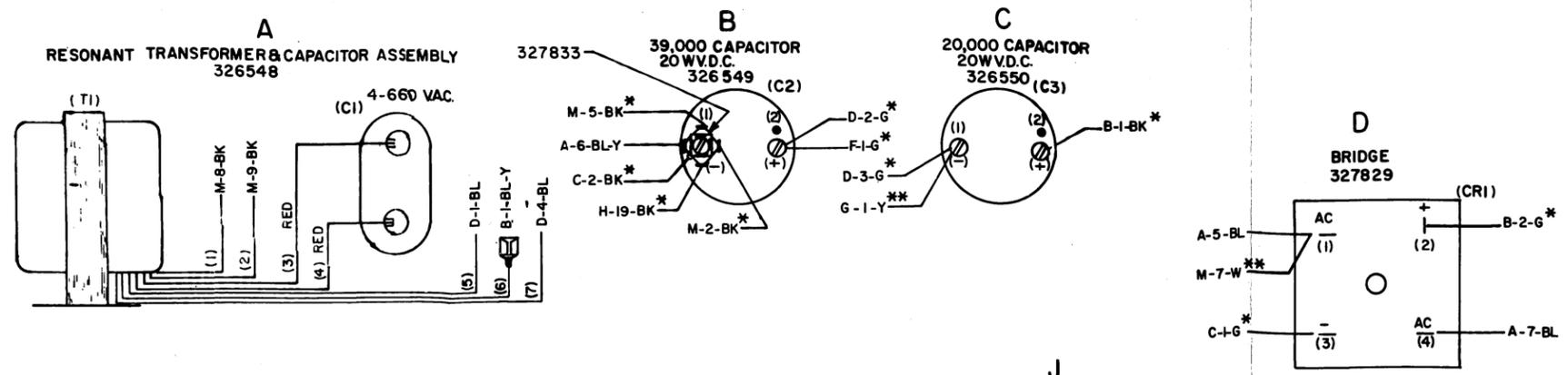
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8359 WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-11-68	19371-R
2	8-29-68	95998

- NO. NOTES
1. WIRING LEGEND:
K-B-W
WIRE COLOR CODE
DISTANT TERMINATING DESIGNATION
DISTANT TERMINATING AREA.
 2. TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY AND ARE NOT MARKED ON COMPONENT.
 3. COLOR CODE LEGEND:
BK-BLACK G-GREEN
BR-BROWN BL-BLUE
R-RED P-PURPLE
S-SLATE O-ORANGE
Y-YELLOW W-WHITE
 4. ASSOCIATED SCHEMATIC 8358 WD.
 5. WIRE GAGE:
* DENOTES 14AWG.
** DENOTES 18AWG.
Δ DENOTES 20AWG.
ΔΔ DENOTES 22AWG.
 6. ASSOCIATED CABLE 326557
 7. ALL RESISTORS 1/2 WATT AND RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED.
 8. ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.



ACTUAL WIRING DIAGRAM FOR POWER SUPPLY (327803)

APPROVALS

D AND R <i>ASX</i>	E OF M <i>C</i>
-----------------------	--------------------

E-NUMBER

PROD. NO. 8359 WD.

DATE 3-12-68

P.D. FILE NO. G-A354AA

DRAWN W.R.B. CHKD. *JS*

ENGD. M.J.R. APPD.

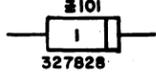
TELETYPE CORPORATION

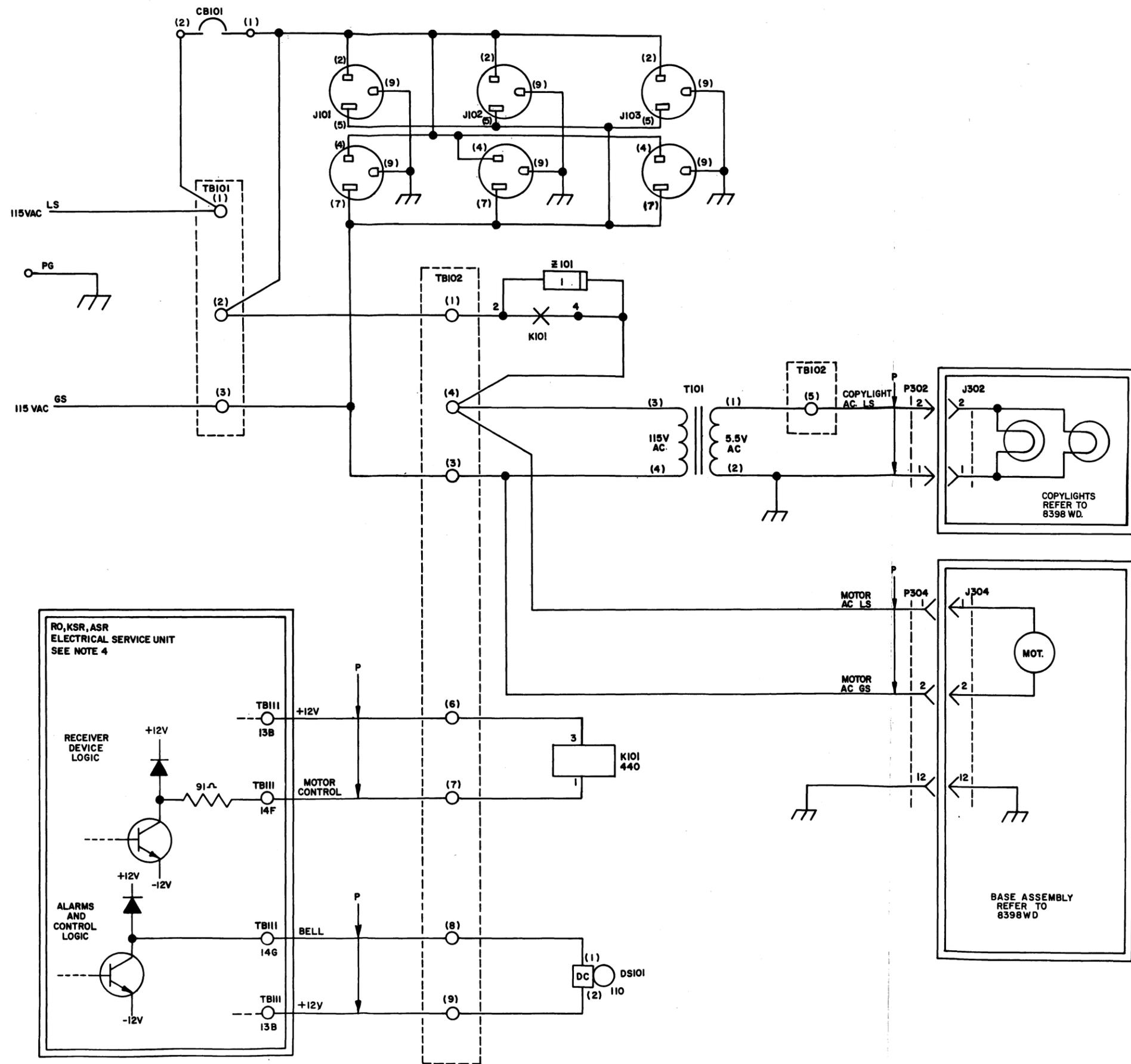
8359 WD

8360WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-27-68	19260-R
2	5-29-69	99312-1

- NO. NOTES**
- ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
 - TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESIS ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
 - THE RESISTANCE OF ALL RELAY COILS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
 - COMPONENTS ENCLOSED IN SOLID DOUBLE LINES ARE PRESENTED FOR REFERENCE ONLY.
 -  INDICATES FEMALE TERMINAL AND
 INDICATES MALE TERMINAL
 - NETWORK:**
 Z101
 327828
 120 0.32
 - REFERENCE ACTUAL WIRING DIAGRAM: 8361WD.
 - REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY.
 -  INDICATES TWISTED PAIR OF WIRES WHICH ARE PART OF ELECTRICAL SERVICE UNIT INTERFACE CABLE.



SCHEMATIC WIRING DIAGRAM FOR UTILITY STRIP 326593

APPROVALS

D AND R <i>AJK</i>	E OF M <i>[Signature]</i>
-----------------------	------------------------------

E-NUMBER
PROD. NO. 8360WD

DATE 2-27-68
P.D. FILE NO. G-A354AA

DRAWN RJP	CHKD. <i>[Signature]</i>
ENG. MJR	APPD. <i>[Signature]</i>

TELETYPE CORPORATION

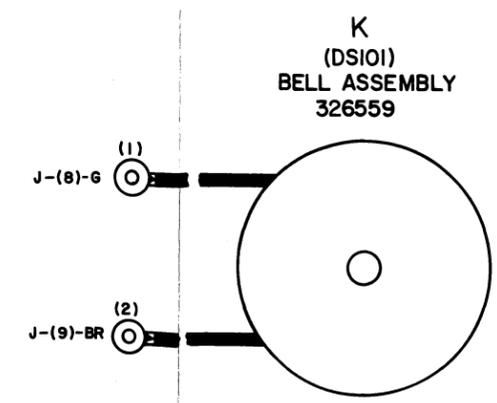
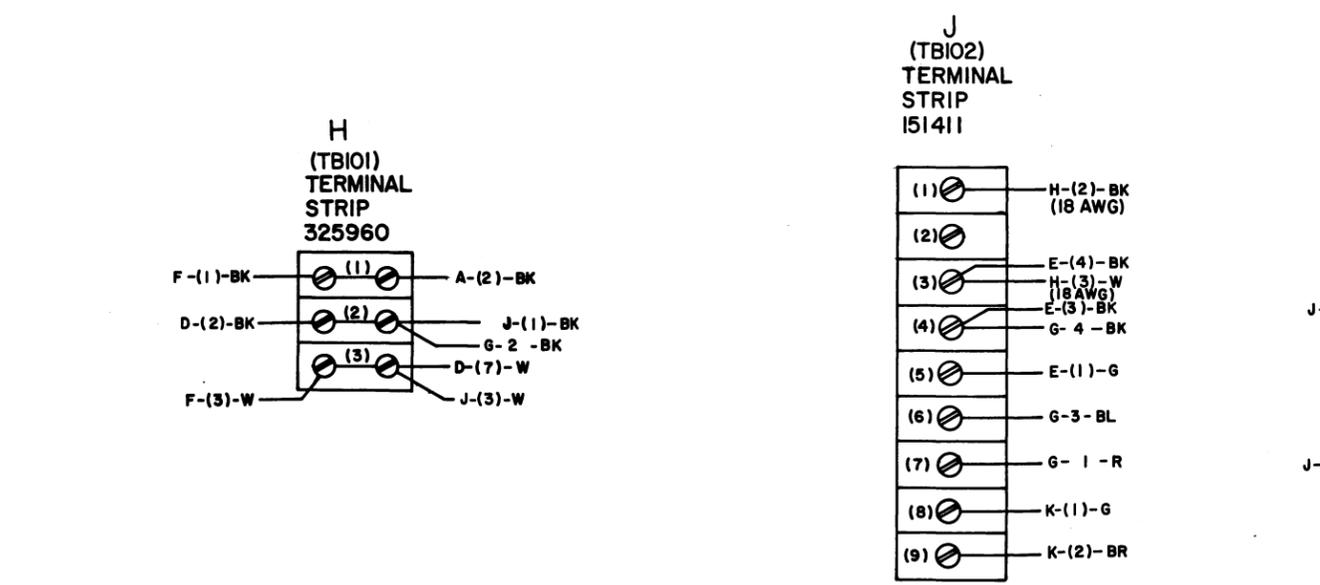
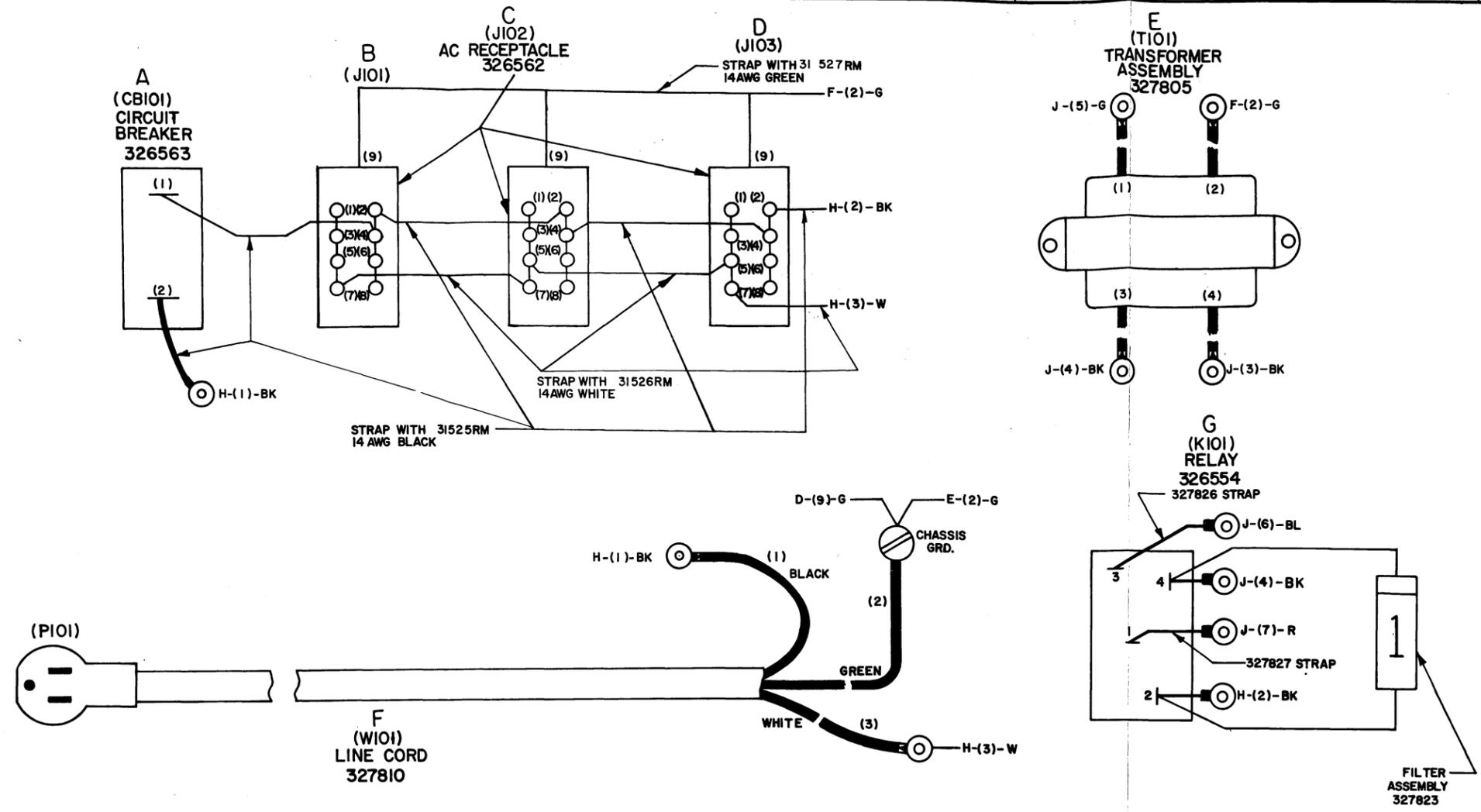
8360WD

8361WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-27-68	19260-R
2	3-6-69	96510

- NO. NOTES.
1. WIRING LEGEND:
 K-(9)-W
 WIRE COLOR CODE
 DISTANT TERMINATING DESIGNATION.
 DISTANT TERMINATING AREA.
 2. TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY AND NOT MARKED ON COMPONENT.
 3. CIRCUIT BREAKER, CB101, A.C. RECEPTACLES, J101, 2, AND RELAY, K101, ARE VIEWED FROM TERMINAL END.
 4. COLOR CODE:
 BK-BLACK G-GREEN
 BR-BROWN BL-BLUE
 R-RED P-PURPLE
 O-ORANGE S-SLATE
 Y-YELLOW W-WHITE
 5. ASSOCIATED SCHEMATIC: 8360WD.



ACTUAL WIRING DIAGRAM FOR UTILITY STRIP

APPROVALS

D AND R	E OF M
<i>HJR</i>	<i>CT</i>

E-NUMBER

PROD. NO. 8361WD.

DATE 1-8-68

P.D. FILE NO. G-A354AA

DRAWN RJP CHKD.

ENGD. MJR APPD.

TELETYPE CORPORATION

8361WD

8365WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-30-68	19568-R
2	1-15-69	96482
3	2-24-69	96867
4	5-15-69	99159

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

1. COLOR CODE:
BK-BLACK R-RED
BR-BROWN S-SLATE
BL-BLUE P-PURPLE
G-GREEN Y-YELLOW
O-ORANGE W-WHITE
2. N.O. - NORMALLY OPEN
N.C. - NORMALLY CLOSED
L - LAMP
3. ASSOCIATED CABLE ASSEMBLIES: 326571 & 327807.
4. IN ARRANGEMENTS THAT USE 3 CABLES. A 327807 CABLE ASSEMBLY MUST BE ORDERED SEPARATELY.
5. IN ARRANGEMENTS WHERE 2 CABLES ARE SUPPLIED, BUT ONLY ONE SWITCH IS USED. SPARE CABLE TO BE TIED BACK INTO CABINET.
6. POWER CONNECTIONS FOR 327807 CABLES:
- | CABLE | WIRE COLOR | WIRING FIELD TERMINAL NO. |
|-------|------------|---------------------------|
| A | BK | C12 |
| | G | A12 |
| B | BK | C13 |
| | G | A12 |
| C | BK | C14 |
| | G | A13 |
7. PROGRAMMING:
1. THE STANDARD ARRANGEMENTS ARE AS FOLLOWS.
- | TELETYPEWRITER SET | ARRANGEMENT |
|--------------------|-------------|
| RO | 2 |
| KSR | 5 |
| ASR | 10 |
2. TO CHANGE ARRANGEMENTS
1. DETERMINE FUNCTION REQUIRED
A. USING SHEETS 2,3,4,5 FIND LOCATION OF FUNCTION ON WIRING FIELD.
B. ASSIGN POSITION TO FUNCTION SELECTED ON CONTROL PANEL.
C. FROM SHEETS 2,3,4, DETERMINE COLOR CODE OF WIRES PER SELECTION IN B.
D. CONNECT WIRES TO TERMINAL BOARD TBIII, IN ACCORDANCE WITH DATA OF A.
8. SEE SHEET 6 FOR R-T CONTROL PANEL ARRANGEMENTS. ARRANGEMENT NO. 1 IS THE STANDARD R-T ARRANGEMENT. TO CHANGE R-T ARRANGEMENTS FOLLOW THE PROCEDURE OUTLINED IN NOTE 7 SECTION 2, USING SHEET 6 FOR WIRING INFORMATION.
9. ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
10. POWER CONNECTIONS FOR 326571 CABLE:
- | WIRE COLOR | WIRING FIELD TERMINAL NO. |
|------------|---------------------------|
| G | B12 |
| G-BR | B14 |
| G-BL | B14 |
| BK | C10 |
11. * TWO LETTER SUFFIX DENOTES ELECTRICAL SERVICE UNIT VARIATION.
12. ASSOCIATED (327807) CABLE ASSEMBLIES TO BE LABELLED NEAR CONNECTOR AS FOLLOWS:
- | CABLE LOCATION | PART NO. |
|----------------|----------|
| A | 79267 RM |
| B | 79268 RM |
| C | 79269 RM |
13. WHEREVER TWO TERMINATIONS ARE INDICATED IN ONE SQUARE, CONNECT THEM WITH STRAP 327842. ATTACH THE CONTROL PANEL WIRE TO THE UPPER TERMINATION.
14. KEY TO CORNER SHADING:
 ASSEMBLE THE CONTROL PANEL LENS WITH A 330545 RED TAB.
 ASSEMBLE THE CONTROL PANEL LENS WITH A 330547 GREEN TAB.

FIGURE 1
326566
WIRING FIELD
(TBIII RO, KSR, ASR)
(TBII2 R-T)

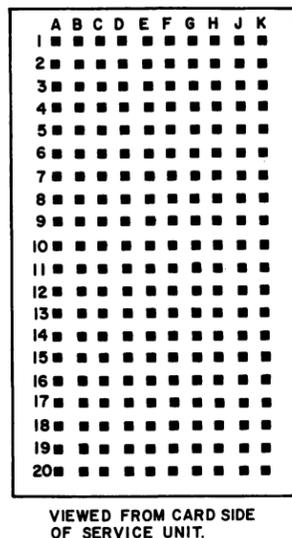


FIGURE 2
327807
CABLE ASSEMBLY

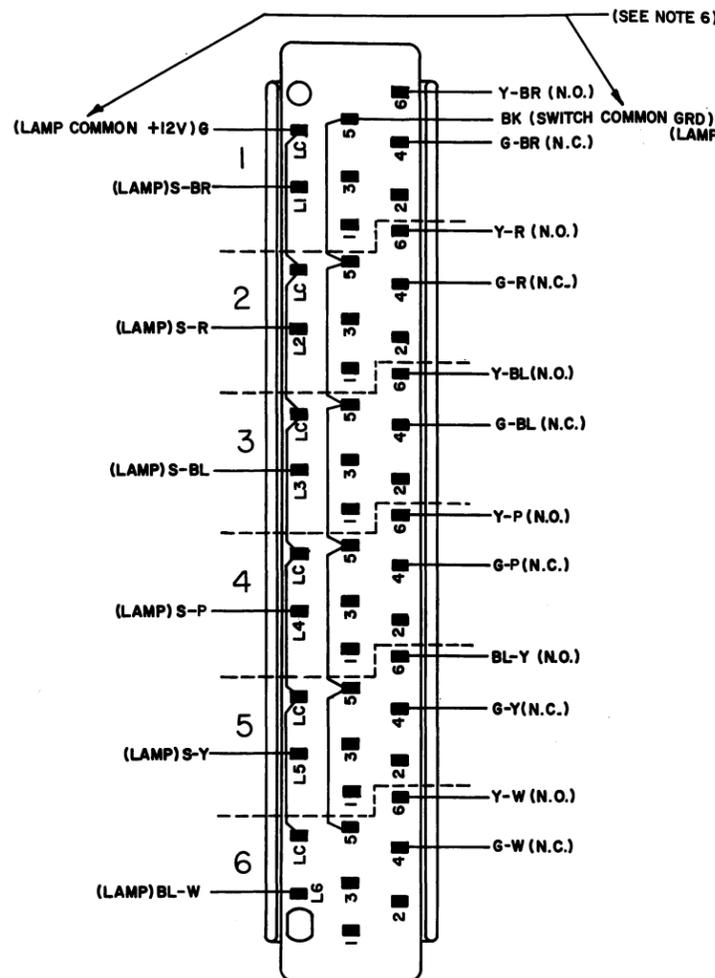


FIGURE 3
326571
CABLE ASSEMBLY
(R-T ONLY)

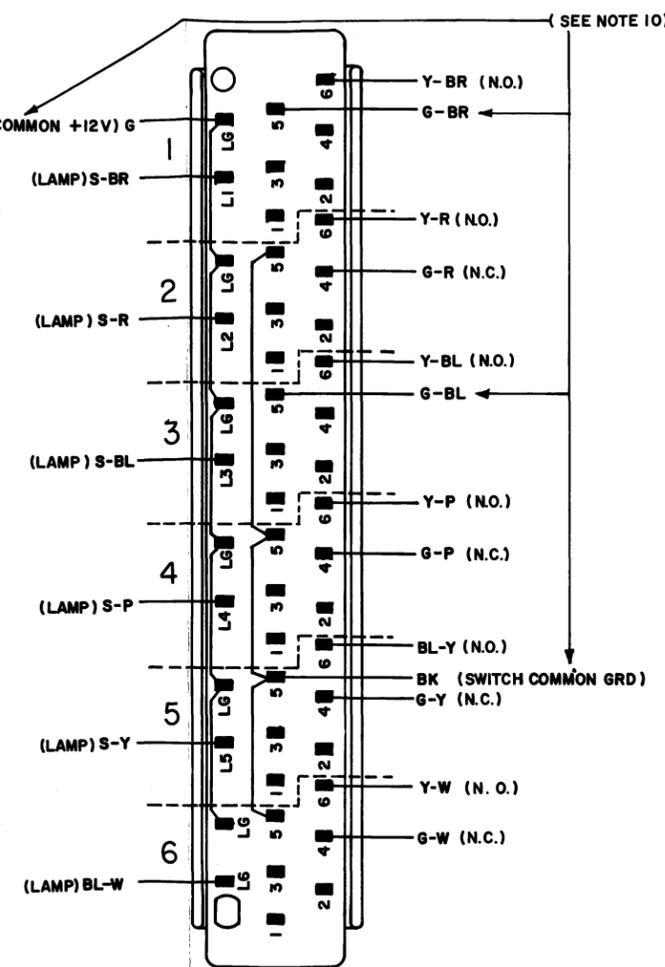


FIGURE 4
(VIEWED FROM FRONT OF UNIT)

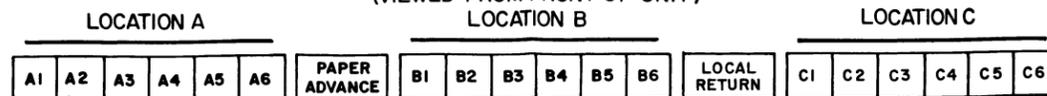
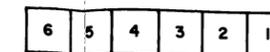


FIGURE 5
(VIEWED FROM TOP OF R-T)



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

ANALYSIS CHART FOR MODEL 37 CONTROL PANEL ARRANGEMENTS

APPROVALS

D AND R *RJK* E OF M *[Signature]*

E-NUMBER

PROD. NO. 8365WD

DATE 4-18-68

R.D. FILE NO. G-A354AA

DRAWN RJP CHKD. *[Signature]*
ENGD. M JR APPD. *[Signature]*

TELETYPE CORPORATION

8365WD

SEE SHEET 1 FOR NOTES.

WIRING FIELD CONNECTIONS FOR YESU 809
(SEE FIGURES 1&2)

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

8365WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-30-68	19568-R
2	2-24-69	96867
3	5-15-69	99159
4	6-19-69	99306

CABLE LOCATION
POSITION NO.
FUNCTION (SEE NOTE 2)
WIRE COLOR
WIRING ARRANGEMENT
APPROPRIATE MARKINGS NO.
(SEE SHEET 5)

NOTE 12

REMARKS:

A						B						C						
A1	A2	A3	A4	A5	A6	B1	B2	B3	B4	B5	B6	C1	C2	C3	C4	C5	C6	
N.C.	N.C.	L	N.O.	N.C.	L	N.O.	N.C.	L	N.O.	N.C.	L	N.O.	N.C.	L	N.O.	N.C.	L	
Y-BR	G-BR	S-BR	Y-R	G-R	S-R	Y-BL	G-BL	S-BL	Y-P	G-P	S-P	BL-W	Y-BR	G-BR	S-BR	Y-R	G-R	S-R

1	AA
2	AB
12	AC
13	AD

SEE NOTE 13

SEE NOTE 13

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.
SHEET 4

ANALYSIS CHART FOR MODEL 37 CONTROL PANEL ARRANGEMENTS

APPROVALS

D AND R	E OF M
---------	--------

E-NUMBER

PROD. NO. 8365WD

DATE 4/18/68

P.D. FILE NO. G A354AA

DRAWN REG	CHKD. <i>[Signature]</i>
ENGD. MJR	APPD. <i>[Signature]</i>

TELETYPE CORPORATION

8365WD

SEE SHEET I FOR NOTES.

CONTROL PANEL MARKINGS
FOR YESU 805,07,09
(SEE FIGURE 4)

NOTE:
REVISION INFORMATION MUST ALSO BE
REFLECTED ON THE ISSUE CONTROL REC-
ORD, WHICH IS A PART OF THIS DRAWING.

8365WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-30-68	19568-R
2	1-15-69	96482
3	5-15-69	99159
4	6-19-69	99306

NOTE II

POSITION NO.

MARKINGS NO.	ASSOC. YESU NO.	WIRING ARR'G'T	SET TYPE	A1	A2	A3	A4	A5	A6	B1	B2	B3	B4	B5	B6	C1	C2	C3	C4	C5	C6
1	809/--	AA	RO							INTRPT		OUT OF SERVICE	ERROR	PAPER ALARM	PTR EOL						
2	809/--	AB	RO							INTRPT	OFF LINE	HERE IS		ALARM	PTR EOL						
3	805/--	AA	KSR							INTRPT	HERE IS	OFF LINE	OUT OF SERVICE	ALARM	PTR EOL						
4	805/--	AB	KSR	INTRPT	PROCEED		HERE IS		OFF LINE							OUT OF SERVICE	ERROR		PAPER ALARM	PTR EOL	
5	805/-- 807/--	AC -AC	KSR		OFF LINE											INTRPT	PROCEED	HERE IS		ALARM	PTR EOL
6	807/--	AA	ASR	K	KT	T	TTS	TTR	OFF LINE							INTRPT	HERE IS	PROCEED	KBD EOL	PAPER ALARM	PTR EOL
7	807/--	AA	ASR	PUNCH GN	PUNCH LOCAL	READER LOCAL	PRINTER LOCAL	KBD LOCAL								INTRPT	HERE IS	PROCEED	KBD EOL	PAPER ALARM	PTR EOL
8	807/--	AB	ASR	INTRPT	PROCEED		HERE IS			K	KT	T	TTS	TTR	OFF LINE		OUT OF SERVICE	ERROR	KBD EOL	PAPER ALARM	PTR EOL
9	807/--	AB	ASR	INTRPT	PROCEED		HERE IS		READER AUTO	PUNCH ON.	PUNCH LOCAL	READER LOCAL	PRINTER LOCAL	KBD LOCAL			OUT OF SERVICE	ERROR	KBD EOL	PAPER ALARM	PTR EOL
10	807/--	AC	ASR	READER AUTO	KBD LOCAL	PRINTER LOCAL	READER LOCAL	PUNCH LOCAL	PUNCH ON							INTRPT	PROCEED	HERE IS	KBD EOL	ALARM	PTR EOL
11	807/--	AD	ASR	SINGLE BID	REPEAT BID			SEND	RECEIVE	PUNCH ON	PUNCH LOCAL	READER LOCAL	PRINTER LOCAL	KBD LOCAL		BUZZER OFF	ERROR	SEND ALARM	OUT OF SERVICE	PAPER OUT	EOL
12	809/--	AC	RO							OFF LINE	RECEIVE	BUZZER OFF	ERROR	OUT OF SERVICE	PAPER OUT						
13	809/--	AD	RO							INTRPT		OFF LINE		ALARM	EOL						
14	805/--	AD	KSR							INTRPT	PROCEED	OFF LINE		ALARM	EOL						
15	807/--	AC	ASR		KBD LOCAL	PRINTER LOCAL	READER LOCAL	PUNCH LOCAL	PUNCH ON							INTRPT	PROCEED		KBD EOL	ALARM	PTR EOL

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

WDP

SHEET 5

ANALYSIS
CHART
FOR
MODEL 37
CONTROL
PANEL
ARRANGEMENTS

APPROVALS

D AND R	E OF M
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E-NUMBER

PROD. NO. 8365WD

DATE 4/18/68

P.D. FILE NO. G-A354AA

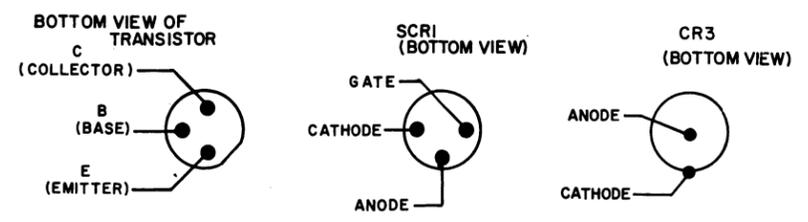
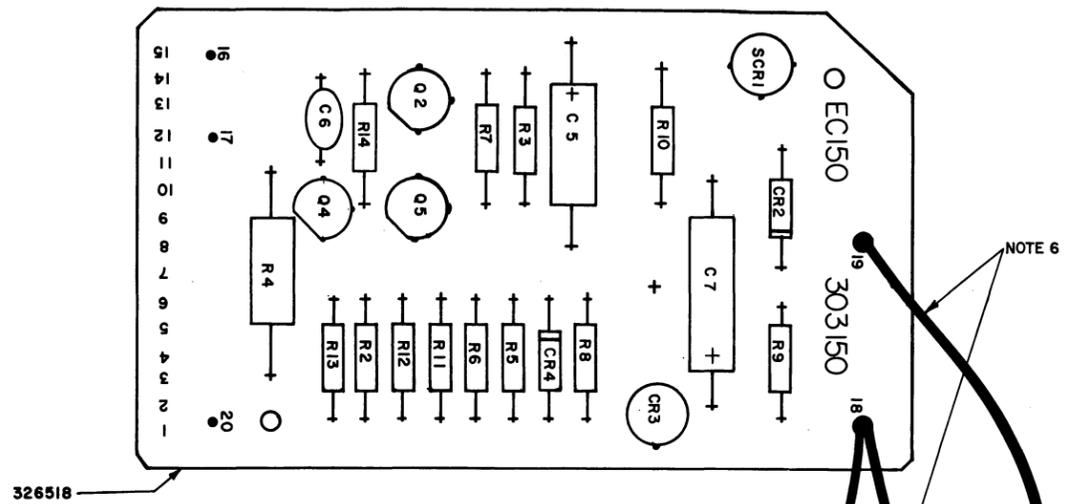
DRAWN REG CHKD. *[Signature]*

ENGD. M.J.R. APPD. *[Signature]*

TELETYPE CORPORATION

8365WD

NO.	NOTES
1.	SEE SPECIFICATION MRS2.001 FOR CIRCUIT BOARD REQUIREMENTS.
2.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY
3.	ASSOCIATED SCHEMATICS ARE: 8358 WD.
4.	ALL CHARACTERS ARE TO BE SILK SCREENED IN WHITE, BLACK, OR RED ENAMEL.
5.	CHARACTER HEIGHT .120 -12POINTS NEWS GOTHIC.
6.	STRAPS TO BE WIRED TO BOTTOM OF TERMINALS NO.18 & 19.



CIRCUIT CARD EC150

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R3	137443	1	RESISTOR, FIXED 1.8K, 1/2W.	
R2	129852	1	RESISTOR, FIXED 2.2K, 1/2W.	
R4	182627	1	RESISTOR, FIXED 390 OHM, 1/4W.	
R5	324657	1	RESISTOR, FIXED 511 OHM, 1/2W.	
R6	301747	1	RESISTOR, FIXED 200 OHM, 1/2W.	
R7	118725	1	RESISTOR, FIXED 270 OHM, 1/2W.	
R8	324657	1	RESISTOR, FIXED 511 OHM, 1/2W.	
R9	320006	1	RESISTOR, FIXED 8.2 OHM, 1/2W.	
R10	129856	1	RESISTOR, FIXED 150 OHM, 1/2W.	
R11	137604	1	RESISTOR, FIXED 620 OHM, 1/2W.	
R12	137441	1	RESISTOR, FIXED 1200 OHM, 1/2W.	
R13	165360	1	RESISTOR, FIXED 4.3K, 1/2W.	
R14	129856	1	RESISTOR, FIXED 150 OHM, 1/2W.	
C5	148837	1	CAPACITOR, 25MFD. 25VDC.	
C6	312385	1	CAPACITOR, 0.1MFD. 10VDC.	
C7	177412	1	CAPACITOR, 100MFD. 25VDC.	
CR2	146762	1	DIODE, IN753A 6.2V.	
CR3	324663	1	DIODE, IN4997	
CR4	321161	1	DIODE, IN748A 3.9V.	
Q2,4,5	324656	3	TRANSISTOR, 2N3569	
SCR1	324662	1	THYRISTOR, 2N4183	
	326584	3	PIN, FORMED.	
	118775	2	PIN, FORMED.	
	327834	1	STRAP	
	327835	1	STRAP	
	327836	1	STRAP	
	326518	1	CIRCUIT BOARD	

303150

REVISIONS

ISSUE	DATE	AUTH. NO.
2	5-8-68	95718
3	6-28-68	95937
4	6-26-69	98762

SHEET 1 OF 2

POWER SUPPLY REGULATOR

APPROVALS

R AND D: *H. J. K.* E OF M: *[Signature]*

E-NUMBER: PROD NO. 303150

DATE: 4-4-68

R&D FILE G-A354AA

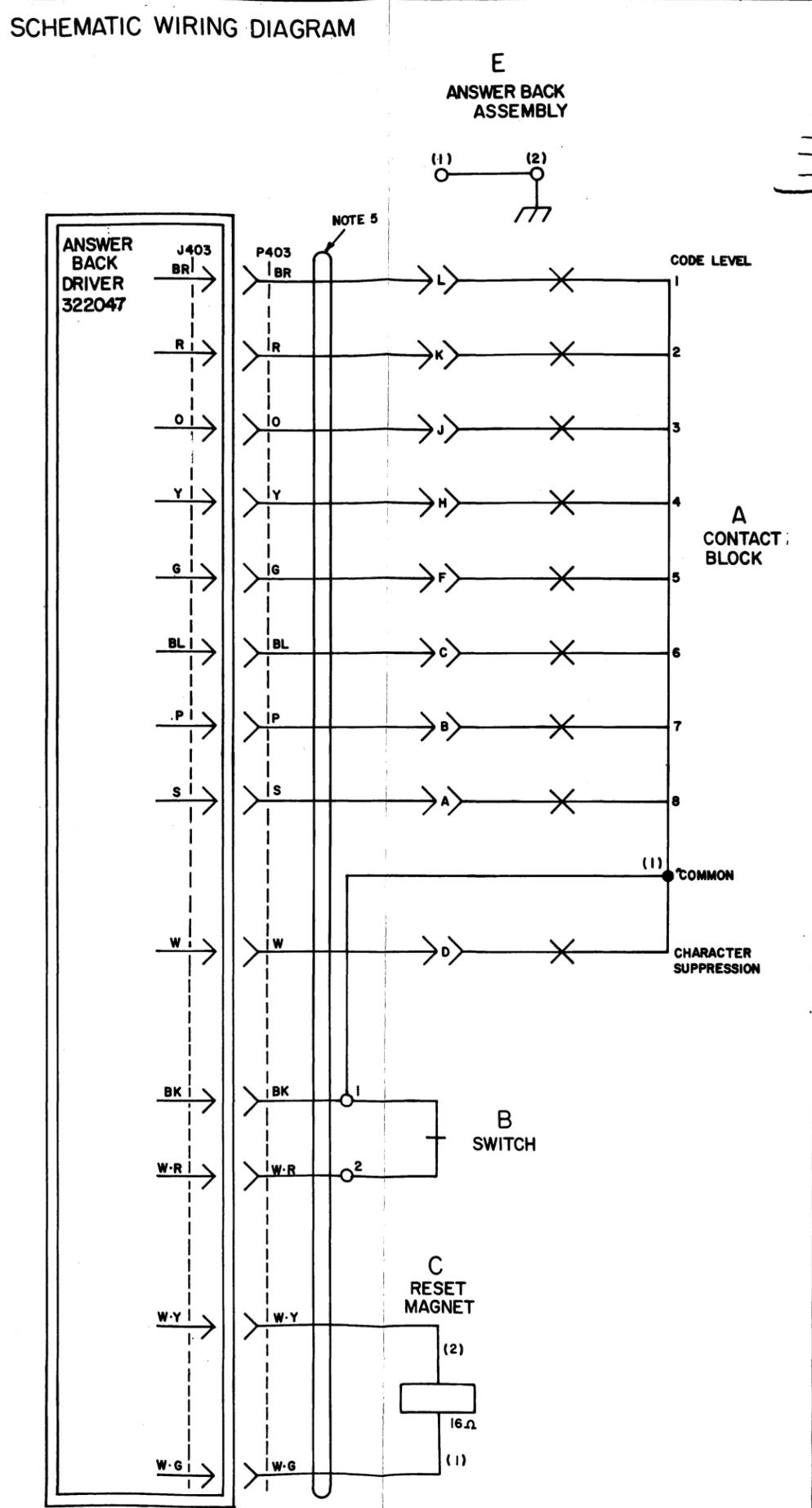
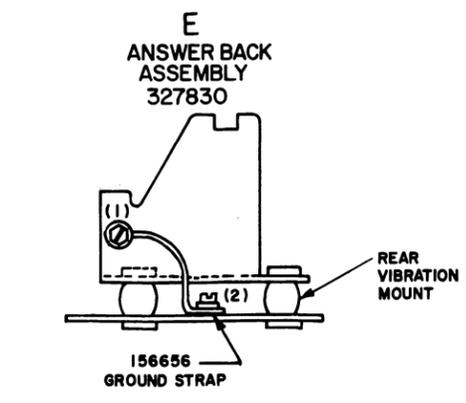
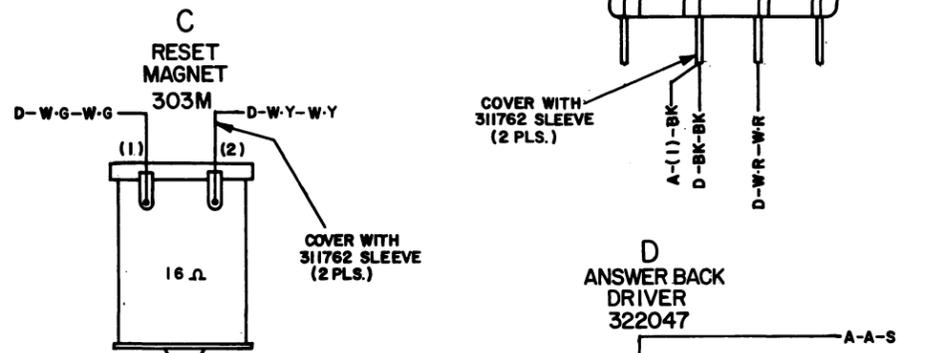
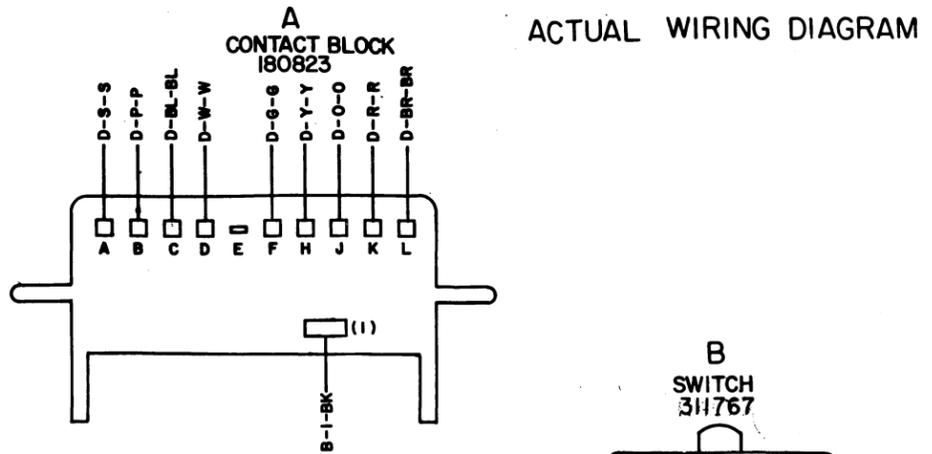
DRAWN W.P.B. CHKD. *[Signature]*
 ENG'D. M.J.R. APP'D. *[Signature]*

TELETYPE CORPORATION

303150

- NO. NOTES
1. WIRING LEGEND:
 2. COLOR CODE:

Y-YELLOW	G-GREEN
W-WHITE	R-RED
S-SLATE	O-ORANGE
P-PURPLE	BR-BROWN
BL-BLUE	BK-BLACK
 3. INDICATES MALE TERMINAL AND INDICATES FEMALE TERMINAL ON CONNECTOR.
 4. CONNECTORS VIEWED FROM WIRED ENDS.
 5. ASSOCIATED CABLE 326568.
 6. REFERENCE SPEC FOR TELETYPE CORPORATION EMPLOYEES ONLY. 61,429S.
 7. REFER TO 8376 WD-CD FOR SCHEMATIC WIRING DIAGRAM AND CIRCUIT DESCRIPTION.



8369 WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	5-2-68	19260 R
2	7-2-68	95827
3	8-23-68	96117
4	1-3-69	96485

ACTUAL & SCHEMATIC WIRING DIAGRAM FOR 327801 ANSWERBACK

APPROVALS

D AND R <i>[Signature]</i>	E OF M <i>[Signature]</i>
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E-NUMBER

PROD. NO. 8369WD

DATE 1-22-68

P.D. FILE NO. G-A354AA

DRAWN RJP

ENG. AB

CHKD. *[Signature]*

APPD. *[Signature]*

TELETYPE CORPORATION

8369WD

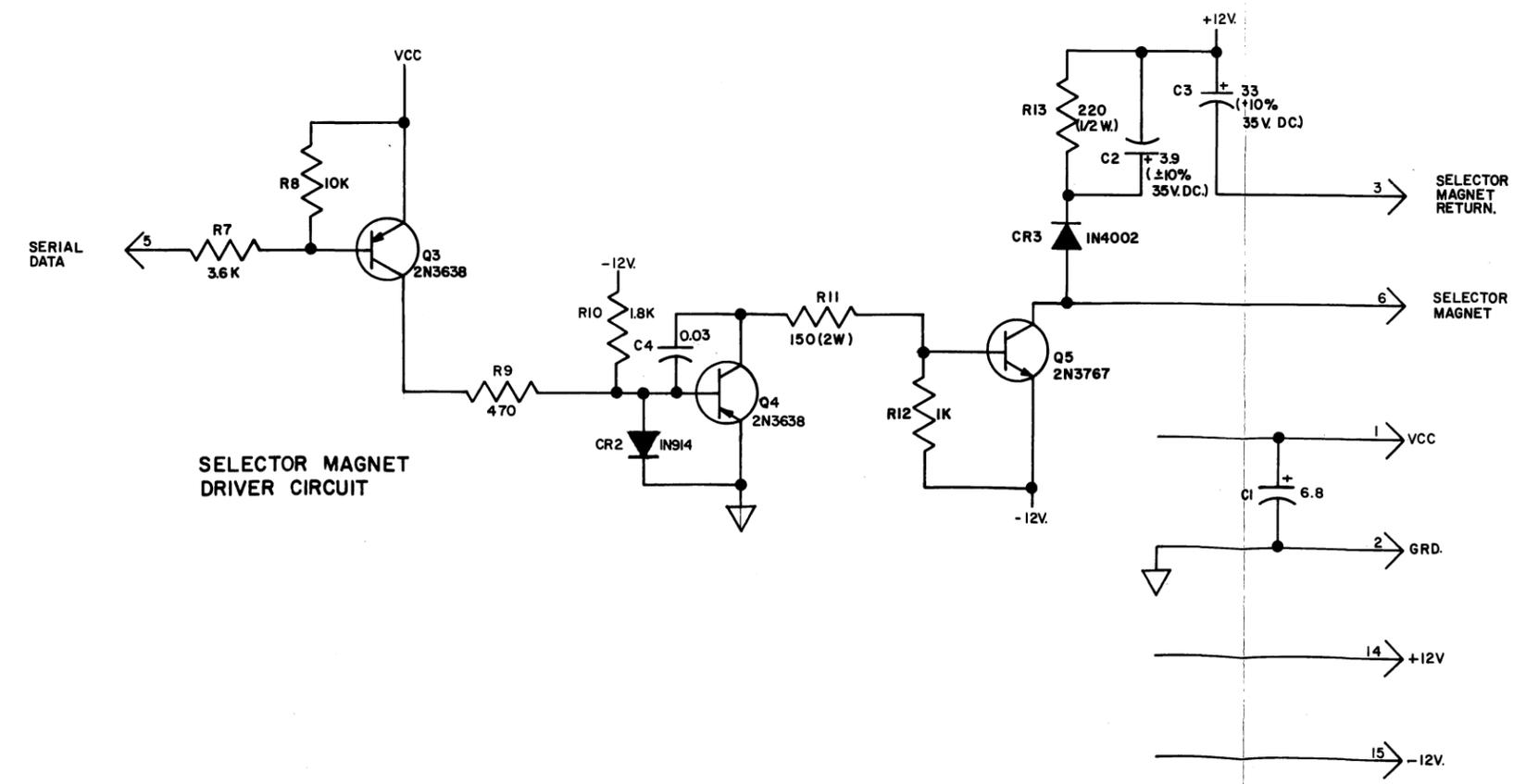
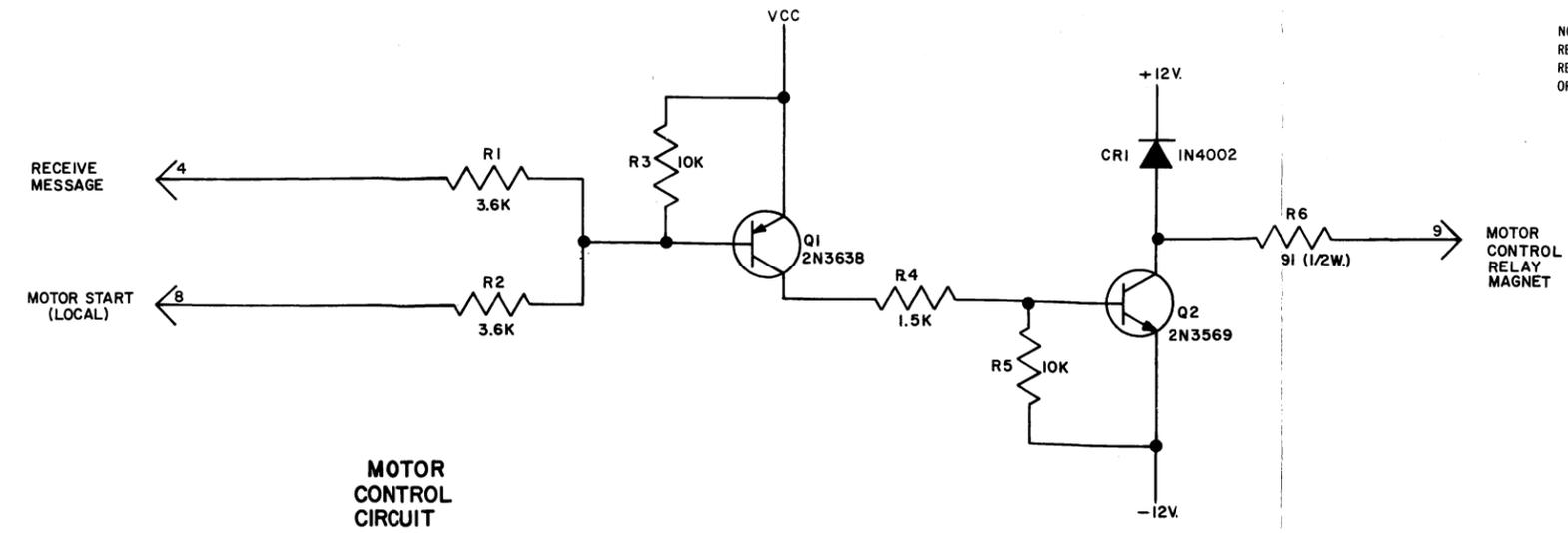
8370WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

NO.	NOTES
1.	ALL VOLTAGES DC. UNLESS OTHERWISE SPECIFIED.
2.	ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
3.	ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
5.	 INDICATES FEMALE AND  INDICATES MALE TERMINAL
6.	REFER TO 303149 FOR ASSEMBLY INFORMATION.
7.	S NUMBER: 61,428 S.
8.	REFERENCE CIRCUIT DESCRIPTION: 8370WD-CD.
9.	 INDICATES CIRCUIT GROUND.

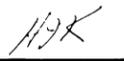


SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET-1

SCHEMATIC WIRING DIAGRAM FOR RECEIVING DEVICE

APPROVALS

D AND R	E OF M
	
E-NUMBER	
PROD. NO. 8370 WD.	
DATE 2-29-68	
P.D. FILE NO. G-A354AA	
DRAWN W.P.B.	CHKD. 
ENGD. C.A.Y.	APPD. 

TELETYPE CORPORATION

8370WD

CIRCUIT DESCRIPTION OF THE RECEIVING DEVICE LOGIC CARD
(ASSEMBLY NUMBER 303149)

TABLE OF CONTENTS

<u>SECTION</u>	<u>DESCRIPTION</u>	<u>TOTAL PAGES IN SECTION</u>
I	General Technical Information	2
II	Detailed Description and Theory of Operation	1

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE RECEIVING DEVICE LOGIC CARD
(ASSEMBLY NUMBER 303149)

SECTION I

GENERAL TECHNICAL DATA

1. BASIC FUNCTION

1.1 The 303149 Receiving Device Logic card combines the function of a selector magnet driver and a motor control relay driver.

1.2 Selector Magnet Driver

The selector magnet driver sinks a steady state current of up to 600 ma DC on a MARK input and sinks zero current on a SPACE input. The MARK input is a logic one, and a SPACE input is a logical zero.

1.3 Motor Control

The motor control relay driver is capable of supplying a current of 40 to 60 ma to operate the motor control relay. The relay will be operated on a logic zero input and released on a logic one input.

2. GENERAL TECHNICAL DATA

2.1 Input-Output Data

2.1.1 The Receiving Device Logic card converts the integrated circuit logic levels to current levels appropriate for magnet operation.

A logic one is defined as a voltage level between 5.0 Volts and 6.6 Volts (usually a logic one approximates the integrated circuit supply voltage). A logic one draws no current from the input of the logic element.

162

Signal voltages between circuit ground potential and +0.5 Volts are considered logic zero.

2.2 Input-Output Characteristics

Motor Control

2.2.1 Receive Message/Motor Start Local (Pins 4 and 8)

These two inputs are connected together in a logical or configuration. A logic zero input will energize the associated motor control relay. Input impedance is 3.6K.

2.2.2 Motor Control Relay Magnet (Pin 9)

The associated motor control relay is connected to this output (typical coil resistance 430 ohms). The output impedance is 91 ohms in series with a -12 Volts. The relay driver output is capable of supplying up to 60 ma of current. Relay magnet drop-out is diode suppressed.

SEE ISSUE CONTROL
RECORD FOR COM-
PLETE LIST OF SHEETS
COMPRISING THIS
W.D.
DRAWING.

Selector Magnet Driver

2.2.3 Send Data (Pin 5)

Under the control of set logic this input is supplied with MARK and SPACE signals corresponding to received data. A logic one signal (MARK) will cause the selector magnet to be energized. A logic zero signal (SPACE) will de-energize the selector magnet. Input and impedance is 3.6K.

2.2.4 Selector Magnet (Pin 6)

The negative end of the selector magnet is connected to this output which will establish a discharge path through a Diode coupled resistor capacitor network. Typical dropout time is approximately 2.50 milliseconds.

2.2.5 Selector Magnet Return (Pin 3)

The positive end of the selector magnet is connected to this output. In series with the selector-coil is a parallel resistor capacitor network which permits maximum current through the coil during SPACE to MARK transitions. Typical MARK hold current is approximately 600 milliamperes. Nominal rise time is 2.25 milliseconds. Typical load supplied is 3.5 ohms 20 millihenries inductance.

2.3 Mechanical Requirements

The motor control amplifier and the selector magnet driver are mounted on a 15-pin circuit board.

2.4 Power Requirements

D.C. Supply

Current Required

+5.0V to +5.50V (+5.25V Nom.)	0 to 20 ma
+11.65 to +13.75V (+12.5V Nom.)	0 to 660 ma
-11.13V to -13.88V (-12.5V Nom.)	0 to 660 ma

2.5 Operating Temperature Range

0°C to 70°C (in free air)

2.6 Storage Temperature Range

-40°C to 70°C

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

- 1.1 Schematic Drawing - 8370 WD.
- 1.2 Assembly Drawing - 303149.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Selector Magnet Driver

2.1.1 The selector magnet driver circuit is a three stage amplifier, designed to operate full on or off without intermediate levels. The input characteristics are matched to the output of currents sinking DTL integrated circuit elements. The output circuit is matched to the characteristics of the 312936 Selector Magnet Assembly.

2.1.2 A logic one signal input, (See Section I-2.1), will turn the output on, picking up the selector magnet armature. The logic one signal turns off Q3, allowing Q4 and Q5 to be turned on. With Q5 turned on, C3 will be charged through the load impedance to give a high initial current. As C3 becomes charged, load current will be limited by the external 50 ohm, 50 watt resistor connected across C3.

2.1.3 With a logic zero signal on the input, (see Section I-2.1), Q3 will be turned on, driving the base of Q4 positive, turning off Q4 and Q5. The positive voltage on the base of Q4 is limited by ground clamp Diode CR2. With Q5 turned off, the load inductance and C3 will discharge through steering Diode CR3, and the discharge network C2, R13. The impedance values of the output circuit are chosen to provide equal selector magnet armature pickup and drop-out times. The characteristics of the (loaded) output circuit will determine the maximum signalling rate. The values chosen will give proper operation with a nominal pulse length of 6 ms or more.

2.2 Motor Control Relay Driver

2.2.1 The motor control relay driver is a two-stage amplifier which is designed to operate full ON or OFF without intermediate levels. This circuit is designed to drive an external motor start relay. Inputs to the motor control relay drive circuit are on Pins 4 and 8. The inputs are connected in a logical OR configuration each having an input resistance of 3.6K. With logic zero, (see Section I-2.1), applied to either input, Q1 is switched ON. This switches Q2 ON, energizing the relay. With logic one applied at both inputs Q1 and Q2 are switched OFF. When Q2 is switched OFF, any positive voltage transient developed by the inductive load will be clamped to the positive supply voltage by CRL.

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8371WD

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1	3-10-69	19887 R

- | NO. | NOTES |
|-----|--|
| 1. | ALL VOLTAGES DC, UNLESS OTHERWISE SPECIFIED. |
| 2. | ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED. |
| 3. | ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED. |
| 4. | <p>INDICATES FEMALE CONNECTOR.
INDICATES MALE CONNECTOR.</p> <p>INDICATES CIRCUIT GROUND.</p> |
| 5. | <p>MLBI
ROW
COLUMN
INTEGRATED CIRCUIT</p> |
| 6. | ASSOCIATED ASSEMBLY: 322059. |
| 7. | S-NUMBER: 61658 S |
| 8. | REFERENCE CIRCUIT DESCRIPTION 8371WD-CD. |
| 9. | WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USE AS AN INVERTER. |
| 10. | LOGIC NEGATION: A SMALL CIRCLE JOIN TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION. |
| 11. | THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE +6V AND 0V, RESPECTIVELY. |
| 12. | VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14, AND GROUND ON PIN 7. THIS APPLIES TO ALL PACKAGES EXCEPT MLBI. |
| 13. | REFER TO 8399WD FOR TRUTH TABLES. |
| 14. | ABBREVIATIONS:
ST - START.
SP - STOP.
TCL - TIMER CONTROL LATCH.
CSL - CHARACTER SAMPLE LATCH.
CCL - CONTROL CHARACTER LATCH.
OBL - OUTPUT BLIND LATCH.
ECL - ESCAPE CHARACTER LATCH.
TCS - TIMER CONTROL SET.
TC - TAKE CHARACTER.
PNC - PRESENT NEXT CHARACTER.
FX32 - FREQUENCY X 32
RS(NOT) - REGISTER SAMPLE NOT.
CP - CLOCK PULSE.
SCS - SHIFT CONTROL SAMPLE.
CC(NOT) - CONTROL CHARACTER NOT. |

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC
WIRING DIAGRAM
FOR
DISTRIBUTOR

APPROVALS

D AND R	E OF M
<i>LDM</i>	<i>[Signature]</i>

E-NUMBER

PROD. NO. 8371 WD.

DATE 4-24-68

P.D. FILE NO. G-A354 AA.

DRAWN W.P.B. CHKD. *[Signature]*

ENGD. A.B. APPD. *[Signature]*

TELETYPE CORPORATION

8371WD

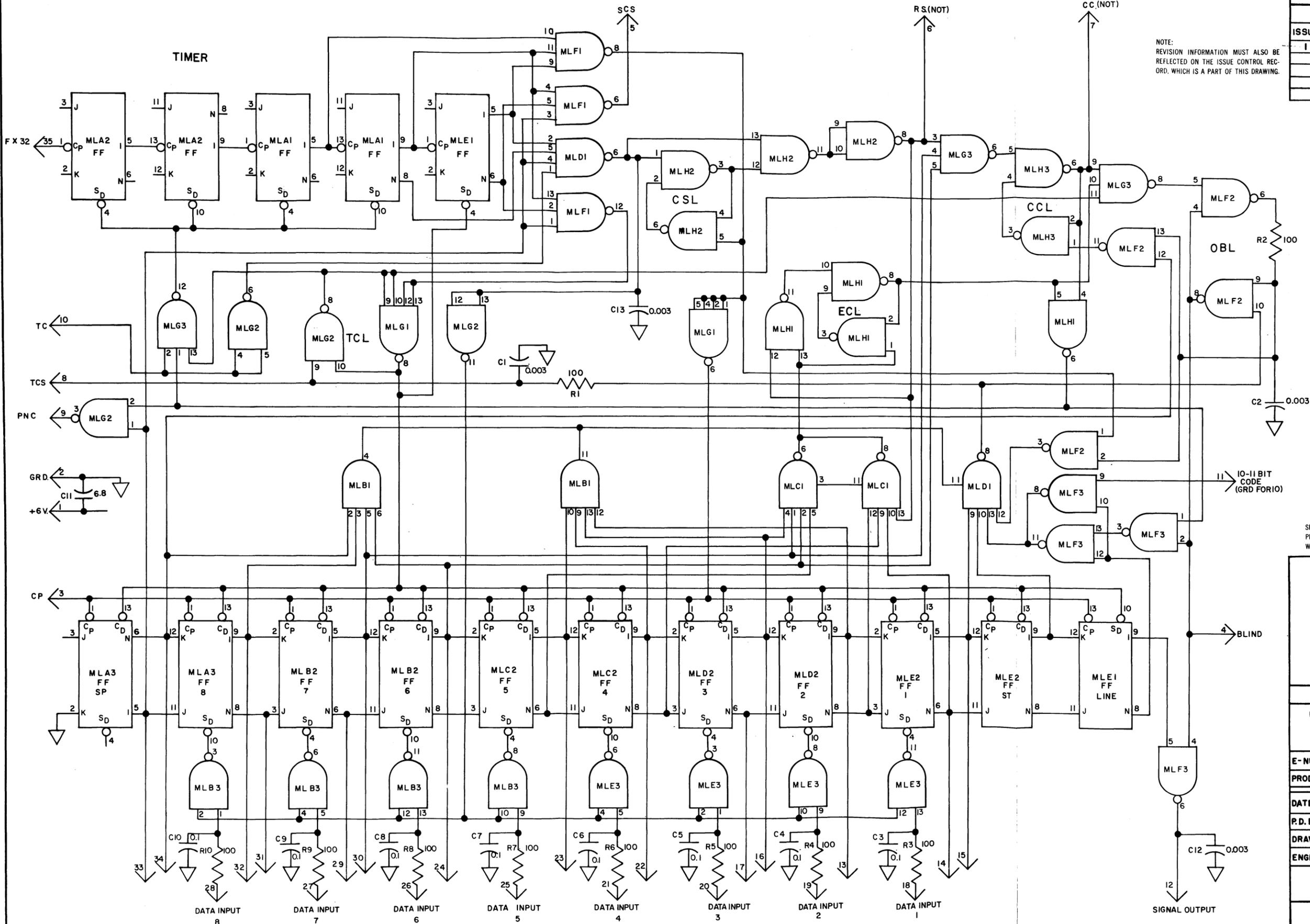
SEE SHEET 1 FOR NOTES.

8371WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-10-69	19887 R

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SCHEMATIC WIRING DIAGRAM FOR DISTRIBUTOR.

APPROVALS

D AND R *[Signature]* E OF M *[Signature]*

E-NUMBER
 PROD. NO. 8371WD
 DATE 4-24-68
 P.D. FILE NO. G-A354AA
 DRAWN W.P.B. CHKD. *[Signature]*
 ENGD. A.B. APPD. *[Signature]*

TELETYPE CORPORATION

8371WD

CIRCUIT DESCRIPTION OF THE ELECTRONIC TRANSMITTING DISTRIBUTOR
(ASSEMBLY NUMBER 322059)

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<u>Section</u>		<u>Total Pages In Section</u>
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II	Detailed Description and Theory of Operation	7

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

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CIRCUIT DESCRIPTION OF THE ELECTRONIC TRANSMITTING DISTRIBUTOR
(ASSEMBLY NUMBER 322059)

SECTION I

GENERAL TECHNICAL DATA

1. BASIC FUNCTION

1.1 The 322059 Circuit Card Assembly is an Electronic Transmitting Distributor with Control Character Detection. The device converts parallel input signals to serial output signals of either 10 or 11 unit code. The parallel input consists of eight information levels (bits). The serial output consists of a start bit, eight information bits, and one or two stop bits. The telegraphic speed is determined by an external oscillator.

1.2 In addition to the basic data transmitting function of the assembly, several other functions are provided. These functions are:

1.2.1 Responds to a character delete signal (blind), and inhibits transmission of a character.

1.2.2 Recognizes ASCII control characters (6th and 7th level spacing), except ESC and electronically delays the transmission of the next character. The delay interval is a fraction more than a character length, depending upon the character unit code.

1.2.3 Recognizes ASCII control character ESC (11011000) and electronically adds a one character delay after the character following the ESC character.

1.2.4 Provides an output signal which indicates that a character is stored in the register and can be decoded.

1.2.5 Provides an output signal which is used to sample conditions prior to the parallel data input sample.

1.2.6 Provides an output signal which indicates that another character may be distributed.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the assembly are all nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts.

2.1.1 Take Character (TC) (Pin 10)

The TC input controls the start of the distribution cycle. When the input is in the 0-state, less than 0.5V, it indicates that a character is available for distribution. Once distribution has commenced, this input will have no further effect until the end of the cycle. This input must be low for at least .25 of a bit before it will be recognized as a legitimate start signal. The device driving the input must be capable of sinking one DTL load.

2.1.2 Data Input (Pins 18, 19, 20, 21, 25, 26, 27, 28)

The device driving these inputs must be capable of sinking one DTL load. These inputs will only have effect on the distributor from .5 to .75 of a bit after the TC input first reverts to the low state. At all other times these inputs will not affect the distributor.

2.1.3 Blind Input (Pin 4)

A momentary low on this lead blinds the line to the distribution of the following character. The device driving this input must be capable of sinking four DTL loads. This input should never be allowed to revert to the 0-state except when the PNC output is low. Otherwise, the line would be blinded somewhere in the middle of a character, resulting in an errored character being transmitted. The low on the blind input must be removed before the end of the blinded character to allow the distributor to reset the Output Blind Latch.

2.1.4 Control Character Latch (CC(NOT)Inhibit)(Pin 7)

This input is grounded to disable the control character blind feature (See Paragraph 1.2.2). The device driving this input should be capable of sinking three DTL loads.

2.1.5 Register Condition (TCS)

This input may be grounded in order to clear the register. This may be a requirement in some applications where at times certain characters will not be transmitted. The device driving this input should be capable of sinking three DTL loads.

2.1.6 F X 32 (Pin 35)

This input is from an external oscillator. The frequency of the oscillator must be 32 times the desired bit-rate. The device driving this input must be capable of sinking two DTL loads.

2.1.7 10-11 Unit Option (Pin 11)

This input is grounded when the distributor is operating with a 10 unit character code. It is opened or high for 11 unit operation. The device driving this input must be capable of sinking one load.

2.2 Output Characteristics

The outputs from this assembly are all nand type Diode Transistor Logic (DTL) outputs. The outputs will be rated by the number of DTL loads it can sink. Each DTL load is approximately 1.4 ma.

2.2.1 Present Next Character (PNC) (Pin 9)

This circuit is capable of driving eight DTL loads. When the distributor is idle, this output will be 0-state (approximately .3V).

2.2.1 (Continued)

When this output is low, a character may be presented for distribution. It will revert to the 1-state (approximately Vcc) at the beginning of a distributor cycle. It will remain in the 1-state until the character has been distributed, at which time it will revert again to the 0-state.

2.2.2 Serial Data Output (Pin 12)

A mark signal is represented by a 1-state at this output and a space signal by the 0-state. This output sinks up to eight DTL loads.

2.2.3 Control Character Recognition [CC (NCT)] (Pin 7)

This output is the same as the Control Character Lat ch Inhibit input. This output will change from the 0-state to the 1-state when a control character is recognized, and will remain in the 1-state for a time duration of 1.1 characters. It is capable of sinking six DTL loads.

2.2.4 Clock Pulse (CP) (Pin 3)

The clock pulse output is a timing output. This output reverts to the one state for approximately .12 of a bit, occurring at the trailing edge of each transmitted bit.

2.2.5 Register Sample [RS (NOT)] (Pin 6)

The Register Sample output is approximately .12 bits in duration occurring between .75 to .87 of a bit following the start of the distributor. When this output reverts from its normally low state to the 1-state, it indicates that a character is in storage, and the parallel data outputs of the register may now be sampled. This output is capable of sinking current from seven additional DTL loads.

2.2.6 Parallel Data Outputs (Pins 14, 17, 29, 31)

When these parallel outputs are in the 1-state it indicates that a mark is stored in the particular position that the given lead is monitoring. These outputs are capable of sinking seven DTL loads.

2.2.7 Parallel Data Outputs (Pins 13, 15, 16, 22, 23, 24, 30, 32)

When these parallel outputs are in the 1-state it indicates that a space is stored in the particular position that the lead is monitoring. Pins 13, 15, 16, 22, 23, and 32 are capable of sinking six DTL loads. Pins 24 and 30 are capable of sinking five DTL loads.

2.2.8 Shift Control Sample (SCS) (Pin 5)

The output of SCS reverts to the 0-state from .25 to .5 of a bit after the start of the distributor. It is a timing signal occurring prior to

2.2.8 (Continued)

the character sample, and may be used to set up characters in external logic prior to the character sample by the distributor.

2.2.9 Stop Output (SP) (Pins 33, 34)

Pin 33 is in the 1-state when a stop bit is set in the SP Flip-Flop. This is a timing signal which may be used by external logic to identify that a character is being distributed. Pin 33 is capable of sinking four DTL loads. Pin 34 is capable of sinking five external DTL loads.

2.3 Size

The distributor is a 5-3/4 inch by 4-1/4 inch circuit card which mates with a standard 36 pin circuit card connector.

2.4 Options Available

2.4.1 The distributor may be changed from eleven unit code to ten unit code by grounding Pin 10.

2.4.2 Another option is the electronic insertion of an idle time, one character in duration, following each ASCII control character except control character ESC. This feature may be removed by grounding Pin 7. Grounding Pin 7 also removes the electronic insertion of a character interval for the character following the control character ESC.

2.5 Miscellaneous Requirements

2.5.1 Power Supply Requirement

VDC	I (ma)
+5V to +6.6V	520 ma (max)

2.5.2 Operating Temperature Range

0°C to 70°C (free air)

2.5.3 Storage Temperature Range

-40°C to +70°C

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

- 1.1 Assembly drawing 322059 (MC059) and schematic drawing 8371 WD.
- 1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

- 2.1 Refer to the timing diagram, flow chart and the schematic 8371 WD to aid in understanding the following discussion.

The flow chart should be used as an outline. When two lines enter a symbol, it is implied that either input causes the function in the symbol to be performed. It is not intended that any of the symbols be construed to represent logic functions. The flow chart is intended to relate circuit operation with respect to time.

2.2 Starting Function

Assume that the distributor is idle, i.e., no character is being distributed. In this state the distributor issues a present next character command (PNC in 0-state) which indicates to external logic that a character may be presented for distribution. The command to begin the distribution cycle is presented on the take character lead. This command (TC in 0-state) releases and controls the timer through M1G3-12.

The TC must remain ON for at least .25 of a bit, after which time the timer is locked on by the timer control latch, TCL, for one distribution cycle. Should TC turn off anytime prior to .25 bit, the timer will be recycled to the 0-count. This time period provides integration to reject noise pulses at the TC input.

When the time out reaches .25 of a bit, two gates M1F1-6 and M1F1-12 change to the 0-state. M1F1-6 provides the shift-control sample (SCS) signal at Pin 5, while M1F1-12 sets the timer control latch (TCL). An output from TCL locks the timer on, committing the distributor to a complete character cycle. (As a condition, the take character input must remain on for .75 of a bit to assure that a character is correctly entered into the shift register.)

2.3 Preliminary Events

The shift-control signal (SCS) started at .25 of a bit remains on until .5 bit. This signal is used by keyboard logic to perform a controlling function.

At .5 of a bit gate M1D1-6 changes to the 0-state. This condition causes the character sample latch to set and opens the character input gates M1B3 and M1E3 to accept data signals. A 1-state on any data input level sets a MARK into the corresponding register flip-flop. The sample period lasts for one quarter bit (until .75 of a bit after TC) at which time M1D1 reverts back to the one-state. If TC is removed prematurely i.e., before .75 bit the

2.3 (Continued)

character sample period will be terminated early or may not occur at all. TC may be removed after .75 bit.

Immediately following the character sample period the register sample (RS) pulse is developed. This is a positive going output which appears on Pin 6. This output, lasting .12 bits, indicates to external logic that a character has been stored in the register and may now be sampled. Internally this signal enables the control character detected gate MLG3-6, whose functions will be further discussed in the control character section.

At approximately .87 of a bit, the clock pulse changes to the 1-state, priming the data flip-flops. At exactly 1-bit time (.13 bits later) the clock pulse reverts to the 0-state. At this time each data bit stored in the distributor is shifted one position. Additional clock pulses shift the data to the LINE flip-flop, which becomes the output signal. This continues for nine additional clock pulses, (10 for an 11-unit code), at which time the register will have been cleared (all flip-flops in the space condition). The distribution cycle is now completed.

2.4 Serializing Function

The serializing function is performed by the shift register. It consists of eleven clocked flip-flops, labeled on the schematic as Stop (SP), Start (ST), Line (LINE) and Data Levels 1 through 8. Information is transferred into the shift register on a parallel basis. When the Sp input of any flip-flop reverts to the 0-state, a mark is set in that position of the distributor. Positions SP, ST and LINE are set internally. The elements are cascaded in such a manner that a positive pulse applied to the CP input of the flip-flop will result in each flip-flop assuming the state of the preceding flip-flop when the pulse is removed. Therefore, the shift register performs the function of serializing parallel input signals.

When the distributor is idle, TCL is used to hold the register in the no character stored state, that is, data positions 1 through 8 and ST are held spacing while SB and LINE are held marking. The result is that a character cannot be set in the register until TCL is set, which occurs .25 of a bit after TC. Data bits are read into the register during the character sample period, .5 to .75 of a bit after TC. A 1-state on any data input during the sample period sets a mark into the corresponding data flip-flop. Likewise a 0-state on any data input for the duration of the sample period holds the corresponding data flip-flop in its cleared state (corresponding data flip-flop remains spacing). When the character sample period has passed, the data input leads have no further effect on the distributor.

One bit time after TC, the first clock pulse occurs. Each data bit in the register is shifted one position. After nine additional clock pulses, (10 for 11 unit code) the entire register will have been cleared to the spacing condition, that is, a space stored in each flip-flop. Register condition gate, MLD1-8, then reverts to the 0-state. MLD1-8 resets the timer control latch, TCL, and the output blind latch, OBL, if it had been previously set. TCL clamps the register and sets a MARK in the SB flip-flop which in turn causes the present next character, PNC, command to be issued. A new cycle may now begin.

2.5 Control Character Operation

Another function of the distributor is to insert a marking interval of approximately one character length after the transmission of each control character. This time period is needed by the typing unit to detect, respond, or perform logic associated with certain control characters prior to the transmission of the next character. This feature may be inhibited by grounding the CC (NOT) lead, Pin 7.

When a control character has been entered in the distributor, its presence is recognized by the control character recognition gate, MLC3-6. This gate has inputs to monitor the registers sixth and seventh level for a spacing condition and a lead to monitor the register sample time. After the data has been loaded into the register (.5 to .75 bit after TC), the register sample lead, RS, reverts to the one-state (from .75 to .87 bit after TC). Therefore, for all control characters the control character recognition gate sets the control character latch, CCL.

The control character is then transmitted as any other character. After the control character has cleared the register, the register condition gate MLD1-8 resets the timer control latch, TCL. At this time the output blind latch, OBL, is set via gate MLC3-8, for all control characters except ESCAPE (ESC), which will be discussed later. The output blind latch keeps the signal output at Pin 12 in a MARK state. The control character latch, set previously, inhibits the present next character (PNC), output and provides the input required to cycle the distributor for another character interval. After the register is empty (the stop bit has moved through the register), the TCL and OBL are reset by the register condition gate MLD1-8.

When operating in 10 unit code the detection of a control character causes the distributor to shift into the 11 unit code for the control and delay character. This adds two bit intervals to the control character-delay character length. When in 10 or 11 unit code, an additional interval, approximately .87 bit, is provided by gate MLF2-3. These added time intervals are necessary to insure that all typing unit responses are completed before another character is transmitted.

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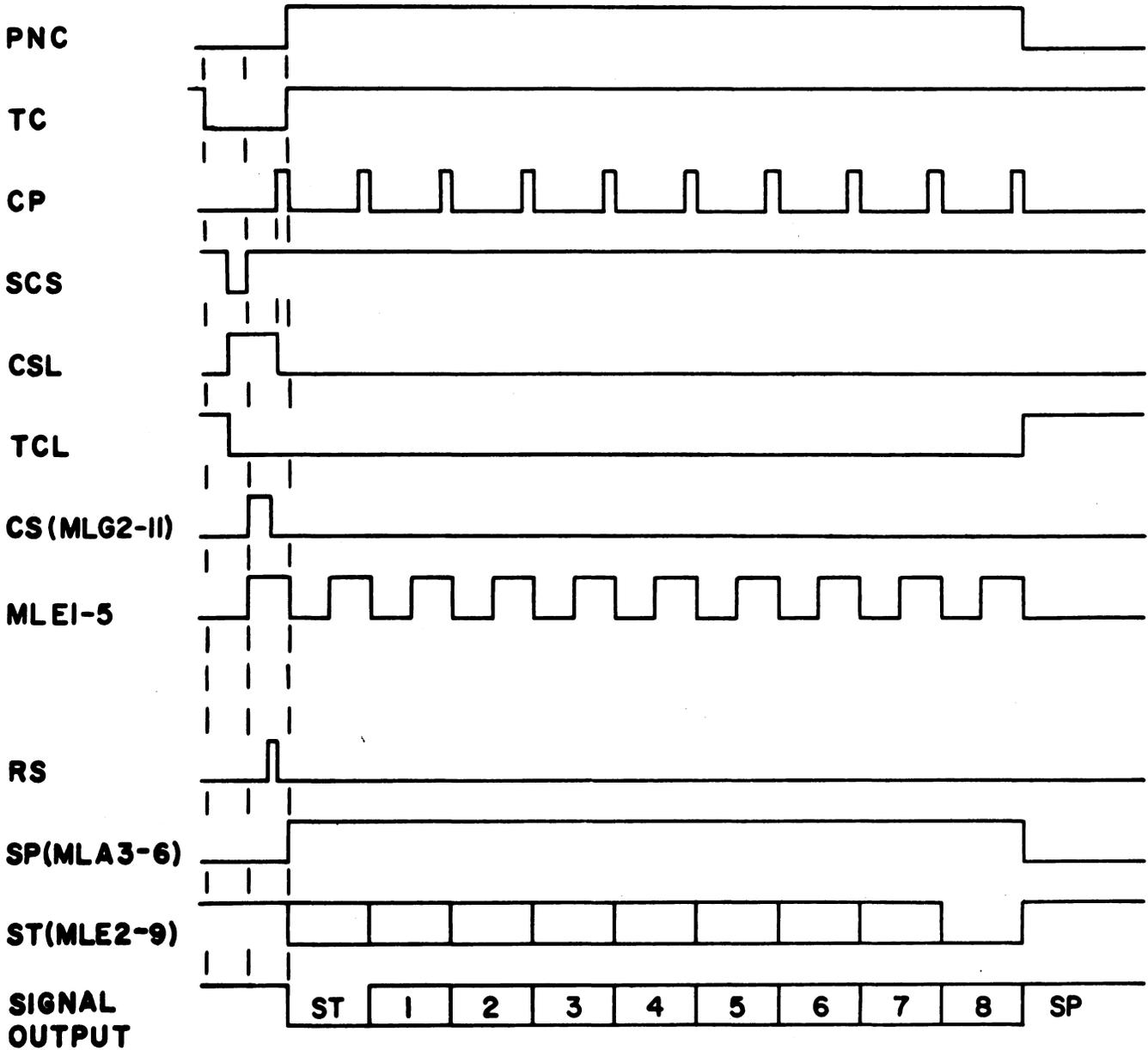
2.6 ESCAPE Character Operation

Another function of the distributor is to insert a marking interval of approximately one character length after the transmission of the character following the control character ESC. No delay is provided after the ESC character. The control character ESCAPE in itself performs no function in the typing unit. The character following ESCAPE is used by the typing unit to perform a function. The delay, therefore, is added after this two character ESCAPE sequence to allow the typing unit to complete its control function before transmission of the next character. This feature may also be inhibited by grounding the CC (NOT) lead, Pin 7.

2.6 (Continued)

An escape character is detected in the escape recognition gate MLC1-6 and MLC1-8 which in turn sets the escape character latch, ECL. ECL inhibits the operation of the output blind latch, OBL, and allows the present next character, PNC, to be issued immediately after the control character ESCAPE has been transmitted. The control character latch CCL, however, remains set. A character other than ESCAPE resets ECL which in turn removes the inhibit from gate MLC3-8. The distributor now operates as if a control character had been detected.

DISTRIBUTOR TIMING DIAGRAM

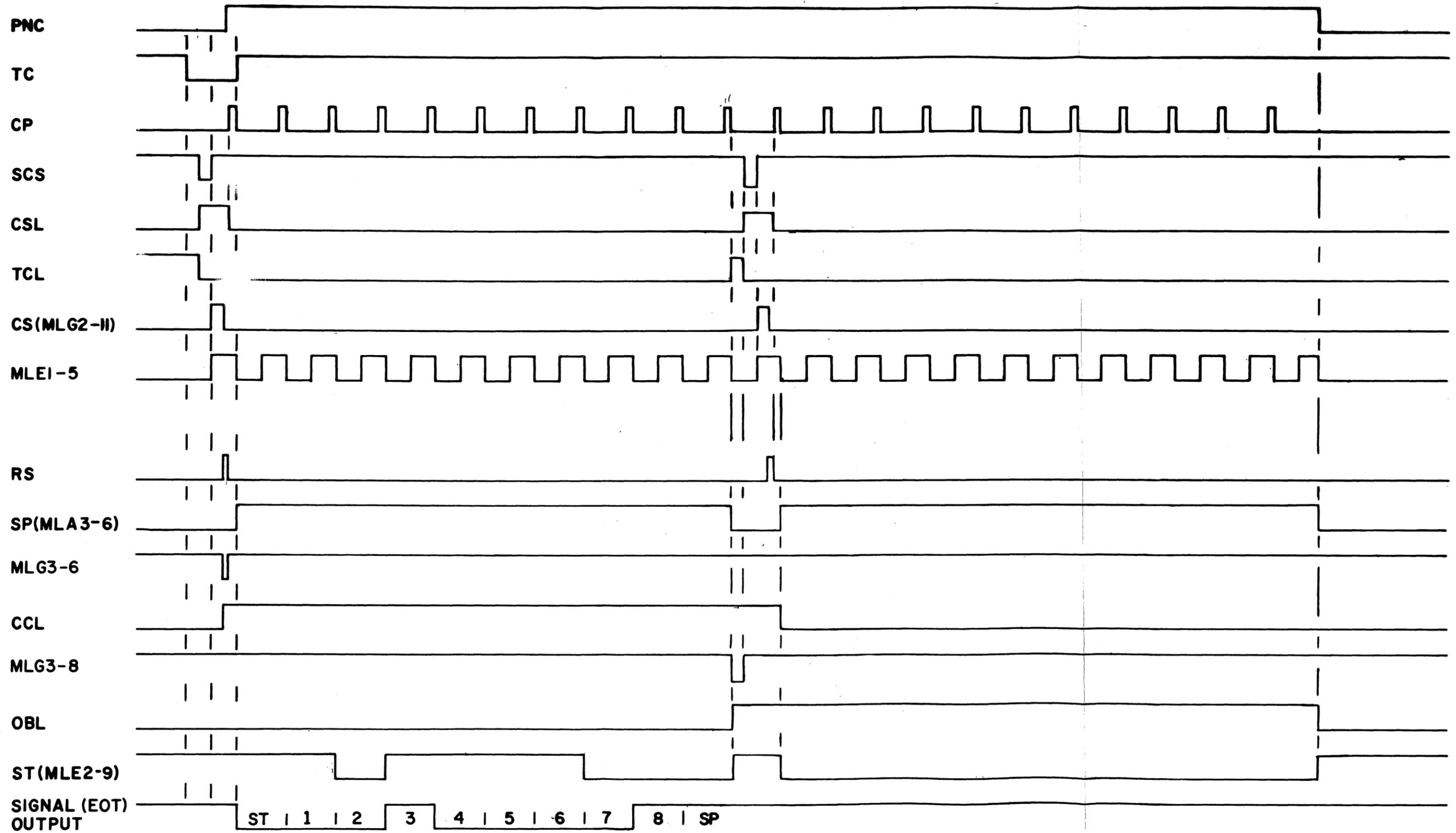


90

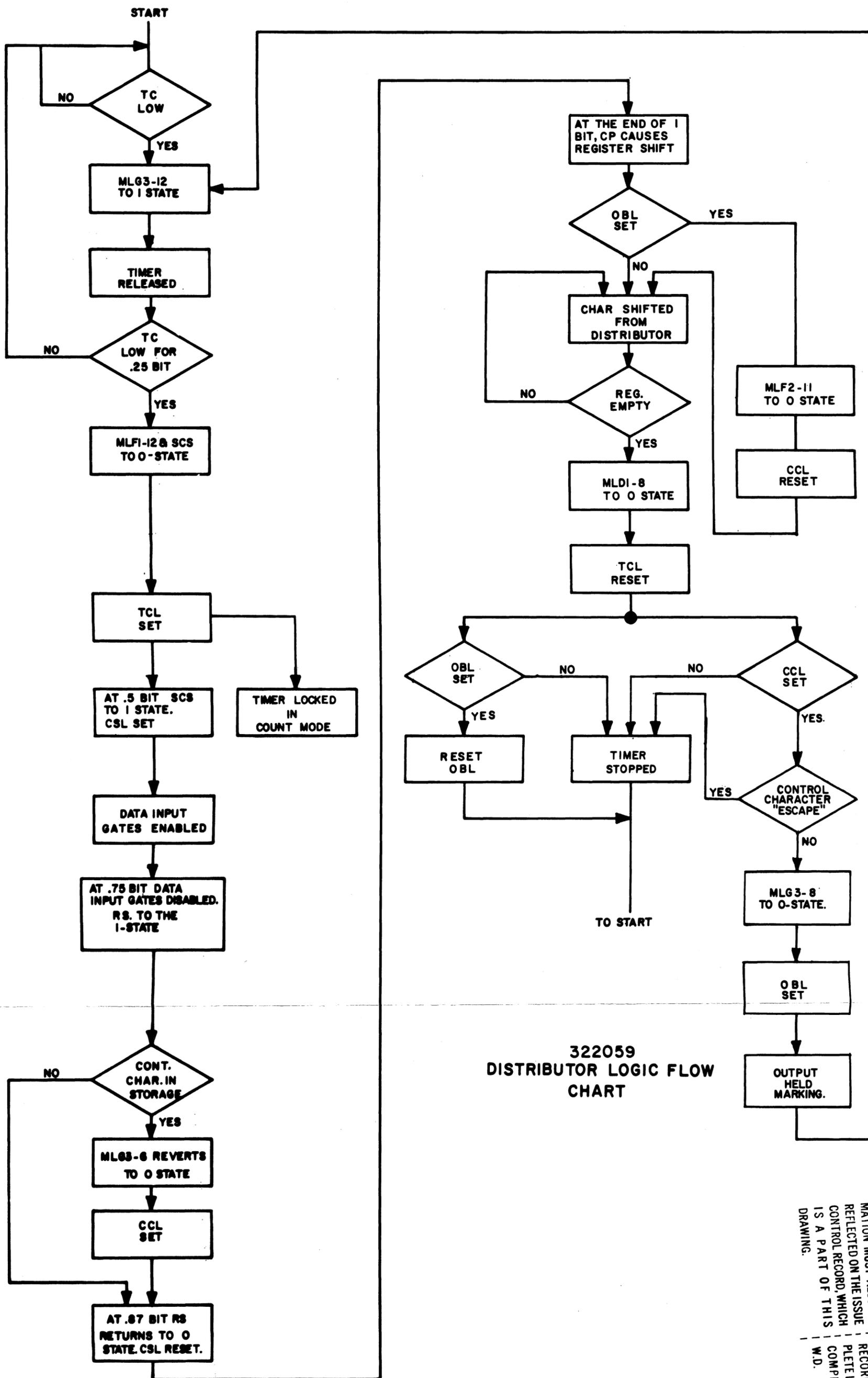
NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

DISTRIBUTOR TIMING DIAGRAM
FOR CONTROL CHARACTERS
(ESCAPE EXCLUDED)



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322059
DISTRIBUTOR LOGIC FLOW
CHART

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CIRCUIT DESCRIPTION OF THE KSR SEND CONTROL CARD
(ASSEMBLY NUMBER 322304)



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NOTE:
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PLETE LIST OF SHEETS COMPRISING THIS
W.D.

CIRCUIT DESCRIPTION OF THE KSR SEND CONTROL CARD
(ASSEMBLY NUMBER 322304)



SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The basic function of the 322304 KSR Send Control Card is to coordinate two sending devices, which are the Keyboard and Answer Back, for operation in conjunction with a transmitting distributor.

1.2 Each device works into the logic through a peripheral interface consisting of five leads. These are:

1.2.1 Message Available

When the lead is in the 0-state (low) the device is indicating to the Send Control, that it is capable of sending a message.

1.2.2 Send Message

This lead, in the 0-state, is an indication from the Send Control to the device that it was successful in obtaining sending priority.

1.2.3 Send Ready

A "low" on this lead tells the Send Control that the device is ready to start sending a message. This means that any or all functions necessary, before the device can begin sending, have been performed.

1.2.4 Present Character

When this lead is in the 0-state, the distributor is indicating to the device via the Send Control that its shift register is empty and is capable of accepting a character for distribution.

1.2.5 Character Available

This lead in the 0-state is an indication from the device to the distributor via the Send Control that a character is ready for distribution and the distributor should commence its distribution cycle.

1.3 A contention Latch (CNL) assigns sending priority to that device which first presents a Message Available indication.

1.4 There are three possible modes of operation.

1.4.1 KBD Sending "local".

1.4.2 KBD Sending "on-line".

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

1.4.3 Answer Back Sending "on-line".

1.5 This assembly provides three methods of starting the Answer Back. These are:

1.5.1 Manual Start

1.5.2 Stunt Box Operated Start

1.5.3 Automatic Start (On Line Handshake)

1.6 This assembly provides the serial EIA Signal output to the line interface unit.

1.7 This assembly contains the Proceed Lamp driver.

2. Input Characteristics

2.1 The inputs to the circuit assembly are either EIA (RS-232-B) or Nand type integrated Diode Transistor Logic (DTL) inputs. EIA inputs are defined in Electronic Industries Association Standard RS-232-B. Each DTL input is approximately 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than +6.6 volts or more negative than -.7 volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +6V and 0V respectively. A logic one (high) draws no current from the input of the logic element.

2.1.1 Keyboard Message Available (Pin B8)

This input when in the 0-state (low), is an indication from the Keyboard to the Send Control that the Keyboard is capable of sending a character. The device driving this input must be capable of sinking one DTL load.

2.1.2 Keyboard Send Ready (Pin B10)

A low on this input tells the Send Control that the Keyboard is ready to start sending a character. This lead is a turn-around of the Keyboard Send Message output (Pin B7) through the Keyboard interface card. The device driving this input must be capable of sinking one DTL load.

2.1.3 Keyboard Character Available (Pin B6)

When this input is low, the Keyboard is indicating to the distributor via the Send Control that a character is ready for distribution, and the distributor should start its distribution cycle. During normal operation this input will be low for 1 bit time before the start bit of each character. The device driving this input must be capable of sinking one DTL load.

2.1.4 Line Shift Control Sample (Pin B25)

This input is normally high and goes low .25 bits after the Keyboard Character Available goes low and remains low for .25 bits. The device driving this input must be capable of sinking one DTL load.

2.1.5 Present Next Character (Pin B34)

This input, low in the idle state, is an indication to the Send Control that the distributor's shift register is empty and capable of accepting a character for distribution. It goes high at the beginning of the start bit of each character and remains high for the duration of the character. The device driving this input must be capable of sinking one DTL load.

2.1.6 Line Tabulation (Pin B27)

This input is low throughout any tabulation function of the printer while it is "on-line" and high at all other times. It serves to inhibit "on-line" transmission during tabulation. The device driving this input must be capable of sinking two DTL loads.

2.1.7 Local Tabulation (Pin B22)

This input is low throughout any tabulation function of the printer while it is off-line (local), and high at all other times. It serves to inhibit local transmission during tabulation. The device driving this input must be capable of sinking two DTL loads.

2.1.8 Send Interrupt (Pin B31)

This input is normally high and goes low (spacing) whenever an interrupt is generated. The device driving this input must be capable of sinking one DTL load.

2.1.9 Signal Output (Line) (Pin B32)

This input is the serial signal output of the distributor during "on-line" transmission. It is high for a MARK and low for a SPACE. The device driving this input must be capable of sinking one DTL load plus the loads required for local Signal Output (Pin A32).

2.1.10 Printer Local (Pin B29)

This input inhibits the answer back from starting if the Printer receives the ENQ character, while in the local mode. It is high in the "on-line" mode and low in the "local" mode. The device driving this input must be capable of sinking the one DTL load.

2.1.11 Normalize (Pin A31)

This input is high while the printer motor is running "on-line" and is used to disable the two-second Ring Indicator timer. Normalize low enables the timer. The device driving this input must be capable of sinking one DTL load.

2.1.12 Ring Indicator (CE) (KIA) (Pin A22)

This input is normally low (0 to -25V) and goes high (+3V to +25V) every time the bell in the data set rings. It is used to condition the answer back's automatic start circuit (RIL).

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2.1.13 ENQ (S.B.) (Pin B28)

This input is normally high. It is switched low for a nominal period of 20 ms everytime the Printer receives the ENQ control character. The device driving this input must be capable of sinking one DTL load.

2.1.14 Here Is (Pin A29)

This input is normally high. Any negative transition on this input causes the answer back to start.

2.1.15 Answer Back Message Available (Pin B19)

This input behaves in the same manner as KBD MA (See Section I-2.1.1). It switches low at the beginning of a message and remains low for the entire duration of a message.

2.1.16 Answer Back Send Ready (Pin B21)

This input behaves in the same manner as KBD Send Ready (See Section I-2.1.2). It switches low at the beginning of a message and remains low for the entire duration of a message.

2.1.17 Answer Back Character Available (Pin B18)

This input behaves in the same manner as KBD Character Available (See Section I-2.1.3). It switches low at the beginning of a message and remains low for the entire duration of a message.

2.1.18 Keyboard Local (Pin B5)

This input conditions the Send Control for "line" or "local" operation of the keyboard. It is high if the KBD has been selected to send "on-line" and low if it has been selected to send locally. It inhibits locally generated data from being sent "on-line". The device driving this input must be capable of sinking two DTL loads.

2.1.19 Clear to Send (CB) (EIA) (Pin A24)

When this EIA input is high (+3V to +25V), it enables the Keyboard or Answer Back for "on-line" operation. If it is low (0V to -25V), the Contention Latch (CNL) is disabled and neither Keyboard nor Answer Back is able to operate "on-line".

2.1.20 Halt (Pin B30)

This input must be high during the time that Clear to Send is high to enable the Keyboard to send "on-line". If this input goes low and remains low during the time that the Keyboard is sending "on-line", Keyboard transmission will immediately stop. It has no effect on Answer Back operation. The device driving this input must be capable of sinking two DTL loads.

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2.2 Output Characteristics

The output from this assembly are either EIA (RS-232-B), Diode Transistor Logic (DTL), or transistor driver outputs. EIA outputs are defined in Electronic Industries Association Standard RS-232-B. DTL outputs are rated according to the number of DTL loads each can sink. Each load is approximately 1.4 ma.

2.2.1 Keyboard Send Message (Pin B7)

This output in the 0-state is an indication from the Send Control to the Keyboard, that it was successful in obtaining sending priority. This output switches low at the beginning of each character, and is capable of sinking eight DTL loads.

2.2.2 Keyboard Present Character (Pin B9)

This output, when in the 0-state, is an indication to the Keyboard that the distributor's shift register is empty and capable of accepting a character for distribution. KBD Message Available, Send Message, and Send Ready, must all be low and as long as they remain such, this output will be under the control of the Present Next Character output of the distributor. This output will sink seven DTL loads.

2.2.3 Keyboard Shift Control Sample (SCS) (Pin B3)

This output is normally high and goes low for -.25 bits after Keyboard Present Character has gone low. This output will sink eight DTL loads.

2.2.4 Line Take Character (Pin A23)

When this output switches to the 0-state, the command is from the Send Control to the distributor to commence its distribution cycle. This output switches low for one bit time before the beginning of the start bit of each character and remains low for one bit time. This output will sink eight DTL loads.

2.2.5 Send Data (EIA) (Pin A28)

This output is the serial EIA data signal. It is marking when the voltage is between 0V to -25V and spacing when it is between +3V to +25V.

2.2.6 Space On-Line (Pin A33)

This input is normally high (marking) and goes low whenever a spacing bit is generated "on-line" or "local". This output will sink eight DTL loads.

2.2.7 Mark On-Line (Pin B33)

This output is the inverse of Space On-Line (See Section I-2.2.6). This output will sink seven DTL loads.

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2.2.8 Request to Send (EIA) (Pin A34)

This EIA output is held high +3V to +25V continuously, indicating a continuous request to send to the Data Set.

2.2.9 Answer Back Start (Pin A29)

This output switching from high to low is the Answer Back start command. This output will sink seven DTL loads.

2.2.10 Answer Back Send Message (Pin B4)

This output behaves in the same manner as KBD Send Message (See Section I-2.2.1) except that it switches low at the beginning of a message and remains low for the entire duration of a message.

2.2.11 Answer Back Present Character (Pin B20)

This output behaves in the same manner as KBD Present Character (See Section I-2.2.2).

2.2.12 Proceed Lamp (Pin A27)

This output drives the Proceed Lamp located on the control strip. When this output is "on" it provides power to light the lamp indicating that the set is ready to commence sending "on-line".

2.2.13 Signal Output (Local) (Pin A32)

This output is the serial signal output from the distributor and is used for off-line (local) operation of the KSR Set. This output is driven by the distributor and has no load current sinking capability of its own.

2.2.14 Ring Indicator (Pin A26)

This output normally high, is the inverse of the EIA (CE) Ring Indicator signal on Pin A22. Data sets using a pulsed Ring Indicator will cause this lead to switch low for approximately one second, everytime the bell in the hand set rings. Data sets utilizing a continuous Ring Indicator, will cause this lead to switch low at the beginning of a call, and to remain low until the end of that call.

2.2.15 Clear to Send (Pin A21)

This output, normally high, is the inverse of the EIA (CB) Clear to Send signal on Pin A24. This output switching low at the start of a call and remaining low throughout the entire duration of a call enables on line transmission.

2.3 Mechanical Requirements

The KSR Send Control is a 5-3/4 x 4-1/4 inch 72-pin circuit card designed to mate with a standard 72-pin connector.

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2.4 Power Supply Requirements

<u>Pin</u>	<u>VDC</u>	<u>Current Maximum</u>
B1	+5.0V to +6.6V (+5.25V Nom.)	
B2	Circuit Ground	
B35	+11.65V to +13.75V (+12.5V Nom.)	
B36	-11.13V to -13.88V (-12.5V Nom.)	

2.5 Temperature Range

The ambient operating temperature range is from 0°C to 70°C.
Storage temperature range is from -40°C to +70°C.

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SECTION II



DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic drawing 322304 (MC304) and 8773WD respectively.

1.2 Logic symbols and truth table 8399WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

Refer to the 8773WD schematic and attached timing diagrams as an aid to understanding the following description.

2.2 Keyboard Local Operation

The signal exchange between the Keyboard, Send Control and Distributor occurs in the following manner. Assume that the KSR Set has been selected to operate in the local mode. Pins B5 and B29 are both low. This forces the MLE2-1 input to the Contention Latch (CNL) high. With no Clear to Send present, the ML1-11 output is low, keeping the Reset side of the latch high, inhibiting local operation of the Answer Back (Answer Back Send Message high).

The KBD Message Available, MLE2-2, input to CNL is low. Depressing a key on the Keyboard causes KBD M.A. (Pin B8) to switch low, forcing MLE2-2 to go high. Since all RESET inputs to the Contention Latch (CNL) are now high, the latch is SET and will indicate KBD Send Message (Pin B7 low). KBD Send Message, connected to KBD Send Ready (Pin B10), via the KBD interface circuit card, forces the MLB2-13 input high. MLB2 inputs 1 and 2 both high, indicate that no tabulation function is in process and that the distributor's shift register is empty and ready to accept a character for distribution. Consequently, since all inputs to MLB2-12 are high, KBD Present Character (Pin B9) will switch low, forcing MLE1-3 to remain high even if KBD Message Available should revert high, thereby keeping the KBD Send Message output low until the CNL is RESET.

A KBD Character Available indication received from the KBD on Pin B6 causes KBD Take Character (Pin A23) to go low. Take Character low causes the distributor to start its distribution cycle. One bit time later, the distributor will remove PNC (Pin B34 high) indicating that the character has been taken. PNC remains high until the character has been shifted out of the distributor's shift register, at which time it will revert low and wait for the beginning of the next character.

PNC going high causes MLB2-2 to go low, forcing KBD Present Character high enabling MLE1-3 to revert low at the end of the KBD message available indication. The KBD Present Character output is returned

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to the KBD Character Available input (Pin B6 goes high) via the keyboard interface card and if Answer Back Character Available (Pin B18) is also high, the Take Character output (Pin A23) will switch high, thus preventing the distributor from starting another cycle.

Shift Control Sample (Pin B25) is an input coming from the distributor (low for .25 bit, .25 bits after Take Character has switched low) which is routed to the Keyboard interface card by way of MLA2-6 and 8 and output Pin B3 (KBD Shift Control Sample).

2.3 On-Line Operation

The signal exchange between the Keyboard, Send Control and Distributor during "on-line" operation is the same as that previously discussed for "local" operation. In this case, either the Keyboard or Answer Back is able to send on-line provided that MLA1-11 is high (CTS present) and MLE1-6 is high (Proceed indication from MLA2-2 low). There is no local mode for the Answer Back and it will receive an AB Send Message (Pin B4) whenever all inputs to MLE2-8 are high. If CTS is not present, the Contention Latch (CNL) will be disabled, due to lows on MLE2-11 and MLE2-1, and neither KBD nor Answer Back will be able to transmit "on-line". A Halt indication (Pin B30 low) will stop "on-line" transmission from the Keyboard by preventing KBD Send Message from switching low during the entire time the Halt indication is present. The MLA2-2 and MLE1-6 gates which force a low at the MLE2-1 input to the Contention Latch (CNL) during a Halt indication do not affect "on-line" operation of the Answer Back because the MLE2-11 input to the latch remains high as long as a CTS indication is present.

With the Keyboard "on-line" (Pin B5 high), Clear to Send present (+EIA), and no Halt indication (Pin B30 high), all inputs to the Contention Latch (CNL), except the two inputs coming from the M gates (MLE1-3, MLC2-6) will be high. In this condition the set and reset sides of the CNL Latch are both high and ready for a Message available signal from either the Answer Back or Keyboard. If KBD Message Available occurs, first, the Keyboard has control and an Answer Back Message Available on MLE2-10 cannot affect the present state of the latch until KBD Send Message reverts high. If the Answer Back had sent the first Message Available, the KBD Send Message would have been disabled (MLE2-13 low) until Answer Back Send Message returned high.

2.4 Transmitter Stop

During tabulation, Line Tab (Pin B27) switching low at any time during the course of an "on-line" message, indicates that a Printer tabulation function is in process and will stop the line transmitter while it is low, by disabling the Present Character to the Keyboard or Answer Back by means of either input MLB2-1 or MLB2-4 respectively. A local tabulation indication (low) on Pin B22 performs the same function of stopping the KBD during local operation (Answer Back is never allowed to operate in the "off-line" mode).

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2.5 Answer Back Start Logic

The Answer Back can be started in any one of three ways, taking the first step of its cycle when a high to low transition appears on Pin A29.

2.5.1 Manual Start

The Answer Back is started manually by depressing the "Here Is," Switch located on the control panel. This action due to gates MLD1-6, MLD1-11 and components R26 and C6 is transformed into an approximately 1 millisecond long negative pulse into the set side of the Ring Indicator latch (RIL), setting the reset side of the latch high. The reset side of the RIL latch gated together with the CTS signal, which is a high on ML1-3. This negative pulse, used to trip off the Answer Back, is formed by the RIL latch being reset approximately 1 milliseconds after it was set.

2.5.2 Stunt Box Operated Start

The Answer Back can also be started by operation of the Printer ENQ stunt box contact. For this to occur the Printer must be in the "on-line" mode, MLB2-9 input high, and the Line TC must be idle (no "on-line" transmission in process) keeping the MLB2-11 input high. Should the Printer now receive the ENQ character, the ENQ contact will close for approximately 20 ms forcing the MLB2-10 input high via MLC2-3, making the MLB2-8 output low, thereby starting the Answer Back.

The purpose of gating the set side of the Character Sent latch (CSL) with the inverse of the ENQ stunt box closure, is to prevent starting one's own Answer Back whenever the ENQ character is sent on line. This is accomplished by Line TC setting the set side of the CSL latch low for a period of 250 milliseconds from the beginning of the start bit of the ENQ character. The stunt box closure occurring 14 to 15 bits after the negative transition of the start bit is unable to cause MLB2-8 to go low, because the MLB2-11 input is keeping it high. The 250 millisecond time interval is the period of the CSL Reset timer, which resets the CSL latch at the end of its cycle.

2.5.3 Automatic Start

The Answer Back automatic start logic consists of the Ring Indicator latch (RIL) formed by MLD1-8 and MLE1-11, which is controlled by RI and the RIL Reset Timer. The circuit functions in the following manner. In the OFF state RI (CE), normalize and CTS (CB) are all low. The timer is not running and the RIL latch is reset keeping ML1-3 high. RI (CE) going high starts the timer by switching the reset side of the RIL latch high. ML1-3 remains high because CTS (CB) is still low at this time, keeping ML1-2 low by way of ML1-11. Normalize must switch high within 2 seconds after RI (CE) switched high for the RIL latch to remain in its present state. If normalize does not switch high within the specified time, the RIL reset timer will run its full 2 second cycle resetting the RIL latch, thereby preventing the CTS (CB) signal from starting the Answer Back.

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2.5.3 (Continued)

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Assume the RIL latch remains set. CTS (CB) switching high results in a negative pulse at ML1-3. This negative pulse which starts the Answer Back is formed by the RIL latch being reset approximately 10 microseconds after CTS (CB) switched high. The 10 microsecond delay on reset is accomplished by the integrating network consisting of R25 and C9.

2.6 RIL and CSL Reset Timers

These timers are conventional unijunction (UJT) relaxation oscillators, with periods of 2 seconds and 250 milliseconds respectively.

The RIL Reset Timer functions in the following manner. Whenever ML1-11 is high, transistor Q9 is on and capacitor C12 is charged to +12.5V holding the emitter of the UJT at ground potential. ML1-11 switching low, turns off transistor Q9, which in turn allows C12 to discharge through R18 causing the voltage at the emitter of the UJT to rise exponentially toward +12.5V. When this voltage reaches a value V_p (characteristic of the UJT $V_p = n V_{BB} + V_D$) the UJT will fire and the C12 charging current through R11 will produce a positive spike at B1 of the UJT. This spike is inverted by ML1-3, resetting the RIL latch, forcing ML1-11 high thereby disabling the timer.

The CSL Reset Timer functions in exactly the same manner in conjunction with the Character Send Latch (CSL). The only difference is in the values of C11 and R33 which establish the desired time constant.

2.7 EIA Input Amplifiers

EIA input amplifiers, such as those which route RI and CTS onto the card, are common emitter amplifiers which convert EIA voltages ranging from +3 to +25V volts to a DTL low (0 volts) and EIA voltages ranging from 0 to -25 volts to a DTL high (+Vcc). Thus there is a logic inversion when a signal passes through an EIA input amplifier (an EIA high is a DTL low and an EIA low is a DTL high). In the EIA RI amplifier, R21 is a base current limiting resistor, which presents an input impedance of 4.7K ohm to the device driving this input. Diode CR1 prevents an excessive V_{BE} from damaging Q10. R2 reduces the effects of collector to base leakage and improves switching time. R20 is the collector load resistor.

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2.8 Line Data Amplifier (EIA)

The serial signal output of the distributor, which is high for a MARK and low for a SPACE, is monitored by Pins A32 and B32. ML1-6 inverts this signal, before it is used, to drive the EIA Signal output amplifier, consisting of Q3 and Q5. The amplifier output on Pin A28 is an EIA voltage as described in EIA Standard RS-232-B. It is low (0 to -25V) for a MARK and high (+3V to +25V) for a SPACE. The other input (Pin B31) to ML1-6, monitors the Send Interrupt signal, which is a nominal 250 ms of continuous space. ML1-3 inverts the signal input to the EIA output amp. Its output on Pin A33 is an exact duplication of either signal input to ML1-6.

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2.8 (Continued)

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The ML1-6 output brought out on Pin B33 is the inverse of either signal input to ML1-6. Locally generated Keyboard data cannot be sent "on-line" because KBD "local" (low on Pin B5) keeps the line Data Amp marking by means of R7 connected to the base of Q3.

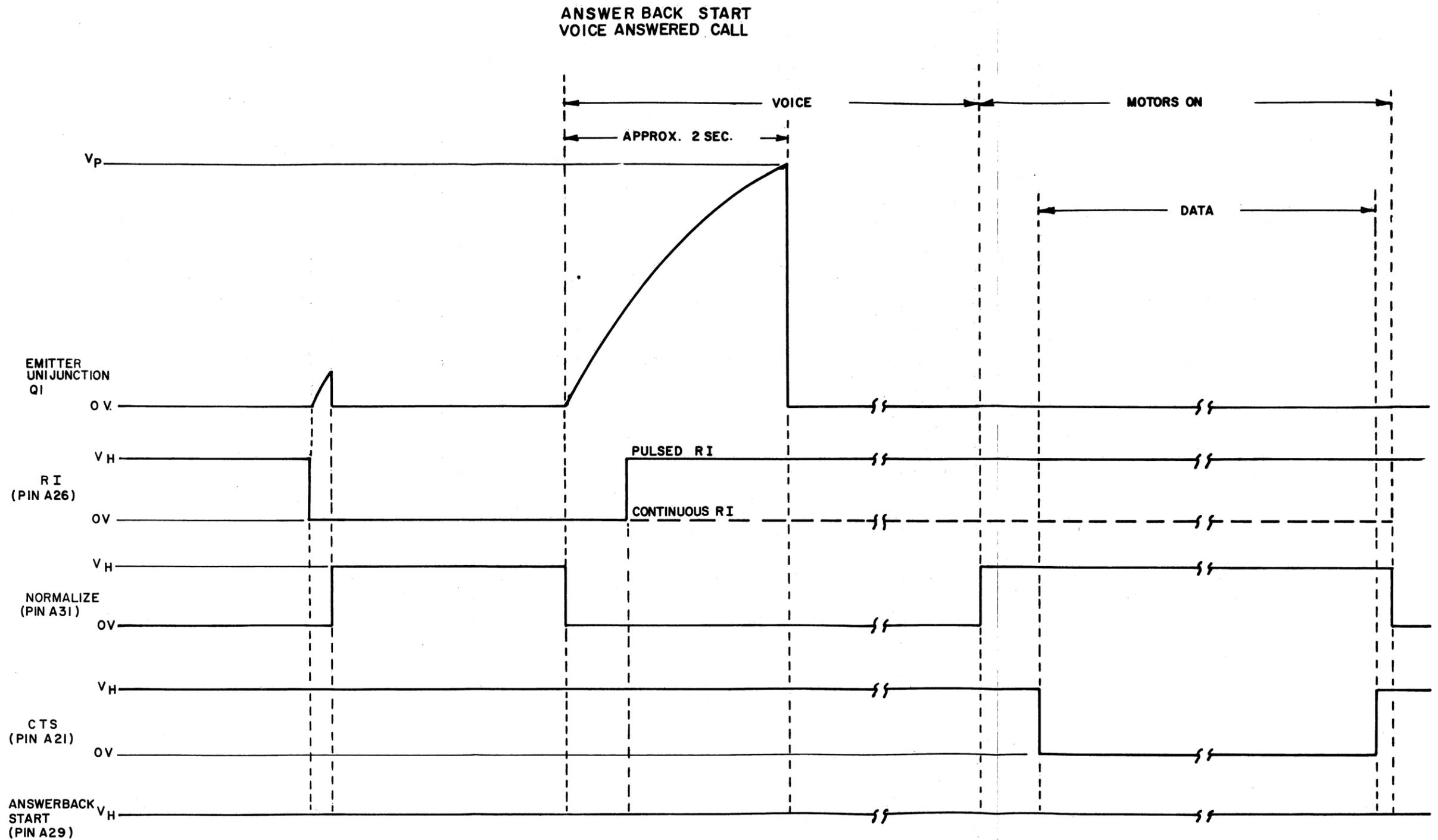
2.9 Proceed Lamp Amplifier

The Proceed Lamp Amplifier consisting of Q4 and Q7 is driven via ML1-8 and inverter ML2-2. The amplifier is used to light the "Proceed" lamp located on the control strip, by applying approximately 24 volts across the lamp through R35, a current limiting resistor. Any time a CTS indication is present, the ML2-2 output will be low, turning the amplifier "On", thereby lighting the "Proceed" lamp. A "Halt" indication (low on Pin B30) will force ML2-2 high and turn the "Proceed" light off.

2.10 The integrating networks throughout the card are for noise protection.

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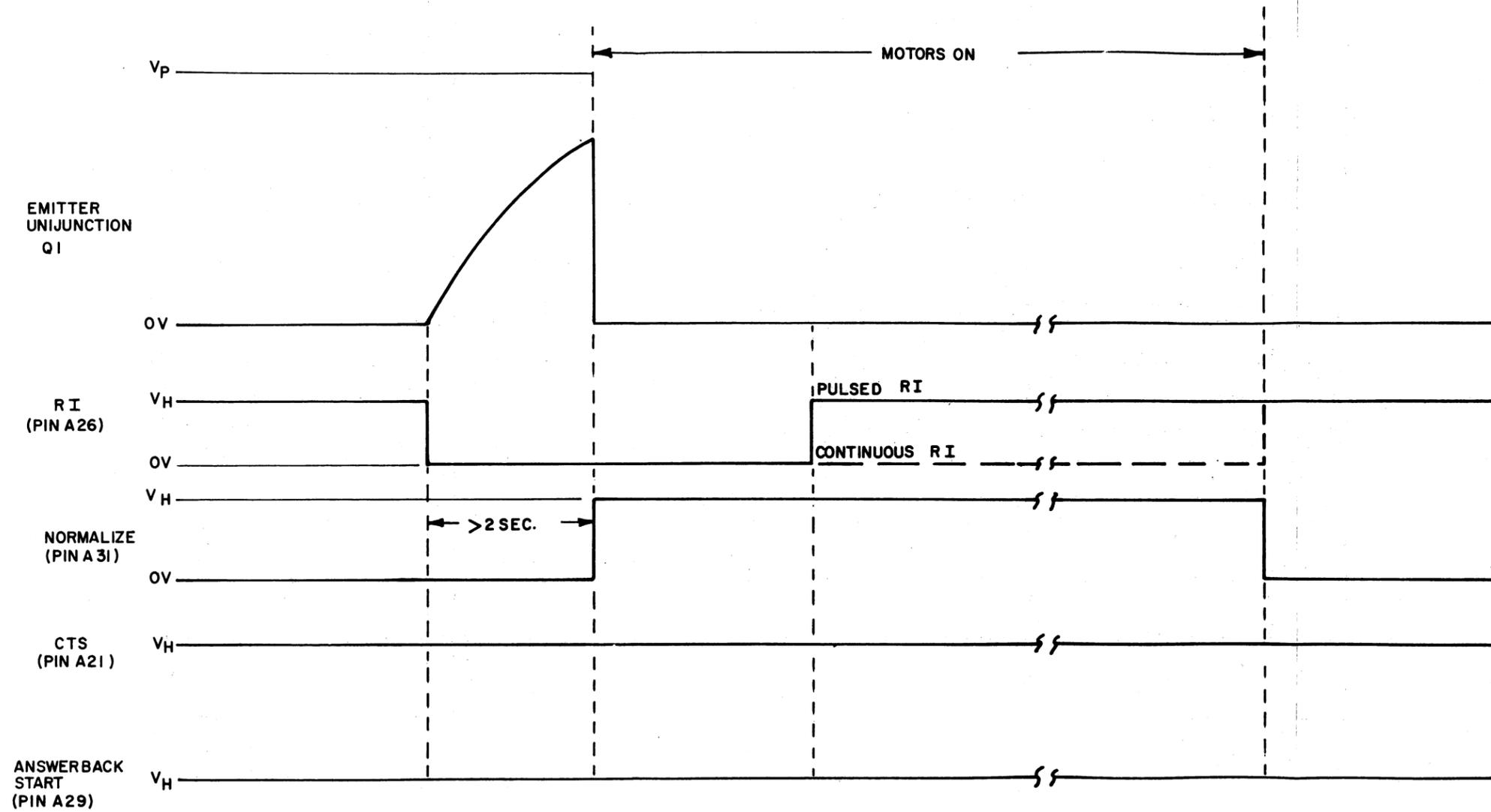
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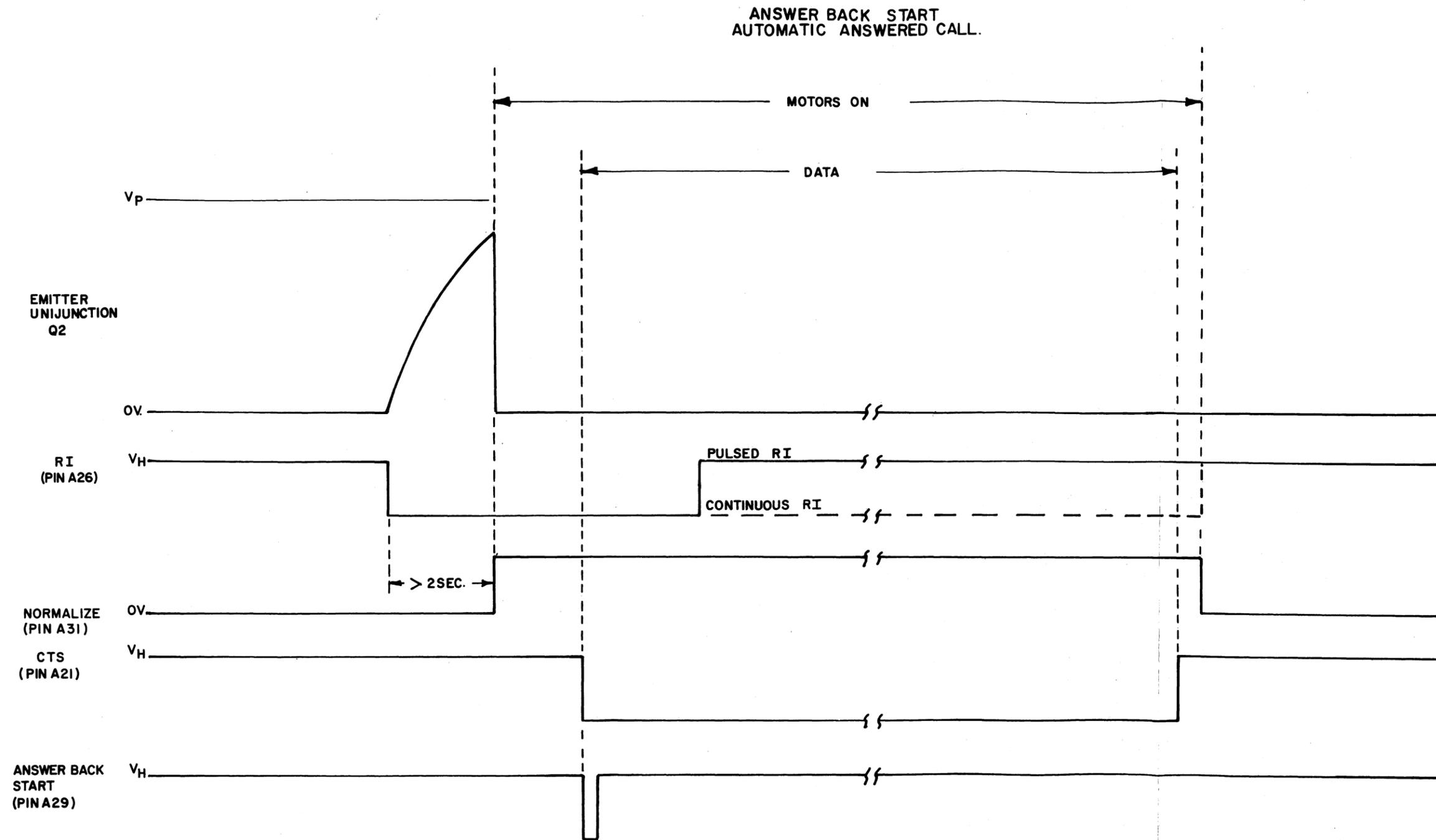
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W.D.

ANSWER BACK START
AUTOMATIC ANSWERED CALL
NO CLEAR TO SEND



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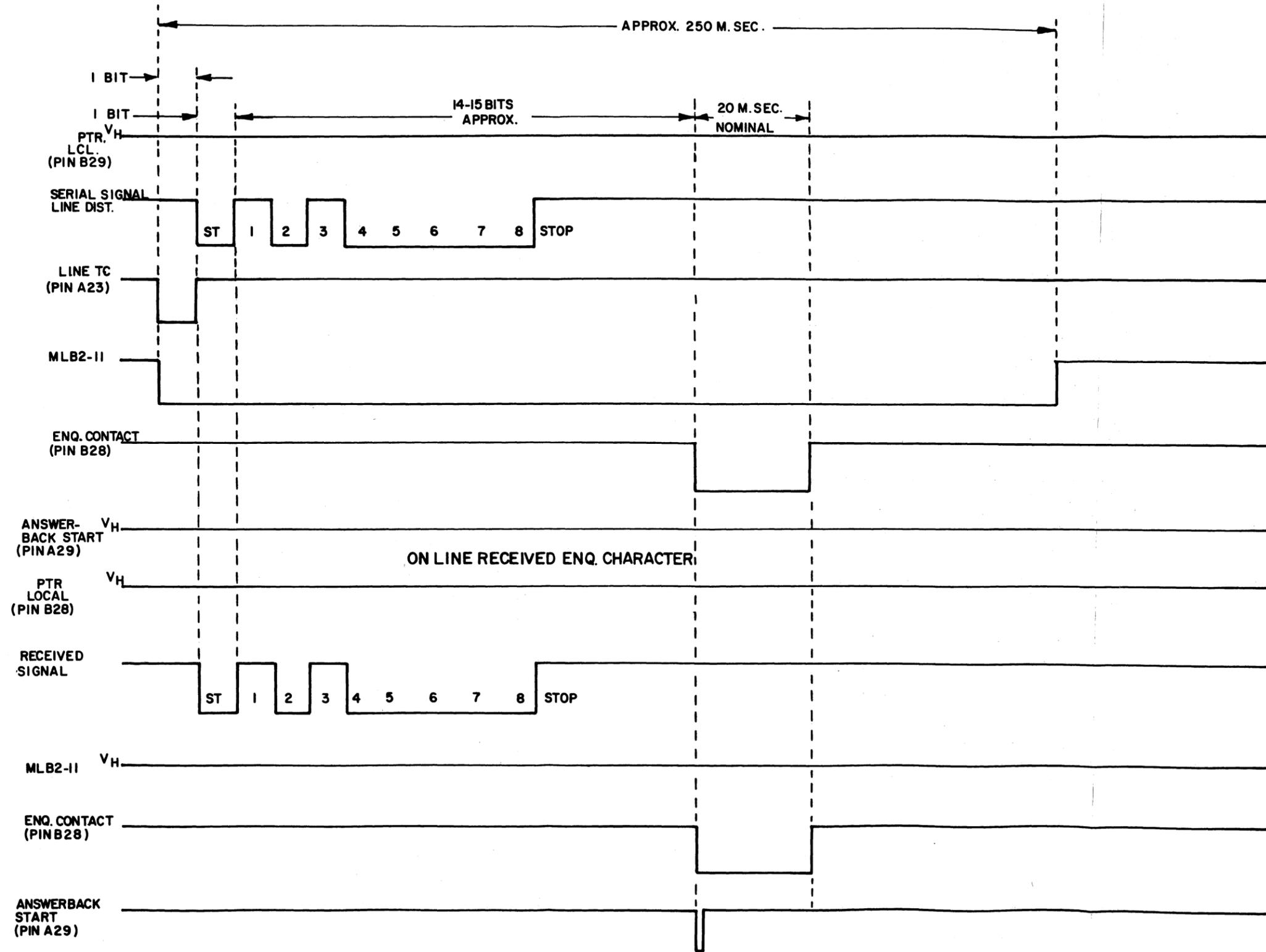
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ON LINE GENERATED ENQ. CHARACTER.



ON LINE RECEIVED ENQ. CHARACTER.

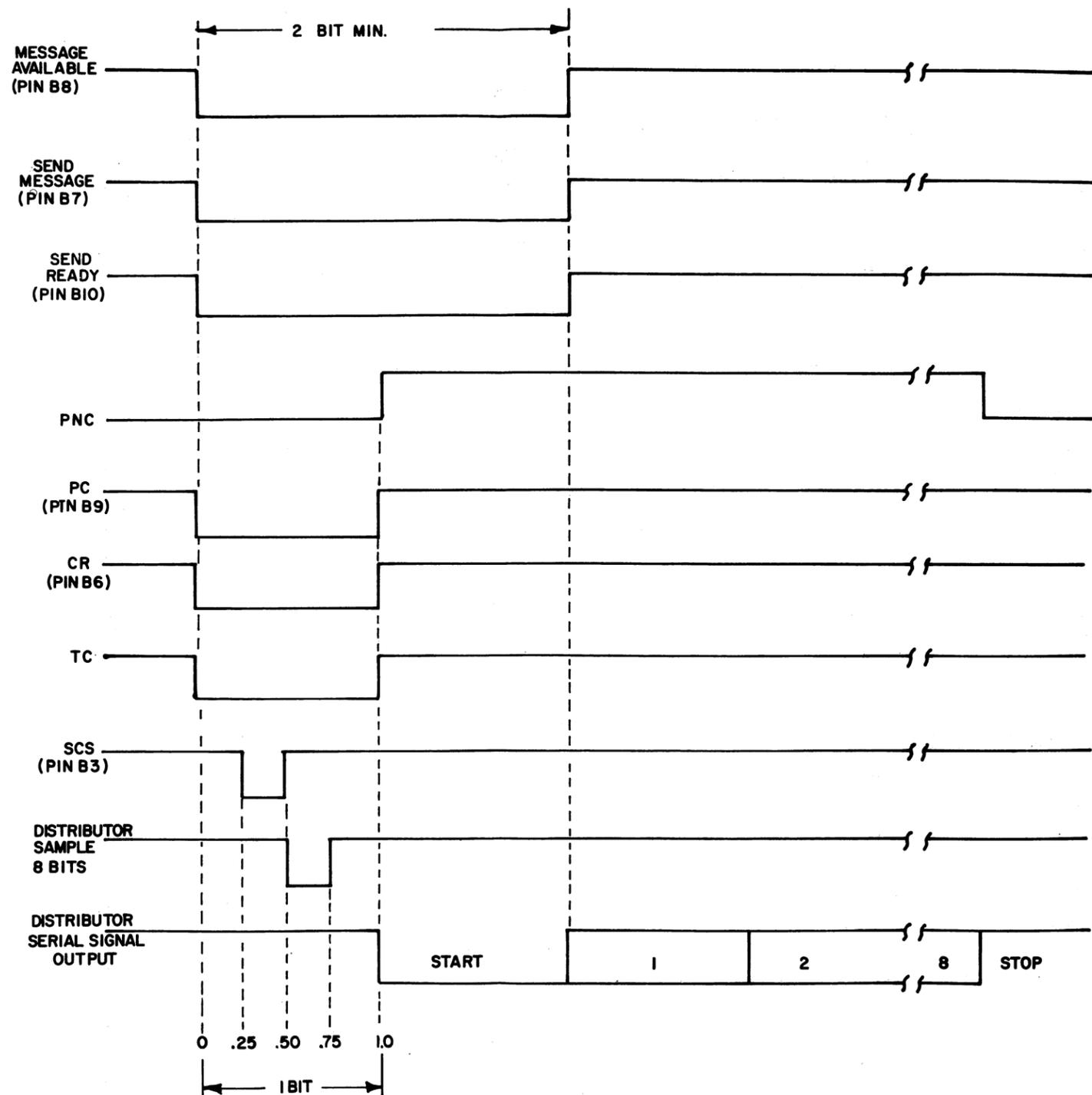
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KEYBOARD LINE OR LOCAL OPERATION



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CIRCUIT DESCRIPTION OF KEYBOARD CONTROL LOGIC
(ASSEMBLY NUMBER 322044)

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CIRCUIT DESCRIPTION OF KEYBOARD CONTROL LOGIC
(ASSEMBLY NUMBER 322044)

SECTION I

1. BASIC FUNCTION

1.1 The 322044 Circuit Card Assembly used in the Model 37 Service Unit converts the keyboard parallel input information levels (bits) to eight parallel output information levels (bits) representing USASCII characters. The card is capable of generating 128 distinct characters. These include 95 graphic characters, 32 control characters, and the delete character.

1.1.1 Provisions are made for "piggy back" mounting of the "Character Counter" Logic Card (322045) for specific ASR applications.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the assembly are obtained from the keyboard contacts referenced to circuit ground. Each DTL input is a nominal 3.2 ma load on the signal source or contact.

2.1.1 Data Input (Pins 3,4,14,13,12,11,8,7)

The data inputs, bits 1 through 8, consist of MARKS or SPACES. The input logic levels are defined by using negative logic. That is, a MARK is a logic voltage level between circuit ground and +0.5 volts (low). A SPACE is a logic voltage level between +5.0 volts and +6.6 volts (high).

The KEYBOARD CONTROL, SHIFT INHIBIT, and SHIFT inputs are defined by using negative logic. A closed contact is referenced to circuit ground and is considered a logic one. An open contact is referred to the nominal 5.25 volt supply through a 3.6K ohm pull-up resistor and is considered a logic zero.

2.1.2 Keyboard Control (Pin 16)

The device driving this input must be capable of sinking 2 DTL loads (1 DTL load = 1.4 ma). This input is normally "low" except when generating control characters on keys which can perform other functions (EOT, ENQ).

2.1.3 Shift Inhibit (Pin 15)

The device driving this input must be capable of sinking 2 DTL loads. This input is normally high except when generating control characters on keys which can perform no other function and characters which are not affected by shift to upper case.

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2.1.4 Shift (Pin 29)

The device driving this input must be capable of sinking 2 DTL loads. This input is low when generating the lower case keyboard characters, high when generating upper case characters, and high or low when generating control characters.

2.1.5 Present Character (Pin 21)

The device driving this input must be capable of sinking 1 DTL load. This input is normally "high" when the machine is idle and goes "low" for 1 bit time when a character is generated.

2.1.6 Shift Control Sample (Pin 23)

The device driving this input must be capable of sinking 1 DTL load. This input is normally high when the machine is idle and goes "low" .25 bit after PC and remains low for .25 bit.

2.1.7 Message Available (Pin 25)

A KEYBOARD AUX. closure connects Pins 25 and 26. This action generates a "MESSAGE AVAILABLE" signal which is sensed by the SEND CONTROL.

2.1.8 Keyboard Aux. N.O. (Pin 26)

The KEYBOARD AUX. normally open contact closes when a character is generated and is high at all other times. This contact closure initiates the movement of data from the card input to card output.

2.2 Output Characteristics

The outputs from this assembly are all Diode-Transistor Logic (DTL) type outputs. Output current sinking and fan out capability can be determined from the Manufacturers Specifications.

2.2.1 Data Output (Pins 6,5,10,9,18,19,20,17)

These outputs are capable of sinking approximately 16 ma each. The data output pins will be "high" (MARK) when Pin 21 is "high" and will be "high" (MARK) or "low" (SPACE) when Pin 21 and 23 are low, depending upon the character generated.

2.3 Character Counter Inputs

The 322045 Character Counter, when used, obtains its data inputs (bits 1 through 8) from those pins suffixed with an "M" (see schematic 8874 WD).

The Character Counter outputs STEP FORWARD, STEP REVERSE and RESET, enter the Keyboard Control Logic card on Pins 48, 46 and 47 respectively,

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

and leave via Pins 32, 34 and 33 respectively. For further information refer to schematics 8374 WD, 8375 WD and 8380 WD.

2.4 Mechanical Requirements

The 322044 Card Assembly is a standard 5-3/4 inch by 4-1/4 inch 36-pin circuit card which is inserted into a 36-pin edge card connector.

2.5 Power Supply Requirement

<u>Vcc (DC)</u>	<u>Current (ma) Max.</u>
+5.0 Volts to +6.6 Volts	175 ma
* -11.13 Volts to -13.88 Volts (12.5V Nom.)	20 ma

* Not required for card tests, but required for operation in Model 37.

2.6 Temperature Range

The operating temperature range is from 0°C to 70°C in free air. The storage temperature range is from -40°C to +70°C.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SECTION II

DETAILED DESCRIPTION AND THEORY OF
OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic drawing 322044(MC044)and 8374 WD, respectively.

1.2 Logic symbols and truth tables 8399 WD.

1.3 8375 WD and 8380 WD (Character Counter).

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

Refer to the 8374 WD schematic, attached timing diagrams, and USASCII Code Chart as an aid in the following discussion.

Timing Diagram 1 is representative of the timing MARK-SPACE sequence involved in getting a data bit to the Model 37 electronic distributor for a lower case "a". Timing Diagram 2 shows the general timing sequence for any USASCII character generated. Timing Diagram 3 shows the general timing sequence for proper card operation.

2.2 Operating Sequence

When the keyboard is idle, bits one through eight are marking. Assume that the lower case "a" bit sequence has just been keyboard generated. The chart below shows the logic input states. (Refer to USASCII code chart).

INPUT DATA BIT	PIN NUMBER	*BIT LEVEL
b1	3	MARK
b2	4	SPACE
b3	14	SPACE
b4	13	SPACE
b5	12	SPACE
b6	11	MARK
b7	8	MARK
b8	7	MARK

NOTE: REVISION INFORMATION MUST BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

FUNCTION	PIN NUMBER	*LOGIC LEVEL
CONTROL	16	1
SHIFT	29	1

* Logic Level 1 = Bit Level Mark = Circuit Ground

Logic Level 0 = Bit Level Space = Supply Voltage (Vcc)

Output data bits one through four (Pins 6, 5, 10, 9) are still "MARKING" because the associated output gates have not been enabled by the "PRESENT CHARACTER" (PC) gate signal. Effectively, input data bits 1 through 4 are waiting at the input of their respective output gate (MLF3-9, MLF3-12, MLF3-2, MLF3-5) for the gate signal which allows them to appear at the output.

Output data bits 5 through 8 are still "MARKING" because the associated output gates have not been enabled by the PC signal. Input data bits five through eight are at their respective latch driver inputs (MLE1-10, MLF1-12, MLF2-10, MLE2-12) waiting for the "SHIFT CONTROL SAMPLE" (SCS) gate signal.

The CONTROL, SHIFT INHIBIT, and SHIFT signals are waiting at their respective latch driver inputs for the SCS gate signal.

KEYBOARD AUX. N.O. contact closes when a bit sequence is generated. This action connects Pin 26 to Pin 25. With Pin 25 "low", a PRESENT CHARACTER gate signal is generated by the send control card. This signal causes MLC3-8 to go "high" and gate bits 1 through 4 to the output pins. Bit 1 is "MARKING". Bits 2, 3 and 4 are "SPACING". The PC input (Pin 21) remains "low" ¹⁵² for one bit time. This action primes the bit latches for SCS input. The SCS input goes "low" .25 bit after PC and remains "low" for .25 bit. The latch drivers are enabled and bits 4 through 8 appear at the output. Bit 5 is "SPACING". Bits 6, 7 and 8 are marking. Bits 1 through 8 have been transmitted to the card outputs and can be entered into the electronic distributor shift register. At .5 bit time the distributor samples the output data bits and enters the data bits into the shift register.

The chart below shows the state of the output data bits just prior to distributor sampling.

OUTPUT DATA BIT	PIN NUMBER	*BIT LEVEL
b1	6	MARK
b2	5	SPACE
b3	10	SPACE
b4	9	SPACE
b5	18	SPACE
b6	19	MARK
b7	20	MARK
b8	17	MARK

* MARK = Logic 1 = Supply Voltage (Vcc)

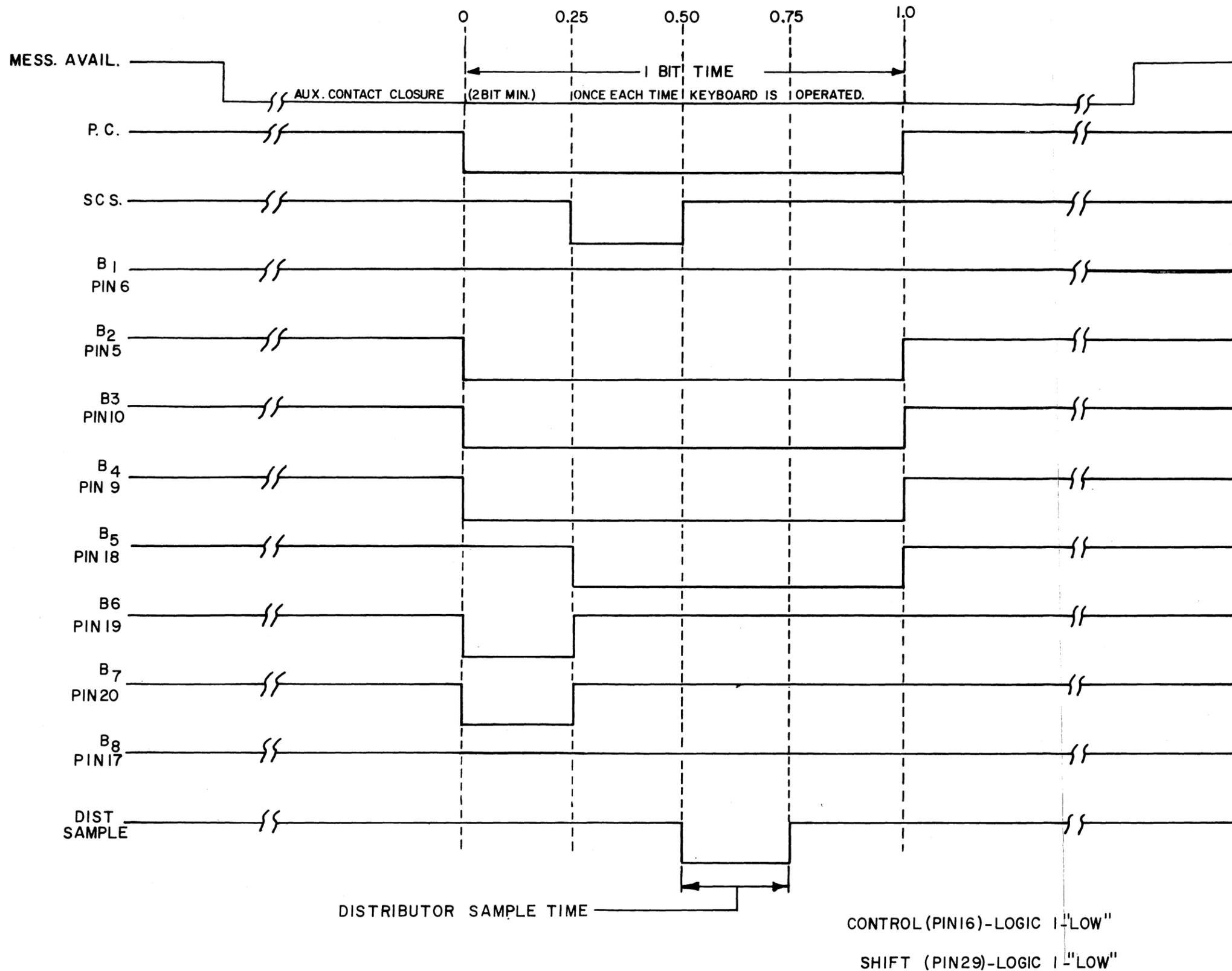
* SPACE = Logic 0 = 0 - +0.5 Volts

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

At 1 bit time, the PC and MESSAGE AVAILABLE inputs go "high". This action resets the outputs of bit latches 5 through 8 (MLE1-6, MLF1-6, MLF2-6, MLE2-6) "low". MLB2-6 and MLC2-6 are also reset to the "low" state. MLF3-10, MLF3-13, MLF3-1, MLF3-4, MLD3-9, MLD3-5, MLD3-2, MLD3-12 are brought "low" by a "high" PC input. Bits 1 through 8 are all marking and the logic is idle.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

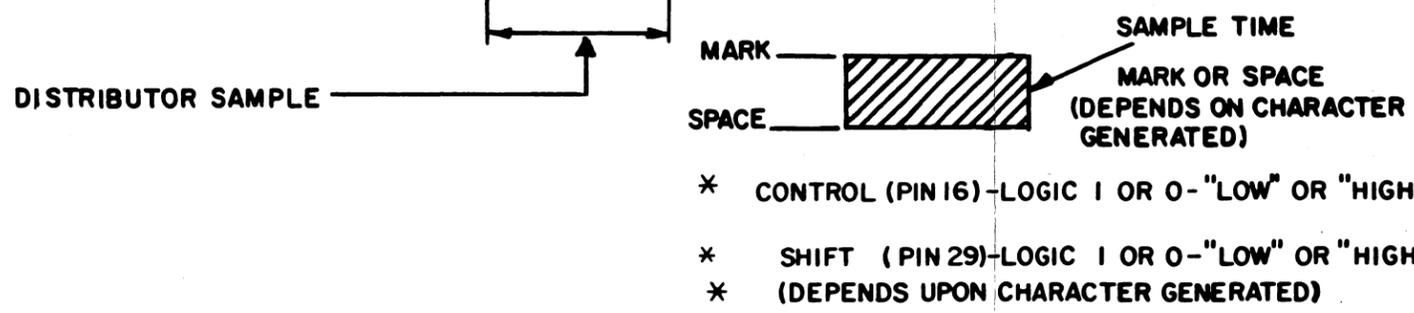
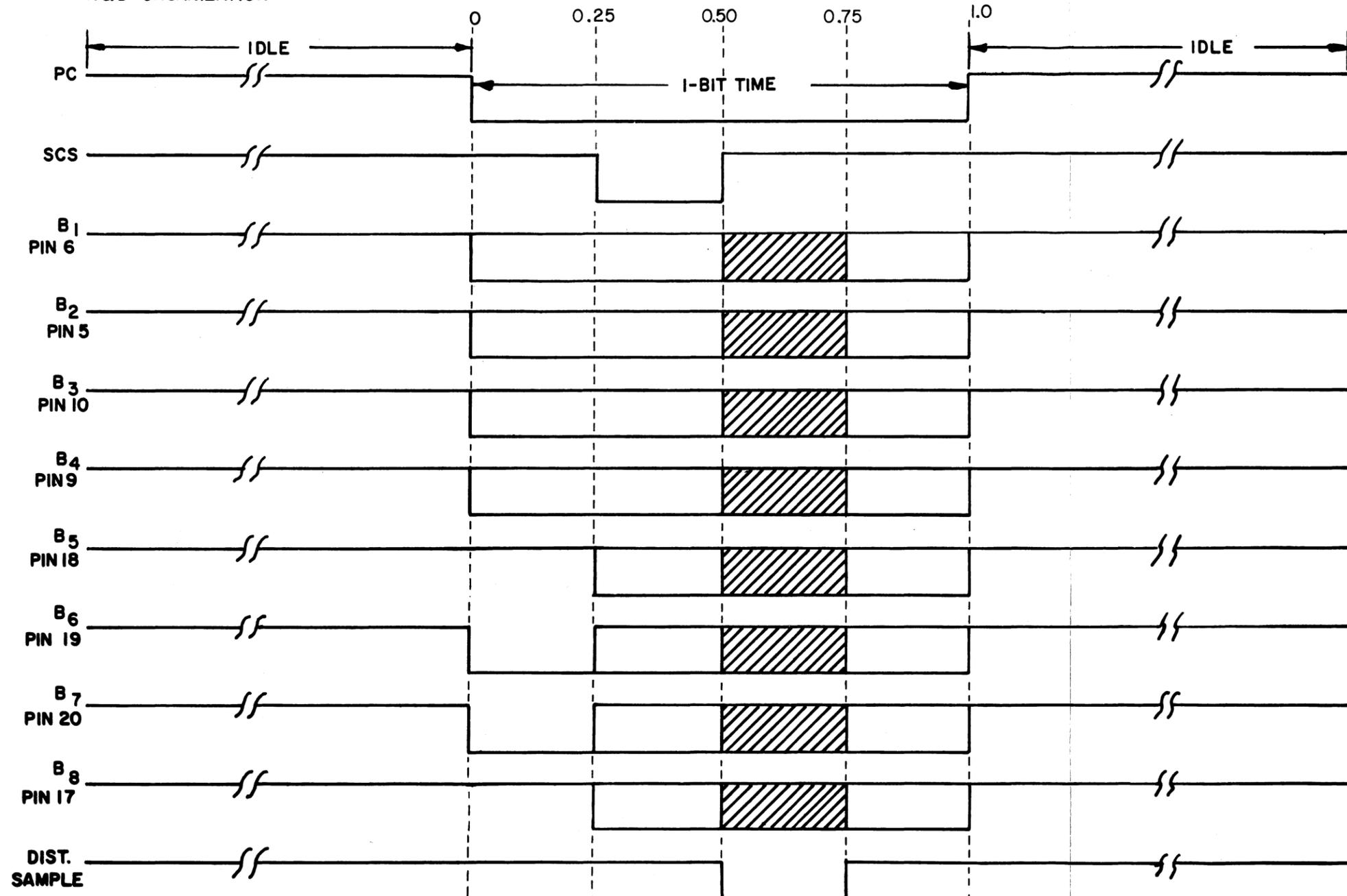


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MODEL 37 TIMING DIAGRAM-1
(LOWER CASE "a" CHARACTER GENERATION)

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

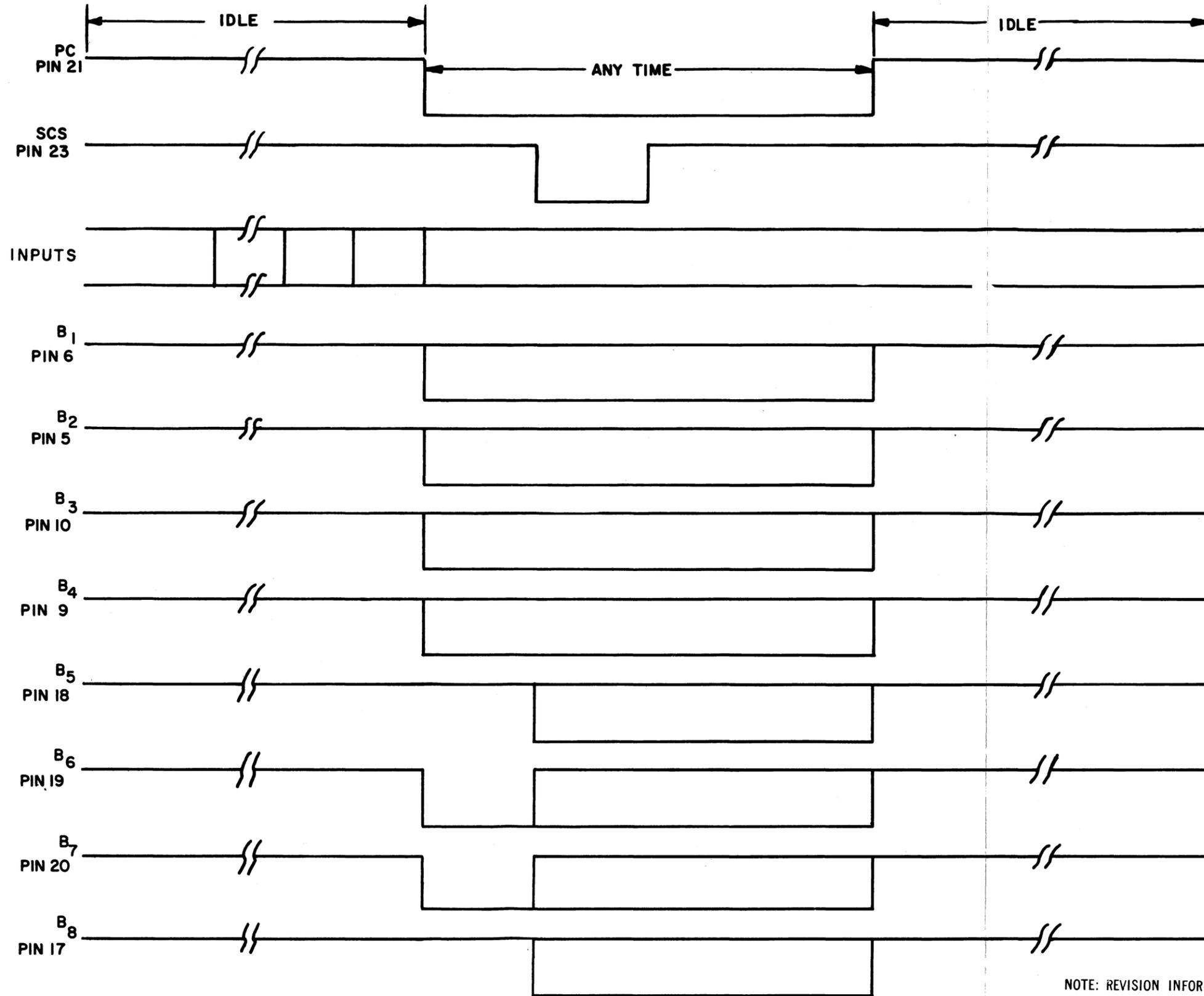
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.



MODEL 37
GENERAL TIMING DIAGRAM - 2

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.



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GENERAL TIMING DIAGRAM - 3

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

8376WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	1-3-69	96485
3	2-27-69	96898

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET-1

ANSWER BACK DRIVER

APPROVALS

D AND R	E OF M
<i>HJK</i>	<i>[Signature]</i>

E-NUMBER

PROD. NO. 8376 WD

DATE 4-8-68

P.D. FILE NO. G-A354AA

DRAWN W.P.B.

CHKD. *[Signature]*

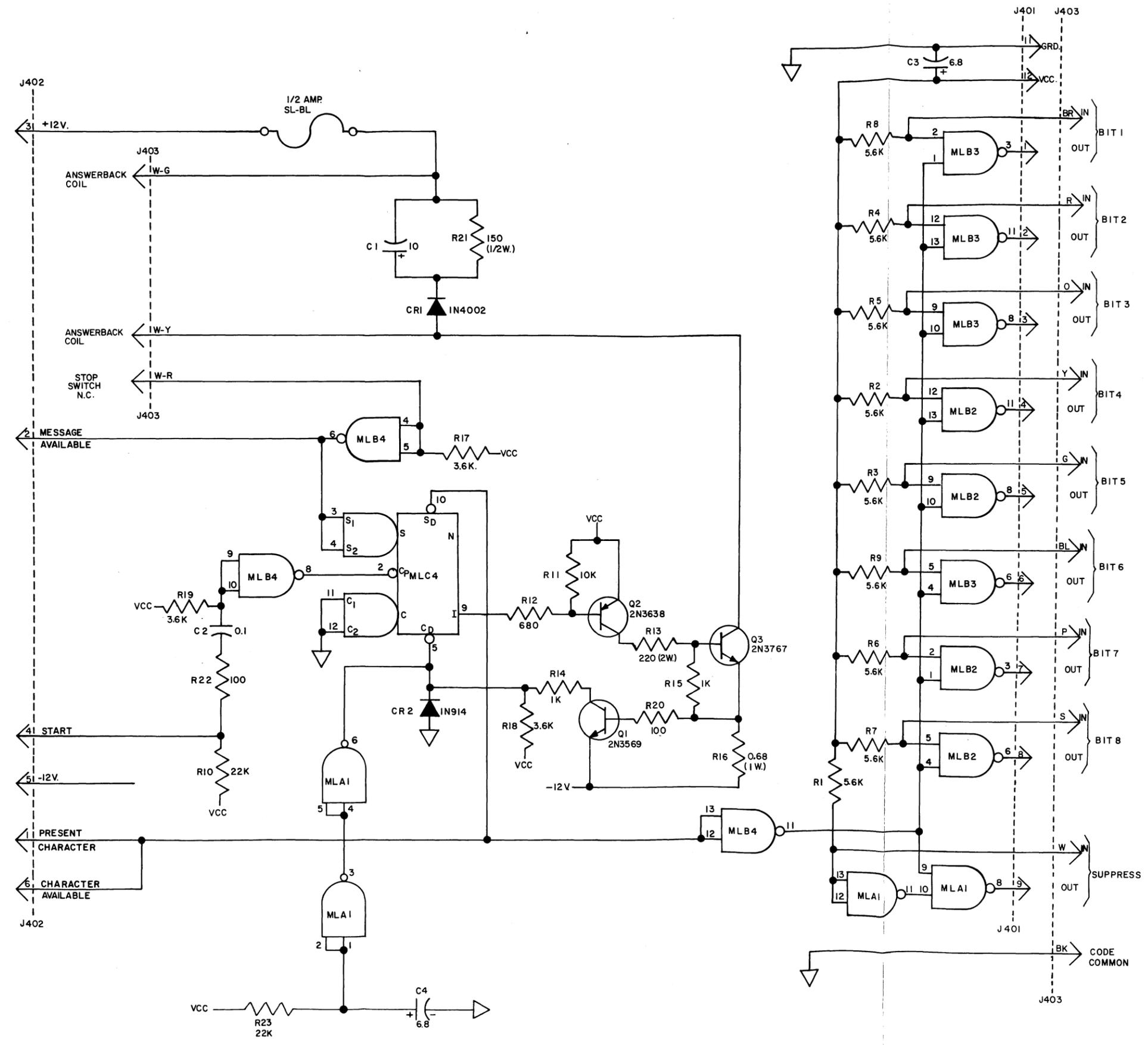
ENGD. A.B.

APPD. *[Signature]*

TELETYPE CORPORATION

8376WD

- | NO. | NOTES |
|-----|---|
| 1. | ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED. |
| 2. | ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED. |
| 3. | ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED. |
| 4. | <ul style="list-style-type: none"> —○— INDICATES FEMALE AND —→ INDICATES MALE TERMINALS |
| 5. | REFER TO 322047 FOR ASSEMBLY INFORMATION. |
| 6. | S NUMBER 61,429 S. |
| 7. | INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD. |
| 8. | LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION. |
| 9. | WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USE AS AN INVERTER. |
| 10. | VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14, AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES. |
| 11. | THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY. |
| 12. | REFER TO 8399WD. FOR TRUTH TABLES. |
| 13. | COLOR CODE LEGEND: |
| 14. | REFERENCE CIRCUIT DESCRIPTION 8376WD-CD |
| 15. | ↓ INDICATES CIRCUIT GROUND. |



CIRCUIT DESCRIPTION OF THE ANSWER BACK DRIVER CARD
(ASSEMBLY NUMBER 322047)

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<u>SECTION</u>	<u>DESCRIPTION</u>	<u>TOTAL PAGES IN SECTION</u>
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II	Detailed Description and Theory of Operation	2

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION FOR THE ANSWER BACK DRIVER CARD
(ASSEMBLY NUMBER 322047)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322047 Circuit Card Assembly is the electronic circuit portion for the 327801 Answer Back Assembly. The card contains logic necessary for the data outputs, and the logic required to drive the answer back coil. It is mounted to a plate with two circuit card clamps.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the circuit assembly are of two types: Nand type integrated Diode Transistor Logic (DTL) and contact inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of the DTL inputs be more positive than 8 volts or more negative than -.7volt.

2.1.1 Present Character (Pin 1, J402)

The Present Character input controls the read-out of the data bits and initiates the timing to step the answer back drum to the next position. When this lead reverts to the 0-state, the answer back begins to step and the data leads are sampled. The device driving this input must be capable of sinking three DTL loads.

2.1.2 Data Inputs (Color BR, R, O, Y, G, BL, P, S, W)

These inputs are connected to the data contacts 1 through 8 and the suppress contact which ride the answer back drum. A contact closure is defined as a MARK while a contact open is defined as a SPACE. A closure on the Suppress input produces a suppression command. These contacts must be capable of sinking two DTL loads.

2.1.3 Start (Pin 4, J402)

An 0-state on this lead produces the pulse necessary to start the answer back cycle. The device driving this input must be capable of sinking two DTL loads.

2.1.4 Code Common (Pin BK)

This input is the common contact for the answer back code contacts. The lead connects to the circuit board ground lead.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.1.5 Stop Switch (Pin W-R)

This contact input from a switch is closed when the answer back drum is in its home position. This switch must be capable of sinking two DTL loads.

2.2 Output Characteristics

The outputs from this assembly are Nand type integrated Diode Transistor Logic (DTL) outputs unless otherwise specified. The outputs will be rated by the number of DTL loads which may be driven. (Each DTL load is approximately 1.4 ma.)

2.2.1 Message Available (Pin 2, J402)

This output, when in the 0-state, indicates that the sending device is selectable and has a message. It is capable of driving seven DTL loads.

2.2.2 Character Available (Pin 6, J402)

This output is a turn-around of the present character input. It indicates that a character is present and should now be taken. This lead is capable of sinking three loads less than the capability of the present character input.

2.2.3 Data Outputs (Pins 1,2,3,4,5,6,7,8,9 of J401)

These outputs present the MARK or SPACE bit information of a character to external logic. A 1-state indicates a MARK while a 0-state indicates a SPACE. A SUPPRESS command is indicated by a 0-state. Each output is capable of driving eight external DTL loads.

2.3 Miscellaneous Requirements

2.3.1 Power Supply Inputs

Integrated Circuit Voltage and Current.

<u>Pin</u>	<u>V_{DC}</u>	<u>I Max. (MA)</u>
J401-12	+5V to +6.6V	110
J401-11	GND	

Coil Voltage and Current.

<u>Pin</u>	<u>V_{DC}</u>	<u>I Max. (MA)</u>
J402-3	+12	1.2
J402-5	-12	1.2

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.3.2 Operating Temperature Range

0°C to 70°C (free air).

2.3.3 Storage Temperature Range

-40°C to +70°C.

2.4 Size

The card size is 4 inches by 4½ inches.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly Drawing 322047 (MCO47) and Schematic Drawing 8376 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

The answer back assembly consists of a mechanical mechanism and an electronic circuit. The mechanism contains a stepping motor which moves a codable drum. Contact fingers ride the tines of the drum. The electronic circuit drives the stepping motor and provides the read-out for the contacts. Operation of the answer back circuitry is as follows:

Symbols and nomenclature referred to in this discussion are found on 8376 WD. Assume that the answer back drum is in its idle state; a START command is absent and no MESSAGE AVAILABLE is presented.

A START command initiates answer back operation. A low input in Pin 4 couples through a filter network consisting of R10, R22, R19 and C2 and into gate MLB4-8. This circuit combination provides a momentary clock pulse to the drive flip-flop, MLC4, for each START command. At clock time flip-flop MLC4 sets, causing the answer back drum to move to the first position. This is accomplished through the drive circuitry consisting of transistors Q1, Q2 and Q3.

169 Transistor Q3 acts as a switch which allows current to flow through the answer back coil. Q3 is driven by buffer amplifier Q2. When flip-flop MLC4 is set, Q2 is turned on which subsequently turns on Q3. Q3 permits current to build in the answer back coil at an exponential rate.

$$- R/L t$$

$$I=V/R e$$

This current flows through resistor R16. As the current through the coil increases, the voltage developed across R16 increases. This voltage build-up causes a slight current flow through transistor Q1. When the current through the coil is approximately 600 ma, Q1 conducts sufficiently to clear the MLC4 drive flip-flop on its C_D input. With the drive flip-flop cleared, Q2, Q3 and Q1 turn off. The answer back coil releases the armature which subsequently pulls the answer back drum to the 1st position.

At this time the normally closed STOP switch contact has opened, providing a MESSAGE AVAILABLE indication and disabling the synchronous inputs of the MLC4 flip-flop (the START input now has no effect on the circuit). Control of the answer back is now under the direction of the PRESENT CHARACTER input, Pin 1.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

The terminal logic takes the MESSAGE AVAILABLE indication from the answer back logic and decides when to issue a PRESENT CHARACTER command. When the terminal issues the PRESENT CHARACTER (PC) command, three functions occur: data bits are presented at the data output gates for the duration of PC, the drive flip-flop is set through the S_D input, and a CHARACTER AVAILABLE is issued on Pin J402-6. Setting the drive flip-flop initiates the process of advancing the answer back drum to the next position in the same manner discussed previously. Flip-flop MLC4 turns transistor Q2 on which turns transistor Q3 on. The answer back armature begins to pick-up. Transistor Q1 monitors the coil current in order to clear the drive flip-flop at the proper time.

The PRESENT CHARACTER input has simultaneously initiated both the cycle to advance the answer back drum and the read-out of the character. The PRESENT CHARACTER command, normally one bit in length, must be removed before the answer back armature is fully attracted and before the drum is moved. Movement to the next position requires a time of approximately two bits at a 150 wpm character rate. Therefore, sufficient time is allowed to read the character before the drum is advanced.

Reading and advancing the answer back drum occurs with each PC command. When the drum advances to the home position, the STOP switch closes, causing removal of the MESSAGE AVAILABLE indication and priming the synchronous input of the drive flip-flop. The terminal logic does not issue further PRESENT CHARACTER commands when MESSAGE AVAILABLE has been removed. The answer back circuit is now in an idle state. The answer back may be started again by a START command on Pin J402-4.

The network consisting of element C1, R21 and CR1 provides noise suppression from the answer back coil.

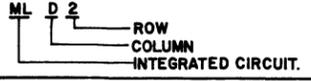
NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

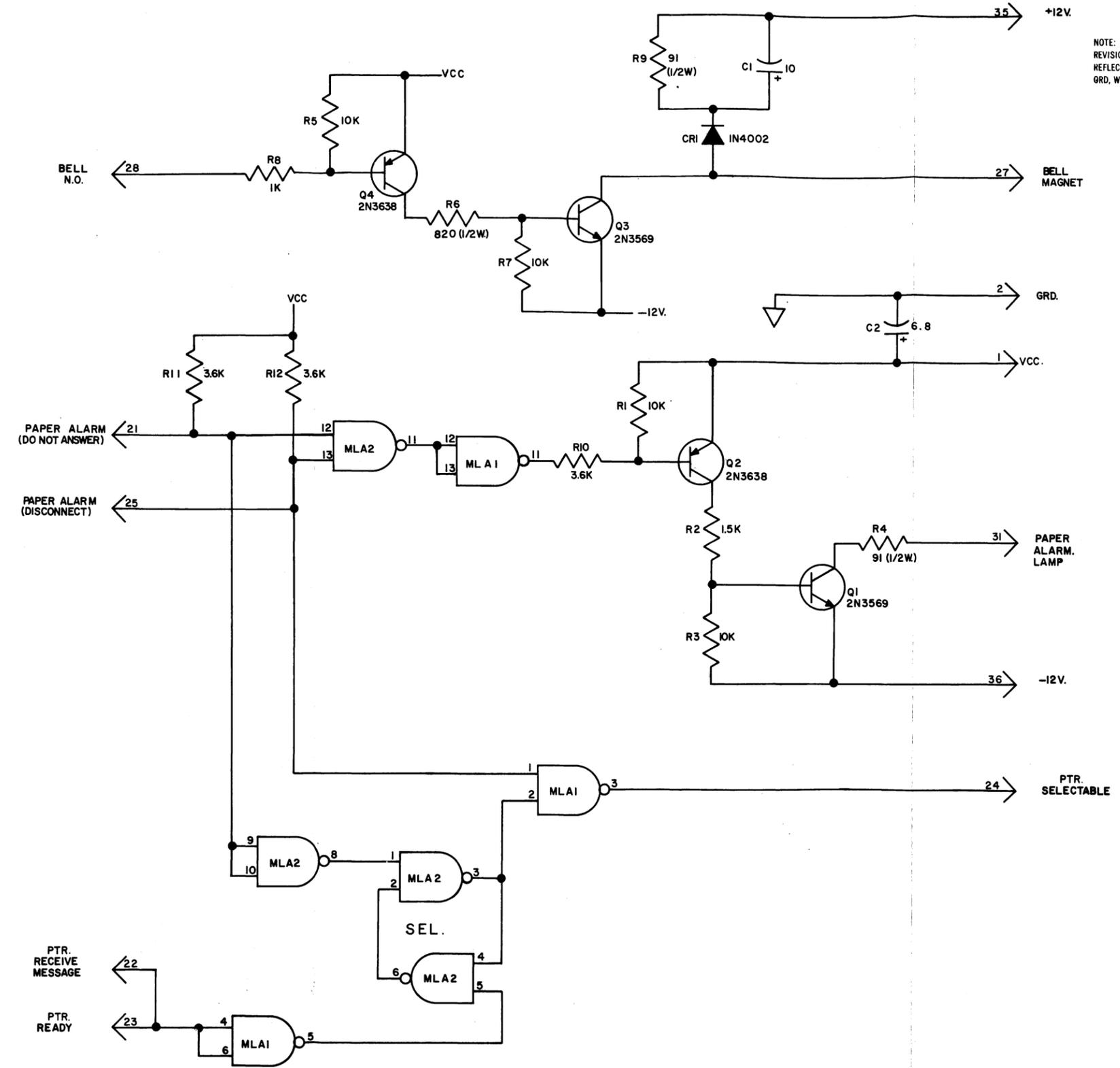
8377WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

- NO. NOTES.
1. ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
 2. ALL RESISTORS 1/4 WATT, AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
 3. ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
 4.  INDICATES FEMALE AND  INDICATES MALE TERMINAL
 5. REFER TO 322050 FOR ASSEMBLY INFORMATION.
 6. S NUMBER 61,519S.
 7. INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD:

 8. THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY.
 9. LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
 10. WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
 11. VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
 12. SEE 8399WD FOR TRUTH TABLES.
 13. REFERENCE CIRCUIT DESCRIPTION 8377WD-CD.
 14. ABBREVIATIONS USED:
SEL. - SELECTABLE ENABLE LATCH.
 15.  INDICATES CIRCUIT GROUND.



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET-1

SCHEMATIC WIRING DIAGRAM FOR ALARMS AND CONTROL

APPROVALS

D AND R <i>HAR</i>	E OF M <i>[Signature]</i>
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E-NUMBER
 PROD. NO. 8377WD
 DATE 3-1-68
 R.D. FILE NO. G-A354AA
 DRAWN W.P.B. CHKD. *[Signature]*
 ENGD. R.E.L. APPD. *[Signature]*

TELETYPE CORPORATION

8377WD

CIRCUIT DESCRIPTION OF THE ALARMS AND CONTROLS CARD
(ASSEMBLY NUMBER 322050)

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<u>SECTION</u>	<u>DESCRIPTION</u>	<u>TOTAL PAGES IN SECTION</u>
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II	Detailed Description and Theory of Operation	1

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE ALARMS AND CONTROLS CARD
(ASSEMBLY NUMBER 322050)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322050 Alarm and Control device logic card performs the function of a bell driver and logically controlled paper alarm.

1.2 The bell driver sinks a nominal current of 230 ma on a logic zero input and sinks zero current on a logic one input. The bell serves as an attention getting device.

1.3 The logically controlled paper alarm sinks a current of 30 ma (nominal) to operate the "PAPER ALARM" panel indicator lamp. The lamp will be turned ON on a logic zero input and turned OFF on a logic one input. The paper alarm signifies a "DO NOT ANSWER" or "DISCONNECT" condition.

1.4 Additional Features

1.4.1 The terminal remains "SELECTABLE", when a "DO NOT ANSWER" condition occurs and becomes "NON-SELECTABLE" after message transmission is completed.

1.4.2 A "DISCONNECT" condition renders the set "NON-SELECTABLE" by means of a direct disconnect line.

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

A logic one is defined as a voltage level between +5.0 volts and +6.6 volts (Usually a logic one approximately equals the integrated circuit supply voltage.) or an open circuit. In either case, a logic one draws no current from the input of the logic element.

Signal voltages between circuit ground potential and +0.5 volts are considered logic zero. Logic currents that flow into the signal source are a function of the element driven, source impedance, supply voltage, and the value of pull up resistor used, if any. Refer to manufacturers specifications for loading information.

2.1.1 Bell In (Pin 28)

This input is high during normal set operation and high and low during an alarm condition (pulse width approximately 30 milliseconds).

2.1.2 Paper Alarm (DO NOT ANSWER) (Pin 21)

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

This input is high during normal set operation and low during a "DO NOT ANSWER" alarm condition. The driving source must be capable of sinking 3 DTL loads. (1 DTL load = 1.4 ma)

2.1.3 Paper Alarm (DISCONNECT) (Pin 25)

This input is high during normal set operation and low during a "DISCONNECT" alarm condition. The driving source must be capable of sinking 3 DTL loads.

2.1.4 PTR Receive Message-PTR Ready (Pins 22, 23)

This input is low while the printer motor is in operation and high at all other times. The driving source must be capable of sinking 1 DTL load.

2.1.5 Paper Alarm Lamp (Pin 31)

The Paper Alarm Lamp is turned on by a zero output from the inverter M1A1 Pin 11, and indicates to the operator that the printer is in a paper alarm condition.

2.1.6 Printer Selectable (Pin 24)

This output is normally low, but will be high when the printer is not selectable (paper alarm). The paper alarm (DO NOT ANSWER) does not immediately affect Printer Selectable, whereas the Paper Alarm (DISCONNECT) immediately causes Printer Selectable to go high (non-selectable). This output is capable of driving 8 DTL loads.

2.1.7 Bell Driver

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A logic zero applied to the input of the bell driver (Pin 28), turns the output transistor on and rings the bell. A logic one turns the output transistor off and no current flows through the bell winding.

2.2 Mechanical Characteristics

The integrated circuit logic and driver amplifiers are mounted on a printed circuit card which is inserted in a conventional 36-pin edge card connector.

2.3 Power Requirements

<u>Vcc (DC)</u>	<u>Current Maximum</u>
+5.0V to +6.6V (+5.25V Nom.)	85 ma
+11.65 to +13.75V (+12.5V Nom.)	275 ma
-11.13V to -13.88V (-12.5V Nom.)	275 ma

2.4 Temperature Range

The ambient temperature range for operation is from 0°C to 70°C in free air. Non-operating storage temperature is from -40°C to 70°C.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

- 1.1 Assembly and Schematic drawing 322050, (MC050) and 8377 WD, respectively.
- 1.2 Logic Symbols and Truth Tables Per 8399 WD.
- 1.3 Integrated circuit information per manufacturers specifications.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Bell Driver

2.1.1 The bell driver circuit is a two stage amplifier, designed to operate full ON or OFF without intermediate levels.

A logic zero applied to the input of Q4 results in a positive going pulse at the base of Q3. As a result, Q3 is turned ON and approximately 24 volts DC is applied to the bell winding. The bell (collector current of Q3) current rises exponentially to a nominal value of 230 ma. The rise time of the current waveform is determined by the inductance and series resistance of the bell winding.

A logic one applied to the input of Q4 causes Q4 collector current to decrease to zero. As a result, a negative going pulse appears at the base of Q3. Q3 is now in the "OFF" state. The bell winding discharges its energy through CR₁ and the discharge network R₉, C₁. The pickup and dropout times are not adjustable and for a given bell are a function of the charge path, discharge network, and winding inductance which determine the electrical time constant.

2.2 Paper Alarm

2.2.1 The "Paper Alarm (DISCONNECT)" is used where immediate alarm action is required and is a logic zero during the alarm condition. The alarm signal goes through two stages of inversion and turns ON the paper alarm lamp. The alarm signal also appears on MLA1 Pin 1 and immediately switches the output high, causing "Printer Selectable" Pin 24 to go to the non-selectable state (high). The "Paper Alarm (DO NOT ANSWER)" is used to disable the "Printer Selectable" (Pin 24) whenever Receive Message (Pin 22) is high. Thus, if the alarm occurs during a message (Printer Receive Message in zero state), the alarm lamp will turn on, but the Printer Selectable will remain low until Printer Receive Message goes high at the end of the message. This sequence is controlled by the Selectable Enable Latch (SEL) which is gated by Printer Receive Message MLA1 Pin 5 and will transfer the Paper Alarm indication (zero), from MLA2 Pins 9 and 10 to MLA1 Pin 2, whenever Printer Receive Message goes high. Thus Printer Selectable goes high.

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SEE SHEET 1 FOR NOTES

8383WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

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SHEET 2

SCHEMATIC WIRING DIAGRAM FOR RECEIVE CONTROL (WITH REGENERATOR)

APPROVALS

D AND R *HRK* E OF M *[Signature]*

E-NUMBER

PROD. NO. 8383 WD.

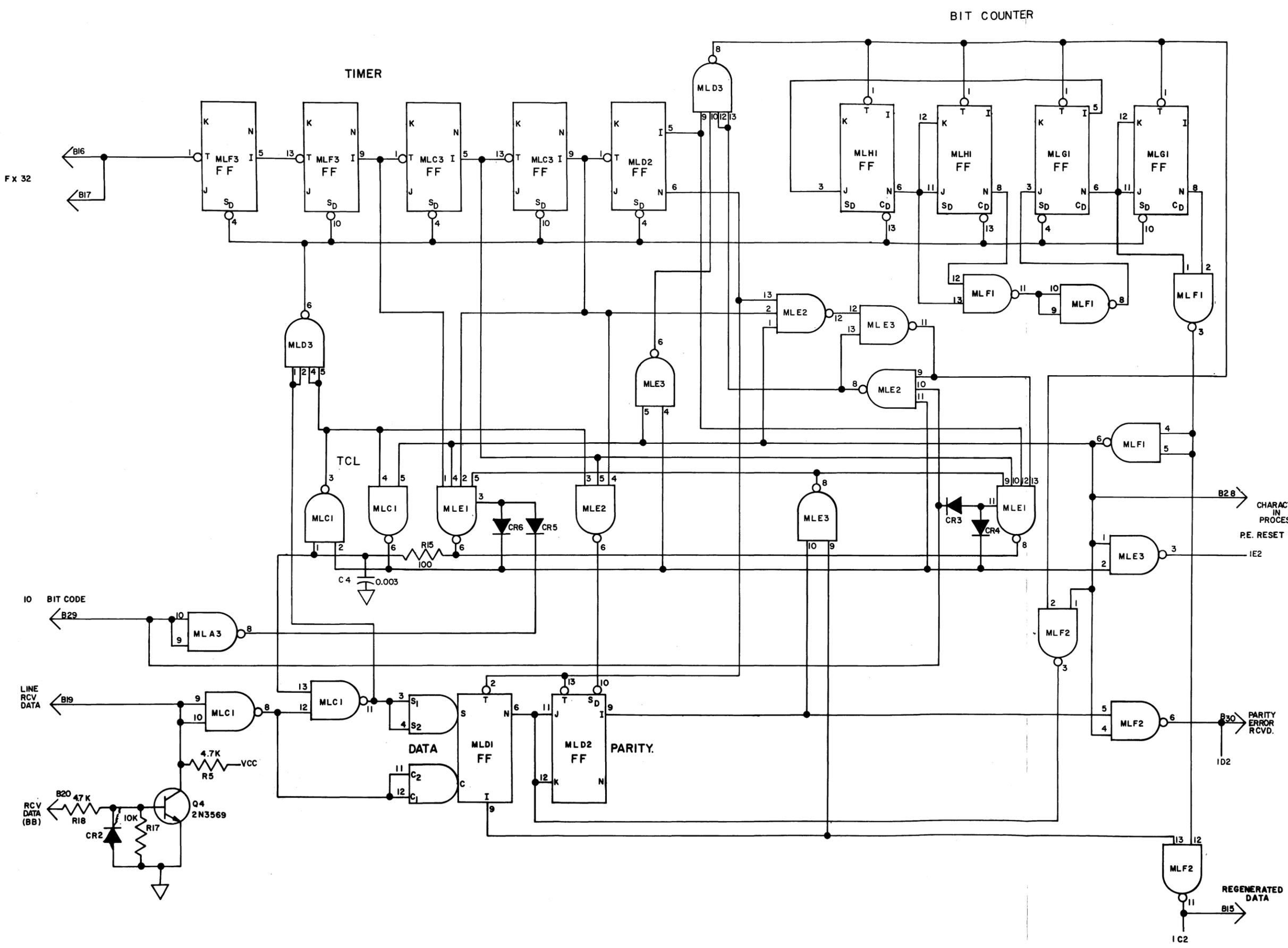
DATE 3-6-68

P.D. FILE NO. G-A354AA

DRAWN W.R.B. CHKD. *[Signature]*
 ENGD. A.B. APPD. *[Signature]*

TELETYPE CORPORATION

8383WD



FX 32

10 BIT CODE

LINE RCV DATA

RCV DATA (BB)

B28 CHARACTER IN PROCESS P.E. RESET

B30 PARITY ERROR RCVD.

REGENERATED DATA B15

CIRCUIT DESCRIPTION OF THE RECEIVE CONTROL CARD
(W/REGENERATOR)
(ASSEMBLY NUMBER 322062)

TABLE OF CONTENTS

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II	Detailed Description and Theory of Operation	11

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CIRCUIT DESCRIPTION OF THE RECEIVE CONTROL CARD
(ASSEMBLY NUMBER 322062)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322062 Circuit Card Assembly controls and directs telegraph signals to the appropriate receiving device. The circuit receives serial input signals and provides serial output signals. An EIA input amplifier receives incoming on-line signals. Signals generated locally are received directly from sending distributors.

1.2 Several other functions are provided. These functions are:

1.2.1 Signal regeneration which changes input line data signals distorted 40% or less to output signals with less than 3% distortion. The regenerator assures a minimum character length of 9.8 units at 150 baud (150 wpm) and 10.6 units of 110 baud (100 wpm).

1.2.2 Detects improper received signal parity and provides power to an external parity error detection indicator lamp.

1.2.3 Half or full duplex selection - controls operation in either the half or full duplex mode.

1.2.4 Line or local tabulation - locks all sending devices during tabbing functions.

1.2.5 An output to indicate a receiving device in alarm - indicates an alarm condition for receivers.

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2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the circuit assembly are either EIA (RS-232-B) or nanc type integrated diode transistor logic (DTL) inputs. EIA inputs are defined in Electronic Industries Association Standard RS-232-B. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts.

2.1.1 Received Data (Pin 20)

This input receives an EIA data signal from the signal line. This input is marking when the voltage is between 0V to -25V and is spacing when the voltage is between +3V to +25V. A spacing signal greater than .5 bit in length forces the regenerator to cycle and monitor the line for the duration of one character.

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2.1.2 10-11 Bit Code (Pin 29)

This input is grounded when the regenerator is operating with signals containing 10 bits per character (one stop bit). It is open or high for characters containing 11 bits (two stop bits). The device driving this input must be capable of sinking three DTL loads.

2.1.3 FX32 (Pin 16)

This input is from an external oscillator. The frequency of the oscillator must be 32 times the desired bit rate. The device driving this input must be capable of sinking two DTL loads.

2.1.4 HDX N.O. (Pin 34)

This input is normally in the 1-state. When in the full duplex mode (FDX), a low (0-state) on this input will change the logic to half duplex mode. This contact must be capable of sinking two DTL loads.

2.1.5 FDX N.O. (Pin 26)

This input is normally in the 1-state. When in the half-duplex mode (HDX) a low on this input will change the logic to the full duplex mode. This contact must be capable of sinking two DTL loads.

2.1.6 Normalize (Pin 33)

This input is normally in the 1-state. At certain times it is desirable to condition selected set logic to a predetermined state. A low input on this lead will condition the full-half duplex latch (FHDL) to the half duplex state. This input represents one DTL load.

2.1.7 Signal Output (Local) (Pin 13)

This input is connected to the local distributor's data signal output and represents one DTL load. The signal moves through gated logic to the proper receiving device.

2.1.8 Signal Output (Line) (Pin 27)

This input is connected to the line distributor's data signal output and represents one DTL load. The signal moves through gated logic to the proper receiving device.

2.1.9 Parity Error N.O. (Pin 25)

This input is normally in the 1-state. A low on this input will reset the parity error lamp latch (PELL) which turns off the parity error received lamp driver. The device driving this input must be capable of sinking two DTL loads.

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2.1.10 Line Trouble Indication (Pin 21)

This is an EIA input from an external control device or from a data set. It identifies an abnormal line condition. An ON condition causes the Parity Error or Line Trouble lamp to light.

2.1.11 Tab N.C. (Pin 22)

This is a contact input from the typing unit indicating to a local sending device that a tabbing condition is in process. The contact must be capable of sinking two DTL loads.

2.1.12 Tab N.O. (Pin 23)

Same as Section 2.1.11.

2.1.13 Printer Local (Pin 14)

This input primarily directs the proper data signals (line or local) to the typing unit and primes certain "receiver in alarm" gates. It also inhibits the line tab and parity error outputs (ribbon shift) when the printer is in the local mode. This input represents one DTL load.

2.1.14 Printer Selectable (Pin 10)

This lead monitors the typing unit's paper supply. With a full paper supply the lead is normally in the 0-state. It should revert to the 1-state when a paper out condition exists or upon termination of a call if a low paper condition exists. This lead represents one DTL load.

2.1.15 Printer Ready (Pin 9)

This input is normally low when the printer motor is operating. It reverts to the 1-state when the motors are OFF. This information is used to prime "alarm" logic. This lead represents one DTL load.

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2.1.16 Punch Ready (Pin 7)

This input is normally low when the punch motor is operating. When the punch motor is OFF, it reverts to the 1-state. It is used to prime "alarm" logic. The input represents one DTL load.

2.1.17 Punch Local (Pin 8)

This input directs the proper data signals (line or local) to the punch and primes certain "receiver in alarm" gates. When this lead is in the 0-state, the punch receives local data. In the 1-state and no blind condition, the punch receives line data. This lead represents one DTL load.

2.1.18 Punch Blind (Pin 6)

When this input is in the 0-state, the punch is blinded to data signals. This input represents five DTL loads.

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2.1.19 Punch Selectable (Pin 4)

This lead monitors the punch tape supply. With a full tape supply the lead is normally in the 0-state. It should revert to the 1-state when a paper out condition exists or upon termination of a call if a low tape condition exists. This lead represents one DTL load.

2.2 Output Characteristics

The outputs from this assembly are either nand type diode transistor logic (DTL) or transistor driver outputs. Each output will be rated by the number of DTL loads it can sink. Each DTL load is approximately 1.4 ma.

2.2.1 Line Received Data (Pin 19)

This output follows the EIA received signal input lead. This lead is in the 0-state when the EIA input is spacing and is in the 1-state when the EIA input is marking. It is used in other system logic to indicate the presence of a long spacing signal. This output will sink 20 DTL type loads.

2.2.2 Regenerated Data (Pin 15)

This output provides a data signal derived from the received signal input lead which is practicably distortion free. This lead is in the 1-state for a MARK and in the 0-state for a SPACE. This output will sink seven loads.

2.2.3 Parity Error Received (Pin 30)

This output, normally in the 1-state, reverts to the 0-state whenever a character is detected with incorrect vertical parity. This indication is presented at the end of the errored character. This lead will sink six loads.

2.2.4 Full Duplex (FDX) (Pin 24)

For half duplex operation this output is in the 1-state. When a full duplex command is received, this output reverts to the 0-state. It is capable of sinking four loads.

2.2.5 Tab (Line) (Pin 31)

This output is normally in the 1-state. When a tabbing function occurs with the unit in the local and half duplex mode, the lead reverts to the 0-state until the tabbing function is completed. This indication is used in other system logic to intercept the line distributor's "PRESENT NEXT CHARACTER" (PNC) output. It will sink eight DTL loads.

2.2.6 Tab (Local) (Pin 12)

This output is normally in the 1-state. When a tabbing function occurs with the typing unit in the local mode, the lead reverts to the 0-state until the tabbing function is completed. This indication is used in other system logic to intercept the local distributor's "PRESENT NEXT CHARACTER" output. It will sink eight DTL loads.

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2.2.7 Printer Serial Data (Pin 11)

This lead presents serial data derived from the incoming signal line from the line/local distributor to the printer selector magnet driver. It is in the 1-state for a marking bit and in the 0-state for a spacing bit. This output will sink seven DTL loads.

2.2.8 Punch Serial Data (Pin 3)

This lead presents serial data derived from the incoming signal line or from the line/local distributor to the punch selector magnet driver. A marking bit is in the 1-state and a spacing bit is in the 0-state. This output will sink seven DTL loads.

2.2.9 Receiver in Alarm (Pin 5)

This output indicates to external logic that a receiving device is in an alarm condition or that no receiving device is available. This lead is normally in the 1-state but changes to the 0-state when an alarm condition is present. This output will sink four DTL loads.

2.2.10 Parity Error Not (Pin 32)

This output normally in the 0-state reverts to the 1-state upon the reception of a parity errored character and remains in the 1-state until a character with the correct parity is received. This signal is used in external logic to change the color of the printed character. Eight loads may be attached to this lead.

2.2.11 Line Trouble/Parity Error Lamp (Pin 18)

This output drives a lamp located on the control strip to indicate a parity error. A parity error will cause this lead to change to the "ON" state providing power to this lamp. It remains in this state until manually reset.

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2.2.12 Character in Process (Pin 28)

When this lead is in the 1-state, the regenerator is idling. This lead reverts to the 0-state during the time in which a character is processed through the regenerator. This output will sink one DTL load.

2.3 Size

The receive control card measures 5-3/4 x 4-1/4 inches. It is designed to mate with a standard 36 pin circuit card connector.

2.4 Options

2.4.1 10-11 Unit Code

The receive control may be changed from an eleven unit code to ten unit code by grounding Pin 29.

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2.4.2 Half Duplex (Strap A)

The assembly may be permanently strapped for half-duplex by having strap A in place.

2.4.3 Full Duplex (Strap B)

The assembly may be permanently strapped for full duplex by having strap B in place and removing strap A.

2.4.4 Auxiliary Receiver (Strap C)

Strap C remains in place when an auxiliary receiving device, such as a reperforator, is part of the system. It is used to indicate, along with other receiving devices, a capability to receive incoming line data. If no receiving device is in the line mode, an alarm condition is generated.

2.5 Miscellaneous Requirements

2.5.1 Power Supply Requirements

VDC

I ma (max)

5V to 6.6V

390 ma

2.5.2 Operating Temperature Range

0°C to 70°C (free air)

2.5.3 Storage Temperature Range

-40°C to +70°

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SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 See assembly drawing 322062 (MCO62) and schematic drawing 8383 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 General

The Receive Control card assembly is described in two parts, signal regeneration (regenerator) and data control (receive control). Refer to the timing diagrams, flow chart, and schematic 8383 WD to aid in understanding the following description. The flow chart is intended to be used as a guide to help in understanding the operation of the regenerator. It should be studied in conjunction with the circuit schematic and timing diagram. The rectangular symbols denote functions that are to be performed, and the triangular shaped symbols denote a decision point. It is not intended that any of the symbols be construed to represent logic functions. The flow chart is primarily intended to relate circuit operation with respect to time.

2.2 Regenerator

The mode of operation described first is for characters of 10 unit code. This requires a ground or 0-state on Pin 29.

Assume that the regenerator is in an idle condition. The timer is not operating because the output of the Start Gate, MLD3-6, is in the 0-state. This gate is in the 0-state when the receive signal input is MARKING continuously and the Timer Control Latch, TCL, has been reset. TCL resets at the end of each character.

When a SPACING signal (Start bit) appears at the receive signal input, Pin 20, the output of MLC1-11 switches to the 0-state. This forces the Start Gate to the 1-state, releasing the timer.

After 1/2 bit time duration, a clock pulse appears at MLD3-8. This sets a one count in the bit counter, which in turn sets TCL via MLF1-3 and MLF1-6. The output of the TCL clamps the Start Gate "ON" for a full character interval. Control of the timer is now removed from the signal line.

If the SPACING signal is not present for a full 1/2 bit interval, however, the TCL will not have been set. Consequently, as the Receive Signal Input returns to a MARK, the Start Gate reverts to a 0-state, clearing the timer to the idle state. A character, therefore, will not be regenerated.

When the SPACING signal is longer than 1/2 bit, the timer is locked on and delivers clock pulses at bit frequency. These pulses are used to

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cycle the bit counter, the data flip-flop, and the parity flip-flop. The function of each of these circuits is as follows:

2.2.1 Bit Counter

The function of the bit counter, composed of four binary elements and two gates arranged to operate as a decade counter, is that of timing out a character interval. When a count of ten is reached, the output of MLF1-3 switches to the 0-state. (Refer to the diagram and timing chart of Figure 1 for information on intermediate states of the bit counter.)

2.2.2 Data Flip-Flop

Clock pulses generated by the timer process data through the Data Flip-Flop, MLD1. Incoming line data (which may be distorted) appears at the synchronous set and clears inputs of MLD1. This data is sampled and read into the data flip-flop by the clock pulses. The inverted output of the data flip-flop, distortion free, is applied to the Regenerated Data Gate, MLF2-11.

2.2.3 Parity Flip-Flop

The function of the parity flip-flop is to search for even parity on the 8 data bits of a character. The parity flip-flop changes states each time a MARK signal from the data flip-flop is read into it by the timer clock. The inverted output of the parity flip-flop is applied directly to the Parity Error Received Gate, MLF2-6, where it is sampled at the end of each character by the bit counter. The output of the gate remains in the 1-state for correct parity or, conversely, switches to the 0-state if a parity error has been detected.

2.2.4 Timer Control Latch Reset

After the 10th count is reached, the timer continues counting for an interval designed to guarantee regeneration of a minimum length stop bit. When operating in the 10 unit character code, this time period is approximately 0.3 of a bit. At this time Stop Bit Regenerator Gate, MLE1-6, has three of its four inputs primed (extender inputs CR5 and CR6 primed by 10 unit code and TCL respectively) to reset the timer control latch. The remaining input is controlled by the Synchronism Gate, MLE3-8, which senses for either the presence of correct parity or the presence of a marking bit in the data flip-flop. If either is present the regenerator is considered to be in synchronism with the signal line and gate MLE3-8 is in the 1-state. Now all inputs of the stop bit regenerator gate are in the 1-state, resetting TCL and the timer. The regenerator now waits for a new character.

If the regenerator is not in apparent synchronism with the signal line, i.e., parity incorrect and no marking bit in the data flip-flop, Synchronism Gate, MLE3-8, will not permit the stop bit regenerator gate to reset TCL and the timer. The regenerator continues to run 0.3 of a bit

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beyond the next clock pulse or pulses until the conditions for synchronism are achieved. Only then will TCL and the timer be reset. The regenerator logic is now conditioned for the start of a new character. It waits for the next 1/2 bit SPACING "start" signal to begin a new cycle.

For units operating with characters consisting of 11 bits, i.e., with two stop bits, Stop Bit Regenerator Gate, MLE1-6, is electrically replaced by Stop Bit Regenerator Gate MLE1-8. This is accomplished by removing the ground on Pin 29. MLE1-6 is inhibited through its CR5 input while MLE1-8 is primed through its CR3 input. The Stop Bit Regenerator Gate, MLE1-8, operates in a very similar manner to MLE1-6. Its function, however, is to time out 1.1 bit elements instead of .3 elements after the 10th count. Three inputs are used for this purpose, two from the timer and one from a latch made up of MLE3-11 and MLE2-8.

The MLE2-12 gate has inputs from the timer such that when .75 bits are sensed, the MLE3-11, MLE2-8 latch is set. Approximately .35 bits later the two inputs to MLE1 from the timer are high. If apparent synchronization is present (MLE3-8 high) the Stop Bit Regenerator Gate switches to the 0-state, resetting TCL. When TCL is reset, the MLE3-11, MLE2-8 latch is reset, and MLE1-8 is inhibited via diode CR4.

2.2.5 Parity Count Inhibit Gate

The function of the Parity Count Inhibit Gate, MLF2-3, is to prevent sampling for parity of the incoming signal during a stop bit. When the first clock pulse occurs, the stop bit of the previous character is stored by the data flip-flop. Consequently, the first clock pulse should not sample the data flip-flop for parity. Also, when operating in the 11 unit character mode, the last clock pulse of a character occurs during the stop pulse and, therefore, should not be permitted to sample the data flip-flop. During both these time periods the output of MLF2-3 is low and the parity flip-flop is inhibited.

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2.3 Receive Control

The second major function of the receive control circuit card is: to direct data received from a multiplicity of sources to the proper receiving device, to control the receiving alarm indicators, and to perform miscellaneous control functions associated with the receivers.

2.3.1 Receive Data Logic

Data is received from three sources. These are: regenerated data from the regenerator, data generated by the on-line sending distributor, and data generated by the local sending distributor. Assume a half duplex operating mode. Data received from the local sending distributor passes through MLG3-6 and primes output serial data gates associated with the printer and punch. Data associated with the line distributor passes through MLB1-3, MLB1-6 (primed in the half duplex mode) and MLF2-8. The MLF2-8 output also

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primes serial data gates associated with the printer and punch. Receive data from the regenerator passes through MLF2-8 and also primes serial data gates associated with the punch and printer.

The input at Pin 14 is low when the printer is in the local mode, and high when it is in the on-line mode. Consequently, MLG3-11 is primed only when the printer is in the on-line mode. Thus, local data appears at Pin 11, the printer serial data output, when a printer local command appears at Pin 14, and on-line data appears at Pin 11 when an on-line command appears at Pin 14.

When the punch is in the local mode a low appears at Pin 8, and when the punch is on-line a high appears at that input. This input primes gate MLG2-6 which has as its second input the punch blind signal received at Pin 6. The punch blind signal is low when the punch is to be blinded and high when it is to be enabled. Thus, when the punch is local and enabled, only local data will appear at Pin 3, the punch serial data output. When the punch is enabled, on-line (Pin 8 high) and only on-line data will appear at Pin 3. When the input received at Pin 6 is low, signifying that the punch is to be blinded, the output at Pin 3 will remain continuously MARKING.

2.3.2 Receive Alarms

The output at Pin 5, receiver in alarm, is high when all receivers are functioning normally and low for an alarm condition. An alarm condition exists when one of the receiving devices is unable to function, i.e., out of paper, or, when no receiver is in the on-line condition during receipt of a message. The following are alarm conditions:

Condition 1: The printer is on-line, the printer motors are not yet up to speed (printer not ready, Pin 9 high), and a spacing bit is received on line. MLH2-12 is switched.

Condition 2: The printer is on-line and a paper alarm is present. MLG2-8 is switched.

Condition 3: No receiving device is in the on-line mode. MLG2-11 is switched.

Condition 4: The punch is on-line and a tape alarm is present. MLH2-6 is switched.

Condition 5: The punch is on-line, the punch motors are not yet up to speed (punch not ready, Pin 7 high), and a spacing bit is received on line. MLH1-6 is switched.

All alarm gate outputs are connected together and appear at Pin 5. For applications where a printer must be on-line for a call to be received, strap C is removed. With strap C removed, MLC2-11 will switch to an alarm condition whenever the printer is off-line.

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2.3.3 Tabbing Contro

The purpose of the tabbing control logic is to prevent transmission from a local reader or keyboard until response to a tabbing function is completed by the local printer. The tabbing latch, TABL, is set by a contact on the typing unit during tabbing and is reset by a contact when the tabbing is complete. The output of this latch at MLB1-8 primes the MLAL-6 and the MLG2-3 gates. The MLG2-3 gate has two inputs. The second input is primed while the printer is in the local mode. The MLAL-6 gate has three inputs. The second input is high while the printer is on-line, and a third input to the MLAL-6 gate is high when the unit is in the half duplex mode. Thus a line tab indication at Pin 31 (0-state) will be present only when the typing unit is on-line, tabbing is in process, and the terminal is in the half duplex mode. A tab condition will be present at Pin 12 (0-state) only when the printer is in the local mode and tabulation is in process.

2.3.4 Full Duplex

A full duplex latch, FHDL, is operated directly from the typing unit. When a full duplex command is sensed, Pin 26 is shunted to ground (0-state) setting the latch. The latch is reset when a half duplex command at Pin 34 is sensed, or when the system is normalized by a logical zero at Pin 33. The output of the latch, MLAL-12, at Pin 24, is a logical zero for full duplex and a logical one for half duplex. The output of FHDL also primes gates MLB1-6 and MLAL-6. When in the full duplex mode, locally generated line data will not pass through MLB1-6 and, therefore, will not be copied by the local printer. When in the full duplex mode, and while a tabulation is taking place, the line tab output will remain high. Transmission by a local reader or keyboard will continue, therefore, since the system is in full duplex mode.

The system may be wired permanently full duplex or permanently half duplex. For permanent full duplex, strap B should be connected and strap A removed. For permanent half duplex operation, strap A should be connected and strap B removed. For on-line control, both straps are removed.

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2.3.5 Parity Error Display Logic

Parity errors may be displayed in either or both of two ways. These are a lamp located on the control panel, or, by a ribbon shift to print the errored character in red. When a parity error is detected by the parity error circuitry of the regenerator, the parity error lamp latch, PELL, and the parity error ribbon latch, PERL, are both set. The output of the PELL latch drives a lamp amplifier composed of transistors Q2 and Q1, having an output at Pin 18. The output is turned ON, a logical lamp zero for a parity error. The output may also be turned ON by an EIA input (1-state) at Pin 21, the line trouble indication input. The "Parity Error or Line Trouble" output may optionally display either parity error or line trouble (Carrier Fail) or both. The PELL latch, and the associated parity error or line trouble lamp is turned OFF by a logical zero applied

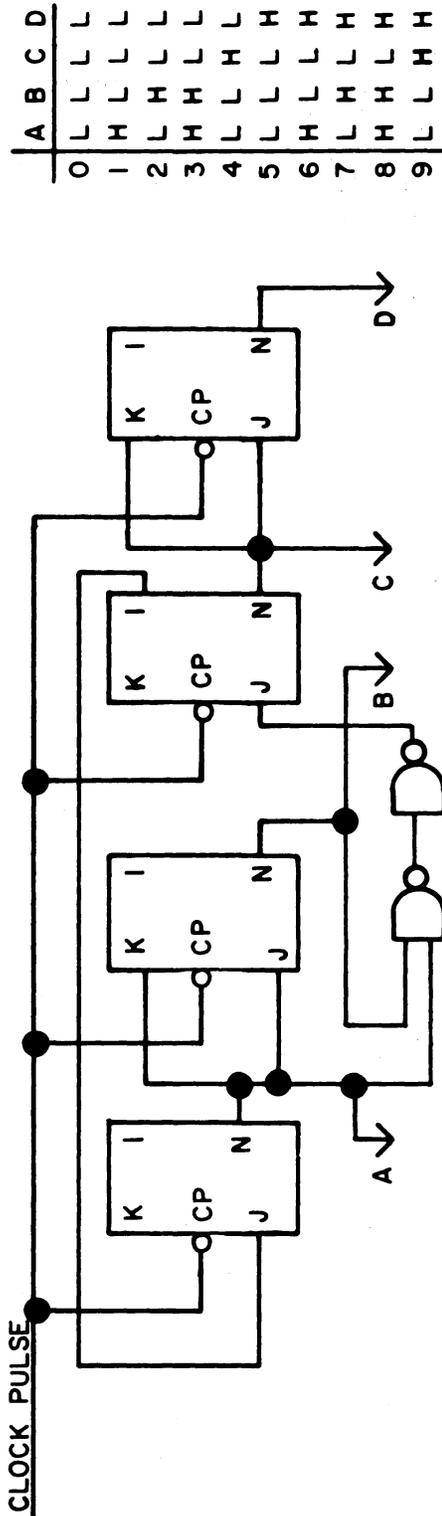
NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. | SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

at Pin 25. The logical zero is derived from a reset switch contact closure on the control panel.

As an option, the parity error causes the printing of the errored character in red via the PERL latch. The output of this latch is applied through MLA3-3 and MLA3-6 to Pin 32. A logical one at Pin 32 operates the ribbon magnet through an amplifier on the ribbon magnet amplifier card. At the end of a character, the PERL latch is reset by the regenerator or by receipt of a SPACING signal identifying the beginning of the next character. A second input to the MLA3-3 gate prevents operation of the parity error ribbon circuitry when the printer is in the local mode.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

BIT COUNTER DIAGRAM AND
TIMING CHART



	A	B	C	D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	L	H
5	L	L	H	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	L	H

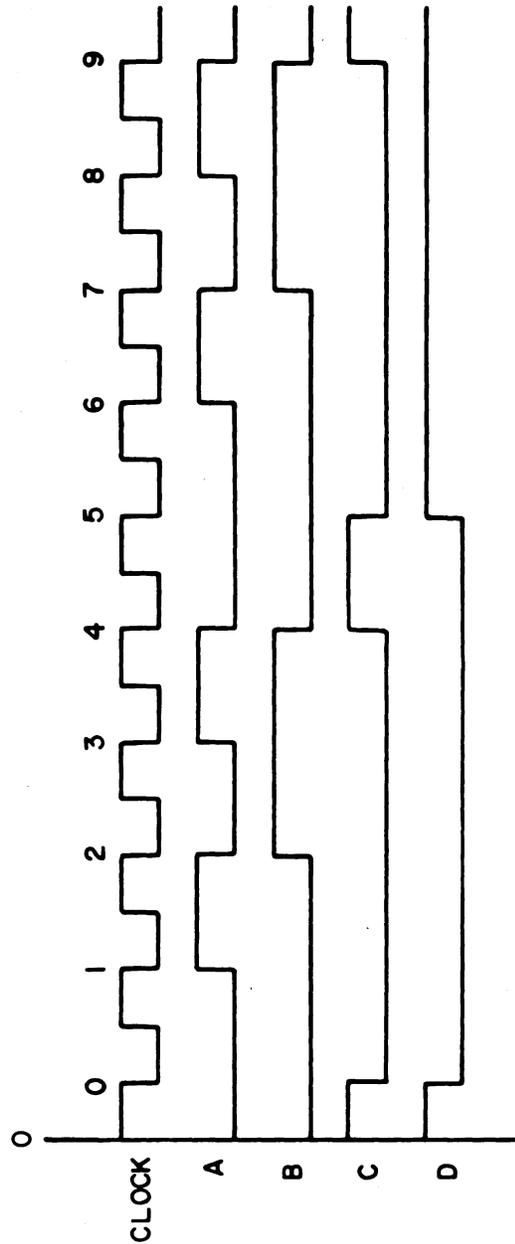
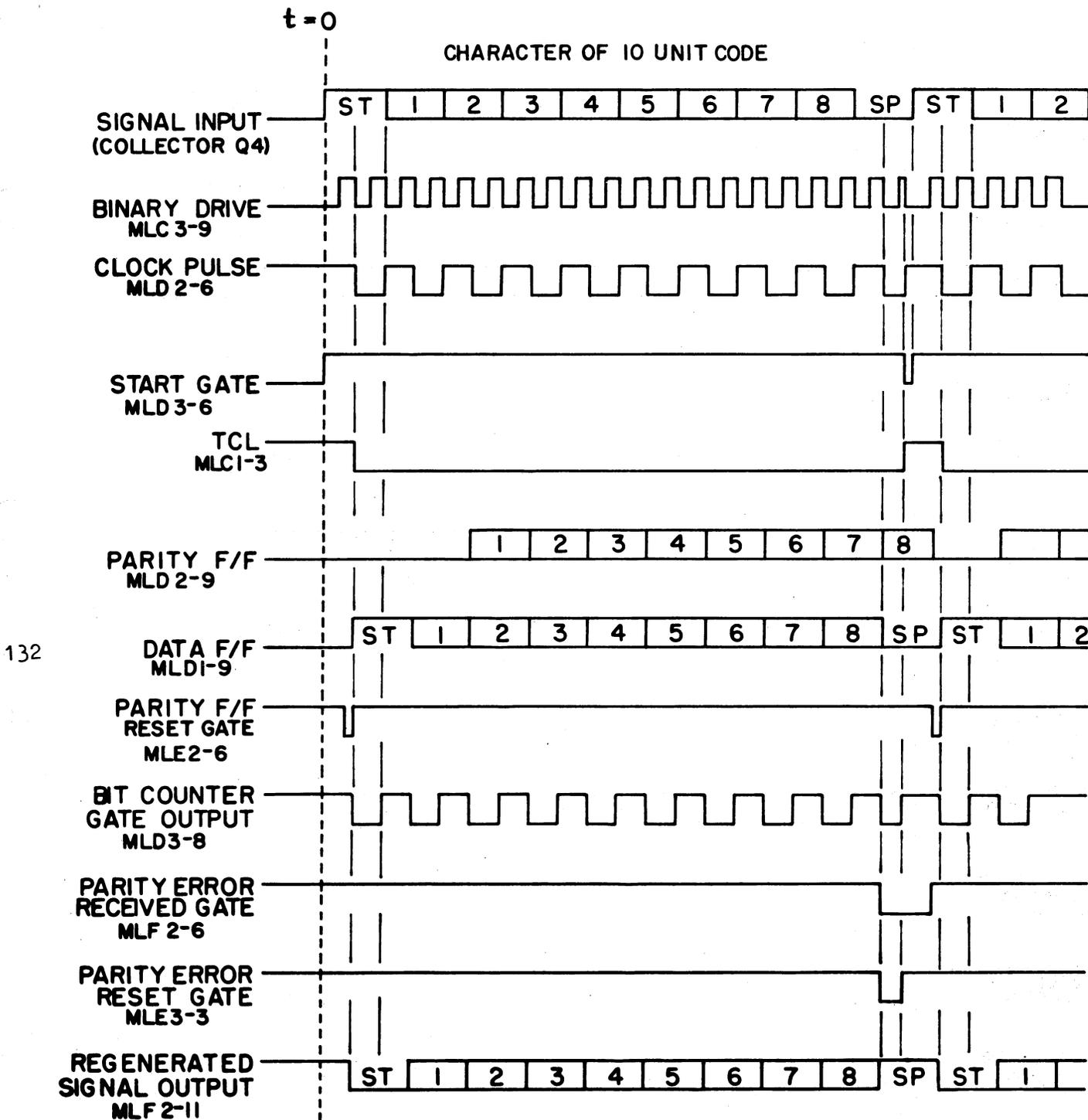


FIGURE 1

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL ASSEMBLY

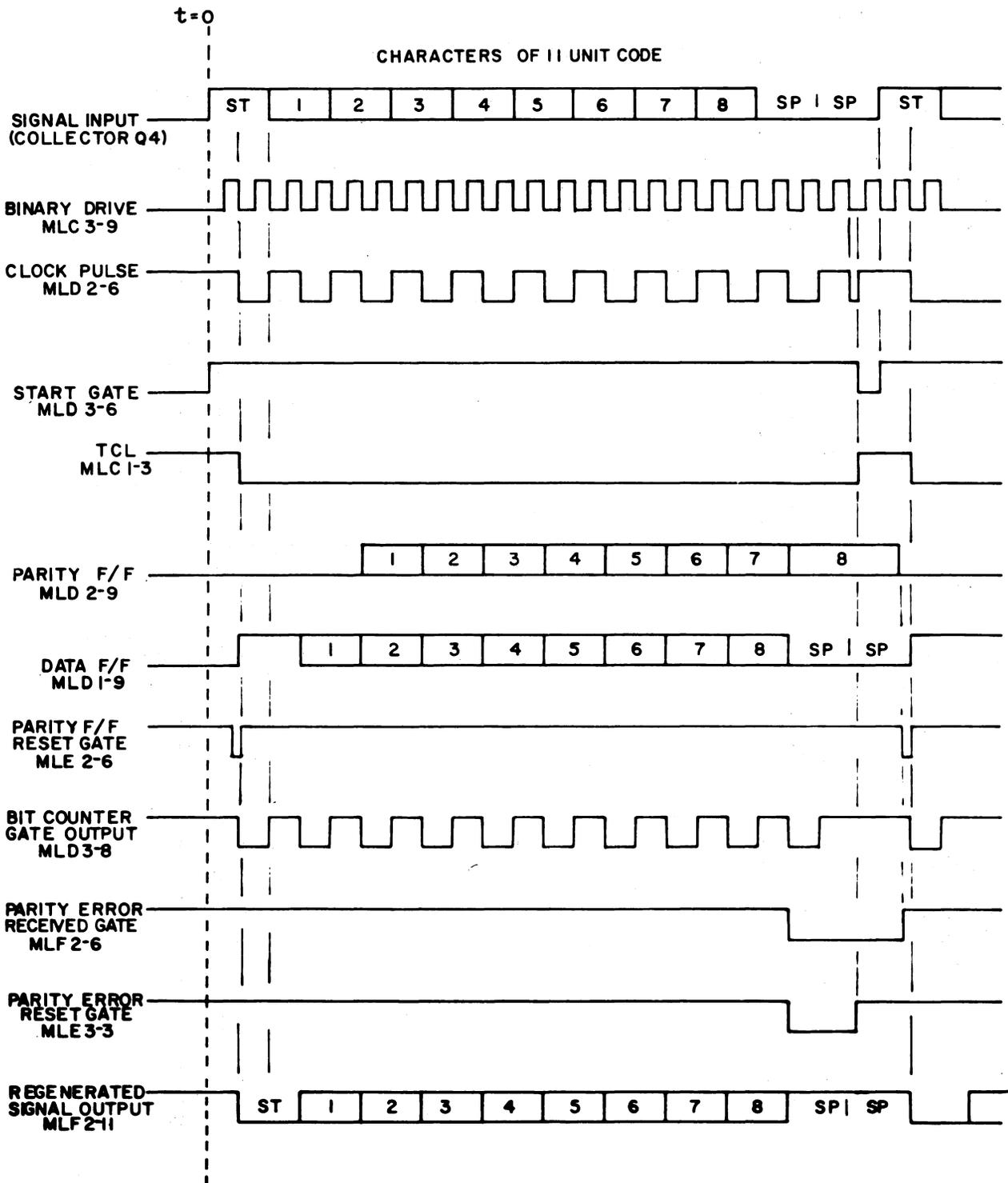


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FIGURE 2

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL ASSEMBLY



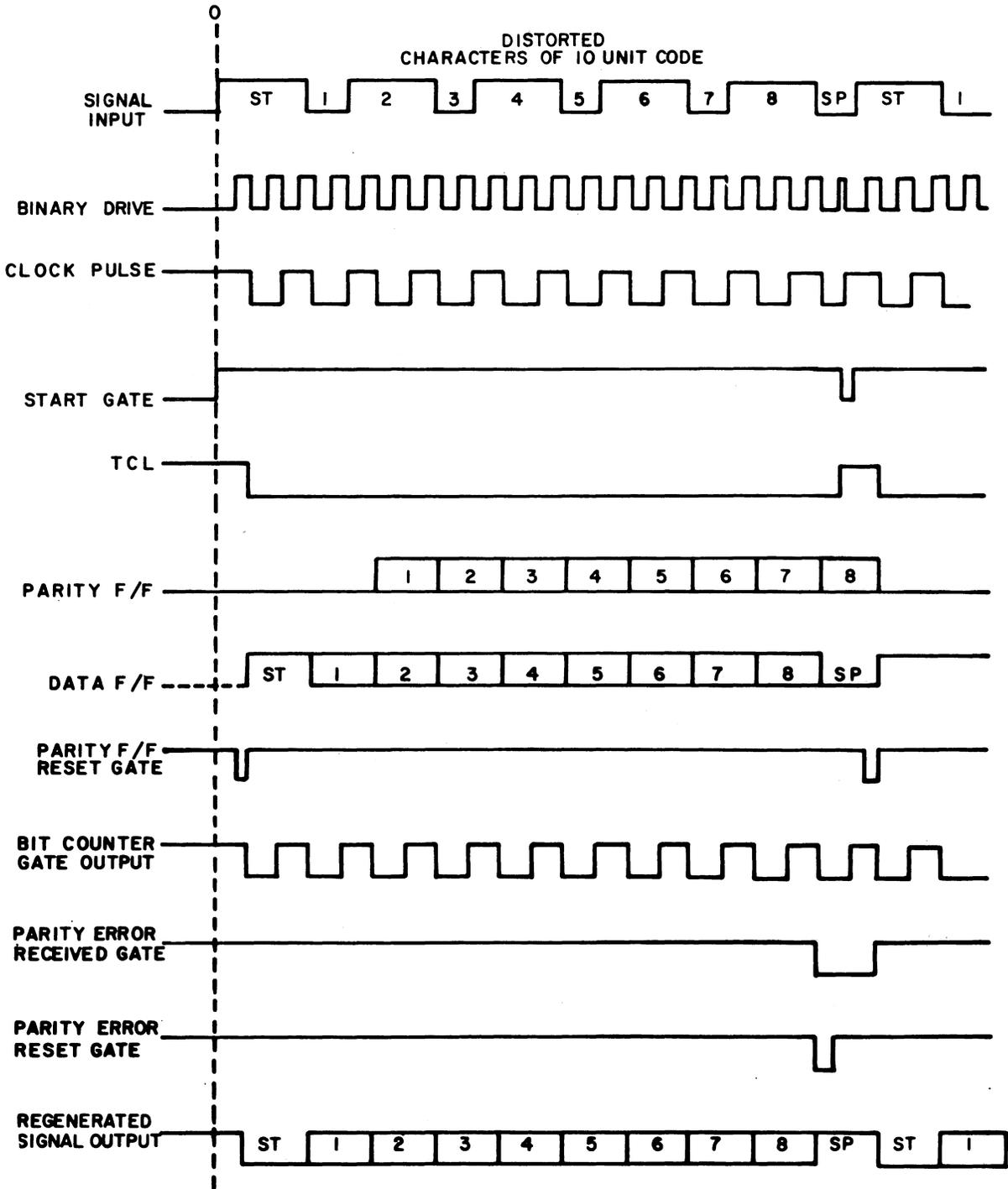
133

FIGURE 3

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

TIMING DIAGRAM
RECEIVING SIGNAL REGENERATOR
P/O 322062 RECEIVE CONTROL
ASSEMBLY.

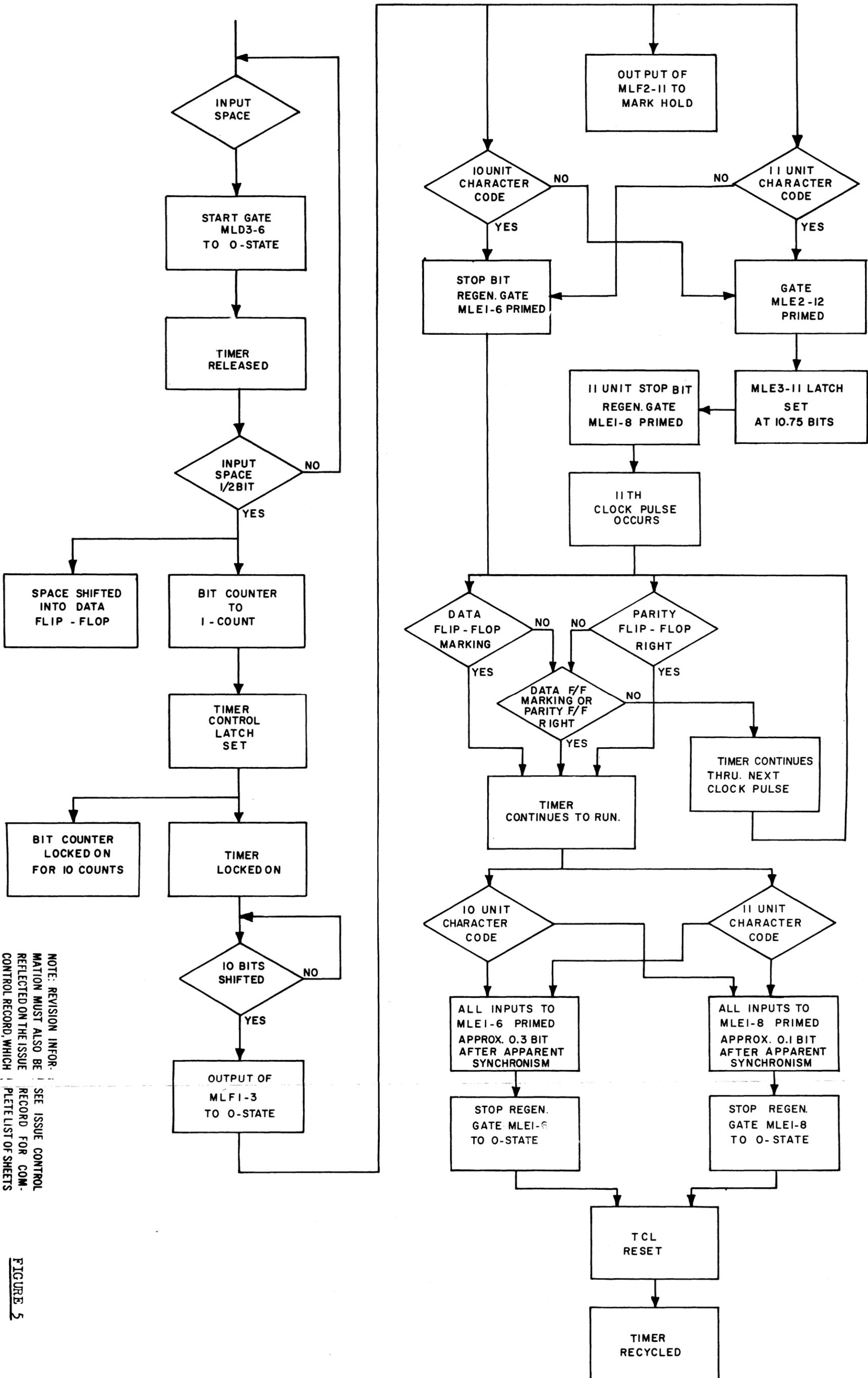


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FIGURE 4

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

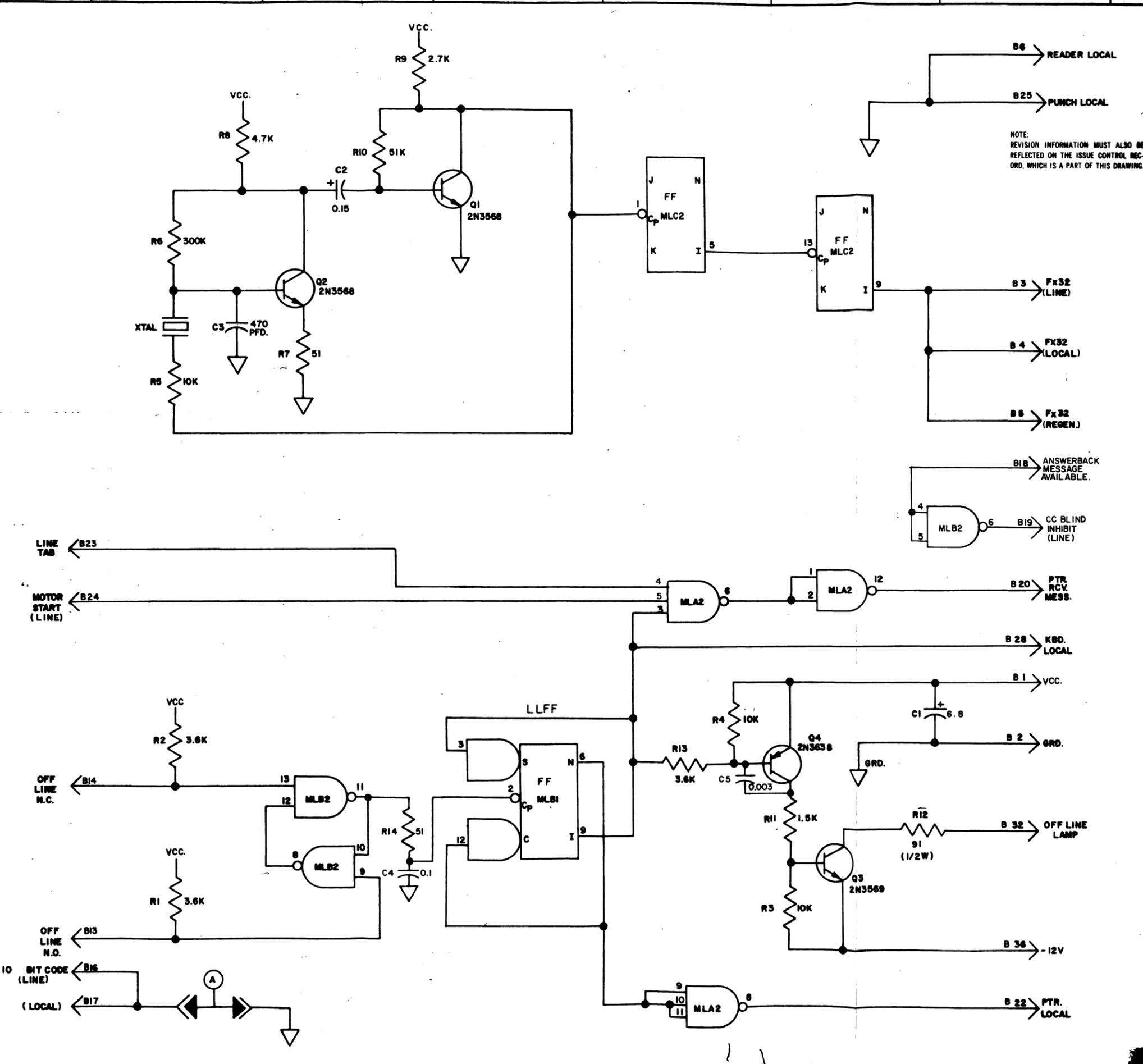


NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS D.W.D.

FIGURE 5

- NO. NOTES
1. ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
 2. ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED.
 3. ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
 4.  INDICATES FEMALE TERMINAL AND  INDICATES MALE TERMINAL
 5. REFER TO 322067 FOR ASSEMBLY INFORMATION.
 6. S NUMBER: 61516 S.
 7. INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD:
ML D 2
└── ROW
└── COLUMN
└── INTEGRATED CIRCUIT
 8. THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY.
 9. LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
 10. WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
 11. VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
 12. REFER TO 8999WD FOR TRUTH TABLES.
 13. OPTIONS:
A - 10-11 BIT CODE.  ADD STRAP FOR 10 BIT CODE.
 14. REFERENCE CIRCUIT DESCRIPTION: 8387 WD-CD.
 15. ABBREVIATIONS USED:
LLFF - LINE LOCAL FLIP-FLOP



8387 WD

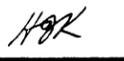
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ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R
2	10-22-68	96395

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SCHEMATIC WIRING DIAGRAM FOR KSR MODE CONTROL

APPROVALS

D AND R	E OF M
	

E-NUMBER

PROD. NO. 8387 WD

DATE 9-9-68

P.D. FILE NO. 6-A384AA

DRAWN W.P.B. CHKD. 

ENGR. REL. APPR. 

TELETYPE CORPORATION

8387 WD

CIRCUIT DESCRIPTION OF THE KSR MODE CONTROL CARD
(ASSEMBLY NUMBER 322067)

TABLE OF CONTENTS

<u>SECTION</u>	<u>DESCRIPTION</u>	<u>TOTAL PAGES IN SECTION</u>
I	General Technical Information	3
II	Detailed Description and Theory of Operation	3

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE KSR MODE CONTROL CARD
(ASSEMBLY NUMBER 322067)

SECTION I

1. BASIC FUNCTION

1.1 The 322067 Circuit Card Assembly is a mode control and set clock for Model 37 KSR sets operating at 150 wpm with 10 unit code (150 baud).

1.2 Two mutually exclusive mode selections are provided by one switch:

A. OFF-LINE

B. ON-LINE

1.3 The mode control circuit is associated with a switch and a 30 ma @24V lamp on the control panel located above the keyboard.

1.3.1 When the switch is lighted, the set is in the "OFF-LINE" (local) mode.

1.3.2 When the switch is not lighted, the set is in the "ON-LINE" mode.

1.3.3 Fixed outputs are provided to maintain any punch or reader, which may be associated with the set, in the "OFF-LINE" mode.

2. GENERAL TECHNICAL DATA (All card pins appear on the "B" (non-component) side of the card.)

2.1 Input Characteristics

The inputs to the assembly are positive nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +5.25V and 0V respectively. A logic one (high) draws no current from the input of the logic element.

2.1.1 "OFF-LINE" Mode-Switch (N.O. Pin 13, N.C. Pin 14)

The momentary break-before-make transfer mode switch generates a square pulse through a latch circuit, formed by a pair of gates, and into the toggle input of a J-K flip-flop. The flip-flop changes output state each time the mode switch is pressed. The device driving this input must be capable of sinking two DTL loads. (See General Timing Diagram)

2.1.2 Motor Start (Pin 24)

This pin is low to start the printer and punch motors during "ON-LINE" operation and is one DTL load.

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2.1.3 Line Tabulation (Pin 23)

This pin is low throughout any tabulation function which is started while the printer is "ON-LINE" and high at all other times. The device driving this input must be capable of sinking one DTL load.

2.1.4 Answer Back Message Available (Pin B18)

This lead is low throughout any Answer Back cycle. It is high at all other times. The device driving this input must be capable of sinking one DTL load.

2.2 Output Characteristics

2.2.1 Off-Line Lamp (Pin 32)

When the flip-flop output, MLB1 Pin 9 is low, the lamp associated with the "OFF-LINE" switch is lighted by a lamp driver circuit, Q3 and Q4 (Pin 32) which applies approximately 24 volts across the bulb.

2.2.2 Keyboard Local (Pin 28)

The output of the flip-flop is also routed off the card to control other circuitry in the set and will be low during the "OFF-LINE" (Local) mode (Pin 28). This output is capable of driving 7 DTL loads.

2.2.3 Printer Local (Pin 22)

This pin is low when the "OFF-LINE" (Local) mode is selected, (same as Pin 28), and is capable of driving 8 DTL loads.

2.2.4 Punch Local (Pin 25)

This pin is low at all times and will keep any associated punch in the "OFF-LINE" mode at all times.

2.2.5 Reader Local (Pin 6)

This pin is low at all times and will keep any associated reader in the "OFF-LINE" mode at all times.

2.2.6 Set Clock (Internal to Card)

The set clock is a crystal controlled multivibrator operating at 128 times the bit rate (19.2KHZ @ 150 baud). (See General Timing Diagram)

2.2.7 Clock Pulse (Pin 3,4,5)

The set clock frequency is divided by four by a pair of flip-flops and is available as an output of 32 times the bit rate and is capable of driving ten DTL loads.

2.2.8 10-11 Bit Code Selection (Pins 16, 17)

Strap A is provided to ground the 10 bit input lead on the electronic distributor used in the set. If this strap is removed, an 11 bit code will be generated, but a different crystal is required to obtain the correct bit rate as indicated in Section 2.2.5.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.2.9 Printer Receive Message (Pin 20)

A low on this pin indicates to the printer that its motor should be started. This pin will be low when in the "OFF-LINE" mode or during tabulation on-line, or when "motor start" is low. This output is capable of driving eight DTL loads.

2.2.10 Control Character Blind Inhibit (Line) (Pin B19)

This output in the 0-state, inhibits the line distributor from pausing for one character interval, following the transmission of a control character. This output is capable of driving eight DTL loads.

2.3 Mechanical Requirements

The 322067 card assembly is a standard 5-3/4 inch by 4-1/4 inch 36-pin circuit card which is inserted into a 36-pin edge card connector.

2.4 Power Supply Requirements

<u>Vcc(DC)</u>	<u>Current Maximum</u>
+5.0V - +6.6V (+5.25V Nom.)	60 ma
+11.65V - +13.75V (+12.5V Nom.)*	30 ma
-11.13V - -13.88V (-12.5V Nom.)	30 ma

* +12.5 Volts is used for the lamps.

2.5 Temperature Range

The ambient temperature range for operation is from 0°C to 70°C in free air. Non-operating storage temperature is from -40°C to 70°C.

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SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

- 1.1 Assembly and schematic drawings 322067 (MC067) and 8387 WD.
- 1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 Mode Switching

The mode switch is comprised of a momentary contact transfer switch (break before make) containing a lamp indicator. When the switch is operated, the normally closed contact opens first enabling the input to the associated gate, which is part of a latch arrangement. The input of this gate is held low, however, by the other half of the latch associated with the normally open contact. Next, the normally open contact closes, driving the input of its associated gate low and switching the output high. The output of the gate associated with the normally closed contact then switches low, causing a high to low transition on the input to the J-K flip-flop, changing its state. (The output of the J-K flip-flop changes state each time a high to low input transition occurs on the input.)

When the mode switch is released, the normally open contact returns to its open condition and enables the input to its associated gate. Next, the normally closed contact returns to its closed condition, putting a low input on its gate, which returns the output of the latch to a high. This low to high transition occurs on the input to the J-K flip-flop, but has no effect on its output.

The output of the flip-flop drives a lamp through an amplifier (Pin 32), and also leaves the card to control other circuitry (Pin 22 and 28).

2.2 Lamp Driver

A low input to the lamp driver provides a current path through the 3.6K resistor and from the base of a PNP transistor. The transistor turns on, and provides a bias current through the 1.5K ohm resistor to turn on the NPN transistor. This transistor acts as a switch connecting the lamp from the +12.5 volt supply, through a 91 ohm limiting resistor, to the -12.5 volt supply. Thus the lamp is turned on.

2.3 Set Clock

2.3.1 The set clock is a crystal controlled, astable multivibrator composed of Q1 and Q2 operating at 128 times the bit rate. The transistors are arranged as grounded emitter inverting amplifiers with R7 providing

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some stabilization and feedback for Q2 and R10 providing bias for Q1. R6 provides collector feedback and base bias for Q2. C2 couples the output of Q2 to the base input of Q1. A quartz crystal provides feedback from the collector of Q1 through current limiting resistor R5 and into the base of Q2 at the critical frequency of the crystal. A negative transition on the C2 base momentarily turns it off, thus causing a positive transition to be coupled by C2 into the Q1 base, momentarily turning it on and causing a negative transition to be coupled through the crystal and again momentarily turn Q2 off. C2 decouples oscillations of higher harmonics that might occur due to stray capacitances associated with the crystal.

The output of Q1 is also connected to the input of the J-K flip-flop, where every negative transition causes a change in the state of its output, thus dividing the frequency in half. This signal is again divided in half by the other J-K flip-flop. The clock signal leaves the card as Fx32.

2.4 Motor Control (Line)

Punch and printer motors are turned on whenever the set is either in the "OFF-LINE" mode, or when a message is being received "ON-LINE". Additionally, the typing unit motors are held "on" while tabulating "ON-LINE", even though a message has been completed.

2.4.1 A "motor start" signal, signifying that a message is present "ON-LINE", enters the assembly and is gated with the keyboard local and line tabulation signals, and is then inverted, so that the "Printer Receive Message" output will be low when a "motor start" signal is received, or when the keyboard is in the "local" mode.

2.5 Control Character Blind Inhibit

The control character blind is a 13 bit marking interval following the transmission of every control character. This delay is necessary to provide sufficient time for the printer to execute any one of its control functions, before beginning to receive the next character. 116

A low on Pin B19 inhibits the delay feature on the line distributor. The delay is disabled during all Keyboard transmission, because Answer Back Message Available is high during this time keeping MLB2-6 low. Whenever the Answer Back is sending, Answer Back Message Available is low, enabling the delay by keeping MLB2-6 high.

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SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

GENERAL TIMING DIAGRAM

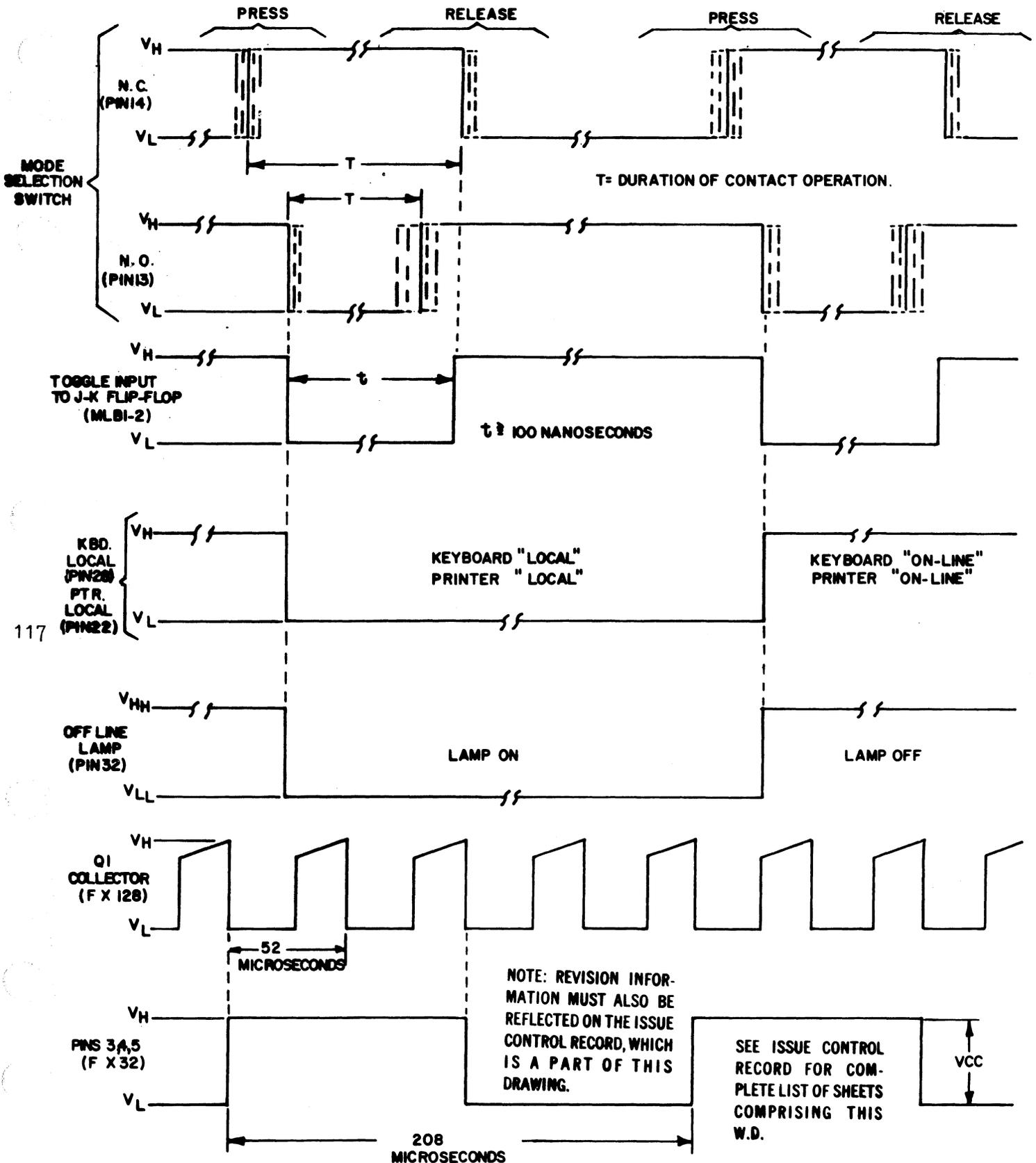


FIGURE 1

8388WD

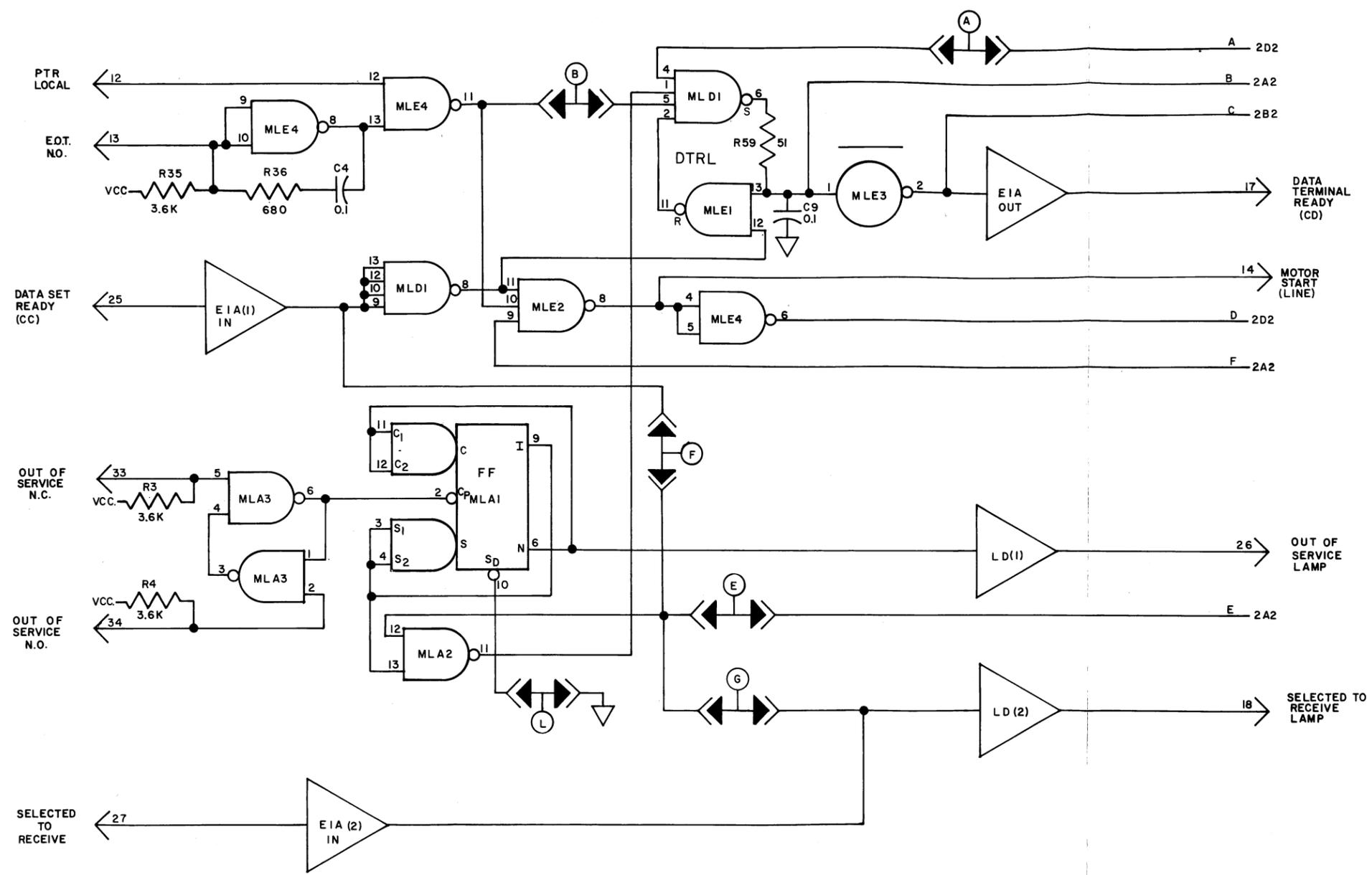
REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

NOTE:
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- NO. NOTES**
- ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
 - ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
 - ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
 - INDICATES FEMALE AND
 - INDICATES MALE TERMINALS
 - REFER TO 322068 FOR ASSEMBLY INFORMATION.
 - S NUMBER: 61,521S.
 - INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD:
 - CROSS REFERENCE NOTATION ON SCHEMATIC
 - LOGIC NEGATION: A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
 - WHEN ALL INPUTS OF A NANDGATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
 - VCC IS PROVIDED TO THE INTEGRATED CIRCUIT PACKAGE ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
 - SEE 8399WD FOR TRUTH TABLES.
 - THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY.
 - CARD OPTIONS:
STRAP MUST BE ADDED TO OBTAIN OPTION.

STRAP	OPTION
A	ALARM DISCONNECT.
B	EOT DISCONNECT.
C	PRIVATE LINE MOTOR CONTROL DISCONNECT.
D	PRIVATE LINE MOTOR CONTROL ENABLE.
E	PRIVATE LINE OUT OF SERVICE ENABLE.
F	DATAPHONE OUT OF SERVICE ENABLE.
G	PRIVATE LINE OUT OF SERVICE ENABLE.
H	BREAK DETECT DISABLE.
K	SEND BREAK ON PARITY ERROR.
L	OUT OF SERVICE DISABLE.
M	SEND BREAK DISABLE
Y	PROCEED CONTROL DISABLE
 - REFERENCE CIRCUIT DESCRIPTION: 8388WD-CD.
 - ABBREVIATIONS USED:
MCL - MOTOR CONTROL LATCH.
MTL - MARK TIME LATCH.
RIL - RECEIVE INTERRUPT LATCH.
PCL - PROCEED CONTROL LATCH.
DTRL - DATA TERMINAL READY LATCH.
 - INDICATES CIRCUIT GROUND.



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SHEET 1

SCHEMATIC WIRING DIAGRAM FOR CHANNEL CONTROL

APPROVALS

D AND R <i>HJR</i>	E OF M <i>[Signature]</i>
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E-NUMBER
 PROD. NO. 8388 WD.
 DATE 3-29-68
 P.D. FILE NO. G-A354AA
 DRAWN W.P.B. CHKD. *[Signature]*
 ENGD. C.A.Y. APPD. *[Signature]*

TELETYPE CORPORATION

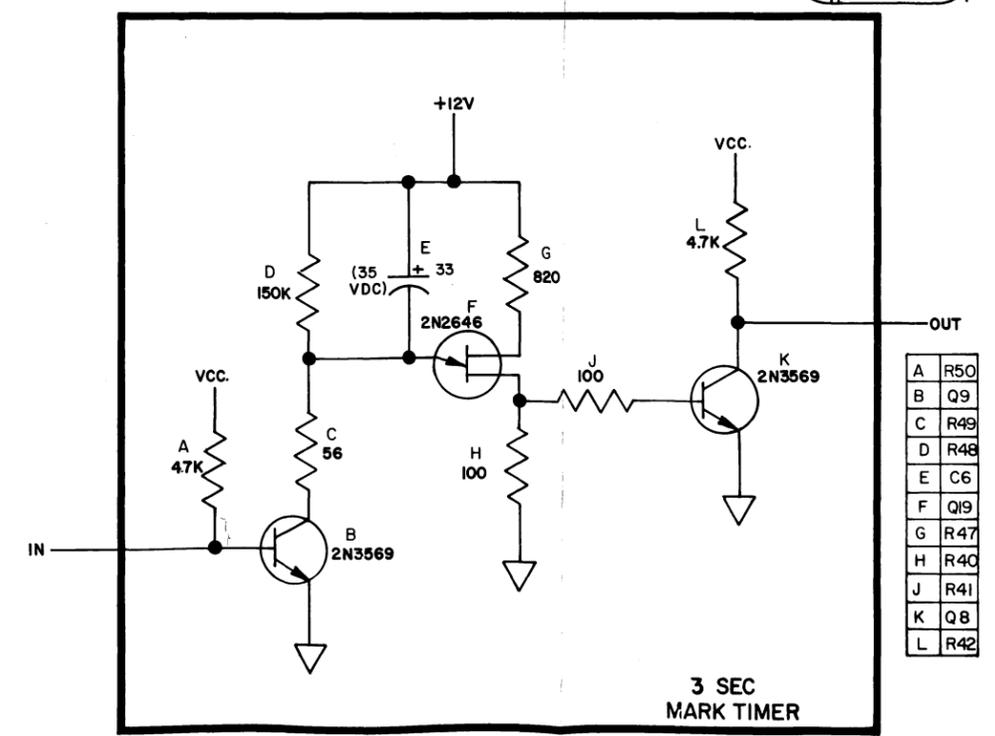
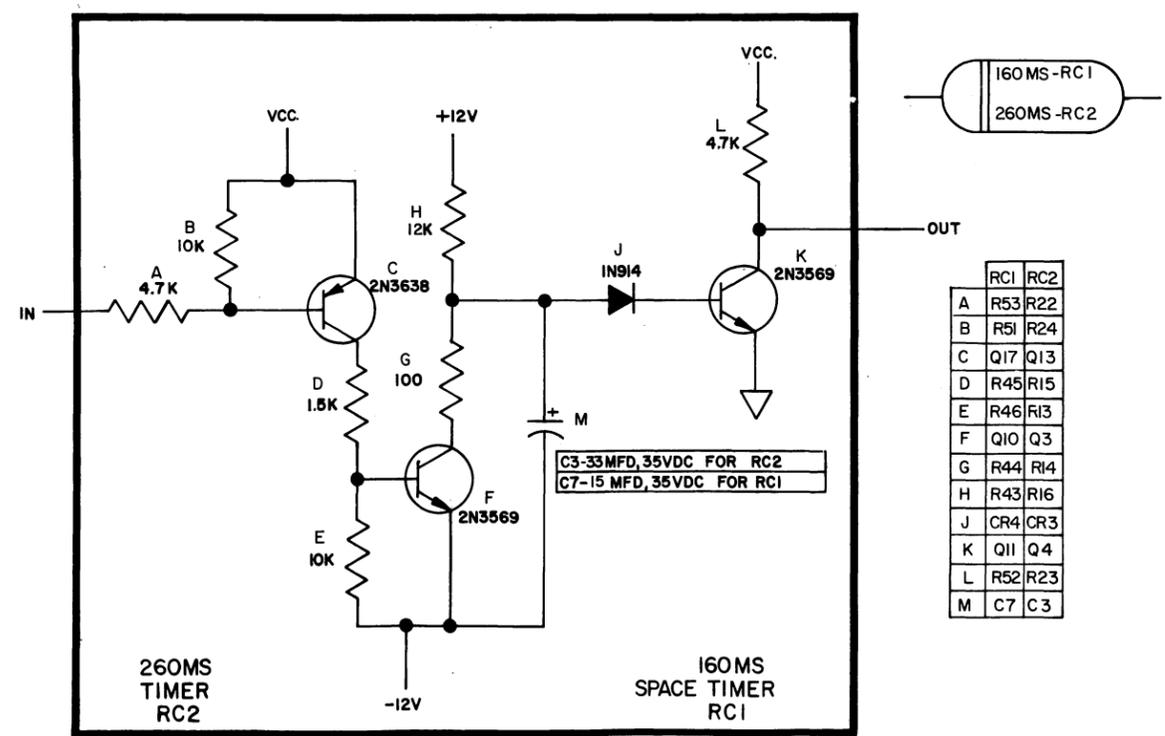
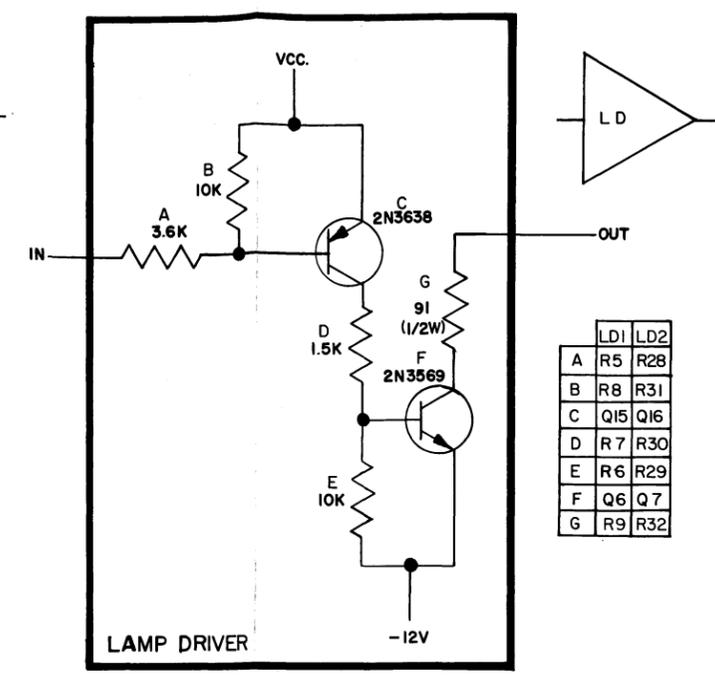
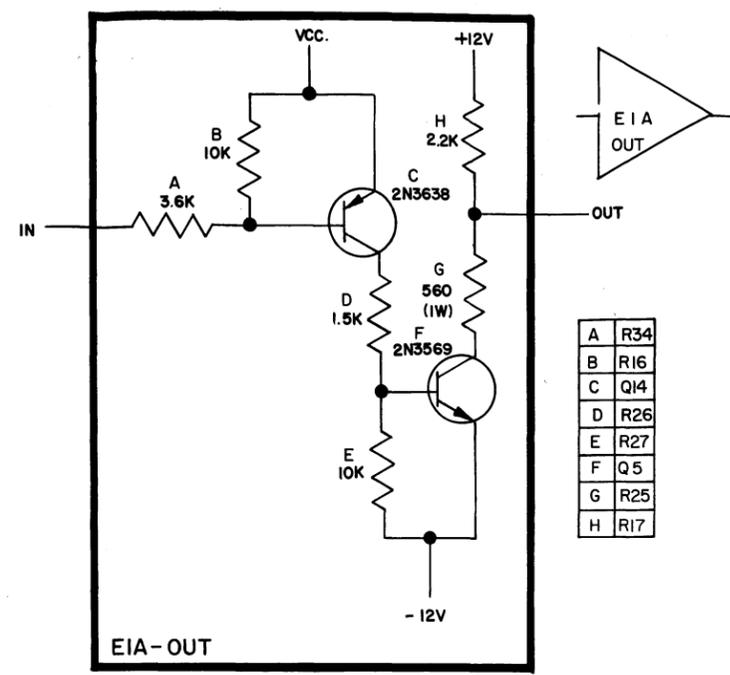
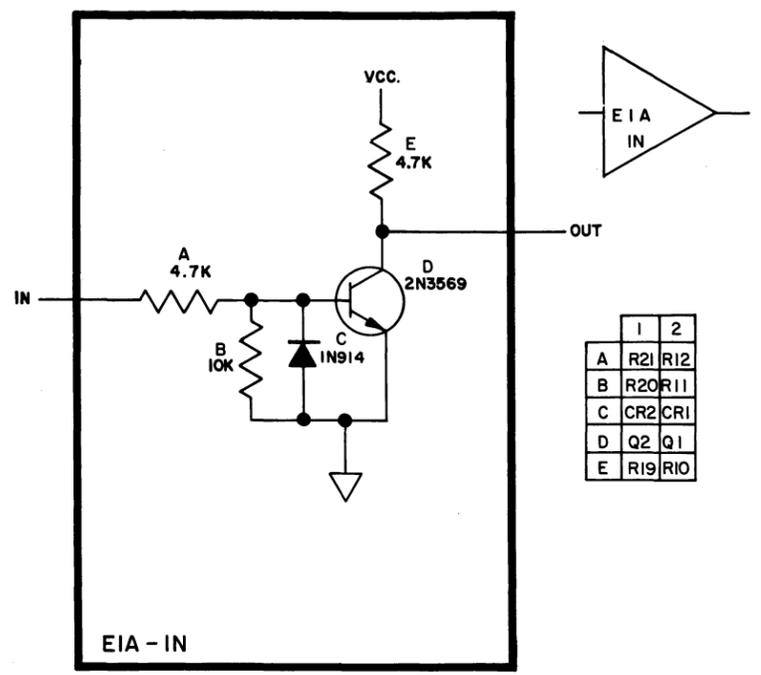
8388WD

8388WD

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W.D.

SHEET 3

SCHEMATIC
WIRING DIAGRAM
FOR
CHANNEL
CONTROL

APPROVALS

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E-NUMBER

PROD. NO. 8388WD.

DATE 1-2-68

P.D. FILE NO. G-A354AA

DRAWN RJP

CHKD. *[Signature]*

ENGD. CAY

APPD. *[Signature]*

TELETYPE
CORPORATION

8388WD

CIRCUIT DESCRIPTION OF THE CHANNEL CONTROL CARD
(ASSEMBLY NUMBER 322068)

TABLE OF CONTENTS

<u>SECTION</u>	<u>DESCRIPTION</u>	<u>TOTAL PAGES IN SECTION</u>
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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.	SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.
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CIRCUIT DESCRIPTION OF THE CHANNEL CONTROL CARD
(ASSEMBLY NUMBER 322068)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322068 Circuit Card Assembly provides information to the data set or other line interface unit about the receiving status of the terminal and accepts information about the line connection status of the terminal.

1.2 Additional Features

Timed Send interrupt generation

Timed Receive interrupt detection

On-Line Motor start control for switched or non-switched service

On-Line transmission control

Out of service, do not answer

2. GENERAL TECHNICAL DATA

2.1 Input Characteristics

The inputs to the assembly are positive nand type integrated Diode Transistor Logic (DTL) inputs. Each DTL input is approximately a 1.4 ma load to the device sinking current from it. At no time should any of these inputs be more positive than 8 volts or more negative than -.7 volts. Voltage levels represented by the 1-state (high) and 0-state (low) are approximately +6V and 0V respectively. A logic one (high) draws no current from the input of the logic element.

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2.1.1 Line Receive Data (Pin 9)

This pin is high when data is not being received or when the signal line is MARKING, and goes low when the signal line is SPACING. Interrupt, a space on line of at least 195 m.s., will appear on this pin.

2.1.2 Line Send Data (Pin 10)

This pin is high when data is not being sent or when a mark is being sent, and will go low when space is sent on line.

2.1.3 Proceed N.O. (Pin 20)

This lead is normally high and goes low when the proceed switch is operated. This low will reset the Proceed Control Latch (PCL).

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.1.4 ACK N.O. (Pin 19)

This lead is normally high and goes low when an ACK character is detected in the printer function box. This low will reset the Proceed Control Latch (PCL).

2.1.5 NAK N.O. (Pin 23)

This lead is normally high and goes low whenever a NAK character is detected in the printer function box. This low will set the Proceed Control Latch (PCL).

2.1.6 Receiver in Alarm (Pin 29)

This lead is normally high and goes low when a line receiver goes into an alarm condition. A low on Pin 29 starts a SEND INTERRUPT signal and resets the Data Terminal Ready Latch (DTRL).

2.1.7 Interrupt Switch (N.O. Pin 32) (N.C. Pin 31)

These pins accept a break-before-make transfer switch, with the common terminal grounded. Operating the switch starts a send interrupt signal.

2.1.8 Parity Error Received (Pin 30)

A low on this pin starts a send interrupt signal.

2.1.9 Printer Local (Pin 12)

This pin must be made low when the printer function box is "off-line" (local).

2.1.10 EOT N.O. (Pin 13)

This pin must be made low momentarily when the ASCII character EOT is detected by the printer function box.

2.1.11 Data Set Ready (Pin 25) (EIA Lead CC)

The voltage, current, impedance and logic characteristics of this lead are defined by EIA Specification RS232B.

2.1.12 Out of Service Switch (N.O. Pin 34) (N.C. Pin 33)

These pins accept a break-before-make transfer contact with grounded common terminal. Operating the switch turns on the out of service lamp, and causes the line interface unit (e.g. Dataphone Data Set) not to answer any calls.

2.1.13 Selected to Receive (Pin 27)

The voltage, current, and impedance characteristics of this lead are defined by Section 4 of EIA Specification RS232B.

NOTE: REFERENCE INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.1.13 (Continued)

When the lead is "ON", the set will be prepared to receive a message and the "selected to receive" lamp will light.

2.2 Channel Control Outputs

2.2.1 Normalize (Pin 22)

This lead is low when there is no on-line call in process. The lead is used to restore circuits affecting on-line operation to a pre-selected "Normal" state after a call.

2.2.2 Send Interrupt (Pin 28)

This lead goes low for approximately 200 to 350 m.s. when the SEND INTERRUPT circuit is operated.

2.2.3 Halt (Pin 21)

This lead goes low when sending on-line is not permitted.

2.2.4 Selected to Receive Lamp (Pin 18)

See Section I, Paragraph 2.1.13 above.

2.2.5 Out of Service Lamp (Pin 26)

See Section I, Paragraph 2.1.12 above.

2.2.6 Motor Start (Pin 14)

This pin goes low when a call is in process, and is used to start all set motors.

2.2.7 Data Terminal Ready (Pin 17) (EIA Lead CD)

The voltage, current, impedance, and logic characteristics of this lead are defined by EIA Specification RS232B.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

1.1 Assembly and Schematic Drawing 322068 (MC068) and 8388WD, respectively.

1.2 . Logic symbols and truth tables per 8399WD.

2. DETAILED DESCRIPTION AND THEORY OF OPERATION

2.1 MOTOR CONTROL

The MOTOR START lead (Pin 14) low, starts all set motors. The conditions permitting "MOTOR START" are variable by strap option on the channel control card.

Output 8 of MLE2 controls "MOTOR START" and will be low only when Inputs 9, 10 and 11 of MLE2 are high.

MLE2 Input 9 controlled by MCL Section II, Paragraph 2.2.3 below
MLE2 Input 10 controlled by EOT Section II, Paragraph 2.2.2 below
MLE2 Input 11 controlled by DSR Section II, Paragraph 2.2.1 below

2.2 Switched Service Motor Control

In switched service, "MOTOR START" is controlled by "DATA SET READY" Pin 25 (EIA Lead CC). If the set motors are to be stopped or kept from starting by some condition in the terminal, "DATA TERMINAL READY" (Pin 17 - EIA Lead CD) will be turned off. The line interface unit must recognize DTR off as a request for "Disconnect" when DSR is on, and as a request for "DO NOT ANSWER" when DSR is off.

2.2.1 DATA SET READY (DSR) (EIA LEAD CC)

When Pin 25, "DATA SET READY" is high (per EIA Specification RS232B), amplifier A-1 is turned on, holding Inputs 9, 10, 12 and 13 of MLD1 low. Output 8 of MLD1 drives Input 11 of MLE2 high.

If Inputs 9 and 10 of MLE2 are also high, "MOTOR START" (Pin 14) will turn on (low).

Amplifier A-1 output is also connected to Strap F, to control the "OUT OF SERVICE" option. See Section II, Paragraph 3.2.3 below.

2.2.2 End of Transmission (EOT)

Input 10 of MLE2 will be low during the time that "EOT N.O." (Pin 13) is low and "PRINTER LOCAL" (Pin 12) is high. If Strap "B" is installed, the same signal will reset DTRL, turning off "DATA TERMINAL READY" (Pin 17 - EIA Lead CD).

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SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

NOT REVISION MATERIAL MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

2.2.3 Motor Control Latch (MCL)

For switched service, MCL is held reset, by installing Strap C, holding Input 9 of MLE2 high.

2.3 Private Line Motor Control (Non-Switched Service)

In non-switched service, DSR (Pin 25) may be on continuously, indicating that the line interface unit is always ready to operate. The set motors will run continuously.

If this condition is undesirable, the optional idle line motor turn off circuit may be enabled by removing Straps C, F and M, and installing Straps D and E.

2.3.1 Data Set Ready

The line interface unit should keep Data Set Ready (Pin 25) ON continuously, keeping Input 11 of MLE2 high (See Section II, Paragraph 2.2.1 above).

2.3.2 End of Transmission (EOT)

Output 11 of MLE4 will be momentarily low when EOT is detected (See Paragraph 1.12 above). Input 10 of MLE2 will be low, turning off "MOTOR START" (Pin 14) and turning on "NORMALIZE" (Pin 22) through MLE4 Output 6. Strap "D", installed, allows this signal to set MCL and MTL. MCL, Set, holds Input 9 of MLE2 low, keeping "MOTOR START" (Pin 14) off.

2.3.3 Idle Line Turn-Off

Timer E, nominally 3 seconds, sets the MARK TIMER LATCH (MTL) and the MOTOR CONTROL LATCH (MCL) when timed out. MCL, Set, holds Input 9 of MLE2 low, keeping "MOTOR START" (Pin 14) off. Timer E is saved (kept from timing out), by low (Spacing) signals on Pin 9, "LINE RECEIVE DATA", or Pin 10 "LINE SEND DATA". Either of these low inputs will force Output 6 of MLE4 high, Output 10 of MLE3 low, and Output 12 of MLE3 high. (MLE3 Output 12, low, shunts the base of Q9, allowing Timer E to time out. MLE3-12, high, allows Q9 to turn on, with base current through R50. The high state of MLE3 Output 12 will be voltage limited to the base emitter drop of Q9, about 0.6 volts. Measurements to determine the "ON" or "OFF" state of inverter MLE3-12 must be made at MLE3 Input 13).

2.3.3.1 Automatic Motor Turn Off

Uninterrupted marking (high) on line data Pins 9 and 10 for 3 seconds (nominal) allows Timer E to time out, setting MTL and MCL. Input 9 of MLE2 is held low by MCL Set and the motors stop.

2.3.3.2 Re-start from Automatic Stop

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. | SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

2.3.3.2.1 REMOTE Re-Start

A spacing signal (low) on either Pin 9 or Pin 10 resets MTL and saves Timer E. MTL, Reset, places a high on Input 4 of MLE1. When Pin 9 "LINE RECEIVE DATA" and Pin 10 "LINE SEND DATA" are both high, Input 5 of MLE1 will also be high. With Inputs 4 and 5 of MLE1 high, Output 6 of MLE1 will go low, resetting MCL. MCL Reset places a high on Input 9 of MLE2, and the set motors will start.

Since the set motors are not started until the signal line (Pins 9 and 10) is again marking in both directions, the receiving devices at the called terminal will detect a single ASCII "DELETE" character.

2.3.3.2.2 LOCAL Re-Start

The set motors are re-started in an originating terminal by sending INTERRUPT.

When INTERRUPT is sent, (see Section II, Paragraph 5 below) Inputs 9 and 10 of MLE2 are high, forcing Output 8 low, and resetting MCL. MCL Reset places a high on Input 9 of MLE2. If EIA Lead CC (Data Set Ready) is not off, and EOT is not received, the set motors will start. The receivers in the calling terminal do not detect spacing on line when INTERRUPT is sent. No "Hit" characters are generated.

The called station set motors are started on RECEIVE INTERRUPT as described in Section II, Paragraph 2.3.3.2.1 above. Receivers in the called station will detect one ASCII "Delete" character.

3. TERMINAL STATUS (DATA TERMINAL READY)

Data Terminal Ready (Pin 17 - EIA Lead CD) is driven by amplifier B. A low input to amplifier B drives Pin 17 negative, indicating to the line interface unit that the terminal is not ready to operate.

3.1 General

Three optional conditions are available to turn off Data Terminal Ready

Receiver in Alarm	Section II, Paragraph 3.2.1
EOT	Section II, Paragraph 3.2.2
Out of Service	Section II, Paragraph 3.2.3

Any one of these conditions will reset DTRL, placing a high on Input 1, of MLE3, forcing Output 2 of MLE3 and the input of amplifier B low. This turns off Data Terminal Ready. The reset condition must be removed before DTRL can be set. DTRL is set by a low on Output 8 of MLD1, which is low when Data Set Ready, EIA Lead CC, Pin 25 is OFF (Negative on Pin 25).

If Data Set Ready (Pin 25) is on continuously, as in non-switched service, DTRL cannot be set and none of the terminal status options should be used.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

3.2. Additional Outputs

DTRL Set output is connected to Input 3 of MLE3 to perform a transmitter control function. See TRANSMITTER CONTROL, Section II, Paragraph 4 below.

Output 2 of MLE3 is connected to Input 1 of MLF4 to inhibit detection of RECEIVED INTERRUPT when Pin 17, Data Terminal Ready, is low.

3.2.1 Receiver in Alarm

RECEIVER IN ALARM (Pin 29) is low when the condition of the line receivers prevents terminal operation, e.g. Paper out etc. See Specification Number 61434 for a description of the conditions on RECEIVER IN ALARM.

Strap A, installed, permits RECEIVER IN ALARM, low, to reset DTRL.

Pin 29, low, also initiates SEND INTERRUPT. See Section II, Paragraph 5 below for a description of the SEND INTERRUPT circuit.

3.2.2 EOT Received On Line (See Section II, Paragraph 2.2.2)

3.2.3 Out of Service

3.2.3.1 General

The Out of Service option allows the operator to disable the terminal. This may be desirable during routine maintenance. (Changing forms, printer ribbons, etc.)

The option is enabled by removing Strap "L", and is operative only when the terminal is idle. The idle condition of the terminal is determined on the basis of strap options depending on the type of service in which the terminal is being used.

3.2.3.2 Operation

The lighted "OUT OF SERVICE" transfer switch is connected to Pins 33 and 34. Cycling the switch produces a single positive to negative transition on the toggle input of the "OUT OF SERVICE" flip-flop, ML1 Input 2, causing the flip-flop to change state. When Output 6 of ML1 is low, the "OUT OF SERVICE" lamp will be lighted.

The inverse output of ML1, Output 9, is connected to Input 13 of ML2 and will be high when the "OUT OF SERVICE" lamp is lit.

When Input 12 of ML2 is also high, Output 11 of ML2 will be forced low, resetting DTRL. DTRL, reset, turns off Data Terminal Ready (Pin 17).

Three straps are provided for optional control of ML2 Input 12, depending on the type of service in which the terminal is being used.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.



3.2.3.2 (Continued)

Strap F installed: "OUT OF SERVICE" reset DTRL when "Data Set Ready" EIA lead CC, Pin 25, is off. Used in switched service.

Strap G installed: "OUT OF SERVICE" resets DTRL when "Selected to Receive" Pin 27, is off. Used in some non-switched services.

Strap E installed: "OUT OF SERVICE" resets DTRL when MCL is set. The set motors are stopped when MCL is set. Used with idle line turn off, in non-switched service.

4. TRANSMITTER CONTROL

HALT, Pin 21 is provided to inhibit on line transmission. The signal acts on the send control circuit (8382WD-CD;KSR sets or 8381WD-CD; ASR Sets) to light the "PROCEED" lamp when transmission is permitted.

The "HALT" signal should inhibit all transmitting devices except the answerback. This allows the answerback in a called terminal to generate the character which removes "HALT" (ACK).

"HALT", Pin 21 may be operated by the RECEIVE INTERRUPT circuit; see Section II, Paragraph 6 below.

4.1 "HALT", Pin 21, is controlled by the PROCEED CONTROL LATCH, (PCL). When PCL is set, Inputs 3, 4, and 5 of MLC4 are high and Output 6 is low, holding "HALT", Pin 21, low. PCL, reset, forces MLC4 Output 6 high, but "HALT" Pin 21 may be held low by "RECEIVE INTERRUPT". See Section II, Paragraph 6 below.

4.2 PCL Set (HALT in Effect)

4.2.1 NAK

Detection of the ASCII character NAK causes a contact closure on Pin 23, "NAK N.O.", setting PCL.

4.2.2 NORMALIZE

The "NORMALIZE" output (Pin 22) is derived from the Motor Start lead Pin 14. When Motor Start is high, indicating no MOTOR START, Inputs 4 and 5 of MLE4 are high and Output 6 of MLE4 is low, indicating "NORMALIZE". NORMALIZE sets PCL.

4.2.3 Received interrupt- Delection of interrupt signal sets PCL.

4.3 Proceed Control Latch (PCL) Reset (HALT not in effect)

4.3.1 ACK

Detection of the ASCII character ACK causes a contact closure on Pin 19, "ACK N.O.", resetting PCL.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.



4.3.2 PROCEED Switch

The normally open PROCEED switch, connected to Pin 20, when operated, resets PCL. Operation of the PROCEED switch assumes that "HALT" (Pin 21) will go high.

4.4 PCL Disable

PCL may be held reset by installing Strap Y. This will prevent operation of "HALT" by PCL. Install Strap H to inhibit operation of HALT by RIL.

5. SEND INTERRUPT

The INTERRUPT switch, a break-before-make transfer switch, is connected to Pins 31 and 32. Cycling the switch produces a single positive to negative transition on Input 2 of MLA2. This transition is inverted twice by MLA2-3 and MLA2-6, then integrated by the network C-10 - R60 and applied to the toggle input of MLB1. MLB1 is primed by having "clear" Inputs 11 and 12 connected to Vcc and "Set" Inputs 3 and 4 grounded. This prime causes the negative going transition on Input 2 to drive the Normal output, Output 6, low. Output 6 is connected to Pin 28, send interrupt. Output 9, the inverted output, goes high when Output 6 goes low.

Output 9, high, removes the bias current sink for Q13, which turns off, turning off Q3. Q3 off allows C3 to charge through R16, with a time constant of 330 milliseconds. When the voltage at the anode of CR3 reaches approximately +1.2 volts with respect to ground, Q4 turns on with bias current through R16. The time required to reach turn on will be .806 (330) milliseconds or about 263 milliseconds, nominal.

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Q4, turned on, holds Input 10 of MLB1, the set direct input, low. This drives MLB1 Output 6 high, ending the INTERRUPT, and forces MLB1 Output 9 low. This turns on Q13 and Q3, capacitor C3 discharges through R14 and Q3, and Q4 turns off. When Q4 turns off, the low on MLB1, Input 10 is removed, MLB1 remains set, with Output 6 high, and Output 9 low, until another positive to negative transition is detected at MLB1 Input 2.

The SEND INTERRUPT circuit is also triggered, as described above, when "RECEIVER IN ALARM" (Pin 29) is low. For the conditions under which "RECEIVER IN ALARM" is low, see Specification No. 61,434.

6. RECEIVED INTERRUPT

RECEIVED INTERRUPT timer RC1 controls PCL, which can operate "HALT" (Pin 21).

"INTERRUPT" is detected on Pin 9, LINE RECEIVE DATA, and is defined as a continuous Space on Line of more than 205 ms. LINE SEND DATA (Pin 10) must not contain the "SEND INTERRUPT" signal, generated by MLB1 and RC2.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

6. (Continued)

Pin 9, "LINE RECEIVE DATA" is low when the received data lead from the line interface unit is spacing. Output 6 of MLF4 will be high, holding Input 2 of MLF4 high. If DTRL is set, indicating that the terminal is ready to operate, Input 1 of MLF4 will also be high, and output 3 of MLF4 will be forced low. This drives Output 8 of MLE3 high, removing the bias current sink for Q17, the input transistor of RC1. Q17 turns off, turning off Q10. Q10 off allows C7 to charge through R43. When the anode of CR4 reaches approximately +1.2V DC with respect to ground, Q11 turns on with bias current through R43.

C-7 charges to +1.2V in approximately .806 (12K ohms)(15 mfd) = 144 ms.

Q11, turned on, sets PCL, forcing "HALT" low.

"HALT", low, should act on the send control card (8381WD-CD) to turn off the "PROCEED" lamp, and inhibit transmission from keyboard (KSR Sets) or keyboard and reader (ASR Sets).

The "RECEIVE INTERRUPT DETECTION" circuit may be disabled by installing Strap H.

REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

8389WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-25-68	19568-R

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET-1

SCHEMATIC WIRING DIAGRAM FOR TWO COLOR RIBBON CONTROL

APPROVALS

D AND R <i>HR</i>	E OF M <i>✓</i>
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E-NUMBER

PROD. NO. 8389WD.

DATE 4-19-68

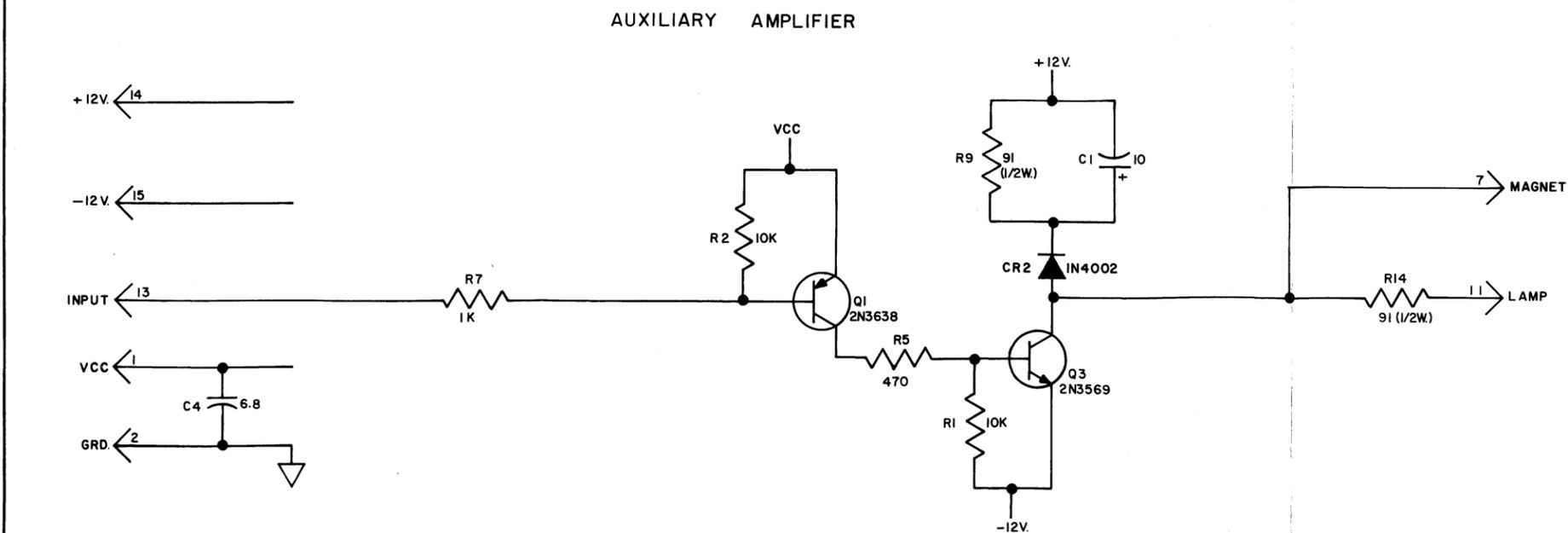
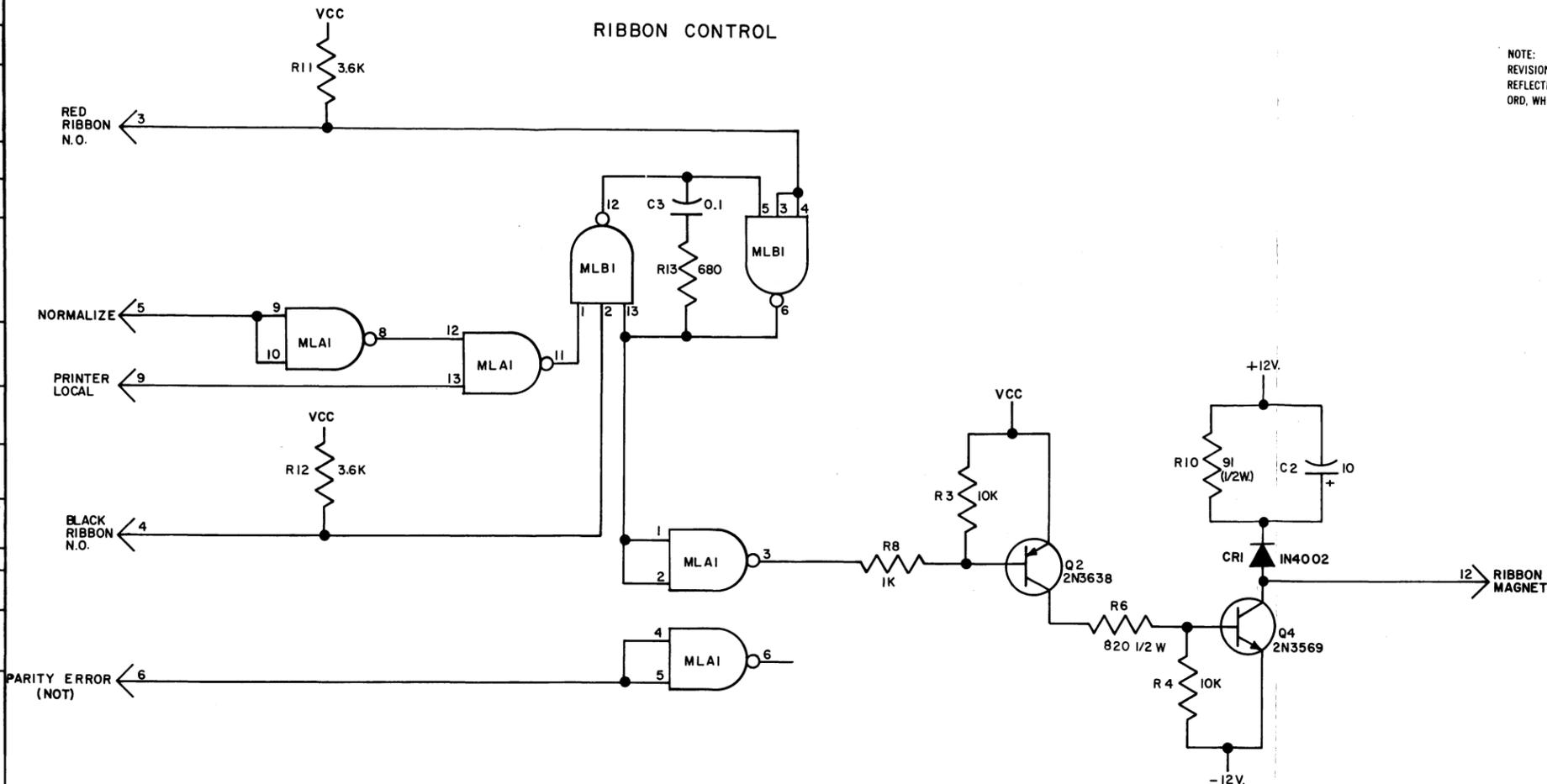
P.D. FILE NO. G-A354AA

DRAWN W.P.B.	CHKD. <i>HR</i>
ENGD. R.E.L.	APPD. <i>HR</i>

TELETYPE CORPORATION

8389WD

- NO. NOTES
- ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
 - ALL RESISTORS 1/4 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
 - ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
 - INDICATES FEMALE AND
 INDICATES MALE TERMINAL
 - REFER TO 322070 FOR ASSEMBLY INFORMATION.
 - S NUMBER: 61,510 S.
 - INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD:
 - THE INCLUDED SCHEMATIC UTILIZES POSITIVE LOGIC. VOLTAGE LEVELS REPRESENTED BY THE 1-STATE AND 0-STATE ARE VCC AND 0V, RESPECTIVELY.
 - LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
 - WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER, THE GATE IS USED AS AN INVERTER.
 - VCC IS PROVIDED TO THE INTEGRATED CIRCUIT ON PIN 14 AND GROUND ON PIN 7, THIS APPLIES TO ALL PACKAGES.
 - REFER TO 8399WD FOR TRUTH TABLES.
 - REFERENCE CIRCUIT DESCRIPTION 8389WD-CD.
 - INDICATES CIRCUIT GROUND.



CIRCUIT DESCRIPTION OF THE TWO COLOR RIBBON CONTROL CARD
(ASSEMBLY NUMBER 322070)

TABLE OF CONTENTS

<u>SECTION</u>	<u>DESCRIPTION</u>	<u>TOTAL PAGES IN SECTION</u>
I	General Technical Information	3
II	Detailed Description and Theory of Operation	2

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NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

CIRCUIT DESCRIPTION OF THE TWO COLOR RIBBON CONTROL CARD
(ASSEMBLY NUMBER 322070)

SECTION I

GENERAL TECHNICAL INFORMATION

1. BASIC FUNCTION

1.1 The 322070 Two Color Ribbon Control Card performs the function of ribbon color selection (red or black) upon receipt of proper control signals.

1.2 Additional Features

1.2.1 An additional driver is available for application as a solenoid driver or lamp driver. (Optional suggested use would be to light a lamp upon receipt of SHIFT IN or OUT code.)

1.2.2 The ribbon mechanism is reset to black ribbon at the end of a call ("ON-LINE" mode).

1.3 Ribbon Magnet

The ribbon magnet sinks a steady state current of 230 ma DC (nominal) when a logic zero is present on ML11 Pin 3 and is in the off state when a logic one is present.

1.4 Auxiliary Driver

When operating as a solenoid driver, the DC resistance of the winding must be at least 110 ohms in order to stay within the safe operating area of Q3. If operated as a lamp driver, a 24 volt DC lamp must be used, (recommended lamp Part No. 327061).

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1.5 Two-Color Ribbon (Option)

The two-color ribbon control card is an option. It must be provided whenever two-color printing is a terminal requirement. The card plugs into a pre-wired printed circuit card connector and requires no field assembly or adjustment.

2. GENERAL TECHNICAL DATA

2.1 Input-Output Data

2.1.1 The ribbon magnet driver converts the integrated circuit logic inputs to current levels appropriate for ribbon magnet operation.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

A logic one is defined as a voltage level between +5.0 volts and +6.6 volts (usually a logic one approximates the integrated circuit supply voltage). A logic one draws no current from the input of the logic element.

Signal voltages between circuit ground potential and +0.5 volts are considered logic zero. Logic currents that flow into the signal source are a function of the element driven, supply voltage, and the value of pull-up resistor used, if any. For additional loading information refer to the manufacturer's specification.

2.2 Input Characteristics

2.2.1 Red Ribbon N.O. (Pin 3)

This input is normally high except during receipt of a red ribbon signal. In Model 37 application, Pin 3 is connected to a N.O. stunt box contact which closes for approximately 20 ms when red printing is desired. The driving source must be capable of sinking approximately two DTL loads. (One DTL load approximately equals 1.4 ma.)

2.2.2 Normalize (Pin 5)

The NORMALIZE input resets the ribbon mechanism to black ribbon when the printer is ON-LINE. This input is high at all times except when a NORMALIZE signal is present. The driving source must be capable of sinking one DTL load.

2.2.3 Printer Local (Pin 9)

This input is low when the printer is operated in the LOCAL mode and high in the ON-LINE mode. The driving source must be capable of sinking one DTL load.

2.2.4 Black Ribbon N.O. (Pin 4)

This input is normally high except during receipt of a BLACK RIBBON signal. In Model 37 application, Pin 4 is connected to a stunt box contact which closes for approximately 20 ms when black printing is desired. The driving source must be capable of sinking one DTL load.

2.2.5 Parity Error Not (Pin 6)

The PARITY ERROR NOT input is low (LOCAL or ON-LINE mode) as long as proper coding exists and high when a parity error exists. The driving source must be capable of sinking one DTL load.

2.2.6 Input-Auxiliary Driver (Pin 13)

The input characteristics were designed to be compatible with DTL integrated circuit logic elements. A logic one (high) input causes current to flow through the load. A logic zero (low) results in no current flow through the load. The driving source must be capable of sinking approximately three DTL Loads.

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IS A PART OF THIS
DRAWING.
W.D.

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REFLECTED ON THE ISSUE
CONTROL RECORD, WHICH
IS A PART OF THIS
DRAWING.

2.2.7 Input Ribbon Magnet Driver (MLA1 Pin 3)

Refer to Section I - 2.2.6.

2.3 Output Characteristics

2.3.1 Auxiliary Driver

The auxiliary driver circuit is a two stage amplifier designed to operate full on or full off without intermediate levels. The collector circuit of Q3 contains a transient suppression network consisting of CR2, R9 and C1. When used as a lamp driver, RL4 limits lamp surge current to a value within safe operating limits.

2.3.2 Ribbon Magnet

The ribbon magnet driver is a two stage amplifier designed to operate full on or full off without intermediate levels. The collector circuit of Q4 contains a transient suppression network consisting of CR1, R10, and C2. The output circuit is matched to the ribbon magnet assembly. The impedance values of the output circuit have been chosen to provide equal pick-up and drop-out times at some level of ribbon magnet armature spring tension.

2.4 Mechanical Requirements

The 322070 Card Assembly is a standard 15 pin circuit card which is inserted into a 15 pin edge card connector.

2.5 Power Supply Requirements

<u>Vcc (DC)</u>	<u>Current (ma) Max.</u>
+5.0V - +6.6V	125 ma
+11.65V - +13.75V (+12.5V Nom.)	500 ma
-11.13V to -13.88V (-12.5V Nom.)	500 ma

2.6 Temperature Range

The operating temperature range is from 0°C to 70°C in free air. The storage temperature range is from -40°C to +70°C.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING. SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SECTION II

DETAILED DESCRIPTION AND THEORY OF OPERATION

1. ASSOCIATED DOCUMENTS

- 1.1 Assembly and schematic drawings 322070 (MC070) and 8389 WD.
- 1.2 Logic symbols and truth table 8399 WD.

2. DETAILED DESCRIPTION

2.1 Ribbon Magnet Driver

Assume the printer is "ON-LINE" and a terminal is receiving and printing data in black, (ribbon magnet de-energized). Under these conditions Pins 3, 5, 9; 4 are high, Pin 6 is low, MLAl Pin 3 is high, MLBl Pin 13 is low, and MLBl Pin 12 is high. Assume a "RED RIBBON" bit sequence has been detected by the stunt box and Pin 3 goes low for approximately 20 ms. Latch MLBl Pin 13 changes states. MLBl Pin 13 is high, MLBl Pin 12 is low, and MLAl Pin 3 is low. A low level (logic zero) input to the ribbon magnet driver causes collector current to flow through R4 and R6. The current flow through R4 results in a positive signal at the base of Q4 (NPN transistor). Q4 is turned full on and the ribbon magnet assembly is energized. The printer now prints the data in red. The ribbon magnet will remain energized until the end of the transmitted message at which time a "NORMLIZE" pulse (low) resets MLBl (Pin 13 low, Pin 12 high) or a "BLACK RIBBON" bit sequence is detected by the stunt box and Pin 4 goes low for approximately 20 ms.

175 Assume a "NORMLIZE" pulse (low) has been received on Pin 5. A low on MLAl Pin 11 resets MLBl latch (Pin 12 high, Pin 13 low) and MLAl Pin 3 is now high. Collector current ceases to flow through R4 which results in a negative going pulse at the base of Q4. Q4 is turned off and the ribbon magnet is de-energized. The ribbon magnet assembly has been reset to black printing.

If a "BLACK RIBBON" bit sequence detected by the stunt box causes Pin 4 to go low while printing in red, MLBl latch is reset (Pin 12 high, Pin 13 low) and MLAl Pin 3 high. Q4 is now in the "off" state and the ribbon magnet is de-energized. The ribbon magnet assembly has been reset to black printing.

In the "LOCAL" or "ON-LINE" mode, a PARITY ERROR results in a shift from black ribbon to red ribbon. The driver and ribbon magnet assembly is capable of switching from black to red and from red to black within one character time. The ribbon magnet is energized when Pin 6 goes high (MLAl Pin 6 low). The "PARITY ERROR NOT" input has direct control over the driver when Pin 6 is high.

When operating in "LOCAL" mode, Pin 9 is low and MLAl gate is disabled (MLAl Pin 11 high). MLBl latch is now under direct control of the "Red Ribbon" and "Black Ribbon" inputs.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.	SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.
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R13 and C3 constitute an RC noise filter. Noise voltages caused by stunt box contact closures or undesirable bounce are integrated so MLB1 latch does not switch to the wrong state.

The transient suppression network consisting of CR1, R10 and C2 dissipates the energy stored in the ribbon magnet winding when Q4 is turned off. This network prevents large inductive voltage spikes from avalanching Q4 collector to emitter.

The two stage auxiliary driver is identical to the ribbon magnet driver. Refer to Section I - 2.2.6 and 2.3.1 for information concerning input and output characteristics, respectively.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

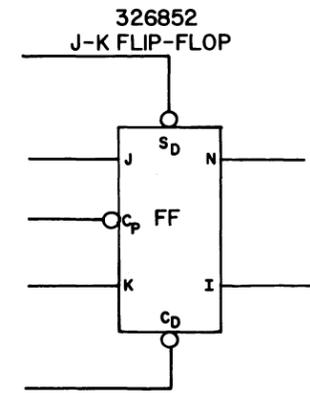
SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

REVISIONS

ISSUE	DATE	AUTH. NO.
-1	5-3-68	19208-R

- NO. NOTES**
- GRAPHICAL SYMBOLS AND THE ASSOCIATED TRUTH TABLES ILLUSTRATED ON THIS PAGE ARE TYPICAL SYMBOLS USED IN TELETYPE CORPORATION APPARATUS.
 - LOGIC NEGATION - A SMALL CIRCLE (O) DRAWN AT THE POINT WHERE A SIGNAL LINE JOINS A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
 - STATE DESIGNATIONS:
1- STATE = +6V
0- STATE = 0V
 - WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USED AS AN INVERTER.
 - ABBREVIATIONS USED:
O- LOW STATE (MORE NEGATIVE)
1- HIGH STATE (MORE POSITIVE)
X- STATE OF INPUT DOES NOT AFFECT STATE OF CIRCUIT
NC- NO CHANGE
U- INDETERMINATE STATE

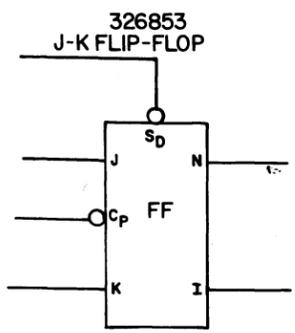
N_M- STATE OF N AT TIME M.
 \overline{N}_M - INVERSION OF STATE OF N AT TIME M.



326852
J-K FLIP-FLOP

ASYNCHRONOUS TRUTH TABLE 326852

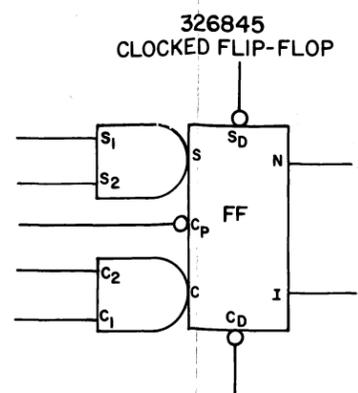
S _D	C _D	N	I
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1



326853
J-K FLIP-FLOP

ASYNCHRONOUS TRUTH TABLE 326853

S _D	N	I
1	NC	NC
1	0	1
0	1	0



326845
CLOCKED FLIP-FLOP

ASYNCHRONOUS TRUTH TABLE 326845

C _D	S _D	N	I
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	1	1

SYNCHRONOUS TRUTH TABLE 326845

S ₁	S ₂	C ₁	C ₂	N
0	X	0	X	NC
0	X	X	0	NC
X	0	0	X	NC
X	0	X	0	NC
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

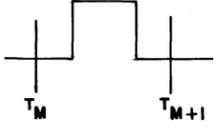
J-K TRUTH TABLES (CONNECT S₂ TO I, C₂ TO N)

T _M	T _{M+1}
S ₁	C ₁
0	0
1	0
0	1
1	1

J-K TRUTH TABLE BOTH TYPES

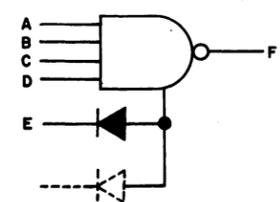
T _M	T _{M+1}
J	K
0	0
1	0
0	1
1	1

CLOCKED PULSE WAVE FORM



ASYNCHRONOUS INPUTS, DIRECT SET (S_D) AND DIRECT CLEAR (C_D), OVERRIDE THE SYNCHRONOUS INPUTS. THEY ARE INDEPENDENT OF ALL OTHER INPUTS.

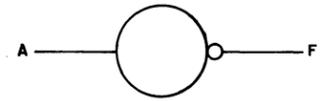
NAND GATE



A	B	C	D	E	F
1	1	1	1	1	0
1	0	0	0	0	1
0	0	0	0	0	1
0	1	1	1	1	1

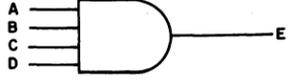
A, B, C, D OR E LOW (0) CAUSES F TO GO HIGH (1)

INVERTER



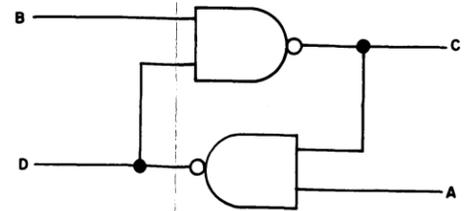
A	F
0	1
1	0

GATE EXTENDER



E = A · B · C · D

SET-RESET FLIP-FLOP UTILIZING NAND GATES



A	B	C	D
0	0	1	1
0	1	0	1
1	0	1	0
1	1	NC	NC

LOGIC SYMBOLS AND TRUTH TABLES

APPROVALS

D AND R	E OF M
<i>[Signature]</i>	<i>[Signature]</i>

E-NUMBER

PROD. NO. 8399WD

DATE 2-12-68

P.D. FILE NO. G-A354AA

DRAWN RJP

ENG. MJR

CHKD. *[Signature]*

APPD. *[Signature]*

TELETYPE CORPORATION

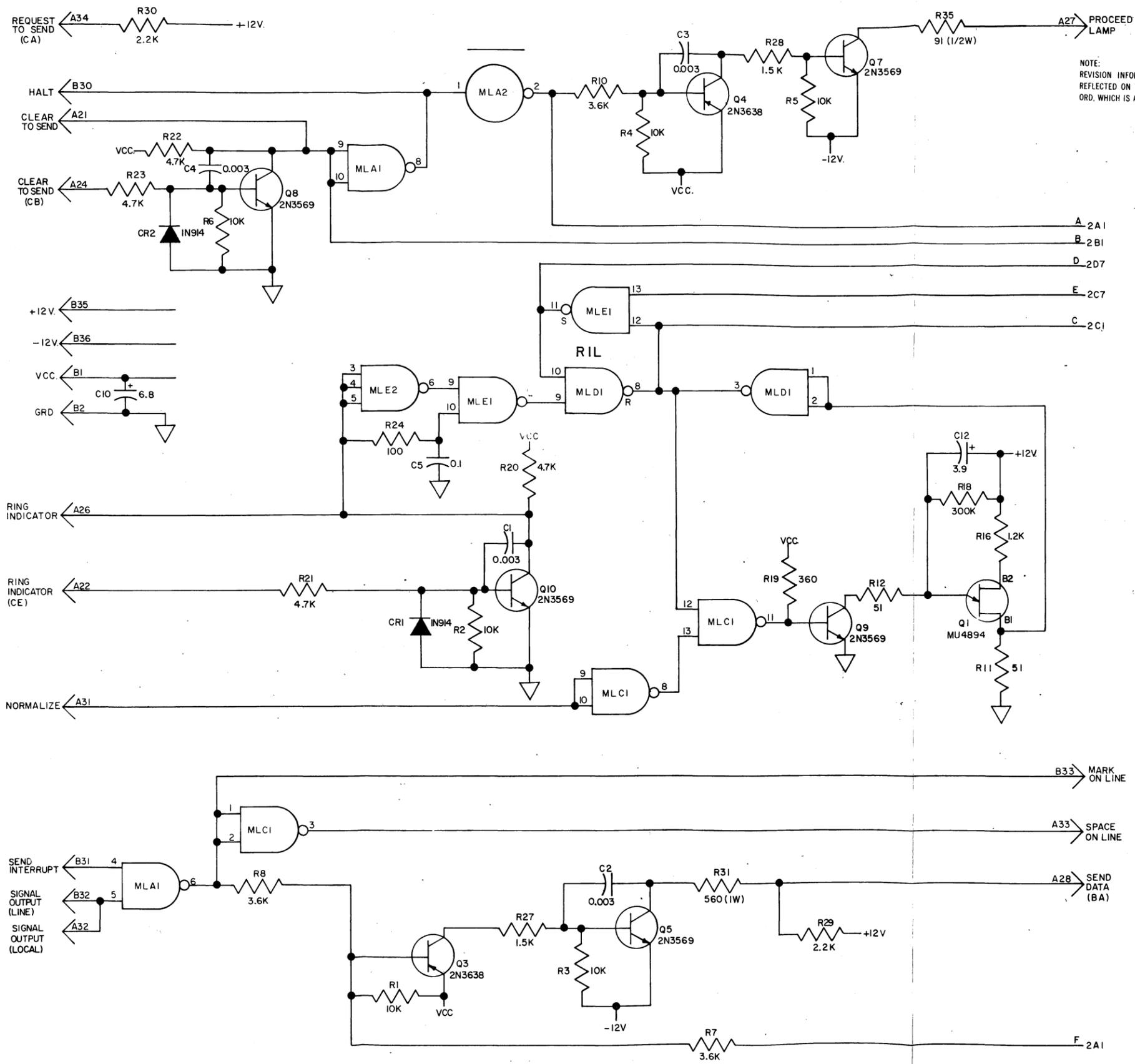
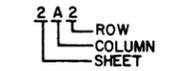
8773WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	11-21-68	19778R

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING.

- NO. NOTES
- REFER TO 322304 FOR ASSEMBLY INFORMATION.
 - S-NUMBER - 61,618S.
 - ALL RESISTORS 1/4 WATT, AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
 - ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
 - ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
 - INTEGRATED CIRCUIT PACKAGE LOCATION ON CIRCUIT BOARD.
 - CROSS REFERENCE NOTATIONS ON SCHEMATIC.
 - LOGIC NEGATION - A SMALL CIRCLE JOINED TO A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
 - STATE DESIGNATIONS:
I - STATE = VCC.
O - STATE = 0V.
 - REFER TO 8399 WD FOR TRUTH TABLES.
 - WHEN ALL INPUTS OF A NAND GATE ARE TIED TOGETHER THE GATE IS USED AS AN INVERTER.
 - VCC IS PROVIDED TO THE INTEGRATED CIRCUIT ON PIN 14, AND GROUND ON PIN 7. THIS APPLIES TO ALL PACKAGES.
 - REFERENCE CIRCUIT DESCRIPTION 8773W.
 - ABBREVIATIONS USED:
RIL - RING INDICATOR LATCH.
CNL - CONTENTION LATCH.
CSL - CHARACTER SENT LATCH.



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W.D.

SHEET 1

SCHEMATIC WIRING DIAGRAM FOR KSR SEND CONTROL

APPROVALS

D AND R	E OF M
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E-NUMBER

PROD. NO. 8773WD

DATE 9-30-68

P.D. FILE NO. G-A354AA

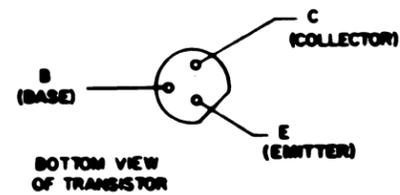
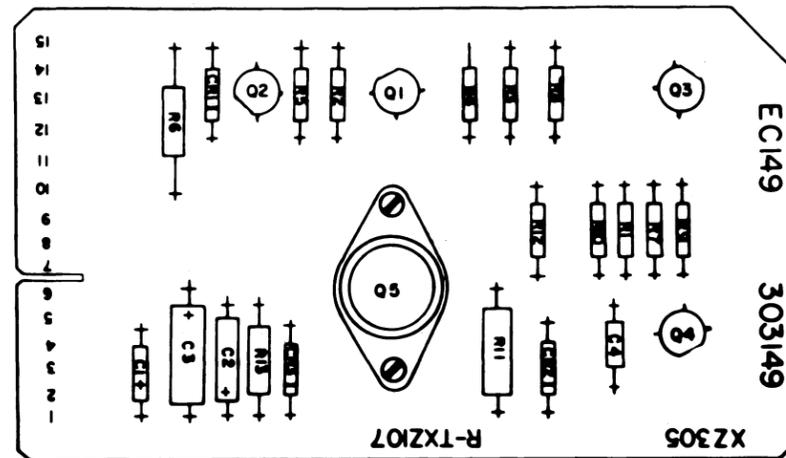
DRAWN WPB CHKD. *[Signature]*

ENG. CAY. APPD. *[Signature]*

TELETYPE CORPORATION

8773WD

- NO. NOTES
- SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.
 - REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY
 - ASSOCIATED SCHEMATICS 8370WD



Q1-3-4

CIRCUIT CARD EC				
REF. DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
R1-2	315958	2	RES. FIXED 3.6K	1/4W
R3	320275	1	" " 10K	1/4W
R4	315954	1	" " 1.5K	1/4W
R5	320275	1	" " 10K	1/4W
R6	182514	1	" " 91	1/2W
R7	315958	1	" " 3.6K	1/4W
R8	320275	1	" " 10K	1/4W
R9	320276	1	" " 470	1/4W
R10	321507	1	" " 1.8K	1/4W
R11	139336	1	" " 150	2W
R12	321213	1	" " 1K	1/4W
R13	118724	1	" " 220	1/2W
C1	327831	1	CAPACITOR DISC 6.8 MFD 6V DC	
C2	326591	1	" TANT. 3.9 MFD 35V DC	
C3	326592	1	" TANT. 33 MFD 35V DC	
C4	326752	1	" .03 MFD 50V DC	
Q2	324656	1	TRANSISTOR 2N3569	
Q3	315931	1	" 2N3638	
Q4	326594	1	" 2N3767	
CR1	321949	1	DIODE 1N4002	
CR2	197464	1	" 1N914	
CR3	321949	1	" 1N4002	
	326508	1	BOARD ETCHED CIRC.	
	3598	2	NUT	
	154335	2	SCREW	
	107116	2	LOCKWASHER	

303149

REVISIONS		
ISSUE	DATE	AUTH. NO.
6	11-15-68	96464-1

WDP

SHEET 1

RECEIVING
DEVICE

APPROVALS

R AND D	E OF M
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E-NUMBER
PROD NO 303149

DATE 8-11-67
R&D FILE G-A354AA
DRAWN R. J. P. CHKD
ENGD M. J. R. APPD

TELETYPE CORPORATION

303149

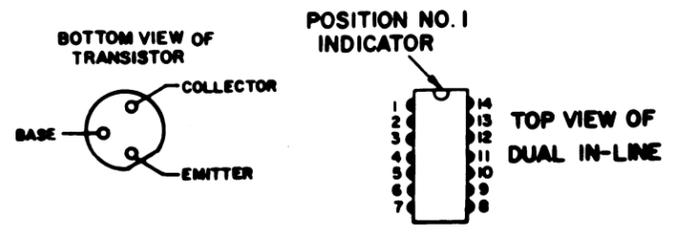
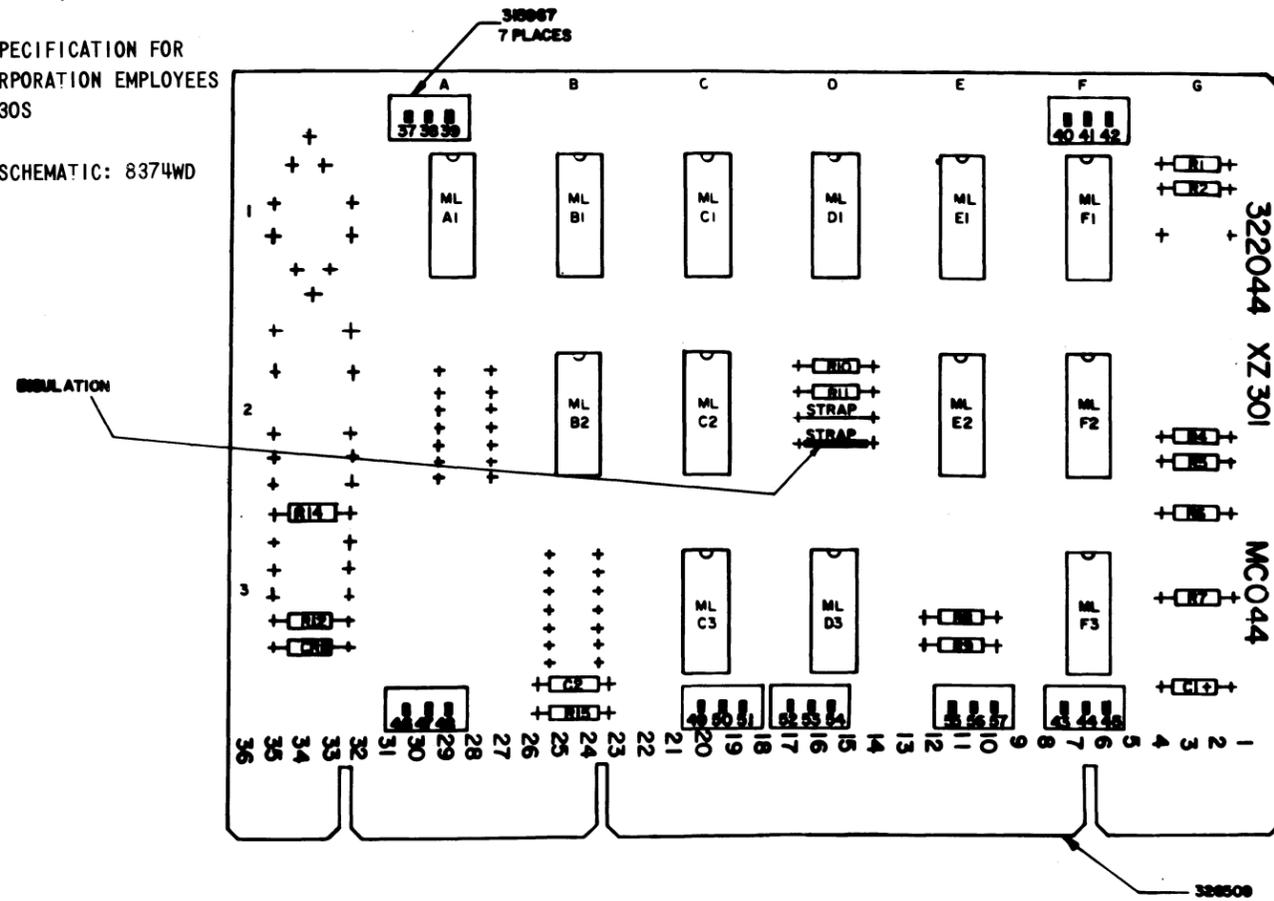
NO. NOTES

1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD
 ML D 2
 ROW
 COLUMN
 INTEGRATED CIRCUIT

2 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

3 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY: 61,430S

4 ASSOCIATED SCHEMATIC: 8374WD



CIRCUIT CARD EC			
REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION
MLA1	326830	1	INTEGR. CIRC.
MLB1	326862	1	" "
MLC1	326862	1	SAME AS MLB1
MLD1	326846	1	INTEGR. CIRC.
MLE1	326846	1	SAME AS MLD1
MLF1	326846	1	" " "
MLB2	326846	1	" " "
MLC2	326846	1	" " "
MLE2	326846	1	" " "
MLF2	326846	1	" " "
MLC3	326832	1	INTEGR. CIRC.
MLD3	326846	1	SAME AS MLD1
MLF3	326846	1	" " "
R1-R2	315958	2	RESISTOR, 3.6K 1/4 W
R12	315955	1	" 2.2K 1/4 W
R14	315971	1	" 680 1/4 W
R15	315958	8	" 3.6K 1/4 W
C1	327831	1	CAPACITOR 6.8MFD 6V DC
CR1	197464	1	DIODE 1N914
	39603RM	2	STRAP 24 GA .007"
	315967	7	CONTACT STRIP
	326509	1	CIRCUIT BOARD
R15	315947	1	RESISTOR 51 1/4 W
		1	INSULATION
C2	312385	1	CAPACITOR 1 MED 10V

R4-R11

322044

REVISIONS

ISSUE	DATE	AUTH. NO.
-6	11-15-68	96464

WDP

SHEET 1

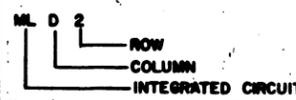
KEYBOARD
CONTROL
LOGIC

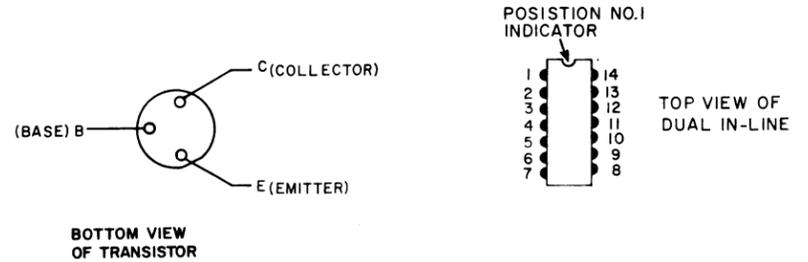
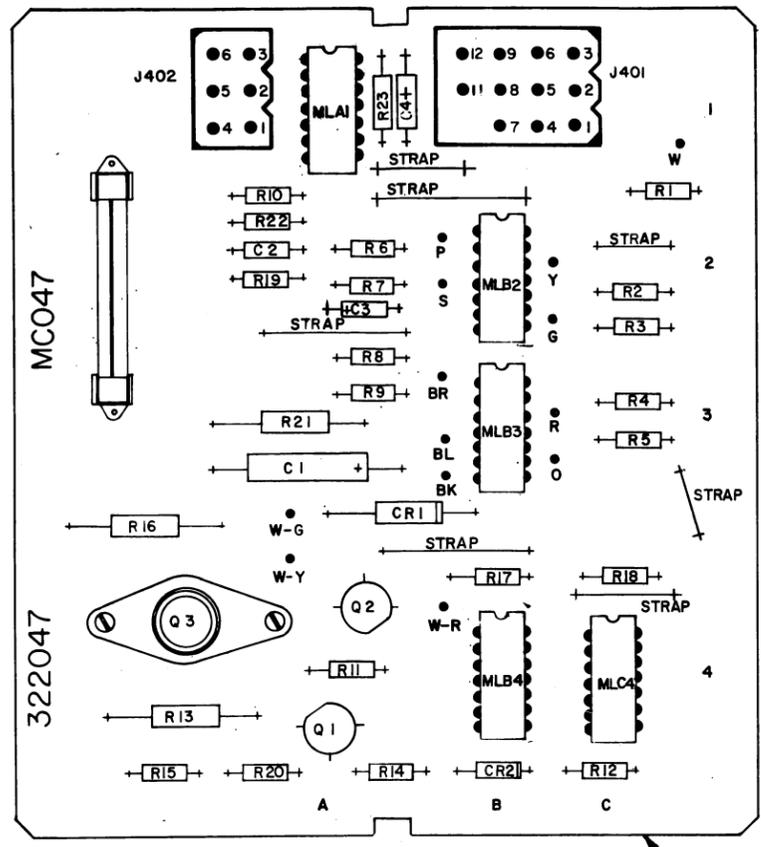
APPROVALS

R AND D	E OF M
<i>[Signature]</i>	<i>[Signature]</i>
Z-NUMBER	
PROG NO. 322044	
DATE 11-9-67	
R&D FILE G-A354AA	
DRAWN R. J. P.	CHKD.
ENGD. C. A. Y.	APPD.

TELETYPE CORPORATION

322044

- NO. NOTES**
- INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD.

 - SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS
 - REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY 614293
 - ASSOCIATED SCHEMATICS ARE: 8376WD.



CIRCUIT CARD MCO47

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1-9	315960	9	RESISTOR FIXED 5.6K 1/4W	
R11	320275	1	RESISTOR FIXED 10K 1/4W	
R12	315971	1	RESISTOR FIXED 680 OHM 1/4W	
R13	199839	1	RESISTOR FIXED 220 OHM 3W	
R14-15	321213	2	RESISTOR FIXED 1K 1/4W	
R16	326303	1	RESISTOR FIXED .68 OHM 1W	
R17-19	315958	3	RESISTOR FIXED 3.6K 1/4W	
R20-22	315948	2	RESISTOR FIXED 100 OHM 1/4W	
R21	143658	1	RESISTOR FIXED 150 OHM 1/2W	
R10,23	315972	2	RESISTOR FIXED 22K, 1/4W	
C1	326590	1	CAPACITOR 10 MFD	
C2	312385	1	CAPACITOR 0.1 MFD	
C3-4	327831	2	CAPACITOR 6.8 MFD, 6VDC	
CR1	321949	1	DIODE 1N4002	
CR2	197464	1	DIODE 1N914	
MLA1	326846	4	INTEGRATED CIRCUIT	
MLB2			SAME AS MLA1	
MLB3			SAME AS MLA1	
MLB4			SAME AS MLA1	
MLC4	326845	1	INTEGRATED CIRCUIT	
Q1	324656	1	TRANSISTOR 2N3569	
Q2	315931	1	TRANSISTOR 2N3638	
Q3	326594	1	TRANSISTOR 2N3767	
	39603RM	7	STRAP 1.2 INCH	
	171595	2	FUSE HOLDER	
	117176	1	FUSE 1/2 AMP. SL BL	
	182641	17	CONNECTOR PINS (MALE)	
	326584	13	CONNECTOR PINS (MALE)	
	326512	1	CIRCUIT BOARD	
	182650	1	6 PIN PLUG J402	
	182647	1	12 PIN PLUG J401	
	151637	4	SCREW 4-40	
	151880	4	NUT	
	3640	4	LOCKWASHER	

322047

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-25-68	19101-R
2	6-7-68	95788
3	8-23-68	96117
4	1-3-69	96485
5	2-27-69	96898
6	6-2-69	96898-1-RC

SHEET 1 OF 2

ANSWER BACK DRIVER

APPROVALS

P AND D <i>APK</i>	E OF M <i>✓</i>
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E-NUMBER

PROD NO 322047

DATE 12-20-67

R&D FILE G-354AA

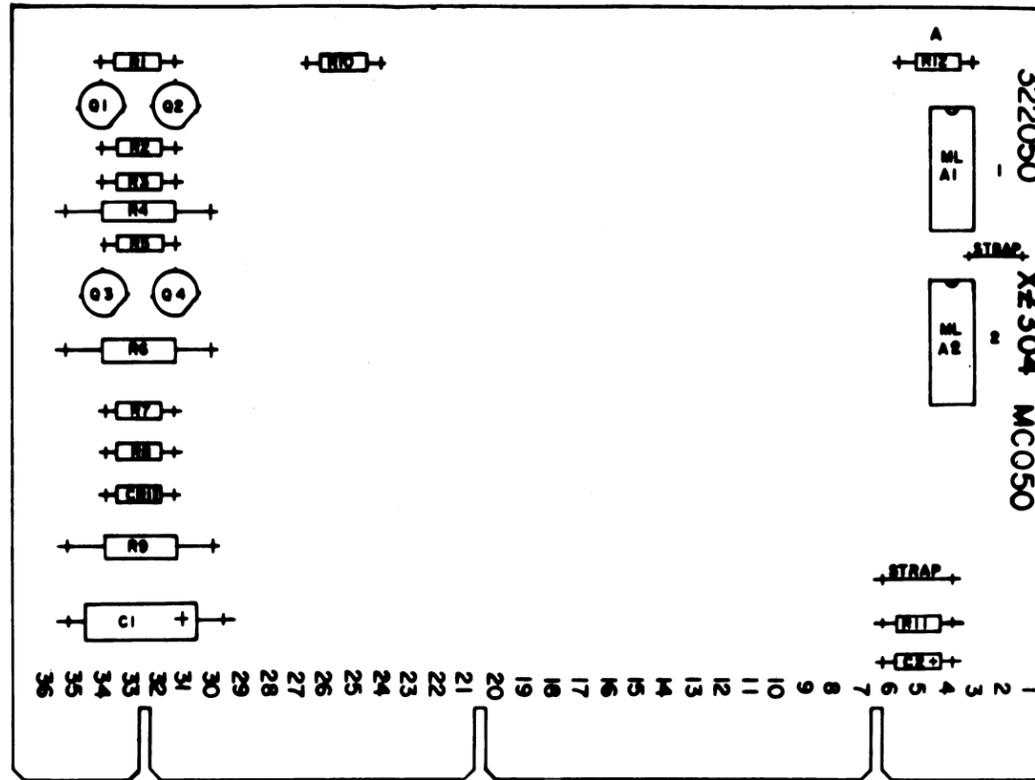
DRAWN WPB CHKD *DEB*

ENGD. REL APPD *DEB*

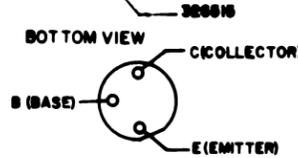
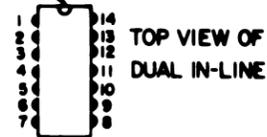
TELETYPE CORPORATION

322047

- NOTES**
- INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD.
 - SEE SPECIFICATION MR2,001 FOR CIRCUIT BOARD REQUIREMENTS.
 - REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY 618198.
 - ASSOCIATED SCHEMATICS ARE: 8377 WD.



POSITION NO. 1 INDICATOR



*R6 IS 470 OHMS ON SOME CARDS

CIRCUIT CARD MC050

REF. DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	328948	1	INTEGRATED CIRCUIT	
MLA2	328948	1	INTEGRATED CIRCUIT	
R1	320275	1	RESISTOR 10K 1/4W	
R2	315954	1	RESISTOR 15K 1/4W	
R3	320275	1	RESISTOR 10K 1/4W	
R4	182514	1	RESISTOR 81 OHMS 1/2W	
R5	320275	1	RESISTOR 10K 1/4W	
*R6	137438	1	RESISTOR 820 OHMS 1/2W	
R7	320275	1	RESISTOR 10K 1/4W	
R8	321213	1	RESISTOR 1K 1/4W	
R9	182514	1	RESISTOR 81 OHMS 1/2W	
R10-12	315958	3	RESISTOR 3.6K 1/4W	
C1	326580	1	CAPACITOR 10 MFD 50V	
C2	327031	1	CAPACITOR 0.01MFD, 6VDC	
CR1	321948	1	DIODE 1N4002	
Q1	324858	1	TRANSISTOR 2N3569	
Q2	315931	1	TRANSISTOR 2N3638	
Q3	324858	1	TRANSISTOR 2N3569	
Q4	315931	1	TRANSISTOR 2N3638	
	39603RM	2	STRAP .700 24 GA	
	326515	1	CIRCUIT BOARD	

322050

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-28-68	10001 R
2	6-7-68	88788
3	8-4-68	98308
3A	3-28-69	98818
4	11-15-69	96464

WDP

SHEET 1 OF 2

ALARMS AND CONTROL

APPROVALS

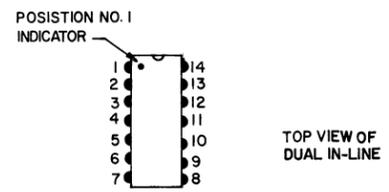
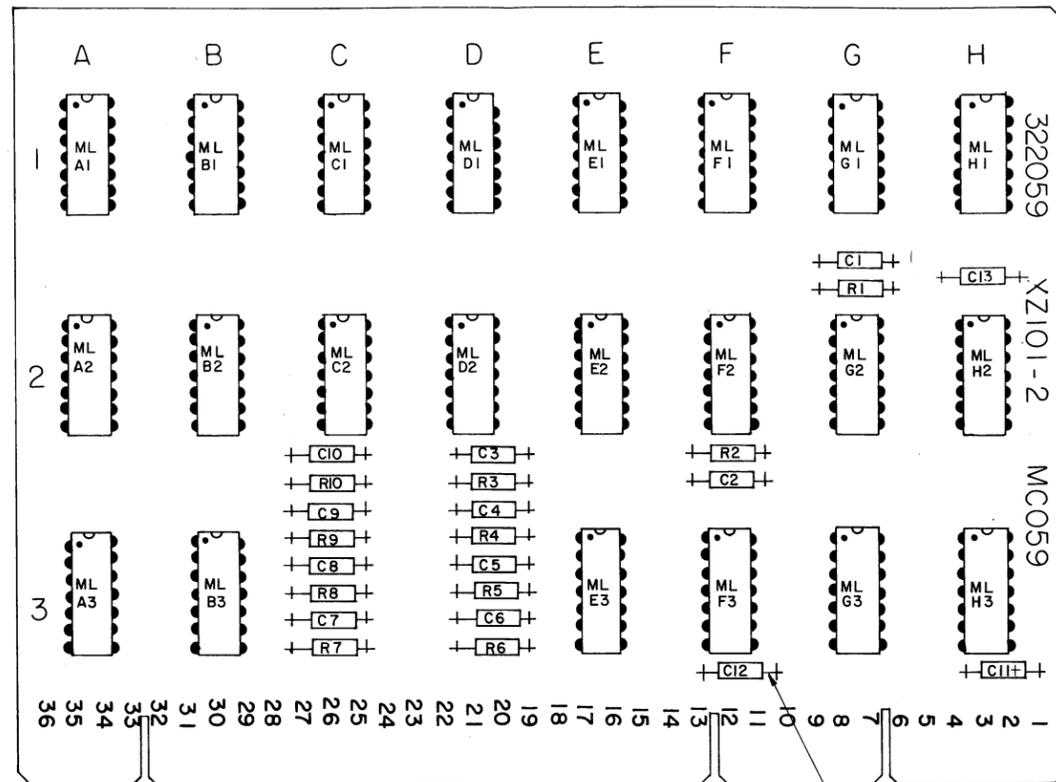
R AND D: *[Signature]* E OF M: *[Signature]*

E-NUMBER
 PROD NO. 322050
 DATE 12-1-67
 R&D FILE 8-A384AA
 DRAWN WPS CMK
 ENGD REL APPD *[Signature]*

TELETYPE CORPORATION

322050

NO.	NOTES
1.	INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD 
2.	SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
3.	REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY:
4.	ASSOCIATED SCHEMATICS ARE 8371WD.
5.	CIRCUIT DESCRIPTION 8371WD-CD.
6.	ALL CHARACTERS ARE TO BE SILK SCREENED IN WHITE, RED, OR BLACK ENAMEL.
7.	CHARACTER HEIGHT .120-12 POINTS NEWS GOTHIC.



326537
60340RM SLEEVING, (2 PLS.)

CIRCUIT CARD MC 059

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326853	3	INTEGRATED CIRCUIT 853	
MLA2			SAME AS MLA1	
MLA3	326852	5	INTEGRATED CIRCUIT 852	
MLB1	326833	1	INTEGRATED CIRCUIT 833	
MLB2			SAME AS MLA3	
MLB3	326846	8	INTEGRATED CIRCUIT 846	
MLC1	326830	2	INTEGRATED CIRCUIT 830	
MLC2			SAME AS MLA3	
MLD1			SAME AS MLC1	
MLD2			SAME AS MLA3	
MLE1			SAME AS ML A1	
MLE2			SAME AS MLA3	
MLE3			SAME AS ML B3	
MLF1	326862	2	INTEGRATED CIRCUIT 862	
MLF2			SAME AS ML B3	
MLF3			SAME AS ML B3	
MLG1	326832	1	INTEGRATED CIRCUIT 832	
MLG2			SAME AS ML B3	
MLG3			SAME AS ML F1	
MLH1			SAME AS ML B3	
MLH2			SAME AS ML B3	
MLH3			SAME AS ML B3	
RI-10	315948	10	RESISTOR, FIXED 100 OHM, 1/4W.	
C1,2,12,13	171583	4	CAPACITOR, .003MFD.	
C3-10	312385	8	CAPACITOR, 0.1MFD.	
C11	327831	1	CAPACITOR, 6.8MFD.	
	326537	1	CIRCUIT BOARD, ETCHED.	
	60340RM	2	SLEEVING.	

322059

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-10-69	19888 R

SHEET 1 OF 2

DISTRIBUTOR

APPROVALS

R AND D: *[Signature]* E OF M: *[Signature]*

E-NUMBER

PROD NO. 322059

DATE 6-18-68

R&D FILE G-A354AA

DRAWN W.P.B. CHKD. *[Signature]*

ENGD. A.B. APPD. *[Signature]*

TELETYPE CORPORATION

322059

NO. NOTES

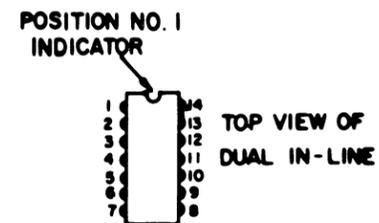
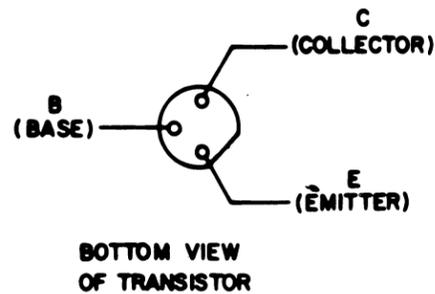
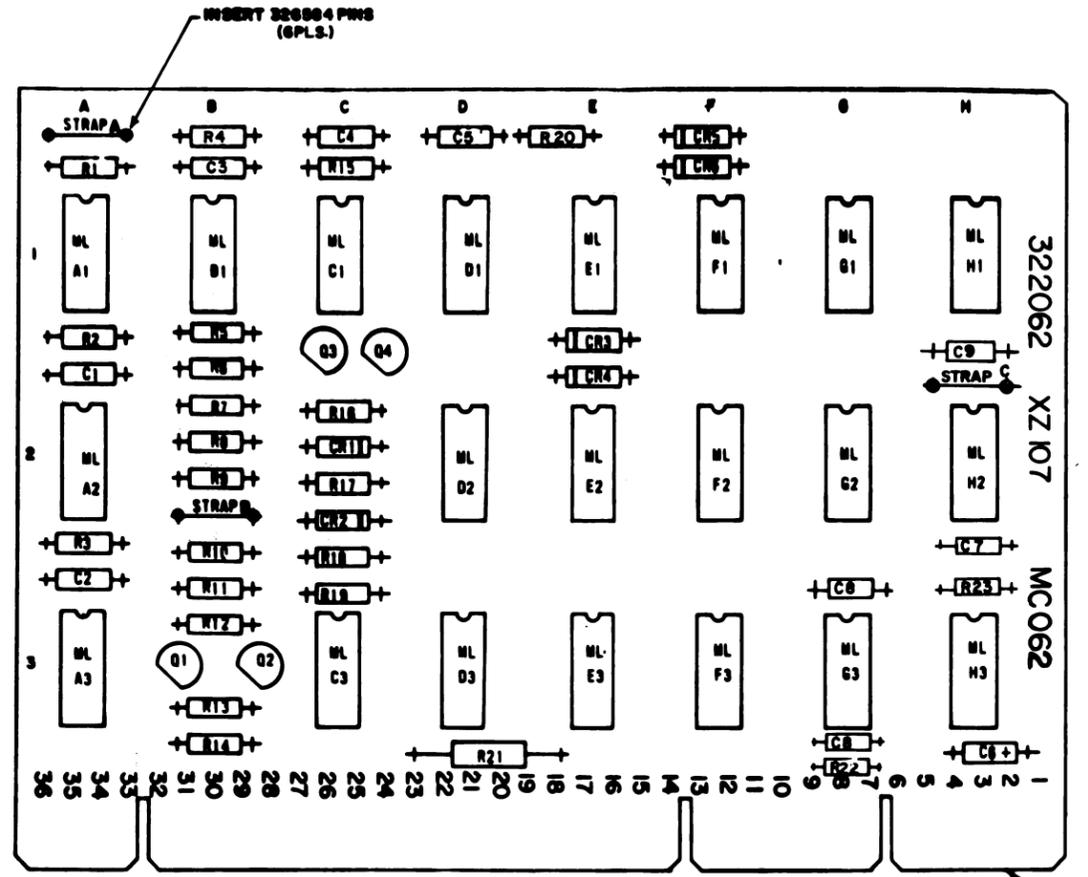
1 INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD
ML D 2
ROW
COLUMN
INTEGRATED CIRCUIT

2 SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS.

3 REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY: 61,434S

4 ASSOCIATED SCHEMATIC: 8383WD

5 STRAPS A, B, AND C ARE TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.



CIRCUIT CARD EC

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326862	1	INTEGR. CIRC. 862	
MLB1	326846	1	" " 846	
MLC1	326846	1	" " 846	
MLD1	326845	1	" " 846	
MLE1	396830	1	" " 830	
MLF1	326846	1	" " 846	
MLG1	326852	1	" " 852	
MLH1	326852	1	" " 852	
MLA2	326846	1	" " 846	
MLD2	326853	1	" " 853	
MLE2	326862	1	" " 862	
MLE2	326846	1	" " 846	
MLG2	326846	1	" " 846	
MLH2	326862	1	" " 862	
MLA3	326846	1	" " 846	
MLC3	326853	1	" " 853	
MLD3	326832	1	" " 832	
MLE3	326846	1	" " 846	
MLE3	326853	1	" " 853	
MLG3	326846	1	" " 846	
MLH3	326830	1	" " 830	
R1	315958	1	RES. FIXED. 3.6K	1/4W
R2	315986	1	" " 6.2K	1/4W
R3-R4	315971	2	" " 680	1/4W
R5-R6	315959	2	" " 4.7K	1/4W
R7-R10	315958	4	" " 3.6K	1/4W
R11	320275	1	" " 10 K	1/4W
R12	315958	1	" " 3.6K	1/4W
R13	315954	1	" " 1.5K	1/4W
R14	320275	1	" " 10 K	1/4W
R15.22.23	315948	3	" " 100	1/4W
R16-R17	320275	2	" " 10 K	1/4W
R18-R19	315959	2	" " 4.7K	1/4W
R20	315971	1	" " 680	1/4W
R21	182514	1	" " 91	1/2W
C1.3.7.8	312385	5	CAPACITOR .1 MFD	12V DC
C4.8.9	171583	3	" .003	100V DC
C5	312385	1	" .1 MFD	12V DC
C6	327831	1	" 6.8 MFD	6V DC
Q1	324858	1	TRANSISTOR 2N3569	
Q2	315931	1	" 2N3638	
Q3-4	324658	2	" 2N3569	
CR1-6	197464	6	DIODE 1N914	
	39803RM	3	STRAP - NOTE 5	
	326584	6	FORMED PIN	
	326526	1	CIRCUIT BOARD	

322062

REVISIONS

ISSUE	DATE	AUTH. NO.
4	11-15-68	96464

WDP

SHEET 1

RECEIVE CONTROL

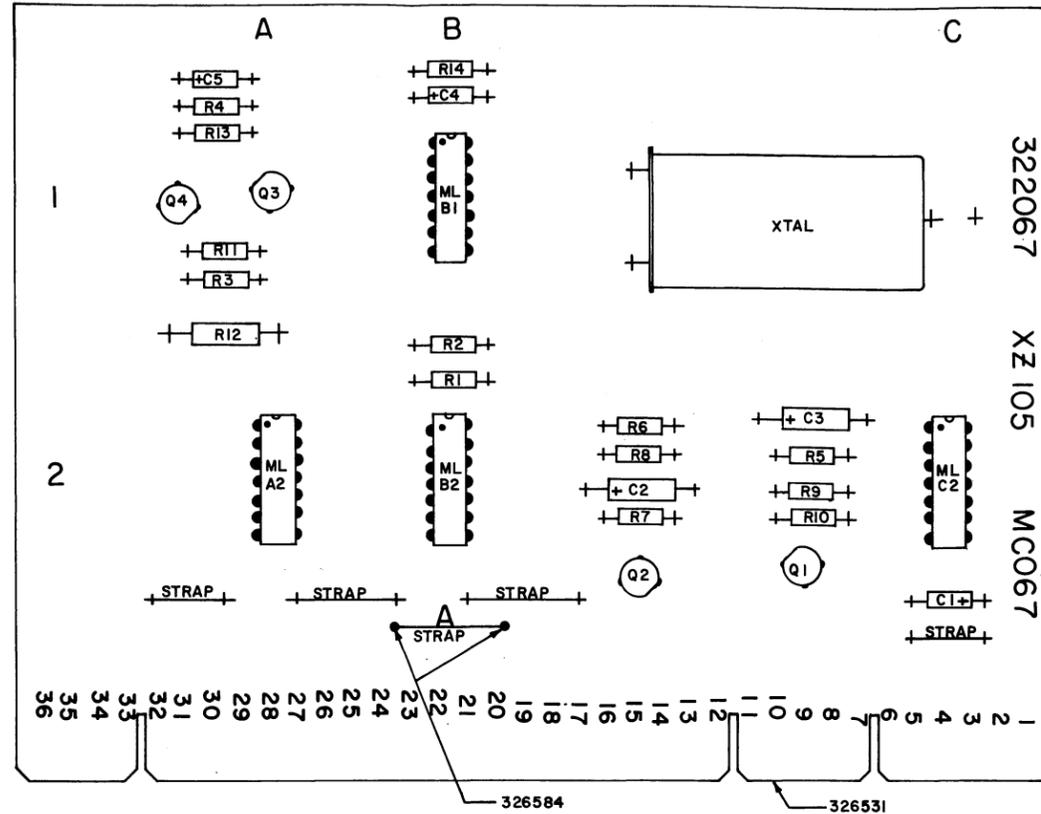
APPROVALS

R AND D	E OF M
E-NUMBER	
PROD NO 322062	
DATE 12-12-67	
R&D FILE G-A354AA	
DRAWN R. J. P.	CHKD
ENGD. A. B.	APPD

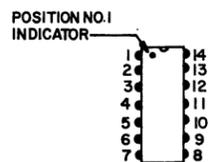
TELETYPE CORPORATION

322062

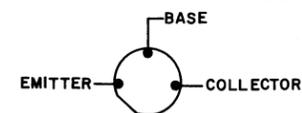
- NO. NOTES**
- INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD.
 - SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
 - S-NUMBER 61,516S.
 - ASSOCIATED SCHEMATIC: 8387 WD.
 - STRAP "A" TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.
 - ALL CHARACTERS TO BE SILK SCREENED IN WHITE, BLACK, OR RED ENAMEL.
 - CHARACTER HEIGHT .120-12 POINTS NEWS GOTHIC.



TOP VIEW OF INTEGRATED CIRCUIT PACKAGE.



BOTTOM VIEW OF TRANSISTOR



CIRCUIT CARD MC067

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA2	326862	1	INTEGRATED CIRCUIT 862	
MLB1	326845	1	INTEGRATED CIRCUIT 845	
MLB2	326846	1	INTEGRATED CIRCUIT 846	
MLC2	326853	1	INTEGRATED CIRCUIT 853	
R1,2	315958	3	RESISTOR, FIXED 3.6K, 1/4 W.	
R3,4,5	320275	3	RESISTOR, FIXED 10K, 1/4 W.	
R6	315974	1	RESISTOR, FIXED 300K, 1/4 W.	
R7	315947	2	RESISTOR, FIXED 510HM, 1/4 W.	
R8	315959	1	RESISTOR, FIXED 4.7K, 1/4 W.	
R9	315956	1	RESISTOR, FIXED 2.7K, 1/4 W.	
R10	321510	1	RESISTOR, FIXED 51K, 1/4 W.	
R11	315954	1	RESISTOR, FIXED 1.5K, 1/4 W.	
R12	182514	1	RESISTOR, FIXED 910HM, 1/2 W.	
R13			SAME AS R1.	
R14			SAME AS R7.	
C1	327831	1	CAPACITOR, 6.8 MFD.	
C2	310926	1	CAPACITOR, 0.15 MFD.	
C3	315976	1	CAPACITOR, 470 PFD.	
C4	312385	1	CAPACITOR, 0.1 MFD.	
C5	171583	1	CAPACITOR, 0.003 MFD.	
Q1,2	315930	2	TRANSISTOR, 2N3568	
Q3	324656	1	TRANSISTOR, 2N3569	
Q4	315931	1	TRANSISTOR, 2N3638	
	39603RM	2	STRAP, 0.7 INCHES	
	39603RM	3	STRAP, 0.9 INCHES	
	326584	2	PINS, FORMED.	
	326531	1	CIRCUIT BOARD.	
XTAL	327276	1	CRYSTAL 19.2 KHZ.	

322067

REVISIONS

ISSUE	DATE	AUTH. NO.
1	3-25-68	19091-R
2	6-7-68	95788
3	8-14-68	96060
4	10-22-68	96395

SHEET 1 OF 2

KSR
MODE
CONTROL

APPROVALS

R AND D: *HJK* E OF M: *U*

E-NUMBER
PROD NO. 322067

DATE 9-12-68

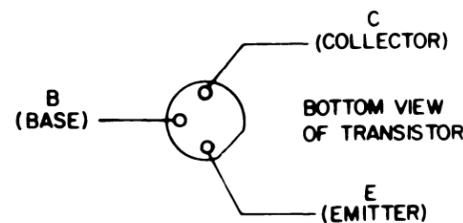
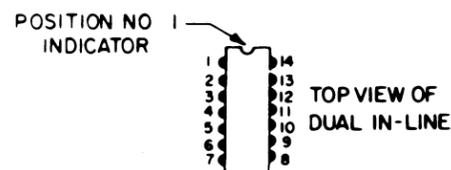
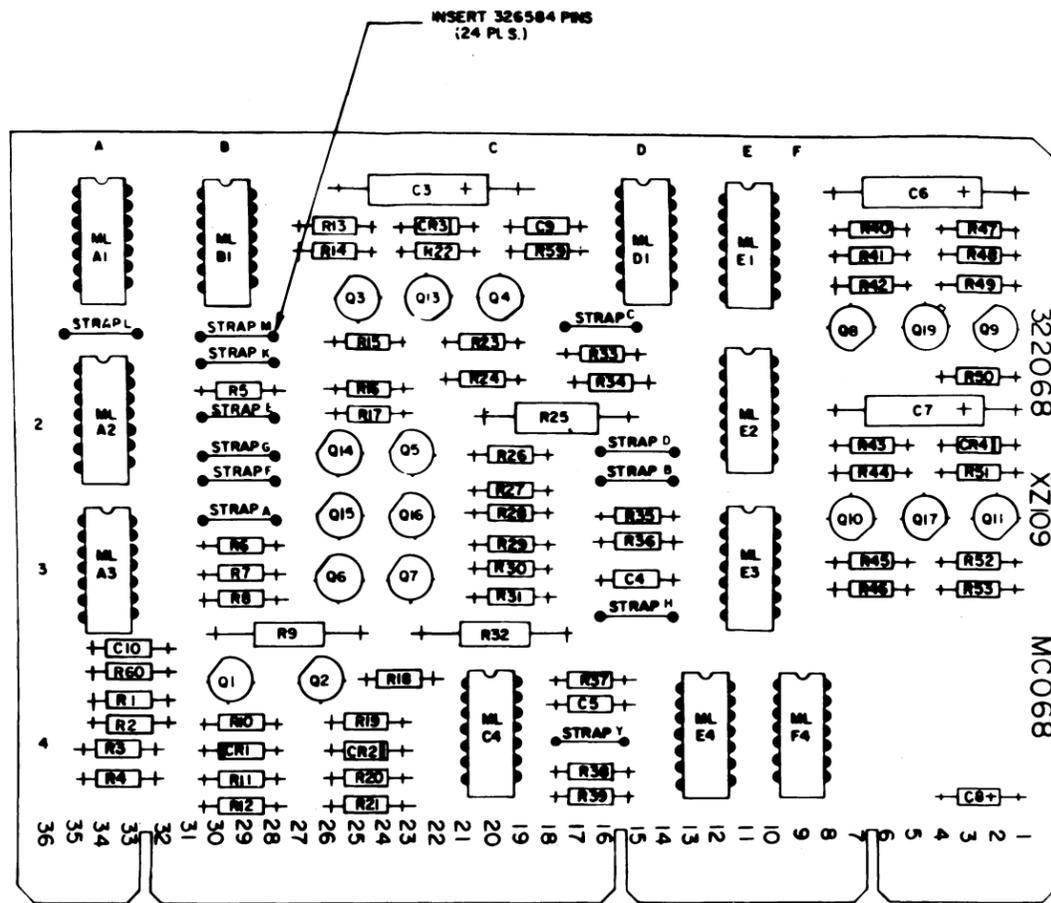
R&D FILE G-A354AA

DRAWN W.R.B. CHKD. *[Signature]*
ENG. C.A.Y. APPD. *[Signature]*

TELETYPE CORPORATION

322067

- NO. NOTES
- INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD
ML D 2
ROW
COLUMN
INTEGRATED CIRCUIT
 - SEE SPECIFICATION MR2.001 FOR CIRCUIT BOARD REQUIREMENTS
 - REFERENCE SPECIFICATION FOR TELETYPE CORPORATION EMPLOYEES ONLY 615215
 - ASSOCIATED SCHEMATICS ARE: 8388 WD.
 - STRAPS ARE TO BE ADDED AFTER TESTING HAS BEEN COMPLETED.



CIRCUIT CARD MC 068

REF DESIG.	TELETYPE PART NO	TOTAL QTY	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326845	1	INTEGRATED CIRCUIT 845	
MLB1	326845	1	INTEGRATED CIRCUIT 845	
MLD1	326830	1	INTEGRATED CIRCUIT 830	
MLE1	326846	1	INTEGRATED CIRCUIT 846	
MLA2	326846	1	INTEGRATED CIRCUIT 846	
MLE2	326862	1	INTEGRATED CIRCUIT 862	
MLA3	326846	1	INTEGRATED CIRCUIT 846	
MLE3	326836	1	INTEGRATED CIRCUIT 836	
MLC4	326862	1	INTEGRATED CIRCUIT 862	
MLE4	326846	1	INTEGRATED CIRCUIT 846	
MLF4	326846	1	INTEGRATED CIRCUIT 846	
R1-4	315958	4	RESISTOR, FIXED 3.6K 1/4W	
R59	315947	1	RESISTOR, FIXED 51 Ω 1/4W	
R5	315958	1	RESISTOR, FIXED 3.6K 1/4W	
R6	320275	1	RESISTOR, FIXED 10K 1/4W	
R7	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R8	320275	1	RESISTOR, FIXED 10K 1/4W	
R9	182514	1	RESISTOR, FIXED 91 Ω 1/2W	
R10	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R11	320275	1	RESISTOR, FIXED 10K 1/4W	
R12	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R13	320275	1	RESISTOR, FIXED 10K 1/4W	
R14	315948	1	RESISTOR, FIXED 100 Ω 1/4W	
R15	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R16	320275	1	RESISTOR, FIXED 10K 1/4W	
R17	315955	1	RESISTOR, FIXED 2.2K 1/4W	
R18	315958	1	RESISTOR, FIXED 3.6K 1/4W	
R19	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R20	320275	1	RESISTOR, FIXED 10K 1/4W	
R21-3	315959	3	RESISTOR, FIXED 4.7K 1/4W	
R24	320275	1	RESISTOR, FIXED 10K 1/4W	
R25	171441	1	RESISTOR, FIXED 560 Ω 1W	
R26	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R27	320275	1	RESISTOR, FIXED 10K 1/4W	
R28	315958	1	RESISTOR, FIXED 3.6K 1/4W	
R29	320275	1	RESISTOR, FIXED 10K 1/4W	
R30	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R31	320275	1	RESISTOR, FIXED 10K 1/4W	
R32	182514	1	RESISTOR, FIXED 91 Ω 1/2W	
R33	320275	1	RESISTOR, FIXED 10K 1/4W	
R34-5	315958	2	RESISTOR, FIXED 3.6K 1/4W	
R36-7	315971	2	RESISTOR, FIXED 680 Ω 1/4W	
R38-9	315958	2	RESISTOR, FIXED 3.6K 1/4W	
R40-1	315948	2	RESISTOR, FIXED 100 Ω 1/4W	
R42	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R43	321545	1	RESISTOR, FIXED 12K 1/4W	
R44	315948	1	RESISTOR, FIXED 100 Ω 1/4W	
R45	315954	1	RESISTOR, FIXED 1.5K 1/4W	
R46	320275	1	RESISTOR, FIXED 10K 1/4W	
R47	315952	1	RESISTOR, FIXED 820 Ω 1/4W	
R48	326601	1	RESISTOR, FIXED 150K 1/4W	
R49	326598	1	RESISTOR, FIXED 56 Ω 1/4W	
R50	315959	1	RESISTOR, FIXED 4.7K 1/4W	
R51	320275	1	RESISTOR, FIXED 10K 1/4W	
R52-3	315959	2	RESISTOR, FIXED 4.7K 1/4W	
R60	315947	1	RESISTOR, FIXED 51 Ω 1/4W	
Q1-11	324656	11	TRANSISTOR 2N3569	
Q13-17	315931	5	TRANSISTOR 2N3638	
Q19	321512	1	TRANSISTOR 2N2646	
CR1-4	197464	4	DIODE 1N914	
C9	312385	1	CAPACITOR 1 MFD 10V DC	
C3	326592	1	CAPACITOR 33 MFD	
C4-5	312385	2	CAPACITOR 1 MFD 10V DC	
C6	326592	1	CAPACITOR 33 MFD 35V DC	
C7	300027	1	CAPACITOR 15 MFD 35V DC	
C10	312385	1	CAPACITOR 1 MFD 10V DC	
	39603RM	12	STRAP .700 24 AWG NG1E 5	
	326584	24	FORMED PIN	
	326532	1	CIRCUIT BOARD	
C8	327831	1	CAPACITOR 6.8 MFD 6V DC	

322068

REVISIONS

ISSUE	DATE	AUTH. NO.
5	8-2-68	95997
5A	1-22-69	96747
5B	1-23-69	96771
6	11-15-68	96464
7	2-19-69	96464-1

SHEET 1 OF 2

CHANNEL CONTROL

APPROVALS

R AND D: *L & M* E O M: *✓*

PROD NO 322068

DATE 12 68

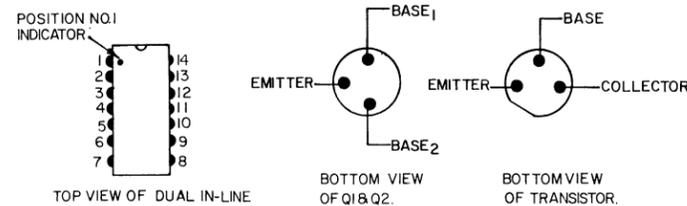
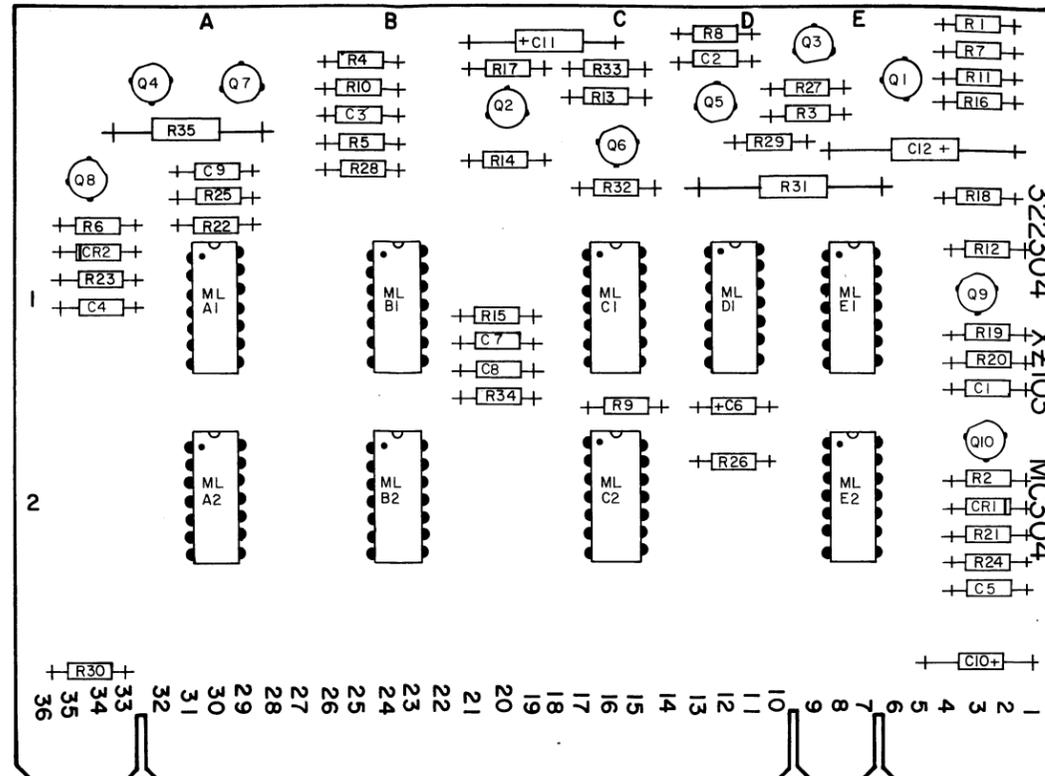
PROB FILE G A354AA

DRAWN W P B CHKD
ENGR C A Y APPD D E H

TELETYPE CORPORATION

322068

- NO. NOTES.
- INTEGRATED CIRCUIT ELEMENT LOCATION ON CIRCUIT BOARD.
 - SEE SPECIFICATION MR 2.001 FOR CIRCUIT BOARD REQUIREMENTS.
 - S-NUMBER: 61,618 S
 - ASSOCIATED SCHEMATIC: 8773 WD.
 - ALL CHARACTERS TO BE SILK SCREENED IN WHITE, RED, OR BLACK ENAMEL.
 - CHARACTER HEIGHT .120-12 POINTS NEWS GOTHIC.



CIRCUIT CARD MC304

REF. DESIG.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
MLA1	326846	6	INTEGRATED CIRCUIT 846	
MLA2	326836	1	INTEGRATED CIRCUIT 836	
MLB1			SAME AS MLA1	
MLB2	326862	2	INTEGRATED CIRCUIT 862	
MLC1			SAME AS MLA1	
MLC2			SAME AS MLA1	
MLD1			SAME AS MLA1	
MLE1			SAME AS MLA1	
MLE2			SAME AS MLB2	
R1-6	320275	6	RESISTOR, FIXED 10K, 1/4W.	
R7-10	315958	4	RESISTOR, FIXED 3.6K, 1/4W.	
R11-15	315947	5	RESISTOR, FIXED 51 OHM, 1/4W.	
R16-17	315953	2	RESISTOR, FIXED 1.2K, 1/4W.	
R18	315974	1	RESISTOR, FIXED 300K, 1/4W.	
R19	326602	1	RESISTOR, FIXED 360 OHM, 1/4W.	
R20-23	315959	4	RESISTOR, FIXED 4.7K 1/4W.	
R24-26	315948	3	RESISTOR, FIXED 100 OHM, 1/4W.	
R27-28	315954	2	RESISTOR, FIXED 1.5K, 1/4W.	
R29-30	315955	2	RESISTOR, FIXED 2.2K, 1/4W.	
R31	171441	1	RESISTOR, FIXED 560 OHM, 1W.	
R32	326602	1	RESISTOR, FIXED 360 OHM, 1/4W.	
R33	321510	1	RESISTOR, FIXED 51K, 1/4W.	
R34	326598	1	RESISTOR, FIXED 56 OHM, 1/4W.	
R35	182514	1	RESISTOR, FIXED 91 OHM, 1/2W.	
C1-4	171583	4	CAPACITOR, 0.003 MFD. 75V.	
C5,7,8,9	312385	4	CAPACITOR, 0.1 MFD. 10V.	
C6,10	327831	2	CAPACITOR, 6.8 MFD. 6V.	
C11-12	326591	2	CAPACITOR, 3.9 MFD. 35V.	
CRI-2	197464	2	DIODE, 1N914.	
Q1-2	327812	2	TRANSISTOR, MU4894	
Q3-4	315931	2	TRANSISTOR, 2N3638	
Q5-10	324656	6	TRANSISTOR, 2N3569	
	326543	1	CIRCUIT BOARD	

322304

REVISIONS

ISSUE	DATE	AUTH. NO.
1	12-20-68	19777 R

SHEET 1 OF 2

KSR SEND CONTROL

APPROVALS

R AND D	E OF M
E-NUMBER	
PROD NO. 322304	
DATE 9-26-68	
R&D FILE G-A354AA	
DRAWN W/PB	CHKD
ENGD. CAY	APPD

TELETYPE CORPORATION

322304

REVISIONS

ISSUE	DATE	AUTH. NO.
1	10-7-65	17311-R
2	8-26-66	91768
3	4-14-67	92496
4	7-14-67	94250
5	4-9-68	95429
6	8-23-68	95969

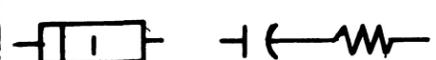
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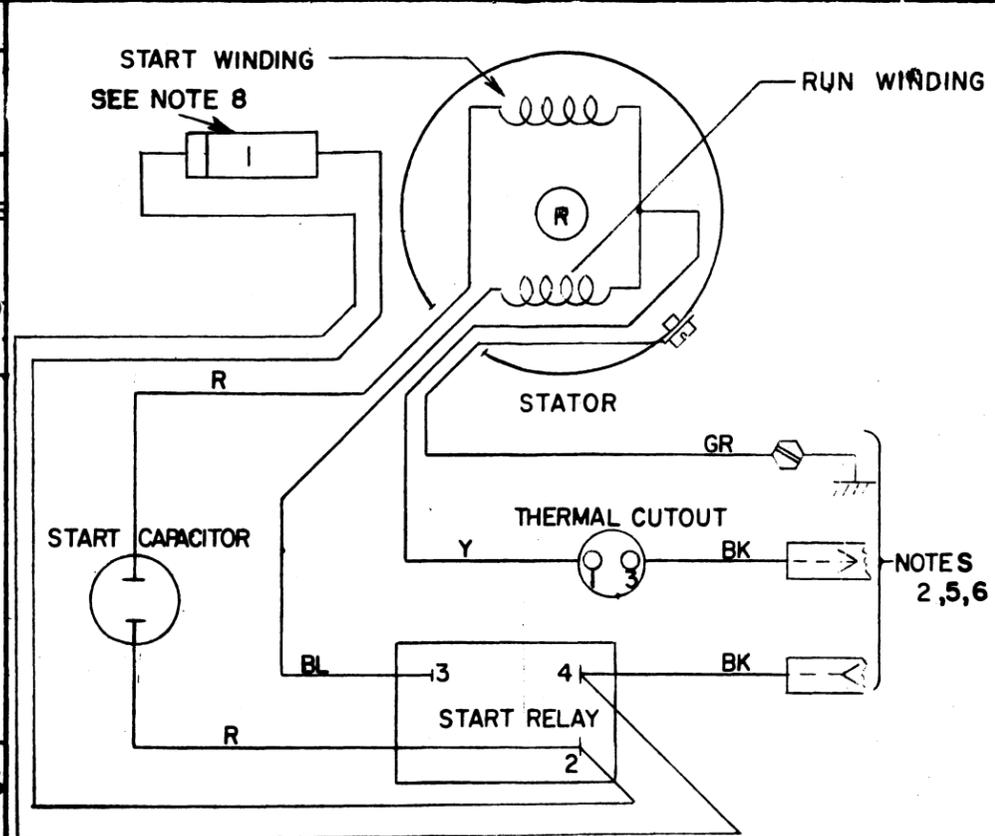
D

C

B

A

NO.	NOTES
1	SYNCHRONOUS MOTOR OPERATES ON REGULATED 60~±1% AC ONLY
2	BLACK LEADS ARE KEYED TO POLARITY BY MEANS OF OPPOSITE CONNECTORS. ALL UNITS MUST CONFORM—ATTACH GREEN LEAD TO CRADLE WHICH IS GROUNDED THRU THE BASE.
3	<p>WIRE COLOR CODE</p> <p>BK — BLACK</p> <p>W — WHITE</p> <p>R — RED</p> <p>GR — GREEN</p> <p>BL — BLUE</p> <p>Y — YELLOW</p>
4	TO BE USED WITH 115 V.A.C.±10% SOURCE ONLY
5	<p>—>> INDICATES MALE CONNR.</p> <p>—<< INDICATES FEMALE CONNR.</p>
6	LEAD FROM THERMAL CUT OUT TO BE CONNECTED TO LIVE SIDE OF AC POWER LINE.
7	STARTING CAPACITOR VALUE 43-48 MFD
8	 <p>327828 0.3 120</p>



YMU 2 SYNCHRONOUS MOTOR UNIT

WDP

ACTUAL WIRING
DIAGRAM OF MODEL
37 MOTOR UNIT
YMU 2

APPROVALS

D AND R <i>HJR</i>	E OF M <i>W</i>
-----------------------	--------------------

E NUMBER

PROD NO.

DATE *8/13/65*

P.D. FILE NO. *3-7-65*

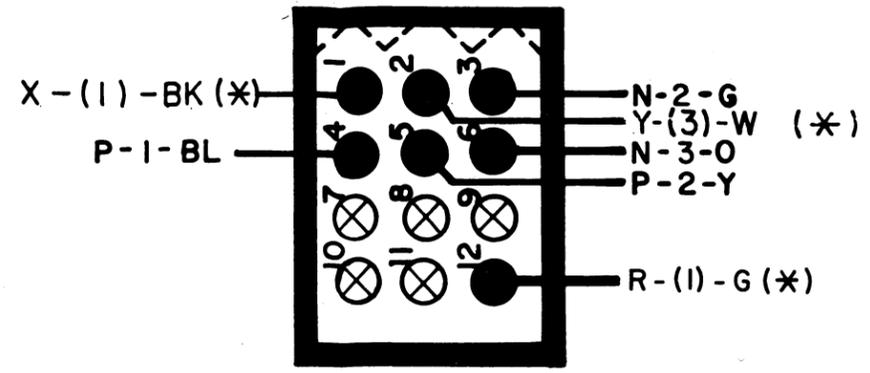
DRAWN *ED* CHKD *hde*

ENG. *File* APPD *...*

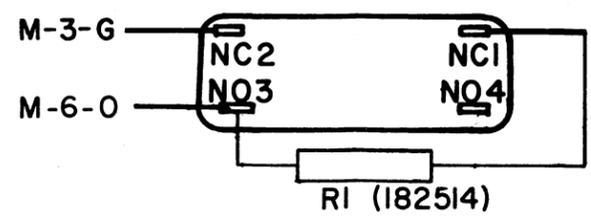
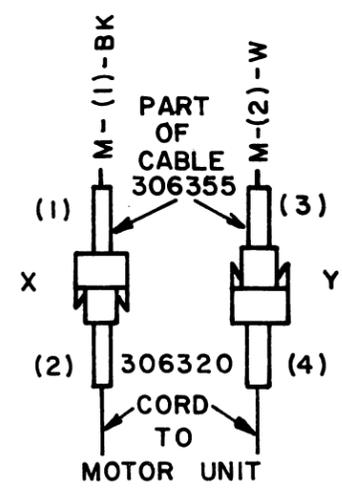
TELETYPE CORPORATION

6

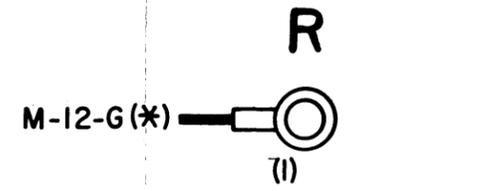
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1.	WIRING LEGEND:
2.	ALL WIRE 24 GA. UNLESS OTHERWISE SPECIFIED.
3.	*DENOTES 18 GA. WIRE
4.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
5.	CONNECTOR VIEWED FROM TERMINAL END.
6.	ASSOCIATED CABLE: 306355 CABLE ASSEMBLY
7.	ASSOCIATED SCHEMATICS: 7880WD (I/O), 8398WD (EIA)
8.	COLOR CODE BK - BLACK W - WHITE BL - BLUE O - ORANGE Y - YELLOW G - GREEN
9.	
10.	MOTOR CORD ASSEMBLY 306320



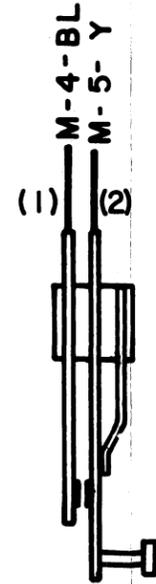
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M
181721
BASE CONNECTOR



N
E. O. L. SWITCH



R
BASE GROUND CONNECTION



P
KEYBOARD RESET CONTACT

7874 WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	10-7-65	17311-R
2	12-13-65	89508
3	1-18-66	89515
4	7-12-66	90675
5	10-24-66	92154
6	5-20-68	95656
7	11-14-68	96411

WDP

ACTUAL WIRING DIAGRAM FOR MODEL 37 BASE (YB 800)

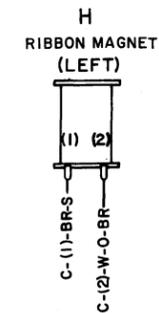
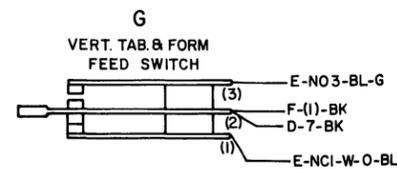
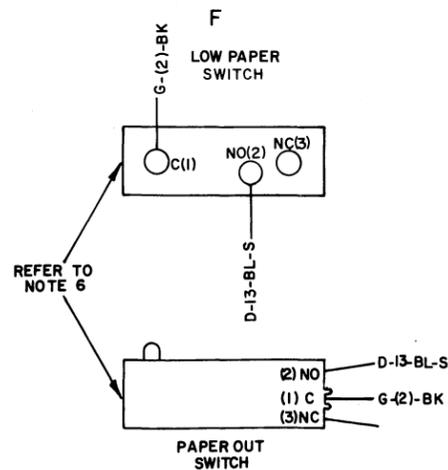
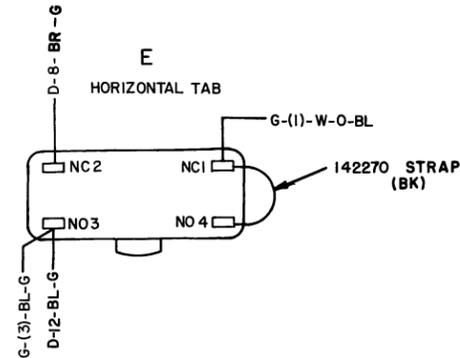
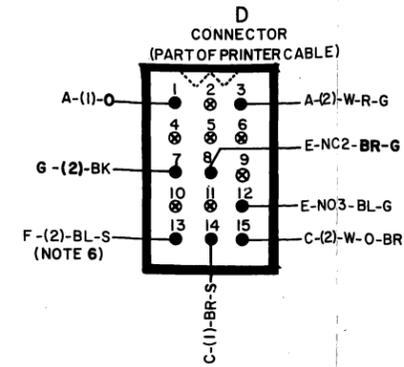
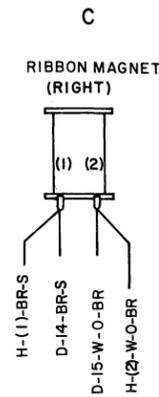
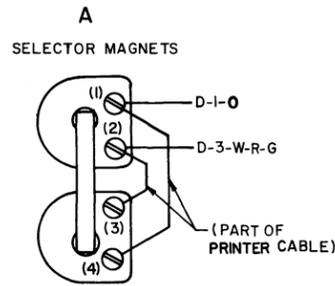
APPROVALS	
D AND R	E OF M
E-NUMBER	
PROD. NO. 7874 WD	
DATE: 9-22-65	
P.D. FILE NO. 1-30.354AA	
DRAWN JCH	CHKD.
ENGD. JCH	APPD.
TELETYPE CORPORATION	
7874 WD	

8362WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-27-68	19260-R
2	7-12-68	97839
3	1-8-69	96481

- NO. NOTES
1. WIRING LEGEND:
 K-B-W
 WIRE COLOR CODE.
 DISTANT TERMINATING DESIGNATION.
 DISTANT TERMINATING AREA.
 2. TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY & NOT MARKED ON COMPONENT.
 3. CONNECTOR VIEWED FROM TERMINAL END.
 4. ALL WIRE 24 AWG UNLESS OTHERWISE SPECIFIED.
 5. COLOR CODE LEGEND:
 BK - BLACK G - GREEN
 BR - BROWN BL - BLUE
 R - RED P - PURPLE
 O - ORANGE S - SLATE
 Y - YELLOW W - WHITE
 6. CONNECT WIRES TO AREA F AS SHOWN PER PRINTER REQUIREMENTS



ACTUAL WIRING DIAGRAM FOR MODEL 37 TYPING UNITS YP806,808, YP811,814.

APPROVALS

D AND R <i>[Signature]</i>	E OF M <i>[Signature]</i>
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E-NUMBER
 PROD. NO. 8362WD
 DATE 10-24-67
 P.D. FILE NO. 43-A25AA
 DRAWN W.P.B. CHKD. *[Signature]*
 ENGD. M.J.R. APPD. *[Signature]*

TELETYPE CORPORATION
 8362WD

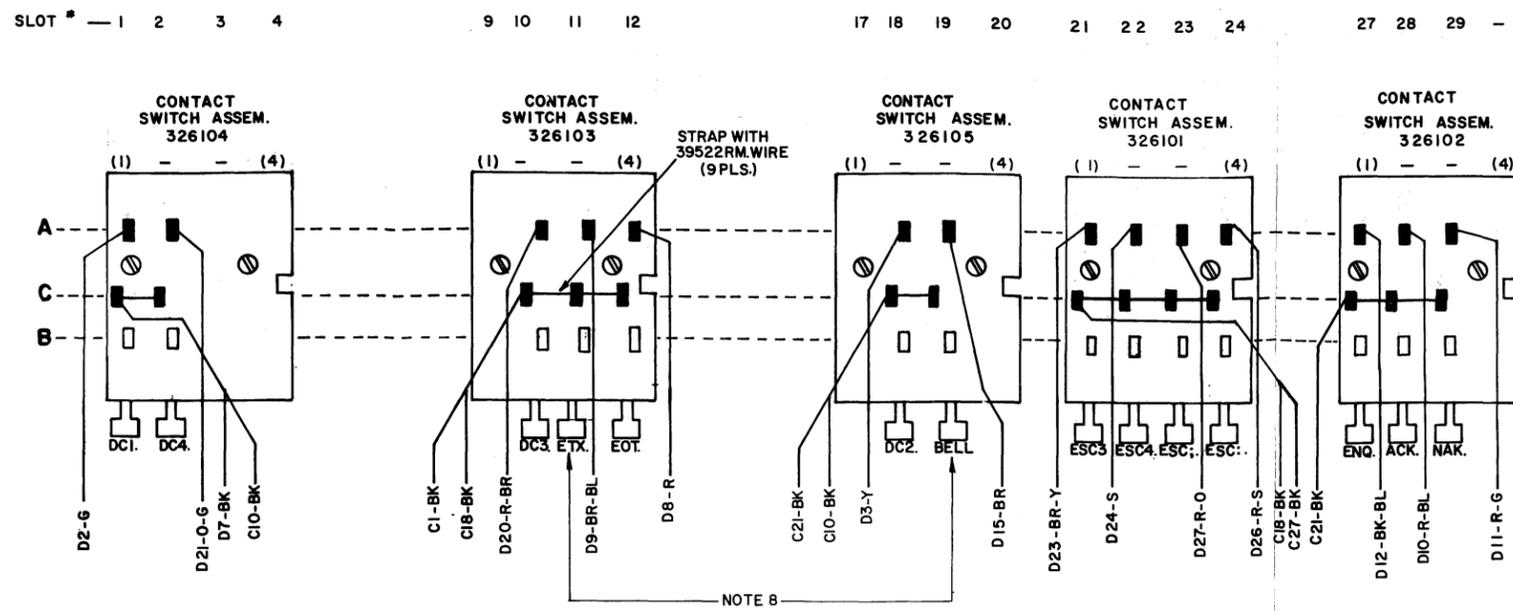
8363 WD

REVISIONS

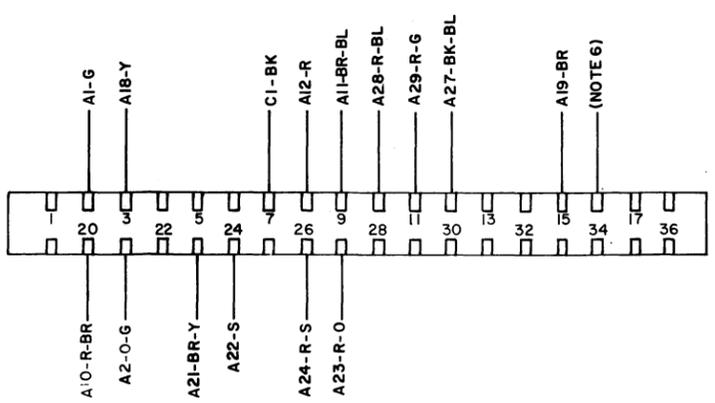
ISSUE	DATE	AUTH. NO.
1	10-24-68	19260 R
2	4-22-69	99032

- NO. NOTES**
- WIRING LEGEND:**
 - ASSOCIATED CABLE: 327817**
 - COLOR CODE:**

BK - BLACK	G - GREEN
BR - BROWN	BL - BLUE
R - RED	P - PURPLE
O - ORANGE	S - SLATE
Y - YELLOW	W - WHITE
 - TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE, AND ARE NOT MARK ON COMPONENT.**
 - ALL UNUSED WIRES SHOULD BE TIED BACK ON CABLE BODY, CARE SHOULD BE TAKEN TO AVOID SHORTING OF UNTERMINATED WIRES TO PRINTER FRAME.**
 - YAC STUNT BOX ARRANGMENT HAS BELL LOCATED IN SLOT NO.11 WITH ITS ASSOCIATED D15-BR WIRE.**



D
(J308)
CONNECTOR
161238



ACTUAL WIRING DIAGRAM FOR STUNT BOX ARRANGEMENT
 YAE - 319776
 YAC - 319875
 YAJ - 319655

APPROVALS

D. AND R <i>[Signature]</i>	E OF M <i>[Signature]</i>
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E-NUMBER
 PROD. NO. 8363 WD.
 DATE 2-27-68
 P.D. FILE NO. G-A354AA
 DRAWN W.P.B. CHKD. *[Signature]*
 ENGD. M.J.R. APPD. *[Signature]*

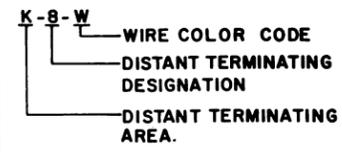
TELETYPE CORPORATION

8363 WD

8364WD

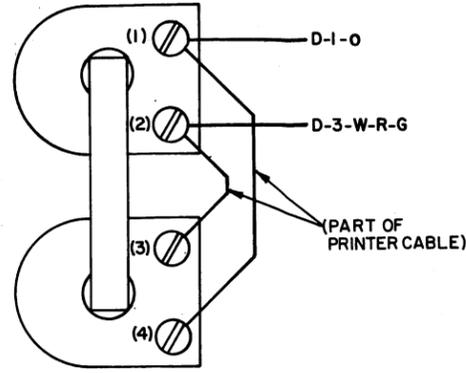
REVISIONS

ISSUE	DATE	AUTH. NO.
1	5-27-68	19260-R
2	9-17-68	97842
3	1-2-69	96573

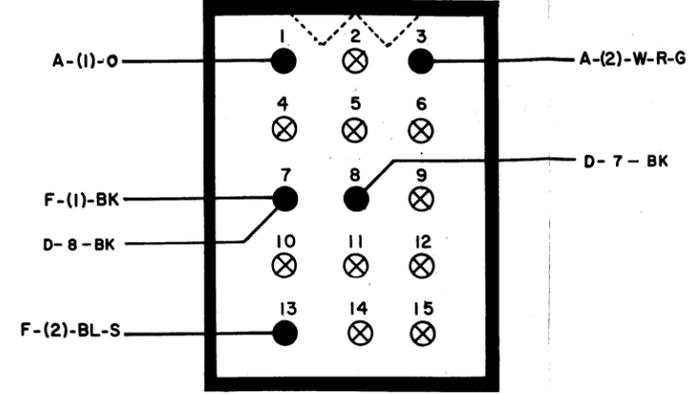
- NO. NOTES
1. WIRING LEGEND:

 2. TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY & NOT MARKED ON COMPONENT.
 3. CONNECTOR VIEWED FROM TERMINAL END.
 4. ALL WIRE 24 AWG. UNLESS OTHERWISE SPECIFIED.
 5. ASSOCIATED CABLE: 327B14.
 6. COLOR CODE LEGEND:

BK-BLACK	G-GREEN
BR-BROWN	BL-BLUE
R-RED	P-PURPLE
O-ORANGE	S-SLATE
Y-YELLOW	W-WHITE
 7. ALL UNUSED WIRES SHOULD BE TIED BACK ON CABLE BODY. CARE SHOULD BE TAKEN TO AVOID SHORTING OF UNTERMINATED WIRES TO THE PRINTER FRAME.
 8. THE LOW PAPER SWITCH IS NOT PART OF THE BASIC PRINTERS. IT BELONGS TO THE LOW PAPER MOD. KIT NO. 319650.

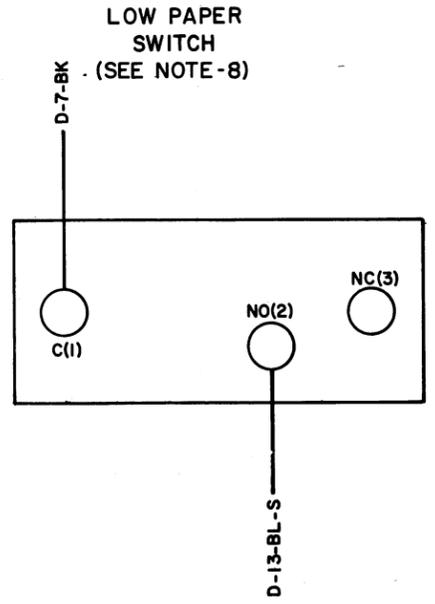
A
SELECTOR MAGNETS



D
CONNECTOR
(PART OF PRINTER CABLE)



F (OPTIONAL)



ACTUAL WIRING DIAGRAM FOR MODEL 37 TYPING UNIT YP810, 813

APPROVALS

D AND R <i>HR</i>	E OF M <i>[Signature]</i>
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E-NUMBER

PROD. NO. 8364 WD

DATE 3-5-68

P.D. FILE NO. G-A354 AA

DRAWN W.P.B. CHKD. *[Signature]*

ENGD. M.J.R. APPD. *[Signature]*

TELETYPE CORPORATION

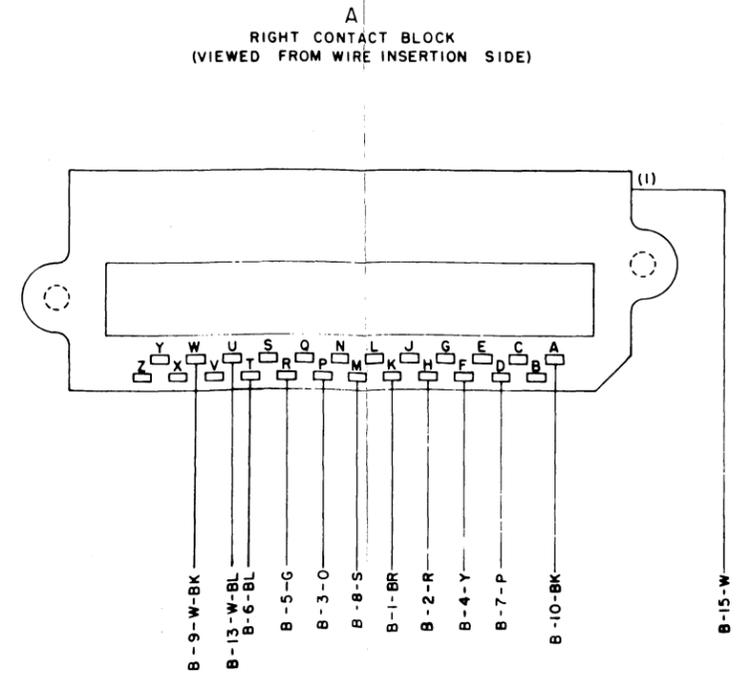
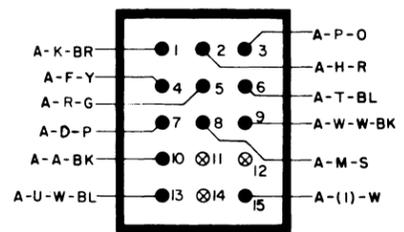
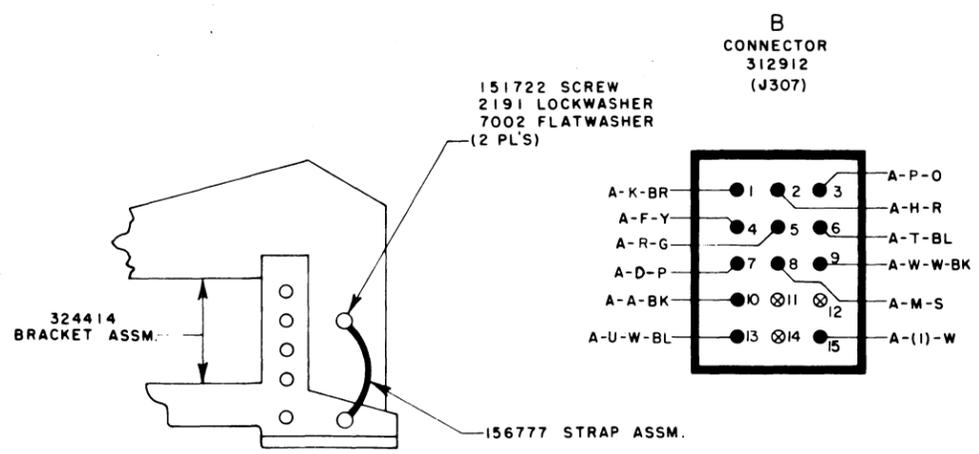
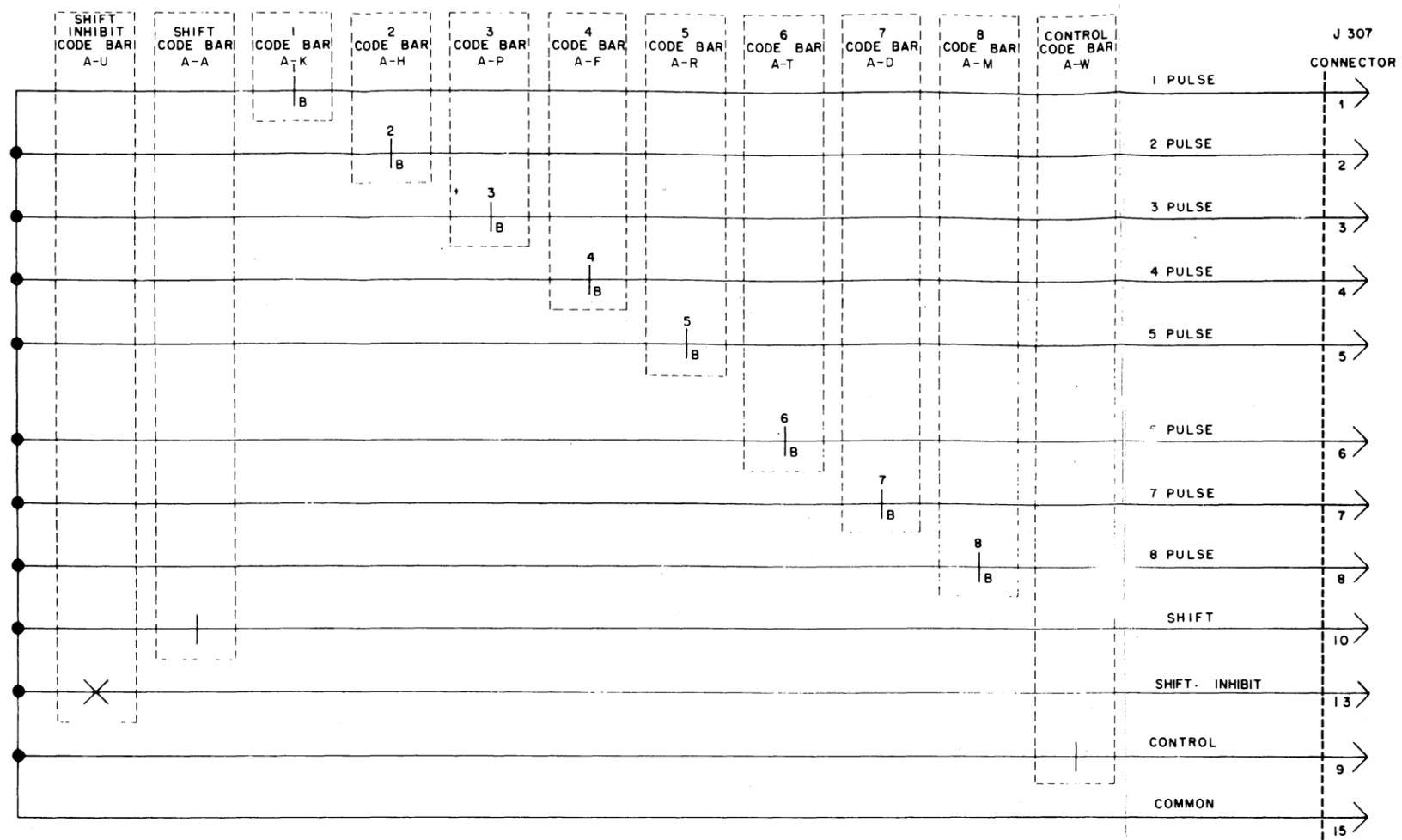
8364 WD

8500 WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	1-31-68	19025-R

- NOTES**
1. WIRING LEGEND
 2. ALL WIRE 24 AWG.
 3. TERMINALS DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
 4. 1 THROUGH 8 CODE BARS ARE SHOWN IN THE MARKING POSITION. SHIFT, CONTROL AND SHIFT INHIBIT CONTACTS ARE SHOWN IN THE UNOPERATED POSITION.
 5. ASSOCIATED CABLE :
324407
 6. → INDICATES MALE TERMINAL ON CONNECTOR.
 7. ALL COMPONENTS VIEWED FROM WIRE INSERTION SIDE.

SCHEMATIC



ACTUAL

ACTUAL AND SCHEMATIC WIRING DIAGRAMS FOR YK801 AAY THROUGH ZZY

APPROVALS	
D AND R	E OF M
E-NUMBER	
PROD. NO. 8500 WD	
DATE 10-6-67	
P.D. FILE NO. 1-18.354AA	
DRAWN <i>IMO</i>	CHKD. <i>JK</i>
ENG. S.M.G.	APPD. <i>JK</i>

TELETYPE CORPORATION

8500 WD