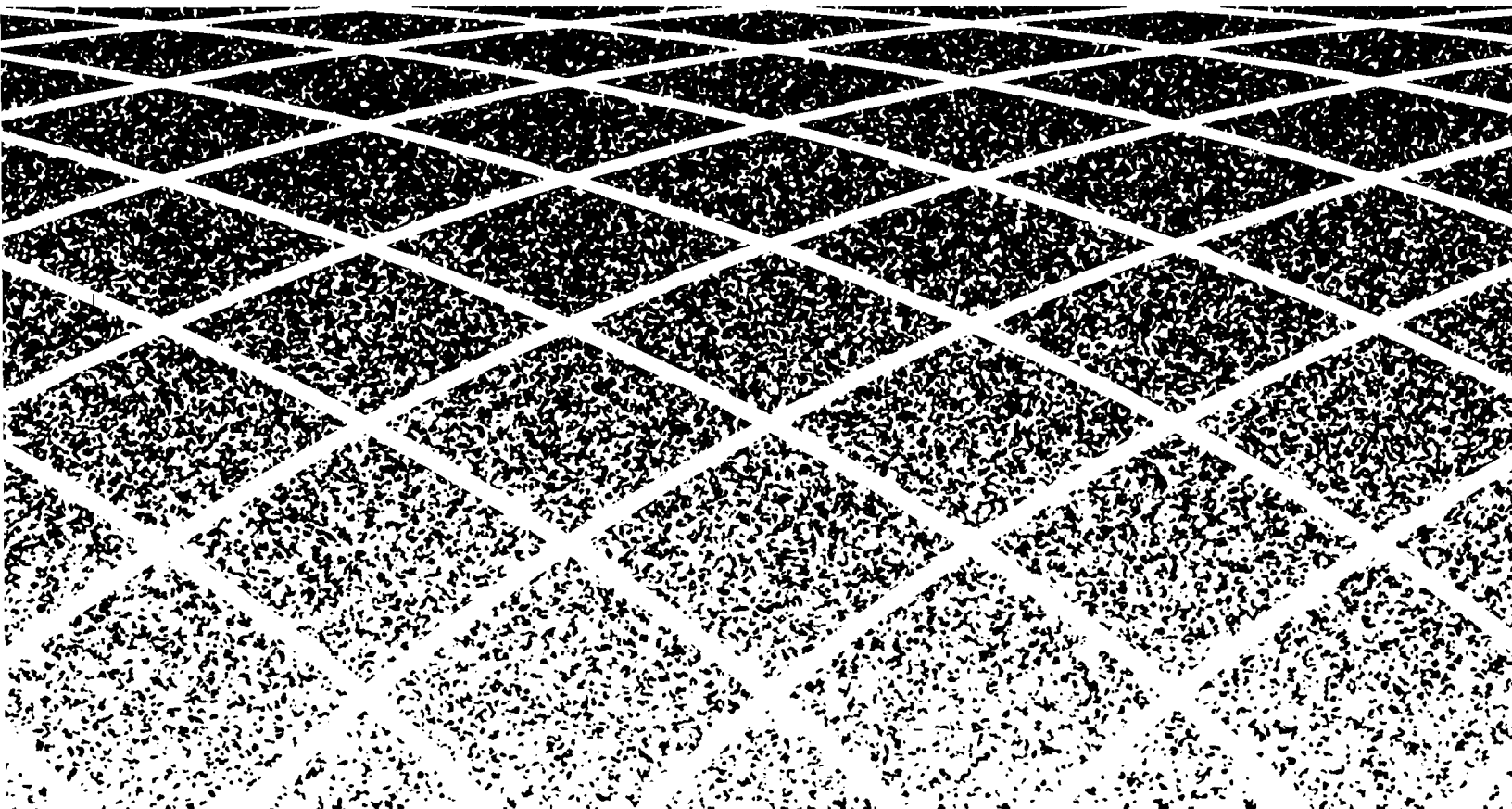
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March 1996

# DACS IV-2000 (512) Digital Access and Cross-Connect System IV-2000 Release 5.0

## Reference Manual



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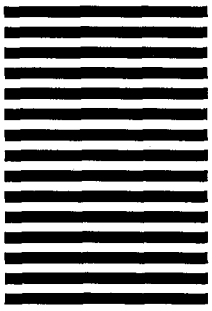
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# Preface

## Purpose

This manual provides detailed, functional descriptions of the system architecture, hardware, software, configurations, and features for the DACS IV-2000 (512) Release 5.0.

New features described in this guide include: capacity expansion (CE); optical remoting (OR); DS3 Clear-Channel cross-connection (DS3cc); DS3 to STS-1 gateway cross-connection; DS3 path identification for the AT&T transport self-identification plan (TRANSID); full-time DS1 performance monitoring of DS1 tributaries on DS3 facilities without loss of system capacity; unframed DS3; DS3 terminal loopbacks; DS3 test access; enhanced Synchronizer Module; and VT group numbering.

## Audience

The *DACS IV-2000 (512) Release 5.0 Reference Manual* is intended primarily for network planners, administrators, maintenance engineers, and technical personnel who require an in-depth knowledge of the DACS IV-2000.

## Document Summary

This document comprises the following chapters:

- **Preface** includes the purpose, the audience, and a summary of this document. It also lists referenced and related documents and ordering instructions.
- **Chapter 1 - Introduction** offers a brief overview of the AT&T 2000 family of transmission products and an overview of the DACS IV-2000 and its benefits.
- **Chapter 2 - System Features** details major features of the DACS IV-2000.
- **Chapter 3 - System Bays** describes the DACS IV-2000 equipment bays.
- **Chapter 4 - Collocated Configuration Control Architecture** describes the DACS IV-2000 (512) control architecture for collocated interface bay configurations.
- **Chapter 5 - Remote Complex Configuration Control Architecture** describes the DACS IV-2000 (512) control architecture for optically tied Remote Complex configurations.
- **Chapter 6 - Interface Bay Hardware** describes the components of the Interface Modules. Also included is information on DS1 Performance Monitoring Hardware considerations.
- **Chapter 7 - Power and Miscellaneous Hardware** describes fan assemblies, BNC Connectors, EMC Enclosures, power, and fuses.
- **Chapter 8 - User Interfaces** describes the format of commands and messages, system addressing, user passwords, user/superuser privileges, administrative links, and indicators and switches for the DACS IV-2000.
- **Appendix A - Technical Specifications** contains technical specifications of the DACS IV-2000.
- **Appendix B - Alarm, Scan, and Control Points** contains information describing the interface between the DACS IV-2000 and telemetry operating systems (OSs).
- **Glossary** defines terms used in the DACS IV-2000 documents.
- **Acronyms** provides full terms for the acronyms used in this document.
- **Index** provides page location information used in this document.

## Print Conventions

This manual uses the following print conventions:

- *Italic* type represents documentation titles, primarily AT&T customer documents and Bell Communications Research (Bellcore) technical references and technical advisories.
- **`Constant Width Bold`** type displays information you input, primarily commands.
- `Constant Width` displays information the system outputs, primarily messages.

## Referenced Documents

Table 1 lists Bellcore standards referenced in this document to provide additional technical information, specifications, or other supporting information.

Table 1. **Bellcore Reference Documents**

| Document Number | Document Title |
|---|---|
| TR-TSY-000009 | *Asynchronous Digital Multiplexer Requirements and Objectives* (Issue 1, May 1986) |
| TR-NWT-000063 | *Network Equipment-Building System (NEBS) Generic Equipment Requirements (A Module of LSSGR, FR-NWT-000064 and of TSGR, FR-NWT-000440)* (Issue 5, September 1993) |
| FR-NWT-000064 | *LATA Switching Systems Generic Requirements (LSSGR): 1993 Edition* (Issue 93, February 1993) |
| TR-TSY-000179 | *Software Quality Program Generic Requirements (SQPR) (A Module of ROGR, FR-NWT-000796)* (Issue 2, June 1993) |
| TR-TSY-000191 | *Alarm Indication Signal Requirements and Objectives (A Module of TSGR, FR-NWT-000440)* (Issue 1, May 1986) |
| TA-NWT-000199 | *Specification of Memory Administration Messages at the OS/NE Interface* (Issue 7, January 1993) |
| TA-NWT-000200 | *Specification of Maintenance Messages at the OS/NE Interface* (Issue 5, December 1990) |

Table continued on next page.

Table 1. **Bellcore Reference Documents (Continued)**

| Document Number | Document Title |
|---|---|
| TR-NWT-000233 | *Wideband and Broadband Digital Cross-Connect Systems Generic Criteria* (Issue 3, November 1993) |
| GR-253-CORE | *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria (A Module of TSGR, FR-NWT-000440)* (Issue 2, December 1995) |
| TR-TSY-000282 | *Software Reliability and Quality Acceptance Criteria (SRQAC) (A Module of ROGR, FR-NWT-000796)* (Issue 1, December 1986) |
| TR-NWT-000332 | *Reliability Prediction Procedure for Electronic Equipment (A Module of ROGR, FR-NWT-000796)* (Issue 5, September 1992) |
| TA-NWT-000474 | *Proposed Changes to TR-TSY-000474, Network Maintenance/Network Element Generic Requirements* (Issue 1, December 1991) |
| TR-NWT-000811 | *OTGR: Operations Application Messages - TL1 Message Index* (Issue 2, May 1992) |
| TR-NWT-000818 | *OTGR Section 6.1: Network Maintenance: Access and Testing - Generic Test Architecture* (Issue 1, November 1992) |
| TR-TSY-000499 | *Transport Systems Generic Requirements (TSGR): Common Requirements (A Module of TSGR, FR-NWT-000440)* (Issue 4, Revision 1, April 1992) |
| TR-TSY-000820 | *OTGR: Network Maintenance: Transport Surveillance - Generic Digital Transmission Surveillance, Section 10.1 (A Module of OTGR, FR-NWT-000439)* (Issue 2, February 1988) |
| TR-TSY-000824 | *OTGR: User System Interface User System Access, Section 10.1 (A Module of OTGR, FR-NWT-000439)* (Issue 2, February 1988) |
| TR-NWT-000833 | *OTGR: Operations Application Messages Network Maintenance: Generic Requirements for Network Element and Transport Surveillance Messages, Section 12.3 (A Module of OTGR, FR-NWT-000439)* (Issue 5, Revision 2, April 1993) |

Table continued on next page.

Table 1. **Bellcore Reference Documents (Continued)**

| Document Number | Document Title |
|---|---|
| TR-NWT-000835 | *OTGR: Operations Application Messages - Network Element (NE) Security Parameter Messages, Section 12.5 (A Module of OTGR, FR-NWT-000439)* (Issue 3, Revision 1, May 1991) |
| GR-1244-CORE | *General Reliability Requirements for Digital Cross-Connect Systems* (Issue 1, June 1995) |
| TR-NWT-001089 | *Electromagnetic Compatibility and Electrical Safety Generic Criteria for Network Telecommunications Equipment (A Module of LSSGR, FR-NWT-000064 and TSGR, FR-NWT-000440)* (Issue 2, June 1993) |
| SR-STS-001665 | *Network Monitoring and Analysis Generic Network Element Interface Support* (Issue 2, December 1992) |
| SR-STS-001578 | *OPS/INE Generic Interface Support* (Issue 2, December 1992) |

Table 2 lists ANSI standards referenced in this document to provide additional technical information, specifications, or other supporting data.

Table 2. **American National Standards Institute Documents**

| Document Number | Document Title |
|---|---|
| ANSI T1.105 | *Digital Hierarchy - Optical Interface Rates and Formats Specifications (SONET) - 1991* |
| ANSI T1.107 | *Telecommunications - Digital Hierarchy - Supplement to Formats Specifications (Synchronous Digital Data Format); Supplement T1.107A - 1990, Supplement T1.107B - 1991 (ESCA)* |
| ANSI T1.107a | *Telecommunications - Digital Hierarchy - Supplement to Formats Specifications (Synchronous Digital Data Format); Supplement T1.107A - 1990, Supplement T1.107B - 1991 (ESCA)* |
| ANSI T1.403 | *Carrier-to-Customer Installation - DS1 Metallic Interface* |
| ANSI T1M1.3 | These are standards in draft form, dealing with telecommunications maintenance/performance issues. |

## Related Documents

The following documents provide additional information about the DACS IV-2000 and can be ordered after the general availability date of this release:

- *DACS IV-2000 (512) Release 5.0 Operations and Maintenance*
  AT&T 365-340-901

  This manual provides detailed procedures for daily operations, trouble-clearing procedures, and routine maintenance of the DACS IV-2000 (512).

- *DACS IV-2000 (512) Release 5.0 Commands and Messages*
  AT&T 365-340-902

  This manual describes each command and its associated output response messages, including error codes. The appendices include command name, parameter, and state modifier acronym tables, activity menus, user privilege codes, state names, and state diagrams.

- *DACS IV-2000 (512) Release 5.0 Quick Reference Job Aids*
  AT&T 365-340-903

  These laminated aids contain command names, error codes, fuse locations, test access, port addressing, loopbacks, monitored parameter default and range values.

- *DACS IV-2000 (512) Release 5.0 Applications, Planning, and Ordering*
  AT&T 365-340-904

  This guide addresses network planners, account representatives, account executives, and engineers. It describes DACS IV-2000 features, applications, and ordering information.

- *DACS IV-2000 (512) Release 5.0 Software Release Description*
  AT&T 365-340-905

  This document contains upgrade procedures for the new software release. It relates status of problems fixed in previous releases, and operating issues for the current software release. (You cannot order this document as a stand-alone item; it only accompanies the software.)

## Electronic Documentation

AT&T DACS IV-2000 customer documentation is available on CD-ROM. Consult your AT&T account executive for details.

## Ordering Documents

To order copies of documents available for this release, send or call in an order using the title and its associated 9-digit document number as provided above:

- To order by mail:

  AT&T
  Customer Information Center
  Attention: Order Entry Section
  2855 N. Franklin Road
  P. O. Box 19901
  Indianapolis, IN 46219

- To order by telephone (Monday through Friday):

  United States: 1-800-432-6600 (7:30 a.m. to 6:30 p.m. EST)

  Canada: 1-800-255-1242

  Worldwide: Toll: 1-317-352-8557

- To order by FAX:

  1-317-352-8484

For RBOC/BOC customers, orders should be processed through the Company Documentation Coordinators.

For commercial customers, a check, money order, purchase order number, or charge card number is required with all orders. Make checks payable to AT&T. Consult your local AT&T account executive for pricing information.

AT&T entities should use Form IND 1-80.80 FA, available through the Customer Information Center.

# Introduction

# 1

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# Contents

# Introduction

# 1

The DACS IV-2000 (512) Release 5.0 is a software-based, high-capacity, digital cross-connect system that merges cross-connect and multiplexer functions. It helps manage DS1, DS3, and EC-1[1] facilities more efficiently by automating network route restoration, remote service and facility provisioning, and remote surveillance and test access. Its software-controlled cross-connect facility allows centralization and automation of operation, administration, maintenance, and provisioning functions.

The DACS IV-2000 terminates DS1, DS3, and STS-1 signals and cross-connects DS1, DS3, STS-1, and VT1.5 signals from transmission facilities or from DS1, DS3, and/or STS-1 based network elements. All cross-connections occur at the 1.728-Mb/s signal level. In the case of an STS-1 clear-channel Synchronous Payload Envelope (cc-SPE) signal or DS3cc signal, a group of 30 1.728-Mb/s signals is used. The DACS IV-2000 cross-connects:

- each DS3 signal as a clear-channel DS3 signal, or demultiplexes the DS3 signal into 28 DS1 signals to access the switch network.
- each STS-1 signal as a clear-channel STS-1 signal, to a DS3 as a gateway, or demultiplexes the STS-1 signal into 28 VT1.5 tributaries, which can be cross-connected as VT1.5 or DS1 signals.

1. Electrical Carrier-1 (EC-1) is the industry standard nomenclature for an electrical STS-1 signal.

The system architecture supports a wide range of termination mixes. The number of ports allocated to DS1, DS3, or EC-1 terminations depends on the particular application. The extreme cases are when all of the ports are allocated for STS-1 signals (480 STS-1s), DS3 signals (496 DS3s)[1], or for DS1 signals (13,888 DS1s).

The DACS IV-2000 accommodates synchronous optical network (SONET) STS-1 interface signals to support SONET-to-SONET cross-connections and provides a gateway between asynchronous and SONET networks.

The equipment architecture reduces start-up configuration costs, increases modular growth capability, and allows for reduced floor space. These benefits allow the DACS IV-2000 (512) to be deployed economically in any size office.

## AT&T 2000 Product Family

AT&T is focused on a carefully planned and growing product family designed to provide total network solutions. The 2000 Product Family complies with the SONET standard and builds on items that customers have found necessary to build an efficient and successful network. It includes single-ended maintenance features and in-service upgrade capabilities. The system's modular design allows graceful in-service upgrades to accommodate both synchronous and asynchronous network communications.

The AT&T 2000 product family includes:

- FT-2000 OC-48 Lightwave System — a high-capacity, synchronous digital transmission system.
- DDM-2000 OC-3/OC-12 Multiplexer — a low-capacity, synchronous digital transmission system. The DDM-2000 OC-3/OC-12 multiplexer is designed for loop feeder or interoffice applications.
- DACS III-2000 Cross-Connect System — a software-based, high-capacity, digital cross-connect system that automates many functions performed by manual DSX-3 cross-connect frames.
- DACS IV-2000 (256) Cross-Connect System — a software-based, high-capacity, digital cross-connect system that merges cross-connect and multiplexer functions. It provides interfaces at the STS-1/DS3/DS1 signal rates and cross-connects at the STS-1/VT1.5/DS3/DS1 signal levels.

1. The number 496 is based on the use of DS3 Interface Bays. The DS3 Interface Bays have been rated Discontinued Availability.

- DACS IV-2000 (512) Cross-Connect System — a software-based, high-capacity, digital cross-connect system that merges cross-connect and multiplexer functions. It provides interfaces at the STS-1/DS3/DS1 signal rates, cross-connects at the STS-1/VT1.5/DS3/DS1 signal levels, and has twice the capacity of the (256) system.
- DACScan®-2000 Controller — a workstation that automates control over diversely located network elements, such as the DACS III-2000 and DACS IV-2000 cross-connect systems.
- SLC®-2000 Access System — a system that supports standard switch interfaces such as TR08 and TR303, as well as standard feeder interfaces at DS1 and SONET OC-3 rates.
- Business Remote Terminal-2000 (BRT-2000) — a terminal that provides access for businesses through sophisticated fiber optic telecommunications equipment.

# System Overview

This section describes the DACS IV-2000 (512) system functionality and architecture.

## System Functionality

The following sections explain the DACS IV-2000 in terms of system capacity, signal types, and how these signals function within the system.

### System Capacity

The electronic digital switch in a fully equipped DACS IV-2000 cross-connects any of the following signal types:

- a maximum of 13,888 DS1 signals
- a maximum of 496 DS3 signals
- a maximum of 480 STS-1 signals
- a maximum of 13,440 VT1.5 tributaries of STS-1 signals
- various combinations of the above (not exceeding the switch capacity of 13,888 DS1/13,440 VT1.5).

## Signal Types

The DACS IV-2000 can processes the following signal types: Digital Signal, level 1 (DS1); Digital Signal, level 3 (DS3); Synchronous Transport Signal, level 1 (STS-1); and Virtual Tributary, level 1.5 (VT1.5).

### DS1 Signal

A DS1 is a logical signal with a data rate of 1.544 Mb/s (ANSI T1.107). A DS1 signal is produced by combining 24 DS0 signals (8 bits per DS0) and one synchronizing bit, thereby transmitting 193 bits per frame.

DS1 signals arrive at the frame in any of three ways:

- on DS1 transmission facilities
- as tributaries (components) on DS3 transmission facilities
- as tributaries [VT1.5(DS1)] on Electrical Carrier-1 (EC-1) transmission facilities.

### DS3 Signals

A DS3 signal is a logical or electrical bipolar with three-zero substitution (B3ZS) signal with a data rate of 44.736 Mb/s (ANSI T1.107). For the DACS IV-2000, a traffic-carrying DS3 signal is either framed or unframed (MUX3 only). A framed signal is made up of 28 DS1 signals and control bits used for synchronization and other purposes.

The DS3 signal consists of a succession of masterframes approximately 106 ms long. Each masterframe contains seven subframes, each of which consists of eight data blocks. A data block contains one control bit and 84 data bits, with three data bits coming from each of the 28 DS1 signals that make up the DS3 signal. An unframed DS3 is any DS3 conformant to electrical specifications in ANSI T1.102-1994.

Network elements (NEs), such as the DACS IV-2000, use the control bits to demultiplex the DS3 signals and determine whether to add stuff bits to maintain synchronization of the DS3 signals. DS3 signals arrive at the frame as DS3 facilities.

### STS-1 Signals

An STS-1 is the basic building block signal in the SONET standard ANSI T1.105 and Bellcore TR-TSY-000253. An STS-1 signal has a data rate of 51.84 Mb/s. An STS-1 signal frame consists of 90 columns and 9 rows of 8-bit bytes, for a total of 810 bytes (6480 bits) for a frame length of 125 µs. The first three columns of an STS-1 signal are the transport overhead, which contain overhead bytes of section (9 bytes) and line (18 bytes) layers. The remaining 87 columns of 9 rows of bytes (783 bytes) carry the STS-1 synchronous payload envelope (SPE).

The first column of an SPE defines the STS-1 path overhead (POH), and the remaining columns are available for the payload. The STS-1 SPE can begin anywhere in the STS-1 envelope capacity. (Typically, an STS-1 SPE begins in one frame and ends in the next, although an STS-1 SPE can be wholly contained in one frame.)

The STS-1 payload pointer contained in the transport overhead defines the beginning of the STS-1 SPE. The STS-1 POH is associated with each payload and is used to communicate functions from the point where a service is mapped into the STS-1 SPE to its delivery point.

The DACS IV-2000 can process any of the following information supplied by an STS-1 SPE:

- STS-1 [Virtual Tributary, level 1.5 STS-1 (VT1.5)] — is an STS-1 signal in which the SPE contains 28 floating VT1.5 signals and access to the VT1.5s by the DACS IV-2000 is required. Virtual tributaries are used to transport sub-STS-1 payloads.
- STS-1 [clear channel SPE STS-1 (cc-SPE)] — is an STS-1 signal in which the SPE contents are arbitrary (that is, the SPE can contain 28 VT1.5s, one DS3cc, or some unspecified payload) and access to the payload by the DACS IV-2000 is not required.

STS-1 signals arrive at the frame as EC-1 facilities.

### VT1.5 Signals

A VT1.5 signal is a subrate of a SONET STS-1 logical signal and has a data rate of 1.728 Mb/s. In the 90-column, 9-row structure of the STS-1 SPE, a VT1.5 occupies 3 columns.

VT-structured STS-1 SPEs are divided into 7 VT groups. Each VT group occupies 12 columns of the 9-row structure. The 12-column VT group structure can accommodate four 3-column VT1.5s per group.

The floating mode of operation (supported by the DACS IV-2000) minimizes delay for distributed VT switching.

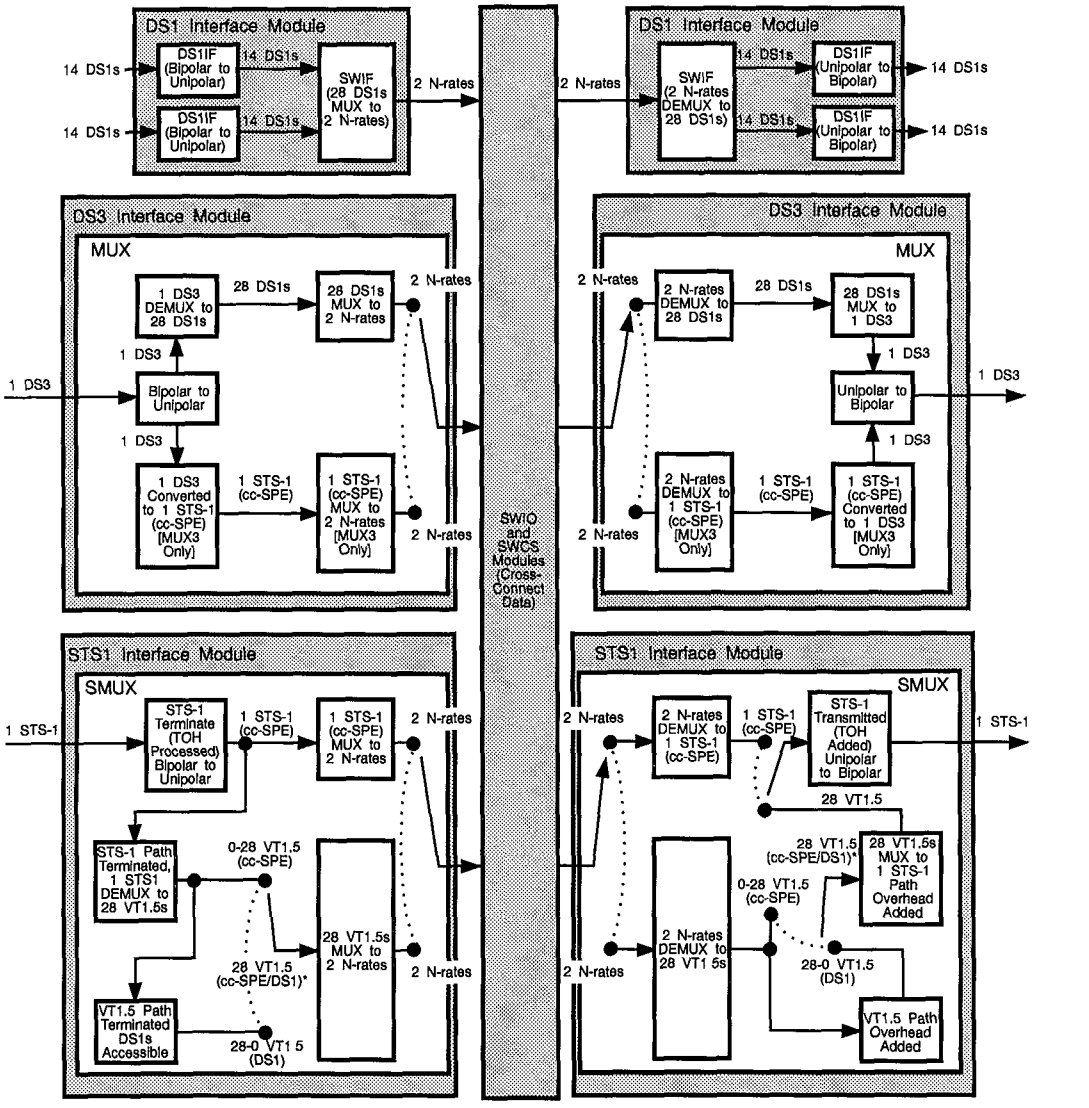
The DACS IV-2000 accepts the following VT1.5 mappings (signal formats are defined in Bellcore GR-253-CORE):

- VT1.5 clear-channel SPE (cc-SPE) — is a VT1.5 signal in which the SPE contents are arbitrary and access to the payload by the DACS IV-2000 is not required. VT1.5(cc-SPE) signals processed by the DACS IV-2000 must use the floating mode of operation. They can be mapped as:
  - Asynchronous — clear channel transports that meet DSX-1 requirements [Bellcore TR-TSY-000499]
  - Byte-synchronous — allows downstream SONET network elements direct identification and access to the 24 DS0 channels that are carried
  - Bit-synchronous — special case mapping of a DS1 signal in the floating VT mode.
- VT1.5(DS1) — is a VT1.5 signal in which the SPE contains one DS1 signal and access to the DS1 signal is required by the DACS IV-2000. VT1.5(DS1) signals processed by the DACS IV-2000 must use the floating mode of operation and must be mapped as asynchronous.

VT1.5 signals can arrive at the frame only as tributaries of EC-1 facilities.

## Signal Paths

To support the different types of signals, the DACS IV-2000 provides DS1, DS3, and STS1 Interface Modules. These modules receive and process the signals, send them to the VT1.5/DS1 switch for cross-connection, regenerate the cross-connected signals, and transmit the signal downstream. Figure 1-1 shows the paths of different signal types (DS1, DS3, and STS-1) within the DACS IV-2000.




* VT1.5(cc-SPE) and VT1.5(DS1) are cross-connected on a per tributary basis. The 28 tributaries that make up an STS-1 signal can contain a mix of VT1.5(cc-SPE) and VT1.5(DS1) signals totalling 28.

Figure 1-1. **DS1, DS3, and STS-1 Signal Paths**

## DS1 Signals

In the receive stage, 28 DS1 signals are received by a DS1 interface group (two DS1IF and one SWIF circuit pack) within a DS1 Interface Module (Figure 1-2). Each DS1IF circuit pack converts 14 DS1 signals from bipolar to unipolar and sends the signals to the SWIF circuit pack. The SWIF circuit pack multiplexes 28 DS1 signals into two N-rate signals (27.648 MHz) and sends the N-rate signals to the SWIO Module for cross-connection.

In the transmit stage, the SWIF circuit pack receives two N-rate signals containing cross-connected DS1 signals from a DS1, DS3, or STS1 Interface Module and demultiplexes the N-rate signals into 28 DS1 signals. Each DS1IF circuit pack receives 14 DS1 signals from the SWIF circuit pack, converts the signals from unipolar to bipolar, and transmits the 14 DS1 signals downstream.

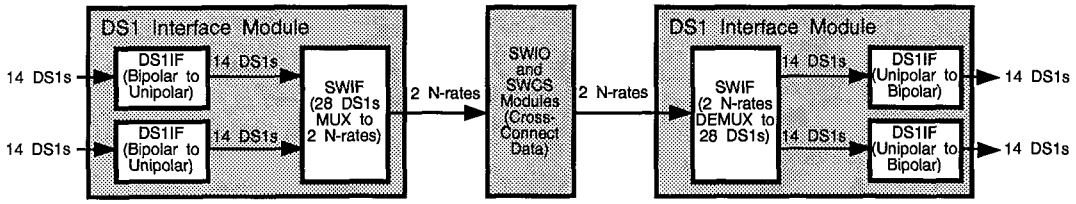



Figure 1-2. **DS1 Signal Path via DS1 Interface Modules**

## DS3 Signals

In the receive stage, a MUX circuit pack within a DS3 Interface Module receives a single DS3 signal (see Figure 1-3). The DS3 signal is processed, depending upon which MUX circuit pack is used, as follows:

- The MUX1 or MUX2 circuit pack converts the DS3 signal from bipolar to unipolar, demultiplexes the DS3 signal into 28 DS1 signals, multiplexes the 28 DS1 signals into two N-rate signals, and sends the N-rate signals to the Switch Module for cross-connection.
- The MUX3 circuit pack processes the DS3 as above, or if provisioned for clear-channel (cc) cross-connection of the DS3, converts the DS3 signal from bipolar to unipolar, maps it into the synchronous payload envelope (SPE) of an STS-1 signal, multiplexes the STS-1 into two N-rate signals, and sends the N-rate signals to the Switch Module for cross-connection.

In the transmit stage, the MUX circuit pack receives two N-rate signals containing cross-connected DS1 signals from a DS1, DS3, or STS1 Interface Module or if provisioned for clear-channel (cc) cross-connect, receives two N-rate signals containing cross-connected DS3cc signals from a DS3CC, or STS1 Interface-16 Module. The N-rate signals are processed, depending upon which MUX circuit pack is used, as follows:

- The MUX1 or MUX2 circuit pack demultiplexes the N-rate signals into 28 DS1 signals, multiplexes the 28 DS1 signals into one DS3 signal, converts the DS3 signal from unipolar to bipolar, and transmits the DS3 signal downstream.
- The MUX3 circuit pack processes the N-rate signals as above, or if provisioned for clear-channel (cc) cross-connection of the DS3, the MUX3 circuit pack demultiplexes the N-rate signals into 1 STS-1 (cc-SPE) signal, converts the STS-1 (cc-SPE) to 1 DS3 signal, converts the DS3 signal from unipolar to bipolar, and transmits the DS3 signal downstream.

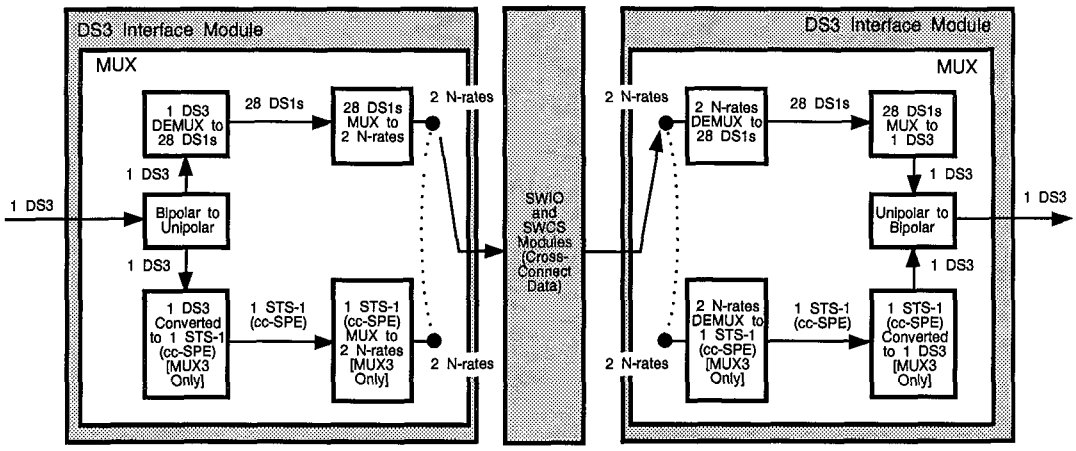
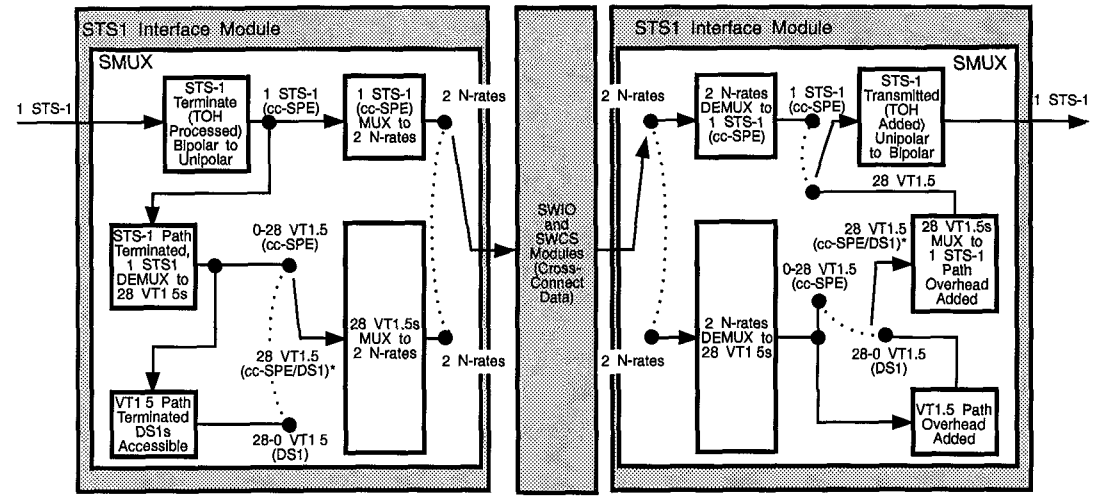



Figure 1-3. **DS3 Signal Path via DS3 Interface Modules**

## STS-1 Signals

In the receive stage, an SMUX circuit pack within an STS1 Interface Module receives a single STS-1 signal (Figure 1-4). The SMUX circuit pack terminates the transport overhead of the STS-1 signal and converts the STS-1 signal from bipolar to unipolar. Depending on the information to be cross-connected, the SMUX circuit pack performs the following functions:

- STS-1(cc-SPE) — the SMUX circuit pack demultiplexes the STS-1 signal into two N-rate signals and sends the N-rate signals to the SWIO Module for cross-connection. Cross-connecting an STS-1 signal as an STS-1(cc-SPE) signal preserves the path of the STS-1 signal through the DACS IV-2000.
- VT1.5(cc-SPE) — the SMUX circuit pack terminates the STS-1 path and demultiplexes the STS-1 signal into 28 VT1.5 tributaries. Each tributary that is to be cross-connected as a VT1.5(cc-SPE) signal receives no more processing before being multiplexed into two N-rate signals and sent to the SWIO Module for cross-connection. Cross-connecting VT1.5 tributaries as a VT1.5(cc-SPE) preserves the path of the VT1.5 tributary through the DACS IV-2000.




* VT1.5(cc-SPE) and VT1.5(DS1) are cross-connected on a per-tributary basis. That is, the 28 tributaries that make up a STS-1 signal can contain a mix of VT1.5(cc-SPE) and VT1.5(DS1) signals totalling 28.

Figure 1-4. **STS-1 Signal Path via STS1 Interface Modules**

- VT1.5(DS1) — the SMUX circuit pack terminates the STS-1 path and demultiplexes the STS-1 signal into 28 VT1.5 tributaries. Each tributary that is to be cross-connected as a VT1.5(DS1) signal has the VT1.5 path terminated so that the DS1 signal can be accessed before being multiplexed into two N-rate signals and sent to the SWIO Module for cross-connection. This allows the DACS IV-2000 to cross-connect DS1 signals to and from STS1 interfaces, providing the synchronous/asynchronous gateway.

In the transmit stage, the SMUX circuit pack receives two N-rate signals containing cross-connected signals from a DS1, DS3, or STS1 Interface Module for VT1.5(DS1) signals, or an STS1 Interface Module for STS-1(cc-SPE) and VT1.5(cc-SPE) signals. Depending on the type of signals received from the SWIO Module, the SMUX circuit pack performs the following functions:

- STS-1(cc-SPE) — the SMUX circuit pack multiplexes the N-rate signals into one STS-1 signal.
- VT1.5(cc-SPE) — the SMUX circuit pack demultiplexes the N-rate signals into 28 VT1.5 tributaries. For tributaries that are cross-connected as VT1.5(cc-SPE) tributaries, no other processing is performed before multiplexing the 28 VT1.5 tributaries that make up an STS-1 signal [combination of VT1.5(cc-SPE) and/or VT1.5(DS1)] into one STS-1 signal and adding the STS-1 path overhead.
- VT1.5(DS1) — the SMUX circuit pack demultiplexes the N-rate signals into 28 VT1.5 tributaries. For tributaries that are cross-connected as VT1.5(DS1) tributaries, the SMUX adds the VT1.5 path overhead before multiplexing the 28 VT1.5 tributaries that make up an STS-1 signal [combination of VT1.5(cc-SPE) and/or VT1.5(DS1)] into one STS-1 signal and adding the STS-1 path overhead.

After generating the STS-1 signal, the SMUX circuit pack adds the STS-1 transport overhead, converts the STS-1 signal from unipolar to bipolar, and transmits the STS-1 signal downstream. For detailed information on all functions performed by the various interface modules and circuit packs, refer to Chapter 3.

## Cross-Connection Capability

Cross-connections may be done at the DS1, DS3, VT1.5, or STS-1 signal level.

When cross-connections are done at the DS1 signal level within a MUX circuit pack, the DS3 signal is demultiplexed into 28 DS1 signals before being sent to the switch matrix.

The SONET interface of the DACS IV-2000 can deliver an STS-1 SPE to the switch matrix to make an STS-1(cc-SPE) cross-connect, or deliver a VT1.5 tributary to the switch matrix to make a VT1.5(cc-SPE) or DS1 (VT1.5/DS1) cross-connect.

The STS-1(cc-SPE) and VT1.5(cc-SPE) signals are cross-connected between STS1 Interface Modules only. A DS1 signal can be cross-connected between DS1, DS3, or STS1 Interface Modules. This allows for both SONET-to-SONET and SONET-to-asynchronous signal interworking, thus achieving gateway functionality.

For a DS3 clear-channel cross-connection, an incoming DS3 signal is connected to another MUX3 circuit pack. In the opposite direction of transmission, the STS-1 signal is extracted from the received pair of N-rate signals from the switch matrix. The DS3 signal is then extracted from the SPE of the STS-1 signal transmitted toward the facility.

For a DS3/STS-1 gateway connection, the signal from the switch matrix is connected to an SMUX1 circuit pack. When this is received from the switch matrix, the transport overhead is added, and an STS1 (DS3) is transmitted toward the facility.

## Facility Administration Capability

A DS1 signal arriving at a DS1 port, a DS3 port, or an STS-1 port can be cross-connected to any output ports. This capability permits both grooming (rearrangement of DS1 components of DS3 or STS-1 signals) and adding or dropping DS1 components of DS3 or STS-1 signals. On the other hand, if none of the DS1 signals within a DS3 or STS-1 signal requires modification before being cross-connected, you can cross-connect all the tributaries of the DS3 or STS-1 signal with a single command.

Similarly, VT1.5 signals arriving as tributaries of an STS-1 signal can be groomed, added, or dropped the same way.

Bridging is the cross-connection of one input port to two output ports. This capability allows for test access to DS1, DS3, VT1.5, or STS-1 signals, and the rerouting (rolling) of signals (temporarily or permanently). DS1, DS3cc, VT1.5, and STS-1 signals can all be bridged by a single command.

- For a DS3cc cross-connection, this signal is connected to a MUX3 circuit pack.
- For a DS3 to STS1 gateway connection, this signal is connected to an SMUX circuit pack.

### Fully Protected Circuit Packs

If a traffic-carrying circuit pack in the DACS IV-2000 fails, the main controller automatically switches to a protection standby circuit pack and reports the failure. The frame also monitors the performance of its other subassemblies and the facilities it cross-connects. When appropriate, it activates alarms, issues failure reports, and sends alarm indication signals downstream.

## Controller Architecture

The DACS IV-2000 control architecture (Figure 1-5) is a distributed multiprocessor design that supports concurrent execution and performs real-time operations. The architecture consists of the following systems:

- High-Capacity Controller System
  - — Duplicated Control Complexes (CPU/MTC/SCI/SSC/UI/OUI circuit packs)
  - — Enhanced Communications Interface (ECI)
  - — Synchronizer Module
- Unit Controller System
  - — Unit Controllers
  - — Interface Circuit Packs
  - — DS3 Performance Monitoring (DS3PM) over a TABS interface (optional).
- Remote Unit Interface System (Remote Complexes Only)
  - — Remote Unit Interface (UIA/UIB/SCI/CLKGN circuit packs)
  - — Optical Extension to/from the HCC and Switch Matrix
  - — Remote Communications Interface (RCI) to the ECI.

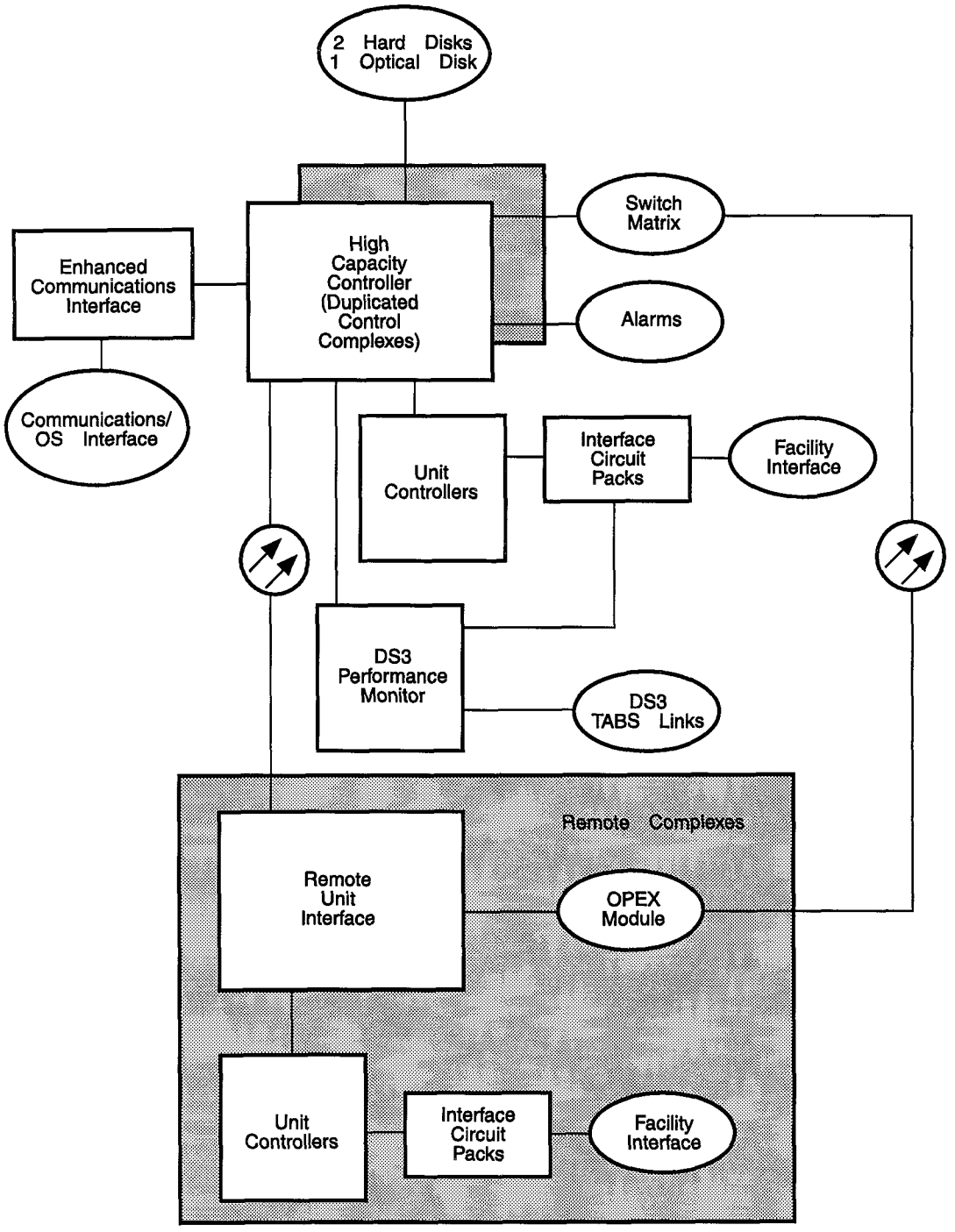



Figure 1-5. **System Controller Architecture**

## High-Capacity Controller System

The central component of the high-capacity controller system is the duplicated controller complex (CC). The CC:

- Runs application software to perform all system administration functions including cross-connection, provisioning, test access, and synchronization for the SONET interfaces
- Serves as the central point of coordination for all system maintenance functions such as diagnostics, fault recovery, and alarms
- Performs all database management functions for the system, with the secondary storage controller providing the interface between the main processor and the nonvolatile storage devices (disk and optical drives).

The Enhanced Communications Interface (ECI) supports the user interface to the duplicated control complex. The ECI:

- Parses commands and generates messages to support the system interface languages: TL1 (Transaction Language 1) and TABS (Telemetry Asynchronous Block Serial)
- Provides the physical and electrical interfaces supporting synchronous (X.25) and asynchronous (Snider, telemetry) protocols.

The two ECI circuit packs are equipped to provide redundancy or to provide additional communication links.

The DACS IV-2000 Release 5.0 contains a Synchronizer Module which accepts two external DS1 timing references. In the event of a timing reference failure, the synchronizer automatically switches to the secondary reference. If both references fail, the synchronizer operates in a stratum 3 holdover mode. The synchronizer is fully protected; if one synchronizer side fails, the system switches to the other side.

## Unit Controller System

The unit controllers (UCs) maintain the DACS IV-2000 high-capacity controller system facility interfaces. The UCs support the high-capacity controller by:

- Providing communications with the interface circuit packs
- Performing real-time maintenance functions such as hardware fault detection.

Individual controllers on some of the enhanced interface circuit packs provide expanded real-time capabilities for features such as enhanced DS1, DS3, and SONET performance monitoring.

The DS3PM circuit pack supports the TABS interface to the DS3 performance data.

**NOTE:**
The DS3PM circuit pack is not required unless you are using TABS interface language. The DS3PM circuit pack is supported in collocated interface bays but not in Remote Complex interface bays.

### Remote Unit Interface System

The Remote Unit Interface (RUI) system provides the following functions:

- Optical Unit Interfaces (OUIs), which replace the UI circuit packs in the HCC Module, provide LAN distribution functions for the (512) Switch Complex and also provide optical interface (for control) to the Remote Complexes.
- The UIA and UIB circuit packs provide LAN hubbing functions from the OUI circuit packs to the Remote Unit Interface.
- RCI provides RS232-to-RS422 conversion for CILINKs to the Remote Complex.
- Optical Extension (OPEX) circuit packs optically connect the Remote Complex interface modules to the Switch Complex Optical SWIO (OSWIO) circuit packs (OSWIO circuit packs replace the SWIO circuit packs).

## Hardware Architecture

The DACS IV-2000 hardware consists of an arrangement of a Switch Complex, collocated interface bays and/or Remote Complexes. The Switch Complex contains one Main Controller Bay and two Switch Bays. Up to sixteen interface bays (with up to four Fuse and Alarm Bays) can be collocated with the Switch Complex. A Remote Complex can be used in place of collocated interface bays and consists of an Optical Extension Bay and up to eight interface bays. All Switch Complex and enhanced interface bay types use the seismic bay framework.

### Equipment Bays

The bay types are:

- Main Controller (MC) Bay — provides the control for the system. This bay contains a fan assembly to provide cooling of the associated equipment.
- Switch (SW) Bay — provides the cross-connections and interbay cabling. This bay contains a fan assembly to provide cooling of the associated equipment.
- Fuse and Alarm (FS & ALM) Bay — provides fuses for up to four collocated interface bays.

- Optical Extension (OPEX) Bay — provides the interface for extending the N-rate signals from the interface bays of a DACS IV-2000 Remote Complex onto fiber-optic cables to the SWIO Modules of the Switch Complex. The controller functions are also extended from the High-Capacity Controller (HCC) to the Remote Complex by fiber optic cables.
- DS1 Interface (INTFC) Bay — provides the interface for up to 868 DS1 signals (equivalent to 31 DS3 signals). Air baffles are provided for equipment cooling.
- Enhanced DS1 Interface (INTFC) Bay — provides the interface for up to 868 DS1 signals (equivalent to 31 DS3 signals). This bay contains a fan assembly to provide equipment cooling and also provides additional space for cable routing.
- DS3 Interface (INTFC) Bay — provides the interface for up to 62 DS3 signals (equivalent to 1736 DS1 signals). Air baffles are provided for equipment cooling.

**NOTE:**
The DS3 Interface Bay has been rated Discontinued Availability.

- STS1/DS3 Interface (INTFC) Bay — provides the interface for up to 60 DS3 or STS-1 signals (each DS3 is equivalent to 28 DS1 signals). This bay contains a fan assembly to provide equipment cooling.
- Enhanced STS1/DS3 Interface (INTFC) Bay — provides the interface for up to 60 DS3 or STS-1signals (each DS3 is equivalent to 28 DS1 signals). This bay contains a fan assembly to provide equipment cooling and also provides additional space for cable routing.
- STS1/DS3/DS1 Interface (INTFC) Bay — provides the interface for:
  - — Up to 420 DS1 signals (equivalent to 15 DS3 signals) and
  - — Up to 46 DS3 signals (equivalent to 1288 DS1 signals) and no STS-1 signals, up to 31 DS3 signals (equivalent to 868 DS1 signals) and 15 STS-1 signals, or up to 30 STS-1 signals and no DS3 signals.

  Air baffles are provided for equipment cooling.
- Enhanced STS1/DS3/DS1 Interface (INTFC) Bay — provides the interface for:
  - — Up to 420 DS1 signals (equivalent to 15 DS3 signals) and
  - — Up to 46 DS3 signals (equivalent to 1288 DS1 signals) and no STS-1 signals, up to 31 DS3 signals (equivalent to 868 DS1 signals) and 15 STS-1 signals, or up to 30 STS-1 signals and no DS3 signals.

  This bay contains a fan assembly to provide equipment cooling and also provides additional space for cable routing.

## Equipment Modules

The system bays contain modules comprising circuit packs to create the different functional segments of the DACS IV-2000. Figure 1-6 (Collocated configuration) and Figure 1-7 (Remote Complex configuration) are functional block diagrams showing the main components of the DACS IV-2000 (512).

Each module in the system is equipped with circuit packs. These circuit packs are required to perform the functions of the system.

The High-Capacity Controller, Memory Storage, Switch Center Stage, and Switch Power Modules (located in the Switch Bays) are always fully equipped with the required circuit packs.

The Remote Complex is equipped with circuit packs UIA and UIB to communicate with the OUI circuit packs in the HCC. These interface by a duplex optical link.

The Switch Input/Output Modules located in the Switch Bays and the DS1, DS3, and STS1 Interface Modules located in the interface bays are equipped as required with circuit packs, depending on service requirements.

The Synchronizer Module must be fully equipped when used in systems supporting SONET interfaces and/or DS3 Clear-Channel cross-connections. Use either Version 1 or Version 2 circuit packs with this release.

Circuit packs are identified by functional name and circuit pack code. A suffix number after a circuit pack functional name indicates a series version. When there is no suffix number, a **1** is assumed. Higher series versions can be substituted in slots labeled for a lower series version, but not the reverse. For example, a PWRE3 circuit pack can be substituted in a slot labeled PWRE, but a PWRE1 circuit pack cannot be substituted in a slot labeled PWRE2 or other higher series version.

## Switch Complex Modules

The (512) Switch Complex consists of two Switch Bays and the Main Controller Bay. The modules housed in these bays are:

- Two Switch Bays
  - — Switch Input/Output (SWIO) Module — performs the cross-connection functions in conjunction with the Switch Center Stage Modules. For systems that use Remote Complexes, the associated modules are equipped with optical SWIO (OSWIO) circuit packs in place of SWIO circuits packs to allow for the receiving/transmitting of the extended N-rate signals from optical fiber cable from/to the Optical Extension (OPEX) Module.
  - — Switch Center Stage (SWCS) Module — performs the cross-connection functions in conjunction with the Switch Input/Output Modules.

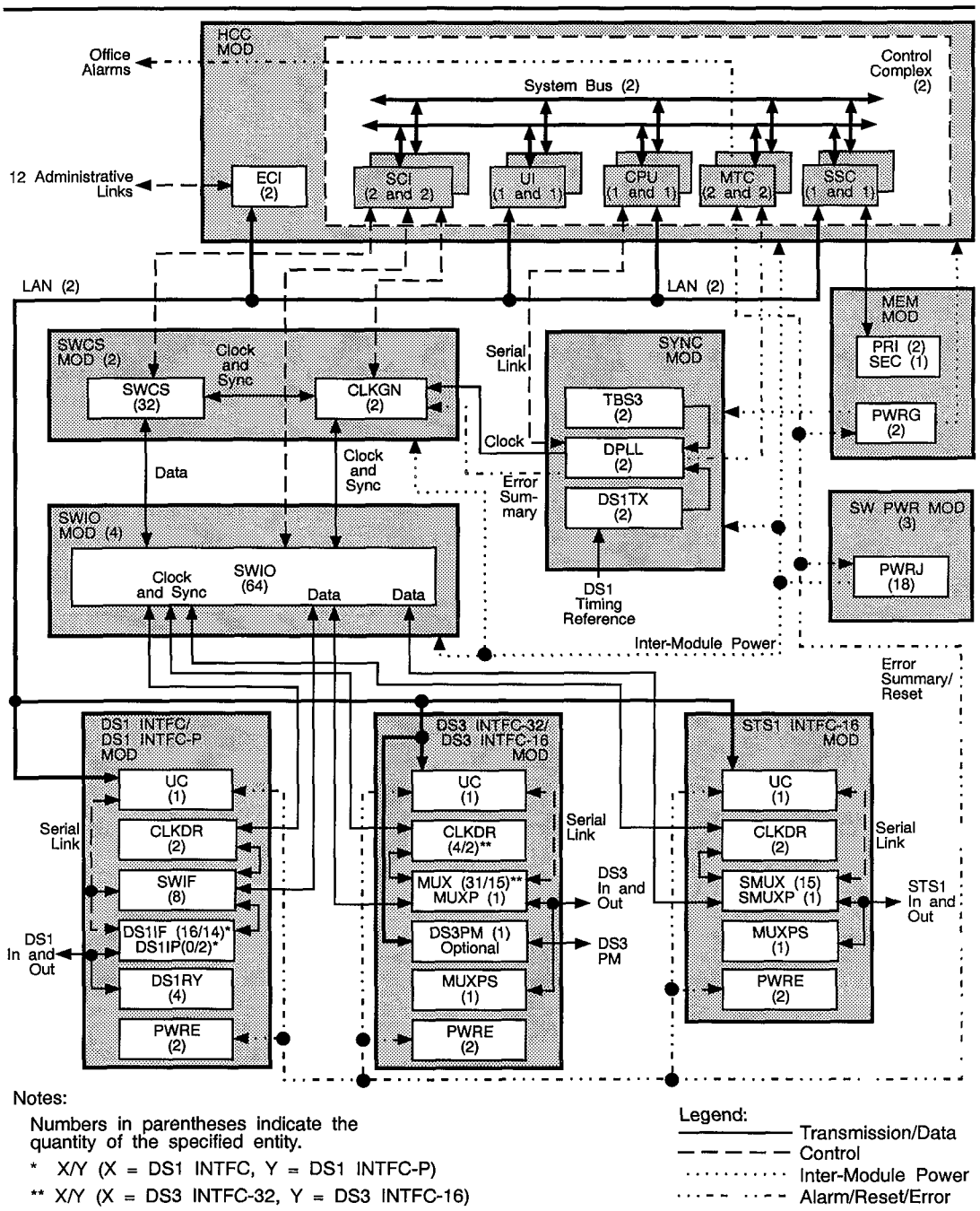
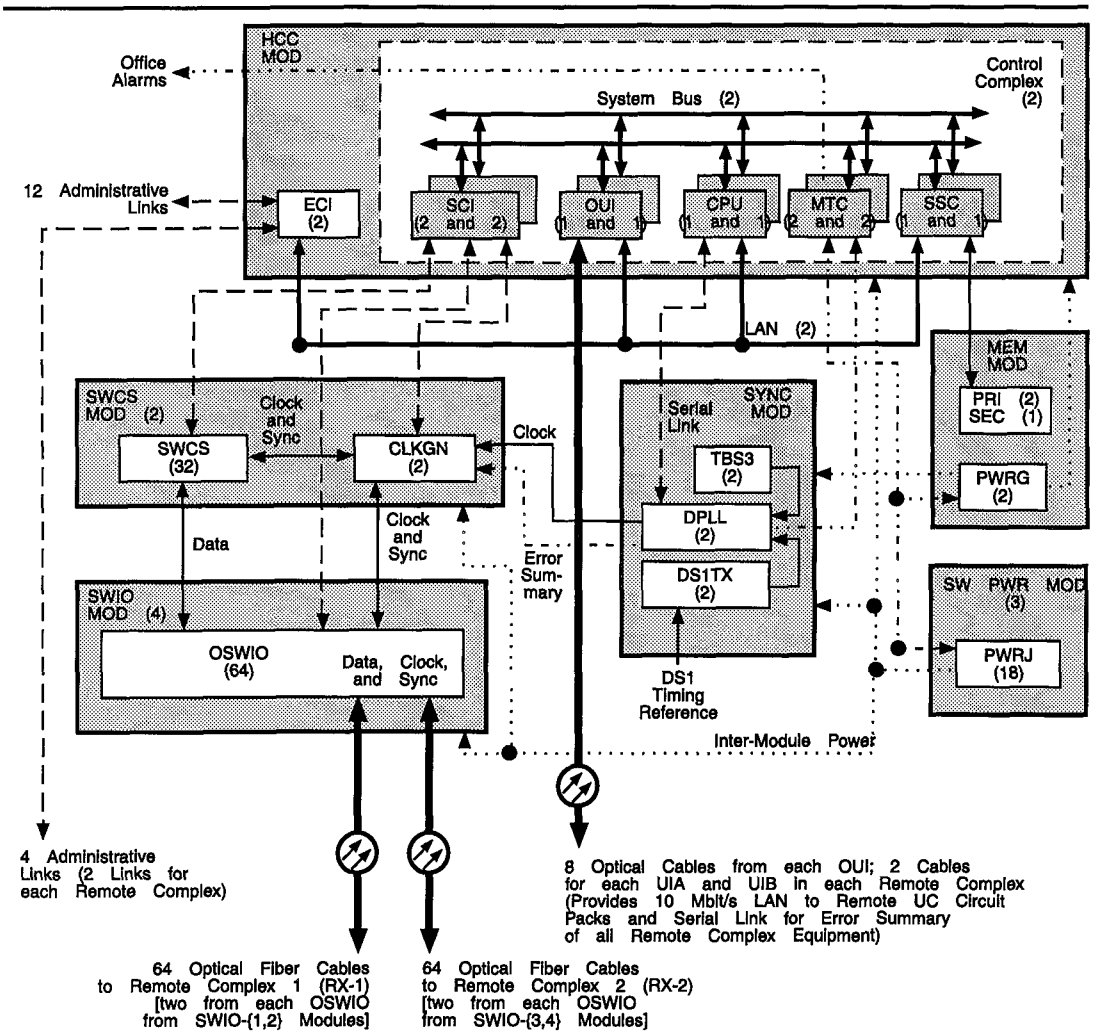



Figure 1-6. **Functional Block Diagram — Collocated Configuration**




Notes:

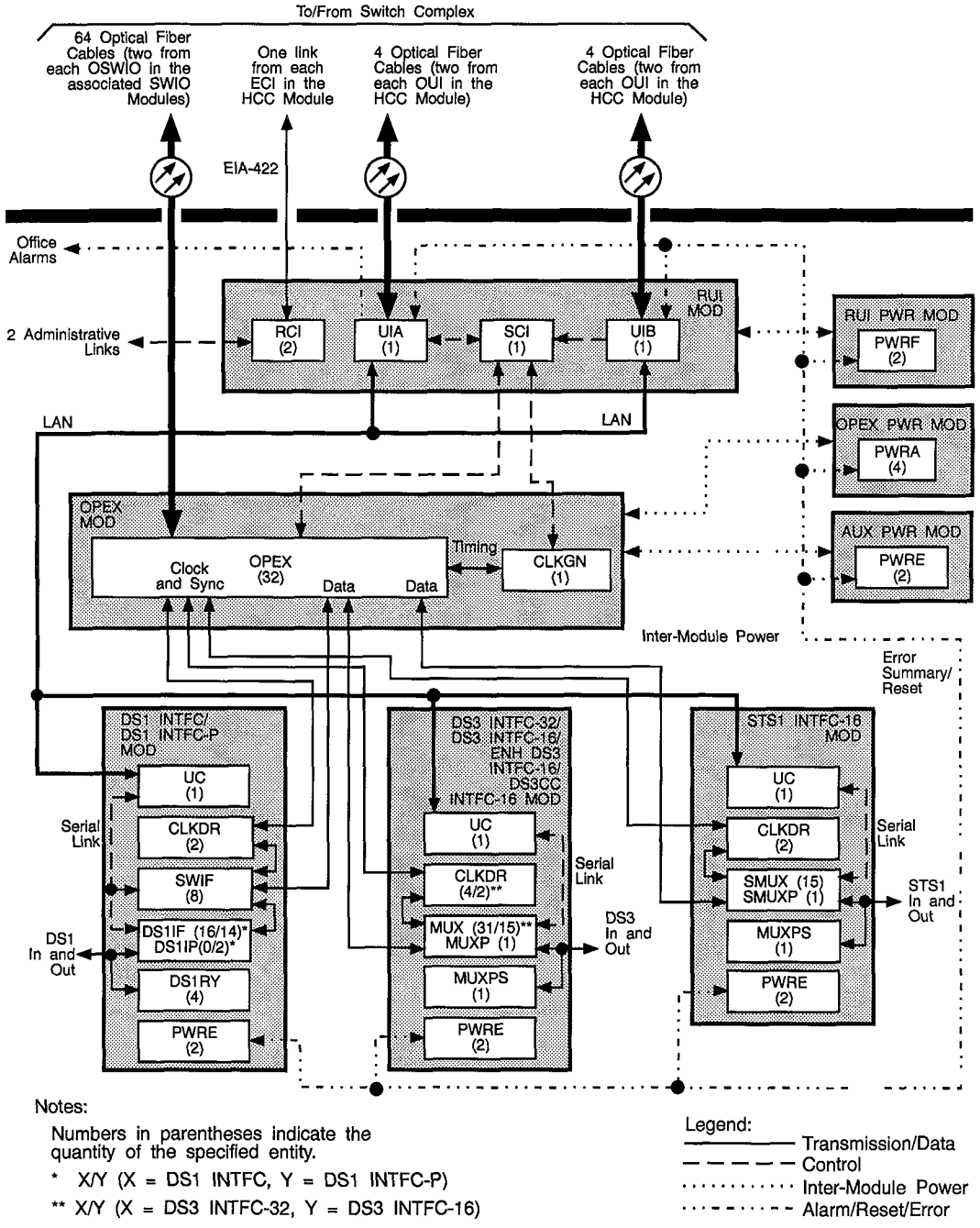
Numbers in parentheses indicate the quantity of the specified entity.

Legend:

- Transmission/Data
- Control
- Inter-Module Power
- Alarm/Reset/Error

A. Switch Complex

Figure 1-7. **Functional Block Diagram — Remote Complex Configuration (Sheet 1 of 2)**




## B. Remote Complex

Figure 1-7. **Functional Block Diagram — Remote Complex Configuration (Sheet 2 of 2)**

- Main Controller Bay
  - — High-Capacity Controller (HCC) Module — manages the user interface (administrative links), performs user-specified functions, and coordinates database management, maintenance, and fault recovery operations. For systems that use Remote Complexes, this module also provides the controlled functions to the Remote Complex. These functions are communicated over fiber optic cables to the Remote Unit Interface (RUI) Module.
  - — Switch Power (SW PWR) Module — provides the +5 Vdc and -5 Vdc power and fuse protection for the High-Capacity Controller, the Switch Input/Output, and the Switch Center Stage Modules.
  - — Synchronizer (SYNC) Module — generates the timing information for the DACS IV-2000.
  - — Memory Storage (MEM) Module — provides primary and secondary program and database backup capabilities. In addition, provides the means to load new software release onto the frame. Also provides the +12 Vdc and -12 Vdc power for the MEM and HCC modules.

## Remote Complex Modules

The Remote Complex is a DACS IV-2000 (256) frame (containing at least one Interface Bay and an OPEX Bay) whose Switch Module is replaced with an OPEX Module and connected with optical fiber to the Switch Input/Output (equipped with OSWIO circuit packs) Module in the Switch Complex of a (512) system with at least 256 DS3 equivalents available. The modules contained in the OPEX Bay are:

- Optical Extension (OPEX) — is based on the Switch Module in the (256); it contains circuit packs for optically connecting the N-rate signals to and from the Remote Complex Interface Modules and the switch matrix (OSWIO and SWCS circuit packs) of the Switch Complex.
- Optical Extension Power (OPEX PWR) — provides the +5V required by the OPEX circuit packs.
- Auxiliary Power (AUX PWR) — provides the -5.2V power for the OPEX Module.
- Remote Unit Interface (RUI) — contains the Unit Interface (UIA and UIB) circuit packs that optically extend the controller functions from the High-Capacity Controller in the Switch Complex to the Remote Complex. In addition, the RUI Module contains the Remote Communications Interface (RCI) circuit packs that are used to provide a communications interface terminal at the Remote Complex.
- Remote Unit Interface Power (RUI PWR) — provides power and fuse protection for the RUI Module.

## Interface Modules

Interface Bays are available for either collocation with the Switch Complex or with a Remote Complex. When collocated with the Switch Complex, Fuse and Alarm Bays are required to provide fuse protection for up to four Interface Bays. Fuse protection for remote Interface Bays are provided by the Fuse and Alarm Panel in the OPEX Bays. The following Interface modules can be equipped in the various interface bays:

- DS1 Interface (INTFC) Module — provides up to 224 DS1 interfaces for the incoming and outgoing DS1 facilities or network elements. These modules accept DS1 signals (in a format that is compatible with a DSX-1) and interface these signals to and from the Switch Module. Protection for the interfaces of these modules are provided by the DS1 Interface-Protection Module contained in the same DS1 Interface Bay.
- DS1 Interface-Protection (INTFC-P) Module — provides up to 196 DS1 interfaces for the incoming and outgoing DS1 facilities or network elements. These modules accept DS1 signals (in a format that is compatible with a DSX-1) and interface these signals to and from the Switch Module. These modules provide protection for itself in addition to the other DS1 Interface Modules (up to three) within the same DS1 Interface Bay.
- DS3 Interface-32 (INTFC-32) Module — provides up to 31 DS3 interfaces with protection for incoming and outgoing DS3 facilities. These modules accept DS3 signals in a M13 or C-bit parity format compatible with a DSX-3 and interface the signals to and from the Switch Module.
- DS3 Interface-16 (INTFC-16) Module — provides up to 15 DS3 interfaces with protection for incoming and outgoing DS3 facilities. These modules accept DS3 signals in a M13 or C-bit parity format compatible with a DSX-3 and interface the signals to and from the Switch Module.
- Enhanced DS3 Interface-16 (ENH DS3 INTFC-16) Module — provides up to 15 DS3 interfaces with protection for incoming and outgoing DS3 facilities. These modules accept framed DS3 signals in a format compatible with a DSX-3 and interface the signals to and from the Switch Module. In this module, the DS1s within the received DS3s can have full-time DS1 performance monitoring, without loss of system capacity.
- DS3 Clear-Channel Interface-16 (DS3CC INTFC-16) Module — provides up to 15 DS3 interfaces with protection for incoming and outgoing DS3 facilities. These modules accept DS3 signals in a format compatible with a DSX-3 and interface the signals to and from the Switch Module. When the MUX3 circuit pack is operating in the DS1 mode, the received DS3 must be framed. When the MUX3 circuit pack is operating in the clear-channel mode, the received signal format can be framed or unframed. In this module, the DS1s within the received DS3s can have full-time DS1 performance monitoring, without loss of system capacity.

- STS1 Interface-16 (INTFC-16) Module — provides up to 15 interfaces with protection for incoming and outgoing EC-1 facilities. These modules accept STS-1 signals in a format compliant with the SONET specifications and interface the signals to and from the Switch Module.

# System Features

# 2

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# System Features

# 2

This chapter introduces the new features that are available with the DACS IV-2000 (512) Release 5.0 and summarizes the features that were introduced with earlier releases.

## New Features

The DACS IV-2000 (512) Release 5.0 offers the following new features:

- In-Service Capacity Expansion of DACS IV-2000 (256) System
- Optical Remoting of Interface Bay Complexes
- DS3 Clear-Channel Cross-Connection
- DS3 to STS-1 Gateway Cross-Connection
- DS3 Path Identification for the AT&T Transport Self-Identification Plan (TRANSID)
- Full-Time Performance Monitoring of DS1 Tributaries within DS3 Facilities without loss of capacity
- Unframed DS3 Signals
- DS3 Terminal Loopback
- DS3 Test Access
- VT1.5 group/port numbering
- Synchronizer Enhancements
  - — firmware download
  - — end-of-range for timing references
  - — standby monitoring.

## Capacity Expansion of the DACS IV-2000 (256) System

Capacity expansion allows customers to minimize the number of DACS IV-2000 systems needed in larger offices by absorbing one or two DACS IV-2000 (256) system into the Switch Complex of a DACS IV-2000 (512) system. This simplifies facility provisioning and reduces the number of facilities required between DACS IV-2000 frames.

With this feature, the capacity of a DACS IV-2000 (256) system can be expanded to that of a DACS IV-2000 (512) system while maintaining service and with no need to rearrange the EC-1, DS3, or DS1 cabling to the existing bay lineup. You are able to grow the original (256) system bay lineup to its full capacity of 256 equivalent STS-1/DS3s (service and protection), and grow an additional capacity of 256 equivalent STS-1/DS3s in interface bays located in the same lineup with the DACS IV-2000 (512) Switch Complex or in a second Remote Complex.

Capacity expansion is supported for all allowable system configurations of the DACS IV-2000 (256). The DACS IV-2000 (256) Interface Bays can be located remotely from the DACS IV-2000 (512) Switch Complex (up to 1000 feet cabling distance from the existing system). The DACS IV-2000 (256) system database is automatically converted to Release 5.0, and all cross-connection maps associated with the interface bays, modules, and facilities are preserved during the capacity expansion (no loss of service).

Use of the capacity expansion feature reduces the number of intertie facilities necessary. Capacity expansion is accomplished using optical remoting.

## Optical Remoting of Interface Bay Complexes for the DACS IV-2000 (512) System

To provide flexibility in the placement of interface bays within a central office, the DACS IV-2000 supports optical remoting of one or two Remote Complexes.

Each Remote Complex can support half the system capacity, with the remaining half of the capacity supported by either collocated interface bays or by a second Remote Complex.

The DACS IV-2000 (512) allows optical remoting of up to 248 STS1/DS3 equivalent ports to one Remote Complex and up to 248 STS1/DS3 equivalent ports to another Remote Complex. (This remoting is done through the use of OSWIO-fiber-OPEX links.) A total of 496 STS1/DS3 equivalent capacity can be remoted.

The maximum distance between the DACS IV-2000 (512) Switch Complex and the Remote Complexes is 1000 cable feet of optical fiber.

## Optical Extension Bay

The capacity of a DACS IV-2000 (256) system is expanded to that of a DACS IV-2000 (512) system by using Optical Extension (OPEX) circuit packs in the DACS IV-2000 (256) Optical Extension Bay to extend the N-rate signals from the interface bays onto fiber-optic cables.The fiber-optic cables terminate on Optical Switch Input/Output (OSWIO) circuit packs in the Switch Complex of the DACS IV-2000 (512).

The OPEX circuit packs receive N-rate data from the facility interface modules, multiplex it to a higher line rate (1.106 Gbps), convert it to an optical signal, and send it over the fiber to its corresponding OSWIO circuit pack at the DACS IV-2000 (512) Switch Complex.

## Optical Switch Input/Output

The OSWIO circuit pack, which is plug-compatible with the existing SWIO circuit pack, provides:

- SWIO functionality
- Circuitry for multiplexing and demultiplexing data signals to the optical line rate
- Optical interfaces to send and receive transmission data and timing information to and from the Remote Complex.

## Remote Communication Links

This feature is associated with the optical remoting feature. The two ECI circuit packs in pre-Release 5.0 High-Capacity Controller Modules provided twelve administrative links (six per ECI circuit pack). These links are identified as CILINK 1-1 through CILINK 1-6 and CILINK 2-1 through CILINK 2-6. As part of the optical remoting feature, the two ECI circuit packs in the (256) system are replaced with one or two Remote Communications Interface (RCI) circuit packs that are interfaced to the ECI circuit packs in the (512) system. The new RCI circuit packs provide one link each, at the two Remote Complexes. These additional links for the two Remote Complexes are identified as CILINK 1-7 and 2-7 for Remote Complex 1, and 1-8 and 2-8 for Remote Complex 2.

The two spare links already available on each of the (512) ECI6 circuit packs provide additional asynchronous link capability for the Remote Complexes. Providing a pair of Snider links at each of the Remote Complexes allows the central office technician the flexibility to monitor and maintain the DACS IV-2000 system from either a Remote Complex or from the (512) Switch Complex.

## Optical Remoting Configurations

The DACS IV-2000 (512) Release 5.0 supports two optical remoting configurations, which are described below and shown in Figure 2-1.

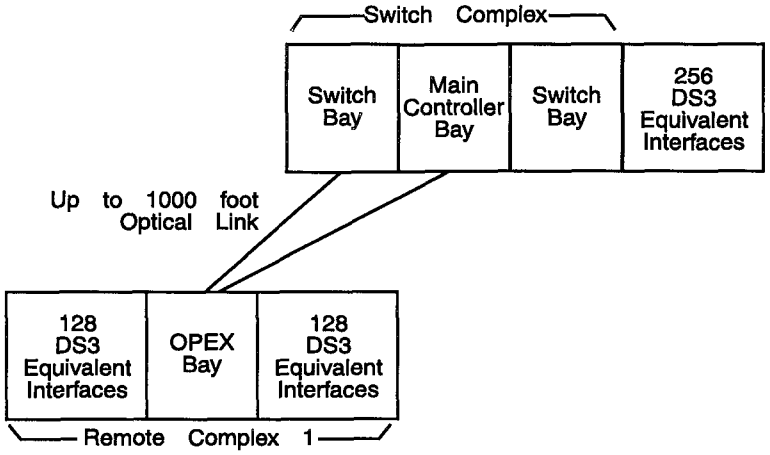
- A single DACS IV-2000 (256) frame that may have been in service and capacity-expanded to a DACS IV-2000 (512) frame. Any facilities that were tied between the (256) and (512) systems are now available for additional capacity (Figure 2-1A).

  In Figure 2-1A, the circuit packs within the Switch Bay of the (256) system are replaced, thereby converting the Switch Bay to an Optical Extension (OPEX) Bay. The OPEX Bay is then connected with optical cable to the associated SWIO Modules in the Switch Complex of a half-equipped (512) system. The (256) system then becomes a Remote Complex of the (512) system.

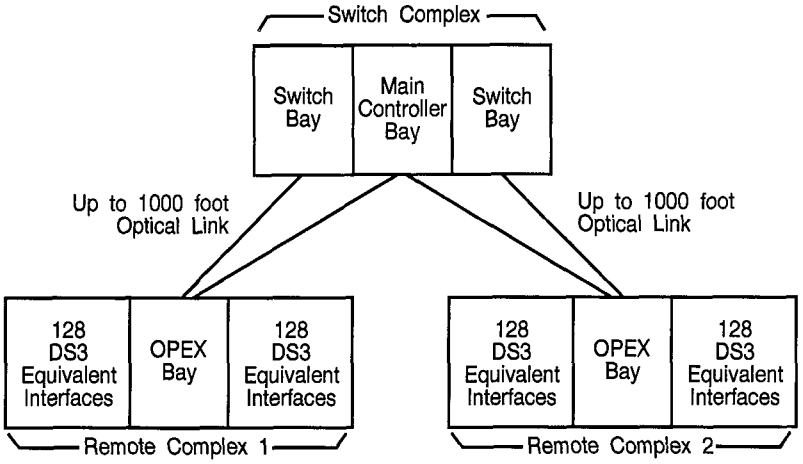
- Two DACS IV-2000 (256) frames and a DACS IV-2000 (512) Switch Complex. Either Remote Complex (or both) may have been capacity expanded to the (512) (Figure 2-1B).

  In Figure 2-1B, the (512) bay lineup consists of only the Switch Complex. The two (256) systems (either fully equipped or partially equipped) are located within 1000 cable feet of a (512) Switch Complex. During one capacity expansion procedure, the circuit packs within one of the (256) Switch Bays are replaced, thereby converting the Switch Bay to an OPEX Bay. The OPEX Bay is then connected with optical cable to the associated Switch Bay in the (512) Switch Complex. This (256) system now becomes a Remote Complex of the (512) system. During a second capacity expansion procedure, a second (256) system can be capacity-expanded onto the (512) Switch Complex.

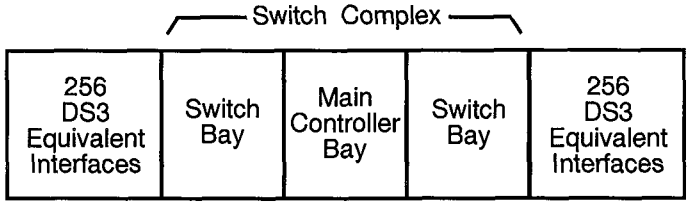
- Figure 2-1C shows a single DACS IV-2000 (512) Switch Complex with collocated interface bays. Since no (256) frames are used, optical remoting is not used in this configuration.




**A. Single Remote Complex**




**B. Two Remote Complexes**




**C. 512 Collocated System (No Remoting)**

Figure 2-1. **Optical Remoting Configurations**

## Upgrade Overview

You can control the Remote Complex by replacing the High-Capacity Controller Module circuit packs with new circuit packs that receive control information over fiber-optic cables from the High-Capacity Controller. Replace the unit controllers (UCs) and clock distributors in the Remote Complex with new UCs and clock distributors that communicate with the Control Complex via a 10-Mb/s LAN. Replace the SWIO circuit packs with OSWIO circuit packs on the associated (512) Switch Bay. In addition, the following changes are made to support capacity expansion and optical remoting:

- The Clock Distributor 2 (CLKDR2) circuit pack replaces the Clock Distributor 1 (CLKDR1) circuit pack.
- The OPEX Module replaces the Switch Module
- The OPEX PWR Module replaces the Switch Power Module
- The RUI Module replaces the RC Module (becoming an extension of the HCC Module)
- The RUI PWR Module replaces the RC Power Module
- Remove the Synchronizer Module from the OPEX Bay
- Remove the PWRG circuit packs and the SWCS circuit packs from the OPEX Module.

The upgrade is accomplished entirely through circuit pack replacement and fiber-optic cable installation. The fiber is connected to the circuit pack faceplates. The only access to the backplane that may be required is:

- Installation of a 1-Mb/s LAN Interface Assembly to support the DACSmate™ connection for DACS IV-2000 (256) systems that do not already have it installed
- Installation of the new DACSmate cable assembly for DACS IV-2000 (512) systems shipped prior to General Availability (GA) for customers who are upgrading with the optional Remote Communication Links.

Once upgraded, the DACS IV-2000 (256) becomes a Remote Complex of the DACS IV-2000 (512), located within 1000 cable feet.

If the DACS IV-2000 (256) that is to be capacity-expanded has a Synchronizer Module provisioned, the DACS IV-2000 (512) must have a Synchronizer Module installed and in service. Either version 1 or version 2 circuit packs may be installed on the DACS IV-2000 (512), regardless of what version synchronizer is active on the DACS IV-2000 (256).

The DACSmate workstation communicates with each DACS IV-2000 frame via CILINK 1-1 and the frames' internal LANs. Because the DACS IV-2000 (256) has a 1-Mb/s LAN and the DACS IV-2000 (512) has a 10-Mb/s LAN, DACSlink 2.0 must be used to provide the 10:1 bridge function. The DACSmate must be located within 330 cable feet of the DACS IV-2000 frame; the DACSlink rollup bay must be located within 50 cable feet (RS-232 limitation) of the DACS IV-2000 (512) frame. If you need to go beyond 330 feet, use fiber adapters.

Prior to the execution of the capacity expansion procedure, an automated consistency check of the system databases must be performed. Inconsistencies (such as hourly vs. 15-minute performance monitoring bins) must be identified and eliminated before proceeding with capacity expansion.

The entire capacity expansion procedure, excluding preparation time, should be completed in one eight-hour period. (Time is measured from the point when facility cross-connection provisioning is unavailable until it becomes available again.) During this time, automatic protection switching and alarm reporting should not be disabled for more than four hours.

The upgrade procedure will not cause more than three short signal disruptions to any traffic carried by the system. Prior to the capacity expansion procedure, you will be able to designate up to 233 bidirectional DS1/VT1.5 circuits as high-priority and they should have no signal disruptions of more than 60 ms.

The N-rate and interface cabling within the DACS IV-2000 (256) system will not be moved or otherwise affected during capacity expansion.The -48V power cabling to the DACS IV-2000 (256) system will not be moved or otherwise affected during capacity expansion.

## DS3 Clear-Channel Cross-Connection

DS3 clear-channel cross-connection capability is particularly valuable in smaller central offices where, for example, a separate DACS III-2000 is not cost-effective, but where a need exists for DS3 reconfiguration services. DS3 clear-channel allows a DACS IV-2000 to perform the functions of a DACS III-2000 for the DS3 ports equipped with the new circuit pack (MUX3). This flexibility is particularly needed for ports that interface to signals from an end customer (for example, loop access to a business) because the end customer may want to use the same DS3 facility at times to carry DS1 signals and at other times to carry DS3 signals for applications such as video conferences.

The DACS IV-2000 can bridge DS3 connections by cross-connecting the DS3 or STS1 input port of any connection to any DS3 or STS1 output port without affecting service in the existing path. This feature is used for DS3 facility rolling.

## MUX3 Circuit Pack

The new DS3 interface circuit pack (MUX3) is provisionable to either demultiplex the DS3 into DS1 tributaries or to map the entire DS3 (including overhead bits) into N-rate signals for transmission to the switch matrix. In the latter mode, a clear-channel (cc) cross-connection of the DS3 signal is supported to another MUX3 or SMUX1 interface circuit pack.

The MUX3 circuit packs support DS3 clear-channel cross-connections to other MUX3 circuit packs or gateway connections to SMUX1 circuit packs. In a DS3 clear-channel cross-connection, all received bits in the incoming signal, including all overhead bits, are transmitted unchanged. If there is a loss-of-signal (LOS) condition on the received DS3, a DS3 AIS signal is sent toward the switch matrix. A MUX3 circuit pack that is provisioned for DS3 cross-connection, but where no cross-connection has been established, can transmit a DS3 idle signal.

## DS3 to STS-1 Gateway Cross-Connection

As telecommunications networks evolve to SONET, there is a mix of synchronous and asynchronous transport and a corresponding need to provide connections between them and facilitate rolls of DS3 facilities to SONET.

With Release 3.0, the DACS IV-2000 had the capability to provide a gateway between synchronous and asynchronous signals at the VT1.5/DS1 level; it did not have the capability to extract a DS3 signal directly mapped into an STS-1.

In Release 5.0, the new MUX3 circuit pack has the capability to map the incoming DS3 signal into the STS-1 format for cross-connection through the switch matrix to an SMUX circuit pack. In the opposite direction of transmission, an STS-1 signal is sent through the switch matrix and then mapped into the DS3 format. This provides the capability to connect DS3 signals that have been carried on SONET transmission systems as DS3-mapped STS-1s to existing asynchronous DS3 equipment.

The DACS IV-2000 Release 5.0 supports cross-connections between DS3s that interface to MUX3 circuit packs and STS-1s that interface to SMUX1 circuit packs. The received DS3 signal is mapped into the synchronous payload envelope (SPE) of an STS-1in accordance with Bellcore GR-253-CORE, *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria* (Issue 2, December 1995). The resulting STS-1 signal is then transmitted toward the switch matrix in the N-rate format compatible with the SMUX1 circuit pack. In the opposite direction of transmission, the STS-1 signal is extracted from the received pair of N-rate signals from the switch matrix. The DS3 signal is then extracted from the SPE of the STS-1 and transmitted toward the facility. Gateway cross-connections are denied if the incoming STS-1 has a signal label indicating that it is not carrying an asynchronous DS3.

If a gateway cross-connection exists between a MUX3 and an SMUX, and a signal label match failure (SLMF) is detected, the DACS IV-2000 Main Controller (MC) reports the SLMF facility failure condition as an SMUX-detected failure condition and reports the SWSLMF facility failure condition as a MUX3-detected failure condition.

When SLMF is detected by a MUX3 cross-connected as a DS3 clear-channel circuit, MC reports this as a SWSLMF condition.

If a loss-of-signal (LOS) condition exists on the received DS3, a DS3 AIS signal is mapped into the transmitted STS-1. If STS-1 AIS, STS-1 idle, or an STS-1 with other than DS3 mapping is received from the switch matrix, a DS3 AIS is transmitted toward the facility. If a DS3 LOS or LOF is detected by the MUX3 circuit pack, any existing DS1 alarms associated with this DS3 are retired. If a gateway cross-connection is present between a MUX3 and an SMUX, the MUX3 is able to detect the STS path yellow facility condition.

Bridging and one-way and two-way rolling are supported for DS3 signals interfacing to the MUX3 circuit pack when it is provisioned to support DS3 clear-channel cross-connections and DS3 to STS-1 cross-connections.

## DS3 Path Identification for the AT&T Transport Self-Identification Plan

The AT&T Transport Self-Identification (TRANSID) Plan uses data links within the DS1 and DS3 facilities to carry unique identifiers that specify the endpoints of the facility, the equipment type and location that generated the signal, and the type of signal (normal traffic, idle signal, or a test signal). TRANSID is available only with the MUX2 (AKM68) and the MUX3 (AKM91) circuit packs.

DS3 path identification lets you assign a set of identifiers to each transmitted C-bit parity DS3 facility. (The identifiers are carried in the row 5 terminal-terminal data link of the C-bit format.) You can also assign an "expected received" identifier to each DS3 port, and the DACS IV-2000 compares the "expected received" identifier with the actual identifier read from the incoming DS3 facility. A mismatch generates autonomous alarms or, provisionably, substitutes DS1 AIS downstream to prevent inadvertent cross-connection of an incorrect facility.

Benefits of DS3 path identification include faster provisioning and testing of circuits, since the facility IDs can be retrieved directly from the DACS IV-2000 rather than requiring separate test signals to confirm path continuity. In the event of a reroute to restore traffic after a failure (such as a cable cut), the DS3 path identification feature can eliminate the need for separate continuity checking of the alternate paths before restoring traffic.

The TRANSID DS3 Path ID feature has four basic capabilities; it can:

- Provision and retrieve the identification for each DS3 signal
- Autonomously transmit and read the DS3 identification in the data link of a C-bit parity format signal; that is, read/write row 5 of the C-bit parity DS3 signal
- Take appropriate actions if a mismatch occurs between the expected and actual Common Language Location Identifier (CLLI) and Common Language Facility Identifier (CLFI), or if a DS3 identification cannot be read on the incoming C-bit parity format signal

- Construct and transmit the appropriate DS3 identification for the C-bit parity format signal if a protection switch occurs.

TRANSID is supported for DS3 signals terminating on MUX2 and MUX3 circuit packs. MUX3 circuit packs that are provisioned for clear-channel cross-connection (either to another DS3 or to an STS1) support reading of the TRANSID identifiers, but not provisioning of the transmitted values or of "expected received" values.

## Full-Time Performance Monitoring of DS1 Tributaries within DS3 Signals

Performance monitoring (PM) of DS1 facilities has been a major customer application of the DACS IV-2000, replacing much more expensive collocated monitoring equipment. The MUX3 hardware also supports monitoring of the DS1 signals received from the switch matrix and transmitted to the DS3 facility.

The MUX3 circuit pack provides full-time path PM of all 28 DS1 tributaries on the received DS3 facility with no need to bridge to a separate circuit pack (the PMGR circuit pack in previous releases).

**NOTE:**
DS1 far-end performance monitoring, per AT&T TR-54016, is not supported in this release.

The MUX3 circuit pack supports full-time path PM of all DS1 tributaries in the incoming DS3 signal that are either superframe (SF) or extended superframe (ESF) format. Received SF format tributaries are monitored by counting errors in the framing bits. Received ESF tributaries are monitored using the CRC-6 code and framing-bit errors. Far-end performance monitoring is supported on ESF format using the ANSI T1.403 Performance Report Message (PRM) on the facility data link.

## Unframed DS3 Signals

The unframed DS3 signal feature enables the DACS IV-2000 to support unformatted DS3 signals. The 45-MB data signals are sent through the DACS IV-2000 without loss of bandwidth.

## DS3 Terminal Loopback

The DACS IV-2000 supports DS3 terminal loopback for DS3 clear-channel or DS3-to-STS-1 cross-connection. When it is provisioned for DS3 clear-channel or DS3-to-STS-1 cross-connection, you can establish a terminal loopback for DS3 signals cross-connected as DS3 clear-channel signals. The incoming DS3 signal is bridged in the switch matrix to go to both the original cross-connection output port and the output port associated with the same input port (that is, on the same MUX3). Bipolar violations are not preserved for terminal loopbacks. Refer to the section titled Loopback Test Access on page 2-55.

## DS3 Test Access

The DACS IV-2000 supports test access for DS3 signals interfacing to the MUX3 circuit pack when it is provisioned to support DS3 clear-channel cross-connections and DS3-to-STS-1 cross connections.

Any MUX3 circuit pack that is not being used to carry traffic can be provisioned as a DS3 test access port. The same modes are available for the DS3 as are available for DS1 and STS1 test access.

## VT1.5 Numbering Scheme

The DACS IV-2000 Release 5.0 provides users the ability to choose between two numbering schemes to address VT1.5 signals within an STS-1. One method is to number the VT1.5 signals sequentially (1 through 28); this is known as the port numbering method and is analogous to the numbering of DS1 signals within a DS3 signal. The second method is to use the combination of VT group and VT1.5 port; this is known as the group numbering method. The selection of the VT1.5 numbering scheme is done on a per-user basis (`ENT-SECU-USER` or `ED-SECU-USER` commands).

**NOTE:**
In the software, the port numbering method is referred to as `VT1.5NUM` and the group numbering method is referred to as `VTGROUP`.

## Enhanced Synchronizer Module

DACS IV-2000 synchronization (first introduced in Release 3.0) allows the DACS IV-2000 to act as a gateway between synchronous and asynchronous networks. The DACS IV-2000 (512) Release 5.0 provides enhancements to the Synchronizer Module that comply with Bellcore GR-1244-CORE[1], *Clocks for the Synchronized Network: Common Generic Criteria* (Issue 1, June 1995) and Bellcore GR-253-CORE, *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria* (Issue 2, December 1995).

In addition to its previous capabilities, the Synchronizer Module now has the following enhancements:

- Contains LEDs on its version 2 circuit packs to indicate active or alarm states [see Circuit Pack Alarms on page 2-88]. The intensity, arrangement, label position, and spacing for the LEDs comply with the requirements of TR-TSY-000824, OTGR Section 10.1: *User System Interface User System Access* (Issue 2, February 1988).

  The Synchronizer Module must contain the same vintage (version 1 and version 2) circuit packs on each side. To facilitate a smooth transition to version 2, the software supports both version 1 circuit packs (DPLL1, DS1TX1, TBS31) and version 2 circuit packs (DPLL2, DS1TX2, TBS32). In normal operation, all three circuit packs of the same vintage are on both SYNC side must be of the same vintage. If they are not, the Synchronizer circuit packs cannot be restored via the same `RST-EQPT` command. If circuit packs of the same vintage are on both SYNC sides and the circuit packs are not in a failed state, no synchronizer hardware-related alarms appear on the system.
- Supports field-upgradable firmware to minimize future hardware changes (firmware download)
- Offers improved lock-time performance
- Locks to an external reference when modulated with input jitter per GR-1244-CORE.
- End-of-range for timing references
- Stand-by monitoring.

See the sections titled Synchronizer (SYNC) Module on page 4-15 or Synchronizer (SYNC) Module on page 5-26, for detailed information.

1. Provisionable revertive/non-revertive reference switching is currently not supported.

# Feature Description

The DACS IV-2000 (512) Release 5.0 supports the following features, which were introduced in previous releases:

- SONET Networking
- Upgrade
- Cross-Connections
- Bridging and Rolling
- Loopbacks
- Test Access
- Performance Monitoring
- High-Capacity Controller
- Duplex Power Configuration
- Performance Monitor Test Signal Generator Receiver and Test Signal Identification
- Alarm Reporting
- Communications and OS Interfaces
- Facility Maintenance
- Facility Failure Detection
- Frame Maintenance
- Protection Switching.

## SONET Networking

The DACS IV-2000 provides SONET networking, which is the ability to perform all of the functionality associated with SONET interconnection. The SMUX circuit pack terminates an EC-1 facility and allows for cross-connection of the entire STS-1 SPE, demultiplexing of VT1.5-based STS-1s and cross-connection of VT1.5s to other SONET interfaces, or cross-connection of DS3s (when equipped with the MUX3 circuit pack) or DS1s. This same circuit pack also provides in-line performance monitoring of the SONET signal, including VT1.5 tributaries of the STS-1. Additional circuit packs are not required, and no deloading of switch capacity is required to accommodate the SONET performance-monitoring feature.

The DACS IV-2000 also supports operational, maintenance, and administrative features necessary for full SONET networking capability.

## SONET Interface

The DACS IV-2000 is fully compliant with SONET STS-1 industry standards, allowing interconnection with AT&T's transmission equipment (such as DDM-2000 and FT-2000) and any other vendor equipment that meets these standards. The DACS IV-2000 provides for EC-1 SONET termination on STS1 interfaces. STS1 interfaces are housed in STS1 Interface-16 modules located in the STS1/DS3 Interface Bay or the STS1/DS3/DS1 Interface Bay.

The DS3 Interface-32 Module in the STS1/DS3/DS1 Interface Bay can be replaced with an STS1 Interface-16 Module to provide for an additional 15 STS-1 signals of capacity. This results in a reduction of total system capacity, because 16 slots in the module must be left unequipped.

The capacity of the STS1/DS3 Interface-16 Module is designed to support fifteen service circuit packs and one protection circuit pack. Each SMUX circuit pack terminates one EC-1 line and supports all of the SONET capabilities described in this chapter.

## Upgrade

The DACS IV-2000 (512) Release 5.0 supports two distinct types of upgrades:

- Minimal upgrade of a DACS IV-2000 (512) Release 3.0 to a DACS IV-2000 (512) Release 5.0. If you have a DACS IV-2000 (512) pre-Release 3.0, you must first upgrade to Release 3.0.
- Capacity expansion upgrade of a DACS IV-2000 (256) Release 3.0, Release 4.0, or Release 5.0 to a DACS IV-2000 (512) Release 5.0. If you have a DACS IV-2000 (256) Pre-Release 3.0, you must first upgrade to a (256) Release 3.0.

**NOTE:**
There is no Release 4.0 for the (512) platform.

## Minimal Upgrade

A minimal upgrade of a DACS IV-2000 (512) Release 3.0 to a DACS IV-2000 (512) Release 5.0 requires no hardware changes. However, to take advantage of new features introduced in Release 5.0:

- Replace at least one MUX2 circuit pack with a MUX3 circuit pack (or all MUX2 circuit packs, only within the module, with MUX3 circuit packs to use the clear-channel feature). The PMGR circuit packs are no longer needed, thereby enabling you to provision additional MUX2 and/or MUX3 circuit packs.
- A Synchronizer Module is required for clear-channel operations.
- Replace the MUXP2 circuit pack with the MUXP3 circuit pack.

## Capacity Expansion

The capacity expansion upgrade is accomplished entirely through circuit pack replacement, fiber-optic cable installation, and database mapping in both the (256) and (512) systems.

To support capacity expansion, use DACSmate software to perform the upgrade. Also, the (256) system must contain a 1-Mb/s LAN interface assembly to connect to the DACSmate PC, and a DACSmate cable assembly must be present on the (512) system.

In the case of the (256) platform, the software is upgraded as part of the capacity expansion process. Note that unit numbering must be taken into consideration because some unit numbers on the (256) and the (512) before the expansion may be identical. Also upgrade associated operations systems.

To support the capacity expansion upgrade to Release 5.0, replace circuit packs in both systems. For the Switch Complex, replace:

- SWIO2 (ERA4) with OSWIO (ERY1)
- UI3 (ERA10) with OUI (ERT1)
- Eight PWRJ (568A) [specifically {1,3}–{1,2,5,6}] with PWRJ (568B) if remote interfaces are used
- Filler assemblies and covers with applicable equipment.

For the Remote Complex, replace:

- SWIO1 (AWR6) with OPEX (ERW3)
- MTC3 (AWR10) with UIA (ERW1)
- UI2 (AWR12) with UIB (ERW2)
- CPU2 (AWP6) with BXC3 (AWP20)
- CLKGN1 (if present) must be replaced with CLKGN2 (AWR7)
- ECI3 (AWP8) with RCI (AWP19)
- UC2 (AKM59B) with UC4 (AKM88B)
- CLKDR1 (AKM56) with CLKDR2 (AKM90).

## Transmission Interfaces

The DACS IV-2000 provides the following interface bay types:

- DS1 Interface Bay: contains three DS1 Interface Modules and one DS1 Interface Protection Module, which provide the interface for up to 868 DS1 signals (equivalent to 31 DS3 signals)
- STS1/DS3 Interface Bay: contains a combination of four DS3 Interface-16 or STS1 Interface-16 Modules, which provide the interface for up to 60 DS3 signals (no STS1 Interface Modules) or 60 STS-1 signals (no DS3 Interface-16 Modules)

- STS1/DS3/DS1 Interface Bay, which contains:
  - — One DS1 Interface Module and one DS1 Interface Protection Module, which support up to 420 DS1 signals (equivalent to 15 DS3 signals)
  - — One DS3 Interface-32 Module and one DS3 Interface-16 or STS1 Interface-16 Module.

  When equipped with a DS3 Interface-16 Module, the bay supports up to 46 DS3 signals. When equipped with an STS1 Interface-16 Module, the bay supports up to 31 DS3 signals and 15 STS-1 signals.

Refer to the section titled Bay Configurations on page 3-20 for examples of fully configured systems.

Note that the DS3 Interface Bay has been rated Discontinued Availability. The DS3 Interface-32 Module is still available on the STS1/DS3/DS1 Interface Bay. The existing DS3 Interface Bays will continue to be supported.

## Cross-Connections

The DACS IV-2000 provides end-to-end SONET cross-connections and SONET/asynchronous gateway connections. This feature allows SONET-to-SONET and SONET-to-asynchronous signal interworking.

The DACS IV-2000 electronically cross-connects DS3, DS1, VT1.5, and STS-1 signals. The cross-connections are implemented with a three-stage space division switch. The DACS IV-2000 switch network is nonblocking and can perform the following types of cross-connections:

- STS-1 (clear-channel SPE) signals between SONET interfaces. By cross-connecting STS-1 (clear-channel SPE) signals, SONET end-to-end path connectivity is maintained via the DACS IV-2000.
- VT1.5 signals between SONET interfaces. VT1.5 end-to-end path connectivity is maintained through the DACS IV-2000 with this type of cross-connection.
- DS1 signals between SONET interfaces. DS1 signals are accessed by terminating the path of the VT1.5 signals and extracting the DS1 signal.
- DS1 gateway cross-connection between SONET and DS1/DS3 interfaces. These types of cross-connections provide the SONET/asynchronous gateway connection.
- DS1 signals between DS1/DS3 interfaces
- DS3 gateway cross-connection between SONET and DS3 interfaces. These types of cross-connections provide the SONET/asynchronous gateway connection.
- DS3 Clear-Channel signals between DS3 interfaces.

Release 5.0 supports both one-way and two-way DS3 Clear-Channel cross-connections between any pair of MUX3 DS3 interfaces or between a MUX3 DS3 interface and a SONET STS-1 interface. DS3 signals can be demultiplexed into DS1 tributaries for cross-connection as individual DS1s, or the entire DS3 can be mapped into N-rate signals for transmission to the switch matrix.

The MUX3 circuit pack has the capability to map the incoming DS3 signals into the STS-1 format for cross-connection through the switch matrix to an SMUX circuit pack. This provides the ability to connect DS3 signals that have been carried on SONET transmission systems as DS3-mapped STS-1s to existing asynchronous DS3 equipment.

The DACS IV-2000 can perform one-way, two-way, and bridged cross-connections. These functions can be performed on DS1, DS3, VT1.5, and STS-1 signals. The DACS IV-2000 implements cross-connections from commands received over one of the administrative links from either a local terminal or from a centralized operations center. In addition to implementing cross-connections, commands are provided for map retrieval. These commands are used to retrieve more data about input ports that are mapped to output ports. In addition, data can be retrieved about DS1 ports that are transmitting quasi-random signals.

## DS1 Cross-Connections

The DACS IV-2000 switch network can cross-connect up to 6,944 DS1 (240 equivalent DS3) one-way signals from terminating DS3, DS1, and STS-1 facilities and/or network elements.

The DACS IV-2000 can cross-connect a DS1 signal on any incoming port to any outgoing port. This allows DS1 grooming (the rearrangement of DS1 signals in DS3 signals and/or STS-1 signals) on the DS3 or STS-1 facilities without the need for back-to-back multiplexers. This feature also allows adding or dropping DS1 signals from outgoing or incoming DS3 or STS-1 facilities as well as DS1-to-DS1 cross-connections. Figure 2-2 shows these capabilities (for simplicity, only one-way cross-connections are shown).

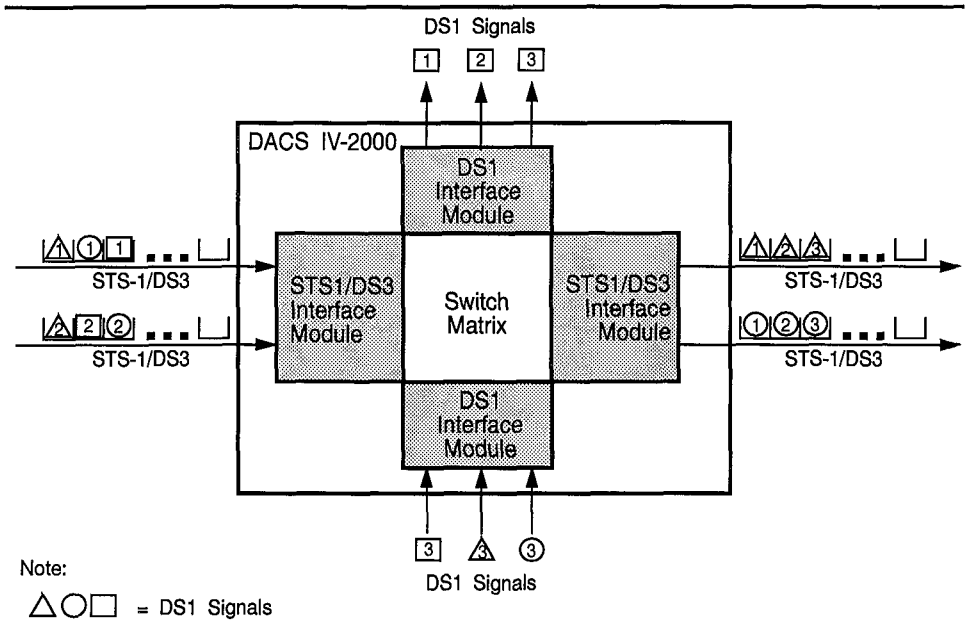
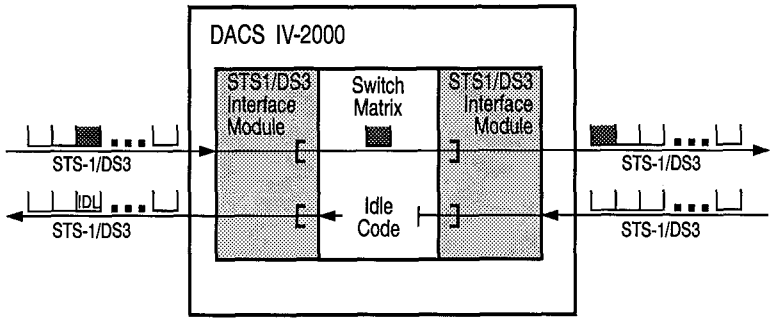



Figure 2-2. **DS1 Cross-Connects (One-Way)**

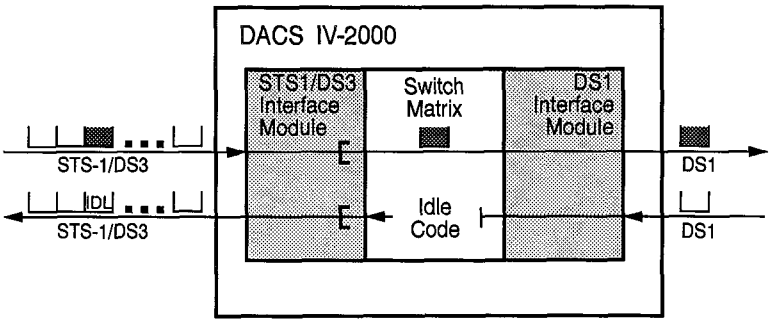
Three types of DS1 cross-connections are possible with the DACS IV-2000: One-Way, Two-Point DS1 cross-connect; Two-Way, Two-Point DS1 cross-connect; and Bridged DS1 cross-connect.

- One-Way, Two-Point DS1 Cross-Connection — Figure 2-3 shows the DACS IV-2000 can cross-connect one direction only of a two-point DS1 cross-connection. The corresponding DS1 in the other direction can be independently cross-connected or terminated with no cross-connection, in which case a DS1 idle code or other external generator signal pattern is transmitted on the unused DS1 facility. The DS1 idle code consists of unframed all ones.



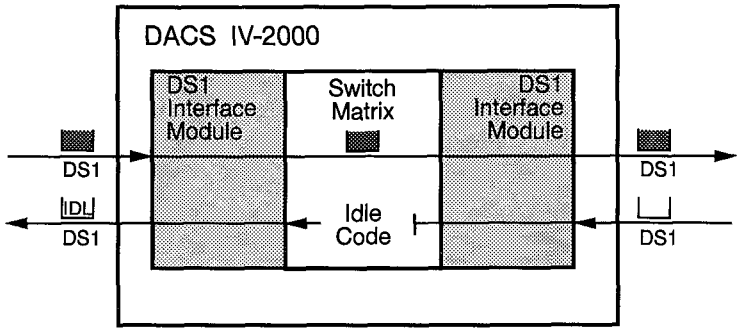

Notes:
IDL = DS1 Idle Code
⊣ = Termination
[ = MUX/DEMUX

**A. STS-1/DS3 to STS-1/DS3**




Notes:
IDL = DS1 Idle Code
⊣ = Termination
[ = MUX/DEMUX

**B. STS-1/DS3 to DS1**

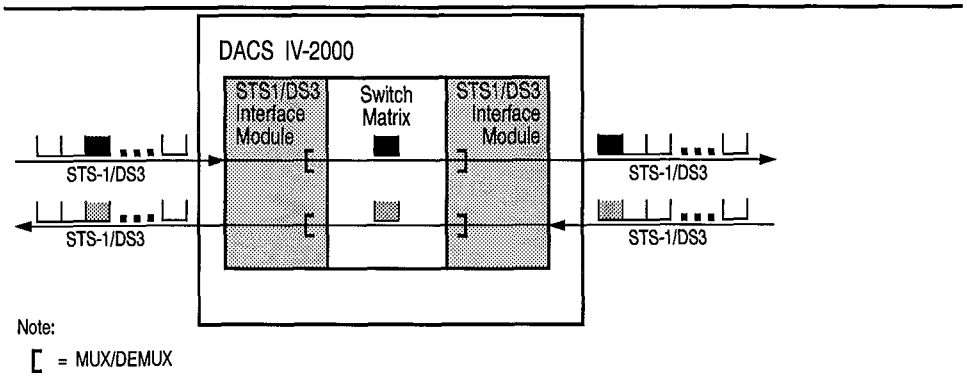



Notes:
IDL = DS1 Idle Code
⊣ = Termination

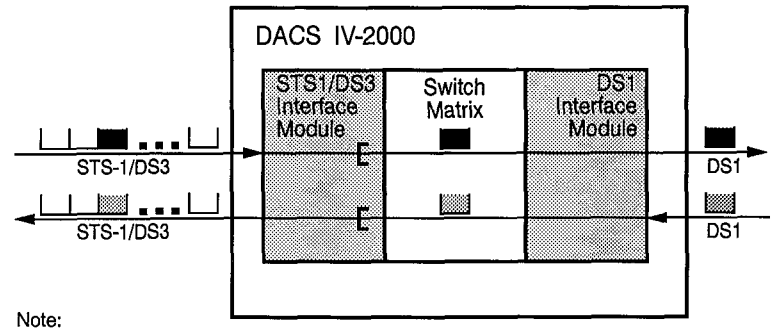
**C. DS1 to DS1**

Figure 2-3. **One-Way, Two-Point DS1 Cross-Connection**

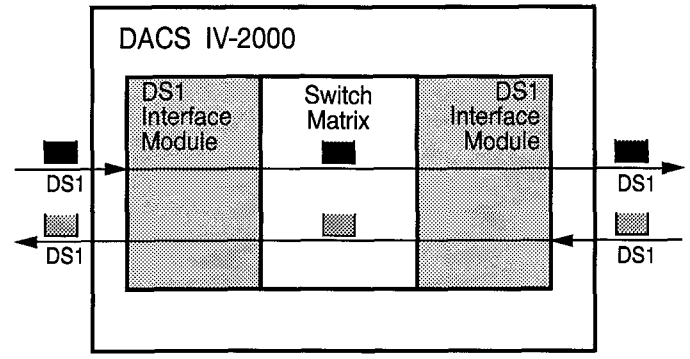
- Two-Way, Two-Point DS1 Cross-Connection — Figure 2-4 shows examples of a two-way, two-point DS1 cross-connection. With a single command, the DACS IV-2000 can cross-connect both directions of a DS1 signal on any incoming DS1, DS3, or STS-1 port to any outgoing DS1, DS3, or STS-1 port.




**A. STS-1/DS3 to STS-1/DS3**



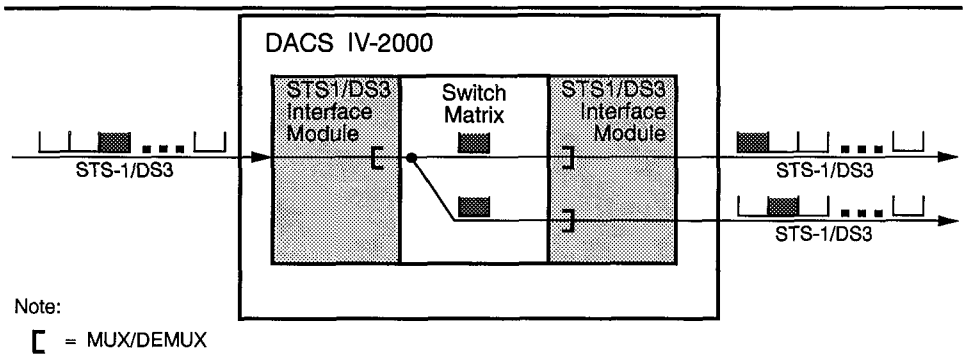

**B. STS-1/DS3 to DS1**



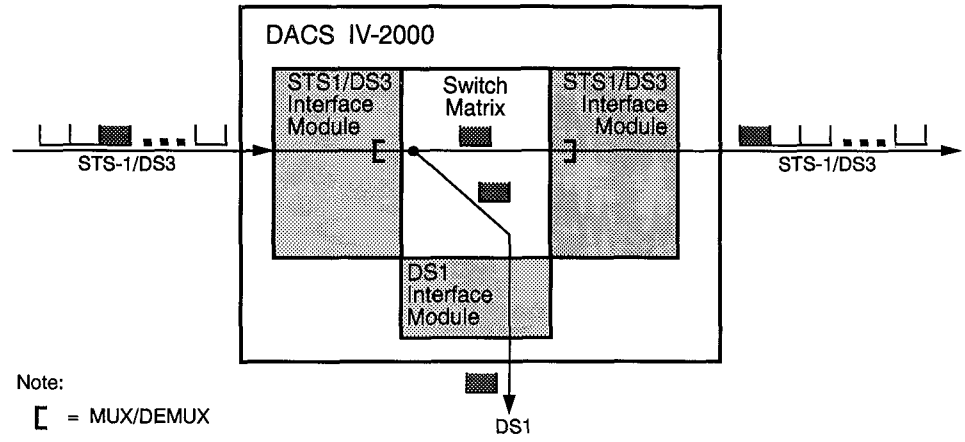

**C. DS1 to DS1**

Figure 2-4. **Two-Way, Two-Point DS1 Cross-Connection**

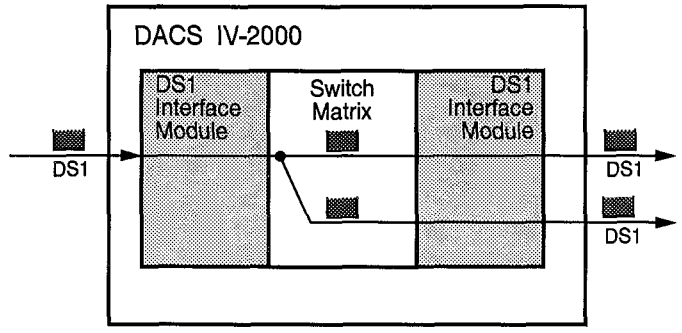
- Bridged DS1 Cross-Connection — Figure 2-5 shows examples of the DACS IV-2000 bridging existing DS1 connections by cross-connecting the DS1, DS3, or STS-1 input port of the existing connection to a second DS1, DS3, or STS-1 output port without affecting service in the existing path. This feature is used for DS1 facility rolling.




**A. STS-1/DS3 to STS-1/DS3**




**B. STS-1/DS3 to DS1**



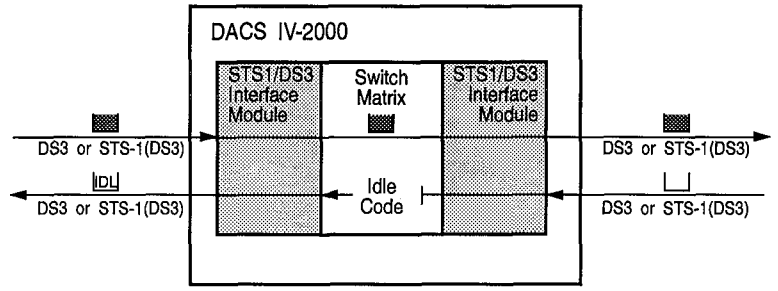

**C. DS1 to DS1**

Figure 2-5. **Bridged DS1 Cross-Connections**

## DS3 Cross-Connections

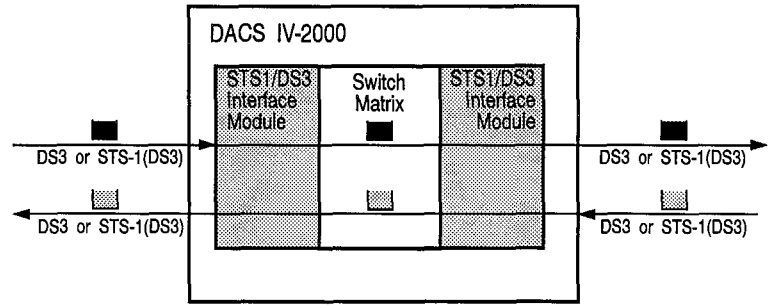
The DACS IV-2000 switch network can cross-connect up to 240 DS3 signals from terminating T3 facilities (on MUX3 circuit packs) and/or network elements. The DACS IV-2000 can cross-connect a DS3 signal on any incoming DS3 port to any outgoing DS3 port. In addition, if an STS-1 port is provisioned for DS3 signals, a gateway connection can be made between an STS-1 port and a DS3 port. Three types of DS3 cross-connections are possible with the DACS IV-2000:

- Two-Point DS3 Cross-Connection, One-way — Figure 2-6A shows a one-way DS3 cross-connection of a two-point cross-connection. The corresponding DS3 signal in the other direction can be independently cross-connected or terminated with no cross-connection, in which case a DS3 idle signal is transmitted on the unused T3 facility.
- Two-Point DS3 Cross-Connection, Two-way — Figure 2-6B shows a two-way DS3 cross-connection of a two-point cross-connection. A single command can cross-connect both directions of an DS3 signal on any incoming DS3 port to any outgoing DS3 port.
- Bridged DS3 Cross-Connection — Figure 2-6C illustrates how the DACS IV-2000 can bridge any existing DS3 connection by cross-connecting the DS3 input port of the existing connection to a second DS3 output port without affecting service in the existing path. This feature allows for DS3 facility rolling.

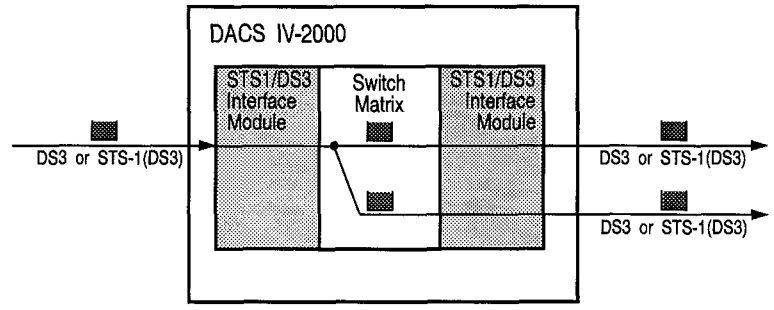



Notes:
IDL = DS3 Idle Signal
⊣ = Termination

**A. Two-Point, One-Way**




**B. Two-Point, Two-Way**



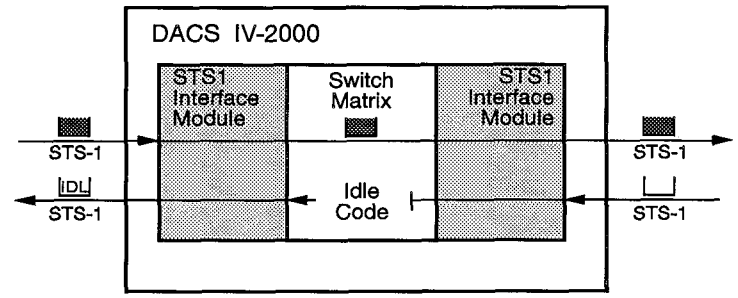

**C. Bridged Cross-Connection**

Figure 2-6. **DS3 Cross Connections**

## STS-1 Cross-Connections

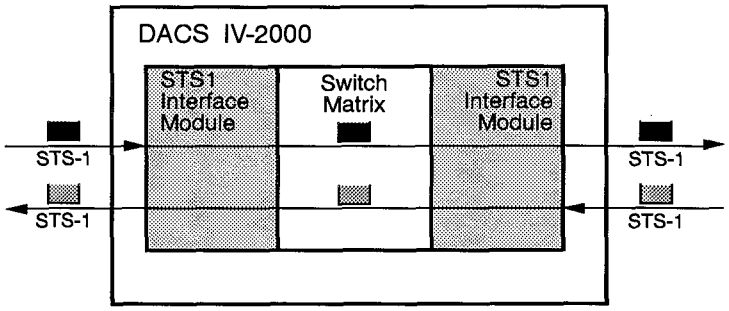
The DACS IV-2000 switch network can cross-connect up to 240 STS-1 signals from terminating EC-1 facilities and/or network elements. The DACS IV-2000 can cross-connect an STS-1 signal on any incoming STS1 port to any outgoing STS1 port. Three types of STS-1 cross-connections are possible with the DACS IV-2000:

- Two-Point STS-1 Cross-Connection, One-way — Figure 2-7A shows a one-way STS-1 cross-connection of a two-point cross-connection. The corresponding STS-1 signal in the other direction can be independently cross-connected or terminated with no cross-connection, in which case an STS-1 path Alarm Indication Signal (AIS) is transmitted on the unused EC-1 facility.
- Two-Point STS-1 Cross-Connection, Two-way — Figure 2-7B shows a two-way STS-1 cross-connection of a two-point cross-connection. A single command can cross-connect both directions of an STS-1 signal on any incoming STS1 port to any outgoing STS1 port.
- Bridged STS-1 Cross-Connection — Figure 2-7C illustrates how the DACS IV-2000 can bridge any existing STS-1 connection by cross-connecting the STS1 input port of the existing connection to a second STS1 output port without affecting service in the existing path. This feature allows for EC-1 facility rolling.

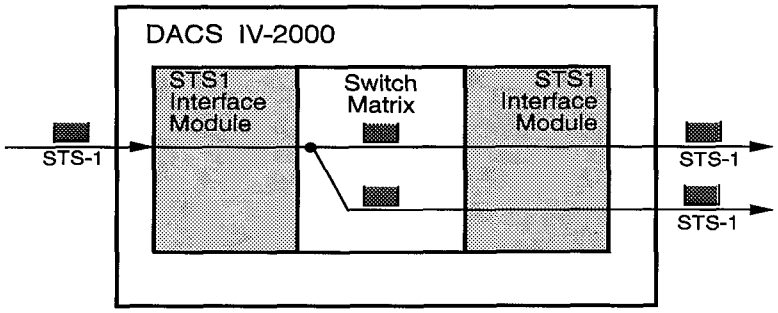



Notes:
IDL = STS-1 Path AIS
⊣ = Termination

**A. Two-Point, One-Way**




**B. Two-Point, Two-Way**



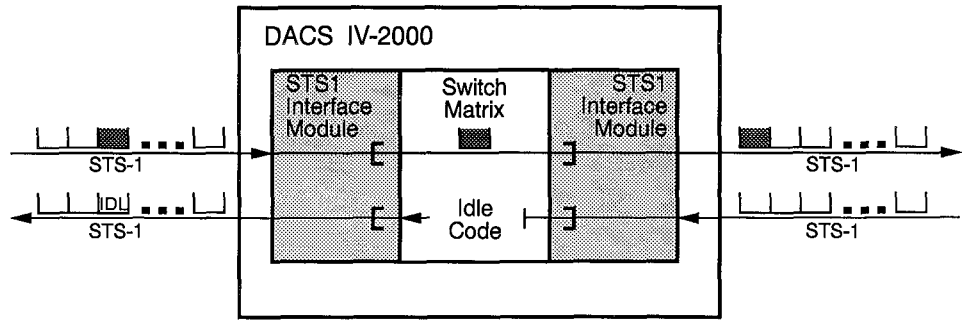

**C. Bridged Cross-Connection**

Figure 2-7. **STS-1 Cross Connections**

## VT1.5 Cross-Connections

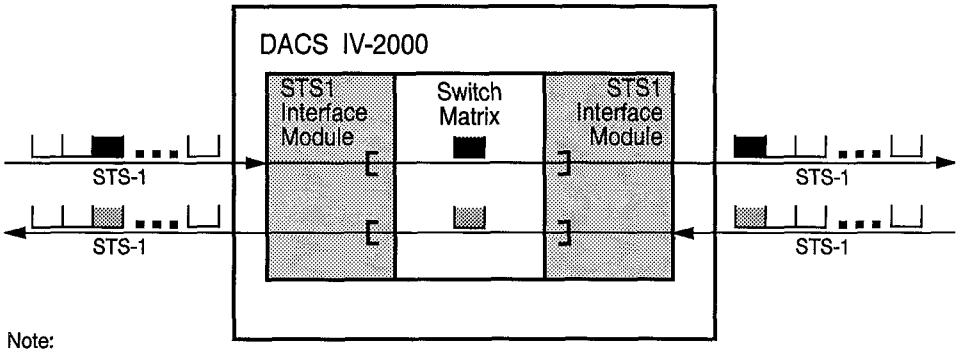
The DACS IV-2000 switch network can cross-connect up to 6720 VT1.5 one-way signals (240 equivalent STS-1signals) from terminating EC-1 facilities and/or network elements. The DACS IV-2000 can cross-connect a VT1.5 signal on any incoming STS1 port to any outgoing STS1 port. Three types of VT1.5 cross-connections are possible:

- Two-Point VT1.5 Cross-Connection, One-way — Figure 2-8A shows a one-way VT1.5 cross-connection of a two-point cross-connection. The corresponding VT1.5 signal in the other direction can be independently cross-connected or terminated with no cross-connection, in which case a VT path AIS is transmitted on the unused VT1.5 facility.
- Two-Point VT1.5 Cross-Connection, Two-way — Figure 2-8B shows a two-way VT1.5 cross-connection of a two-point cross-connection. A single command can cross-connect both directions of an VT1.5 signal on any incoming STS1 port to any outgoing STS1 port.
- Bridged VT1.5 Cross-Connection — Figure 2-8C shows how the DACS IV-2000 can bridge any existing VT1.5 connection by cross-connecting the VT1.5 input port of the existing connection to a second VT1.5 output port without affecting service in the existing path. This feature allows for VT1.5 facility rolling.



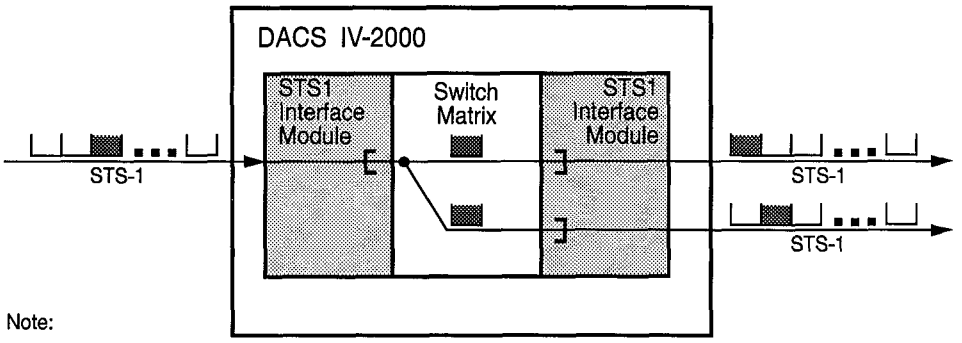

Notes:
IDL = VT Path AIS
⊣ = Termination
[ = MUX/DEMUX

**A. Two-Point, One-Way**




Note:
[ = MUX/DEMUX

**B. Two-Point, Two-Way**




Note:
[ = MUX/DEMUX

**C. Bridged Cross-Connection**

Figure 2-8. **VT1.5 Cross-Connection**

## DS1 and VT1.5 Mappings

The industry uses two methods to number DS1 signals within DS3 signals and VT1.5 signals within STS-1 signals. One method is to number the DS1/VT1.5 signals sequentially (1 through 28); this is known as the *sequential numbering method.* The second method is to use the combination of the VT1.5 group and the VT1.5 port; this is known as the *group/port numbering method.* The first column in Table 2-1 and in Table 2-2 shows the sequential numbering method; the next two columns show the group/port numbering method. In the two tables, notice that DS1s within DS3s and VT1.5s within STS-1s are mapped to different DS2/VT groups and DS1/VT1.5 ports. In Table 2-1, DS2 group 1 is associated with DS1 signals 1 through 4, while in Table 2-2, VT group 1 is associated with VT1.5 signals numbered 1, 8, 15, and 22.

**NOTE:**
The DS2 groupings in Table 2-1 are shown to illustrate the relationship among signal types. DS2 groups are not used in DACS IV-2000.

Network elements can use either numbering method. Up to Release 4.0, the DACS IV-2000 accepted only the sequential numbering method. The group/port numbering method is only used for VT1.5 or DS1 signals within VT1.5 signals. Beginning with Release 5.0, the DACS IV-2000 supports both the sequential numbering method and the group/port numbering method. Add-drop multiplexers (ADMs), which generally associate a single low-speed circuit pack with four ports with a VT group, use the VT group and VT1.5 port numbering method.

Before Release 5.0, when cross-connecting asynchronous and synchronous information from other network elements (such as the DDM-1000 or DDM-2000) that use the DS2/VT group and DS1/VT1.5 port numbering method, within the DACS IV-2000, the signal numbering methods for all network elements had to be taken into consideration when setting up the `ENT-CRS-T1` command. With Release 5.0, the `ENT-SECU-USR` and `ED-SECU-USR` commands enable the System Administrator to provision the way signals are mapped on a user-by-user basis. Refer to the *DACS IV-2000 (512) Release 5.0 Commands and Messages* manual (AT&T 365-340-902).

In the sequential numbering method, signals are identified using a unit-slot-port format (for example, 25-12-8). In the group/port numbering method, signals are identified using a unit-slot-group-port format. (For example, 25-12-1-2.)

The following examples show how the numbering of signals is maintained for three different types of cross-connections through the DACS IV-2000:

- Example 1 shows an *asynchronous-to-asynchronous* (asynchronous) environment where the DACS IV-2000 receives a DS3 signal from one DDM-1000, cross-connects a DS1 signal within that DS3 to a DS1 signal within another DS3, and transmits the new DS3 signal to a second DDM-1000.

  Since only asynchronous network elements are used, only the sequential numbering method can be used.

- Example 2 shows an *asynchronous-to-synchronous* (asynchronous gateway) environment where the DACS IV-2000 receives a DS3 signal from a DDM-1000, cross-connects a DS1 signal within that DS3 to a VT1.5(DS1) signal within an STS-1, and transmits that STS-1 signal to a DDM-2000.

  Since both asynchronous and synchronous network elements are used, both the sequential numbering method and group/port numbering method can be used.

- Example 3 shows a *synchronous-to-synchronous* (SONET) environment where the DACS IV-2000 receives an STS-1 signal from one DDM-2000, cross-connects a VT1.5(DS1) signal within that STS-1 to a VT1.5(DS1) signal within another STS-1, and transmits the new STS-1 signal to a second DDM-2000.

  Since only synchronous network elements are used, both the sequential numbering method and group/port numbering method can be used.

In the examples, the DSX-1 panels are used to show how the numbering of DS1 and VT1.5 signals corresponds when looking at both ends of the signal path. The same locations at the DSX-1 panels are used for each example. Note that the `ENT-CRS-T1` command differs depending on the cross-connection type used (asynchronous, asynchronous gateway, or SONET).

Note that the mapping is performed either internally by the DACS IV-2000 (sequential numbering method) or externally by the user (group/port numbering method).

Table 2-3 summarizes the DS1 and VT1.5 mappings used in the examples.

Table 2-1. DS1 Signal Numbering Within DS3 Signals

| DS1s Within DS3 | DS2 Group | DS1 Port Within DS2 Group | DS1s Within DS3 | DS2 Group | DS1 Port Within DS2 Group |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 17 | 5 | 1 |
| 2 | | 2 | 18 | | 2 |
| 3 | | 3 | 19 | | 3 |
| 4 | | 4 | 20 | | 4 |
| 5 | 2 | 1 | 21 | 6 | 1 |
| 6 | | 2 | 22 | | 2 |
| 7 | | 3 | 23 | | 3 |
| 8 | | 4 | 24 | | 4 |
| 9 | 3 | 1 | 25 | 7 | 1 |
| 10 | | 2 | 26 | | 2 |
| 11 | | 3 | 27 | | 3 |
| 12 | | 4 | 28 | | 4 |
| 13 | 4 | 1 | | | |
| 14 | | 2 | | | |
| 15 | | 3 | | | |
| 16 | | 4 | | | |

Table 2-2. VT1.5 Signal Numbering Within STS-1 Signals

| VT1.5 Within STS-1 | VT Group | VT1.5 Port Within VT Group | VT1.5 Within STS-1 | VT Group | VT1.5 Port Within VT Group |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 15 | 1 | 3 |
| 2 | 2 | 1 | 16 | 2 | 3 |
| 3 | 3 | 1 | 17 | 3 | 3 |
| 4 | 4 | 1 | 18 | 4 | 3 |
| 5 | 5 | 1 | 19 | 5 | 3 |
| 6 | 6 | 1 | 20 | 6 | 3 |
| 7 | 7 | 1 | 21 | 7 | 3 |
| 8 | 1 | 2 | 22 | 1 | 4 |
| 9 | 2 | 2 | 23 | 2 | 4 |
| 10 | 3 | 2 | 24 | 3 | 4 |
| 11 | 4 | 2 | 25 | 4 | 4 |
| 12 | 5 | 2 | 26 | 5 | 4 |
| 13 | 6 | 2 | 27 | 6 | 4 |
| 14 | 7 | 2 | 28 | 7 | 4 |

Table 2-3. **Summary of DS1 and VT1.5 Mappings Between DACS IV-2000 and DDM-1000/2000**

| Asynchronous DACS IV-2000 to DDM-1000 | | Synchronous | | | |
|---|---|---|---|---|---|
| | | DACS IV-2000 | | DDM-2000 | |
| DS1s Within DS3 | DS2,DS1 | VT1.5s Within STS-1 | VT Group, VT | VT Group, VT | VT1.5s Within STS-1 |
| 1 | 1,1 | 1 | 1,1 | 1,1 | 1 |
| 2 | 1,2 | 2 | 2,1 | 1,2 | 8 |
| 3 | 1,3 | 3 | 3,1 | 1,3 | 15 |
| 4 | 1,4 | 4 | 4,1 | 1,4 | 22 |
| 5 | 2,1 | 5 | 5,1 | 2,1 | 2 |
| 6 | 2,2 | 6 | 6,1 | 2,2 | 9 |
| 7 | 2,3 | 7 | 7,1 | 2,3 | 16 |
| 8 | 2,4 | 8 | 1,2 | 2,4 | 23 |
| 9 | 3,1 | 9 | 2,2 | 3,1 | 3 |
| 10 | 3,2 | 10 | 3,2 | 3,2 | 10 |
| 11 | 3,3 | 11 | 4,2 | 3,3 | 17 |
| 12 | 3,4 | 12 | 5,2 | 3,4 | 24 |
| 13 | 4,1 | 13 | 6,2 | 4,1 | 4 |
| 14 | 4,2 | 14 | 7,2 | 4,2 | 11 |
| 15 | 4,3 | 15 | 1,3 | 4,3 | 18 |
| 16 | 4,4 | 16 | 2,3 | 4,4 | 25 |
| 17 | 5,1 | 17 | 3,3 | 5,1 | 5 |
| 18 | 5,2 | 18 | 4,3 | 5,2 | 12 |
| 19 | 5,3 | 19 | 5,3 | 5,3 | 19 |
| 20 | 5,4 | 20 | 6,3 | 5,4 | 26 |
| 21 | 6,1 | 21 | 7,3 | 6,1 | 6 |
| 22 | 6,2 | 22 | 1,4 | 6,2 | 13 |
| 23 | 6,3 | 23 | 2,4 | 6,3 | 20 |
| 24 | 6,4 | 24 | 3,4 | 6,4 | 27 |
| 25 | 7,1 | 25 | 4,4 | 7,1 | 7 |
| 26 | 7,2 | 26 | 5,4 | 7,2 | 14 |
| 27 | 7,3 | 27 | 6,4 | 7,3 | 21 |
| 28 | 7,4 | 28 | 7,4 | 7,4 | 28 |

**EXAMPLE 1: Asynchronous-to-Asynchronous Mapping**

An example of asynchronous-to-asynchronous mapping is shown in Figure 2-9, where a DACS IV-2000 is used to cross-connect a DS1 signal within a DS3 signal between two DDM-1000 ADMs that accept DS1 signals from a DSX-1 panel.

- The DS1 signal labeled 7 (or DS1 port 3 of DS2 group 2 on the DSX-1 on the FROM side) is transmitted to the DS1 signal labeled 26 (or DS1 port 2 of DS2 group 7 on the DSX-1) on the TO side.
- The DDM-1000 on the FROM side accepts the DS1 signal on slot 2, port 3 (the mapping is the same as the DS2 group, DS1 port numbering). Using Table 2-3 column 2 for the value 2, 3 of DS2,DS1, the DS1 port from the DSX-1 maps into DS1 7 within the DS3 that is sent to the DACS IV-2000. The DACS IV-2000 cross-connects DS1 7 of the DS3 entering at MUX-17-1 to DS1 26 of the DS1 exiting at MUX-21-1 with the `ENT-CRS-T1::17-1-7,21-1-26;` command.
- The DS3 signal is sent to the DDM-1000 on the TO side, where DS1 26 is mapped to slot 7, port 2. Using column 1 of Table 2-3, the value 26 maps to the value 7,2 in column 2.
- Finally, the DS1 signal is accessed at the DSX-1 on the TO side as DS1 26 (or DS1 port 2 of DS2 group 7).

In this example, the DACS IV-2000 cross-connected the two asynchronous DS1 signals from the DSX-1 panels on a one-for-one basis; that is, DS1 7 on the FROM side is cross-connected to DS1 26 on the TO side.

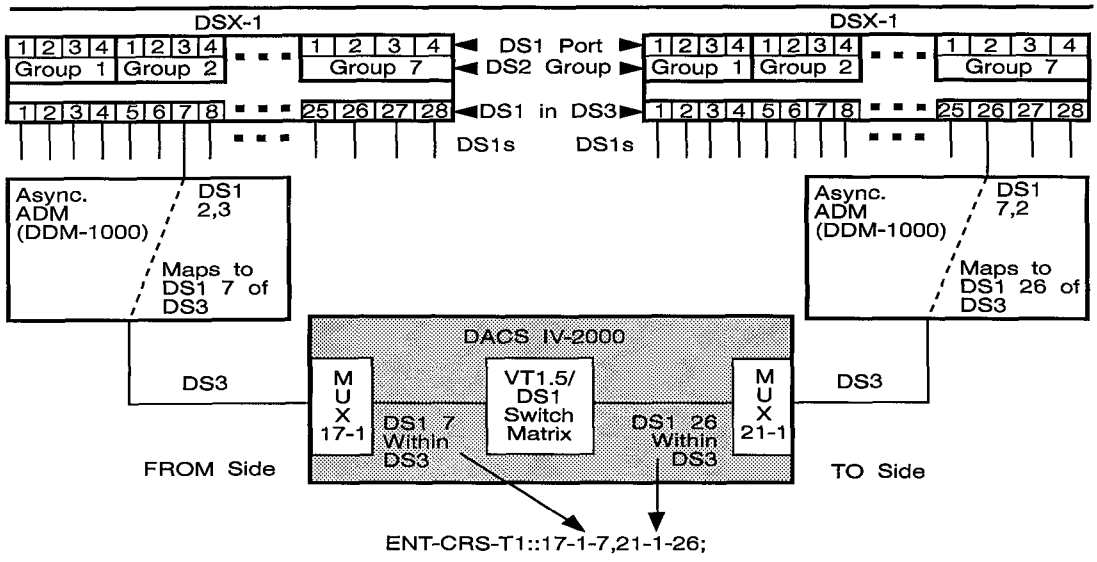



Figure 2-9. **Asynchronous-to-Asynchronous Cross-Connection — TO/FROM Port Identification**

**EXAMPLE 2: Asynchronous-to-Synchronous Mapping**

In Figure 2-10, a DACS IV-2000 is used to cross-connect a DS1 signal within a DS3 signal from an asynchronous ADM (DDM-1000) to a synchronous ADM (DDM-2000) via a VT1.5 signal within an STS-1 signal.

- The DS1 signal labeled 7 (or DS1 port 3 of DS2 group 2 on the DSX-1) on the FROM side is transmitted to the DS1 signal labeled 26 (or DS1 port 2 of DS2 group 7 on the DSX-1) on the TO side.
- The DDM-1000 on the FROM side accepts the DS1 signal on slot 2, port 3. Using Table 2-3 column 2 for the value 2,3 of DS2,DS1, the DS1 port from the DSX-1 maps into DS1 7 within the DS3 that is sent to the DACS IV-2000.
- Using the sequential numbering method, since the VT1.5 signal transmitted to the DDM-2000 on the TO side is mapped differently from the DS1 signal on the FROM side, using Table 2-3 column 5 for the value 7,2 (the DS1 signal at the DSX-1 on the TO side), the DACS IV-2000 must cross-connect the VT1.5 signal that to port 14.
- Using the group/port numbering method, since the TO side is synchronous, 7,2 can be used as the address (no mapping is required).

Therefore (assuming that the DS3 enters the DACS IV-2000 at MUX-17-1 and the STS-1 exits at SMUX-22-1 and assuming that the user is using the sequential numbering method), the `ENT-CRS-T1::17-1-7,22-1-14;` command is used to cross-connect the DS1 at the DSX-1 on the FROM side to the DS1 at the DSX-1 at the TO side. If the group/port numbering method were used, the command would be `ENT-CRS-T1::17-1-7,22-1-7-2.`

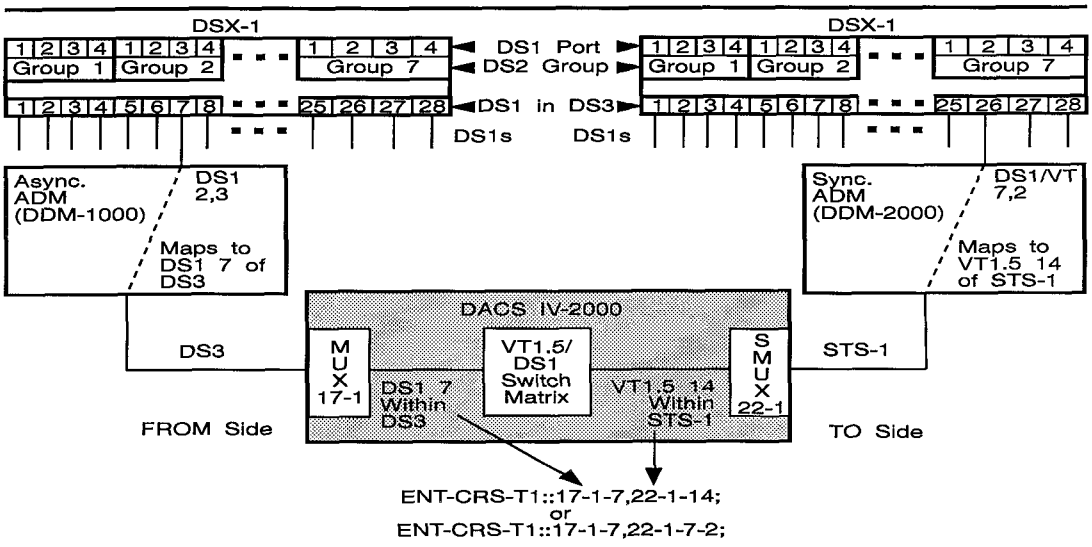



Figure 2-10. **Asynchronous-to-Synchronous Cross-Connection — TO/FROM Port Identification**

**EXAMPLE 3: Synchronous-to-Synchronous Mapping**

In Figure 2-11, a DS1 signal from one DSX-1 is received by another DSX-1 that is transmitted to/from a DACS IV-2000 as a VT1.5 within an STS-1 signal through two synchronous ADMs (DDM-2000s).

- The DS1 signal labeled 7 (or DS1 port 3 of DS2 group 2 on the DSX-1) on the FROM side is transmitted to the DS1 signal labeled 26 (or DS1 port 2 of DS2 group 7 on the DSX-1) on the TO side.

The following two steps assume that you are using the sequential numbering method.

- The DDM-2000 on the FROM side accepts the DS1 signal on slot 2, port 3. Since the DDM-2000 maps this DS1 into a VT1.5 signal, to determine the mapping, use column 5 of Table 2-3. The value 2,3 (VT group, VT) maps to VT1.5 16. Therefore, the DS1 from the DSX-1 on the FROM side is transmitted to the DACS IV-2000 as VT1.5 16 within the STS-1 received at SMUX-18-1.
- The VT1.5 signal transmitted to the DDM-2000 on the TO side is mapped using Table 2-3, column 5, for the value 7,2 (the DS1 signal at the DSX-1 on the TO side). Using SMUX-22-1 as the port the STS-1 is transmitted from, the DACS IV-2000 must cross-connect to VT1.5 14 of the STS-1 signal.

The following step assumes that you are using the sequential numbering method.

- Because the TO and FROM sides are both synchronous, you may specify 7,2 as the destination. (Mapping is done automatically.)

Therefore, assuming that the user is using the sequential numbering method, the `ENT-CRS-T1::18-1-16,22-1-14;` command is used to cross-connect the DS1 at the DSX-1 on the FROM side to the DS1 at the DSX-1 at the TO side. If the group/port numbering method were used, the command would be `ENT-CRS-T1::18-1-2-3,22-1-7-2.`

In this example, both VT1.5 signals at the DACS IV-2000 are mapped as different numbers than the DS1 signals in the first example.

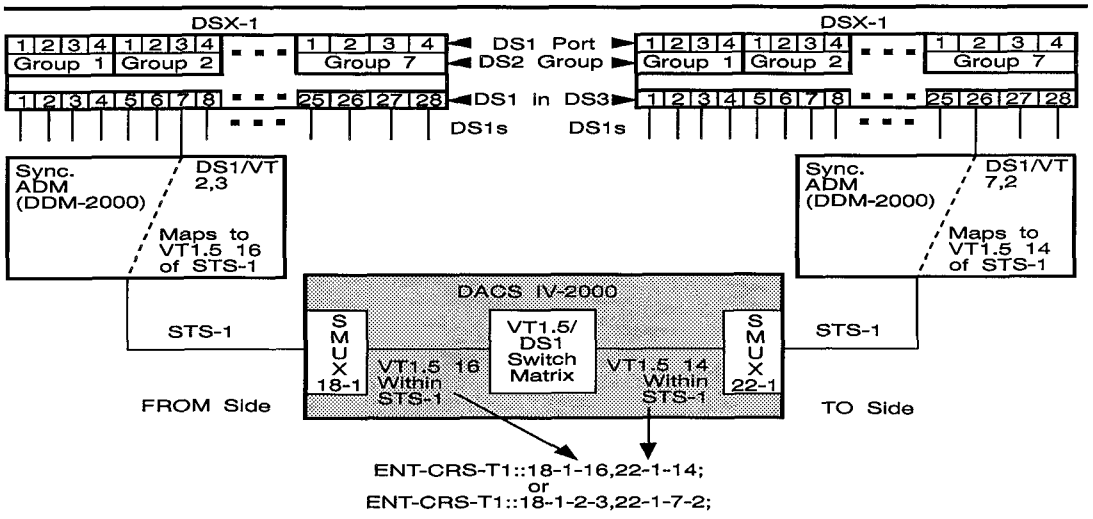



Figure 2-11. **Synchronous-to-Synchronous Cross-Connection — TO/FROM Port Identification**

## Special Service (Redlined) Connections

Circuits that are sensitive or require special care when changing or deleting (such as 911) should be made as special service connections to prevent inadvertent changes in status. When entering cross-connections (one-way, two-way, or bridging), the connections can be specified as a special service (redlined) connections.

Connections specified as special service can only be deleted or modified if they are identified as special service connections using the RDLD value in the Special Service Type parameter, or the YES value in the inclusive parameter.

## Bridging and Rolling

To bridge a facility is to add a connection to an existing connection in less than 1 second for DS1 and VT1.5 signals, and in less than 1 second for STS-1/DS3 signal.

To roll a facility is to break an existing connection while simultaneously establishing a new connection in less than 3 ms.

## Bridging

The DACS IV-2000 can bridge DS1 connections by cross-connecting the DS1 input port of any connection to any DS1 output port on a DS1, DS3, or EC-1 facility without affecting service in the existing path.

The DACS IV-2000 can bridge any VT1.5 connection by cross-connecting the VT1.5 input port to a VT1.5 output port without affecting service in the existing path. This feature allows for VT1.5 facility rolling.

The DACS IV-2000 can bridge any STS-1 connection by cross-connecting an STS1 input port to an STS1 output port without affecting service in the existing path.

The DACS IV-2000 can bridge DS3 connections by cross-connecting the DS3 input port of any connection to any DS3 output port on a DS3 of an EC-1 facility. without affecting service in the existing path. Bridging and one-way and two-way rolling is supported for DS3 signals interfacing to the MUX3 circuit pack when it is provisioned to support DS3 clear-channel cross-connections and DS3 to STS-1 cross-connections.

## Rolling

The DACS IV-2000 supports one-way rolls (each direction of transmission rolled separately) and two-way rolls (both directions rolled together).

### DS1/DS3/STS-1/VT1.5 Facility Roll

The roll feature (rerouting) allows you to reroute a facility from an existing path to a new path in service. This feature is useful for in-service rerouting of traffic to new systems. Rerouting can be temporary or permanent and can be between one-way or two-way cross-connections. Also, this feature can be used to roll service from one central office to another central office.

The following facilities can be rerouted:

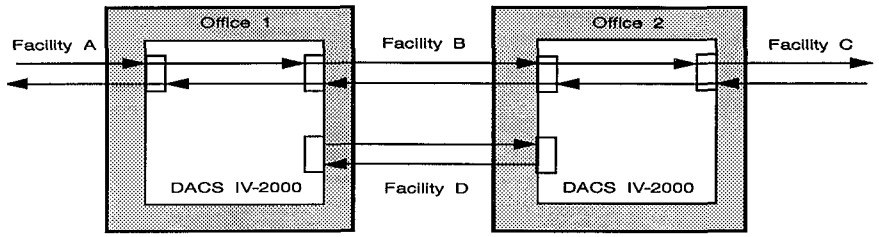
- A DS1 facility
- DS1 tributaries within DS3 facilities or EC-1 facilities
- All 28 DS1 tributaries of a DS3 facility (DS3 rerouting)
- EC-1 facilities and VT1.5 tributaries within EC-1 facilities
- DS3 facilities within a MUX3 circuit pack.

The following two examples show how the roll feature can be used. The first example shows the rerouting of one facility to another facility between two central offices. The second example shows the rerouting of service to a common central office from two other central offices.

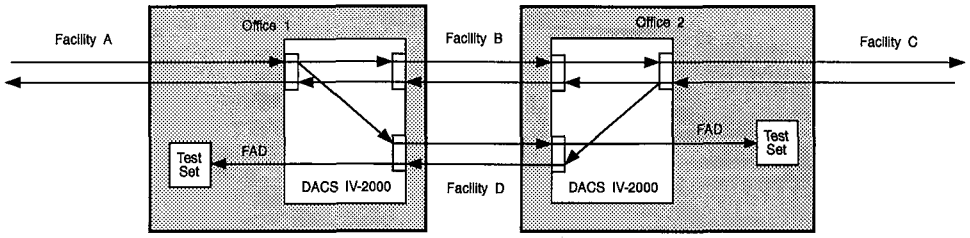
**EXAMPLE 1:**

Figure 2-12 shows how a facility is rerouted to another facility between two central offices. Rerouting of one facility to another facility involves coordination between two DACS IV-2000s as follows:

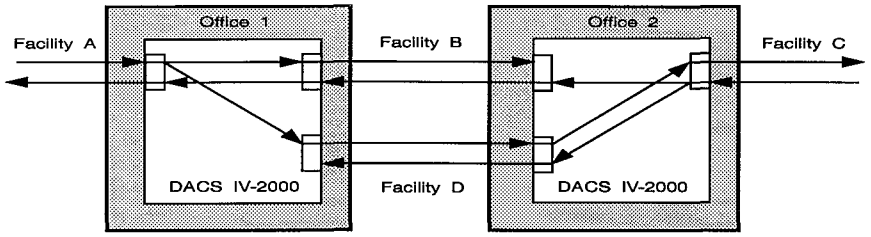
- In Figure 2-12A, Facility B is the original path between offices 1 and 2.
- In Figure 2-12B, a bridge cross-connection is established over Facility D from Office 1 to Office 2 and from Office 2 to Office 1. Test access can be performed to ensure that the signal over Facility D is being transmitted and received.
- In Figure 2-12C, after service over Facility D is tested, service is rolled in Office 2 from Facility B to Facility D.
- In Figure 2-12D, service is rolled in Office 1 from Facility B to Facility D.
- In Figure 2-12E, Facility B is taken out of service using `DLT-CONF` commands.



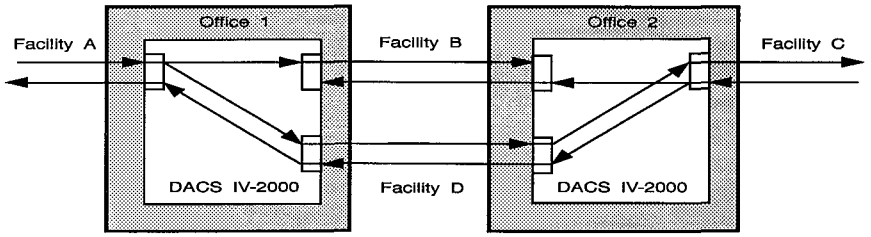

A. Existing Cross-Connections Over Original Facility



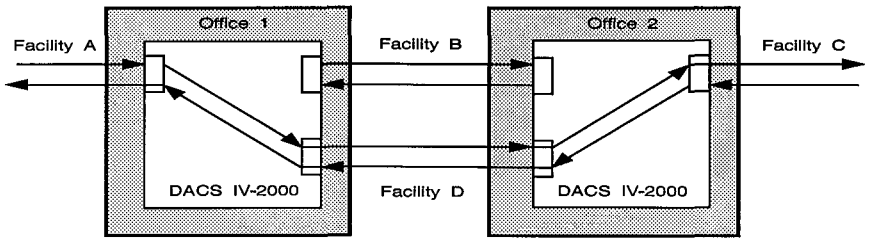

B. Establishing Bridge Connection and Testing New Facility (Test Access)




C. Rolling Service Through Office 2 on New Facility)




D. Rolling Service Through Office 1 on New Facility



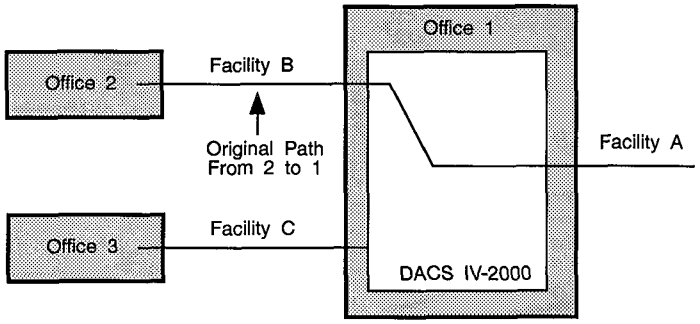

E. Taking Old Facility Out of Service (DLT-CONF Commands)

Figure 2-12. **Facility Roll Between DACS IV-2000 Systems**

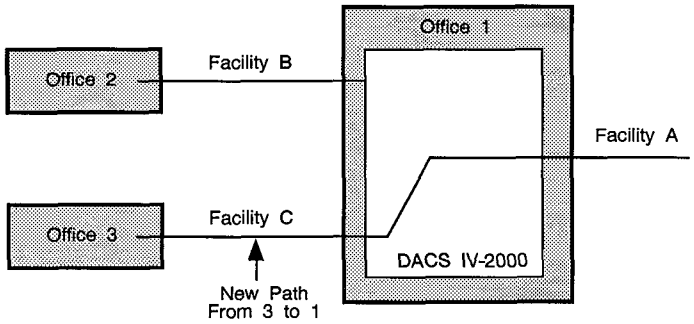
**EXAMPLE 2:**

Figure 2-13 shows how a facility is rerouted from one central office to another central office, with the new facility going to the same central office as the original facility. Rerouting of a facility in this manner involves the use of the ENT-ROLL command as follows:

- In Figure 2-13A, Facility B is the original transmission path between offices 1 and 2.
- Service is rolled (rerouted) from Office 3 through Facility C by entering the ENT-ROLL command on the DACS IV-2000 in Office 1 by using the port connected to Office 3 as the NEWFROM port (Figure 2-13B).




**A. Existing Cross-Connection Between Two Central Offices**




**B. Rolling (Rerouting) Service From New Central Office With ENT-ROLL Command**

Figure 2-13. **Facility Roll Through One DACS IV-2000**

## Loopbacks

The DACS IV-2000 provides DS1, DS3, STS-1, and VT1.5 loopback features that facilitate testing and trouble isolation.

The wideband loopback feature provides a loopback for VT1.5s within incoming STS-1 signals to be looped back through the switch (on a per-tributary basis) to the outgoing STS-1 of the same STS-1 signal. The STS-1 line loopback feature allows for connections of incoming STS-1 signals to the output direction, and maintains all incoming signal code and format violations and timing. Both loopback features are performed without changing any bits in the looped-back signal.

### DS1 Loopbacks

DS1 loopbacks (see Figure 2-14) can be operated on a specified DS1 port or range of DS1 ports, either towards the facility, towards the switch, or through the switch matrix of a DS1 Interface Module, a DS3 Interface Module, or a VT1.5 (DS1) tributary of an STS-1 signal within the system.

DS1 loopbacks can be one of the following four types:

- Line Loopback (LPBKL): The signal from the input port is looped to the output port (towards the facility) at the DS1 Interface Module.
- Terminal Loopback (LPBKT): The signal from the input port is looped to the output port through the switch matrix in the Switch Module. DS1 terminal loopbacks are valid for DS1IF1, MUX1, MUX2, MUX3, or SMUX1 circuit packs.
- Internal Loopback (LPBKI): The signal from the output port is looped to the input port (towards the switch) at the DS1 Interface Module.
- Tributary Loopback (LPBKM): A DS1 tributary signal within a MUX2 or MUX3 circuit pack is looped from the input port to the output port (toward the facility) at the DS3 Interface Module. DS1 tributary loopbacks are valid for either near-end or far-end on MUX2 or MUX3 circuit packs only.

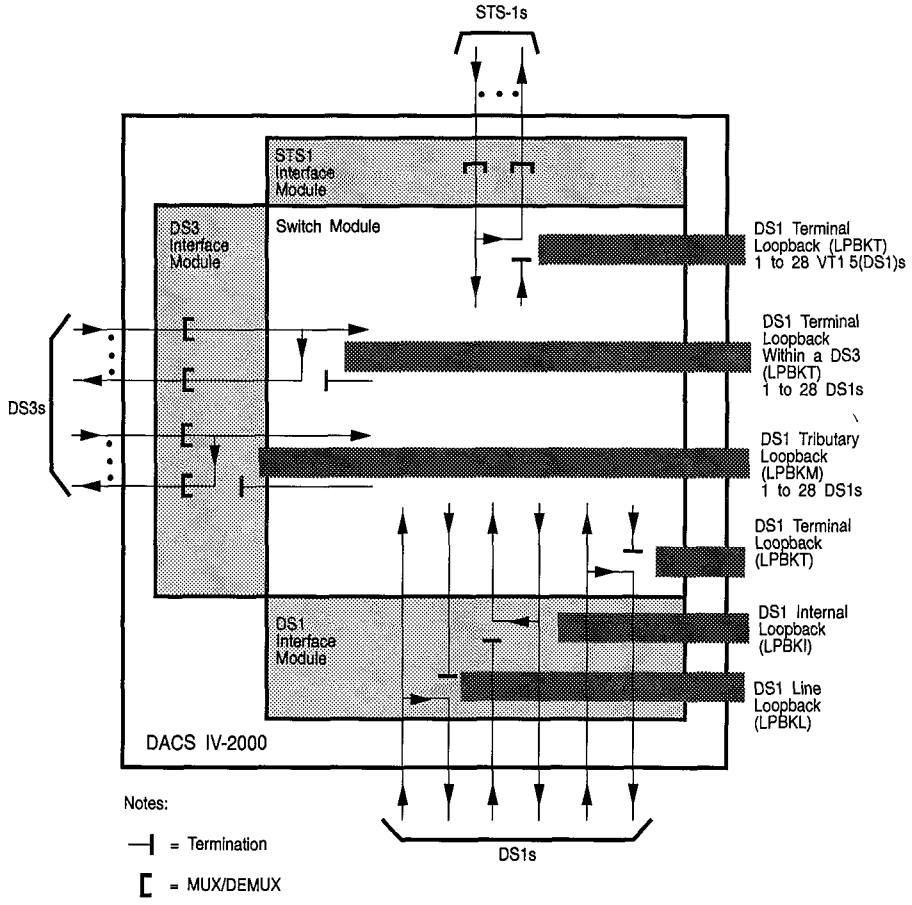



Figure 2-14. **DS1 Loopbacks**

## DS3 Loopbacks

DS3 loopbacks (see Figure 2-15) can be one of the following:

- Line Loopback (LPBKL): The MUX2 and MUX3 circuit packs can retransmit an incoming signal back to the output. The DS3 line loopback is supported in both clear-channel and DS1 modes for MUX3 circuit packs. The DS3 line loopback regenerates the signal to conform to the standard pulse shape and voltage. The entire DS3 bit stream is looped back without modification, and bipolar violations in the incoming signal are preserved at the output. (DS3 line loopbacks can be operated on an incoming DS3 signal directly to the outgoing direction of the same port. This loopback happens directly in the MUX2 or MUX3 circuit pack and keeps the signal from entering the switch matrix; it thus keeps the amount of hardware encountered to a minimum.)
- Terminal Loopback (LPBKT) — MUX3 circuit packs only: When provisioned for clear-channel mode, the MUX3 circuit pack also supports DS3 terminal loopbacks in which the incoming signal is bridged in the switch matrix to go to both the original cross-connection output port and the output port associated with the same input port (that is, on the same MUX3). Bipolar violations are not preserved for terminal loopbacks.

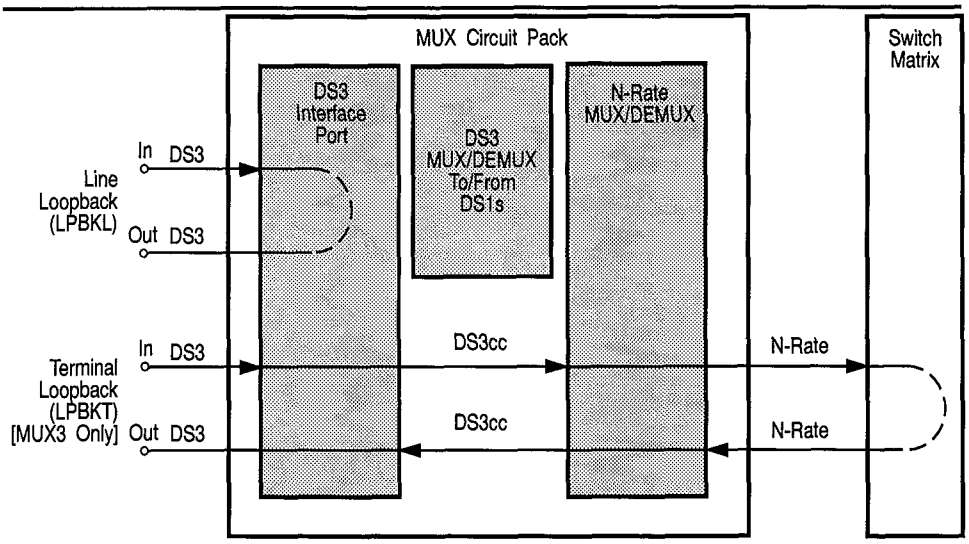



Figure 2-15. DS3 Loopbacks

## STS-1 Loopbacks

STS-1 loopbacks (Figure 2-16) can be operated on a specified STS1 port or range of STS1 ports, either towards the facility or through the switch matrix of an STS1 Interface Module. STS-1 loopbacks can be one of the following types:

- Line Loopback (LPBKL) — loops the signal from the input port to the output port (towards the facility) at the STS1 Interface Module.
- Terminal Loopback (LPBKT) — loops the signal from the input port to the output port through the switch matrix in the Switch Module. STS-1 terminal loopbacks are valid for the near end on SMUX circuit packs.

The STS-1 loopback feature is performed without changing any bits in the looped-back signal.

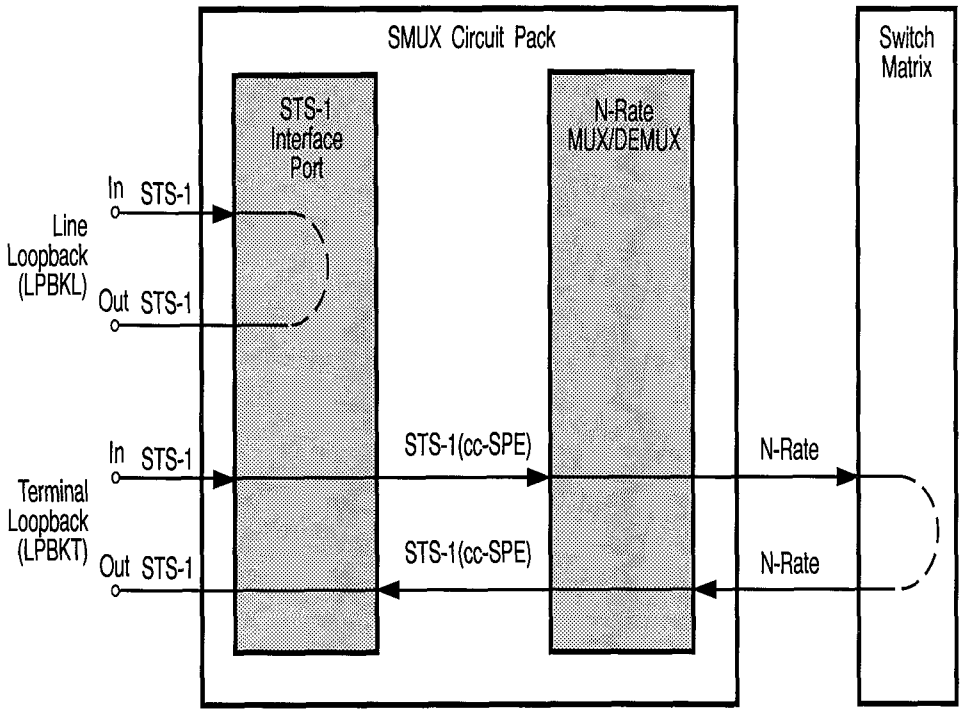



Figure 2-16. **STS-1 Loopbacks**

## VT1.5 Loopbacks

The VT1.5 loopback feature (Figure 2-17) allows VT1.5s within incoming STS-1 signals to be looped back through the switch (on a per-tributary basis) to the outgoing STS-1 of the same STS-1 signal.

VT1.5 loopbacks can be operated on a specified VT tributary of an STS-1 signal as a terminal loopback (LPBKT), which loops the VT1.5 signal from the input port to the output port through the switch matrix in the Switch Module.

The VT1.5 loopback features is performed without changing any bits in the looped-back signal.

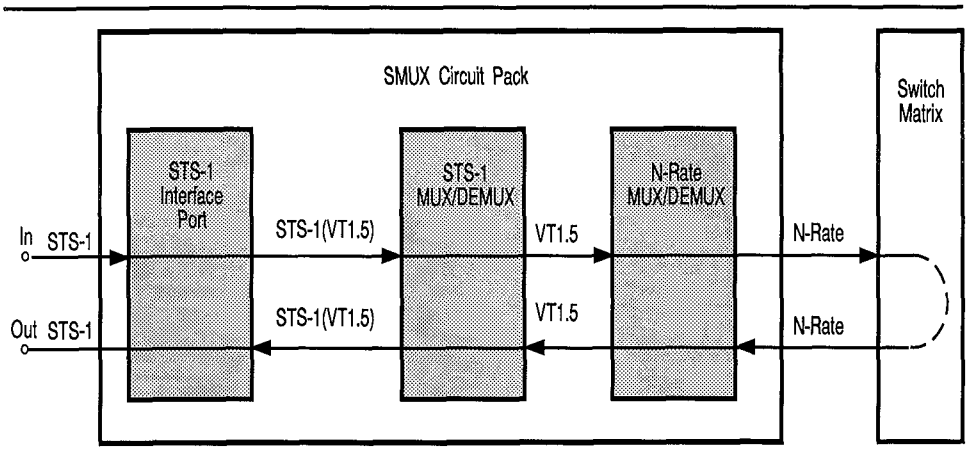



Figure 2-17. **VT1.5 Terminal Loopback**

## Test Access

The ability to supply and monitor DS1, DS3, VT1.5, and STS-1 test signals, split connections, and perform loopbacks can simplify facility turnup and assist in trouble isolation.

The DACS IV-2000 supports all the DS1, VT1.5, and STS-1 test access modes specified in Bellcore TR-NWT-000818, per ANSI T1.403. The test access modes supported are MONE, MONF, SPLTA, SPLTB, SPLTE, SPLTF, LOOPE, LOOPF, MONEF, and SPLTEF. With these capabilities, the system can act as a digital test access unit (DTAU). In addition, the DACS IV-2000 supports test access for DS3 signals interfacing to the MUX3 circuit pack when it is provisioned to support DS3 clear-channel cross-connections and DS3-to-STS-1 cross-connections.

VT1.5 and STS-1 test access connections are accessed via the SONET interface. Individual VT1.5 tributaries must be accessed externally from an STS-1, for which test access is provided.

Any MUX3 circuit pack port that is not being used to carry traffic can be provisioned as a DS3 test access port.

Figure 2-18 shows the test-access naming conventions. The E-End and F-End are arbitrarily designated for a one-way or a two-way cross-connection.[1] For example, the E-End can be designated to correspond to a short-haul transmission path to equipment (such as a DACS III-2000) within the same Central Office; the F-End can be designated to correspond to a long-haul transmission path to another Central Office. The E-End and F-End signals are terminated at DS1, DS3, or STS-1 Interface Modules.

Test access can be established at either the E-End or the F-End through a test-access port (TAP).

The signal path through the frame from the E-End to the F-End is referred to as the A direction, and the signal path from the F-End to the E-End is the B direction. In a one-way cross-connection, the signal travels in the A direction. The In and Out designations indicate the direction to/from the E-End and F-End. After selecting designations of E-End and F-End, these designations must not change during the test-access session.

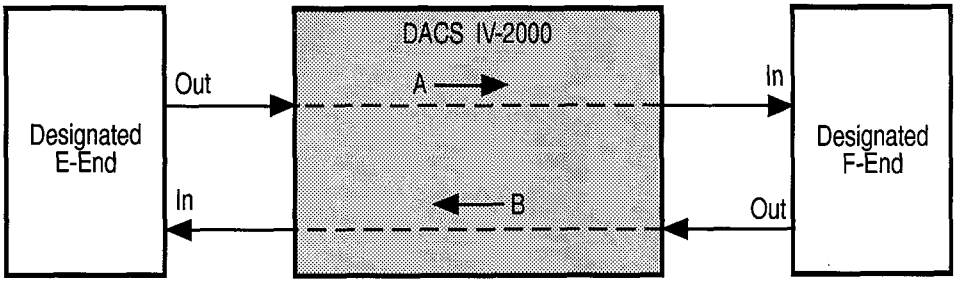



Figure 2-18. **Test Access Conventions**

Ten modes of test access are supported in the DACS IV-2000:

- MONE — The MONE mode of test access monitors the output of the E-End of an idle port, a one-way cross-connection, or a two-way cross-connection. It reads the incoming signal to the DACS IV-2000 in direction A.
- MONF — The MONF mode of test access monitors the output of the F-END of a two-way cross-connection. It reads the incoming signal to the DACS IV-2000 in direction B.

1. Traditionally E-End and F-End mean equipment end and facility end, respectively. However you can designate any port as E-End or F-End.

- MONEF — The MONEF mode of test access monitors both directions of a two-way cross-connection. This mode of test access requires two TAPs. It reads the incoming signals to the DACS IV-2000 (the output from the E-End and F-End) in directions A and B.
- SPLTA — The SPLTA mode of test access splits the E-End (to TAP) to F-End (from TAP) connection of a one-way or two-way cross-connection to allow testing in the A direction.
- SPLTB — The SPLTB mode of test access splits the F-End (to TAP) to E-End (from TAP) connection of a two-way cross-connection to allow testing in the B direction.
- SPLTE — The SPLTE mode of test access splits the E-End to F-End of a one-way or two-way cross-connection to allow testing at the E-End. The incoming signal to the DACS IV-2000 in the A direction goes to the input of the TAP, and the output of the TAP is sent in the B direction.
- SPLTF — The SPLTF mode of test access splits the F-End to E-End of a two-way cross-connection to allow testing at the F-End. The incoming signal to the DACS IV-2000 in the B direction goes to the input of the TAP, and the output of the TAP is sent in the A direction.
- SPLTEF — The SPLTEF mode of test access splits both directions of a two-way cross-connection to allow testing at both the E-End and the F-End. This mode of test access requires two TAPs. The incoming signal to the DACS IV-2000 in the A direction goes to the input of TAP-1, and the output of TAP-1 is sent in the B direction. The incoming signal to the DACS IV-2000 in the B direction goes to the input of TAP-2, and the output of TAP-2 is sent in the A direction.
- LOOPE — The LOOPE mode of test access establishes a terminal loopback on the E-End port and monitors the loopback signal. It reads the incoming signal to the DACS IV-2000 (output from the E-End) in the A direction.
- LOOPF — The LOOPF mode of test access establishes a terminal loopback on the F-End port and monitors the loopback signal. It reads the incoming signal to the DACS IV-2000 (output from the F-End) in the B direction.

In Figures 2-19 through 2-28, three types of lines are used to illustrate the different connections. They are:

- Solid Line — represents the test access path up on the tested cross-connection
- Dotted Line — represents the continuation of an active cross-connection
- Dashed Line — represents one leg of a two-way cross-connection. If only a one-way cross-connection is active, the connection shown by the dashed line does not exist.

## Monitor Test Access

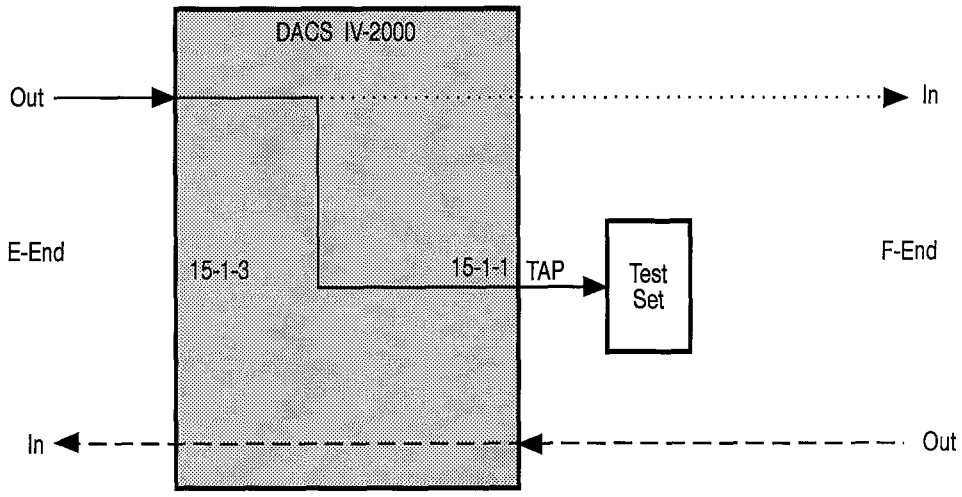
When creating DS1 monitor test-access connections, DS1 ports selected for E-End, F-End, and TAP can be on a DS1, DS3, or STS1 interface circuit pack. When creating VT1.5 and STS-1 monitor test-access connections, VT1.5 and STS1 ports can only be on STS1 interface circuit packs (SMUX).

When creating DS3 monitor test-access connections, DS3 ports selected for E-End, F-End, and TAP must be on a DS3CC interface circuit pack.

### MONE Mode

The MONE mode of test access monitors the E-End of an idle port, a one-way cross-connection, or a two-way cross-connection. It reads the incoming signal in direction A.

In Figure 2-19, a monitor test-access connection is established from a testport located at port 1 of DS1GRP-15-1 to an idle port located at port 3 of DS1GRP-15-1. If the E-End is idle, the connections shown by the dotted and dashed lines are not present. If a one-way cross-connection exists from the E-End to the F-End, the connection shown by the dashed line is not present.



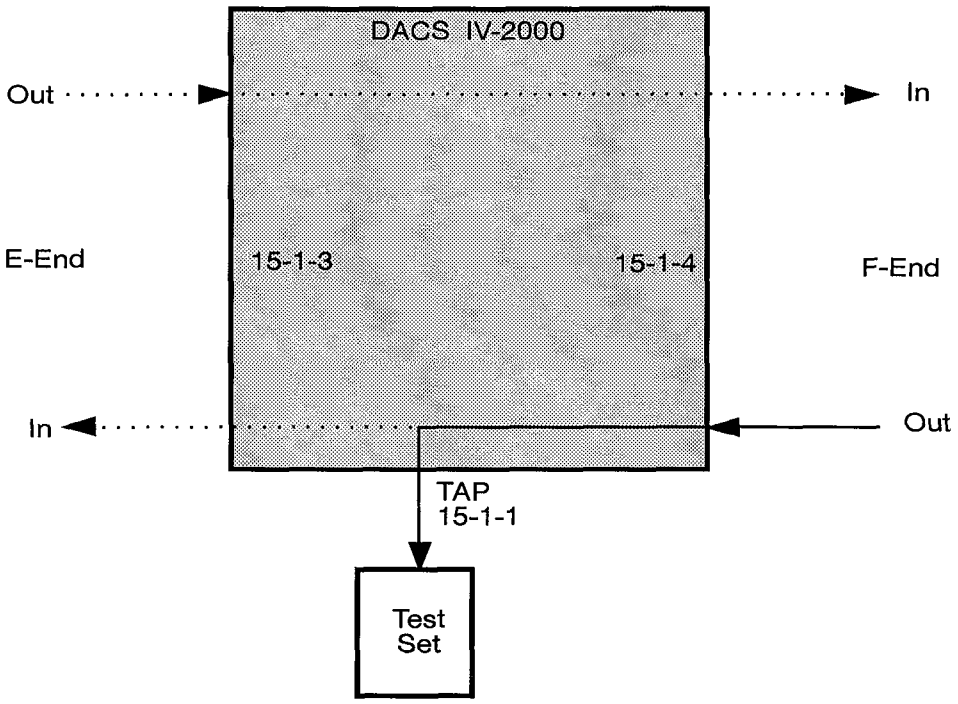

```
CONN-TACC-T1::15-1-1,15-1-3,:::MONE;
```

Figure 2-19. **MONE Mode of Test Access**

### MONF Mode

The MONF mode of test access monitors the F-End of a two-way cross-connection. It reads the incoming signal in direction B.

In Figure 2-20, a monitor test-access connection is established on the F-End of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport.



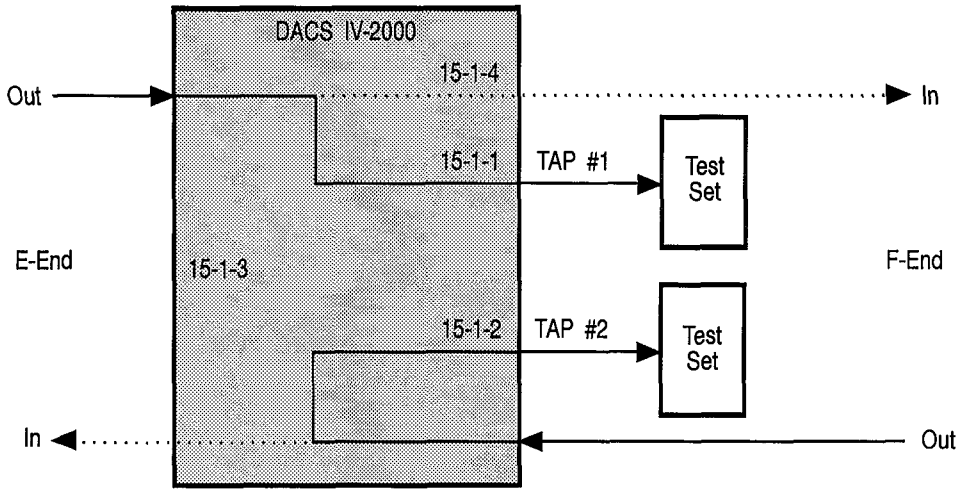

```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::MONF;
```

Figure 2-20. MONF Mode of Test Access

## MONEF Mode

The MONEF mode of test access monitors both directions of a two-way cross-connection. This mode of test access requires two TAPs. It reads the incoming signals in directions A and B.

In Figure 2-21, a monitor test-access connection is established on both the E-End and the F-End of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Ports 1 and 2 of DS1GRP-15-1 as the testport. Only the odd-numbered port of the testport pair is specified in the test-access command and the MONEF mode of test access can only be established on a two-way cross-connection.




```
CONN-TACC-1::15-1-1,15-1-3,15-1-4:::MONEF;
```

Figure 2-21. **MONEF Mode of Test Access**

## Split Test Access

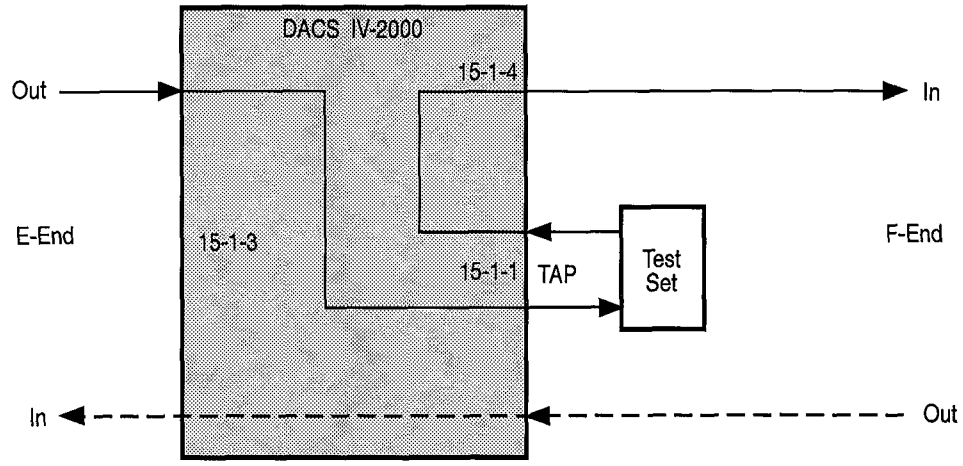
When creating DS1 split test-access connections, DS1 ports selected for E-End, F-End, and TAP can be on a DS1, DS3, or STS1 interface circuit pack. When creating VT1.5 and STS-1 split test-access connections, VT1.5 and STS1 ports can only be on STS1 interface circuit packs (SMUXs).

When creating DS3 split test-access connections, DS3 ports selected for E-End, F-End, and TAP must be on a DS3CC interface circuit pack.

### SPLTA Mode

The SPLTA mode of test access splits the E-End (to TAP) to F-End (from TAP) connection of a one-way or two-way cross-connection to allow testing in the A direction.

In Figure 2-22, a split test-access connection is established in the A direction on a one-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. On a one-way cross-connection from the E-End to the F-End, the connection shown by the dashed line is not present.



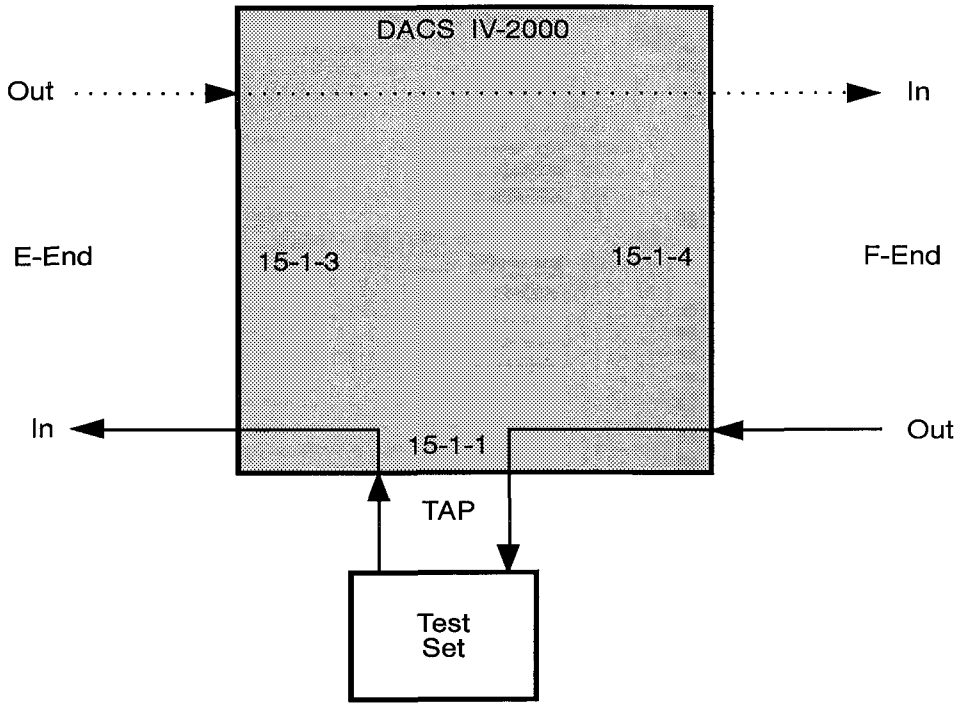

```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTA;
```

Figure 2-22. **SPLTA Mode of Test Access**

### SPLTB Mode

The SPLTB mode of test access splits the F-End (to TAP) to E-End (from TAP) connection of a two-way cross-connection to allow testing in the B direction.

In Figure 2-23, a split test-access connection is established in the B direction on a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport.



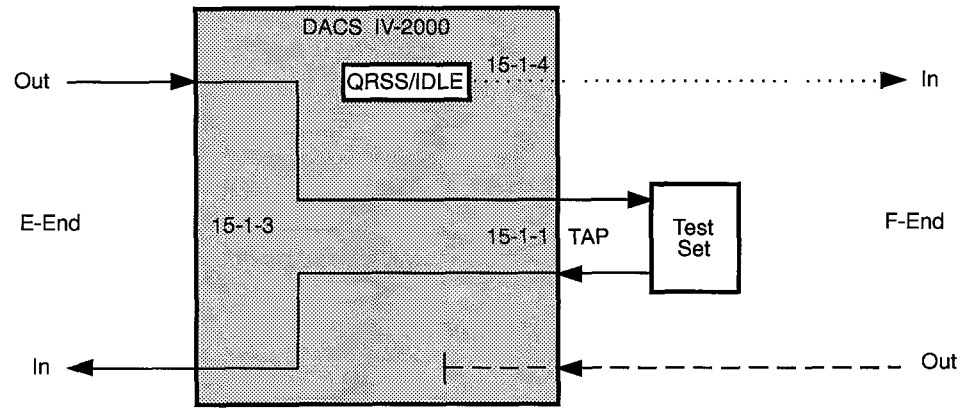

```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTB;
```

Figure 2-23. **SPLTB Mode of Test Access**

### SPLTE Mode

The SPLTE mode of test access splits the E-End to F-End of an idle port, a one-way cross-connection, or a two-way cross-connection to allow testing at the E-End. The incoming signal in the A direction goes to the input of the TAP, and the output of the TAP is sent in the B direction.

In Figure 2-24, a split test-access connection is established at the E-End of a one-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a Quasi-Random Signal Source (QRSS) or IDLE signal is sent to the F-End output port and to any other ports tied to the E-End input port. For a two-way cross-connection, the F-End input port is disconnected from the E-End output port during the test session. If a bridge is tied to the F-End input port, it is not affected. If the E-End port is idle, the signal paths represented by the dotted and dashed lines are not present. If a one-way cross-connection exists from the E-End to the F-End, the signal path represented by the dashed line is not present.




```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTE;
```

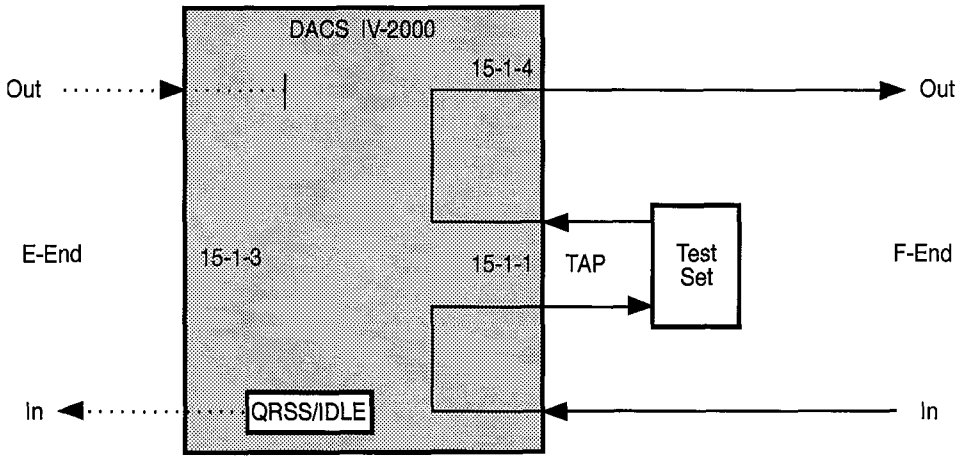
Figure 2-24. **SPLTE Mode of Test Access**

For DS1 SPLTE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5, STS-1, and DS3 SPLTE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

### SPLTF Mode

The SPLTF mode of test access splits the F-End to E-End of a two-way cross-connection to allow testing at the F-End. The incoming signal in the B direction goes to the input of the TAP and the output of the TAP is sent in the A direction.

In Figure 2-25, a split test-access connection is established at the F-End of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1 GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a QRSS or IDLE signal is sent to the E-End output port and to any other ports tied to the F-End input port unless the F-End port is idle. The E-End input port is disconnected from the F-End output port during the test session. If a bridge is tied to the E-End input port, it is not affected.




```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTF;
```

Figure 2-25. **SPLTF Mode of Test Access**

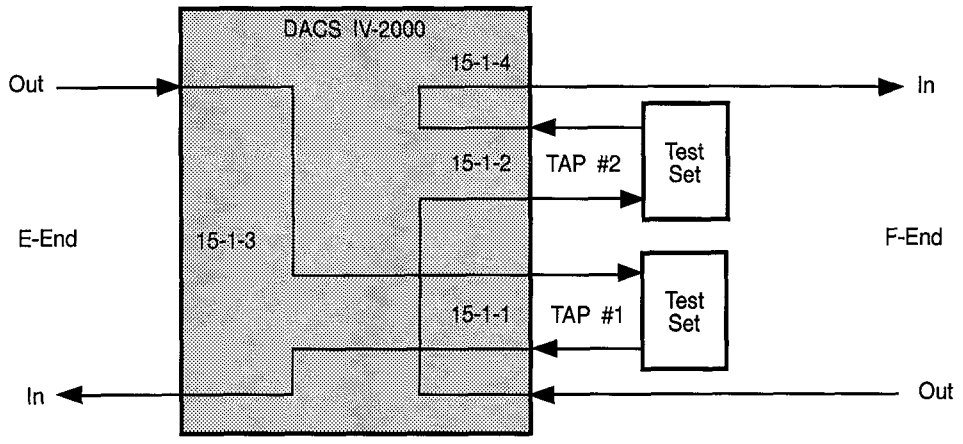
For DS1 SPLTF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5, STS-1, and DS3 SPLTF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

### SPLTEF Mode

The SPLTEF mode of test access splits both directions of a two-way cross-connection to allow testing at both the E-End and the F-End. This mode of test access requires two TAPs. The incoming signal in the A direction goes to the input of TAP-1 and the output of TAP-1 is sent in the B direction. The incoming signal in the B direction goes to the input of TAP-2 and the output of TAP-2 is sent in the A direction.

In Figure 2-26, a split test-access connection is established on both the E-End and the F-End of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Ports 1 and 2 of DS1GRP-15-1 as the testports.

Only the odd-numbered port of the testport pair is specified in the test-access command. The SPLTEF mode of test access can only be established on a two-way cross-connection.




```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::SPLTEF;
```

Figure 2-26. SPLTEF Mode of Test Access

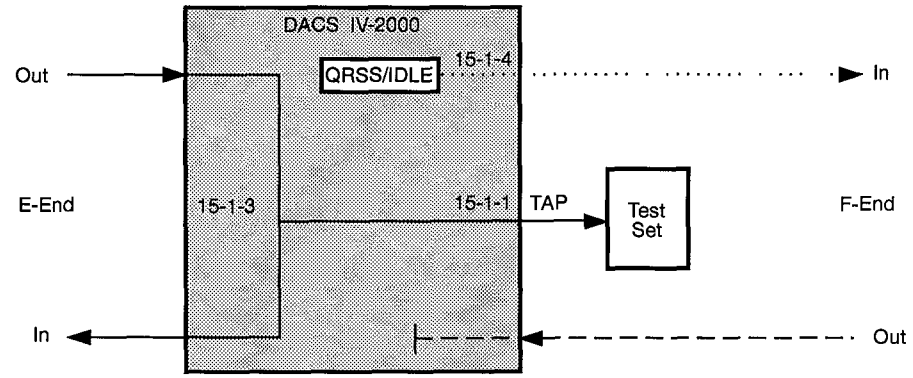
## Loopback Test Access

When creating DS1 loopback test-access connections, DS1 ports selected for E-End, F-End, and TAP can be on a DS1, DS3, or STS1 interface circuit pack. When creating VT1.5 and STS-1 loopback test-access connections, VT1.5 and STS1 ports can only be on STS1 interface circuit packs (SMUX). When creating DS3 loopback test-access connections, DS3 ports selected for E-End, F-End, and TAP must be on a DS3CC interface circuit pack.

### LOOPE Mode

The LOOPE mode of test access establishes a terminal loopback on the E-End port and monitors the loopback signal. It reads the incoming signal in the A direction.

In Figure 2-27, a loopback test-access connection is established on a one-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a QRSS or IDLE signal is sent to the F-End output port The LOOPE mode can be established on either a one-way or a two-way cross-connection. For a two-way cross-connection, the F-End input port is disconnected from the E-End output port during the test session. If a bridge is tied to the F-End input port, it is not affected. If the E-End port is idle, the dotted and dashed connections are not present. If a one-way cross-connection exists from the E-End to the F-End, the signal path represented by the dashed line is not present.




```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::LOOPE;
```

Figure 2-27. **LOOPE Mode of Test Access**

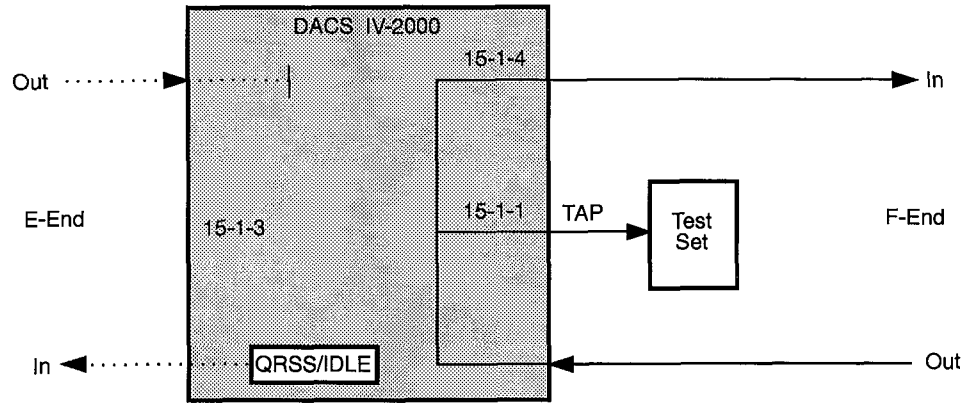
For DS1 LOOPE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5,

STS-1, and DS3 LOOPE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

### LOOPF Mode

The LOOPF mode of test access establishes a terminal loopback on the F-End port and monitors the loopback signal. It reads the incoming signal in the B direction.

In Figure 2-28, a loopback test-access connection is established on a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a QRSS or IDLE signal is sent to the E-End output port. The E-End input port is disconnected from the F-End output port during the test session. If a bridge is tied to the F-End input port, it is not affected.




```
CONN-TACC-T1::15-1-1,15-1-3,15-1-4:::LOOPF;
```

Figure 2-28. **LOOPF Mode of Test Access**

For DS1 LOOPF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5, STS-1, and DS3 LOOPF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

## Performance Monitoring

This section describes STS-1, VT1.5, DS1, and DS3 performance monitoring. The DACS IV-2000 provides DS1 and DS3 performance monitoring in accordance with Bellcore TR-TSY-000820. The DACS IV-2000 supports measurement and reporting of VT1.5 and STS-1 signal degradations in accordance with draft copies of the ANSI T1M1.3 standards. The following paragraphs provide a description of the performance-monitoring features.

**NOTE:**
DS1 far-end performance monitoring per AT&T TR-54016 is not supported in this release.

### DS1 Performance Monitoring

The DS1 performance monitoring feature allows the DACS IV-2000 to monitor the health of DS1 facilities by collecting performance data for those facilities. The incoming DS1 facilities are continuously monitored in the full-time dedicated mode. Dedicated full-time performance monitoring is provided for those DS1 facilities that pass through a SW1F2 or a MUX3 circuit pack. The MUX3 supports dedicated full-time monitoring of DS1 tributaries within the DS3 signals; MUX1 and MUX2 circuit packs do not.

The parameters that are monitored and measured to determine the health of a facility depend on the framing format and the performance monitoring option. The parameters that are monitored and measured also depend on whether near-end (monitored directly by the DACS IV-2000) or far-end (as updated by the upstream NTE) performance monitoring data are requested.

#### Framing Format

Framing format may be extended superframe, superframe, or unframed.

- Extended Superframe (ESF) provides path performance monitoring using cyclic redundancy code (CRC) error checking to monitor the health of the incoming DS1 signal path. The CRC code checks for errors in all the bits of the DS1 signal. ESF format also provides a 4-kb/s data link for communication between network elements connecting the DS1 facility, which can be used to send Performance Report Messages as required by the ANSI T1.403 standard.
- Superframe (SF) provides path performance monitoring using DS1 signal framing bits.

- Unframed (UNF) provides line performance monitoring for all DS1 signal formats coded with alternate mark inversion (AMI) or bipolar with 8-zero substitution (B8ZS). Line performance monitoring is performed using bipolar violation counts to monitor the received signal on the facility; this excludes the bipolar violations that are part of the B8ZS code.

## Performance Monitoring Options

Performance monitoring option may be dedicated full-time, camp-on full-time, or scanned.

### Dedicated Full-Time Monitoring

In the dedicated full-time mode, the health of the DS1 facilities is continuously monitored. Full-time performance monitoring is provided for those DS1 facilities that pass through a SWIF2 or a MUX3 circuit pack. The MUX3 circuit pack supports full-time monitoring of DS1s within the incoming DS3 signals that are either SF or ESF format; MUX1 and MUX2 circuit packs do not.

When using the full-time monitoring option, the software monitors the health of incoming DS1 facilities continuously. It supports both DS1s that terminate on DS1IF circuit packs and DS1 tributaries within a DS3. All 28 of the DS1s associated with the MUX3 circuit pack or any of the 28 DS1s associated with the SWIF2 circuit pack can be provisioned for dedicated full-time performance monitoring. Dedicated full-time monitoring does not reduce the capacity of the DACS IV-2000.

### Camp-on Full-Time Monitoring

The camp-on full-time monitoring option allows the DACS IV-2000 to monitor a specified DS1 or group of DS1s. The system provides two camp-on monitoring options: manual and automatic.

- Manual — Selected ports have a bridge of a DS1 signal passing through a SWIF1 (DS1 Interface Modules), MUX1, or MUX2 (DS3 Interface-16 or DS3 Interface-32 Modules) circuit pack to a port on a PMGR circuit pack established using a command. This type of monitoring is not allowed for facilities terminating on MUX3 or SWIF2 circuit packs. Camp-on full-time monitoring continuously checks the health of DS1 tributaries within DS3 Interface or SMUX Modules as well as DS1 facilities terminating on a DS1 interface (DS1IF). To monitor the DS1s within VT1.5 signals, the signals must be cross-connected through the switch matrix at the DS1 rate. The DACS IV-2000 monitors these signals by bridging the DS1s to a PMGR circuit pack. Using a PMGR circuit pack reduces the cross-connection capacity of the DACS IV-2000 by one DS3 equivalent.
- Automatic — Occurs when the performance monitoring scanning option detects that a DS1 port has degraded service; that port is automatically connected to an available designated automatic camp-on port.

### Scanned Mode Monitoring

The DACS IV-2000 provides scanned monitoring for those DS1 signals that do not need to be monitored on a full-time basis. This option is ideal for checking general network and facility performance health. You can also use scanned monitoring when you require more cost-effective performance monitoring measures. With this method, one PMGR circuit pack can monitor up to 420 DS1 signals whereas one PMGR can monitor only a maximum of 28 DS1 signals when operating in the camp-on mode.

Scanned performance monitoring is not available for DS1 signals within VT1.5 signals or DS1 tributaries of DS3 signals in Enhanced DS3 or DS3 Clear-Channel Interface-16 Modules.

Scanned monitoring is accomplished by bridging 28 DS1 signals to the PMGR circuit pack. In the scanned option, up to 15 selected DS1 signals are monitored by a single port of the PMGR circuit pack in sequential order.

One scanning cycle for each group takes approximately 60 seconds, with about 50 seconds of that cycle actively monitoring the DS1 ports. If the maximum of 15 groups are monitored, then the time to revisit and rescan a DS1 group is 15 minutes. If only five are monitored, then the rescan cycle is five minutes. In the scan mode, all 420 DS1 signals associated with a particular pair of SWIO circuit packs can be sequentially monitored by the PMGR circuit pack, while only 28 DS1 signals of interface capacity are lost (a MUX or a SWIF circuit pack).

The PMGR circuit pack can occupy any MUX circuit pack slot (except the MUXP circuit pack slot) in the DS3 Interface-16 or DS3 Interface-32 Module and/or any SWIF circuit pack slot (except for the protection SWIF slot) in the DS1 Interface Module. When occupying a MUX circuit pack slot, the PMGR circuit pack has the ability to scan DS1 tributaries within a DS3 signal. One PMGR circuit pack can scan all the DS1 tributaries in a DS3 Interface-16 Module, while two PMGR circuit packs (one in the upper half of the module and the other in the lower half) are required in the DS3 Interface-32 Module. A PMGR circuit pack installed in a DS1 Interface Module (DS1 Interface or DS1 Interface-Protection) can scan all the DS1 signals in its module, as well as all the DS1 signals in the DS1 Interface Module (within a DS1 Interface Bay) associated with the SWIO circuit pack pair.

Scanned monitoring is available for ESF- and SF-framed DS1 tributaries within DS3 facilities as well as for similarly framed DS1 signals from DS1 facilities. Because the DACS IV-2000 monitors each DS1 signal for less than 100 percent of the time (varying with the number of DS1 groups scanned), it is not possible to gather as much detail about the DS1 performance as full-time monitoring. Scanned monitoring is not available for DS1 tributaries within EC-1 facilities. These signals must use manual camp-on monitoring.

### DS1 PM Mode Mixing

As described previously, the DACS IV-2000 provides three different DS1 performance-monitoring modes. These modes can be implemented independently or in unison. Any mix of modes can be in operation simultaneously, as dictated by the specific application.

Table 2-4 summarizes the DS1 performance-monitoring capabilities, the mixing and matching of modes, and the typical applications for each option. Restrictions to simplify administration of DS1 performance monitoring can be implemented. For example, full-time monitoring can be implemented for all incoming DS1 facilities and scanned monitoring for all DS1 tributaries of DS3 facilities. This is accomplished by using all SWIF2 circuit packs in the DS1 Interface Modules and by installing PMGR circuit packs in DS3 Interface Modules.

For hardware configuration information, including equipment constraints, refer to the section titled DS1 Performance Monitoring Hardware on page 6-59.

Table 2-4. **DS1 PM Summary**

| Monitoring Characteristics | Monitoring Mode | | |
|---|---|---|---|
| | **Dedicated Full-Time** | **Camp-on Full-Time** | **Scanned** |
| DS1 Signals Monitored | DS1 Facilities | DS1 Facilities<br>DS1s on DS3 Facilities<br>DS1s on EC-1 Facilities | DS1 Facilities<br>DS1s on DS3 Facilities, except ENH DS3 INTFC-16 or DS3CC |
| Parameters Measured | See Table 2-5 | See Table 2-5 | See Table 2-5 |
| Formats Monitored | ESF, SF, and unframed | ESF and SF | ESF and SF |
| Monitoring Coverage | ■ 28 DS1s associated with a SWIF2<br>■ 28 DS1 tributaries of MUX3 DS3 signal | Any ESF-or SF-framed DS1s in the system except those using the dedicated monitoring method | Any ESF- or SF-framed DS1s associated with a PMGR (up to 420 DS1s) except for those using the dedicated monitoring method and those in ENH DS3 INTFC-16 or DS3CC modules. |
| Implementation | ■ SWIF2s monitor 28 assigned DS1s<br>■ Any mix of SWIF and SWIF2 circuit packs allowed in DS1 Interface Module<br>■ MUX3s monitor all 28 tributaries of DS3 signal<br>■ MUX3s allowed in ENH DS3 INTFC -16 or DS3 CC INTFC-16 Modules | ■ PMGR occupies SWIF slot in DS1 Interface Module and/or MUX slot in DS3 Interface Module<br>■ PMGR can monitor any set of DS1s [from any interface module(s)] with any mix of full-time and camp-on<br>■ Any number of PMGRs allowed<br>■ Frame capacity reduced by 28 DS1s per PMGR | ■ DS1 Interface Module<br>— PMGR occupies SWIF slot<br>— 1 PMGR per pair of interface modules (SWIO pair)<br>■ DS3 Interface Module<br>— PMGR occupies MUX slot<br>— 1 PMGR per DS3 Interface-16 module<br>— 2 PMGRs per DS3 Interface-32 Module (1 in upper half and 1 in lower half)<br>■ Frame capacity reduced by 28 DS1s per PMGR |
| Typical Applications | ■ Full-time monitoring of all or large fraction of DS1 facilities | ■ Full-time monitoring of selected DS1s<br>■ Camp-on monitoring of selected DS1s to provide detailed examination of DS1s suspected of being of degraded quality | ■ Monitor performance health of any DS1s that do not require full-time monitoring |

## Monitored Parameters

**NOTE:**
DS1 far-end performance monitoring per AT&T TR-54016 is not supported in this release.

The DACS IV-2000 monitors and reports both path and line performance parameters to verify that service-quality objectives specified in terms of these parameters are being met. Performance monitoring only occurs during available time because service-quality assessments cannot be determined during a period of service outage. From a service perspective, two important criteria must be verified:

- Availability of service, which is measured by the parameter UAS (Unavailable Seconds)
- Quality of service during available time, which is measured by the other performance-monitoring parameters.

In addition to the path and line parameters that are monitored and reported, the DACS IV-2000 can detect incoming trouble condition indicators on SF- and ESF-formatted DS1 signals.

### Near-End Path Parameters

Path performance-monitoring parameters apply only to ESF-formatted and SF-formatted signals. The path performance parameters are determined using the cyclic redundancy check (CRC-6) codes in the ESF format or using framing bit errors (FBE) in the SF format. These near-end path parameters are collected independent of whether the far-end is supporting ANSI T1.403 or AT&T TR-54016. The path parameters are listed below:

- Path Code Violation (CVP) — A count of CRC-6 violations in DS1 ESF- formatted signals or FBEs in DS1 SF formatted signals. A CRC-6 violation occurs when the received CRC-6 code is not identical to the locally calculated CRC-6 code. An FBE occurs when a frame bit error is received in the frame bit pattern of the SF formatted signal.
- Path Out-of-Frame Seconds (OOFS) — A count of out-of-frame (OOF) events occurring over the path. In measuring OOF events, an integration time of one second is used so that all the OOF events within that second are counted as one. An OOF event occurs when a density of two FBEs out of four consecutive frame bits are detected. An OOF defect is terminated when no FBEs occur within four or more consecutive frame bit positions.
- Path Errored Seconds (ESP) — A count of the seconds having at least one CVP or OOF (for ESF-formatted signals) or at least one FBE or OOF (for SF-formatted signals).

- Path Bursty Errored Seconds (BESP) — A count of one-second intervals with 2 to 319 CVPs and no OOFSs (for ESF-formatted signals) or one-second intervals with two to seven FBEs and no OOFSs (for SF-formatted signals). BESP is not monitored during scanned performance-monitoring mode.
- Path Severely Errored Seconds (SESP) — A count of one-second intervals with 320 or more CVPs or an OOF event (for ESF-formatted signals) or one-second intervals with eight or more FBEs or an OOFS (for SF-formatted signals).
- Severely Errored Frame Seconds (SEFS) — A count of one-second performance report message intervals received from the far-end, containing one or more Severely Errored Frame (SEF) events. An SEF event is the occurrence of two or more FBEs within a 0.75-ms window.
- Controlled Slipped Seconds (CSS) — A count of one-second performance report message intervals received from the far-end containing one or more controlled slip (CS) events. A CS is the replication or deletion of the 192 payload bits of a DS1 frame by a path terminating network element. A CS can be performed when a difference exists between the timing of a synchronous receiving terminal and the received signal intervals.
- Unavailable Seconds (UAS) — A period of unavailable time beginning when an SESP occurs within 10 seconds or when an alarm indicating signal (AIS), loss-of-signal (LOS), or loss-of-frame (LOF) trouble condition is declared. Once unavailable, and if no failure is present, the DS1 path becomes available at the onset of 10 contiguous seconds with no SESPs.

**Near-End Line Parameters**

DS1 line parameters only apply to DS1 signals that terminate on DS1 interface circuit packs in the DACS IV-2000. Line performance parameters are determined using bipolar violations. The line parameters are listed below:

- Line Code Violations (CVL) — are illegal bipolar violation (BPV) events. A BPV event for an AMI-coded DS1 signal is the occurrence of a pulse of the same polarity as the previous pulse. A BPV for a B8ZS-coded DS1 signal is the occurrence of a pulse of the same polarity as the previous pulse without being a part of the zero substitution code. This parameter is not monitored during an LOS condition. For unframed (UNF) DS1 signals interfacing with the DACS IV-2000, CVLs are used to determine the bit error rate (BER) of the incoming DS1 signal. Also, signals that are not being monitored by the full-time or camp-on mode have their BER thresholds estimated with CVL counting.
- Line Errored Seconds (ESL) — measures seconds during which at least one CVL has occurred.

- Line Severely Errored Seconds (SESL) — measures seconds with more than 1544 CVLs. This parameter is not monitored during a LOS condition. DS1 AIS is detected by a MUX3 circuit pack from the switch matrix when a DS3 LOS, LOF, or AIS occurs at the other end of a cross-connection.

**Far-End Path Parameters**

Far-end parameters are collected in the system by reading the Extended Superframe (ESF) data link. The ANSI T1.403 standard specifies that the equipment that terminates an ESF DS1 facility monitors the performance of the incoming signal and transmits a performance report to the far end once per second. The report contains performance data for each of the previous four 1-second intervals. The DACS IV-2000 is capable of reading this report and maintaining a database of the far-end performance data.

The parameters defined for near-end paths (except OOFS) are also available for far-end paths.

The far-end path parameters are listed below:

- Severely Errored Frame Seconds (SEFS) — A count of one-second performance report message intervals received from the far-end, containing one or more Severely Errored Frame (SEF) events. An SEF event is the occurrence of two or more FBEs within a 0.75-ms window.
- Controlled Slipped Seconds (CSS) — A count of one-second performance report message intervals received from the far-end containing one or more controlled slip (CS) events. A CS is the replication or deletion of the 192 payload bits of a DS1 frame by a path terminating network element. A CS can be performed when a difference exists between the timing of a synchronous receiving terminal and the received signal intervals.
- Path Code Violation (CVP) — A count of far-end CRC-6 violations occurring during a defined accumulation period. Since far-end CRC-6 errors occurring during each second are reported to the near-end (not as exact counts, but in form), the far-end CVP parameter is accumulated as one of six groups: G1 = 1 CVPs, G2 = 5 CVPs, G3 = 10 CVPs, G4 = 100 CVPs, G5 = 319 CVPs, and G6 = 333 CVPs.
- Path Errored Seconds (ESP) — A count of 1-second performance-report message intervals containing one or more CVP events, one or more SEF events, or one or more CS events.
- Path Severely Errored Seconds (SESP) — A count of 1-second performance-report message intervals containing 320 or more CVP events or one or more SEF events.
- Path Bursty Errored Seconds (BESP) — A count of 1-second-performance report message intervals containing between 2 and 319 CVP events and no SEF events. BESP is not monitored during scanned performance-monitoring mode.

- Unavailable Seconds (UAS) — A period of unavailable time beginning when 10 consecutive seconds with an SESP are occurring or when an alarm indicating signal (AIS), loss-of-signal (LOS), or loss-of-frame (LOF) trouble condition is declared. Once unavailable, and if no failure is present, the DS1 path becomes available at the onset of 10 contiguous seconds with no SESPs.

### Parameter Measurements

The DACS IV-2000 performance monitoring accumulates measurements for the parameters listed in Table 2-5. This table shows those parameters that are measured given the options of dedicated full-time, camp-on full-time, and scanned performance monitoring in conjunction with line format and location.

Table 2-5. **DS1 PM Parameters**

| Location | Monitored Parameter | Dedicated Full-Time | | | Camp-On Full-Time | | | Scanned | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | ESF | SF | UNF | ESF | SF | UNF | ESF | SF | UNF |
| Near-End | CVL | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| | ESL | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| | SESL | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| | CVP | ✓ | ✓ | - | ✓ | ✓ | - | ✓ | ✓ | - |
| | ESP | ✓ | ✓ | - | ✓ | ✓ | - | ✓ | ✓ | - |
| | BESP | ✓ | ✓ | - | ✓ | ✓ | - | - | - | - |
| | SESP | ✓ | ✓ | - | ✓ | ✓ | - | ✓ | ✓ | - |
| | OOFS | ✓ | ✓ | - | ✓ | ✓ | - | ✓ | ✓ | - |
| | UAS | ✓ | - | - | ✓ | - | - | - | - | - |
| | CSS* | ✓ | - | - | - | - | - | - | - | - |
| Far-End | SEFS | ✓ | - | - | ✓ | - | - | ✓ | - | - |
| | ESP | ✓ | - | - | ✓ | - | - | ✓ | - | - |
| | SESP | ✓ | - | - | ✓ | - | - | ✓ | - | - |
| | CVP | ✓ | - | - | ✓ | - | - | - | - | - |
| | BESP | ✓ | - | - | ✓ | - | - | - | - | - |
| | UAS | ✓ | - | - | ✓ | - | - | - | - | - |
| | CSS* | ✓ | - | - | - | - | - | - | - | - |

**Note:** ✓ Denotes parameter being monitored for the given performance-monitoring option and line format.

* This is SLS in previous releases.

Table 2-6 lists the default threshold levels for measured parameters in the dedicated full-time and camp-on performance-monitoring modes. Table 2-7 lists the default threshold levels for measured parameters in the scan performance-monitoring mode. Table 2-8 lists the range of threshold levels for measured parameters in the dedicated full-time and camp-on performance-monitoring modes. Table 2-9 lists the range of threshold levels for measured parameters in the scanned performance-monitoring mode. Threshold levels are given for both short-interval (15-minute and hourly) accumulated data and for daily accumulated data. As indicated, the line performance parameters (CVL, ESL, and SESL) are valid only for the DS1s that terminate on the DACS IV-2000 through a DS1 interface circuit pack.

Table 2-6. **Default Thresholds for Full-Time, Camp-On Full-Time, and Line DS1 Performance Monitoring Dedicated Full-Time/Camp-On Full-Time DS1 PM**

| Monitored Parameter | DS1 Framing Format | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Extended Superframe | | | | Superframe | | Unframed | |
| | Far-End* | | Near-End | | | | | |
| | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily |
| **Dedicated Full-Time (SWIF2 Based) and Camp-on Full-Time (PMGR Based)** | | | | | | | | |
| CVP | 53184 | 132960 | 53184 | 132960 | 6615 | 16540 | - | - |
| ESP | 259 | 648 | 259 | 648 | 38 | 95 | - | - |
| BESP | 100 | 600 | 100 | 600 | 19 | 90 | - | - |
| SESP | 40 | 100 | 40 | 100 | 11 | 27 | - | - |
| OOFS | - | - | 7 | 17 | 7 | 17 | - | - |
| UAS | 10 | 10 | 10 | 10 | 10 | 10 | - | - |
| SEFS | 7 | 17 | - | - | - | - | - | - |
| CSS‡ | 7 | 17 | 7 | 17 | - | - | - | - |
| **Line (DS1IF Based)** | | | | | | | | |
| CVL† | - | - | 53360 | 133400 | 53360 | 133400 | 53360 | 133400 |
| ESL† | - | - | 259 | 648 | 259 | 648 | 259 | 648 |
| SESL† | - | - | 40 | 100 | 40 | 100 | 40 | 100 |

DM (degraded minutes) is no longer supported as of DACS IV-2000 (256) Release 5.0.

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

† Only applicable for DS1 signals terminating on DS1 Interface Modules.

‡ CSS (Controlled Slipped Seconds) was formerly known as SLS (Slipped Seconds).

Table 2-7. **Default Thresholds for Scanned (PMGR Based) DS1 Performance Monitoring**

| Monitored Parameter | DS1 Framing Format | | | | | |
|---|---|---|---|---|---|---|
| | Extended Superframe | | | | Superframe | |
| | Far-End* | | Near-End | | | |
| | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily |
| CVP | - | - | 1772 | 4432 | 177 | 443 |
| ESP | 8 | 21 | 8 | 21 | 1 | 3 |
| SESP | 1 | 3 | 1 | 3 | 1 | 3 |
| OOFS | - | - | 1 | 2 | 1 | 2 |
| SEFS | 1 | 2 | - | - | - | - |

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

Table 2-8. **Threshold Value Ranges for Dedicated Full-Time, Camp-On Full-Time, and Line DS1 Performance Monitoring**

| Monitored Parameter | Far-End* | | | Near-End | | |
|---|---|---|---|---|---|---|
| | 15 Min | Hourly | Daily | 15 Min | Hourly | Daily |
| **Dedicated Full-Time (SWIF2 Based) and Camp-on Full-Time (PMGR Based)** | | | | | | |
| CVP | 0-2097152 | 0-8388608 | 0-134217728 | 0-2097152 | 0-8388608 | 0-134217728 |
| ESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| BESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| SESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| OOFS | - | - | - | 0-900 | 0-3600 | 0-65535 |
| UAS | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| SEFS | 0-900 | 0-3600 | 0-65535 | - | - | - |
| CSS‡ | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| **Line (DS1IF Based)** | | | | | | |
| CVL† | - | - | - | 0-58981500 | 0-235926000 | 0-4294967295 |
| ESL† | - | - | - | 0-900 | 0-3600 | 0-65535 |
| SESL† | - | - | - | 0-900 | 0-3600 | 0-65535 |

DM (degraded minutes) is no longer supported as of DACS IV-2000 (256) Release 5.0.

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

† Only applicable for DS1 signals terminating on DS1Interface Modules.

‡ CSS (Controlled Slipped Seconds) was formerly known as SLS (Slipped Seconds).

Table 2-9. **Threshold Value Ranges for Scanned (PMGR Based) DS1 Performance Monitoring**

| Monitored Parameter | Far-End* | | | Near-End | | |
|---|---|---|---|---|---|---|
| | 15 Min | Hourly | Daily | 15 Min | Hourly | Daily |
| CVP * | - | - | - | 0-65535 | 0-65535 | 0-65535 |
| ESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| SESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| OOFS | - | - | - | 0-900 | 0-3600 | 0-65535 |
| SEFS * | 0-900 | 0-3600 | 0-65535 | - | - | - |

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

The path performance parameters are determined using the cyclic CRC-6 codes in the ESF format or using FBE in the SF format. Line performance parameters are based on bipolar violations.

The monitoring time interval can be provisioned for the short accumulation period measured parameters to be either 15 minutes or 60 minutes. Daily accumulation period parameters are accumulated for 24-hour periods that begin at midnight. Data (for the 15- or 60-minute period) is stored for the preceding 24 hours; daily information is stored for seven days.

### Trouble Condition Reporting

Facility alarm messages are generated if there is a loss-of-signal (LOS) condition or if the Bit Error Rate (BER) threshold is reached or exceeded. The BER is based on BPVs, the framing bits of the SF format, or the CRC-6 bits of the ESF format. The BER alarm threshold can be provisioned to any one of the following rates: $10^{-3}$, $10^{-4}$, $10^{-5}$, $10^{-6}$,$10^{-7}$, $10^{-8}$, or $10^{-9}$ errors per second.

A DS1 on a SWIF2 circuit pack provisioned as unframed uses the CVL algorithm to calculate the BER. An unframed signal riding within a DS3 (a DS1 tributary) does not have its BER calculated.

In addition to reporting the LOS and BER alarms, the DACS IV-2000 reports incoming alarm indication signal (AIS), yellow alarm, and loss-of-frame (LOF) status conditions.

Monitoring for BER threshold crossings is independent of performance monitoring. Therefore, the performance-monitoring feature does not have to be provisioned for the system to monitor the BER count. The system monitors the BER rate for the threshold levels $10^{-3}$ through $10^{-8}$ for SF-formatted signals or $10^{-3}$ through $10^{-9}$ for ESF-formatted signals.

If the BER count for a specific DS1 signal exceeds the threshold, the system sends a `REPT ALM T1` message and flashes the LED on the circuit pack, thereby terminating the DS1 signal.

### DS1 PM Data Reporting

The system database maintains running tallies of all the parameters monitored by the DS1 performance-monitoring hardware. When a parameter count is changed, data is collected based on the parameter and the collection interval previously selected. Each parameter has a predetermined threshold established by the system administrator. If a threshold is reached, the system generates a threshold crossing alert (TCA) message over the administrative links. Records of the processed performance-monitoring data are generated and may be retrieved. The system also provides the capability to schedule performance reports to be generated according to a pre-defined timetable. Schedules can be established for automatic performance reports and can specify:

- Starting time of the first report
- Interval between reports (can be set to a value in the range of 15 minutes to 24 hours for the 15-minute or 1-hour data, or from 1 to 7 days for the daily data)
- Facilities included in the report
- Parameters to be reported
- Monitoring time period covered by each report
- Total number of reports.

**NOTE:**
The current short interval (15-minute or 1 hour) and the current daily total DS1 path performance-monitoring data being collected is lost if:

- A circuit pack fails or is removed in a DS1 protection group (a pair of DS1IFs and SWIF circuit packs)
- A manual switch to protection in a DS1 protection group is made
- A PMGR1 circuit pack fails or is removed
- A UC2 circuit pack in a DS1 interface module and/or a module equipped with PMGR1 circuit packs is extracted, fails or is removed.

Failure of both hard disks (PRI) causes loss of the 7-day history of daily total DS1 performance-monitoring data for all monitored DS1 facilities on the DACS IV-2000.

Any unused ports being monitored, either full-time or scanned, should be provisioned as UNF. Since whole DS1 interface groups or the DS1 ports associated with MUXs can be monitored or scanned, unused ports are included in the monitoring process. Therefore, provisioning unused ports to UNF reduces the number of `REPT EVT T1` messages that are received at the CILINKs.

The system generates scheduled reports using the `REPT PM T1` message. To receive these reports, the administrative link(s) must meet the following conditions:

- The correct authorization code must be logged in.
- Message Screening must be set to **AUTO** or **ALL**.
- User Privilege Code (UPC) of **PM1**, **PM2**, **PM3**, **PM4**, or **PM5** must be used.

The `REPT PM T1` message reports DS1 performance information as scheduled in the **SCHED-PMREPT-T1** command.

If a MUX3 is deprovisioned via the **DLT-EQPT** command, performance monitoring for all DS1 tributaries of that DS3 stops and the collected PM data on that circuit pack are lost. If a MUX3 is extracted from its slot, performance monitoring for all DS1 tributaries of that DS3 stops and the collected PM data on that circuit pack are lost.

If a MUX3 circuit pack is provisioned in the clear-channel mode (to support DS3 clear-channel or gateway connection), DS1 performance monitoring is not supported on the tributaries.

## DS3 Performance Monitoring

You can only use DS3 performance monitoring in collocated configurations. DS3 performance monitoring provides:

- DS3 performance data based on path as well as line parameters
- Processed performance data in compliance with Bellcore TR-TSY-000820 and AT&T Compatibility Bulletin Number 149, *Maintenance Standards for Digital Transmission Systems, Issue 3* (CB149)
- Performance-monitoring data available on all message-based administrative links.
- DS3 performance monitoring is supported on the received DS3 facility in the same way whether the facility is being cross-connected as a DS3 clear-channel (either DS3 to DS3 or DS3 to STS-1) or as DS1 tributaries.
- In addition to supporting asynchronous and C-bit parity formats, the MUX3 circuit pack terminates unframed DS3 signals. Unframed DS3 signals have limited performance monitoring:
  - — BER metric, BPV only
  - — Only line performance
  - — Only Threshold-crossing alerts (TCAs).

Except for the Copy of Parity Bits (CP-BIT) errors of the C-bit parity format, the DACS IV-2000 normally does not monitor the total path of the DS3 signal. This is because upstream equipment cleans up the signal before it reaches the DACS IV-2000. With enhanced performance monitoring, the system now monitors

the F- and M-bits in the DS3 signal to provide DS3 path performance monitoring for the M13 line DS3 format. In addition, the DS3 path performance monitoring for the C-bit parity format is done by monitoring the CP-BITS errors.

### Monitored Parameters

The DACS IV-2000 processes performance data in compliance with CB-149 (PSET#1) and Bellcore TR-TSY-000820 (PSET#2). This applies to the M13 line and C-bit parity Bipolar Violations (BPV) formats, and to line monitoring (LCV and DS3 parity) and path monitoring (DS3 F- and M-bits, DS3 CP-BITS, and DS3 far-end block error bits).

The following performance BER metric parameters can be monitored:

- Bipolar Violations (BPV); BPVs monitored but not stored
- Parity (PTY)
- Copy of Parity Bits (CP-BITS)
- F and M Bits Adjusted (FMA-BITS)
- F and M Bits Nonadjusted (FMN-BITS).

For unframed DS3, the MUX3 circuit pack is not required to provide any functionality that requires it to be able to frame on the DS3 signal, so only line performance parameters can be monitored using B3ZS code violation.

At any given time, only one primitive (BER metric parameter) can be monitored on a DS3 port. The CP-BITS primitive is valid only for the C-bit parity format (not for the M13 line format). In addition, the BER alarm threshold can be provisioned to any one of the following rates: $10^{-3}$, $10^{-4}$, $10^{-5}$, $10^{-6}$,$10^{-7}$, $10^{-8}$, or $10^{-9}$ errors per second.

The BER for a DS3 signal is measured simultaneously between $10^{-3}$ through $10^{-9}$ for BER primitives except parity (P bits). For P-bit metric, $10^{-4}$ through $10^{-9}$ is supported.

With DS3 performance monitoring, the software reports all performance parameters and alarm conditions over any of the DACS IV-2000 administrative links. DS3 performance parameters monitored by the DACS IV-2000 are described below.

**NOTE:**
Removing a MUX3 circuit pack or failure of a MUX3 circuit pack causes the loss of all stored DS3 performance-monitoring data for the associated DS3 facility.

Table 2-10 summarizes the DS3 performance parameters that are monitored by the DACS IV-2000.

Table 2-10. DS3 Performance Monitoring Parameters

| Parameter Set | Path and Line Parameter |
|---|---|
| PSET#1<br>(CB149) | BEC<br>OOFS<br>TPA<br>TPB<br>TPC<br>UAS |
| PSET#2<br>(TR-TSY-000820) | CVL<br>CVP<br>OOFS<br>ESL<br>ESP<br>SESL<br>SESP<br>UAS |

**Parameter Set #1**

The DACS IV-2000 complies with Parameter Set # 1 (PSET#1), as specified by CB-149 requirements. The PSET#1 parameters are:

- Block Error Counts (BEC) — A count of M-frames received with at least one P-bit parity error, one F- and M-bit error, or one line code violation (LCV). A LCV event occurs when bipolar violations (BPV) or excessive zeros (EXZ) are detected. A BPV for a bipolar with 3-zero substitution (B3ZS)-coded DS3 signal is the occurrence of a pulse of the same polarity as the previous pulse without being part of the zero substitution code. An EXZ is the occurrence of any zero string length of 3 bits or more.
- Out-Of-Frame Seconds (OOFS) — A count of OOF events. An OOF event occurs when 3 out of 16 F-bit errors are received or when 2 errored M-bit patterns out of 4 M frames are received.
- Errored Seconds Type A (TPA) — A count of 1-second intervals with no OOF events and exactly one BEC
- Errored Seconds Type B (TPB) — A count of 1-second intervals with no OOF events and between 1 and 44 BECs
- Errored Seconds Type C (TPC) — A count of 1-second intervals with either an OOF event or 45 or more BECs

- Unavailable Seconds (UAS) — Measures the time period that service is unavailable. The line is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, and no failure is present, the path becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the line is unavailable.

PSET#1 performance parameters have thresholds you can set for the current 15-minute interval and for the 96 15-minute (24 hours) rolling total. Their default values for the given time interval are shown in Table 2-11.

Table 2-11. **Monitored Parameters For PSET#1 (CB149) Counters — Register Size and Default Values**

| Parameter | Interval | | | |
|---|---|---|---|---|
| | Current 15 Minutes and Last 96 15-minute intervals | | 24-Hour Total† | |
| | Default | Range | Default | Range |
| Number of Block Errors (BEC)* | 4000 | 0-8458200 | 386500 | 0-811987200 |
| Errored Seconds A (TPA) | 30 | 0-900 | 90 | 0-65535 |
| Errored Seconds B (TPB) | 30 | 0-900 | 90 | 0-65535 |
| Errored Seconds C (TPC) | 20 | 0-900 | 60 | 0-65535 |
| Out-of-Frame Seconds (OOFS) | 10 | 0-900 | 30 | 0-65535 |
| Unavailable Seconds (UAS) | 30 | 0-900 | 90 | 0-65535 |

* MUX2/MUX3 circuit pack only.

† Current day is the sum of hourly intervals beginning at midnight.

When these thresholds are reached, a corresponding TCA message is generated. These thresholds are modifiable, and if you do not specify a threshold crossing level, the DACS IV-2000 assumes the default value for that parameter. If the count of any of the above parameters exceeds the capacity of a specific register, the system pegs the register at the maximum value. The register reinitializes at the end of the data-collection interval after storing the data in memory.

The only allowed DS3 accumulation period for the PSET#1 parameters is the 15-minute interval, which is set during provisioning. A rolling window and a rolling total of the last 96 15-minute intervals are provided. A validity indicator provides an indication of whether data being sent to an operations system (OS) or administrative link is valid and covers the entire accumulation period. This indicator can have a value of `COMPL` (complete), `PRTL` (partial), or `NA` (not available).

**Parameter Set #2**

The DACS IV-2000 complies with Parameter Set # 2 (PSET#2), as specified in Bellcore TR-TSY-000820. The PSET#2 parameters are:

- Coding Violations (CV) — A count of errors detected in an M-frame. M-frame errors are determined from line code violations (LCV), DS3 frame parity errors (P-bit or CP-bit errors), or DS3 F- and M-bit errors. A LCV

event occurs when bipolar violations (BPV) or excessive zeros (EXZ) are detected. A BPV for a B3ZS-coded DS3 signal is the occurrence of a pulse of the same polarity as the previous pulse without being part of the zero substitution code. An EXZ is the occurrence of any zero string length of 3 bits or more.

- Out-Of-Frame Seconds (OOFS) — A count of OOF events. An OOF event occurs when 3 out of 16 F-bit errors are received or when 2 errored M-bit patterns out of 4 M frames are received.
- Errored Seconds (ES) — A count of 1-second intervals in which one or more CVs or one or more OOF events have occurred
- Severely Errored Seconds (SES) — A count of 1-second intervals in which a BER greater than $10^{-6}$ or one or more OOF events have occurred
- Unavailable Seconds (UAS) — Measures the time period that service is unavailable. The line is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, and no failure is present, the path becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the line is unavailable.

PSET#2 performance parameters have settable thresholds for the current 15-minute interval, the current 1-hour interval, and for the 1-day interval (96 15-minute or 24 1-hour intervals). Their default values are given in Table 2-12.

Table 2-12. **Monitored Parameters For PSET #2 (TR820) Counters — Register Size and Default Values**

| Parameter | Interval | | | | | |
|---|---|---|---|---|---|---|
| | Current 15 Minutes | | Current 1 Hour* and Last 24 1-Hour Intervals | | Current Day* and Last 7 Days of daily totals | |
| | Default | Range | Default | Range | Default | Range |
| Coding Violations (CVL/CVP) | 4000 | 0-8458200 | 16100 | 0-33832800 | 386500 | 0-811987200 |
| Errored Seconds (ESL/ESP) | 40 | 0-900 | 40 | 0-3600 | 90 | 0-65535 |
| Severely Errored Seconds (SESL SESP) | 20 | 0-900 | 20 | 0-3600 | 60 | 0-65535 |
| Out-of-Frame Seconds (OOFS) | 10 | 0-900 | 10 | 0-3600 | 30 | 0-65535 |
| Unavailable Seconds (UAS) | 30 | 0-900 | 30 | 0-3600 | 90 | 0-65535 |

* Current hour is the sum of 15-minute intervals beginning on the hour and current day is the sum of hourly intervals beginning at midnight.

When these thresholds are reached, a corresponding TCA message is generated. These thresholds are modifiable, and if a threshold crossing level is not specified, the DACS IV-2000 assumes the default value for that parameter. If the count of any of the above parameters exceeds the capacity of a specific register, then the system pegs the register at the maximum value. The register reinitializes at the end of the data-collection interval after storing the data in the system memory.

The number of received FEBEs is the total number of errored M-frames (that is, the total number of block errors) detected at the far-end. The information is transported to the near-end via the FEBE bits. In the outgoing direction, the transmitted FEBE bits are set whenever a near-end block error occurs. (This is true when the MUX3 circuit pack is in DS1 mode only; in clear-channel mode, transmitted FEBE bits are not modified.)

The DACS IV-2000 allows the user to access performance data stored in 1-day and short intervals. (short intervals may be 15 minutes or 1 hour.) In addition to the short intervals and day counts, and under normal working conditions, the DACS IV-2000 stores: the last 96 15-minute intervals for the previous 24 hours, hourly data for the previous 24 hours, and total daily counts for the previous seven days.

If a MUX3 circuit pack is deprovisioned via the `DLT-EQPT` command, or if it is extracted from its slot, performance monitoring for that DS3 stops and the collected PM data on that circuit pack are lost. If a MUX3 circuit pack is pulled and reinserted, the PM function on the circuit pack is reinitialized and restarted when the MUX3 circuit pack is inserted and auto-provisioned.

When a MUX3 circuit pack is reprovisioned from unframed to framed format or from framed to unframed format, all PM-related parameters and provisioning parameters related to the signal type before the reprovisioning are saved in the database. You can retrieve this information by using the appropriate `RTRV` commands.

## STS-1 and VT1.5 Performance Monitoring

The DACS IV-2000 provides SONET performance monitoring capabilities for intermediate points on the STS-1 and VT1.5 paths as well as at termination points. In this way, the DACS IV-2000 provides a centralized point for monitoring the health of the SONET network.

The MUX3 circuit pack implements the asynchronous-to-SONET gateway function by internally "wrapping" the DS3 signal into an STS1 signal before sending it through the switch matrix. In the opposite direction (from the switch matrix), the MUX3 circuit pack monitors the received STS1s for certain impairments to ensure that the integrity of the cross-connected signal is maintained.

The MUX3 circuit pack detects the following:

- STS1 path trace
- STS1 signal label mismatch
- Internal CRC-6 errors.

For the VT1.5 path, near-end performance monitoring is provided by counting the BIP-2 coding violations using V5 bits 1-2. From these counts, the DACS IV-2000 derives the VT1.5 PM parameters (Table 2-13).

For the STS-1 path, the DACS IV-2000 provides both near-end and far-end performance monitoring. Near-end STS-1 performance monitoring is accomplished by counting the bit interleaved parity-8 (BIP-8) coding violations using the B3 byte. These counts are used to derive the STS path performance monitoring parameters. The far-end parameters are derived by counting the far-end block errors (FEBEs) using G1 bits 1-4.

Table 2-13. **STS-1/ VT1.5 Performance Monitoring Parameters**

| Monitored Parameter | | STS-1 | | | VT1.5 |
|---|---|---|---|---|---|
| | | Section | Line | Path | Path |
| Near-End | SEFS | ✓ | - | - | - |
| | LOSS | ✓ | - | - | - |
| | CV | - | ✓ | ✓ | ✓ |
| | ES | - | ✓ | ✓ | ✓ |
| | ESA | - | ✓ | ✓ | ✓ |
| | ESB | - | ✓ | ✓ | ✓ |
| | SES | - | ✓ | ✓ | ✓ |
| | AISS | - | ✓ | - | - |
| | ALS | - | - | ✓ | ✓ |
| | UAS | - | ✓ | ✓ | ✓ |
| Far-End | CV | - | - | ✓ | - |
| | ES | - | - | ✓ | - |
| | ESA | - | - | ✓ | - |
| | ESB | - | - | ✓ | - |
| | SES | - | - | ✓ | - |
| | UAS | - | - | ✓ | - |

Note: ✓ denotes monitoring is supported.

The DACS IV-2000 provides all of the line performance monitoring and provides the section performance monitoring required for network elements supporting non-repeatered applications (Severely Errored Frame Seconds and Loss of Signal Seconds).

In its implementation of the SONET networking feature, the DACS IV-2000 extends its performance monitoring capabilities of asynchronous signals to SONET signals. Performance monitoring thresholds in the DACS IV-2000 are selectable on a per-parameter, per-channel basis. Threshold crossing alerts are generated when thresholds are reached or exceeded. Performance monitoring reports are available on a scheduled or demand basis. For the SONET signals, the DACS IV-2000 stores 15-minute bins for up to 8 hours, and performance monitoring totals for the current and previous day.

**NOTE:**
If an SMUX circuit pack is removed or fails, all stored STS-1 and/or VT1.5 performance-monitoring data is lost.

## Monitored Parameters

The DACS IV-2000 monitors and reports section, line, and path-performance parameters to verify that service quality objectives specified in terms of these parameters are being met. Performance monitoring only occurs during available time because service-quality assessments cannot be determined during a period of service outage. From a service perspective, two important criteria must be verified:

- Availability of service, which is measured by the parameter Unavailable Seconds (UAS)
- Quality of service during available time, which is measured by the other performance-monitoring parameters.

### Near-End Section Parameters

The following are the STS-1 section performance-monitoring parameters specified by the ANSI T1M1.3 requirements:

- Severely Errored Framing Seconds (SEFS) — The count of 1-second intervals containing one or more OOF events
- Loss of Signal Seconds (LOSS) — The count of 1-second intervals containing one or more LOS defects. An LOS defect is the occurrence of no transitions on the incoming STS-1 signal (before descrambling) for a time period between 2.3 μs and 100 μs. The LOS defect is terminated after a 125-μs interval during which the LOS defect entry criteria is not met.

STS-1 section performance-monitoring parameter thresholds can be set for the current 15-minute interval and for the current day. Default values for the given time intervals are shown in Table 2-14.

### Near-End Line Parameters

The following are the STS-1 line performance-monitoring parameters specified by the ANSI T1M1.3 requirements:

- Coding Violations (CV) — The count of the BIP errors detected at the line layer of the incoming STS-1 signal. The CV counter is incremented for each BIP error detected. That is, each line BIP-8 can detect up to eight errors per STS-1 frame, with each error incrementing the CV counter. CVs for the line layer are collected using the BIP-8s in the B2 byte located in the line overhead of each STS-1 signal.
- Errored Seconds (ES) — A count of 1-second intervals during which one or more CV or AIS defect occurred
- Errored Seconds Type A (ESA) — A count of 1-second intervals during which exactly one line CV and no AIS defects occurred
- Errored Seconds Type B (ESB) — A count of 1-second intervals during which more than one but less than the number of line CVs that cause an SES (the number of line CVs is set by the `SET-TH-NE` command, system default is 12, allowable range is 1 to 55) and no AIS defects occurred.
- Severely Errored Seconds (SES) — A count of 1-second intervals during which the number of line CVs set by the `SET-TH-NE` command is met or exceeded or during which one or more AIS defects occurred
- Alarm Indication Signal Seconds (AISS) — A count of 1-second intervals containing one or more AIS defects. An AIS defect is the occurrence of a 111 pattern in bits 6, 7, and 8 of the K2 byte in five contiguous STS-1 frames. The AIS defect terminates when bits 6, 7, and 8 of the K2 byte do not contain the 111 pattern for five contiguous STS-1 frames.
- Unavailable Seconds (UAS) — measure the duration for which service is unavailable. The line is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, with no failure present, the line becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the line is unavailable.

STS-1 line performance-monitoring parameter thresholds can be set for the current 15-minute interval and for the current day. Default values for the given time intervals are shown in Table 2-14.

### Near-End STS-1 Path Parameters

The following are the STS-1 path performance-monitoring parameters specified by the ANSI T1M1.3 requirements:

- Coding Violations (CV) — The count of the BIP errors detected at the path layer of the incoming STS-1 signal. The CV counter is incremented for each BIP error detected. CVs for the path layer are collected using the BIP-8 in the B3 byte located in the path overhead of each STS-1 signal.

- Errored Seconds (ES) — A count of 1-second intervals during which one or more path CVs, AIS, or LOP defects occurred
- Errored Seconds Type A (ESA) — A count of 1-second intervals during which exactly one path CV and no AIS or LOP defects occurred
- Errored Seconds Type B (ESB) — A count of 1-second intervals during which more than one but less than the number of path CVs that cause a SES (the number of path CVs is set by the SET-TH-NE command [system default is 9, allowable range is 1 to 55]) occurred and no AIS defects occurred
- Severely Errored Seconds (SES) — A count of 1-second intervals during which the number of path CVs set by the SET-TH-NE command is met or exceeded or during which one or more AIS defects occurred
- Alarm Indication Signal/Loss of Pointer Seconds (ALS) — A count of 1-second intervals containing one or more AIS or LOP defects. An STS-1 path AIS defect is the occurrence of all ones in bytes H1 and H2 in three contiguous STS-1 frames. The STS-1 path AIS defect terminates when a valid STS-1 pointer is detected with the New Data Flag (NDF) set to 1001 (inverted) for one frame or 0110 (normal) for three contiguous STS-1 frames. An LOP defect occurs when either a valid pointer is not detected in eight consecutive frames, or when eight consecutive frames are detected with the NDF set to 1001 without a valid concatenation indicator. The LOP defect is terminated when either a valid pointer with a normal NDF (set to 0110) or a valid concatenation indicator is detected for three contiguous frames.
- Unavailable Seconds (UAS) — measure the duration for which service is unavailable. The path is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, with no failure present, the path becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the path is unavailable.

STS-1 path performance-monitoring parameter thresholds can be set for the current 15-minute interval and for the current day. Default values for the given time intervals are shown in Table 2-14.

Table 2-14. **STS-1 Performance Monitoring Thresholds**

| Parameter Name | Accumulation Interval | | | |
|---|---|---|---|---|
| | 15 Minutes | | Day | |
| | Default | Range | Default | Range |
| **Section Performance-Monitoring Parameters (Near-End)** | | | | |
| SEFS | 10 | 0-900 | 100 | 0-86400 |
| LOSS | 10 | 0-900 | 100 | 0-86400 |
| **Path and Line Performance-Monitoring Parameters (Near-End)** | | | | |
| CV | 4666 | 0-46660 | 447900 | 0-4479000 |
| ES | 65 | 0-900 | 648 | 0-86400 |
| ESA | 65 | 0-900 | 648 | 0-86400 |
| ESB | 65 | 0-900 | 648 | 0-86400 |
| SES | 10 | 0-900 | 100 | 0-86400 |
| AISS (line only) | 10 | 0-900 | 100 | 0-86400 |
| ALS (path only) | 10 | 0-900 | 100 | 0-86400 |
| UAS | 10 | 0-900 | 100 | 0-86400 |
| **Path Performance-Monitoring Parameters (Far-End)** | | | | |
| CV | 4666 | 0-46660 | 447900 | 0-4479000 |
| ES | 65 | 0-900 | 648 | 0-86400 |
| ESA | 65 | 0-900 | 648 | 0-86400 |
| ESB | 65 | 0-900 | 648 | 0-86400 |
| SES | 10 | 0-900 | 100 | 0-86400 |
| UAS | 10 | 0-900 | 100 | 0-86400 |

### Far-End STS-1 Path Parameters

For valid far-end monitoring, far-end parameters are derived during 1-second intervals that contain no near-end LOP or AIS defects. For 1-second intervals that do contain near-end LOP or AIS defects, all far-end parameters are set to zero and the invalid data flag is raised. The far-end STS-1 path layer performance is conveyed back to the near-end STS-1 Path Terminating Equipment (PTE) through the path status (G1) byte. Bits 1 through 4 provide a STS-1 path FEBE indication and convey the count of interleaved bit blocks that have been detected in error by the path BIP-8 (byte B3) code. The STS-1 yellow alarm signal conveys the occurrence of AIS or LOP defects detected at the near-end.

Far-end STS-1 path parameters are derived from the STS-1 path FEBE indication and yellow alarm signal and are similar to STS-1 path performance parameters defined for the near-end STS-1 path.

When these thresholds are reached, a corresponding TCA message is generated. These thresholds are modifiable, and if you do not specify a threshold crossing level, the DACS IV-2000 assumes the default value for that parameter. If the count of any of the parameters in Table 2-14 exceeds the capacity of a specific register, the system pegs the register at the maximum value. The register reinitializes at the end of the data collection interval after storing the data in memory.

### Near-End VT1.5 Path Parameters

The following are the VT1.5 path performance-monitoring parameters specified by the ANSI T1M1.3 requirements:

- Coding Violations (CV) — The count of the BIP errors detected at the path layer of the incoming VT1.5 signal. The CV counter is incremented for each BIP error detected. CVs for the path layer are collected using the BIP-2 in the V5 overhead byte of the floating VT.
- Errored Seconds (ES) — A count of 1-second intervals during which one or more path CVs, AIS, or LOP defects occurred
- Errored Seconds Type A (ESA) — A count of 1-second intervals during which exactly one path CV and no AIS or LOP defects occurred
- Errored Seconds Type B (ESB) — A count of 1-second intervals during which more than one but less than the number of path CVs that cause a SES occurred and no AIS or LOP defects occurred. The number of path CVs is set by the `SET-TH-NE` command. System default is 4, allowable range is 1 to 20.
- Severely Errored Seconds (SES) — A count of 1-second intervals during which the number of path CVs set by the `SET-TH-NE` command is met or exceeded or during which one or more AIS or LOP defects occurred

- Alarm Indication Signal/Loss of Pointer Seconds (ALS) — A count of 1-second intervals containing one or more AIS or LOP defects. An AIS defect is the occurrence of all ones in bytes V1 and V2 in three contiguous VT superframes. The AIS defect terminates when a valid VT pointer with a valid VT size is detected with the New Data Flag (NDF) set to 1001 (inverted) for one VT superframe, or 0110 (normal) for three contiguous VT superframes. An LOP defect occur when either a valid pointer is not detected in eight consecutive VT superframes, or when eight consecutive VT superframes are detected with the NDF set to 1001 without a valid concatenation indicator. The LOP defect is terminated when either a valid pointer with a normal NDF (set to 0110), or a valid concatenation indicator is detected for three contiguous VT superframes.
- Unavailable Seconds (UAS) — measure the duration for which service is unavailable. The path is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, with no failure present, the path becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the path is unavailable.

You can set VT1.5 path performance-monitoring parameters thresholds for current 15-minute interval and for the current day. The default values and ranges are shown in Table 2-15.

Table 2-15. **VT1.5 Performance Monitoring Thresholds**

| Parameter Name | Accumulation Interval | | | |
|---|---|---|---|---|
| | 15 Min | | Day | |
| | Default | Range | Default | Range |
| CV | 156 | 0-16383 | 14930 | 0-1048575 |
| ES | 65 | 0-900 | 648 | 0-86400 |
| ESA | 65 | 0-900 | 648 | 0-86400 |
| ESB | 65 | 0-900 | 648 | 0-86400 |
| SES | 10 | 0-900 | 100 | 0-86400 |
| ALS | 10 | 0-900 | 100 | 0-86400 |
| UAS | 10 | 0-900 | 10 | 0-86400 |

When the thresholds are reached, a corresponding TCA message is generated. These thresholds are modifiable, and if you do not specify a threshold crossing level, the DACS IV-2000 assumes the default value for that parameter. If the count of any of the parameters in Table 2-15 exceeds the capacity of a specific register, the system pegs the register at the maximum value. The register reinitializes at the end of the data collection interval after storing the data in memory.

## High-Capacity Controller

The DACS IV-2000 is equipped with two Control Complexes, which maximize control availability and reliability by providing redundancy in the critical parts of the High-Capacity Controller and autonomous recovery from controller failures. The High-Capacity Controller (HCC) Module provides administrative link redundancy and nonvolatile backup memory. The following sections describe additional features provided with the HCC Module.

### Administrative Links

In collocated configurations, two ECI circuit packs provide twelve administrative links (six per ECI circuit pack). The links are identified as CILINK 1-1 through CILINK 1-6 and CILINK 2-1 through CILINK-2-6. The ECI circuit packs can provide administrative link protection by establishing separate links to critical operations systems from each ECI.

In remote configurations, the RCI circuit packs (two in each Remote Complex) provide up to four additional Snider links via the ECI circuit pack(s) in the HCC. These links are identified as CILINK 1-7 and CILINK 1-8, CILINK 2-7 and CILINK 2-8.

### Nonvolatile Backup Memory

The two hard disks are the primary (PRI) nonvolatile backup memory devices for the DACS IV-2000. All database changes are automatically recorded on the disks. A removable read/write optical disk is used to download new software and perform periodic, scheduled backups. The optical disk also backs up the hard disks.

The DACS IV-2000 provides an option to enable automatic database backups from the primary backup medium to the secondary medium. Automatic database backups can be scheduled to execute once in a 24-hour period on selected days or on every day of the week. The primary disk database can also be manually backed up to the secondary disk.

## Secondary Storage Subsystem

The Secondary Storage Subsystem (SSS) consists of a Secondary Storage Controller (SSC), one per Control Complex; two Primary Storage devices (PRI-1 and PRI-2); and a Secondary Storage device (SEC). Functionally, the SSS is responsible for database backup and storage.

The SSS includes two hard disks and a removable optical disk to provide:

- Volatile RAM memory to store relevant system information (such as switch settings and cross-connection maps)
- Primary nonvolatile memory (PRI-1 and PRI-2) of 248 Mbytes
- A SEC, that is, an optical disk drive, which:
  - — has storage capacity of 128 Mbytes
  - — stores system database and the program control out of the equipment or off-site for backup purposes.

The SSS uses the industry-standard SCSI interface for both the primary and secondary nonvolatile memory storage devices.

## Duplex Power Configuration

The DACS IV-2000 (512) Swtich Complex is configured to operate with one or two Lineage® 2000 (or equivalent) battery plants (-48 Vdc nominal) in a central office environment.

With the duplex power architecture, the system receives power from one or two -48V diverse power plants. (A diverse power plant is one that does not share common components, such as BDFBs, rectifiers, batteries, and cable racks.) All -48V power feeds from the BDFB are fused separately at the BDFBs and connected to one or two independent central office battery plants in such a way that loss of one plant does not affect traffic or result in any loss of service (except in a one-battery plant). For more information, refer to the section titled Power Specifications on page A-23.

Pre-Release 4.0 DACS IV-2000 (256) frames capacity expanded are powered by a single power plant (standard) through a BDFB. Starting with Release 4.0 (256) frames capacity expanded and new Remote Complex orders are wired for duplex power and contain the ED-9C114-30 Main Fuse Panel, which contains alarm lamps for each fuse. You cannot upgrade a Remote Complex to duplex power.

## Performance Monitor Test Signal Generator Receiver and Test Signal Identification

This section describes the Performance Monitor Test Signal Generator Receiver (PMGR) and DS1 Signal Identification (TSID).

### PMGR Provisioning

Each PMGR circuit pack supports either the DS1 performance monitoring features or the DS1 TSID feature. You can provision each PMGR circuit pack in the system to specify which of these features it supports. By equipping the system with multiple PMGR circuit packs, both DS1 PM and DS1 TSID features can be simultaneously supported.

### DS1 Test Signal Identification

The DACS IV-2000 provides test signal generators and receivers (TSGRs) at the DS1 rate. This allows the DACS IV-2000 to provide DS1 test signals with unique Test Signal Identification (TSID). The DACS IV-2000 is capable of generating and receiving a TSID signal at the DS1 rate. The DACS IV-2000 provides these capabilities through the performance-monitoring generator receiver (PMGR1) circuit pack. The DACS IV-2000 can also transmit and receive the DS1 TSID through any DS3 multiplexer (MUX) port interface.

With a DS1 TSID, you can:

- Query the system to determine the number of test signal generators and receivers in the system, the test signals that are idle, and the test signals that are being used and by whom they are being used
- Generate a DS1 quasi-random signal with an ID embedded in the DS1 extended superframe (ESF) and data link (DL)
- Receive a DS1 quasi-random signal with an ID embedded in the DS1 ESF DL and request an ID report. Also, any defined error conditions that occur are reported.
- Request the system to read and report the ID from the DS1 ESF DL.

## Alarm Reporting

The DACS IV-2000 provides three levels of alarms: critical, major, and minor.

- A critical alarm indicates a severe, service-affecting condition.
- A major alarm indicates a service-affecting failure, main or unit controller failure, or power supply failure.
- A minor alarm indicates an abnormal condition that is not service-affecting.

Alarms are reported in three places: in the central office (office alarms), in the remote maintenance center (remote alarms), and on the circuit packs (circuit pack alarms).

### Local Office Alarms

The DACS IV-2000 provides the following local office alarm outputs:

- Critical audible
- Critical visual
- Major audible
- Major visual
- Minor audible
- Minor visual
- Main controller failure (processor major) visual.

Local status indicators are provided on the status panel. Detailed alarm information is provided over administrative links. Software-controlled alarms can be delayed to suppress spurious alarms. (The delay is programmable from 1 to 30 seconds.)

The alarm level of incoming DS1, DS3, and EC-1 facility failures can be changed on a per-port basis to major, minor, or no alarm.

The system's Alarm, Scan, and Control (AS&C) points are used with the TABS and TBOS protocols to interface the DACS IV-2000 with operations systems such as Transport Maintenance Administration System (TMAS) and . Three distinct classes of AS&C points exist: alarm points, status points, and control points.

**NOTE:**
Please check the *DACS IV-2000 (512) Release 5.0 Software Release Description* (AT&T 365-340-905) when it becomes available with the software for updates to the AS&C points associated with this release.

An alarm cutoff (ACO) for turning off the audible alarms is provided both on the status panel and at a remote location. Contact closures for visual alarms remain on until the condition causing the alarm is corrected. Parallel alarm closures are also provided by the system.

## Remote Office Alarms

The DACS IV-2000 provides four remote office alarms: critical, major, minor, and processor major, with local status indicators on the status panel circuit pack (see Table 2-16). Detailed alarm information is provided over administrative links. Software-controlled alarms can be delayed in order to suppress spurious alarms. (The delay is programmable from 1 to 30 seconds.)

Table 2-16. **DACS IV-2000 Switch Complex Alarm Indications/Switches**

| Indicators/Switches | Frame | Office | | |
|---|---|---|---|---|
| | Status Panel | Audible | Visual | Remote |
| CR (Critical) indicator | X | X | X | X |
| MJ (Major) indicator | X | X | X | X |
| MN (Minor) indicator | X | X | X | X |
| MC FAIL (Main Controller failure) indicator | X | | X | X |
| ACO indicator | X | | | |
| ACO switch | X | | | X |
| Remote ID indicator (active whenever CR, MJ, MN, or MC FAIL alarm indicators are active) | | | | X |

The alarm level of incoming DS1, DS3, and EC-1 facility failures to major, minor, or no alarm can be changed on a per-port basis. The default alarm level for DS1 facilities is no alarm. The default alarm level for DS3 and EC-1 facilities is major.

AS&C telemetry points and parallel alarm closures and remote reset are provided by the system. The AS&C points are collected by a telemetry remote in the local office and transmitted to the appropriate operations system (OS).

## Circuit Pack Alarms

All circuit packs, except BXA and version 1 synchronizer circuit packs, contain a red LED to aid in trouble isolation. Some circuit packs also contain a green LED to indicate that the circuit pack is active. The LED is mounted so that it is visible while the circuit pack is plugged into the equipment. The power supply circuit packs activate their respective red LEDs when a fault exists, and, because the LEDs are powered from the primary power supply, they light even if logic level power is lost. An alarm indication message is generated for each circuit pack failure.

The Synchronizer Module (with version 2 circuit packs) is a fully duplex module with each synchronizer side comprising three circuit packs: DS1TX2 (DS1 timing extractor 2), TBS32 (time base stratum 3), and DPLL2 (digital phase lock loop 2). Each circuit pack has a green LED and a red LED.

- The red LED (labeled ALM) indicates circuit pack failures. The red LED on any synchronizer module circuit pack (DPLL2, DS1TX2, TBS32) lights continuously while the circuit pack is in a failed condition.
  - — The red LED remains lit for the duration of the failure or 2 seconds, whichever is longer.
  - — The red LED on the DS1TX2 blinks (1 second on, 1 second off) continuously when a reference failure exists on a timing link. The blinking starts immediately upon failure detection and continues as long as the reference failure exists. The blinking stops as soon as the failure is cleared and the reference is declared valid.
- The green LED (labeled ACT) indicates whether the circuit pack is active.
  - — For the DPLL2 and TBS32 circuit packs, the green LED remains lit while the circuit pack is active; that is, the circuit pack is on the active SYNC side. It is extinguished if the circuit pack is not active.
  - — For the DS1TX2 circuit pack, the green LED remains lit while the circuit pack is active; that is, the circuit pack is on the active SYNC side and the SYNC is either in normal or fast mode. It is extinguished if the circuit pack is not active.

**NOTE:**
Whenever the red LED on any synchronizer circuit pack is lit due to any circuit pack failure, the green LED on that circuit pack is extinguished and the circuit pack is removed from service.

## Alarm Conditions and Associated Alarm Levels

Table 2-17 shows alarm condition types and their associated definition for the DACS IV-2000 equipment and facility alarms. Table 2-18 lists the facility and equipment and alarm levels associated with a specific alarm condition.

Table 2-17. **Alarm Conditions**

| Alarm Condition Type | Definition |
|---|---|
| ACPWR | Indicates AC Power Failure detected |
| AIS | Indicates Alarm Indication Signal detected |
| AISFRAMED | Indicates a framed Alarm Indication Signal detected |
| AISL | Indicates Line Alarm Indication Signal detected |
| AISP | Indicates Path Alarm Indication Signal detected |
| AISUNFRAMED | Indicates an Unframed Alarm Indication Signal detected |
| ALLDS2SOOF | Indicates all DS2s in a DS3 signal are Out of Frame |
| ALLREFFAIL | Indicates failure of all synchronizer timing references. |
| BKUPMEMS | Indicates backup to secondary nonvolatile memory failure detected. |
| COM | Indicates a Common Equipment failure detected |
| CONTBUS | Indicates Control Bus failure detected |
| DLI | DS1 data link inaccessable |
| DLN | DS1 data link not responding |
| DS1-AIS | Indicates DS1 Alarm Indication Signal detected |
| DS1IF | Indicates DS1 Interface equipment failure detected |
| DS3FRMTMISMATCH | Indicates DS3 Format Mismatch detected |
| DTLCH | Indicates Data Latch Error detected |
| EOR | Indicates End-of-Range Error detected |
| EXJIT | Indicates Excessive Jitter detected |

Table continued on next page.

Table 2-17. **Alarm Conditions (Continued)**

| Alarm Condition Type | Definition |
|---|---|
| EXPHR | Indicates Excessive Phase Error detected |
| EXTERR | Indicates error detected external to the DACS IV-2000 |
| FANAUX | Indicates fan auxiliary power failure |
| FANFILTER | Indicates fan filter is clogged |
| FANMAIN | Indicates fan main power failure detected |
| FANUNIT | Indicates fan hardware failure detected |
| FERF | Indicates Far-End Receive Failure detected |
| FRD | Indicates security violation has occurred |
| FRQOF | Indicates Frequency Offset Error detected |
| FSNLN | Indicates Frequency Synthesizer Loss of Energy detected |
| FSTO | Indicates PLL Fast Start Time-out detected |
| ICTLR | Indicates Interrupt Controller Error detected |
| IDLE | Indicates Idle signal detected |
| IDMISMATCH | Indicates DS3 Path ID Mismatch |
| IDUNREADABLE | Indicates an unreadable DS3 Path ID |
| IHRER | Indicates Interrupt Holding Register Error detected |
| IMPROPBLK | Indicates Improper Blank circuit pack detected |
| IMPROPRMVL | Indicates Improper Removal detected |
| INC | Indicates Incoming DS3 or DS1 failure detected |
| INHSWPR | Indicates Switch-to-Protection equipment inhibited |
| INHSWWKG | Indicates Switch-to-Working equipment inhibited |
| INT | Indicates Internal hardware fault or failure detected |
| LERDF | Indicates Line-Error Detector Failure detected |
| LOF | Indicates Loss of Frame detected |
| LOP | Indicates Loss of Pointer detected |

Table continued on next page.

Table 2-17. **Alarm Conditions (Continued)**

| Alarm Condition Type | Definition |
|---|---|
| LOS | Indicates Loss of Signal detected |
| MAN | Indicates Manually removed from service |
| MINC | Indicates Multiple Incoming DS1 failures detected |
| MUX | Indicates Multiplex equipment failure detected |
| OOF | Indicates Out of Frame detected |
| PFLCH | Indicates Phase/Frequency Readable Output Latch Error detected |
| PHSTP | Indicates Phase-Step Error detected |
| PSHLN | Indicates Phase Shifter Output Loss of Energy detected |
| RAMER | Indicates RAM Error detected |
| ROMER | Indicates ROM Error detected |
| RTV | Indicates Real-time Violation detected |
| SBITFAIL | Indicates SBIT communications protocol Failure indicating that the far end is not responding to (acknowledging) near end SBIT protocol communication |
| SLMF | Indicates Signal Label Match Failure (at interface end) detected |
| SWSLMF | Indicates Signal Label Match Failure (at switch end) detected |
| SYNCCLK0 | Indicates detected failure is in Side 0 Clock Hardware |
| SYNCCLK1 | Indicates detected failure is in Side 1 Clock Hardware |
| SYNCFRNG | Indicates Synchronizer has made a transition into free-running mode |
| SYNCFST | Indicates Synchronizer has made a transition into fast-start mode |
| SYNCHLDOVR | Indicates Synchronizer has made a transition into holdover mode |

Table continued on next page.

Table 2-17. **Alarm Conditions (Continued)**

| Alarm Condition Type | Definition |
|---|---|
| SYNCPRI | Indicates Synchronizer has detected failure and isolated it to the primary timing reference |
| SYPLN | Indicates Sync Pulse Generator Loss of Energy detected |
| TBCOLD | Indicates Time-Base Oven Cold |
| TBIOER | Indicates Time-Base Communication Error detected |
| TBLEN | Indicates Time-Base Strobe Loss of Energy detected |
| TBNDF | Indicates Time-Base Strobe Energy Detector Failure detected |
| TODC | Indicates Time-of-Day Clock |
| T-BER | Indicates Bit-Error Rate threshold exceeded |
| T-BERL | Indicates Line Bit-Error Rate threshold exceeded |
| TRBER | Indicates High Bit-Error Rate on a Synchronization Timing Reference detected |
| TRMNBER | Indicates Minor Bit-Error Rate on a Synchronization Timing Reference detected |
| URTER | Indicates UART Error detected |
| WRNGPWR | Indicates that the wrong type of PWRJ circuit pack is installed |
| X1LEN | Indicates Loss of Energy on 1-ms Synchronizer Cross-couple detected |
| X3LEN | Indicates Loss of Energy on 30-ms Synchronizer Cross-couple detected |
| XCOOL | Indicates Synchronizer Cross-couple Out-of-Lock Error detected |
| XCRTV | Indicates Synchronizer Cross-couple Real-time Violation Error detected |
| XCSUM | Indicates Synchronizer Cross-couple Summary Error detected |
| XFLRG | Indicates Synchronizer Cross-couple Fast Lock Range Error detected |

Table continued on next page.

Table 2-17. **Alarm Conditions (Continued)**

| Alarm Condition Type | Definition |
|---|---|
| XFQOF | Indicates Synchronizer Cross-couple Frequency Offset Error detected |
| XLKDN | Indicates Synchronizer Cross-couple Communication Link Error detected |
| YEL | Indicates Carrier Group Alarm, Yellow, incoming direction detected |

Table 2-18. **Alarms Associated With Equipment and Facilities**

| Entity | Alarm Condition Types | Alarm Levels |
|---|---|---|
| EC-1 Facilities | AISL, AISP, FERF, LOF, LOP, LOS, SLMF, T-BERL, YEL | MJ, MN, NA |
| T1 Facilities | Near-End (SWIF): DS1-AIS, LOF, LOS, T-BER, YEL<br>Near-End (MUX3): AIS, OOF | MJ, MN, NA |
| | Far-End (MUX2/MUX3): INC, MINC | |
| T2 Facilities | Near-End: OOF | MJ, MN, NA |
| | Far-End: OOF | |
| T3 Facilities | Near-End (MUX1): AIS, LOS, OOF, T-BER<br>Near-End (MUX2): AISFRAMED, AISUNFRAMED, ALLDS2SOOF, DS3FRMTMISMATCH, IDLE, IDMISMATCH, IDUNREADABLE, LOS, OOF, T-BER<br>Near-End (MUX3): AIS, AISFRAMED, AISUNFRAMED, ALLDS2SOOF, DS3FRMTMISMATCH, IDLE, IDMISMATCH, IDUNREADABLE, LOS, OOF, SWSLMF, T-BER | MJ, MN, NA |
| | Far-End (MUX2/MUX3): AIS, IDLE, INC, OOF, SBITFAIL, YEL | |
| VT1.5 Facilities | AISP, LOP, YEL | MJ, MN, NA |
| CILINK | EXTERR, FRD, INT | MN |
| CLKDR2 | IMPROPRMVL, INT | MJ, MN |

Table continued on next page.

Table 2-18. **Alarms Associated With Equipment and Facilities (Continued)**

| Entity | Alarm Condition Types | Alarm Levels |
|---|---|---|
| CLKGN4 | INT, IMPROPRMVL | MJ |
| CC | INT, MAN | MJ, MN |
| DPLL1/DPLL2 | DTLCH, FSNLN, FSTO, ICTLR, IHRER, INT, PFLCH, PSHLN, ROMER, RAMER, RTV, SYPLN, TBLEN, URTER, X1LEN, X3LEN, XCOOL, XCRTV, XCSUM, XFLRG, XFQOF, XLKDN | MJ |
| DS1IF1 | IMPROPBLK, IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| DS1IP1 | IMPROPBLK, IMPROPRMVL, INT | MJ, MN |
| DS1RY1 | IMPROPRMVL, INT | MJ |
| DS1TX1/ DS1TX2 | EXJIT, FRQOF, INT, LERDF, LOF, MAN, OOF, TBLEN, TBNDF | MJ |
| DS3PM2 | INT | |
| ECI6 | INT, TODC | MN |
| Fan Assembly (Switch Complex and Collocated Interface Bays) | FANAUX, FANFILTER, FANMAIN, FANUNIT, INT | MJ, MN |
| Fan Assembly (Remote Complex) | INT | MJ, MN |
| MC | INT, MAN | MJ, MN |
| MTC | INT | MJ, MN |
| MUX1/MUX2/ MUX3 | Near-End: IMPROPBLK, IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| | Far-End (MUX2/MUX3): ACPWR, COM, DS1IF, MUX | MJ, MN, NA |

Table continued on next page.

Table 2-18. **Alarms Associated With Equipment and Facilities (Continued)**

| Entity | Alarm Condition Types | Alarm Levels |
|---|---|---|
| MUXP1/ MUXP2/ MUXP3 | IMPROPBLK, IMPROPRMVL, INT, | MJ, MN |
| MUXPS1 | IMPROPRMVL, INT | MJ, MN |
| OPEX | IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| OSWIO | CONTBUS, IMPROPRMVL, INHSWPR, INHSWWKG, INT, SYNCCLK0, SYNCCLK1 | MJ, MN |
| OUI | INT | MJ, FAILURE |
| PMGR1 | INT | MN |
| PRI4 | INT, MAN | MJ, MN, FAILURE |
| PWRA | IMPROPRMVL, INT | MJ |
| PWRE1/ PWRE2/ PWRE3 | IMPROPRMVL, INT | MJ |
| PWRF | INT | MJ |
| PWRG | INT | MJ |
| PWRJ | IMPROPRMVL, INT, WRNGPWR | MJ |
| RUI (UIA/UIB/ SCI) | INT, MAN | MN |
| SCI2 | INT | MJ, MN, FAILURE |
| SEC4 | BKUPMEMS, INT, MAN | MN |
| SMUX1 | IMPROPBLK, IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| SMUXP1 | IMPROPBLK, IMPROPRMVL, INT | MJ, MN |
| SWCS3 | CONTBUS, IMPROPRMVL, INHSWPR, INHSWWKG, INT, SYNCCLK0, SYNCCLK1 | MJ, MN |

Table continued on next page.

Table 2-18. **Alarms Associated With Equipment and Facilities (Continued)**

| Entity | Alarm Condition Types | Alarm Levels |
|---|---|---|
| SWIF1/SWIF2 | IMPROPBLK, IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| SWIO2 | CONTBUS, IMPROPRMVL, INHSWPR, INHSWWKG, INT, SYNCCLK0, SYNCCLK1 | MJ, MN |
| SYNC | MAN | MJ, MN |
| SYNCN | ALLREFFAIL, SYNCFRNG, SYNCFST, SYNCHLDOVR, SYNCPRI, SYNCSEC | MJ, MN |
| SYNCPRI | EOR, EXJIT, EXPHR, FRQOF, LOS, LOF, PHSTP, TRBER, TRMNBER | MJ, MN |
| SYNCSEC | EOR, EXJIT, EXPHR, FRQOF, LOF, LOS, PHSTP, TRBER, TRMNBER, | MJ, MN |
| TBS31/TBS32 | INT, TBIOER, TBLEN | MJ |
| UC4 | INT, MAN | MJ |
| UI3 | INT | MJ, FAILURE |

### Multiple Alarm Processing

This feature improves the correlation and readability of alarm report messages and enhances system performance. The Multiple Alarm Processing and Reporting feature collects multiple alarms that occur within 1second into a single alarm message. This reduces system overhead, and makes alarm messages easier to read and interpret.

### RTRV-ALM-ALL Command

The `RTRV-ALM-ALL` command can be used to retrieve the active near-end T1, T2, T3, VT1.5, and EC-1 facility alarms, equipment alarms, and link alarms. The output message also indicates if the frame is in critical alarm.

### Alarm Clear Messages

For each alarm condition reported, a message is sent when the alarm is cleared regardless of any other active condition on the same report.

### CB-149 Alarm Compliance

The DACS IV-2000 software provides a clear delay capability that specifies the length of time from the time a condition clears until the associated alarm point is cleared and a message is issued to indicate the cleared condition. The clear delay time is provisionable from 1 to 20 seconds. The alarm is cleared if the condition clears and remains clear for the provisioned clear delay time.

## Communication and OS Interfaces

The user and OS interfaces of the DACS IV-2000 are used in the operations, administration, maintenance, and provisioning of the system.

### Security

The DACS IV-2000 provides a security feature that offers secured access to the Main Controller (MC). This feature includes login and password protection, manual logout, and super-user access to administer logins for MC access. The super user can restrict the access of other users to only that subset of commands they need to do their job. For example, technicians who only need to perform various system queries can be assigned user logins that restrict them from executing potentially service-affecting commands.

## Security Audit

To help system administrators determine if the security of the system has been compromised, the DACS IV-2000 provides a security audit feature to maintain a record of the following security-related events:

- User logins and all autonomous and manual user logouts
- Login creations, deletions, and changes
- Failed login attempts that result in a link lockout
- Input commands issued by a user with the incorrect security level
- Changes of the system time or date
- Edit link security parameters
- Delete security audit records.

The audit log maintains the most recent 100 security related events in nonvolatile memory.

## Message Screening

Five message screening values can be provisioned on a per-link and a per-user basis. When logged into a link, the user value has precedence over the link value. The five message screening values are:

- INPUT — specifies that the user or link receives responses to its own input commands.
- AUTO — specifies that the user or link receives responses to its own input commands and to autonomous messages except for report database change messages due to manual command input.
- ALL — specifies that the user or link receives responses to its own input commands, to autonomous messages except for report database change messages due to manual command input, and to responses to input commands from other users.
- DBAUTO — specifies that the user or link receives responses to its own input commands and to autonomous messages including report database change messages due to manual command input.
- DBALL — specifies that the user or link receives responses to its own input commands, to autonomous messages including report database change messages due to manual command input, and to input commands from other users.

## User Priority Levels

Super users can assign a priority level to a user's login so that commands entered by that user are processed according to the priority level assigned. When commands are entered over the administrative link, the software places each command in a queue. This allows the processor to execute each command one at a time. If a number of commands are in the queue, the processor executes them according to the priority assigned to the user who entered the command.

The five user priority levels are defined as 1 to 5, with 5 being the highest priority level. For example, if the queue contains three commands with the first two entered by a user with a priority level of 3 and the last command entered by a user with a priority of 4, then the processor executes the last command first. If two commands have the same priority, then the processor executes the commands in the order received. This feature is useful in circumstances that require immediate processing of commands, such as enabling cross-connections for restoration.

## Command Verification

The DACS IV-2000 has a command verification feature that reduces the chance of error. The software displays a warning message and requires a confirmation before allowing the processor to execute commands that can affect service or prevent access to the system for extended periods of time. After receiving the warning message, you have the option to modify, cancel, or execute the command. The system administrator can disable this feature for specified user logins, allowing the OS to operate unimpeded by command reviews and warning messages.

The expanded command verification warning messages also inform you when the execution of a `CPY-MEM` command takes longer than 10 minutes.

## X.25 Links

The DACS IV-2000 supports the X.25 Packet Assembler and Disassembler (PAD) and provides an X.25 Clear-to-Send detection.

### X.25 Packet Assembler and Disassembler

Using an external Packet Assembler and Disassembler, an X.25 link can be converted into multiple asynchronous terminal interfaces. The PAD can be used to connect asynchronous terminals to the system for local operation, or to modems for remote (networking) operation (see Figure 2-29). The recommended PAD is a MICOM® box Type 2 X.25 asynchronous PAD.

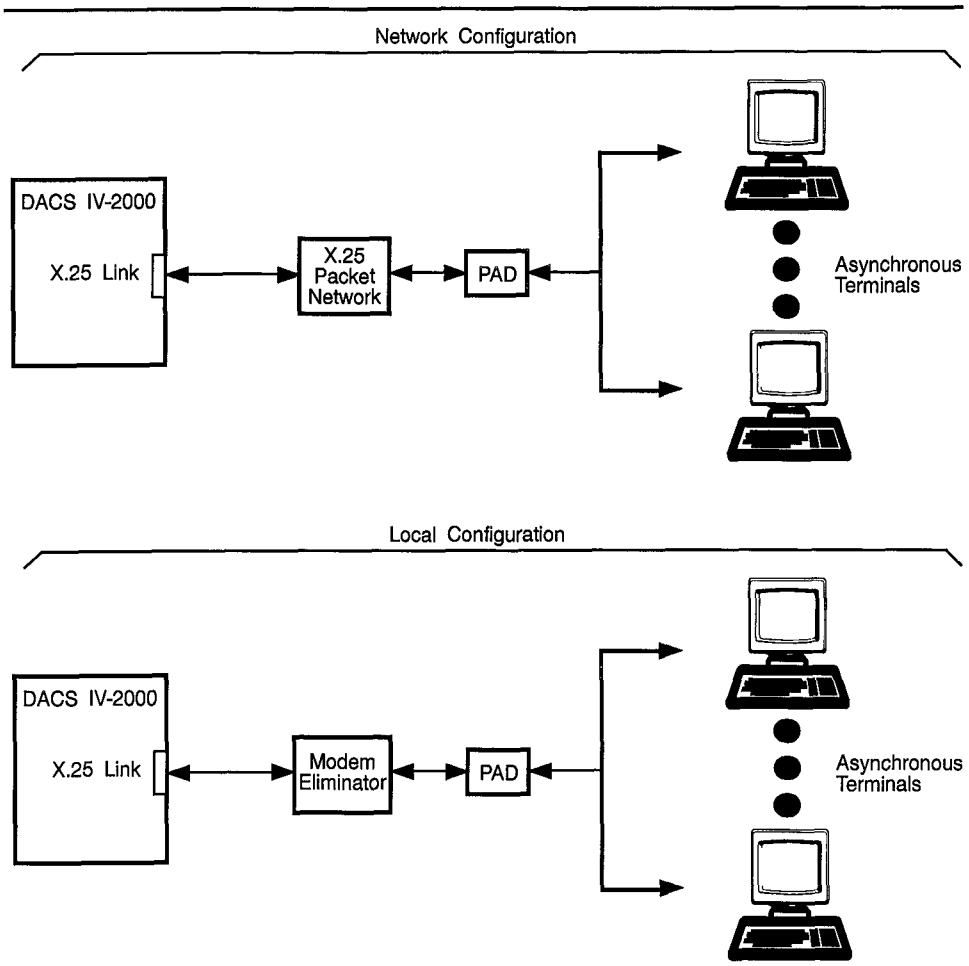



Figure 2-29. **X.25 PAD Applications**

## X.25 Flow Control

With the X.25 flow control feature, commands are never dropped because of full input buffers if the OSs have been suitably coded. Without the X.25 flow control feature, the DACS IV-2000 can not accept commands when the input buffers are full; it drops commands and sends back the input acknowledgment `RL` (retry later). With X.25 flow control, the DACS IV-2000 stops acknowledging X.25 commands when the input buffers are full. By not acknowledging commands, back pressure is applied through the X.25 network and stops the sending system from transmitting commands until the DACS IV-2000 is ready to accept them again.

## Supported Operations Systems

The DACS IV-2000 provides for communications with various Bellcore and AT&T Operations Systems (Figure 2-30). The DACS IV-2000 command message set complies with the current Bellcore TL1 specifications. This message set allows for communicating with Bellcore Operations System/Intelligent Network Element (OPS/INE) and Network Monitoring Analysis (NMA).

### Bellcore Operations Systems

The DACS IV-2000 can communicate with the following Bellcore Operations Systems (OSs):

- Facility and Equipment Planning System (FEPS) is used by capacity planners to plan equipment and facility usage and to forecast demand for new equipment and facilities.
- Trunks Integrated Record Keeping System (TIRKS®) maintains a database of equipment and facilities in the interoffice network to design end-to-end circuits for service provisioning.
- Operations System/Intelligent Network Element (OPS/INE) implements cross-connects in the DACS IV-2000 based on information received from the provisioning system.
- Network Monitoring Analysis (NMA) collects alarms and performance-monitoring data from the DACS IV-2000.
- FLEXCOM/linc supports end-customer control of the DACS IV-2000.
- Integrated Test System (ITS) supports facility testing.

The interface to OPS/INE and NMA is through X.25 links.

In addition to the alarm data from the DACS IV-2000 that are sent to a central OS through TL1 messages, the remote MUX capabilities of the DACS IV-2000 support the communication of alarm data from a DDM-1000 (or any vendor's M13 multiplexer meeting Bellcore TR-TSY-000009 or ANSI TI.107 specifications) to an alarm monitoring OS such as NMA. Because of this capability, direct communication links to the remote M13 for alarm data are not required.

In order for the DACS IV-2000 Release 5.0 to interface with current Bellcore OSs and for full support of the Release 5.0 features, the following releases (or later) of the NMA, OPS/INE, and TIRKS software should be used:

- NMA - Release 6.0
- OPS/INE - Release 2.1
- TIRKS - Release 17.1.

### AT&T Operations Systems

The DACS IV-2000 can communicate with the following AT&T Operations Systems:

- DACScan®-2000 controller automates control over diversely located network elements, such as the DACS III-2000 and DACS IV-2000.
- Remote Measuring System-DS1/Switched Access Remote Testing System (RMS-DS1/SARTS) provides remote testing, executes access commands, and provides performance monitoring (on demand) by the DACS IV-2000.
- Switching Control Center System (SCCS) provides management and surveillance of network elements.
- Total Network Management (TNM) provides management and surveillance of network elements. TNM is a migration of the existing SCCS architecture to the AT&T Star Server® FT Release 2 fault-tolerant computer platform.

In order for the DACS IV-2000 to interface with current AT&T OSs and for full support of the current DACS IV-2000 features, the following releases (or later) of the DACScan-2000 Controller, RMS-DS1/SARTS, and SCCS/TNM software should be used:

- DACScan-2000 Controller - Release 5.2
- RMS-DS1/SARTS - Release 6.0.0.12
- SCCS - Release 13.3
- TNM - Release 2.4.

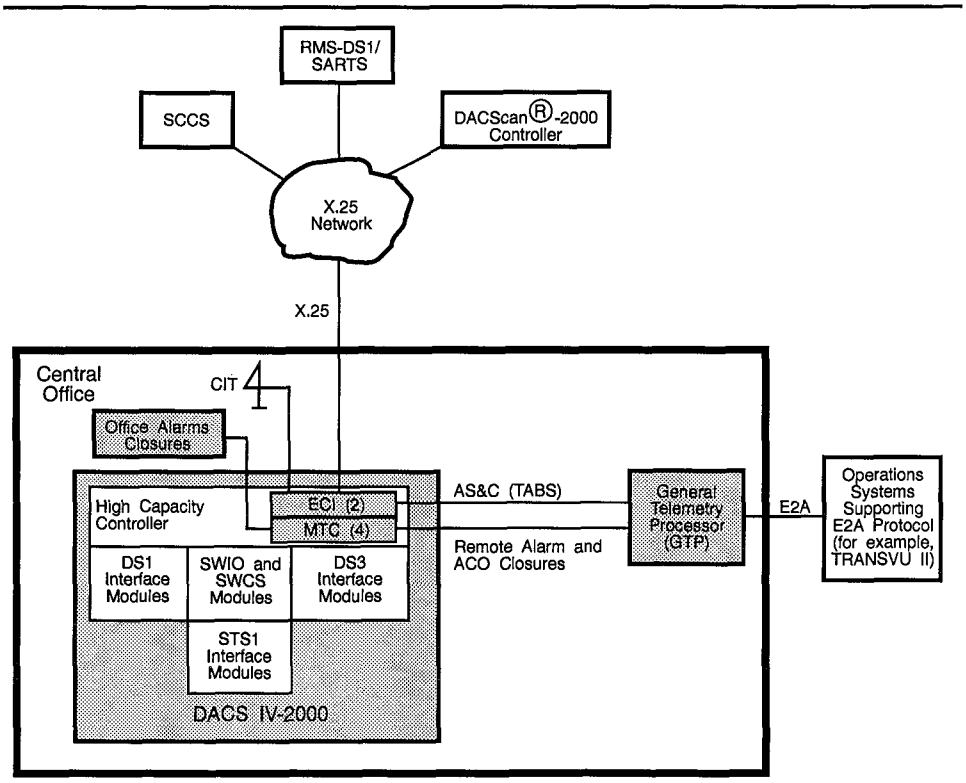



Figure 2-30. **Supported Operations Systems**

## Link Association

When making test access and loopback connections, you can specify that the connection is associated with the user ID and link. When a connection is associated with the link, the connection is automatically disconnected or removed when the user that created the connection logs off. When a test access or loopback connection is made that is not associated with a link, when the user that created the connection logs off the connection remains until it is removed with a `DISC-TACC` (test access) or `RLS-LPBK` (loopback) command.

## Input Command Routing

This feature allows input commands and acknowledgment codes from any administrative link at the DACS IV-2000 frame to be echoed to a specified link. Input commands and acknowledgment codes are echoed through autonomous messages (`REPT LOCL IN`). The following commands support this feature:

- `ACT-ECHO-LINK` activates echoing of input commands from the specified link to another link.
- `CANC-ECHO-LINK` cancels the echoing of input commands from the specified link to another link.
- `RTRV-ECHO-LINK` retrieves the status of echoing of input commands for the specified link.

## Facility Maintenance

Facility maintenance consists of monitoring incoming DS1, DS3, and STS-1 signals; generating alarms and messages when failures are detected; and auditing system security. Facility maintenance features provided by the DACS IV-2000 are described in this section.

## Application of Special Signals

The DACS IV-2000 automatically supplies a DS1, VT1.5, or STS-1 idle signal to the output ports to drive facilities through the switch. If all 28 DS1 tributaries in a DS3 are idle, the system can be provisioned to transmit a DS3 idle signal on the output port. When an incoming signal failure condition is detected at an input port of the switch, a DS1, VT1.5, or STS-1 AIS is supplied to the corresponding output port to replace the failed signal.

The DACS IV-2000 can be provisioned to provide a DS1 test signal supplied by an external test generator, such as a QRSS. One of the DACS IV-2000 DS1 ports must be connected to this generator. A command given to the system, using the broadcast capability of the switch matrix, makes this signal available to any outgoing DS1 port (DS1 or DS3 interface circuit pack). The QRSS can be substituted for normal DS1 data (via user command) when needed for test purposes.

The DACS IV-2000 can insert two special signals onto a specified outgoing facility without taking down the established cross-connection. This feature can be used for verification of facility routing or for testing. The two signals that can be applied are an idle (AIS) signal (unframed all ones) or a DS1 test signal from the external signal generator.

### DS3 AIS and IDLE Signals

If a DS3 facility fails before getting to an upstream network element (such as a DACS III-2000), that network element sends an alarm indication signal (AIS) over the facility to the DACS IV-2000. The AIS inhibits the DACS IV-2000 from generating misleading facility alarms and activates status indications along the path of the DS3 facility. Similarly, if a facility fails coming into the system, the system transmits an AIS to the next network element downstream.

A network element upstream (such as a DACS III-2000) supplies a DS3 idle signal on the DS3 facility if no other signal is connected to the facility at the network element. For example, a DS3 facility can be connected to an incoming port on the DACS IV-2000 coming from a DACS III-2000.

The DACS IV-2000 monitors incoming DS3 ports for DS3 AIS and idle signal. If the DACS IV-2000 detects either of these conditions, the software does the following:

- Inhibits incoming signal failure alarms
- Provides status indications through serial telemetry and over administrative links that indicate detection of AIS or Idle signals
- If AIS, indicates the type of DS3 AIS format.The system can detect two different formats of AIS. Bellcore TR-TSY-000191 specifies that DS3 AIS have valid DS3 framing, information bits set to a repeating `1010` pattern. An alternate CCITT DS3 AIS format specifies an unframed, all-ones signal.

For DS3 facilities requiring any of these capabilities, the MUX2 and MUXP2 (or MUX3 and MUXP3) circuit packs must be used. For DS3 Interface-32 Modules, you must also use Unit Controller 2 (UC2) and Power E3 (PWRE3) circuit packs.

### DS1/DS3 AIS Signals

The DACS IV-2000 automatically supplies a DS1 idle signal (unframed all ones) to any output port that is not cross-connected through the DS1 switch (A DS1 idle signal is identical to a DS1 AIS signal). If all 28 DS1 tributaries in a DS3 are idle, the system can be provisioned to transmit a DS3 idle signal on the output port. If an incoming signal failure is detected at an input port of the DS1 switch, a DS1 (idle) AIS is supplied to the corresponding output port to replace the failed signal.

The detection of signal loss, out-of-frame, or AIS on an incoming DS3 facility causes activation of DS1 AIS on all DS1 tributaries in the DS3 signal.

When an IDLE signal is received, the MUX2/MUX3 circuit pack continues to monitor the transmission path. Because the IDLE signal has valid P-bit, CP-bit parity, and framing bits, the code violation (CV) counter must be incremented for every errored M-frame received. (The CV counter is not incremented for any second in which an LOS condition is detected.)

## Alarm Indication Signals

Alarm indication signals are generated to alert downstream equipment that a failure has been detected on upstream equipment. Refer to Bellcore GR-253-CORE for information on STS-1and VT1.5 signal formats. The following Alarm Indication Signal (AIS) indications are generated by the DACS IV-2000:

- STS-1 AIS Line (AISL) — is generated by section terminating equipment to alert the downstream line terminating equipment that a failure has been detected upstream when an AISL failure state on an incoming STS-1 signal is detected for five consecutive frames. AISL is detected as an all ones pattern in bits 6-8 of byte K2 of the STS-1 signal. The DACS IV-2000 only detects AISLs but does not generate AISLs.
- STS-1 AIS Path (AISP) — is generated by line terminating equipment to alert the downstream STS-1 path terminating equipment that a failure has been detected upstream. AISP is generated by setting bytes H1, H2, H3, and the entire STS-1 SPE to all ones.
- VT1.5 AIS Path (AISP) — is generated to alert the downstream VT1.5 path terminating equipment that a failure has been detected upstream when:
  - — STS-1(VT1.5) signal — an LOS, LOF, AISL, STS-1 LOP, or STS-1 AISP failure state on an incoming STS-1(VT1.5) signal occurs. An VT1.5 AISP is generated in the downstream direction of all associated VT1.5(cc-SPE) tributaries.
  - — VT1.5(cc-SPE) signal — a VT1.5 LOP failure state on any VT1.5(cc-SPE) tributary on an incoming STS-1(VT1.5) signal occurs.

  A VT1.5 AISP is generated by setting bytes V1-V4 and the entire VT1.5 SPE to ones.
- DS1 AIS (DS1, DS3, or STS1 interface) —unframed all-ones signal generated in the downstream direction caused by an upstream equipment failure.
  - — DS1 interface — when a LOS or AIS failure state is entered on any associated incoming DS1 signal
  - — DS3 interface — when a LOS or AIS failure state is entered on any associated DS1 tributary of an incoming DS3 signal
  - — STS1 interface — when a VT1.5 LOP or VT1.5 AISP failure state is entered on any VT1.5(DS1) tributary of an incoming STS-1(VT1.5) signal.

### Yellow Signals

Yellow signals are sent by DS1/STS-1/VT1.5 path-terminating equipment to alert upstream DS1/STS-1/VT1.5 path-terminating equipment that a failure or AIS along the path has been detected and alarmed by the downstream DS1/STS-1/VT1.5 path terminating equipment. The STS-1 yellow signal is indicated by bit 5 of the G1 byte being set to 1. The VT1.5 yellow signal is indicated by bit 8 of the V5 byte being set to 1.

DS1 yellow alarm signals are detected and reported by the DACS IV-2000 on all ports provisioned to support DS1 performance monitoring. STS-1 and VT1.5 yellow alarm signals are detected and reported when received from upstream equipment.

### DS1 Quasi-Random Signals

The DACS IV-2000 can be provisioned to provide an outgoing DS1 signal supplied by an external signal generator. This signal can be quasi-random or another signal pattern. One of the DS1 ports must be connected to the external generator. A command given to the system (using the broadcast capability of the DACS IV-2000 switch matrix) makes this signal available to any outgoing DS1 port. The signal from the external generator is transmitted from all DS1 output ports that are provisioned with an output mode of `QRSS`.

## Facility Failure Detection

DS1, DS3, and STS1 ports are monitored for LOS and for BERs that exceed a user-selectable threshold of $10^{-3}$ through $10^{-9}$, (programmable on a per-port basis). DS3 ports are also monitored for the out-of-frame (OOF) condition. STS1 ports are also monitored for Loss of Frame (LOF), Loss of Pointer (LOP), Section Coding Violation (CV), Line CV, STS-1 Path CV, and VT1.5 Path CV. The STS-1 and VT1.5 Path CVs are gathered for performance monitoring only, and no maintenance signals are generated based on them.

BER is determined as follows:

- DS1 signals — by checking BPVs
- DS3 signals — by checking BPV or parity violations. (On the MUX3 circuit packs, unframed DS3s must be set for BPV.)
- STS-1 signals — by checking bit interleaved parity (BIP).

The occurrence of any facility failure is indicated by a system alarm (Critical, Major, Minor, or no alarm, as provisioned); the appropriate facility failure reports over the administrative links; and a flashing LED on the interface circuit pack associated with the incoming signal.

### Input Port Status (DS1/DS3)

The input port status is provisioned in the DACS IV-2000 to mark DS1 input ports as:

- Driven (DRVN): A good signal is expected and an alarm occurs if the signal is bad.
- Not driven (NDRVN): No valid signal is expected at the port, and the port is not monitored for failures. If the port is formatted, performance monitoring data are accumulated.
- Initialized (INIT): The port is considered nondriven until a valid signal is detected, and when a valid signal is received, status automatically changes to driven.
- Quasi random signal source (QRSS): The port is expecting a DS1 signal provisioned as QRSS.

The input status values for a DS1 tributary within a MUX3 DS3 are DRVN and NDRVN. INIT is not supported. For a MUX3 DS3 port, the input port status values are DRVN, NDRVN, and INIT.

### DS3 Mismatch Detection

Each DS3 port is provisioned for either an M13 or a C-Bit Parity signal type. In previous software releases, when a signal that was not in the provisioned format was received on a port, the DACS IV-2000 generated an alarm. The invalid signal was indicated by either one or more DS2 Out of Frame (DS2OOF) or All DS2 Out of Frame (ALLDS2OOF) alarms. With the DS3 Mismatch Detection feature, the system reports the invalid signal, identifies the source of the problem, and indicates that the invalid DS3 signal is due to a C-Bit Parity/M13 format mismatch. This feature requires that Multiplexer 2 (MUX2) or Multiplexer 3 (MUX3) circuit packs be installed in the DS3 Interface Module.

### Per-Frame Database Change Report

This feature allows the system to report database changes on a per-frame basis. This feature is provisionable at the frame level.

### Port Information Retrieval

The DACS IV-2000 provides a parameter for use when retrieving the status of provisioned ports. Ports are selectable that transmit normal signals, or transmit idle signals, or transmit AIS signals, or transmit a signal from an external DS1 generator.

## Automated Facility Turnup Test

Built-in test signal generators and receivers in the DS1 Interface circuit paths can be used during facility turnup to test facility continuity. A new facility is looped back at the far end, a test signal is applied at the DS1 signal rate, and the presence of the looped-back signal is verified by the test receiver. The system must be equipped with a DS1 Interface Module to have this capability. DS1 and DS3 facilities can be tested, but DS3 facilities are tested as 28 DS1s on an individual DS1 basis. Figure 2-31 provides examples of the automated facility turnup test. For additional information, refer to the section titled "External Cables" of the *DACS IV-2000 (512) Release 5.0 Operations and Maintenance* manual (AT&T 365-340-901).

## Remote Multiplex Communication

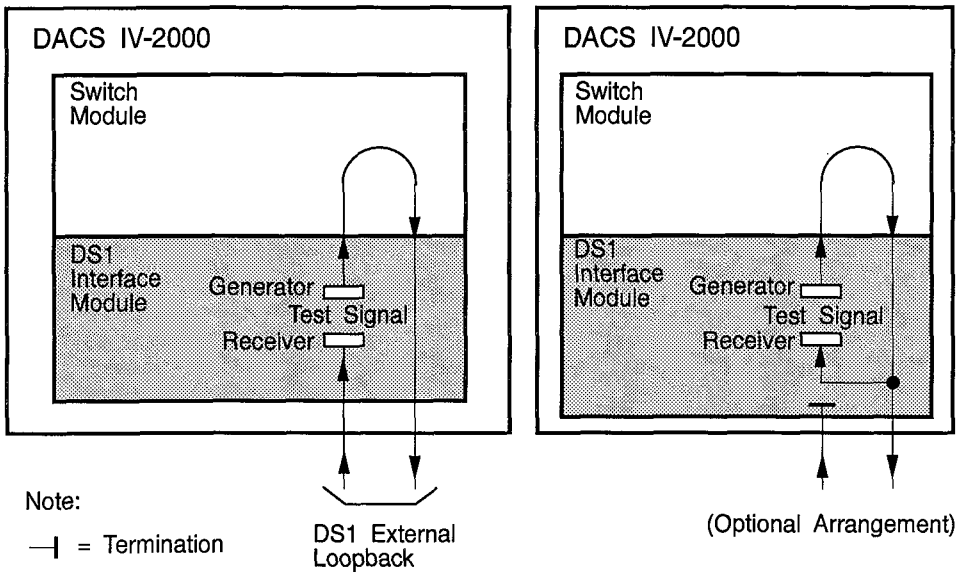
The Remote Multiplex Communication feature enables the DACS IV-2000 to communicate with far-end multiplexers (that is, a DDM-1000 or any M13 multiplexer meeting the TR-TSY-000009 or ANSI TI.107 specifications) by using the DS3 overhead bits. This feature allows the following actions:

- Far-end loopback control
- Response to far-end loopback commands
- Signaling of alarm conditions to the far-end
- Generation of alarm/status messages on far-end conditions.

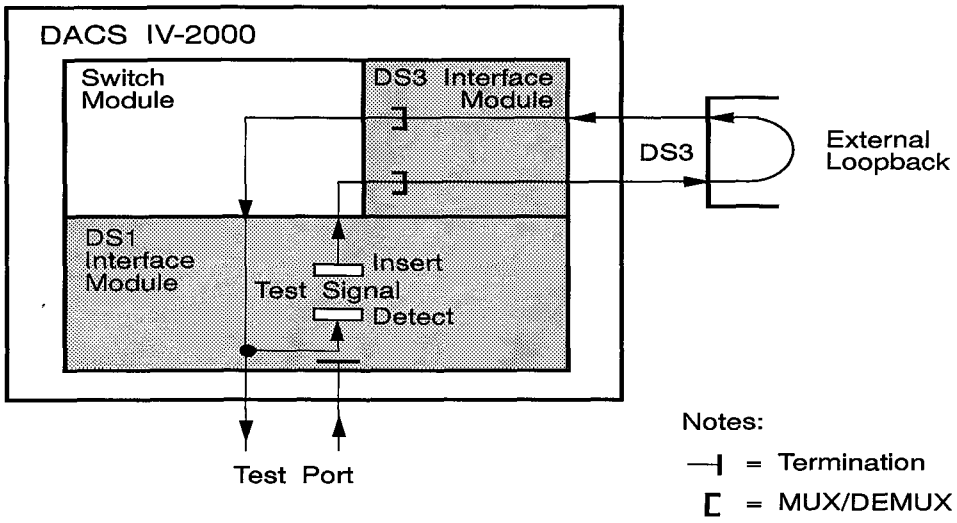
This feature supports the following protocols for communications with multiplexers at the far end of the DS3 facilities:

- DS3 X-bit signaling that indicates far-end DS3 alarm conditions
- DS2 X-bit signaling that indicates far-end DS2 out-of-frame condition
- DS1 loopback control using the DS2 C-bits as specified in Bellcore TR-TSY-000009 (`TR9` value used in `ED-T3` command)
- C-bit parity format far-end alarm and control link for control of DS1 and DS3 loopbacks and reporting of far-end facility and equipment alarm conditions (FEAC) as specified by ANSI T1.107a -1989 (`FEAC` value used in `ED-T3` command)
- S-bit (DS3 stuff bit) communications link used by AT&T DDM-1000 multiplexers for DS1 loopback operations and reporting equipment and facility failure conditions at the far and near ends (`SBIT` value used in `ED-T3` command).

Function and protocol are specified on a per-port basis. This allows the DACS IV-2000 to match capabilities of the far-end multiplexers. For DS3 facilities requiring the remote multiplexer communication feature, the facility must be equipped with MUX2/MUX3 and MUXP2/MUXP3 circuit packs.




**A. Automated Loopback Transmission Test on a DS1 Port**




**B. Automated Loopback Transmission Test on a DS3 Port**

Figure 2-31. **Automated Facility Turnup Test**

The ED-T3 command is used to provision MUX2/MUX3 circuit packs for use with the different remote multiplexer types (TR9, FEAC, or SBIT). In addition, the SET-ATTR-EQPT, SET-ATTR-T1, SET-ATTR-T2, and SET-ATTR-T3 commands are used to set alarm notification levels associated with far-end equipment and facilities.

### DS3 X-Bit Signaling

The DS3 X-bits, when provisioning a MUX2/MUX3 circuit pack for remote multiplexers, allow for the following communications functions:

- Transmit to the far-end equipment that the MUX2/MUX3 circuit pack has detected a DS3 yellow alarm condition (LOF or AIS). The DACS IV-2000 issues a near-end REPT ALM T3 message, indicating the DACS IV-2000 detected the LOF or AIS condition.
- Issue a REPT ALM T3 message with the condition type YEL when the MUX2/MUX3 circuit pack has received indication of a DS3 yellow alarm condition from the far-end equipment.

### DS2 X-Bit Signaling

The DS2 X-bits, when provisioning a MUX2/MUX3 circuit pack for remote multiplexers, allow for the following communications functions:

- Transmit to the far-end equipment that the MUX2/MUX3 circuit pack has detected a DS2 OOF facility condition. The DACS IV-2000 issues a near-end REPT ALM T2 message, indicating the DACS IV-2000 detected the OOF condition.
- Issue a REPT ALM T2 message with the condition type OOF when the MUX2/MUX3 circuit pack has received indication of a far-end DS2 OOF condition from the far-end equipment.

### TR9 Type Remote Multiplexers

Provisioning a MUX2/MUX3 circuit pack for TR9 remote multiplexers allows for the following communications functions:

- Receive far-end requests to establish or release DS1 tributary loopbacks. A REPT DBCHG message is issued when the DACS IV-2000 establishes or releases a loopback due to a remote request.
- If a MUX2/MUX3 circuit pack is not transmitting a DS3 Idle signal, request the far-end equipment to establish or release DS1 tributary loopbacks. Test equipment can be used to determine if the far-end equipment has established or released a loopback requested by the DACS IV-2000.

### FEAC Type Remote Multiplexers

Provisioning a MUX2/MUX3 circuit pack for FEAC remote multiplexers allows for the following communications functions:

- Receive far-end requests (via 16-bit operation and object code words) to establish or release DS1 tributary loopbacks (1 or all 28 associated with the MUX2/MUX3 circuit pack) or DS3 line loopbacks. A `REPT DBCHG` message is issued when the DACS IV-2000 establishes or releases a loopback due to a remote request.
- Request the far-end equipment (via generation of 16-bit operation and object code words) to establish or release DS1 tributary loopbacks (1 or all 28 loopbacks associated with the MUX2/MUX3 circuit pack) or DS3 line loopbacks.
- Transmit to the far-end equipment (via generation of 16-bit operation code-word) that the DACS IV-2000 has detected an equipment or a facility failure. The alarm is declared on the DACS IV-2000 before being transmitted to the far-end. The following failures are reported to the far-end:
  - — Service-affecting DS3 equipment failures — diagnostic audit failures of DS3 hardware
  - — DS3 LOS or T+BER — failure condition received on incoming DS3 signal of MUX2/MUX3 circuit pack communicating with the far end
  - — DS3 OOF, AIS, or IDLE received — conditions received (also includes DS2 OOF) on incoming DS3 signal of MUX2/MUX3 circuit pack communicating with the far-end
  - — Non-service-affecting DS3 equipment failures — failure condition on MUX2/MUX3 circuit pack communication with the far end
  - — Non-service-affecting common equipment failures — failure to SWIO, SWCS, CLKGN, PWRE, CLKDR, UC, SMUX, MUXP2, SWIF, or DS1IF circuit packs associated with the path of the MUX2/MUX3 circuit pack communicating with the far-end
- Issue a `REPT ALM EQPT`, `REPT ALM T1`, `REPT ALM T2`, or `REPT ALM T3` message indicating a far-end equipment or facility failure has been received (via 16-bit operation code word) by the MUX2/MUX3 circuit pack from the far-end. The following alarm conditions are reported by the DACS IV-2000:
  - — MUX — indicates failures associated with far-end DS3 hardware equipment
  - — DS1IF — indicates failures associated with far-end DS1 hardware equipment
  - — COM — indicates failures associated with far-end equipment other than the DS3 hardware within the path of the DS3 signal
  - — AIS — indicates a DS3 AIS signal is received by the far end

- — IDLE — indicates a DS3 IDLE signal is received by the far end
- — INC — indicates a single DS1 LOS or T+BER signal is received by the far-end
- — MINC — indicates multiple DS1 LOS and/or T+BER signals are received by the far end
- — OOF — indicates DS3 or DS2 OOF condition is received by the far end.

### SBIT Type Remote Multiplexers

Provisioning a MUX2/MUX3 circuit pack for SBIT remote multiplexers allows for the following communications functions:

- Issue a `REPT ALM T3` with the alarm condition SBITFAIL when far-end high-speed acknowledgment packets are not received in response to far-end high-speed request packets. During an SBITFAIL condition, requests for operate or release far-end loopbacks are denied.
- Receive far-end requests to establish or release DS1 tributary loopbacks (1 or all 28 associated with the MUX2/MUX3 circuit pack) or DS3 line loopbacks. A `REPT DBCHG` message is issued when the DACS IV-2000 establishes or releases a loopback due to a remote request.
- Request the far-end equipment to establish or release DS1 tributary loopbacks (1 or all 28 loopbacks associated with the MUX2/MUX3 circuit pack). The far-end equipment acknowledges if the loopback is established or denied. If denied, the DACS IV-2000 issues a `REPT EVT T1` message with the condition type `DENYDS1LPCK`.
- Transmit to the far-end equipment that the DACS IV-2000 has detected an equipment or a facility failure. The alarm is declared on the DACS IV-2000 before being transmitted to the far-end. The following failures are reported to the far-end:
  - — Service-affecting DS3 equipment failures — diagnostic audit failures of DS3 hardware
  - — DS3 LOS or T+BER — failure condition received on incoming DS3 signal of MUX2/MUX3 circuit pack communicating with the far end
  - — DS3 OOF, AIS, or IDLE received — conditions received (also includes DS2 OOF) on incoming DS3 signal of MUX2/MUX3 circuit pack communicating with the far end
  - — Non-service-affecting DS3 equipment failures — failure condition on MUX2/MUX3 circuit pack communication with the far end
  - — Non-service-affecting common equipment failures — failure to SWIO, SWCS, CLKGN, PWRE, CLKDR, UC, SMUX, MUXP2, SWIF, or DS1IF circuit packs associated with the path of the MUX2/MUX3 circuit pack communicating with the far end.

- Issue a `REPT ALM EQPT`, `REPT ALM T1`, `REPT ALM T2`, or `REPT ALM T3` message indicating a far-end equipment or facility failure has been received (via 16-bit operation code word) by the MUX2/MUX3 circuit pack from the far-end. The following alarm conditions are reported by the DACS IV-2000:
  - ACPWR — indicates the AC power feed in an unmanned loop cabinet has failed, and the far end is operating on backup battery power
  - MUX — indicates non-service-affecting failures associated with far-end DS3 hardware equipment (for example, MUXR or ELIU of a DDM-1000)
  - DS1IF — indicates service or non-service-affecting failures associated with far-end DS1 hardware equipment (for example, a DS1 circuit pack of a DDM-1000)
  - COM — indicates non-service-affecting failures associated with far-end equipment other than the DS3 hardware within the path of the DS3 signal (for example, power, controller, telemetry circuit pack or a fan on a DDM-1000)
  - AIS — indicates a DS3 AIS signal is received by the far end. This is indicated by all seven DS2 signals being OOF
  - IDLE — indicates a DS3 IDLE signal is received by the far end
  - INC — indicates a single DS1 LOS or T+BER signal is received by the far end
  - MINC — indicates multiple DS1 LOS and/or T+BER signals are received by the far end
  - OOF — indicates DS3 LOS or T+BER condition is received by the far end.

## Frame Maintenance

The features and capabilities of the frame maintenance mechanism are described in this section.

### Incorrect Secondary Disk Load Message

When an attempt is made to copy the database from secondary disk to primary disk, system identifiers (system type, system release, and TID) are compared to the system identifiers in memory (WKG). A warning message is generated if the identifiers differ, and the database transfer is not completed.

### AS&C Activation on Secondary Disk Failures

This feature facilitates remote operations by providing an AS&C point, which is activated whenever a `CPY-MEM` request to the secondary disk (SEC) fails. These failures may not be confined to failures of the secondary disk. The alarm points are held active until the DACS IV-2000 is polled at CILINK 1-4 or CILINK 2-4. After being polled, the alarm points are cleared. In addition, if a `REPT BKUP` message is issued with the status parameter set to `FAIL`, the AS&C points are set.

### Empty Primary Database Check

An empty database is defined as a database with no units provisioned, but otherwise correct. If the frame is instructed to boot a database with this characteristic, the boot fails and the MC is placed in the OOS-MCOND state. A failure message indicates the nature of the failure.

### Disk Verification

This feature automatically verifies and checks the system's ability to access the primary hard disks and the secondary optical disk at least once every 15 minutes. This process detects and reports disk access failures.

### Fault Isolation and Reporting

The DACS IV-2000 can isolate a fault to the incoming facility or equipment. In the case of an equipment failure, the DACS IV-2000 identifies the failed circuit pack by lighting a red LED on the faceplate and generating alarms and administrative link messages.

### Fan Filter Replacement Indication

This feature provides a periodic autonomous message alerting you that the fan filter in the OPEX Bay needs to be replaced. An autonomous message `(REPT FAN FILTER)` is generated when the recommended replacement period of 91 days has expired. The message must be acknowledged manually.

In addition, fan assemblies WP-92310,L4 cause the DACS IV-2000 to generate an alarm for a clogged filter condition (a minor FILTER alarm LED on the fan assembly turns on) and when sensing high preset temperature values. The `REPT FAN FILTER` message can be disabled if the system does not contain an ED-2C816-30,G1 or ED-2C906-30 fan assembly.

## Fan Assembly

Fan assemblies are provided in the Switch Bay, Main Controller, OPEX Bay, and the following interface bays: Enhanced DS1, STS1/DS3, Enhanced STS1/DS3, STS1/DS3/DS1, and the Enhanced STS1/DS3/DS1. The fan assemblies are used to cool the equipment modules. Each fan assembly consists of horizontally mounted fans with a filter, and control switches and indicators. You must keep the air intake (under the assembly) free of obstructions and replace the fan filter on a routine basis.

The WP-92310,L4 and ED-9C130-30 fan assembly monitors air flow and increases air speed to compensate for a partially clogged filter. If the air flow remains insufficient or the temperature exceeds a preset value, an alarm is generated.

## BNC Connectors

The DACS IV-2000 can be equipped with BNC connectors that allow connections to DS3 and EC-1 facilities. BNC connector panels can be ordered with STS1/DS3/DS1, DS3, or STS1/DS3 Interface Bays. The BNC connector panel is provided as part of the electromagnetic compatibility (EMC) enclosure to meet the FCC Class A criteria for EMC, but can be provided optionally without the enclosure.

Advantages of the BNC connectors are:

- The coaxial connections are collected in a single place at a convenient and consistent location.
- A quick, positive connection/disconnection is provided.
- Risks are reduced when handling coaxial lines, since they are kept from the backplane areas.
- A more robust connection is available.
- The coaxial splice is eliminated because the 734A and 735A cables can be brought directly to the frame. The need to downsize to a smaller diameter is eliminated.
- Cable routing and precabling are facilitated. Cables can be pulled from either end with less risk, and if necessary, can be trimmed and re-terminated easily. This minimizes the excess slack problem.
- Standard industry-wide hardware is available, and such items as connectors, tools, and cabling, can be stocked as necessary.

## EMC Enclosures

When fitted with the optional EMC enclosures, the DACS IV-2000 meets the EMC FCC criteria and the electrostatic discharge (ESD) requirements specified in Bellcore TR-NWT-001089.

**NOTE:**
Enclosures must be ordered with any new frame and cannot be field retro-fitted. You cannot use EMC Enclosures on the Remote Complex OPEX Bay.

With the EMC option, the entire front of the DACS IV-2000 is covered with EMC doors. Because of this, you can only view the visual alarm indicators from the front of the frame. However, the EMC enclosure provides a Header Designation Assembly (HDA) at the top of the Switch Bay to house duplicate alarm indicators so they are fully visible to technicians [see the section titled EMC Enclosure Header Alarm Indicators on page 8-21].

## Deny Manual Unit Controller Removal

You cannot manually request removal of a unit controller (UC) from service if any interface circuit pack in that unit is protected. Denying the removal of the UC when an interface circuit pack is protected prevents the interface circuit pack from being unprotected under certain situations.

## Automatic Circuit Pack Restoral

When a failed traffic-carrying circuit pack is replaced, it is automatically returned to service if it passes all system diagnostic tests.

The UC and synchronizer circuit packs are automatically restored when the system is reset provided they are not failed or previously manually removed. The system may be reset by pushing the RESET button, issuing an initialization command, or performing a power-on restart.

## Protection Switching

Protection switching does not take place when the Main Controller is out of service.

## Protection Groups

The DACS IV-2000 architecture divides the circuit packs associated with signal transmission (interfaces and switch matrix) into a number of protection groups. A single failure within a protection group is protected, but additional failures within a single protection group are not protected. Multiple failures occurring in multiple protection groups are protected independently within the individual protection groups.

## Interface Protection Groups

A DS3 interface protection group consists of either a DS3 Interface-32 Module, a DS3 Interface-16 Module, an Enhanced DS3 Interface-16 Module, or a DS3 Clear-Channel Interface-16 Module. The protected entity in a DS3 interface protection group is the MUX circuit pack, which supports one DS3 facility. Each DS3 Interface-32 Module has 32 MUX equipment locations, with 31 of these locations used for service and one used for protection, giving a protection ratio of 1 to 31. Each DS3 Interface-16 Module, Enhanced DS3 Interface-16 Module, or DS3 Clear-Channel Interface-16 Module has 16 MUX equipment locations, with 15 of these locations used for service and one used for protection, giving a protection ratio of 1 to 15.

A DS1 interface protection group consists of all the DS1 Interface Modules within the same bay. The protectable circuit pack in a DS1 interface protection group is a set of three circuit packs, two DS1IF circuit packs and a SWIF circuit pack, which in combination, support 28 DS1 facilities. Each DS1 Interface Module supports eight sets of these circuit packs. An STS1/DS3/DS1 Interface Bay has two DS1 Interface Modules. One DS1 Interface Module uses all eight sets of circuit packs for service. The second DS1 Interface Module uses seven sets of circuit packs for service and one set for protection, thereby providing a 1-to-15 protection ratio. A DS1 Interface Bay has four DS1 Interface Modules. Three use all eight sets of circuit packs for service. The fourth uses seven sets for service and one for protection, thereby providing a 1-to-31 protection ratio.

An STS-1 interface protection group consists of an STS-1 Interface-16 Module. The protectable circuit pack in a STS-1 interface protection group is the SMUX circuit pack, which supports one STS-1 facility. Each STS1 Interface-16 Module has 16 SMUX equipment locations, with 15 of these locations used for service and one used for protection, giving a protection ratio of 1 to 15.

### Failures Within Interface Protection Groups

In an interface protection group, there is a single protection circuit pack and a single protection bus available, so only one protection switch can be performed at a time in that protection group. When a MUX, DS1IF, SWIF, or SMUX circuit pack is protected, relays on the circuit pack are used to switch traffic onto the protection bus, which reroutes the DS3, DS1, or STS-1 signals from that circuit pack to the protection circuit pack. This routing is alternatively performed by contacts on the backplane when a MUX, DS1IF, or SMUX circuit pack is removed from the slot. In order to maintain protection bus continuity, BXA circuit packs must be equipped in unprovisioned slots that are not equipped with MUX, DS1IF, SWIF, or SMUX circuit packs to provide correct protection bus operation.

When you pull a MUX, DS1IF, SWIF, or SMUX circuit pack, protection of another circuit pack in the same protection group can be dropped. In the case of a DS3, or STS-1 interface protection group, it depends on whether the first circuit pack is failed or extracted and the positions in which the circuit packs reside, as to whether or not the pulled circuit pack is protected. In the case of a DS1 interface protection group, no protection is provided until this situation is corrected.

### Failures Between Interface Protection Groups

The DACS IV-2000 protects a single failure in each interface protection group independently of failures in other interface protection groups.

### Switch Protection Group

The switch protection group consists of the SWIO and SWCS circuit packs in the Switch Complex and the associated CLKDR circuit packs in the interface modules. For remote interface modules, the OPEX circuit packs and associated optical fiber are also part of the switch protection group. The protectable circuit pack in the switch protection group is either a SWIO/CLKDR (or OSWIO/OPEX/CLKDR for remote interface modules) circuit pack combination or a SWCS circuit pack. There are 64 SWIO/OSWIO circuit packs, with each circuit pack used to half capacity under normal conditions. The SWIO/OSWIO circuit packs operate in pairs. When a SWIO/OSWIO is protected, its mate circuit pack uses spare capacity to assume the load of the protected circuit pack. There are 32 SWCS circuit packs. Only 31 are needed to provide a nonblocking switch under normal conditions, with the 32nd circuit pack available to protect the others, giving a 1-to-31 protection ratio. Only one SWIO/OSWIO or SWCS circuit pack can be protected at any given time [refer to the section titled Failures Within Switch Protection Groups on page 2-120 for more information].

The CLKDR circuit packs in the DS1, DS3, or STS-1 Interface Modules distribute clock signals from the SWIO/OSWIO circuit packs to the DS1, DS3, or STS-1 interface circuit packs. The failure of a CLKDR circuit pack, therefore, is treated by the system as if the associated SWIO/OSWIO circuit pack failed. Consequently, the switch protection group is extended to include the CLKDR circuit packs in the interface modules.

The OPEX circuit packs in the OPEX Module and associated optical fiber extends the N-rate and clock signals to/from the OSWIO circuit packs from/to the DS1, DS3, or STS-1 interface circuit packs. The failure of an OPEX circuit pack, therefore, is treated by the system as if the associated OSWIO circuit pack failed. Consequently, the switch protection group is extended to include the OPEX circuit packs in the OPEX Module and associated optical fiber.

### Failures Within Switch Protection Groups

When a SWIO (or OSWIO/OPEX or associated optical fiber) or CLKDR circuit pack fails, it is protected by its mate circuit pack; for example, if SWIO-1-1 fails, SWIO-1-2 protects the signals to SWIO-1-1 and the CLKDR (through the OPEX circuit pack for remote interface modules) associated with SWIO-1-2 assumes the signals for the CLKDR associated with SWIO-1-1. In order to support the additional load that is switched onto the mate circuit pack, additional paths through the switch matrix are utilized, and these are provided by the spare 32nd SWCS circuit pack. The need for these paths precludes protecting multiple SWIO or SWCS circuit packs at the same time.

### Failures Between Switch and Interface Protection Groups

Protection switching in the switch protection group requires remapping connections. To perform this within the required time interval, the system maintains prestored maps that are used to protect failures of SWIO/OSWIO and SWCS circuit packs. These prestored maps are updated whenever connections in the switch matrix are changed. Mapping is allowed on all circuit packs while they are protected.

The DACS IV-2000 allows for protection of the switch while one or more interface protection groups are protected. It also allows for protection of one or more interface protection groups while the switch is protected. Due to the prestored map recalculations associated with protection switching, there can be a brief period of time after the protection of an interface group before the switch group can be protected.

## Operational Guidelines

The following operational guidelines must be followed:

- All unprovisioned DS1IF, MUX, and SMUX slots in an interface bay are equipped with a circuit pack, either an unused DS1IF, MUX, or SMUX circuit pack, or a BXA circuit pack.
- Do not pull unprotected traffic-carrying circuit packs from the system.
- Never pull more than one failed circuit pack from one protection group.
- All failures in a protection group should be repaired before performing other maintenance activities in that group.

## System Operation Under Protection

The DACS IV-2000 allows for cross-connections, disconnections, test access, loopback functions, and changes to the output mode on all circuit packs while they are protected.

## Automatic Protection Switching

The DACS IV-2000 circuit packs do not protection switch automatically unless they are carrying traffic. This applies to DS1IF, SWIF, MUX, SMUX, OPEX, SWIO, and OSWIO circuit packs, but it does not apply to SWCS circuit packs because these circuit packs are not associated with specific facilities and because 31 of 32 SWCS circuit packs must be available at all times to guarantee nonblocking.

## Manual Protection Switch

Using the manual protection switch command of either `SW-TOPROTN-EQPT` or `SW-TOWKG-EQPT` always locks the circuit pack in the state (protected or unprotected) to which it is switched. The result is equivalent to issuing an inhibit command (`INH-SW-EQPT`) while in the unprotected or protected state.

If a circuit pack is locked in the protected state, the command `SW-TOWKG-EQPT` causes the circuit pack to switch back to the working state and locks the circuit pack in this state. Therefore, the circuit pack is not subsequently in protection if a failure occurs.

To have the circuit pack revert to the unlocked working state, the `ALW-SW-EQPT` command should be used, which releases the lock and, if the circuit pack is good, automatically switches back to working. The `SW-TOPROTN-EQPT` command can be used on both traffic-carrying and non-traffic-carrying circuit packs.

## LED for Manual Protection Switch

To aid in identifying a circuit pack that has been manually switched to protection, this feature lights the red ALM LED on the interface or switch circuit pack (SWIF, MUX, SWIO, SMUX, or SWCS) when the circuit pack has been manually switched to protection. This is a provisionable feature.

When a manual protection switch has been performed, the red ALM LED on the circuit pack that was switched to protection is constantly lit for the duration of the protection switch. The output response to the command that was used to manually switch the circuit pack to protection contains a warning message that the red ALM LED on the protected circuit pack is lit as a result of this operation.

If a SWIO circuit pack is manually switched to protection, the LED or its associated clock distributor (CLKDR) also lights.

## Autolock

A protected circuit pack cycles through the following states in the protection switching process (assuming no manual locking occurs):

- good/working
- bad/working
- good/protected
- bad/protected.

Normally, the circuit pack is in the good/working state. When a failure occurs, the circuit pack transitions to bad/working. If protection switching is available, the circuit pack transitions to bad/protected. When the problem clears, the circuit pack transitions to good/protected, which is a transient state that is passed through as the circuit pack unprotects and returns to good/working. The state names associated with these four states are:

- ACT = good/working
- ACT-*xxx* = where *xxx* is one of the bad substates: FLT, ABS, BLK, TSTF, or FEF
- OOS-*xxx* = where *xxx* is one of the bad substates: FLT, ABS, BLK, TSTF, or FEF.

The autolock state protects against frequent cycling through the four states due to an intermittent problem. A circuit pack is put into the autolock state when it goes through this cycle *n* times within an *m*-minute period. All autolocks are autonomously released every *x* hours by the system. The values *n*, *m*, and *x* are user provisionable; the default (system initialization) values are:

- *n* = 4 times
- *m* = 10 minutes
- *x* = 24 hours.

Autolock is automatically removed whenever the system is reset or whenever the *n*, *m*, or *x* value is changed; or it can be removed manually by command.

When a circuit pack is in the autolock state, the modifier, ERRANAL, is appended to its state name.

# System Bays

# 3

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# System Bays

# 3

The DACS IV-2000 hardware comprises one Switch Complex (consisting of two Switch Bays and one Main Controller Bay) and from one to sixteen interface bays (containing DS1, DS3, and/or STS1 Interface Modules) in collocated and/or Remote Complex configurations. A Remote Complex consists of an Optical Extension (OPEX) Bay and one to eight interface bays (that is, half of the total system capacity).

The switch contained in the DACS IV-2000 can accept 14,336 input signals. However, 448 paths into the switch are from protection circuit packs, thus limiting the switch to 13,888 traffic-carrying signals. A fully equipped system is capable of making 6,944 two-way DS1 cross-connections.

## System Bays

Release 5.0 of the DACS IV-2000 (512) supports 11 types of system bays:

- Main Controller (MC) Bay — provides the control for the system. This bay contains a fan assembly to provide cooling of the associated equipment.
- Switch (SW) Bay — provides the cross-connections and interbay cabling. This bay contains a fan assembly to provide cooling of the associated equipment.
- Optical Extension (OPEX) Bay — provides the interface for extending the N-rate signals from the interface bays of a DACS IV-2000 Remote Complex onto fiber-optic cables to the SWIO Modules of the Switch Complex. The controller functions are also extended from the High-Capacity Controller (HCC) to the Remote Complex by fiber optic cables.

- Fuse and Alarm (FS & ALM) Bay — provides fuses for up to four collocated interface bays.
- DS1 Interface (INTFC) Bay — provides the interface for up to 868 DS1 signals (equivalent to 31 DS3 signals). Air baffles are provided for equipment cooling.
- Enhanced DS1 Interface (INTFC) Bay — provides the interface for up to 868 DS1 signals (equivalent to 31 DS3 signals). This bay contains a fan assembly to provide equipment cooling and also provides additional space for cable routing.
- DS3 Interface (INTFC) Bay — provides the interface for up to 62 DS3 signals (equivalent to 1736 DS1 signals). Air baffles are provided for equipment cooling.
- STS1/DS3 Interface (INTFC) Bay — provides the interface for up to 60 DS3 or STS-1 signals (each DS3 is equivalent to 28 DS1 signals). This bay contains a fan assembly to provide equipment cooling.
- Enhanced STS1/DS3 Interface (INTFC) Bay — provides the interface for up to 60 DS3 or STS-1signals (each DS3 is equivalent to 28 DS1 signals). This bay contains a fan assembly to provide equipment cooling and also provides additional space for cable routing.
- STS1/DS3/DS1 Interface (INTFC) Bay — provides the interface for:
  - — Up to 420 DS1 signals (equivalent to 15 DS3 signals) and
  - — Up to 46 DS3 signals (equivalent to 1288 DS1 signals) and no STS-1 signals, up to 31 DS3 signals (equivalent to 868 DS1 signals) and 15 STS-1 signals, or up to 30 STS-1 signals and no DS3 signals.

  Air baffles are provided for equipment cooling.
- Enhanced STS1/DS3/DS1 Interface (INTFC) Bay — provides the interface for:
  - — Up to 420 DS1 signals (equivalent to 15 DS3 signals) and
  - — Up to 46 DS3 signals (equivalent to 1288 DS1 signals) and no STS-1 signals, up to 31 DS3 signals (equivalent to 868 DS1 signals) and 15 STS-1 signals, or up to 30 STS-1 signals and no DS3 signals.

  This bay contains a fan assembly to provide equipment cooling and also provides additional space for cable routing.

Table 3-1 identifies the different types of bays and their associated equipment. In addition to the above equipment, if you have purchased the optional EMC enclosures, each bay is equipped with a Header Designation Assembly (HDA). For more detailed information, see the paragraph entitled "EMC Enclosure Header Alarm Indicators" (page 8-21).

Table 3-1. **System Bays and Associated Modules**

| Bay | Module/Panel/Assembly | Units Per Bay | See Note |
|---|---|---|---|
| Main Controller (MC) | Switch Power (SW PWR) | 3 | |
| | Status Panel | 1 | |
| | High-Capacity Controller (HCC) | 1 | |
| | Memory Storage (MEM) | 1 | |
| | Synchronizer (SYNC) | 1 | 2 |
| | Fan Assembly | 1 | |
| Switch (SW) | Switch Input/Output (SWIO) | 2 | 1 |
| | Switch Center Stage (SWCS) | 1 | |
| | Fuse and Alarm (FS & ALM) Panel | 1 | |
| | Fan Assembly | 1 | |
| Optical Extension (OPEX) | Optical Extension (OPEX) | 1 | |
| | Optical Extension Power (OPEX PWR) | 1 | |
| | Auxiliary Power (AUX PWR) | 1 | |
| | Remote Unit Interface (RUI) | 1 | |
| | Remote Unit Interface Power (RUI PWR) | 1 | |
| | Fuse and Alarm (FS & ALM) Panel | 1 | |
| | Fan Assembly | 1 | |
| Fuse and Alarm (FS & ALM) | Fuse and Alarm Panel | 1 | |
| DS1 Interface (DS1 INTFC) | DS1 Interface (INTFC) | 3 | |
| | DS1 Interface-Protection (INTFC-P) | 1 | |
| Enhanced DS1 Interface (ENH DS1 INTFC) | DS1 Interface (INTFC) | 3 | |
| | DS1 Interface-Protection (INTFC-P) | 1 | |
| | Fan Assembly | 1 | |
| DS3 Interface (DS3 INTFC) | DS3 Interface-32 (INTFC) | 2 | 7 |
| | BNC Panel | 1 | |
| STS1/DS3 Interface (STS1/DS3 INTFC) | DS3 Interface-16 (INTFC-16) | 0 to 4 | 6 |
| | Enhanced DS3 Interface-16 (ENH DS3-16) | 0 to 4 | 3, 6 |
| | DS3 Clear-Channel (DS3CC INTFC-16) | 0 to 4 | 3, 6 |
| | STS1 Interface-16 (INTFC-16) | 0 to 4 | 6 |
| | BNC Panel | 1 | |
| | Fan Assembly | 1 | |

See notes at end of table.

Table continued on next page.

Table 3-1. **System Bays and Associated Modules (Continued)**

| Bay | Module/Panel/Assembly | Units Per Bay | See Note |
|---|---|---|---|
| Enhanced STS1/DS3 Interface (ENH STS1/DS3 INTFC) | DS3 Interface-16 (INTFC-16);<br>Enhanced DS3 Interface-16 (ENH DS3-16)<br>DS3 Clear-Channel (DS3CC INTFC-16)<br>STS1 Interface-16 (INTFC-16)<br>BNC Panel<br>Fan Assembly | 0 to 4<br>0 to 4<br>0 to 4<br>0 to 4<br>1<br>1 | 6<br>3, 6<br>3, 6<br>6 |
| STS1/DS3/DS1 Interface (STS1/DS3/DS1 INTFC) | DS1 Interface (INTFC)<br>DS1 Interface-Protection (INTFC-P)<br>DS3 Interface-32 (INTFC-32)<br>DS3 Interface-16 (INTFC-16)<br>Enhanced DS3 Interface-16 (ENH DS3-16)<br>DS3 Clear-Channel (DS3CC INTFC-16)<br>STS1 Interface-16 (INTFC-16)<br>BNC Panel<br>Fan Assembly | 1<br>1<br>0 or 1<br>0 or 1<br>0 to 2<br>0 to 2<br>0 to 2<br>1<br>1 | <br><br>3, 4, 5<br>3, 4,5, 6<br>3, 4, 5, 6<br>3, 4, 5, 6<br>4, 5 |
| Enhanced STS1/DS3/ DS1 Interface (ENH STS1/DS3/DS1 INTFC) | DS1 Interface (INTFC)<br>DS1 Interface-Protection (INTFC-P)<br>DS3 Interface-32 (INTFC-32)<br>DS3 Interface-16 (INTFC-16)<br>Enhanced DS3 Interface-16 (ENH DS3-16);<br>DS3 Clear-Channel (DS3CC INTFC-16);<br>STS1 Interface-16 (INTFC-16)<br>BNC Panel<br>Fan Assembly | 1<br>1<br>0 or 1<br>0 or 1<br>0 to 2<br>0 to 2<br>0 to 2<br>1<br>1 | <br><br>4, 5<br>4, 6<br>3, 4, 5,6<br>3, 4, 5, 6<br>4, 5, 6 |

**Notes**

1. SWIO Modules can contain either SWIO or OSWIO circuit packs: SWIO for collocated interfaces, OSWIO for remote interfaces. You cannot mix circuit pack types within a Switch Bay.
2. The SYNC Module for new systems contains version 2 circuit packs. Existing systems can use either version 1 or version 2 circuit packs.
3. The DS3 Interface-32 Module, DS3 Interface-16 Module, Enhanced DS3 Interface-16, and DS3CC Interface-16 can be referred to generically as DS3 Interface Modules.
4. The total number of DS3 and STS1 Interface Modules in an STS1/DS3/DS1 Interface Bay may not exceed two.
5. STS1/DS3/DS1 and ENH STS1/DS3/DS1 Interface Bays can be equipped with an STS1 Interface-16 Module, Enhanced DS3 Interface-16, or DS3CC Interface-16 in place of the DS3 Interface-32 Module. When used this way, the DACS IV-2000 capacity is decreased by 15 DS3-equivalent signals.
6. The STS1/DS3 Interface-16 shelves can be equipped with DS3 Interfaces, Enhanced DS3 Interface-16, DS3CC Interface-16, or STS-1 Interface-16 Modules. STS1/DS3 Interface Bays can be equipped with any combination of DS3 Interface-16, Enhanced DS3 Interface-16, DS3CC Interface-16, or STS1 Interface-16 Modules totaling four.
7. The DS3 Interface Bay has been rated Discontinued Availability. The DS3 Interface-32 Module is still available on the STS1/DS3/DS1 Interface Bay. The existing DS3 Interface Bays are still supported.

Figures 3-1 through 3-6 illustrate the physical association of collocated and remote bays, units (the shelf positions of interface modules), and interbay cables (refer to the section titled "Interbay Cabling Arrangements" (page 3-32) for more information) in a fully-equipped system with all DS1, DS3/STS1, or DS3 interfaces, respectively.

- The term *Collocated* refers to an interface bay which is physically and electrically connected to the DACS IV-2000 Switch Complex via N-Rate Cables only.
- The term *Remote Complex* refers to an optically remoted (OR) Remote Complex, which is physically separate from the Switch Complex, used to grow to 256 DS3 equivalents. The Remote Complex may have been capacity expanded (CE) to the Switch Complex.

For an example of a collocated interface module using Figure 3-1, look at Unit 11, located in the third column of the second row. The first label in Unit 11 is SWIO 2-7. This represents the Switch Input/Output (SWIO) circuit pack in the SWIO Module that is associated with Unit 11. The designation N-Rate AM indicates half of an N-rate cable (labeled AM) that connects this interface module to the Switch Matrix. The number 9 indicates the DS1 Interface-Protection Module (located in Unit 9) responsible for protecting this interface module. Finally, the number J-11 shows the control cable for this interface module in the bay lineup. Each unit shown in this sample configuration is labeled with the same information.

Note that, on the (512) Switch Complex side, remoting of the interface bays is accomplished by using SWIO Modules (containing OSWIO circuit packs) 1 and 2 for Remote Complex 1 (RX-1), and SWIO Modules 3 and 4 for Remote Complex 2 (RX-2).

For an example of an optically remoted interface module, using Figure 3-2, look at RX-1, Unit 11, located in the third column of the second row. The first label in Unit 11 is SWIO 1-7. This represents the Optical Switch Input/Output (OSWIO) circuit pack in the SWIO Module that is associated with Unit 11. The designation N-Rate AD[1] indicates half of an N-rate cable that connects this interface module to the (512) Switch Complex. The number 9 indicates the DS1 Interface-Protection Module (located in Unit 9) responsible for protecting this interface module. Finally, the number J-7 shows the control cable for this interface module in the bay lineup. Each unit shown in this sample configuration is labeled with the same information.

The unit numbers and control cable numbers shown are the same for any DACS IV-2000 configuration. The examples pictured in these figures are based on maximum DS1, DS3, and STS-1 remote and collocated configurations, but the same numbers are used for other configurations. Refer to the section titled "Interface Module (Unit) Numbering" (page 3-41) for more information.

1. N-rate cables in Remote Complexes are physically labelled the same as (256) frames. The (512) software maps this labelling into the (512) N-rate addressing [refer to the section titled "N-rate Cables for Remote Complex Interface Bays" (page 3-33) for more information on N-rate addressing].

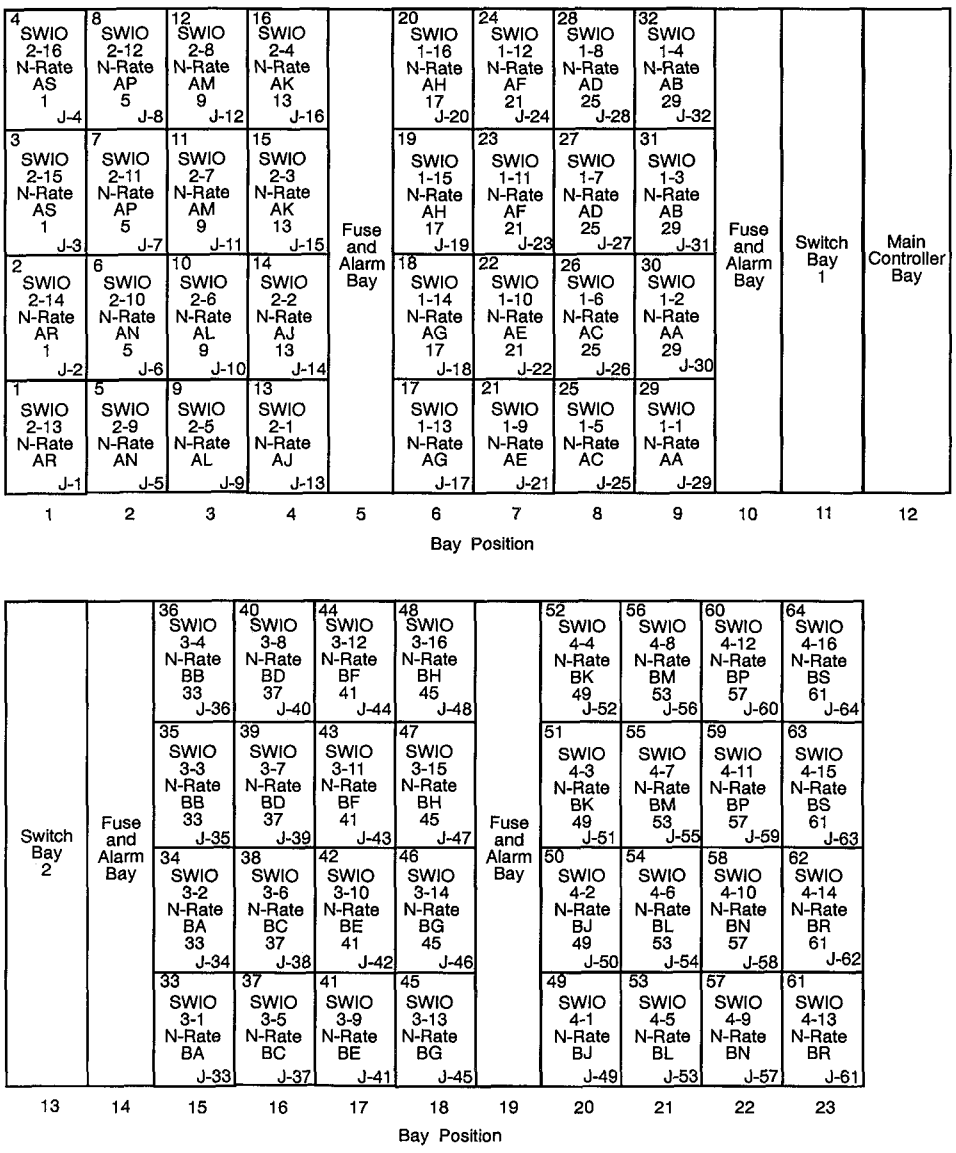
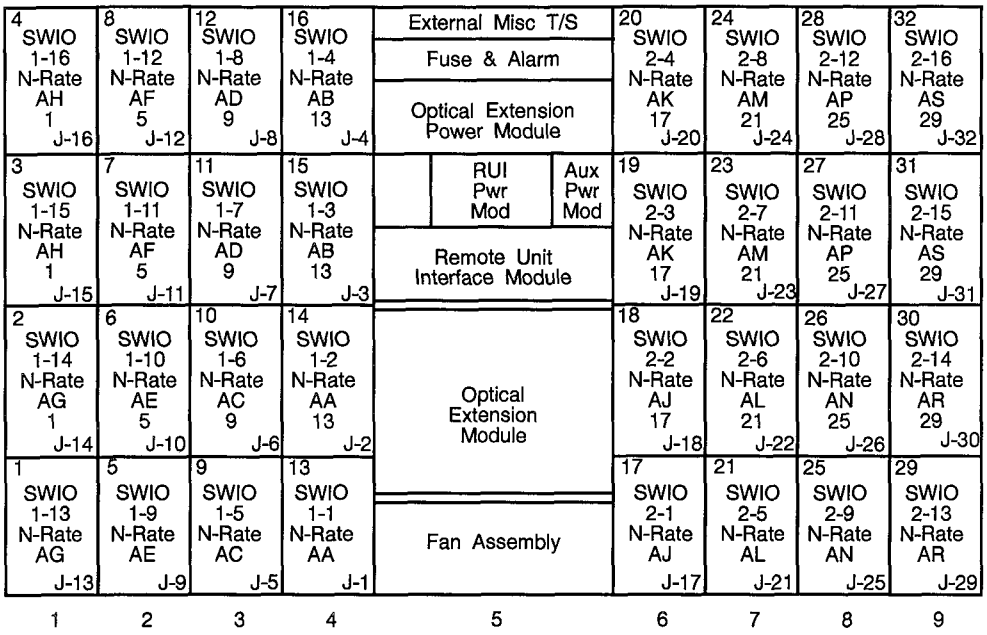
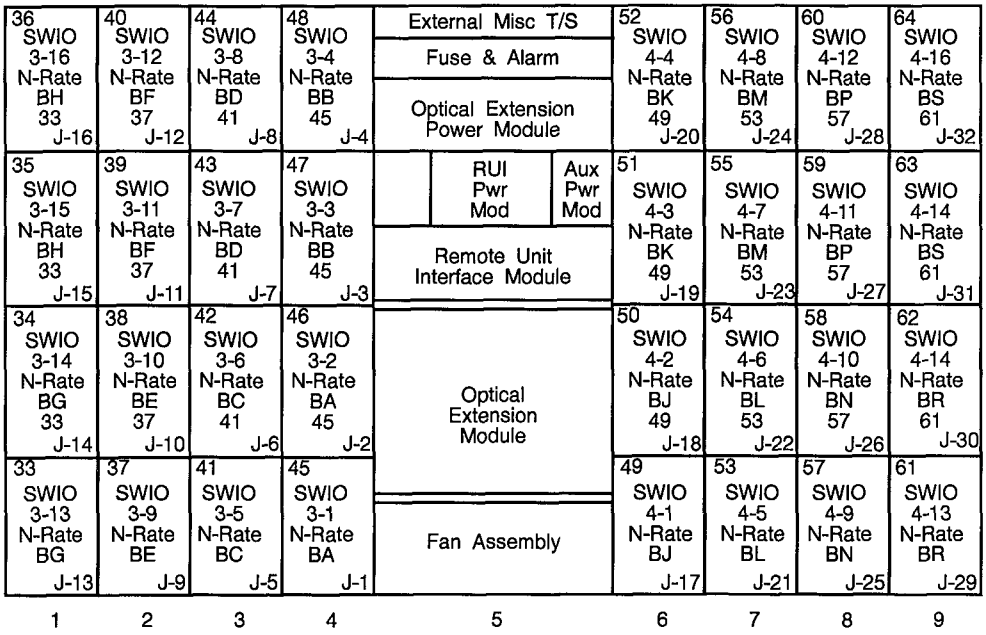



Figure 3-1. **Maximum DS1 Configuration (Collocated)**




Remote Complex 1 (RX-1) Bay Position (Units 1-32)




Remote Complex 2 (RX-2) Bay Position (Units 33-64)

Figure 3-2. **Maximum DS1 Configuration (Remote Complexes)**

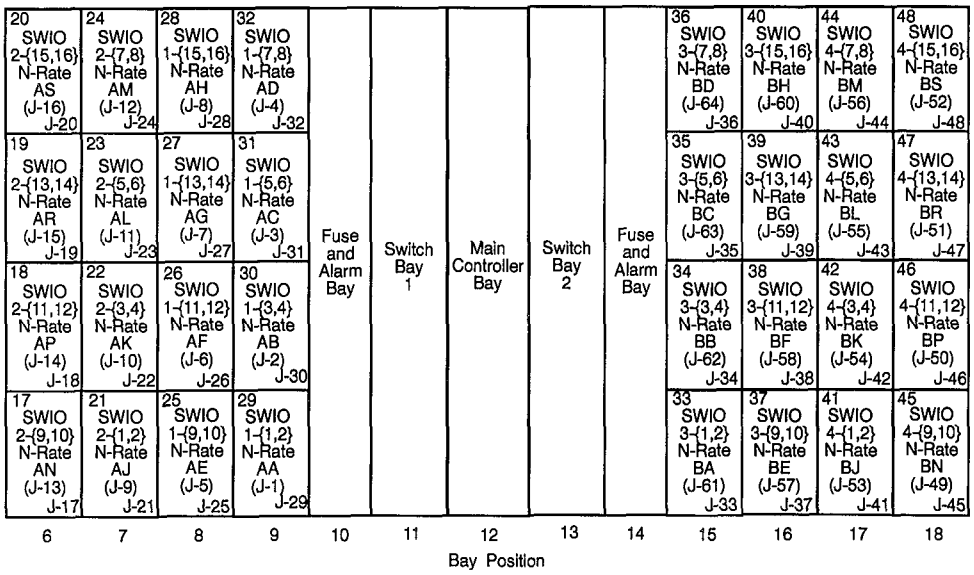



Figure 3-3. **Maximum DS3 Interface-16 Configuration (Collocated)**

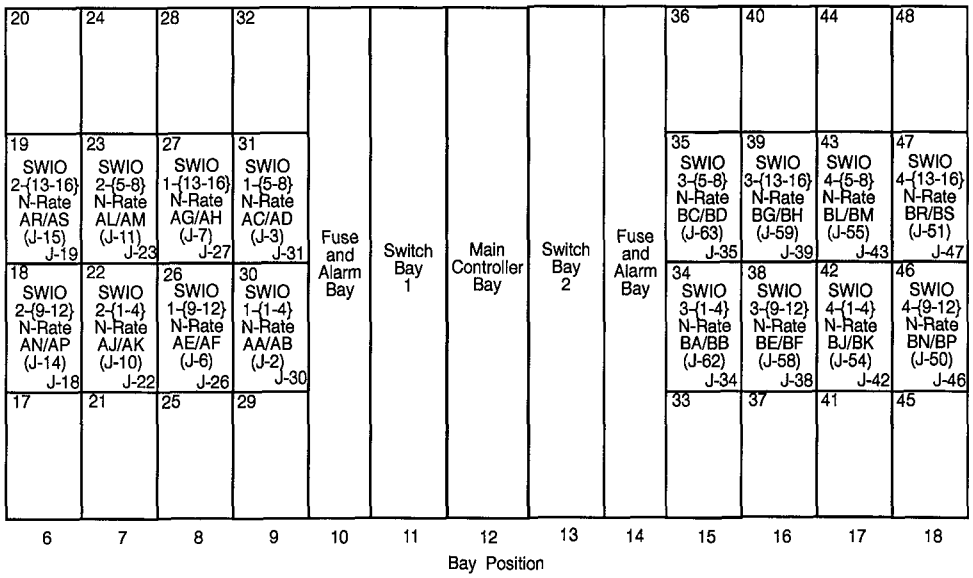
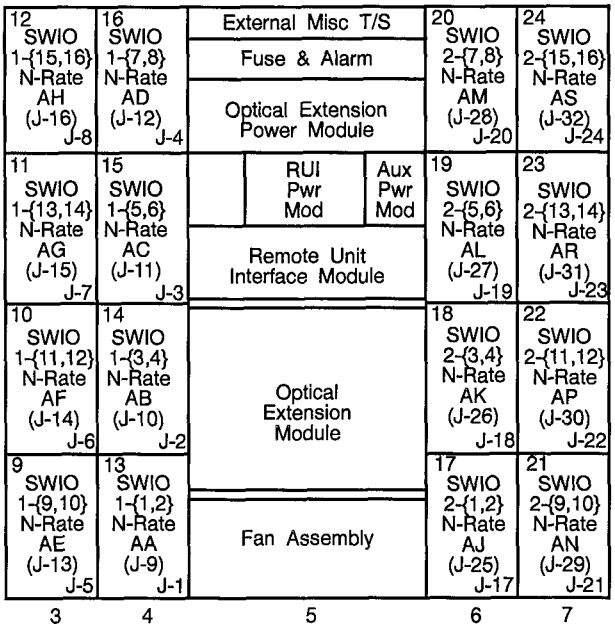
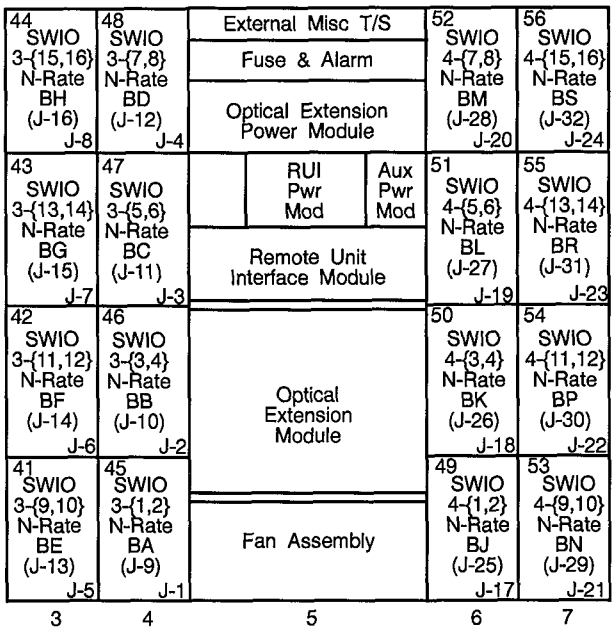



Figure 3-4. **Maximum DS3 Interface-32 Configuration (Collocated)**




Remote Complex 1 (RX-1) Bay Position (Units 1-32)




Remote Complex 2 (RX-2) Bay Position (Units 33-64)

Figure 3-5. **Maximum DS3 or STS1 Interface-16 Configuration (Remote Complexes)**

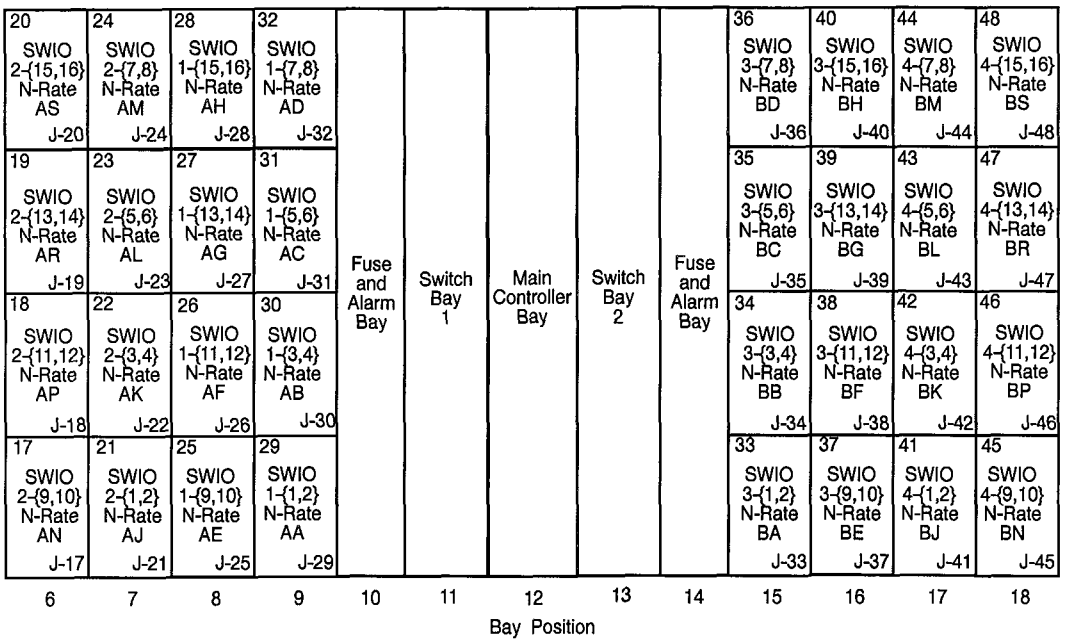



Figure 3-6. **Maximum STS1 Interface-16 Configuration (Collocated)**

# Bay Types

The different bay types that make up the DACS IV-2000 (512) Release 5.0 are described in the following sections.

## Main Controller Bay

The Main Controller (MC) Bay (Figure 3-7) contains three Switch Power (SW PWR) Modules, the High-Capacity Controller (HCC) Module, the Memory Storage (MEM) Module, the Synchronizer (SYNC) Module, the Status Panel, and a Fan Assembly. The Main Controller Bay and the two Switch Bays form the Switch Complex of the DACS IV-2000 (512), and are therefore required for all system configurations.

For Release 5.0 systems with at least one Remote Complex, the HCC Module and Switch Power Modules 1 and 3 require new circuit packs (or circuit pack replacements) to support optical remoting of the Remote Complexes.

Fuse protection is provided by the Fuse and Alarm panel in the Switch Bays.

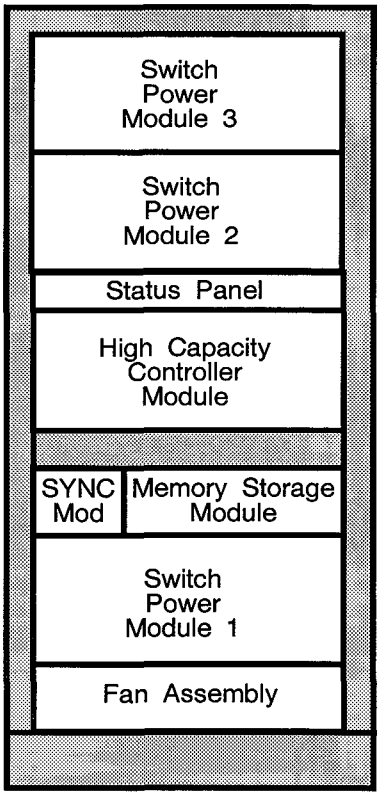


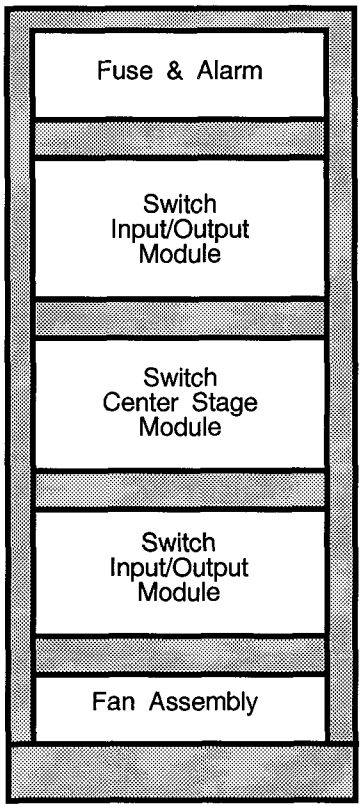

Figure 3-7. **Main Controller Bay**

## Switch Bay

The Switch (SW) Bay (Figure 3-8) contains two Switch Input/Output (SWIO) Modules, the Switch Center Stage (SWCS) Module, the Fuse and Alarm (FS & ALM) panel, and a Fan Assembly. The two Switch Bays and the Main Controller Bay form the Switch Complex of the DACS IV-2000 (512), and are therefore required for all system configurations.

For Release 5.0 systems with at least one Remote Complex, the SWIO shelves require new OSWIO circuit packs or circuit pack replacements to support Capacity Expansion frames and/or Optical Remoting.

Fuse protection is provided by the Fuse and Alarm panel, which provides -48V battery feeder termination and primary fusing. The -48V power feeds are then distributed to the Power Modules within the Main Controller Bay. The TTY circuit connections are located on the back of the Fuse and Alarm panel on these bays.




Front View

Figure 3-8. **Switch Bay**

## Optical Extension (OPEX) Bay

The OPEX Bay contains: the OPEX Power, Remote Unit Interface (RUI), RUI Power, AUX Power, and OPEX Modules, a Fuse and Alarm Panel, and a Fan Assembly (Figure 3-9). The OPEX Bay extends the N-rate signals from the interface bays onto fiber-optic cables to the SWIO Modules in the Switch Complex. The fiber-optic cables terminate on Optical Switch Input/Output (OSWIO) circuit packs on the (512) Switch Bay end.

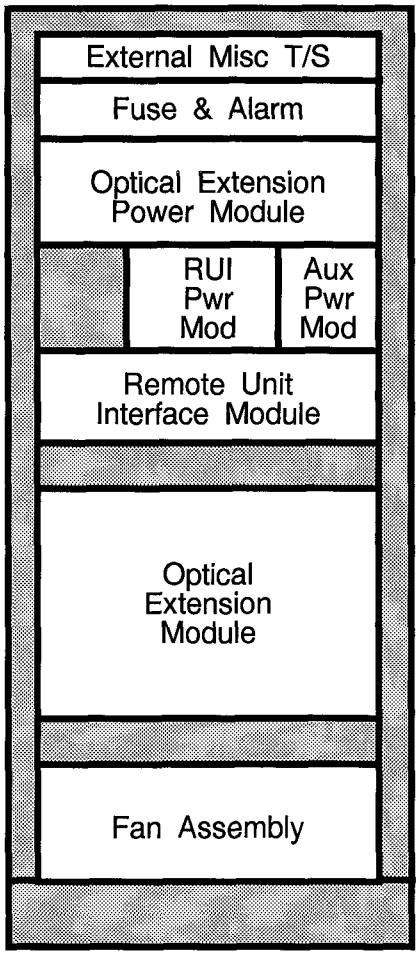
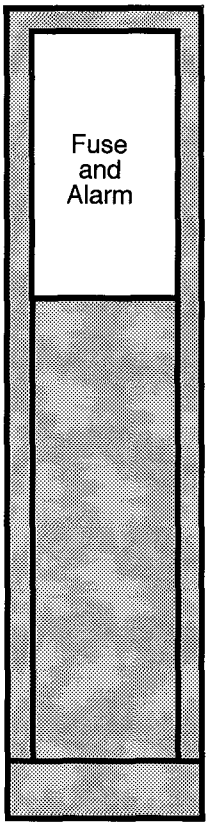



Figure 3-9. **Remote Complex Optical Extension Bay**

## Fuse and Alarm Bay

The Fuse and Alarm Bay (Figure 3-10) contains a fuse and alarm panel to accommodate up to four facility collocated interface bays. It also contains storage space for power cables, N-rate cables, and other cables running between the Switch Bays and facility interface bays. The Fuse and Alarm Bay provides fuse protection for the four adjacent interface bays.




Front View

Figure 3-10. **Fuse and Alarm Bay**

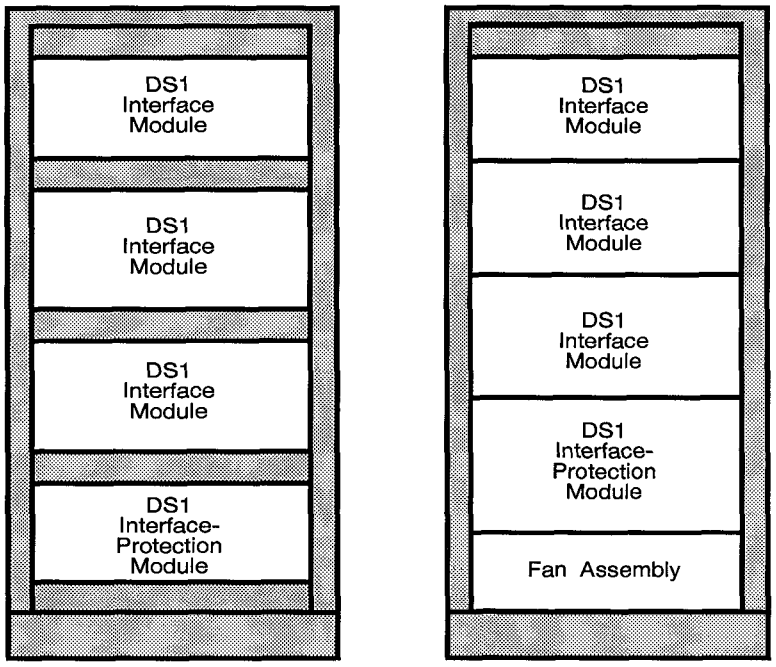
## DS1 Interface Bay

The DS1 Interface Bay (Figure 3-11) contains three DS1 Interface Modules and one DS1 Interface-Protection Module. The DS1 Interface-Protection Module interfaces with up to 196 DS1 signals and each DS1 Interface Module interfaces with up to 224 DS1 signals. Consequently, each DS1 Interface Bay provides a capacity of up to 868 DS1 signals (31 equivalent DS3 signals). However, each PMGR1 circuit pack used for performance monitoring reduces the capacity by 28 DS1 signals.

Circuit protection for the DS1 Interface Bay is provided by the DS1 Interface-Protection Module. This module provides protection for itself and up to three additional DS1 Interface Modules. Protection for the bay is on a 1-to-31 basis.

Fuse protection is provided by an associated Fuse and Alarm Bay for collocated interface modules, or by the fuse and alarm panel of the OPEX Bay in a Remote Complex.

The Enhanced DS1 Interface Bay is functionally identical to the DS1 Interface Bay except that cooling is provided by the Fan Assembly instead of free convection and the seismic bay framework is provided in the enhanced bay.




**A. DS1** **B. Enhanced DS1**

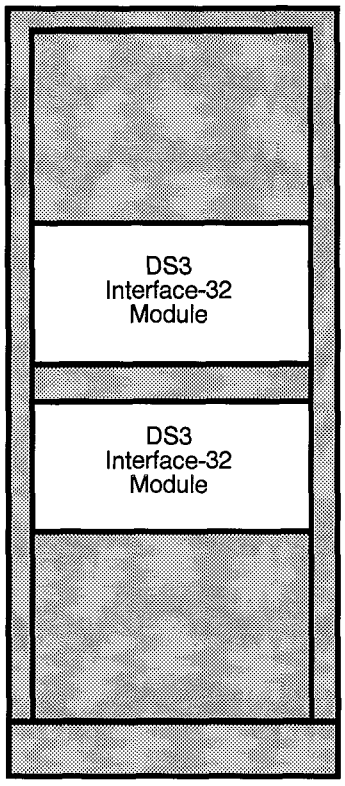
Figure 3-11. **DS1 and Enhanced DS1 Interface Bay**

## DS3 Interface Bay

The DS3 Interface Bay (Figure 3-12) contains two DS3 Interface-32 Modules. Each DS3 Interface-32 Module can be equipped to interface with up to 31 DS3 signals. Each bay provides a capacity of up to 62 DS3 signals (1736 DS1 equivalent signals). However, each PMGR1 circuit pack used for performance monitoring reduces the capacity by one DS3 signal.

Circuit protection for the DS3 Interface Bay is provided on an individual module basis. Each module provides protection for itself and the protection is done on a 1-to-31 basis.

Fuse protection is provided by an associated Fuse and Alarm Bay for collocated interface modules, or by the fuse and alarm panel of the OPEX Bay in a Remote Complex.




Front View

Figure 3-12. **DS3 Interface Bay**

## STS1/DS3 Interface Bay

The STS1/DS3 Interface Bay (Figure 3-13) contains four equipment shelves that can hold DS3, ENH DS3, DS3CC, or STS1 Interface-16 Modules. Each DS3 Interface-16 Module interfaces with up to 15 DS3 signals and each STS1 Interface-16 Module interfaces with up to 15 STS-1 signals. Each bay provides a capacity of up to 60 DS3 signals and/or STS-1 signals.

Circuit protection for the STS1/DS3 Interface Bay is provided on an individual module basis. Each module provides protection for itself and the protection is done on a 1-to-15 basis.

Fuse protection is provided by an associated Fuse and Alarm Bay for collocated units, or by the fuse and alarm panel of the OPEX Bay in a Remote Complex.

The Enhanced STS1/DS3 Interface Bay is functionally identical to the STS1/DS3 Interface Bay except that the seismic bay framework is provided in the enhanced bay.

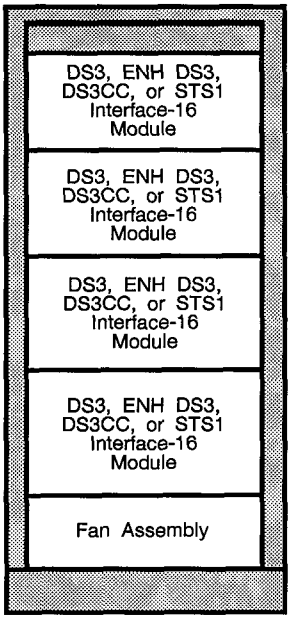



Figure 3-13. **STS1/DS3 and Enhanced STS1/DS3 Interface Bay**

## STS1/DS3/DS1 Interface Bay

The STS1/DS3/DS1 Interface Bay (Figure 3-14) contains one DS1 Interface Module, one DS1 Interface-Protection Module (for a total of 15 DS3 equivalents) plus up to 46 additional DS3 equivalents, as follows:

- The third shelf may contain a DS3 Interface-32 module or a DS3, Enhanced DS3, DS3CC, or STS1 Interface-16 module (31 or 15 DS3 equivalents)
- The fourth shelf may contain a DS3, Enhanced DS3, DS3CC, or STS1 Interface-16 module (15 DS3 equivalents).

The DS1 Interface and DS1 Interface-Protection Modules are identical to those in the DS1 Interface Bay and can be equipped to interface with up to 224 and 196 DS1 signals, respectively.

The DS3 Interface-32 Module can be equipped to interface with up to 31 DS3 signals.

The DS3, ENH DS3, or DS3CC Interface-16 Module can be equipped to interface with up to 15 DS3 signals, while the STS1 Interface-16 Module can be equipped to interface with up to 15 STS-1 signals.

Consequently, each STS1/DS3/DS1 Interface Bay provides a capacity of up to 46 DS3 signals and 420 DS1 signals (15 equivalent DS3 signals) when equipped with a DS3 Interface-32 Module, and a DS3, ENH DS3, or DS3CC Interface-16 Module. It can provide up to 31 DS3 signals, 15 STS-1 signals, and 420 DS1 signals when equipped with a STS1 Interface-16 Module.

It can provide up to 30 STS-1 signals, and 420 DS1 signals when equipped with a DS1 Interface and DS1 Interface-Protection Module and two STS1 Interface-16 Modules.

When using PMGR1 circuit packs for DS1 performance monitoring, each PMGR1 circuit pack reduces the capacity by 28 DS1 signals in the DS1 Interface Modules or 1 DS3 signal in the DS3 Interface-32 or DS3 Interface-16 Modules. PMGR1 circuit packs cannot be used in STS1, ENH DS3, or DS3CC Interface-16 Modules.

Protection for the STS1/DS3/DS1 Interface Bay is provided in two ways:

- Protection for the DS3 and STS1 Interface Modules is on an individual module basis; the DS3 Interface-32 Module is protected on a 1-to-31 basis; and the DS3 and STS1 Interface-16 Module is protected on a 1-to-15 basis.
- The DS1 Interface-Protection Module provides protection for itself plus the DS1 Interface Module. This protection is provided on a 1-to-15 basis.

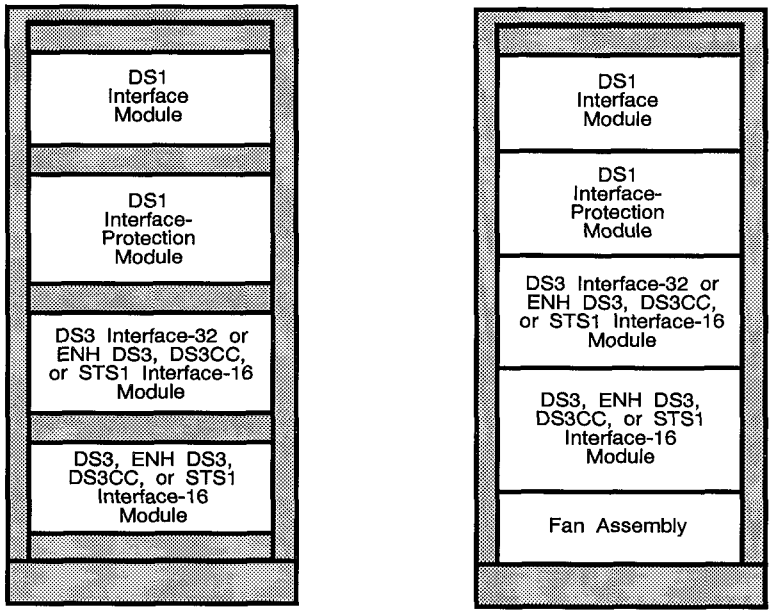



Figure 3-14. **STS1/DS3/DS1 and Enhanced STS1/DS3/DS1 Interface Bay**

Fuse protection is provided by an associated Fuse and Alarm Bay for collocated units, or by the fuse and alarm panel of the OPEX Bay in a Remote Complex.

The Enhanced STS1/DS3/DS1 Interface Bay is functionally identical to the STS1/DS3/DS1 Interface Bay except that cooling is provided by the Fan Assembly and the seismic bay framework is provided in the enhanced bay.

## Bay Configurations

The flexibility provided by the modular design of the DACS IV-2000 allows for different initial bay configurations based on traffic requirements. It can later be expanded to a number of possible bay layouts for a fully configured system. The following sections discuss configuration alternatives.

The four basic types of DACS IV-2000 interface bays enable you to create many possible bay layouts for a fully configured system. Note that the DS3 Interface Bay has been rated Discontinued Availability.

Figure 3-15 shows the three start-up configurations for the Switch Complex. Table 3-2 lists the capacity of each configuration shown in Figure 3-16. Figure 3-16 shows fully configured collocated systems and the typical order in which the systems are expanded. Figure 3-17 shows Remote Complex configurations.

When one Remote Complex is used, there are no interface bays to the left of the Switch Complex (that is, bay positions 1-10 are empty). When two Remote Complexes are used, the 512 bay line-up consists of only the Switch Complex (that is, bay positions 11-13 only). These configurations are not intended to limit the options, but rather represent the range of DS1 terminations, DS3 terminations, and Electrical Carrier-1 (EC-1)[1] terminations.

The DACS IV-2000 can be configured to accommodate changing DS1, DS3, and EC-1 facility needs over time under the cabling constraint that no more than 256 equivalent DS3s/STS-1s (including protection) can be connected on either side of the Switch Complex (two Switch Bays and a Main Controller Bay). Because of this cabling constraint, the Switch Complex is usually located at or near the center of the bay layout of a collocated configuration, as shown in Figure 3-16. A maximum of four STS1/DS3/DS1 Interface Bays, four DS3 Interface Bays or STS1/DS3 Interface Bays, or eight DS1 Interface Bays can be located on either side of the Switch Complex.

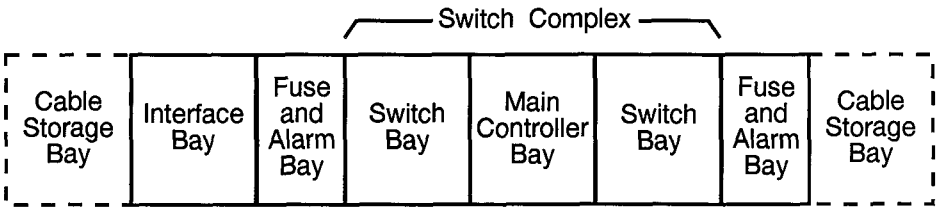
When planning the system layout, keep in mind that the capacity of a DS1 Interface Bay (32 equivalent DS3 signals) is one-half the capacity of an STS1/ DS3/DS1 Interface Bay or a DS3 Interface Bay.

**NOTE:**
A DS1 Interface Bay can be purchased separately, but must be installed in tandem with another DS1 Interface Bay before any other type interface bay can be added to the system.

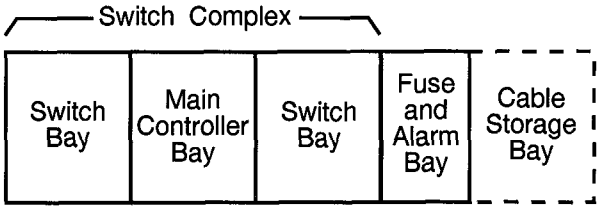
1. Electrical Carrier-1 (EC-1) is the industry standard nomenclature for an electrical STS-1 signal.

Table 3-2. **Interface Capacity for Sample System Configurations**

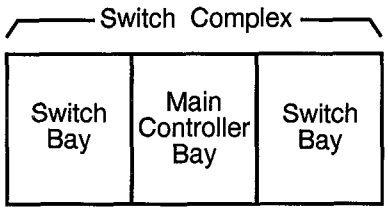
| Configuration Type From Figure 3-16 | STS1 Interface Capacity | DS3 Interface Capacity | DS1 Interface Capacity |
|---|---|---|---|
| STS1/DS3/DS1 | 300/0 | 124/424 | 1680 |
| STS1/DS3/DS1 | 90/0 | 186/276 | 5992 |
| STS1/DS3/DS1 | 60/0 | 124/184 | 8624 |
| STS1/DS3 | 480/0 | 0/480 | 0 |
| DS1 | 0 | 0 | 13,888 |




**A. Switch Complex with No Remote Complexes**




**B. Switch Complex with One Remote Complex**



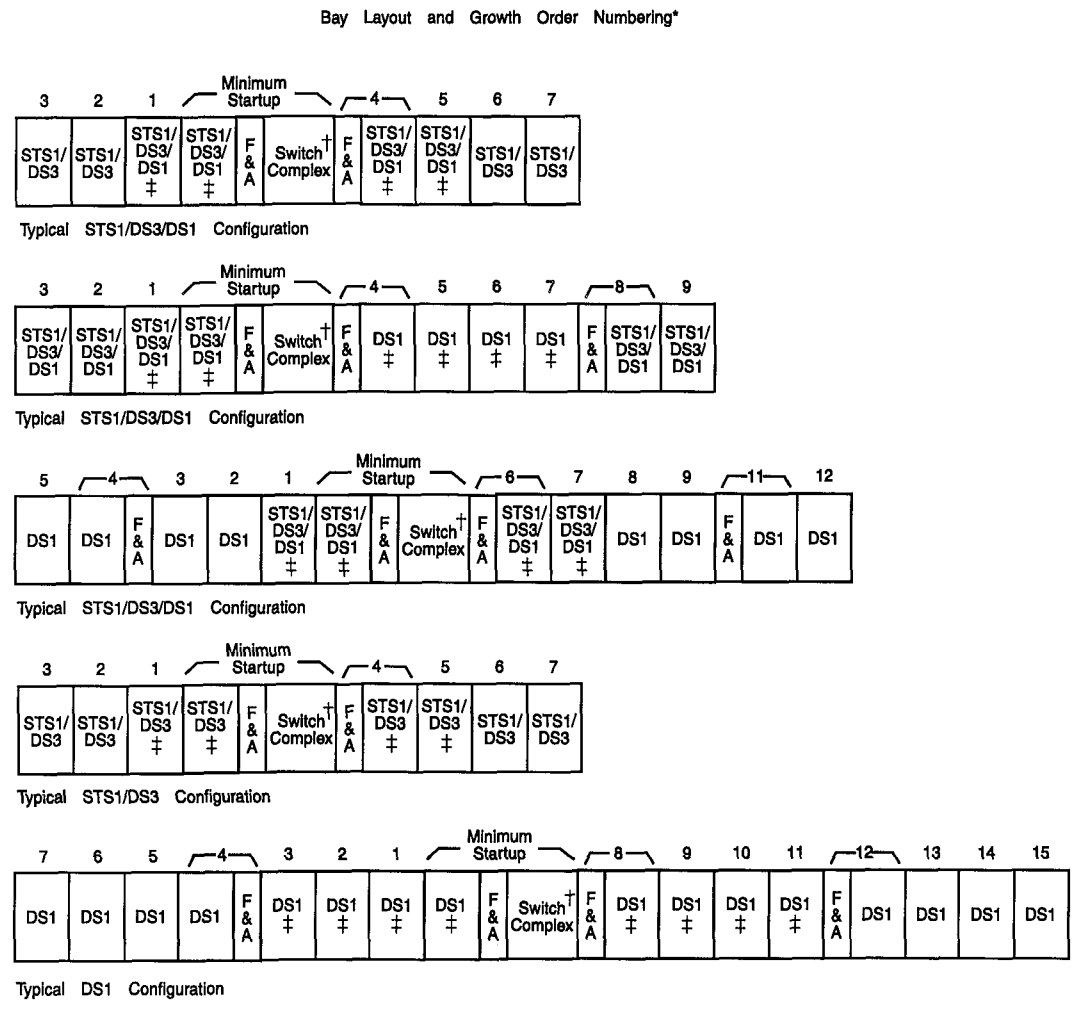

**C. Switch Complex with Two Remote Complexes**

Figure 3-15. **Generalized Minimum Start-up Configurations**

## Digital Systems Access Bay

For DS1 applications requiring 22 gauge (or larger) cable, consider using a Digital Systems Access Bay (DSAB) to eliminate potential cable congestion. For more information on the DSAB, refer to the *Digital Systems Access Bay (DSAB) System Reference Guide* (AT&T 365-301-135).

For DS1 applications in EMC installations, cable entering the system must be 26-gauge cable. If distance constraints require 22-gauge cable in the Central Office, DSAB bays are again recommended.

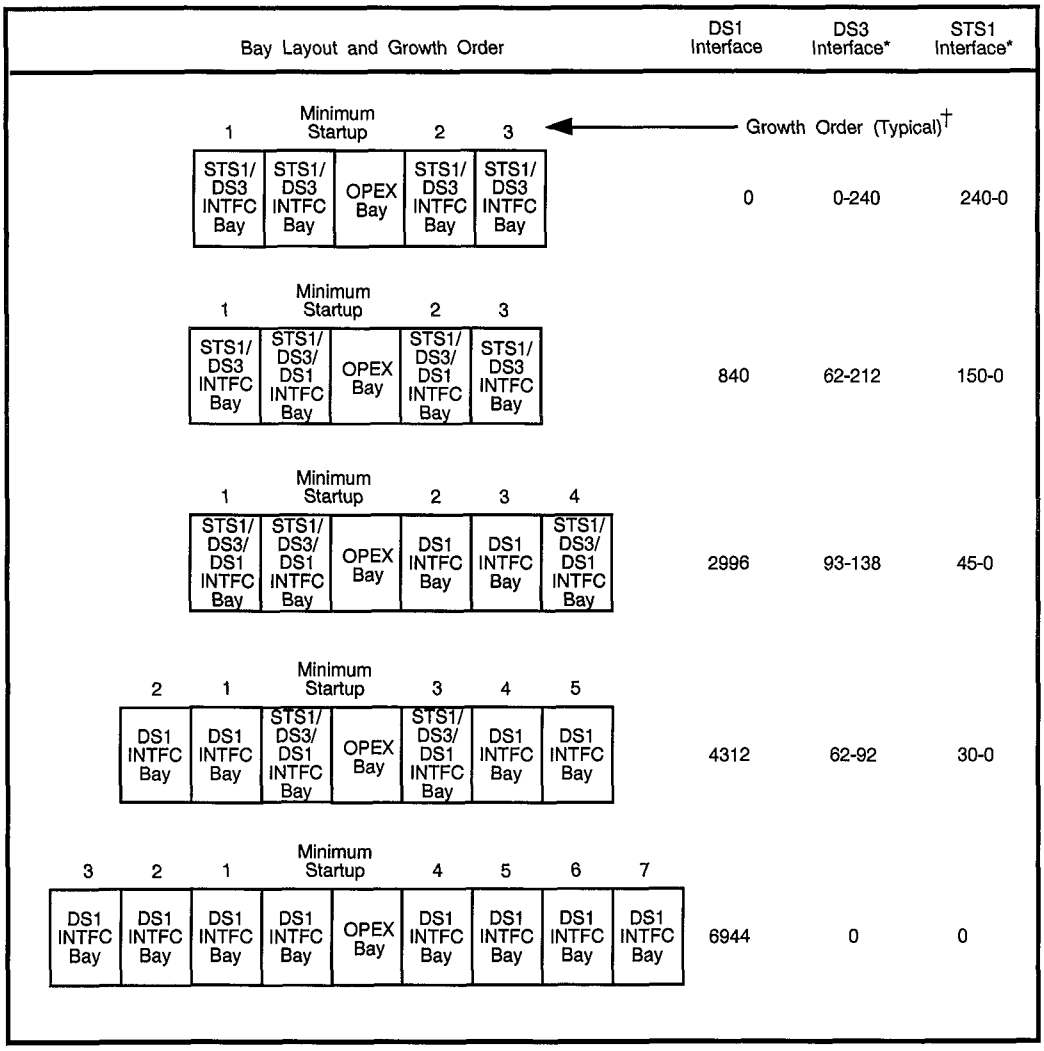



* Adjacent bays can be added to either the left or right side; the growth order shown is for typical growth.

† The Switch Complex is made up of one Main Controller Bay and two Switch Bays.

‡ Enhanced bays required for additional N-rate cables

Figure 3-16. **Sample System Configurations (Collocated Interface Bays)**




* The designation STS1/DS3/DS1 INTFC Bay indicates a standard configuration of 1 DS3 Interface-32, 1 DS3 Interface-16 or STS1 Interface-16, 1 DS1 Interface, and 1 DS1 Interface-Protection Module.

† Adjacent bays can be added to either the left or right side; the growth order shown is for typical growth.

Figure 3-17. **Sample System Configurations (Remote Complexes)**

## Recommended Arrangements

The following physical arrangements are recommended for best system performance.

### Bay Mounting

The DACS IV-2000 Main Controller, Switch, and Interface Bays are each 2 feet 2 inches wide, 7 feet high, and 12 inches deep.

- For a Switch Bay equipped with OSWIO circuit packs, bay-front-mounted fiber organizers are required; the nominal depth of a Switch Bay with optical fiber connections is 13 inches.
- The nominal depth of the EMC-enclosed Switch Bay with optical fiber connections is 14 inches.

The Main Controller, Switch Bay, and Enhanced Interface Bays use the seismic network bay framework. Equipment shelves mounted on these bays are factory installed. The only expansion that occurs is for additional circuit packs or growth bays.

The Optical Extension (OPEX) Bay is 7 feet high, and 2 feet, 2 inches wide. An OPEX Bay without an EMC enclosure is 14 inches deep. An OPEX Bay equipped with the optional EMC enclosure is 15 inches deep.

The Main Controller, Switch, OPEX, Enhanced DS1 Interface, STS1/DS3 Interface and Enhanced STS1/DS3/DS1 Interface Bays have forced-air cooling while the DS1 Interface, DS3 Interface, and STS1/DS3/DS1 Interface Bays are cooled by free convection. Bays equipped with a fan assembly take in air near the floor and exhaust it out the top rear of the bay.

Unequipped circuit pack slots are not permitted and must either contain a circuit pack or be covered with filler assemblies so that cooling air does not escape, but is directed upward through the bay. On bays without a fan assembly, heat baffles are used between the shelves on the interface bays to direct rising heat away from the circuit packs, located above. The initial configuration for:

- collocated systems consists of a Main Controller Bay, two Switch Bays, two Fuse and Alarm Bays, one interface bay, and two Cable Storage Bays. This initial configuration is 10 feet, 10 inches wide.
- one Remote Complex consists of a single DACS IV-2000 (256) frame that may have been in service and capacity-expanded to a DACS IV-2000 (512) frame. Any facilities that were intertied between the (256) and (512) systems are now available for additional capacity.
- two Remote Complexes consists of two DACS IV-2000 (256) frames and a DACS IV-2000 (512) Switch Complex. Either or both Remote Complexes may have been capacity-expanded to the (512) system.

The Cable Storage Bays, located at each end of a collocated lineup, are used to store and protect the cables until they are needed. All bays are bolted to the floor during installation. The interface bay required for the initial configuration is shipped separately.

# Minimum Start-up Configurations

Four initial bay configurations are available for the DACS IV-2000. Each consists of a Switch Complex (Main Controller Bay and two Switch Bays) and one of four interface bays. A particular start-up bay configuration depends on the type of terminations required, such as for STS-1 signals.

A DACS IV-2000 can be configured to accommodate any changing DS1, DS3, and EC-1 facility needs over time under the cabling constraint that not more than 256 equivalent STS1s/DS3s (including protection) be connected on either side of the Switch Complex. Because of this cabling constraint, the Switch Complex is usually located at or near the center of the bay layout. A maximum of four STS1/DS3/DS1 Interface Bays, or STS1/DS3 Interface Bays, or eight DS1 Interface Bays can be located on either side of the Switch Complex.

**NOTE:**
DS1 bays must be installed in pairs, side by side.

When using one Remote Complex, the suggested configuration is to arrange the collocated interface bays on the right side of the Switch Complex (bay positions 14 through 23) with no bays to the left (bay positions 1 through 10). When using two Remote Complexes, there are no bays to the left or right (bay positions 1 through 10 and 14 through 23) of the Switch Complex.

Upon initial shipment, Cable Storage Bays are provided at each end of the lineup to protect and store the unused cables until required. Unequipped interface bays are not provided in any configuration.

## DS3 Configuration

If only DS3 interfaces are required initially, the minimum configuration consists of a Switch Complex and an STS1/DS3 Interface Bay (Figure 3-18) equipped with four DS3 Interface-16 Modules. This configuration has an interface capacity of 60 DS3 signals (STS1/DS3 Interface Bay).

## STS1/DS3 Configuration

If only STS-1 interfaces are required initially, the minimum collocated configuration (Figure 3-18) consists of a Switch Complex and an STS1/DS3 Interface Bay equipped with four STS1 Interface-16 Modules. This configuration has an interface capacity of 60 STS-1 signals.

If a mix of STS-1 and DS3 interfaces is required, the bay configuration (Figure 3-18) consists of a Switch Complex and an STS1/DS3 Interface Bay equipped with STS1 and DS3 Interface-16 Modules totaling four. This configuration has an interface capacity of 60 STS-1 signals and/or DS3 signals.

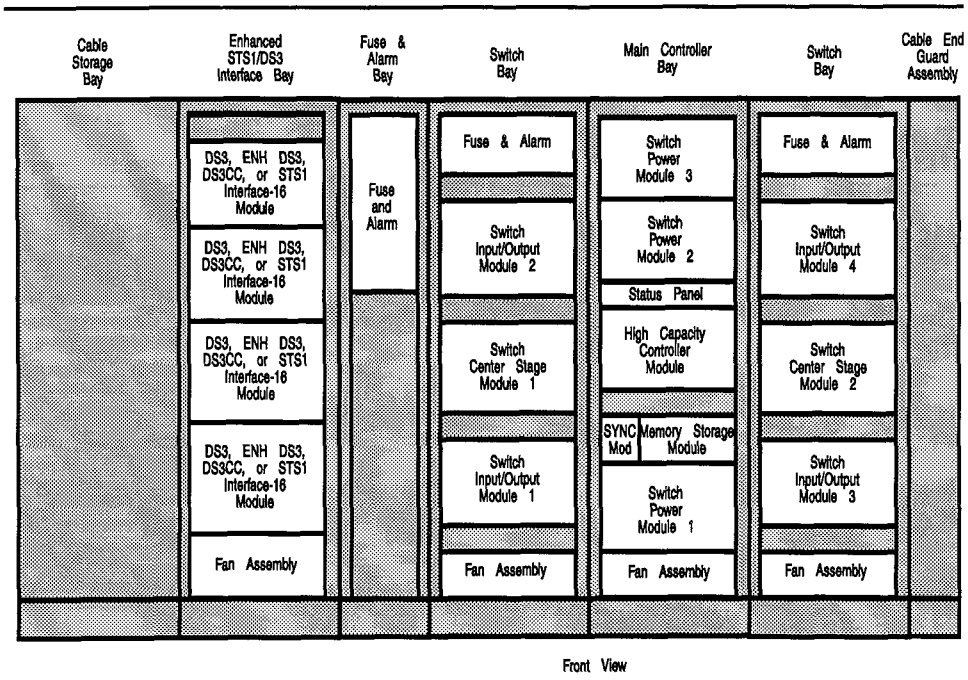



Figure 3-18. **Minimum Start-up Configuration for Collocated STS-1 or DS3 Interfaces Only (STS1/DS3 Interface Bay)**

Figure 3-19 shows the minimum configuration for the STS1/DS3 Remote Complex. The STS1/DS3 Remote configuration consists of an STS1/DS3 Interface Bay equipped with four STS1 Interface-16 Modules and one Switch Bay. This configuration has an interface capacity of 60 STS-1 signals.

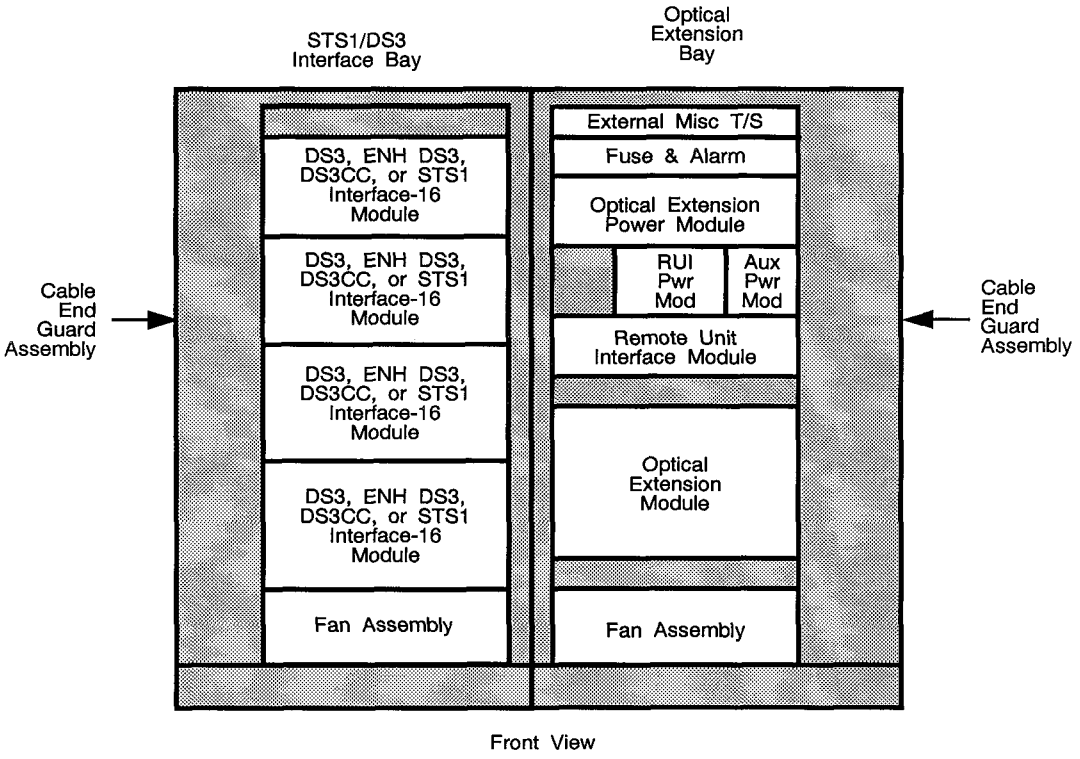



Figure 3-19. **Minimum Start-up Configuration for Remote Complex STS-1 or DS3 Interfaces Only (STS1/DS3 Interface Bay)**

## STS1/DS3/DS1 Configuration

If a mix of DS3 and DS1 interfaces is required, the minimum configuration (Figure 3-20) consists of a Switch Complex and an STS1/DS3/DS1 Interface Bay equipped with one DS1 Interface Module, one DS1 Interface-Protection Module, one DS3 Interface-32 Module and one DS3 Interface-16 Module. This configuration has an interface capacity of 46 DS3 signals and 420 DS1 signals.

If a mix of STS-1, DS3, and DS1 interfaces is required, the bay configuration (Figure 3-20) consists of a Switch Bay and an STS1/DS3/DS1 Interface Bay equipped with one DS1 Interface Module, one DS1 Interface-Protection Module, one DS3 Interface-32 Module and one STS1 Interface-16 Module. This configuration has an interface capacity of 15 STS-1 signals, 31 DS3 signals, and 420 DS1 signals.

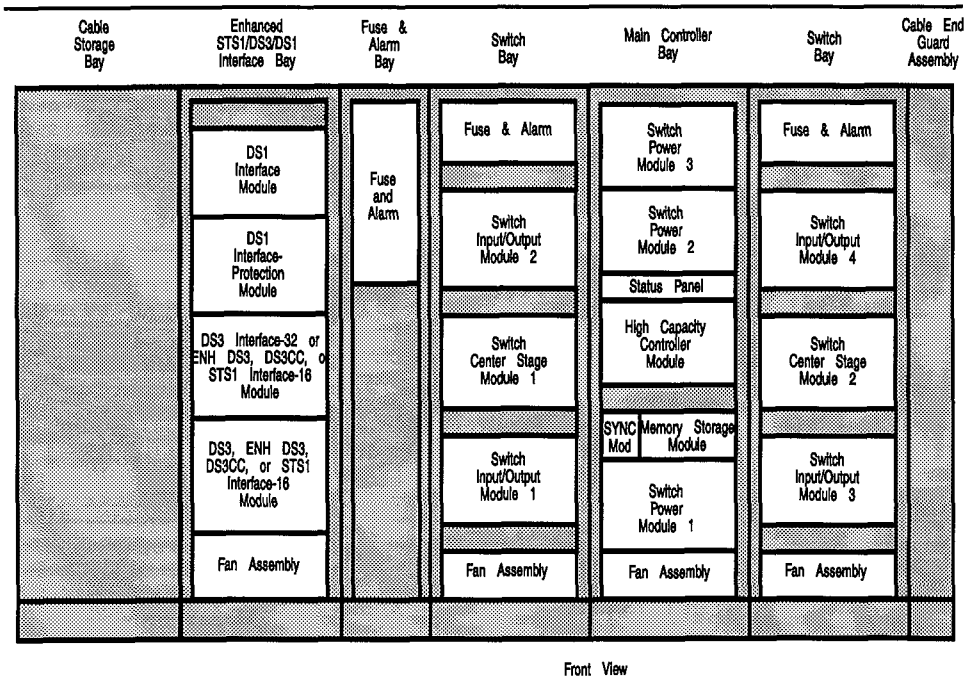



Figure 3-20. **Minimum Start-up Collocated Configuration for STS-1, DS3, and DS1 Interfaces**

Figure 3-21 shows the minimum configuration for the STS1/DS3 Remote Complex. This configuration consists of a Switch Bay and an STS1/DS3/DS1 Interface Bay equipped with one DS1 Interface Module, one DS1 Interface-Protection Module, one DS3 Interface-32 Module and one DS3 Interface-16 Module. This configuration has an interface capacity of 46 DS3 signals and 420 DS1 signals.

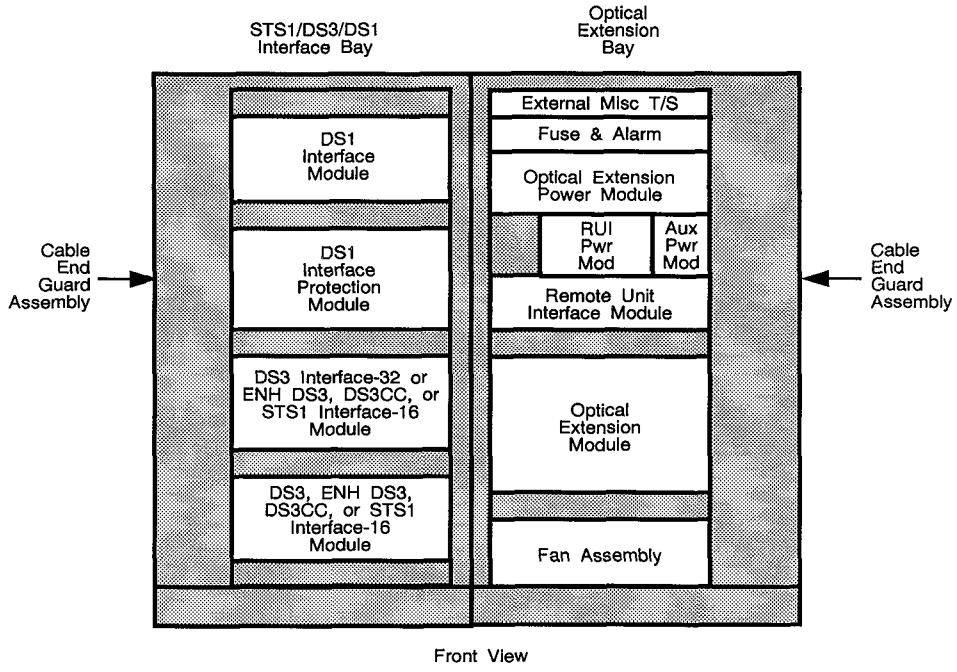



Figure 3-21. **Minimum Start-up Remote Configuration for STS-1, DS3, and DS1 Interfaces**

## DS1 Configuration

If only DS1 interfaces are required initially, the minimum bay configuration (Figure 3-22) consists of a Switch Complex, one Fuse and Alarm Bay, and a DS1 Interface Bay. This configuration has an interface capacity of 868 DS1 signals.

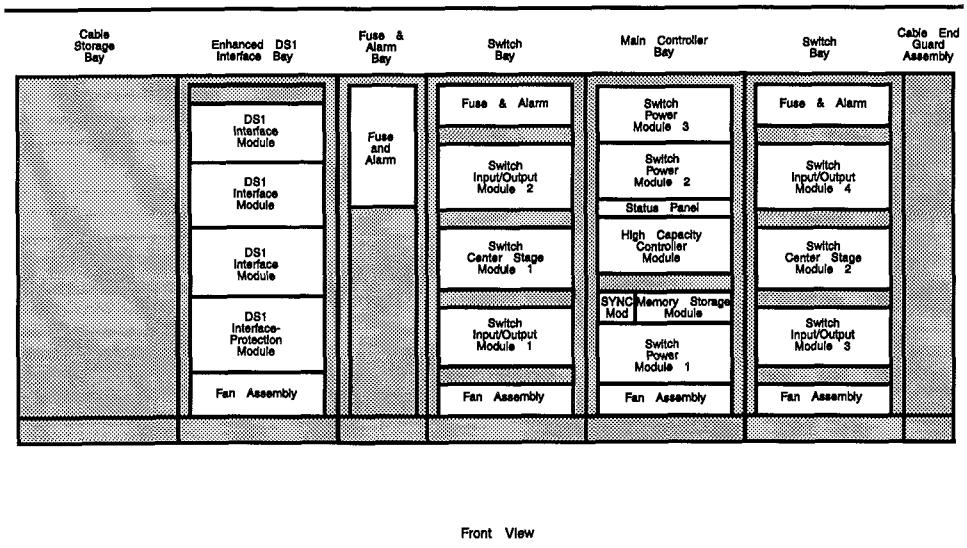



Figure 3-22. **Minimum Start-up Collocated Configuration for DS1 Interfaces Only**

The minimum Remote Complex configuration (Figure 3-23) consists of an OPEX Bay with a DS1 Interface Bay. This configuration has an interface capacity of 868 DS1 signals.

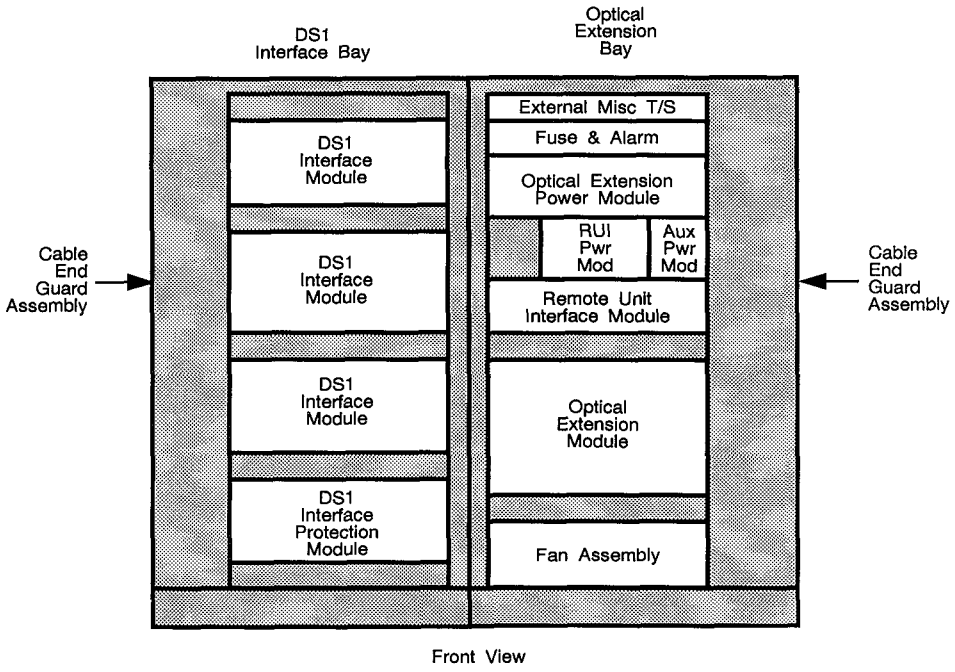



Figure 3-23. **Minimum Start-up Remote Complex Configuration for DS1 Interfaces Only**

# Interbay Cabling Arrangements

There are three types of interbay cables: N-rate, Control, and Fiber Optic cables.

- N-rate cables carry N-rate signals between the SWIO/OPEX Modules in the Switch/OPEX Bays and the interface modules in the interface bays.
- Control cables connect the unit controller (UC) circuit packs in the interface modules to the SWIO circuit packs in the Switch Bays.
- Fiber optic cables extend the N-rate and controller functions from the Switch Complex to its associated Remote Complexes.

## N-rate Cables for Collocated Interface Bays

In a fully equipped frame, N-rate cables carry 4,096 N-rate signals between interface modules and the Switch Bays (1,024 service signals and 1,024 protection signals in each direction). A total of 512 cables is used for this purpose.

These cables are divided into 32 groups designated by letters running from AA through AS and BA through BS, omitting I, O, and Q. (In Remote Complexes the old labelling scheme is altered in the software to map into the (512) labelling scheme.) Each of the 32 groups contains 16 cables. Those in the AA group are labelled J1-AA, J2-AA, ..., J16-AA, for example. J1-AA through J8-AA serve SWIO-1-1, and J9-AA through J16-AA serve SWIO-1-2 (SWIO-1-1's mate circuit pack). Cables J1-AB through J16-AB serve SWIO-1-3 and SWIO-1-4, and so on to J1-BS through J16-BS which serve SWIO-4-15 and SWIO-4-16. Table 3-3 shows the N-rate cable group that serves each SWIO circuit pack.

Each N-rate cable carries eight data and two timing signals, either service or protection, to or from each of four MUX, four SMUX, or four SWIF circuit packs (eight 2-wire pairs) and two 2-wire pairs to carry a clock/synchronizing signal resulting in a total of ten 2-wire pairs per cable.

N-rate Cable groups labelled with the letter A connect to interface modules on the left side of the Switch Complex and N-rate Cable groups labelled with the letter B connect to interface modules on the right side of the Switch Complex as seen from the front of the frame. A DS3 Interface-32 Module requires two N-rate cable groups; a DS3 Interface-16 Module or STS1 Interface-16 requires one N-rate cable group; and two DS1 Interface Modules share an N-rate cable group. N-rate cable group AA connects to the lowest module on the interface bay (Bay 9) closest to the Switch Complex, and the other N-rate cable groups run alphabetically upward and outward from the Switch Complex. N-rate cable groups labelled BA serve the interface bays on the right side of the Switch Complex in a similar fashion.

Table 3-3. SWIO N-Rate Cable Connections (Collocated Interface Bays)

| N-rate Cable Group | SWIO Circuit Packs | | N-rate Cable Group | SWIO Circuit Packs | |
|---|---|---|---|---|---|
| | Cables J1-An — J8-An | Cables J9-An — J16-An | | Cables J1-Bn — J8-Bn | Cables J9-Bn — J16-Bn |
| AA | 1-1 | 1-2 | BA | 3-1 | 3-2 |
| AB | 1-3 | 1-4 | BB | 3-3 | 3-4 |
| AC | 1-5 | 1-6 | BC | 3-5 | 3-6 |
| AD | 1-7 | 1-8 | BD | 3-7 | 3-8 |
| AE | 1-9 | 1-10 | BE | 3-9 | 3-10 |
| AF | 1-11 | 1-12 | BF | 3-11 | 3-12 |
| AG | 1-13 | 1-14 | BG | 3-13 | 3-14 |
| AH | 1-15 | 1-16 | BH | 3-15 | 3-16 |
| AJ | 2-1 | 2-2 | BJ | 4-1 | 4-2 |
| AK | 2-3 | 2-4 | BK | 4-3 | 4-4 |
| AL | 2-5 | 2-6 | BL | 4-5 | 4-6 |
| AM | 2-7 | 2-8 | BM | 4-7 | 4-8 |
| AN | 2-9 | 2-10 | BN | 4-9 | 4-10 |
| AP | 2-11 | 2-12 | BP | 4-11 | 4-12 |
| AR | 2-13 | 2-14 | BR | 4-13 | 4-14 |
| AS | 2-15 | 2-16 | BS | 4-15 | 4-16 |

## N-rate Cables for Remote Complex Interface Bays

In a fully-equipped Remote Complex Interface Bay, cables must carry 2048 N-rate signals between interface modules and the OPEX Bay (512 service signals and 512 protection signals in each direction for a total of 2048).

A total of 256 cables is used for this purpose. These cables are divided into 16 groups and designated by letters running from A through T, omitting I, O, Q, and S. Table 3-4 shows mappings of N-rate cable groups (A-T) that serve 256 frames to each Remote Complex (AA-AS and BA-BS) through the OPEX circuit packs. These mappings show how the Remote Complex equipment is addressed by the Switch Complex.

Each of the 16 groups contains 16 cables. These cables are labelled A through T, for example. J1-A through J8-A serve OPEX-{1,3}-1, and J9-A through J16-A serve OPEX-{1,3}-2 (OPEX-{1,3}-1 circuit pack's mate). Table 3-4 contains the N-rate cable group that serves each OPEX circuit pack.

Table 3-4. 256 Frame to Remote Complex N-Rate/SWIO Mappings

| N-Rate Cable Group | | | SWIO/OSWIO/OPEX Assignment | | |
|---|---|---|---|---|---|
| 256 Frame | Remote Complex 1 | Remote Complex 2 | 256 Frame (SWIO) | Remote Complex1 (OSWIO/ OPEX) | Remote Complex2 (OSWIO/ OPEX) |
| A | AA | BA | 1/2 | 1-1/1-2 | 3-1/3-2 |
| B | AB | BB | 3/4 | 1-3/1-4 | 3-3/3-4 |
| C | AC | BC | 5/6 | 1-5/1-6 | 3-5/3-6 |
| D | AD | BD | 7/8 | 1-7/1-8 | 3-7/3-8 |
| E | AE | BE | 9/10 | 1-9/1-10 | 3-9/3-10 |
| F | AF | BF | 11/12 | 1-11/1-12 | 3-11/3-12 |
| G | AG | BG | 13/14 | 1-13/1-14 | 3-13/3-14 |
| H | AH | BH | 15/16 | 1-15/1-16 | 3-15/3-16 |
| J | AJ | BJ | 17/18 | 2-1/2-2 | 4-1/4-2 |
| K | AK | BK | 19/20 | 2-3/2-4 | 4-3/4-4 |
| L | AL | BL | 21/22 | 2-5/2-6 | 4-5/4-6 |
| M | AM | BM | 23/24 | 2-7/2-8 | 4-7/4-8 |
| N | AN | BN | 25/26 | 2-9/2-10 | 4-9/4-10 |
| P | AP | BP | 27/28 | 2-11/2-12 | 4-11/4-12 |
| R | AR | BR | 29/30 | 2-13/2-14 | 4-13/4-14 |
| T | AS | BS | 31/32 | 2-15/2-16 | 4-15/4-16 |

Since 2048 N-rate signals are handled, each of the 256 cables must carry eight N-rate signals. Each cable also contains two-wire pairs to carry a clock/ synchronizing signal so that each cable contains 20 wires. Any given cable serves four SWIF, four MUX, four SMUX circuit packs, carrying two N-rate signals, either service or protection, to or from each circuit pack.

N-rate Cable groups A through H connect to interface modules on the left side of the OPEX Bay and N-rate Cable groups J through T connect to interface modules on the right side of the OPEX Bay as seen from the front of the Remote Complex. A DS3 Interface-32 Module requires two N-rate cable groups; a DS3 Interface-16 or STS1 Interface-16 Module requires one N-rate cable group; and two DS1 Interface Modules share an N-rate cable group.

N-rate cable group A connects to the lowest module on the interface bay (Bay 4) closest to the OPEX Bay, and the other N-rate cable groups run alphabetically upward and outward from the OPEX Bay. N-rate cable group starting with J serve the interface bays on the right side of the OPEX Bay in a similar fashion.

## Control Cables for Collocated Interface Bays

The 64 control cables that connect the unit controllers to the Switch Bays are labelled J1 through J64. J1 through J32 serve the interface bays on the left side of the Switch Complex, and J33 through J64 serve the interface bays on the right side of the Switch Complex. Numbering of control cables corresponds to the numbering of interface modules (units) in that numbering starts at the bottom of Bay 1 and goes upward and to the right. Just as in the numbering of the 64 units, a number is assigned to each of the four available interface module positions even if some positions are not occupied. For example, a DS3 Interface-32 Module in Bay 9 would have cables J30 and J31 assigned and cables J29 and J32 unassigned.

As many as 32 DS3PM2 circuit packs can be used, one for each DS3 Interface-32 or Interface-16 Module. Numbering of the control cables to DS3PM2 circuit packs to the left of the Switch Complex starts at J1 and runs upward and outward through J16. DS3PM2 circuit pack control cable numbers to the right of the Switch Complex start at J49 with the DS3 Interface Module at the bottom unit position furthest from the Switch Complex and run upward and inward through J64.

These DS3PM2 circuit pack control cable designations are the same as some of the set used for unit controller control cables. However, there is no numbering conflict in a given frame because unit controller control cable designations J1 through J16 are used for Bays 1, 2, 3, and 4 and J49 through J64 are used for Bays 20, 21 22, and 23.

**NOTE:**
You can only use DS3PM circuit packs in collocated configurations.

For any given configuration of DS3 Interface Modules in the frame, a combination of Bays 1, 2, 3, 4, 20, 21, 22, and 23 is not present allowing the use of the associated UC control cables for the DS3PM2 circuit packs.

Table 3-5 shows the control cable assignment for each collocated interface module unit location.

Table 3-5. **Control Cable Assignments for Collocated Bays**

| Unit | Control Cable | Unit | Control Cable | Unit | Control Cable | Unit | Control Cable |
|---|---|---|---|---|---|---|---|
| 1 | J1 | 17 | J17 | 33 | J33 | 49 | J49 |
| 2 | J2 | 18 | J18 | 34 | J34 | 50 | J50 |
| 3 | J3 | 19 | J19 | 35 | J35 | 51 | J51 |
| 4 | J4 | 20 | J20 | 36 | J36 | 52 | J52 |
| 5 | J5 | 21 | J21 | 37 | J37 | 53 | J53 |
| 6 | J6 | 22 | J22 | 38 | J38 | 54 | J54 |
| 7 | J7 | 23 | J23 | 39 | J39 | 55 | J55 |
| 8 | J8 | 24 | J24 | 40 | J40 | 56 | J56 |
| 9 | J9 | 25 | J25 | 41 | J41 | 57 | J57 |
| 10 | J10 | 26 | J26 | 42 | J42 | 58 | J58 |
| 11 | J11 | 27 | J27 | 43 | J43 | 59 | J59 |
| 12 | J12 | 28 | J28 | 44 | J44 | 60 | J60 |
| 13 | J13 | 29 | J29 | 45 | J45 | 61 | J61 |
| 14 | J14 | 30 | J30 | 46 | J46 | 62 | J62 |
| 15 | J15 | 31 | J31 | 47 | J47 | 63 | J63 |
| 16 | J16 | 32 | J32 | 48 | J48 | 64 | J64 |

## Control Cables for Remote Complex Interface Bays

The 32 control cables that connect the unit controllers to the OPEX Bay are labelled J1 through J32. Table 3-6 shows the mappings of the control cables that served a (256) frame to control cable assignments for the Remote Complexes. J1 through J16 serve the interface bays on the left side of the OPEX Bay, and J17 through J32 serve the interface bays on the right side of the OPEX Bay. Numbering of control cables is similar to the letter assignments of N-rate cables in that numbering starts at the bottom of the interface bay (Bays 4 and 6) nearest the OPEX Bay and goes upward and outward. However, just as in the numbering of the 32 units, a number is assigned to each of the four available module positions even if some positions are not occupied. For example, a DS3 Interface-32 Module in Bay 4 would have cables J2 and J3 assigned and cables J1 and J4 unassigned.

Table 3-6. (256) Frame to Remote Complex Control Cable Assignment Mappings

| Unit Numbering | | | J-Cable Numbering | | |
|---|---|---|---|---|---|
| 256 Frame | Remote Complex 1 | Remote Complex 2 | 256 Frame | Remote Complex1 | Remote Complex2 |
| 1 | 1 | 33 | J13 | J13 | J13 |
| 2 | 2 | 34 | J14 | J14 | J14 |
| 3 | 3 | 35 | J15 | J15 | J15 |
| 4 | 4 | 36 | J16 | J16 | J16 |
| 5 | 5 | 37 | J9 | J9 | J9 |
| 6 | 6 | 38 | J10 | J10 | J10 |
| 7 | 7 | 39 | J11 | J11 | J11 |
| 8 | 8 | 40 | J12 | J12 | J12 |
| 9 | 9 | 41 | J5 | J5 | J5 |
| 10 | 10 | 42 | J6 | J6 | J6 |
| 11 | 11 | 43 | J7 | J7 | J7 |
| 12 | 12 | 44 | J8 | J8 | J8 |
| 13 | 13 | 45 | J1 | J1 | J1 |
| 14 | 14 | 46 | J2 | J2 | J2 |
| 15 | 15 | 47 | J3 | J3 | J3 |
| 16 | 16 | 48 | J4 | J4 | J4 |
| 17 | 17 | 49 | J17 | J17 | J17 |
| 18 | 18 | 50 | J18 | J18 | J18 |
| 19 | 19 | 51 | J19 | J19 | J19 |
| 20 | 20 | 52 | J20 | J20 | J20 |
| 21 | 21 | 53 | J21 | J21 | J21 |
| 22 | 22 | 54 | J22 | J22 | J22 |
| 23 | 23 | 55 | J23 | J23 | J23 |
| 24 | 24 | 56 | J24 | J24 | J24 |
| 25 | 25 | 57 | J25 | J25 | J25 |
| 26 | 26 | 58 | J26 | J26 | J26 |
| 27 | 27 | 59 | J27 | J27 | J27 |
| 28 | 28 | 60 | J28 | J28 | J28 |
| 29 | 29 | 61 | J29 | J29 | J29 |
| 30 | 30 | 62 | J30 | J30 | J30 |
| 31 | 31 | 63 | J31 | J31 | J31 |
| 32 | 32 | 64 | J32 | J32 | J32 |

## Fiber Optic Cables

In (512) systems configured with Remote Complex(es), network traffic is carried from the remote interface modules to the Switch Complex by fiber optic cables between the OSWIO circuit packs and the OPEX circuit packs. In addition, controller functions of the HCC Module are extended to the RUI Module by fiber optic cables between the OUI circuit packs and the UIA/UIB circuit packs.

Each OSWIO and OPEX circuit pack is equipped with a pair of fibers, with each fiber carrying traffic in one direction (either from the Remote Complex to the Switch Complex or from the Switch Complex to the Remote Complex). The fiber pairs terminate on OPEX circuit packs at the Remote Complex, and on OSWIO circuit packs at the Switch Complex. The addressing of the OSWIO and the OPEX circuit packs on each end uniquely identifies the pairs of fibers between these two circuit packs.

Each OUI circuit pack is equipped with four pairs of fibers, with each fiber carrying traffic in one direction (either from the Remote Complex to the Switch Complex or from the Switch Complex to the Remote Complex). One pair of fibers services a UIA or UIB circuit pack.

Each UIA and UIB circuit pack is equipped with two pairs of fibers, with each fiber carrying traffic in one direction (either from the Remote Complex to the Switch Complex or from the Switch Complex to the Remote Complex). One pair of fibers services an OUI circuit pack in one of the control complexes.

During the upgrade procedure, the physical circuit pack locations of the OPEX Module are renumbered for consistency with the OSWIO circuit packs in the SWIO Module. Table 3-7 shows the fiber-optic cable labels used in the DACS IV-2000.

Table 3-7. **Fiber-Optic Cable Labelling**

| Remote Complex 1 | | | Remote Complex 2 | | |
|---|---|---|---|---|---|
| **OSWIO End Label** | **(256) SWIO Location** | **OPEX End Label** | **OSWIO End Label** | **(256) SWIO Location** | **OPEX End Label** |
| OSWIO MOD 1-1 | 1 | OPEX MOD 1-1 | OSWIO MOD 3-1 | 1 | OPEX MOD 3-1 |
| OSWIO MOD 1-2 | 2 | OPEX MOD 1-2 | OSWIO MOD 3-2 | 2 | OPEX MOD 3-2 |
| OSWIO MOD 1-3 | 3 | OPEX MOD 1-3 | OSWIO MOD 3-3 | 3 | OPEX MOD 3-3 |
| OSWIO MOD 1-4 | 4 | OPEX MOD 1-4 | OSWIO MOD 3-4 | 4 | OPEX MOD 3-4 |
| OSWIO MOD 1-5 | 5 | OPEX MOD 1-5 | OSWIO MOD 3-5 | 5 | OPEX MOD 3-5 |
| OSWIO MOD 1-6 | 6 | OPEX MOD 1-6 | OSWIO MOD 3-6 | 6 | OPEX MOD 3-6 |
| OSWIO MOD 1-7 | 7 | OPEX MOD 1-7 | OSWIO MOD 3-7 | 7 | OPEX MOD 3-7 |
| OSWIO MOD 1-8 | 8 | OPEX MOD 1-8 | OSWIO MOD 3-8 | 8 | OPEX MOD 3-8 |
| OSWIO MOD 1-9 | 9 | OPEX MOD 1-9 | OSWIO MOD 3-9 | 9 | OPEX MOD 3-9 |
| OSWIO MOD 1-10 | 10 | OPEX MOD 1-10 | OSWIO MOD 3-10 | 10 | OPEX MOD 3-10 |
| OSWIO MOD 1-11 | 11 | OPEX MOD 1-11 | OSWIO MOD 3-11 | 11 | OPEX MOD 3-11 |
| OSWIO MOD 1-12 | 12 | OPEX MOD 1-12 | OSWIO MOD 3-12 | 12 | OPEX MOD 3-12 |
| OSWIO MOD 1-13 | 13 | OPEX MOD 1-13 | OSWIO MOD 3-13 | 13 | OPEX MOD 3-13 |
| OSWIO MOD 1-14 | 14 | OPEX MOD 1-14 | OSWIO MOD 3-14 | 14 | OPEX MOD 3-14 |
| OSWIO MOD 1-15 | 15 | OPEX MOD 1-15 | OSWIO MOD 3-15 | 15 | OPEX MOD 3-15 |
| OSWIO MOD 1-16 | 16 | OPEX MOD 1-16 | OSWIO MOD 3-16 | 16 | OPEX MOD 3-16 |
| OSWIO MOD 2-1 | 17 | OPEX MOD 2-1 | OSWIO MOD 4-1 | 17 | OPEX MOD 4-1 |
| OSWIO MOD 2-2 | 18 | OPEX MOD 2-2 | OSWIO MOD 4-2 | 18 | OPEX MOD 4-2 |
| OSWIO MOD 2-3 | 19 | OPEX MOD 2-3 | OSWIO MOD 4-3 | 19 | OPEX MOD 4-3 |
| OSWIO MOD 2-4 | 20 | OPEX MOD 2-4 | OSWIO MOD 4-4 | 20 | OPEX MOD 4-4 |
| OSWIO MOD 2-5 | 21 | OPEX MOD 2-5 | OSWIO MOD 4-5 | 21 | OPEX MOD 4-5 |
| OSWIO MOD 2-6 | 22 | OPEX MOD 2-6 | OSWIO MOD 4-6 | 22 | OPEX MOD 4-6 |
| OSWIO MOD 2-7 | 23 | OPEX MOD 2-7 | OSWIO MOD 4-7 | 23 | OPEX MOD 4-7 |
| OSWIO MOD 2-8 | 24 | OPEX MOD 2-8 | OSWIO MOD 4-8 | 24 | OPEX MOD 4-8 |
| OSWIO MOD 2-9 | 25 | OPEX MOD 2-9 | OSWIO MOD 4-9 | 25 | OPEX MOD 4-9 |
| OSWIO MOD 2-10 | 26 | OPEX MOD 2-10 | OSWIO MOD 4-10 | 26 | OPEX MOD 4-10 |
| OSWIO MOD 2-11 | 27 | OPEX MOD 2-11 | OSWIO MOD 4-11 | 27 | OPEX MOD 4-11 |
| OSWIO MOD 2-12 | 28 | OPEX MOD 2-12 | OSWIO MOD 4-12 | 28 | OPEX MOD 4-12 |
| OSWIO MOD 2-13 | 29 | OPEX MOD 2-13 | OSWIO MOD 4-13 | 29 | OPEX MOD 4-13 |
| OSWIO MOD 2-14 | 30 | OPEX MOD 2-14 | OSWIO MOD 4-14 | 30 | OPEX MOD 4-14 |
| OSWIO MOD 2-15 | 31 | OPEX MOD 2-15 | OSWIO MOD 4-15 | 31 | OPEX MOD 4-15 |
| OSWIO MOD 2-16 | 32 | OPEX MOD 2-16 | OSWIO MOD 4-16 | 32 | OPEX MOD 4-16 |
| **OUI End Label*** | **UIA/ UIB Location** | **UIA/UIB End Label*** | **OUI End Label*** | **UIA/ UIB Location** | **UIA/UIB End Label*** |
| RX1 OUI 0 (half)<br>RX1 OUI 1 (half) | UIA | CC-0 UIA<br>CC-1 UIA | RX2 OUI 0 (half)<br>RX2 OUI 1 (half) | UIA | CC-0 UIA<br>CC-1 UIA |
| RX1 OUI 0 (half)<br>RX1 OUI 1 (half) | UIB | CC-0 UIB<br>CC-1 UIB | RX2 OUI 0 (half)<br>RX2 OUI 1 (half) | UIB | CC-0 UIB<br>CC-1 UIB |

**Note:** Each fiber-optic cable label identifies a transmit and receive fiber-optic cable. The OUI circuit pack labels identify two sets of transmit and receive cables.

* The OUI circuit pack connection has four fiber-optic cables that are associated with both Remote Complexes. Two of the fiber-optic cables go to Remote Complex 1 and two fiber-optic cables go to Remote Complex 2.

# Module Numbering

The numbering convention used to identify modules within the DACS IV-2000 is from bottom to top and left to right. With the DACS IV-2000 (512), modules using this convention are the three Switch Power Modules, the Switch Input/Output Modules, the two Switch Center Stage Modules, and the 64 interface module shelves.

## Switch Complex Module Numbering

Figure 3-24 shows the numbering of the three Switch Power Modules, the four Switch Input/Output Modules, and the two Switch Center Stage Modules. In identifying these modules, the bottom to top and left to right numbering convention is followed.

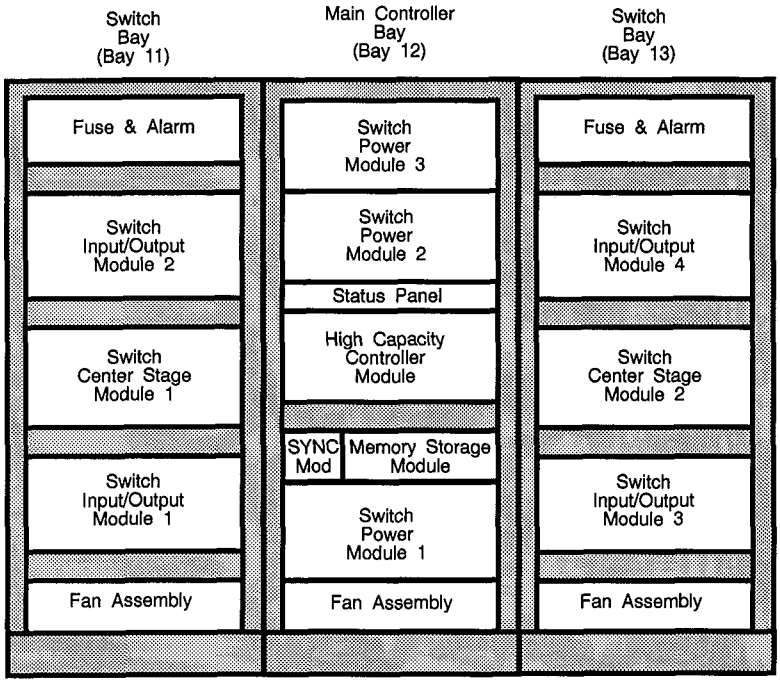



Figure 3-24. **Switch Complex Module Numbering**

## Interface Module (Unit) Numbering

In this section we describe the unit numbering conventions for collocated and remote interface modules. To provide a standard numbering convention for the DACS IV-2000, the complete bay lineup for the system is considered.

### Collocated Interface Bays

Figure 3-25 shows a 23-bay arrangement with each interface bay having four units (shelf positions). The numbering scheme assigns fixed unit numbers to the 64 possible shelf positions in a complete system. The type of module in a shelf position depends on the bay type. For example, an initial six-bay configuration of an STS1/DS3/DS1 Interface Bay, two Switch Bays, a Main Controller Bay, and two Fuse and Alarm Bays has four units. From bottom to top, these units are numbered 29 through 32. For DS3 Interface Bays, shelf positions 1 and 4 remain empty with no unit labels. For example, if an initial arrangement consists of a DS3 Interface Bay, the equipped shelves are units 30 and 31, while the unequipped shelves do not have unit labels.

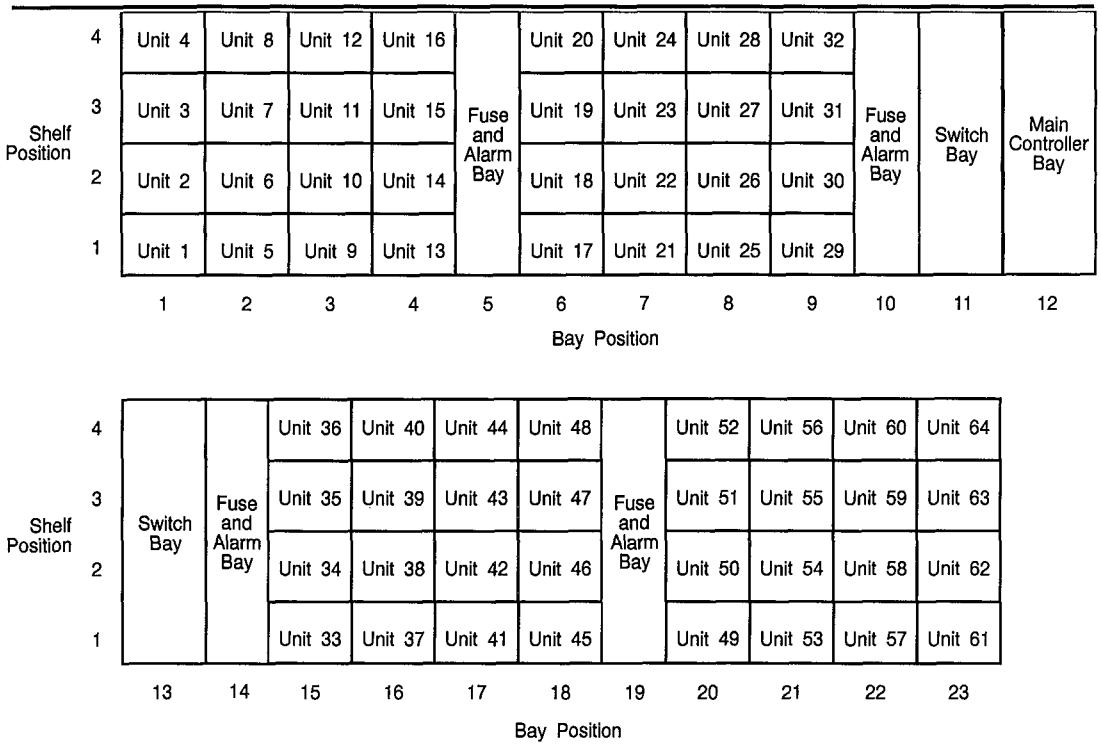



Figure 3-25. **Recommended Interface Module (Unit) Numbering (Collocated Interface Bays)**

## One Remote Complex

Figure 3-26 shows the bay arrangement with one Remote Complex, the Switch Complex, and its associated collocated interface bays. Each interface bay has four units (shelf positions). The numbering scheme assigns fixed unit numbers to the 64 possible shelf positions in a complete system. The type of module in a shelf position depends on the bay type. Note that the unit numbering begins on the Remote Complex, units 1-32. The unit numbering scheme continues with unit 33 being the first interface module collocated with the Switch Complex.

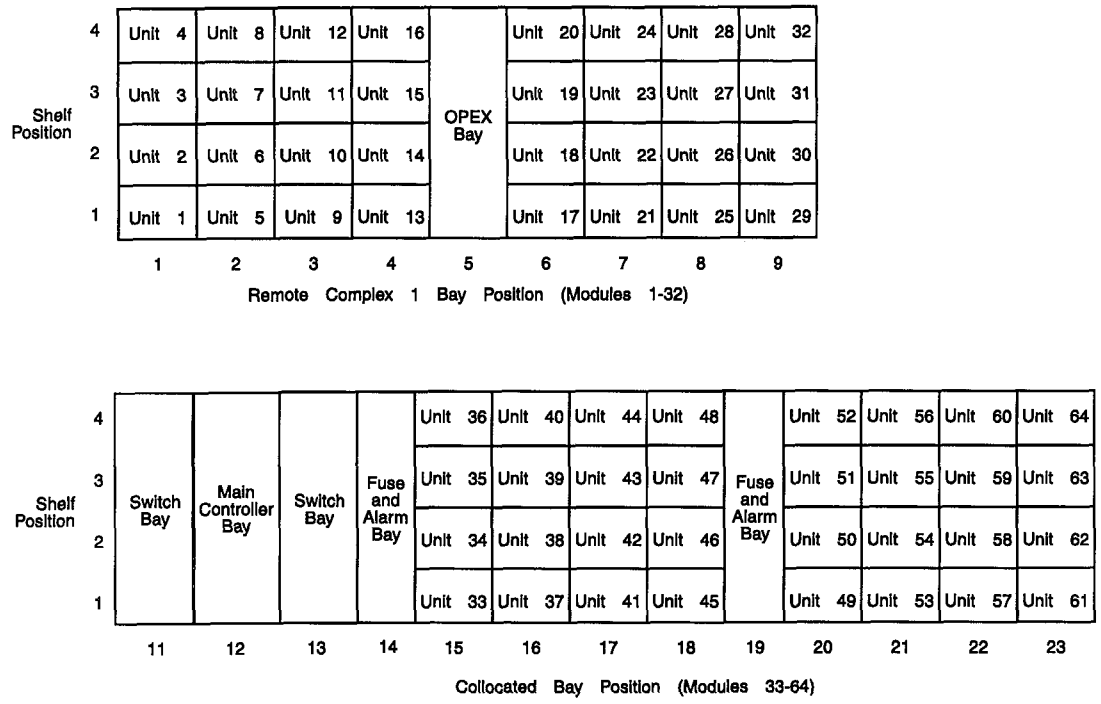



Figure 3-26. **Recommended Interface Module (Unit) Numbering (One Remote Complex)**

## Two Remote Complexes

Figure 3-27 shows the unit numbering scheme if you have a system with two Remote Complexes associated with the Switch Complex. The first remote complex (RX-1) contains units 1-32; the second Remote Complex (RX-2) contains units numbered 33-64.

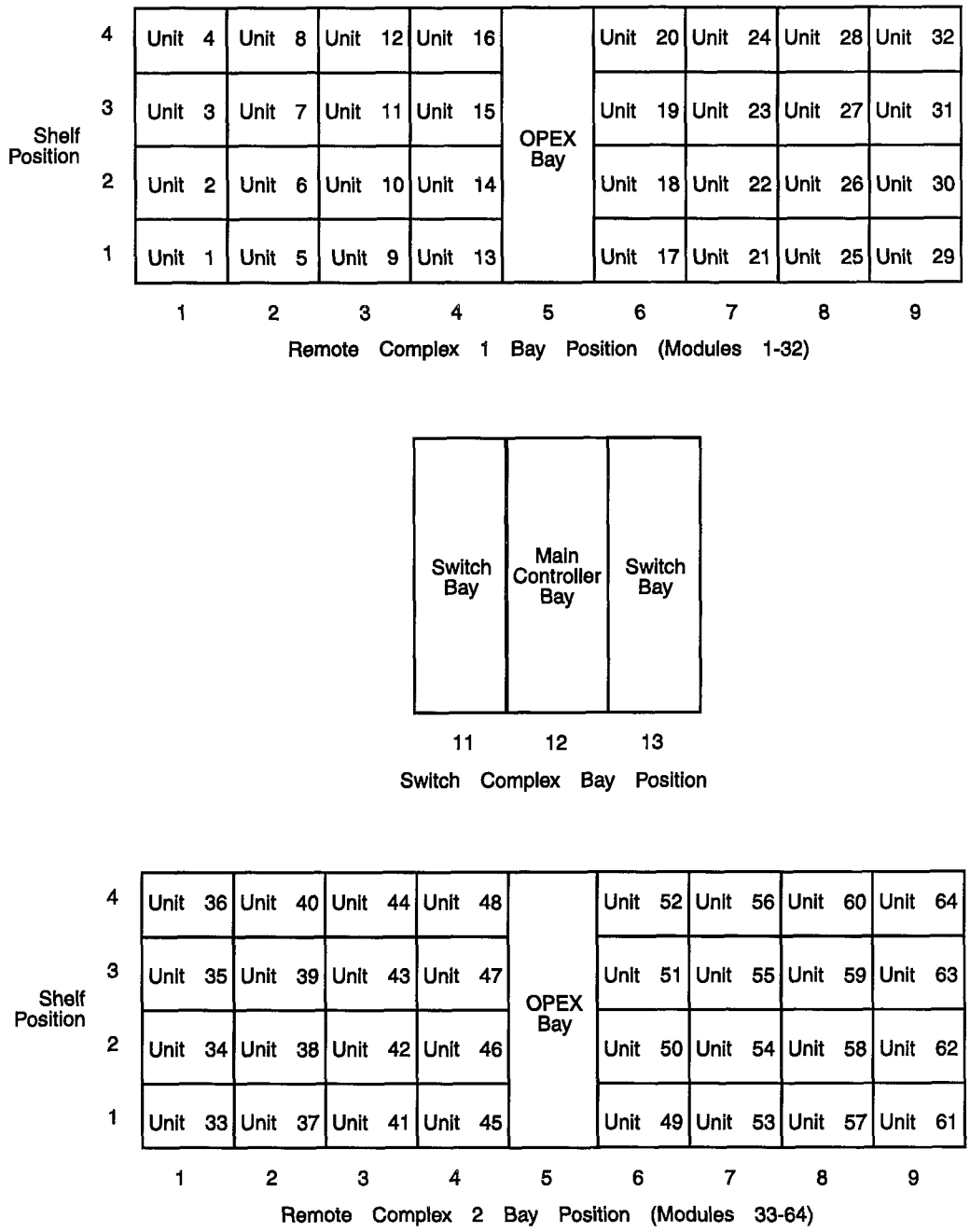



Figure 3-27. **Recommended Interface Module (Unit) Numbering (Two Remote Complexes)**

## Circuit Pack Numbering

The numbering convention used in a central office environment generally differs from the numbering convention used for the DACS IV-2000. The DACS IV-2000 facility numbering convention uses DS3 or STS-1 equivalents that correspond to a Multiplexer (MUX) circuit pack supporting one DS3, a SONET Multiplexer (SMUX) circuit pack supporting one STS-1, or a Switch Interface (SWIF) circuit pack supporting 28 DS1s. If the other end of a facility connected to the DACS IV-2000 connects to a DSX-3 or a DSX-1, it is difficult to reconcile the numbering conventions. The numbering convention uses the slot number in the interface module to designate a DS3, STS1, or a DS1. Table 3-8 shows the valid slot numbers in the DACS IV-2000 frame.

Table 3-8. **Valid Slot Number Conventions**

| Interface Module Type | Slot Number |
|---|---|
| STS1 Interface-16 | 1-15 |
| DS3 Interface-32 | 1-31 |
| DS3 Interface-16 | 1-15 |
| Enhanced DS3 Interface-16 | 1-15 |
| DS3 Clear-Channel Interface-16 | 1-15 |
| DS1 Interface | 1A,1B-8A,8B |
| DS1 Interface-Protection | 1A,1B-7A,7B |

Each slot in a DS3 Interface-32, DS3 Interface-16, Enhanced DS3 Interface-16, DS3 Clear-Channel Interface-16, or STS1 Interface-16 Module corresponds to one MUX/SMUX circuit pack. Each MUX/SMUX circuit pack allows for addressing of 28 DS1/VT1.5 signals within a DS3/STS-1 signal. For example, a DS3 facility terminating in a DS3 Interface Module located in unit 31 on the MUX circuit pack in slot 14 is numbered 31-14. The associated DS1 signals are numbered 31-14-1 through 31-14-28.

To form a DS3 equivalent (identified by the slot number), two DS1IF circuit packs are required. Each DS1IF is associated with 14 DS1 ports. Therefore, one of the DS1IF circuit packs is identified by an A appended to the slot number (addresses ports 1 through 14 of the equivalent DS3) and the other by a B appended to the slot number (addresses ports 15 through 28 of the equivalent DS3). For example, a DS1 facility terminating in a DS1 Interface Module located in unit 24 at slot 8B on port 20 of the DS1IF circuit pack is numbered 24-8-20.

In contrast to the above, a typical DSX numbering convention uses SRV (Service) to designate a DS3 group (28 DS1 signals) and CRT (Circuit) to designate individual DS1 signals within the group.

# Collocated Configuration Control Architecture

# 4

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# Collocated Configuration Control Architecture

# 4

This chapter describes information pertaining to the DACS IV-2000 (512) controller hardware associated with collocated interface bays. If you need information regarding controller hardware associated with Remote Complexes, refer to Chapter 5.

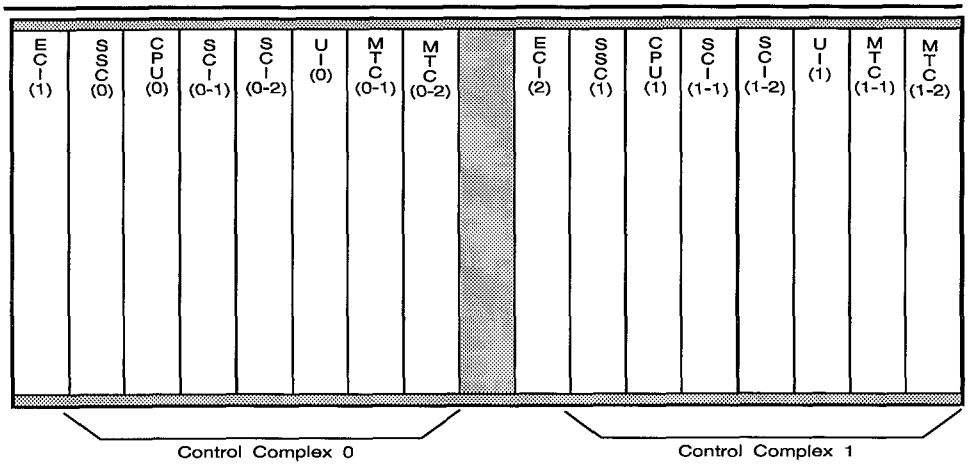
The control architecture for collocated interface bays comprises the following system modules (all contained in the Switch Complex):

- High-Capacity Controller (HCC) Module
- Memory Storage (MEM) Module
- Switch Input/Output (SWIO) Module
- Switch Center Stage (SWCS) Module
- Synchronizer (SYNC) Module
- Switch Power (SW PWR) Module.

Each of these modules, as they apply to collocated interface bays, is described in the sections that follow.

# High-Capacity Controller (HCC) and Memory Storage (MEM) Modules

The High-Capacity Controller (HCC) Module (Figure 4-1) manages the user interface (administrative links), performs user-specified functions, and coordinates database management with the Memory Storage Module, maintenance, and fault recovery operations. Table 4-1 lists the circuit packs contained in the High-Capacity Controller Module.



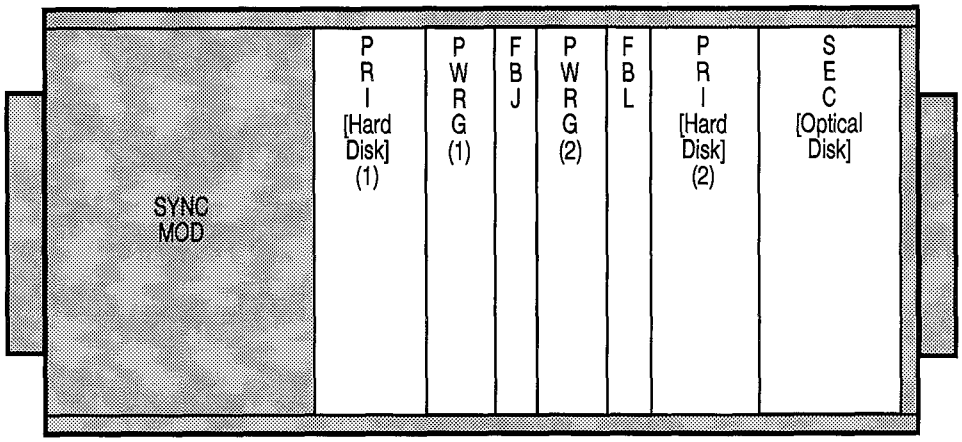

Note: Numbers in parentheses are circuit pack positions in module.

Figure 4-1. **High-Capacity Controller Module**

Table 4-1. **High-Capacity Controller Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| CPU3 | Central Processing Unit 3 | 2 |
| ECI6 | Enhanced Communications Interface 6 | 2 |
| MTC4 | Maintenance Interface 4 | 4 |
| SCI4 | Switch Communications Interface 4 | 4 |
| SSC4 | Secondary Storage Controller 4 | 2 |
| UI3 | Unit Interface 3 | 2 |

The Memory Storage Module (Figure 4-2) houses the secondary storage subsystem and its associated power and fuse block circuit packs. The secondary storage subsystem consists of three storage devices: two primary hard disks (PRI-1 and PRI-2) and a secondary optical disk (SEC). Table 4-2 lists the circuit packs contained in the Memory Storage Module.




Note: Numbers in parentheses are circuit pack positions in module.

Figure 4-2. **Memory Storage Module**

Table 4-2. **Memory Storage Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PRI4 | Primary 4 (Hard Disk) | 2 |
| SEC4 | Secondary 4 (Optical Disk) | 1 |
| PWRG | Power G | 2 |
| FBJ | Fuse Board J | 1 |
| FBL | Fuse Board L | 1 |

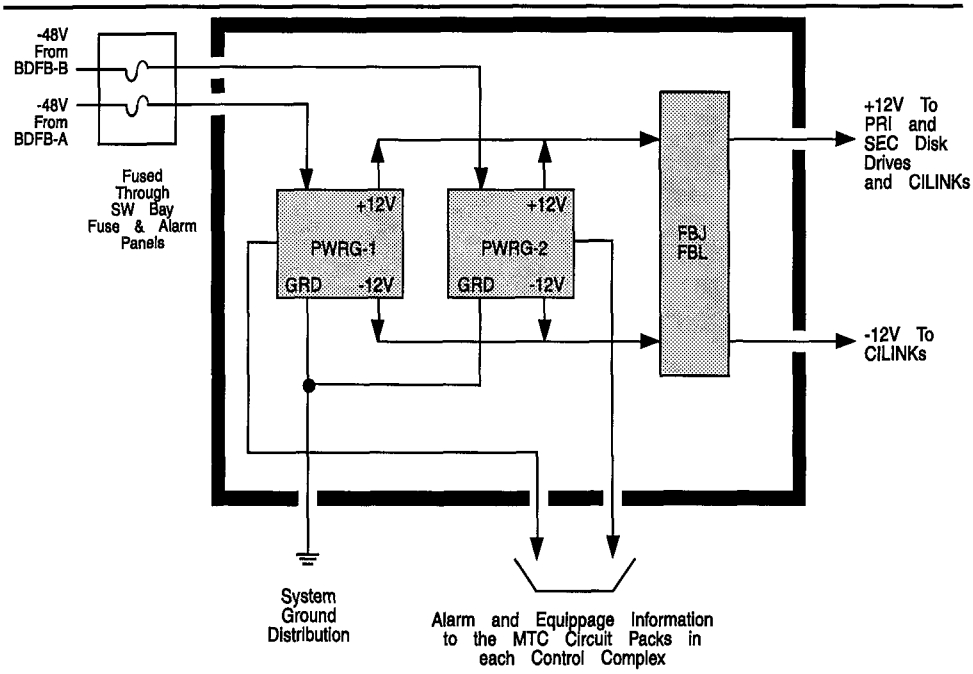



Figure 4-3. **Memory Storage Module — +12V and -12V Power Distribution**

Figure 4-3 shows the +12V and -12V power distribution for the Secondary Storage Subsystem.

Figure 4-4 shows a detailed block diagram of the High-Capacity Controller and Memory Storage Modules. Within the High-Capacity Controller Module are two control complexes. These control complexes provide protection of system control in the event the active control complex fails. A control complex consists of the CPU, SSC, MTC, SCI, and UI circuit packs.

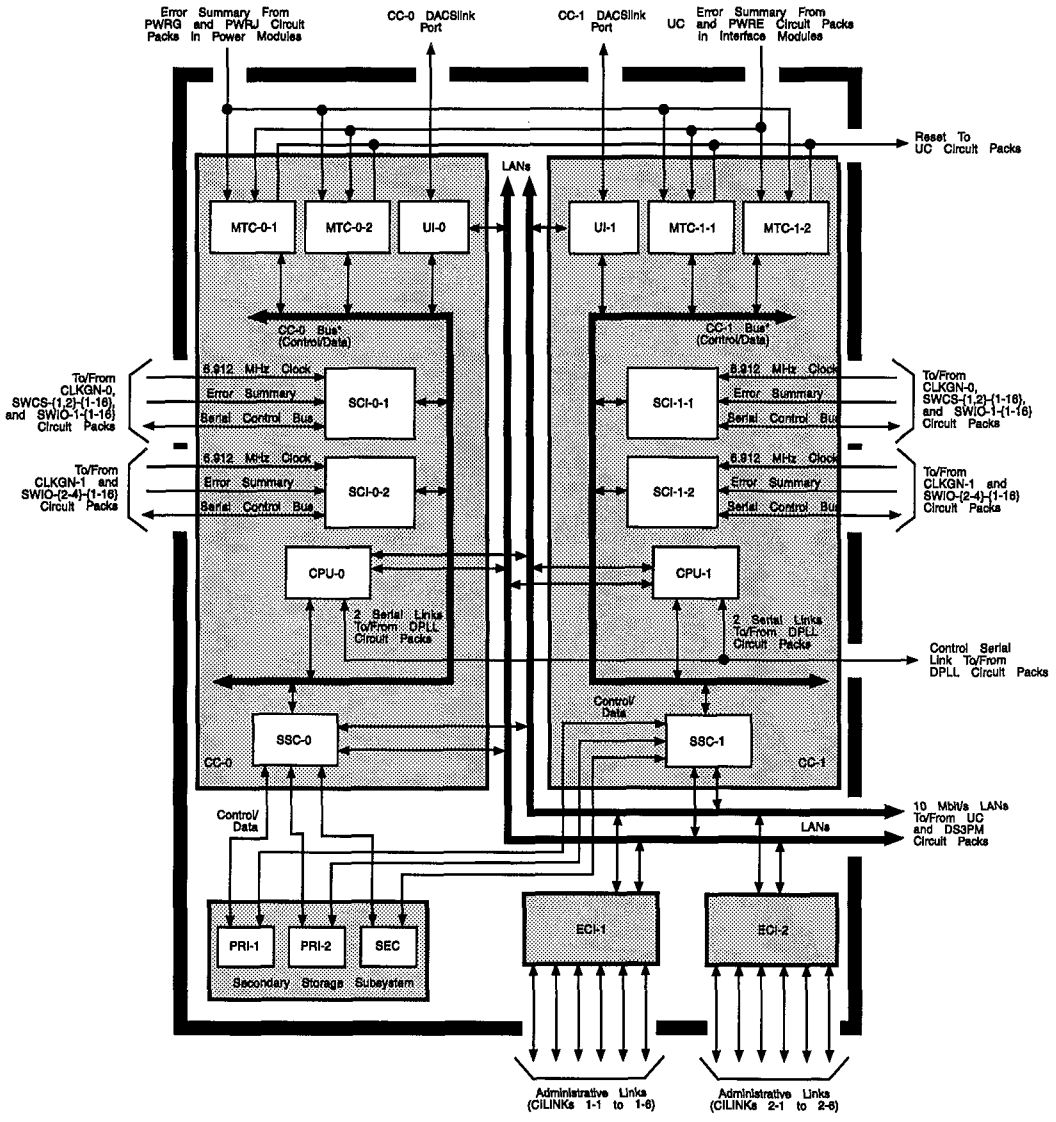



Figure 4-4. **High-Capacity Controller and Memory Storage Modules Block Diagram**

The functions provided by the circuit packs within the High-Capacity Controller and Memory Storage Modules are described in the following sections.

## Central Processing Unit (CPU)

The Central Processing Unit (CPU) controls and coordinates all system functions. The CPU contains the microprocessor circuitry. Two CPU circuit packs are provided with one controlling the system functions and the other in the standby mode in the event the active control complex fails.

## Secondary Storage Controller (SSC)

The Secondary Storage Controller (SSC) controls the start-up and backup of the storage subsystem (hard and optical disks). The active SSC communicates with its associated CPU via the local area network (LAN) to access the primary and secondary storage disks.

## Maintenance Interface (MTC)

The Maintenance Interface (MTC) provides error detection for the High-Capacity Controller Module circuit packs and Switch Power Module circuit packs. The MTC also provides error detection for the Unit Controller (UC) and power circuit packs in the collocated interface modules. The MTC circuit packs contain the contact closures for office alarms and are used to reset UC circuit packs. Control of the MTC circuit pack is provided by its associated CPU circuit pack within the control complex.

## Unit Interface (UI)

The Unit Interface (UI) provides the LAN distribution and error summary functions for the UC and power circuit packs in the collocated interface modules. The UI is the distribution point for communication over the 10-Mb/s LAN.

## Enhanced Communications Interface (ECI)

The Enhanced Communications Interface (ECI) provides the interfaces for remote Operations Systems (OSs) and a local communications interface terminal (CIT). Control and data transfer to or from either CPU is provided through the LAN. ECI circuit packs work independently of each other except for the TABS links. For the TABS links, one ECI circuit pack is designated as the master and the other the slave. When the system is reset, ECI-1 is designated as the master. The TABS link must be connected to the master ECI circuit pack

## Switch Communications Interface (SCI)

The Switch Communications Interface (SCI) provides the communication and maintenance interfaces between the SCI's associated CPU and the SWIO and SWCS Modules circuit packs using a serial bus comprising information from the system bus (control, data, and status). The SCI receives a 6.912-MHz clock from its associated CLKGN to provide timing for the serial bus to the SWIO and SWCS Modules.

## Primary Hard Disk Drives (PRI)

The primary hard disk drives (PRI) are nonvolatile memory for the system and do not require continuous DC power to maintain the contents of their memories. The disks are the primary backup storage devices. The hard disks contain the system software, a current copy of the cross-connect map, and the functional status of the frame. These records are updated automatically by transfers through the SSC circuit pack.

## Secondary Optical Disk Drive (SEC)

The secondary optical disk drive (SEC) is nonvolatile memory for the system and does not require continuous DC power to maintain the contents of its memory. The main function of optical disk storage is to download new software into the system and as secondary memory backup for periodically copying the hard disks. Automatic database backups can be scheduled to execute once in a 24-hour period on selected days or on every day of the week. You can also manually copy the contents of the hard disk to the optical disk or the contents of the internal RAM in the main controller to the optical disk when necessary.

## Power G (PWRG)

The Power G (PWRG) supplies +12V power to the disk drives and +12V and -12V power to the CILINKS provided by the ECI circuit packs. Each PWRG circuit pack can supply the +12V and -12V power necessary for the system in the event a PWRG power circuit pack fails. Each PWRG circuit pack is supplied -48V power from the Battery Distribution Feeder Board (BDFB) that is fused through the Fuse and Alarm panel located in the Switch Bays. Error summary information is provided to the MTC circuit packs contained in the High-Capacity Controller Module.

## Fuse Boards

The Fuse Board J (FBJ) is equipped with 77- and 78-type fuses and provide fuse protection for the +12V and -12V power supply to the Memory Storage and High-Capacity Controller Modules.

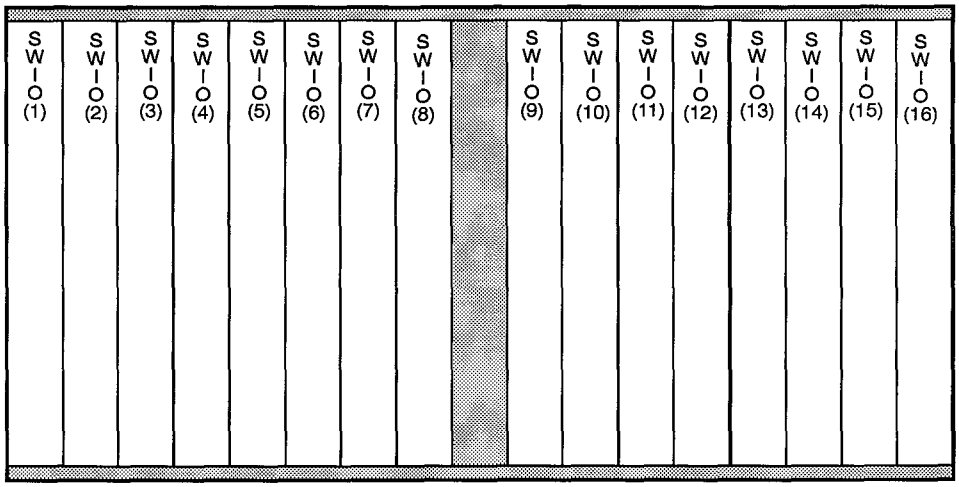
The Fuse Board L (FBL) is equipped with 77- and 78-type fuses and provide fuse protection for the +12V and -12V power supply to the Memory Storage Module and CILINKs.

For more information on fuses, refer to the section titled "Fuses" (page 7-10).

# Switch Input/Output (SWIO) and Switch Center Stage (SWCS) Modules

The Switch Input/Output (SWIO) and the Switch Center Stage (SWCS) Modules form the Switch Matrix. The Switch Matrix is a 3-stage, nonblocking, redundant space switch. The SWIO and SWCS Modules perform the DS1, DS3, STS1, and VT1.5 cross-connection functions.

The four SWIO Modules (Figure 4-5) provide the input and output switch stages of the cross-connect network (switch matrix), the clock and sync signals, and error summary information. Table 4-3 lists the circuit packs contained in the SWIO Module.




Note: Numbers in parentheses are circuit pack position in module.

Figure 4-5. **SWIO Module**

Table 4-3. **SWIO Module Circuit Packs**

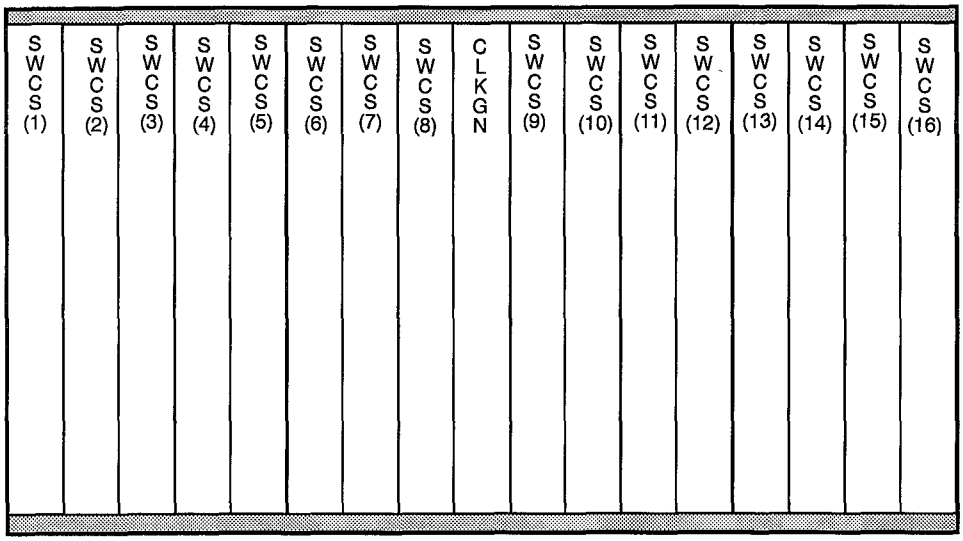
| Name | Function | Quantity |
|---|---|---|
| SWIO2 | Switch Input/Output 2 | 0*-16 (installed in pairs) |
| Apparatus Blank (Double-width) | Filler Assembly | 8**-0 (installed in pairs) |

* At least one SWIO Module must be equipped with at least two SWIO2 circuit packs. An empty SWIO Module must be equipped with 8 Apparatus Blanks or an assembly cover.

** A SWIO Module can contain 8 Apparatus Blanks or be equipped with an assembly cover provided one or more of the SWIO Modules contain at least two SWIO2 circuit packs.

The two SWCS Modules (Figure 4-6) contain twice the number of center stage switch paths as input and output ports. This feature provides the nonblocking capabilities of the switch. Table 4-4 lists the circuit packs contained in the SWCS Module.

Two fully-equipped SWCS Modules are required.




Note: Numbers in parentheses are circuit pack position in module.

Figure 4-6. **SWCS Module**

Table 4-4. **SWCS Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| SWCS3 | Switch Center Stage 3 | 16 |
| CLKGN4 | Clock Generator 4 | 1 |

Figure 4-7 shows a detailed block diagram of the SWIO and SWCS Modules which make up the non-blocking three-stage switch. Sheet 1 of Figure 4-7 shows the clocking/synchronization and control functions, while sheet 2 of Figure 4-7 shows the switching (cross-connection) functions. The circuit packs and their functions are described in the following sections.

## Switch Input/Output (SWIO)

The Switch Input/Output (SWIO) provides the input and output switch stages of the cross-connect network, the clock and sync signals from the CLKGN circuit packs to the CLKDR circuit packs in the collocated interface modules, and error summary information to the SCI circuit packs in the High-Capacity Controller Module. The SWIO circuit packs receive control (clock and cross-connect selection) from the SCI circuit packs and timing information from both CLKGN circuit packs. The SWIO circuit packs provide the input and output stages of the 3-stage switch as follows:

- At the input stage, the SWIO circuit packs receive traffic-carrying signals (referred to as N-rate signals) from interface modules through N-rate cables (R1 Channel). SWIO circuit packs operate in pairs to protect against SWIO circuit pack failures.

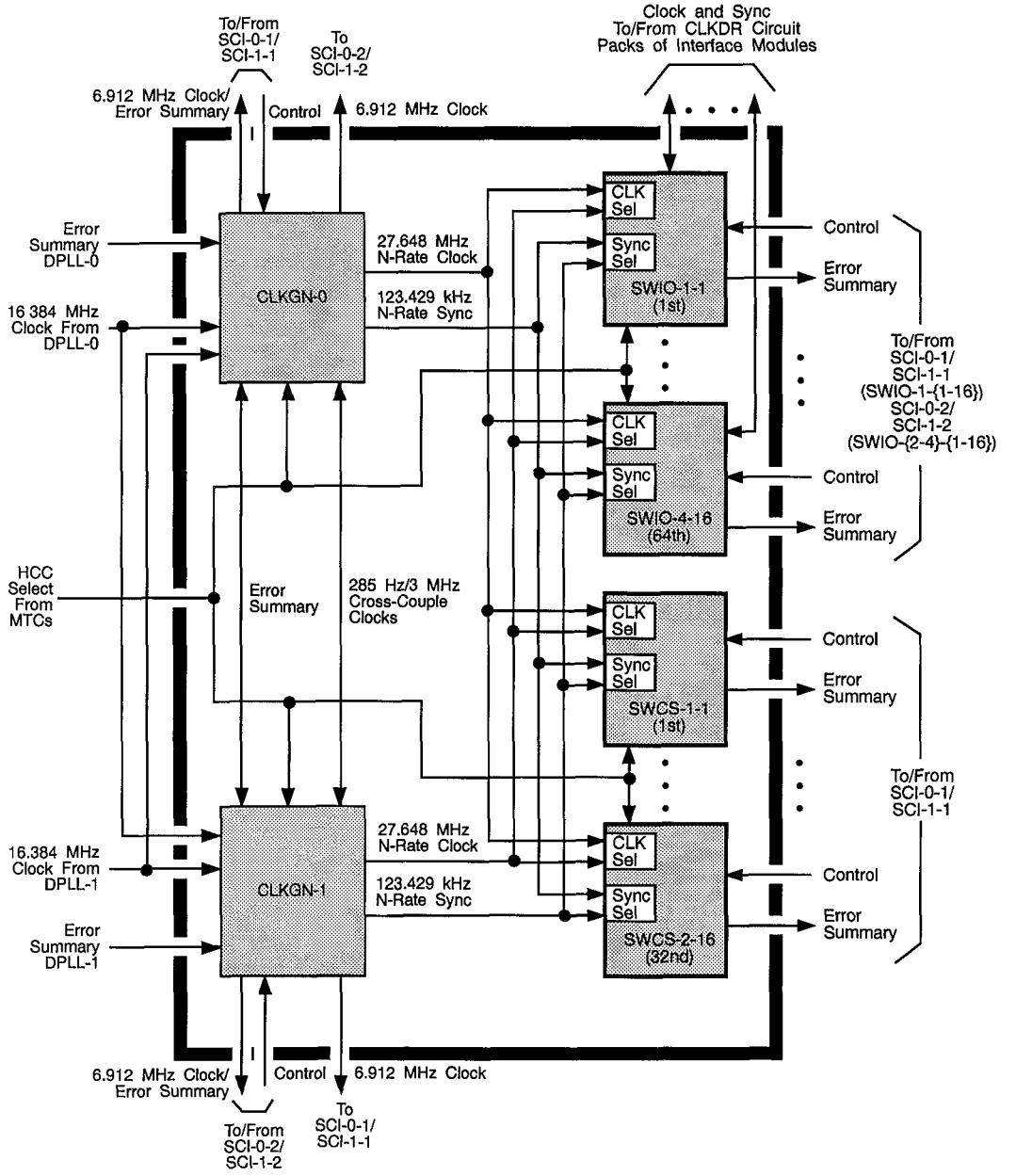
  An odd-numbered circuit pack receives 16 service N-rate signals from one set of SWIF, SMUX, or MUX circuit packs, and 16 protection N-rate signals from another set of SWIF, SMUX, or MUX, circuit packs.

  A SWIO circuit pack normally processes and sends only the service signals it receives to the SWCS circuit packs (X1 Channel). However, if a SWIO or its associated CLKDR circuit pack fails, the main controller (SCI circuit pack) directs its mate SWIO circuit pack to process both sets of signals and send them to the SWCS circuit packs.

  The 32 N-rate signals handled by the SWIO circuit pack in this protection operation contain 480 1.728-bits/s tributaries (32 x 15) capable of directing each of these signals to a different destination. The SWIO circuit pack contains a 480 x 480 switch matrix.

  Each SWIO circuit pack has 32 output ports, one connected to an input port on each of the 32 SWCS circuit packs. These connections form the X1 Channel to the switch center stage.

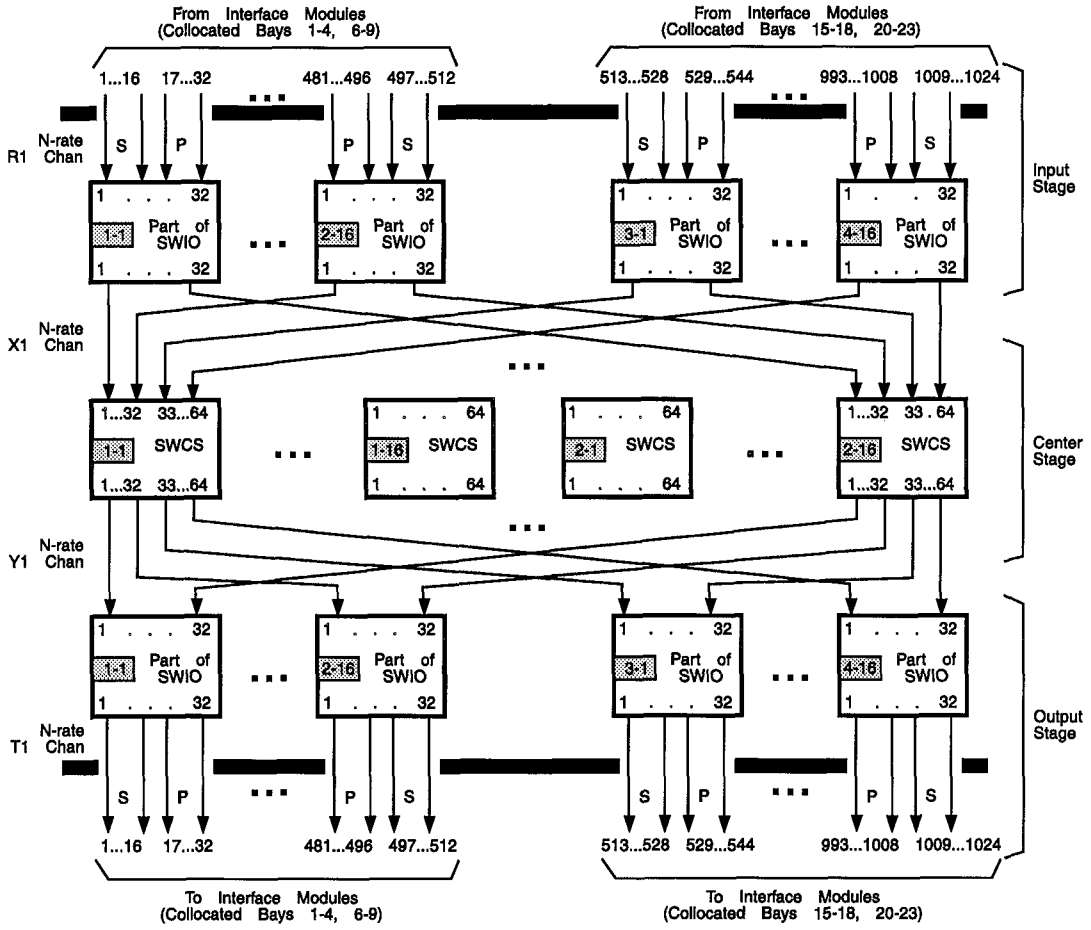
- At the output stage, the SWIO circuit packs receive cross-connected signals from the SWCS circuit packs (Y1 Channel). They then send them to the interface modules through the N-rate cables (T1 Channel). The switch in the output portion of an SWIO circuit pack has the same capacity as the one in the input portion.




**Notes:**
CLK Sel = Clock select
Sync Sel = N-rate synchronizer select

## Timing/Synchronization and Control

Figure 4-7. **SWIO and SWCS Modules Block Diagram (Sheet 1 of 2)**




**Notes:**
SRV - Service
PROTN - Protection
Chan - Channel

**3-Stage Nonblocking Space Switch Matrix**

Figure 4-7. **SWIO and SWCS Modules Block Diagram (Sheet 2 of 2)**

Both the incoming and outgoing signals handled by an SWIO circuit pack are switched to protection if either the input or output portion of the circuit pack fails or its associated CLKDR circuit pack fails. Service and protection signals are fed to pairs of SWIO circuit packs to provide 1-to-1 redundant protection [refer to the section titled "Switch Protection Group" (page 2-119) for additional information on protection]. A fully loaded Switch Complex contains 64 SWIO circuit packs. If fewer than 64 SWIO circuit packs are present, apparatus blank filler assemblies must be inserted into vacant slots.

## Switch Center Stage (SWCS)

The Switch Center Stage (SWCS) provides the center stage for the cross-connect network. The SWCS receives timing and error summary information from both CLKGN circuit packs and N-rate signals from the input stage of the SWIO (X1 Channel). The SWCS circuit packs cross-connect the N-rate signals and provides N-rate signals to the output stage of the SWIO (Y1 Channel).

The switch capacity of the SWCS circuit packs is the same as the input and output stages of the SWIO circuit packs (that is, 896 x 896). SWCS circuit packs do not function in pairs. SWCS circuit pack number 2-16 serves as protection for the other 31 SWCS circuit packs on a 1-to-31 basis [refer to the section titled "Switch Protection Group" (page 2-119) for additional information on protection]. All SWCS circuit packs must be installed in the two SWCS Modules.

## Clock Generator (CLKGN)

The CLKGN circuit packs provide the N-rate clock and synchronization signals to the SWIO and SWCS circuit packs. The CLKGN circuit pack generates the N-rate clock (27.648-MHz) and the N-rate synchronizing (123.429-KHz) signals to the SWCS and SWIO circuit packs by either using a stable on-board 16.384-MHz clock reference (stand-alone mode [asynchronous]) or using a 16.384-MHz clock reference received from the Synchronizer Module (synchronous mode). The clock and synchronizing signals also go through the SWIO circuit packs to the CLKDR circuit packs in the interface modules.

The CLKGN circuit packs are provisioned as Active and Standby (providing a 1-to-1 protection basis). The active and standby CLKGN circuit packs are cross-coupled to minimize the phase skew between the clock sides.

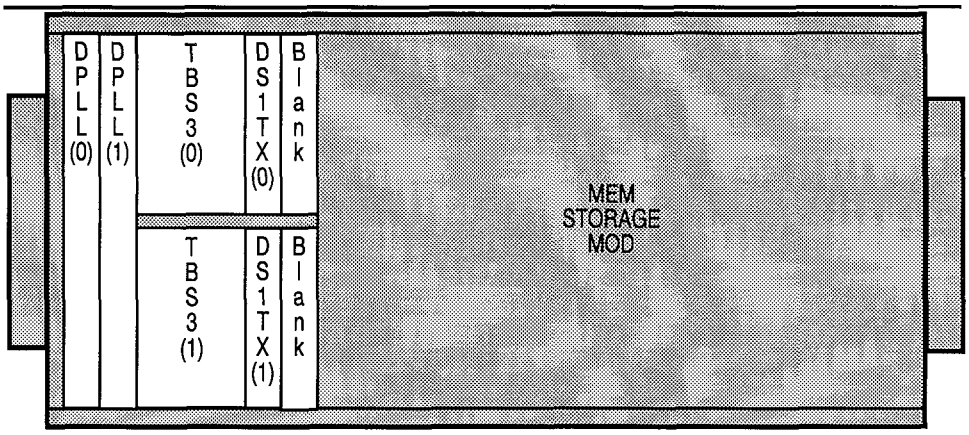
The CLKGN circuit packs provide the SCI (SCI-0-1/SCI-1- provides control for CLKGN-0 and SCI-0-2/SCI-1-2 provides control for CLKGN-1) circuit packs in the High-Capacity Controller Module with a 6.912-MHz clock. The SCI circuit packs provide the CLKGN circuit packs with a data, address, and status interface to the main controller for alarm reporting and provisioning operations.

## Apparatus Blank Filler Assembly

An apparatus blank filler assembly is installed in adjacent, empty SWIO circuit pack slots to keep out dust and foreign objects and to maintain proper air flow from the fan assembly at the bottom of the Switch Bays.

## Synchronizer (SYNC) Module

The Synchronizer (SYNC) Module (Figure 4-8) provides the timing signals to the CLKGN circuit packs in the SWCS Modules for distribution locally within the switch matrix and to the interface modules within the DACS IV-2000. The synchronizer operates in phase-locked mode using one of the two DS1 input references from the Building Integrated Timing Supply (BITS) in the Central Office and has a Stratum 3 holdover capability in the event both of the input references fail. Table 4-5 lists the circuit packs contained in the Synchronizer Module.




Note: Number in parentheses is circuit pack position number in module.

Figure 4-8. **Synchronizer Module**

Table 4-5. **Synchronizer Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| DPLL1 or DPLL2* | Digital Phase Lock Loop 1 or 2 | 2 |
| DS1TX1 or DS1TX2* | DS1 Timing Extractor 1 or 2 | 2 |
| TBS31 or TBS32* | Time Base Stratum 3, 1 or 2 | 2 |
| AWS-type | Blank Filler Assembly | 2 |

* Version 2 circuit packs contain red ALM and green ACT LEDs. The same version must be used on both Synchronizer sides.

Figure 4-9 shows a detailed block diagram of the Synchronizer Module. The functions provided by the circuit packs within the Synchronizer Module follow.

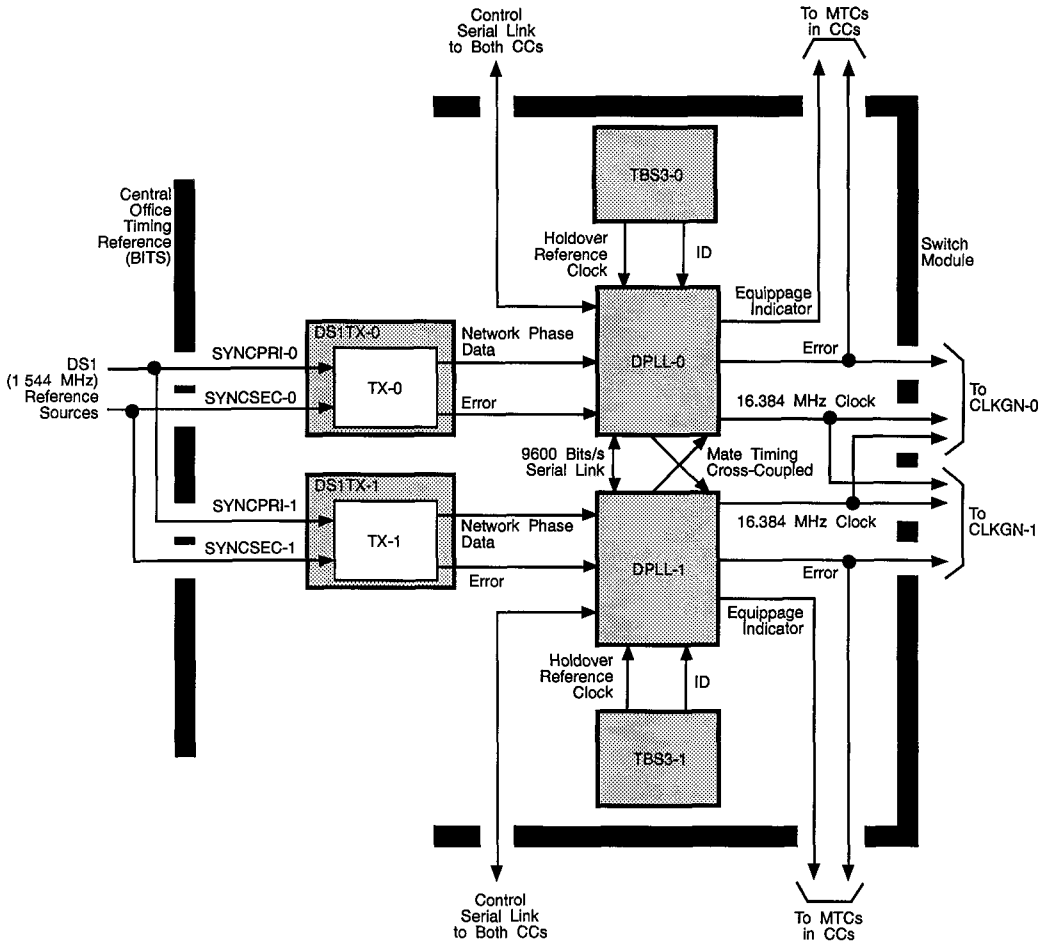



Figure 4-9. **Synchronizer Module Block Diagram**

## DS1 Timing Extractor (DS1TX)

The DS1 Timing Extractor (DS1TX) extracts timing information from up to two incoming DS1 reference signals (1.544-MHz ± 12 ppm), designated SYNCPRI and SYNCSEC, and provides line error monitors and phase detector circuitry to enable the DPLL circuit packs to lock their frequency synthesizer circuitry to one of the two 1.544-Mb/s digital links.

The line error monitors include a digital interface framer device for monitoring the signal failure activity (frame alignment, CRC-6, and loss of frame) on each of the two DS1 reference inputs. If an error occurs, the processor on the DPLL circuit pack is interrupted, indicating DS1 reference signal failure. The phase detector circuitry converts the bipolar DS1 signal to a dual-rail, 100% duty cycle, TTL-compatible signal and extracts the 1.544-MHz clock.

The DS1TX circuit packs can be provisioned to interface with line formats of AMI or B8ZS and framing formats of superframe (SF) or extended superframe (ESF) on a reference basis. You can also monitor loss-of-signal and end-of-range parameters. Refer to the `ED-EQPT` command in the *DACS IV-2000 (512) Release 5.0 Commands and Messages* manual (AT&T 365-340-902).

## Time Base Stratum 3 (TBS3)

The Time Base Stratum 3 (TBS3) contains a precision fixed-frequency oscillator and associated circuitry to provide a stable 5-MHz reference frequency, and a low-level communications link to provide the stable reference frequency required by the DPLL circuit packs' frequency synthesizer circuitry to the DPLL circuit packs. When the DPLL circuit pack enters the holdover mode of operation or when the Synchronizer Module is operated in a stand-alone application, the TBS3 circuit packs determine the output clock stability. The TBS3 circuit pack is compatible with the Stratum 3 of the North American Synchronization Network.

The TBS3 circuit packs and their associated DPLL circuit packs provide the output clock signals. If the TBS3 circuit pack enters an OOS state, its associated DPLL circuit pack enters the OOS-FEF state. After corrective maintenance is performed on the TBS3 circuit pack, both the TBS3 and DPLL circuit packs are put back into service at the same time.

## Digital Phase Lock Loop (DPLL)

The Digital Phase Lock Loop (DPLL) circuit packs receive network phase information that has been derived from reference inputs to the DS1TX circuit packs. The DPLL circuit packs process the phase information to provide the 16.384-MHz master clock (which is synchronized to the digital network) and send timing information to each CLKGN circuit pack in the SWCS Module.

Both DPLL circuit packs are cross-coupled and phase-aligned to the same BITS reference input. The DPLL circuit packs are provided with serial communication links to the High Capacity Controller (HCC) Module (control complex circuitry) and its mate DPLL circuit pack. In addition, the DPLL circuit packs provide alarm and circuit pack installation information (for all equipment associated with the DPLL circuit pack's SYNC side) to the MTC circuit packs in the HCC Module and alarm information to the CLKGN circuit packs in the SWCS Module. The error and circuit pack installation information is used for autonomous switching of circuit packs and/or timing references and alarm reports.

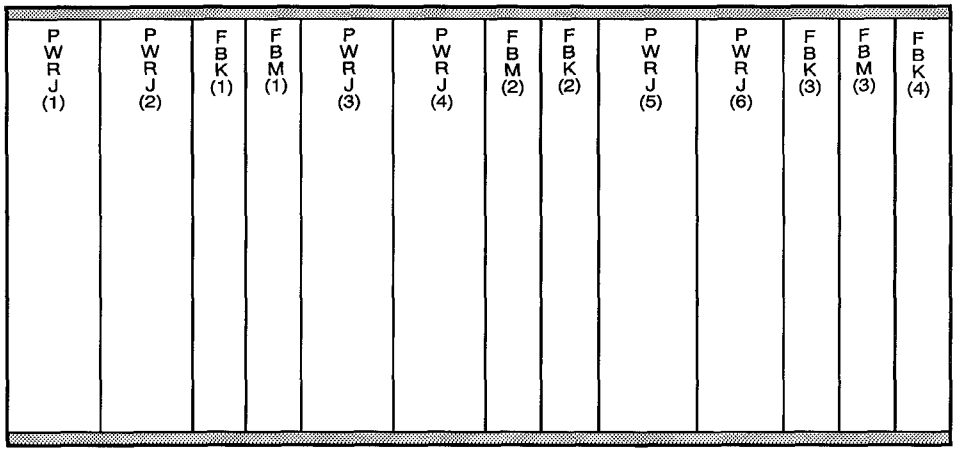
The DPLL circuit packs can operate in one of the following four modes:

- Normal (steady state condition) — provides for maximum jitter filtering phase-locked to the incoming reference signal
- Fast — provides loop time constraints that allow fast lock to the reference input(s)
- Holdover — is entered when a failure occurs, and the output frequency is maintained at the last known good frequency setting
- Free-Run — fixes the output frequency at a rate that is related to the frequency of the clock reference oscillator.

The DPLL circuit packs and their associated TBS3 circuit packs provide the output clock signals. If the DPLL circuit pack enters an OOS state, its associated TBS3 circuit pack enters the OOS-FEF state. After corrective maintenance is performed on the DPLL circuit pack, both the DPLL and TBS3 circuit packs are put back into service at the same time.

## Switch Power (SW PWR) Module

The Switch Power (SW PWR) Module (Figure 4-10) provides +5V and -5V power and fuse protection for the Switch Input/Output, Switch Center Stage, High-Capacity Controller, and Synchronizer Modules. Table 4-6 lists the circuit packs contained in the Switch Power Module.




**Note:** Number in parentheses is circuit pack position number in module.

Figure 4-10. **Switch Power Module**

Table 4-6. **Switch Power Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PWRJ | Power J | 6 |
| FBK | Fuse Board K | 4 |
| FBM | Fuse Board M | 3 |

Figure 4-11 shows a detailed block diagram of the Switch Power Module. The functions provided by the circuit packs within the Switch Power Module are described in the following sections.

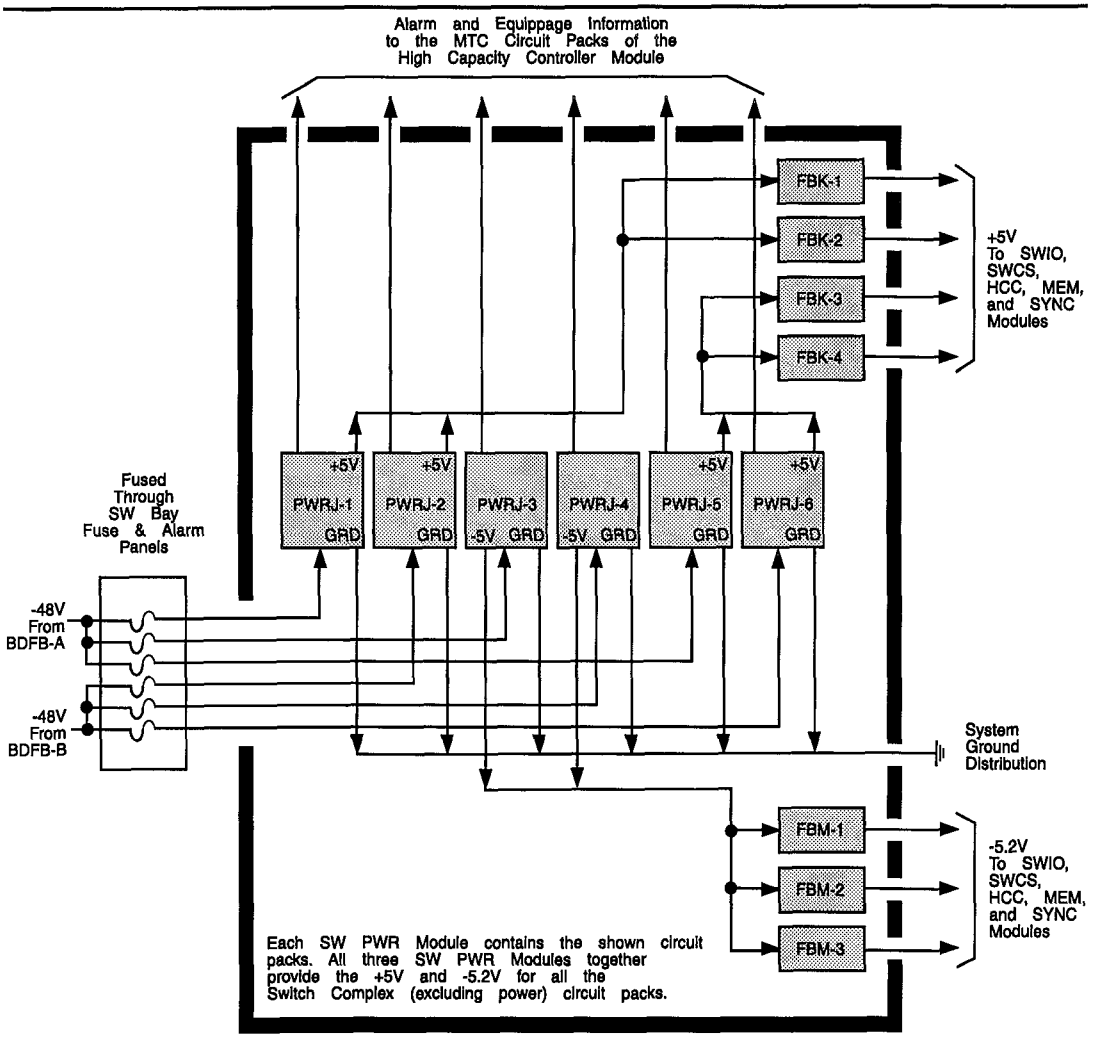



Figure 4-11. **Switch Power Module Block Diagram**

## Power J (PWRJ)

The Power J (PWRJ) circuit packs (six circuit packs for each Switch Power Module) receive -48V power (fuse protected through the Switch Bay Fuse and Alarm Panels) from the Battery Distribution Feeder Boards (BDFBs) and provide +5V and -5.2V power to the SWIO, SWCS, HCC, and SYNC Modules. The PWRJ power circuit packs provide the low-voltage power to common busses that are distributed to the Switch Complex and collocated interface bays. Alarm and equipment information is supplied to the MTC circuit packs of the High-Capacity Controller Module from each PWRJ circuit pack.

The PWRJ circuit packs contained in the three Switch Power Modules are configured into nine groups of two PWRJ circuit packs. One BDFB provides -48V power to one of the PWRJ circuit packs in each group and the other BDFB provides -48V power to the other PWRJ circuit pack within a group. Each PWRJ circuit pack is capable of providing the current load for the entire PWRJ circuit pack group in the event of a failure affecting its mate. Table 4-7 identifies the nine PWRJ groups, the circuit packs powered by the PWRJ group, and the voltage and current loads of each PWRJ group.

Two sets of test points ($V_L+/V_L-$ and $I_L+/I_L-$) on each PWRJ circuit pack are provided to measure output voltage and output current, respectively. The test points labelled $V_L+/V_L-$ are used to measure output voltage. The output voltage for SW PWR Modules 1 through 3, PWRJ circuit packs 1, 2, 5, and 6 is +5.1V ±5%. The output voltage for PWRJ circuit packs 3 and 4 is -5.3V ± 5%. The test points labelled $I_L+/I_L-$ are used to measure output current in terms of millivolts. To obtain the current measurement, divide the reading at $I_L+/I_L-$ by 10 to determine the current in amperes. For example, a reading of 200 mV indicates a current of 20 amperes. Each PWRJ circuit pack can supply an output current of 100 amperes.

## Fuse Boards

The Fuse Board K (FBK) is equipped with 77-type fuses and provides fuse protection for the +5V power supply to the Switch Complex (Main Controller and Switch Bays) circuit packs.

The Fuse Board M (FBM) is equipped with 78-type fuses and provides fuse protection for the -5V power supply to the Switch Complex circuit packs.

For more information on fuses, refer to the section titled "Fuses" (page 7-10).

Table 4-7. **PWRJ Circuit Pack Groups, Output Voltage Loads, and Current Loads for Collocated Configurations**

| PWRJ Circuit Pack Group | Current Load Description | | Output Voltage | Maximum Current Load† |
|---|---|---|---|---|
| | Circuit Pack Location* | Amp Load | | |
| Switch Power Module 1 (SW PWR MOD 1) | | | | |
| PWRJ-1-1<br>PWRJ-1-2 | SWIO-1-{1-16} | 64.0A | 4.845V (min)<br>5.355V (max) | 91.2A |
| | SWIO-3-{1-6} | 24.0A | | |
| | SYNC-0 | 3.23A | | |
| PWRJ-1-3<br>PWRJ-1-4 | SWIO-1-{1-16} | 25.7A | -5.035 (max)<br>-5.565 (min) | 52.1A |
| | SWIO-3-{1-16} | 25.7A | | |
| | SYNC-0 | 0.64A | | |
| PWRJ-1-5<br>PWRJ-1-6 | SWIO-3-{7-16} | 40.0A | 4.845V (min)<br>5.355V (max) | 89.2A |
| | HCC-0 | 49.2A | | |
| Switch Power Module 2 (SW PWR MOD 2) | | | | |
| PWRJ-2-1<br>PWRJ-2-2 | SWCS-1-{1-16}, CLKGN-0 | 75.0A | 4.845V (min)<br>5.355V (max) | 83.5A |
| | PRI-1, SEC | 8.5A | | |
| PWRJ-2-3<br>PWRJ-2-4 | SWCS-1-{1-16}, CLKGN-0 | 45.29A | -5.035 (max)<br>-5.565 (min) | 90.6A |
| | SWCS-2-{1-16}, CLKGN-1 | 45.29A | | |
| PWRJ-2-5<br>PWRJ-2-6 | SWCS-2-{1-16}, CLKGN-1 | 75.0A | 4.845V (min)<br>5.355V (max) | 79.0A |
| | PRI-2 | 4.0A | | |
| Switch Power Module 3 (SW PWR MOD 3) | | | | |
| PWRJ-3-1<br>PWRJ-3-2 | SWIO-2-{1-16} | 64.0A | 4.845V (min)<br>5.355V (max) | 91.2A |
| | SWIO-4-{1-6} | 24.0A | | |
| | SYNC-1 | 3.23A | | |
| PWRJ-3-3<br>PWRJ-3-4 | SWIO-2-{1-16} | 25.7A | -5.035 (max)<br>-5.565 (min) | 52.1A |
| | SWIO-4-{1-16} | 25.7A | | |
| | SYNC-1 | 0.64A | | |
| PWRJ-3-5<br>PWRJ-3-6 | SWIO-4-{7-16} | 40.0A | 4.845V (min)<br>5.355V (max) | 89.2A |
| | HCC-1 | 49.2A | | |

* Failure of both PWRJ circuit packs within a group causes the associated circuit packs to lose service.

† For PWRJ-{1-3}-{1,2,5,6}, 4A per SWIO circuit pack not installed are deducted from the maximum current load. For PWRJ-{1-3}-{3,4}, 1.61A per SWIO circuit pack not installed are deducted from the maximum current load. For example, using PWRJ-1-{1,2} with an empty SWIO Mod 3, the current load is 67.2A (91.2 minus 24)

# Switch Complex Circuit Packs

Table 4-8 lists the circuit pack equipment for the Switch Complex in a collocated interface bay configuration.

Table 4-8. **Circuit Pack Equipment for the Switch Complex**

| Functional Name | Circuit Pack or Equipment Code | Used In | Number Required | See Note |
|---|---|---|---|---|
| AWS-type filler assembly | 846960664 | SYNC Mod | 2 | |
| Apparatus blank cover | 847055563 | SWIO Mod | As required | 1 |
| CLKGN4 (clock generator 4) | ERA6B | SWCS Mod | 1 per module | 2 |
| CPU3 (Central Processing Unit 3) | ERA2 | HCC Mod | 2 | |
| DPLL1/DPLL2 (Digital Phase Lock Loop 1/2) | AWP9/AWP15 | SYNC Mod | 2 | 3 |
| DS1TX1/DS1TX2 (DS1 Timing Extractor 1/2) | AWS5/AWS9 | SYNC Mod | 2 | 3 |
| ECI6 (Enhanced Ccommunications Interface 6) | ERA1B | HCC Mod | 2 | 4 |
| FBJ (Fuse Board J) | ERE2 | MEM Mod | 1 | |
| FBK (Fuse BoardK) | ERD1 | SW PWR Mod | 4 | |
| FBL (Fuse Board L) | ERE3 | MEM Mod | 1 | |
| FBM (Fuse Board M) | ERD2 | SW PWR Mod | 3 | |
| MTC4 (Maintenance interface 4) | ERA9 | HCC Mod | 4 | 5 |
| PRI4 (Primary off-line storage 4) | ERB2 | MEM Mod | 2 | |
| PWRG (Power G) | 428AB | MEM Mod | 2 | |
| PWRJ (Power J) | 568A or 568B | SW PWR Mod | 6 per module | 6 |

Table continued on next page; notes are listed at end of table.

Table 4-8. **Circuit Pack Equipment for the Switch Complex (Continued)**

| Functional Name | Circuit Pack or Equipment Code | Used In | Number Required | See Note |
|---|---|---|---|---|
| SCI4 (Switch Communications Interface 4) | ERA8 | HCC Mod | 4 | |
| SEC4 (Secondary off-line storage 4) | ERB3 | MEM Mod | 1 | |
| SSC4 (Secondary Storage Controller 4) | ERA7 | HCC Mod | 2 | |
| STPNL2 (Status Panel 2) | ED-9C138-30 | HCC Mod | 1 | |
| SWCS3 (Switch Center Stage 3) | ERA5 | SWCS Mod | 16 | 7 |
| SWIO2 (Switch Input/ Output 2) | ERA4 | SWIO Mod | 0-16 | 8,9 |
| TBS31/TBS32 (Time Base Stratum 3 1/2) | AWS3/AWS8 | SYNC Mod | 2 | 3 |
| UI3 (Unit Interface 3) | ERA10 | HCC Mod | 2 | 10 |

Notes:

1. The blank appartus covers (double width) are installed in the SWIO Module in place of SWIO (ERA4) or OSWIO (ERY1) circuit packs when the four SWIO Modules are not equipped with the full complement of 64 SWIO/OSWIO circuit packs.
2. Must use two identical CLKGN4 circuit packs (slots labeled CLKGN in the SWCS Modules).
3. Version 2 synchronizer circuit packs replace version 1 circuit packs for new systems. Existing systems can use either version circuit packs. Version 1 and 2 circuit packs can not be mixed within the same SYNC Module.
4. Two ECI6 circuit packs can exist; the administrative links associated with each circuit pack are 1-1 through 1-6 for ECI-1, and 2-1 through 2-6 for ECI-2.
5. Must use two identical MTC4 circuit packs (slots labeled MTC in the HCC Module).
6. For systems with at least one Remote Complex, SW PWR Modules 1 and 3 must be equipped with eight new PWRJ (568B) circuit packs (that is, PWRJ-{1,3}-{1,2,5,6}). For systems with only collocated interfaces, SW PWR Modules 1 and 3 can have either version of PWRJ circuit packs (that is, 568A or 568B). SW PWR Module 2 can be equipped with either version of PWRJ circuit packs (that is, 568A or 568B).
7. Two identical SWCS Modules are required.
8. No SWIO circuit packs can be contained in an SWIO Module provided at least one SWIO Module contains two SWIO circuit packs.
9. The SWIO circuit packs are installed in pairs. SWIO and OSWIO circuit packs can not be mixed within the same Switch Bay.
10. UI3 circuit packs can not be present if at least one Remote Complex is provisioned.

# Remote Complex Architecture

# 5

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# Remote Complex Configuration Control Architecture

# 5

This chapter describes information pertaining to the DACS IV-2000 (512) controller hardware associated with Remote Complex configurations. If you need information regarding controller hardware associated with collocated interface bays, refer to Chapter 4.

The control architecture for a Remote Complex configuration comprises the following system modules:

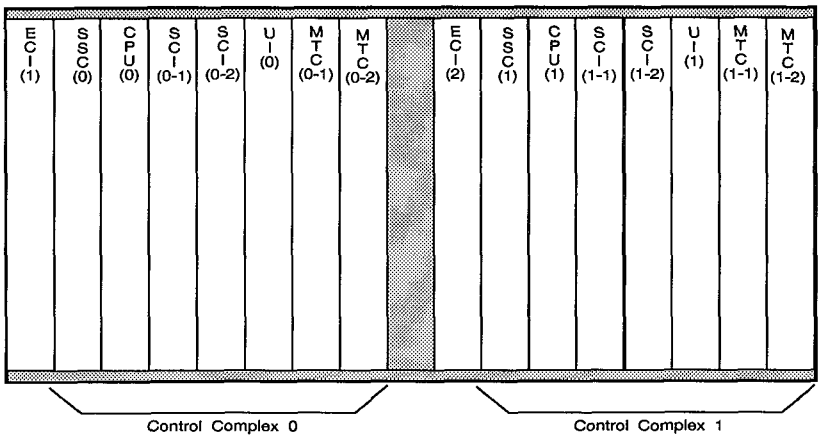
- High-Capacity Controller (HCC) Module [Switch Complex]
- Remote Unit Interface (RUI) Module [Remote Complex]
- Memory Storage (MEM) Module [Switch Complex]
- Switch Input/Output (SWIO) Module [Switch Complex]
- Switch Center Stage (SWCS) Module [Switch Complex]
- Optical Extension (OPEX) Module [Remote Complex]
- Synchronizer (SYNC) Module [Switch Complex]
- Switch Power (SW PWR) Module [Switch Complex]
- Optical Extension Power (OPEX PWR) Module [Remote Complex]
- Remote Unit Interface Power (RUI PWR) Module [Remote Complex]
- Auxiliary Power (AUX PWR) Module [Remote Complex].

Each of these modules, as they apply to Remote Complexes, is described in the sections that follow.

# High-Capacity Controller (HCC) and Memory Storage (MEM) Modules

The High-Capacity Controller (HCC) Module (Figure 5-1) manages the user interface (administrative links), performs user specified functions, and coordinates database management with the Memory Storage Module, maintenance, and fault recovery operations.

For systems with Remote Complex(es), the HCC requires two OUI circuit packs in the UI circuit pack slots. Table 5-1 lists the circuit packs contained in the High-Capacity Controller Module.



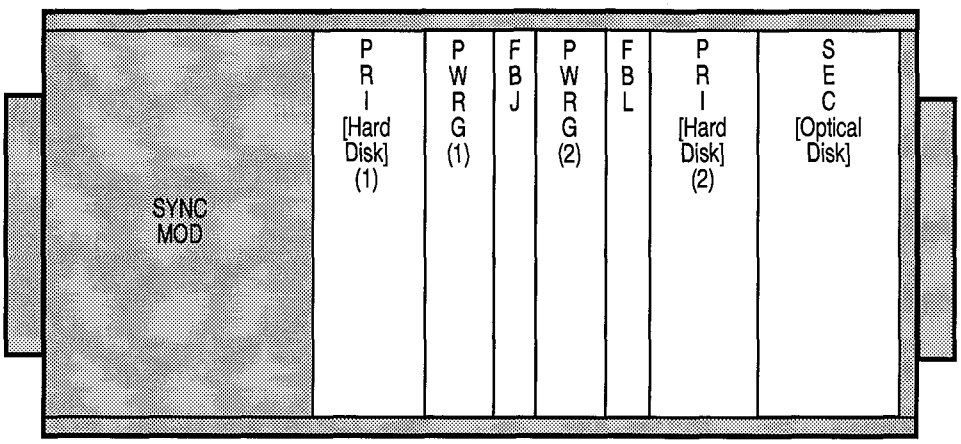

**Note:** Numbers in parentheses are circuit pack position in module. The OUI circuit packs replace the UI circuit packs.

Figure 5-1. **High-Capacity Controller Module**

Table 5-1. **High-Capacity Controller Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| CPU3 | Central Processing Unit 3 | 2 |
| ECI6 | Enhanced Communications Interface 6 | 2 |
| MTC4 | Maintenance Interface 4 | 4 |
| SCI4 | Switch Communications Interface 4 | 4 |
| SSC4 | Secondary Storage Controller 4 | 2 |
| OUI | Optical Unit Interface | 2 |

The Memory Storage Module (Figure 5-2) houses the secondary storage subsystem and its associated power and fuse block circuit packs. The secondary storage subsystem consists of three storage devices: two primary hard disks (PRI-1 and PRI-2) and a secondary optical disk (SEC). Table 5-2 lists the circuit packs contained in the Memory Storage Module.




**Note:** Numbers in parentheses are circuit pack position in module.

Figure 5-2. **Memory Storage Module**

Table 5-2. **Memory Storage Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PRI4 | Primary 4 (Hard Disk) | 2 |
| SEC4 | Secondary 4 (Optical Disk) | 1 |
| PWRG | Power G | 2 |
| FBJ | Fuse Board J | 1 |
| FBL | Fuse Board L | 1 |

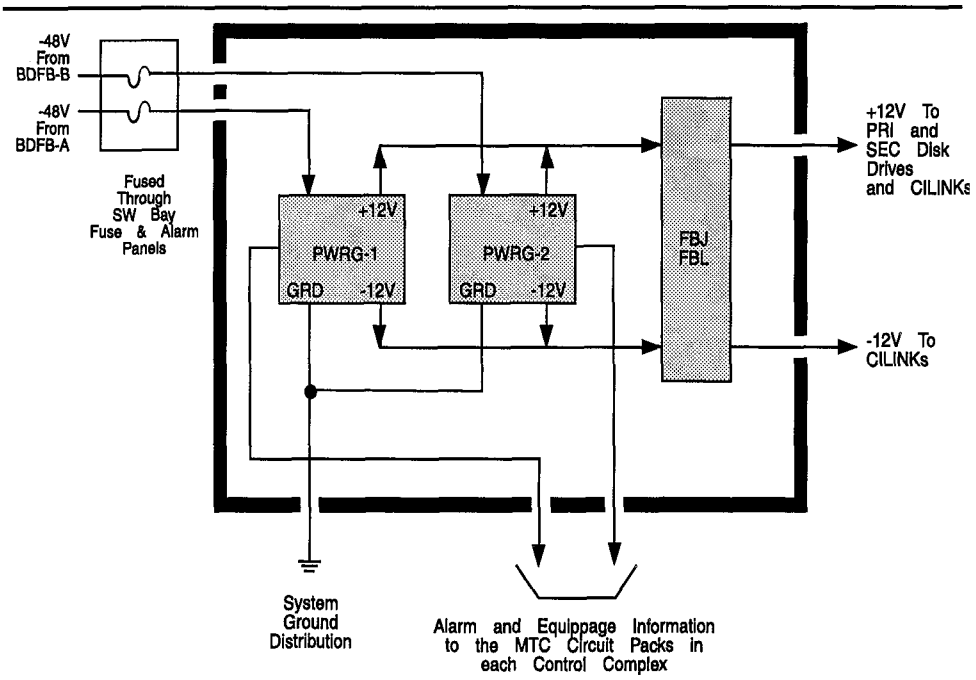



Figure 5-3. **Memory Storage Module — +12V and -12V Power Distribution**

Figure 5-3 shows the +12V and -12V power distribution for the Secondary Storage Subsystem.

Figure 5-4 shows a detailed block diagram of the High-Capacity Controller/ Memory Storage Modules. Within the High-Capacity Controller Module are two control complexes. These control complexes provide protection of system control in the event the active control complex fails. A control complex consists of the CPU, SSC, MTC, SCI and OUI circuit packs.

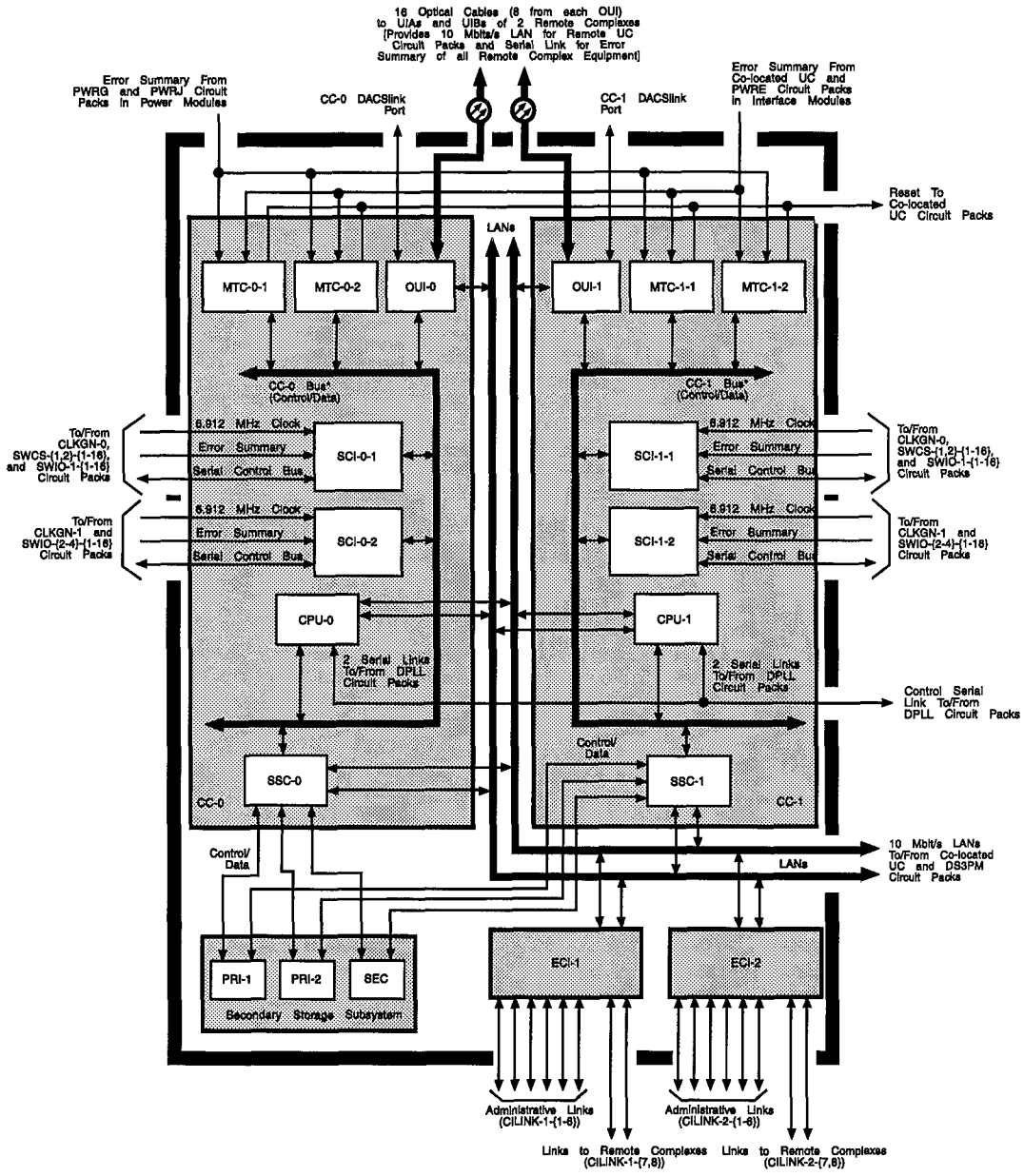



Figure 5-4. **High-Capacity Controller and Memory Storage Modules Block Diagram**

The functions provided by the circuit packs within the High-Capacity Controller and Memory Storage Modules are listed in the following sections.

## Central Processing Unit (CPU)

The Central Processing Unit (CPU) controls and coordinates all system functions. The CPU contains the microprocessor circuitry. Two CPU circuit packs are provided; one controls the system functions and the other is in the standby mode, in the event the active control complex fails.

## Secondary Storage Controller (SSC)

The Secondary Storage Controller (SSC) controls the start-up and backup of the storage subsystem (hard and optical disks). The active SSC communicates with its associated CPU via the local area network (LAN) to access the primary and secondary storage disks.

## Maintenance Interface (MTC)

The Maintenance Interface (MTC) provides error detection for the High-Capacity Controller Module circuit packs and Switch Power Module circuit packs. The MTC circuit packs contain the contact closures for office alarms and are used to reset UC circuit packs. Control of the MTC circuit pack is provided by its associated CPU circuit pack within the control complex.

## Optical Unit Interface (OUI)

The Optical Unit Interface (OUI) circuit pack is a direct replacement for the UI3 circuit pack in the HCC module. The OUI has two bidirectional optical fiber ports for each Remote Complex, one each for the UIA and one each for the UIB circuit packs. Each OUI supports up to two remote locations for a total of eight fibers connecting to the faceplate of the OUI circuit pack. The OUI circuit pack provides the LAN distribution and error summary functions for all of the Remote Complex equipment (including the remote UC and power circuit packs in the interface modules). The OUI circuit pack is the distribution point for communication over the 10-Mb/s LAN.

## Enhanced Communications Interface (ECI)

The Enhanced Communications Interface (ECI) provides the interfaces for remote Operations Systems (OSs) and a local communications interface terminal (CIT) for the Switch Complex and each Remote Complex. ECI circuit packs work independently of each other except for the TABS links. For the TABS links, one ECI circuit pack is designated as the master and the other the slave. When the system is reset, ECI-1 is designated as the master. The TABS link must be connected to the master ECI circuit pack

## Switch Communications Interface (SCI)

The Switch Communications Interface (SCI) provides the communication and maintenance interfaces between the SCI's associated CPU and the SWIO and SWCS Modules circuit packs using a serial bus comprised of information from the system bus (control, data, and status). The SCI receives a 6.912-MHz clock from its associated CLKGN to provide timing for the serial bus to the SWIO and SWCS Modules.

## Primary Hard Disk Drives (PRI)

Primary hard disk drives (PRI) are nonvolatile memory for the system and do not require continuous DC power to maintain the contents of their memories. The disks are the primary backup storage devices. The hard disks contain the system software, a current copy of the cross-connect map, and the functional status of the frame. These records are updated automatically by transfers through the SSC circuit pack.

## Secondary Optical Disk Drive (SEC)

The secondary optical disk drive (SEC) is nonvolatile memory for the system and does not require continuous DC power to maintain the contents of its memory. The main function of optical disk storage is to download new software into the system, and as secondary memory backup for periodically copying the hard disks. Automatic database backups can be scheduled to execute once in a 24-hour period on selected days or on every day of the week. You can also manually copy the contents of the hard disk to the optical disk or the contents of the internal RAM in the main controller to the optical disk when necessary.

## Power G (PWRG)

Power G (PWRG) supplies +12V power to the disk drives and +12V and -12V power to the CILINKs provided by the ECI circuit packs. Each PWRG circuit pack can supply the +12V and -12V power necessary for the system in the event a PWRG power circuit pack fails. Each PWRG circuit pack is supplied -48V power from the Battery Distribution Feeder Board (BDFB) that is fused through the Fuse & Alarm panel located in the Switch Bays. Error summary information is provided to the MTC circuit packs contained in the High-Capacity Controller Module.

## Fuse Boards

The Fuse Board J (FBJ) is equipped with 77- and 78-type fuses and provides fuse protection for the +12V and -12V power supply to the Memory Storage and High-Capacity Controller Modules.

The Fuse Board L (FBL) is equipped with 77- and 78-type fuses and provides fuse protection for the +12V and -12V power supply to the Memory Storage Module and CILINKs.

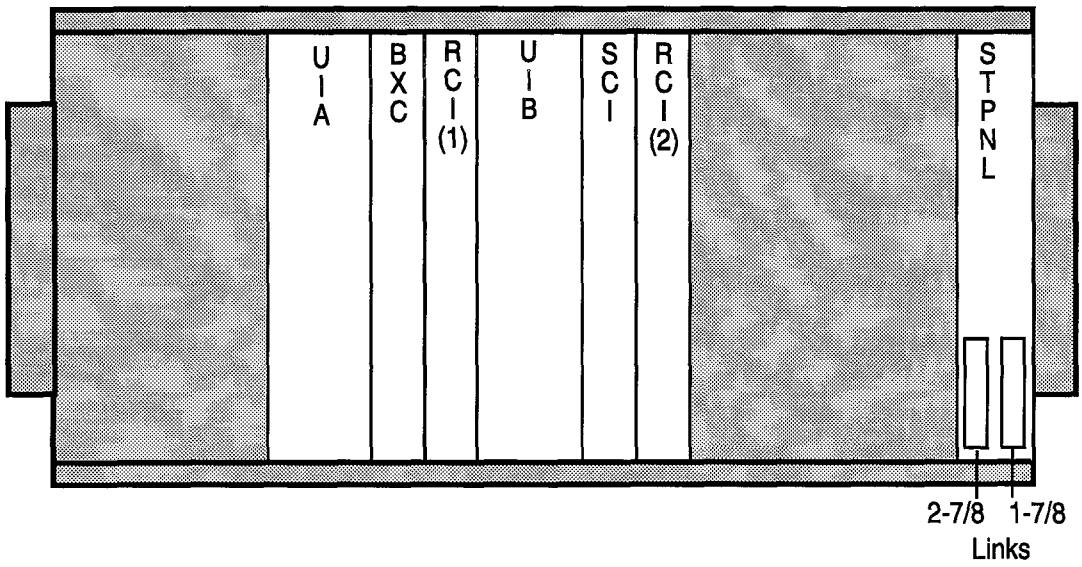
For more information on fuses, refer to the section titled "Fuses" (page 7-10).

## Remote Unit Interface (RUI) Module

The Remote Unit Interface (RUI) Module (Figure 5-5) uses the same shelf hardware and backplane as a DACS IV-2000 (256) Redundant Controller (RC) module and is used for capacity expansion and optical remoting features. The RUI Module comprises the UIA, UIB, BXC, RCI, and SCI circuit packs. In an RUI Module, the circuit packs occupy the following RC circuit pack slots:

- The UIA and UIB circuit packs occupy the MTC-0/SSC-0 and UI/SCI-1 circuit pack slots, respectively.
- The BXC circuit pack occupies the CPU-0 circuit pack slot.
- The SCI circuit pack occupies the SCI-2 circuit pack slot.
- The RCI circuit packs occupy the respective ECI circuit pack slots.

Table 5-3 lists the circuit packs contained in the RUI Module.




**Note:** Numbers in parentheses indicate the actual physical location.

Figure 5-5. **RUI Module**

Table 5-3. **RUI Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UIA | Unit Interface A | 1 |
| UIB | Unit Interface B | 1 |
| BXC | Bus Extender C | 1 |
| RCI | Remote Communications Interface | 2 |
| SCI | Switch Communications Interface | 1 |

Figure 5-6 shows a detailed block diagram of the RUI Module. The functions provided by the circuit packs within the RUI Module are described in the following sections.

## Unit Interface A (UIA) and Unit Interface B (UIB)

In the RUI Module, the UIA and UIB packs occupy the MTC (0) and UI slots respectively.

- The UIA circuit pack terminates two bidirectional fiber ports, one from OUI-0 and one from OUI-1. The UIA replaces the (MTC3) in slot 0 of the Redundant Controller (RC) shelf. The UIA functionality includes office alarms, status panel support, PWR, and fan interrupts. The UIA also monitors the UIB circuit pack status.
- The UIB circuit pack terminates two bidirectional fiber ports, one from OUI-1 and one from OUI-2. The UIB replaces the Unit Interface (UI) circuit pack of the Redundant Controller (RC) shelf. The UIB pack communicates to the OPEX circuit packs via a parallel processor interface to the SCI circuit pack. The UIB also monitors the UIA circuit pack status, the equipage, loss-of-power interrupt, and optical link interrupt.

## Bus Extender C (BXC)

The BXC circuit pack is equipped into the old CPU-0 circuit pack slot of the Remote Complex Module. The BXC is a circuit pack with only printed paths to provide the interconnection required among the SCI, UIA, and UIB circuit packs.

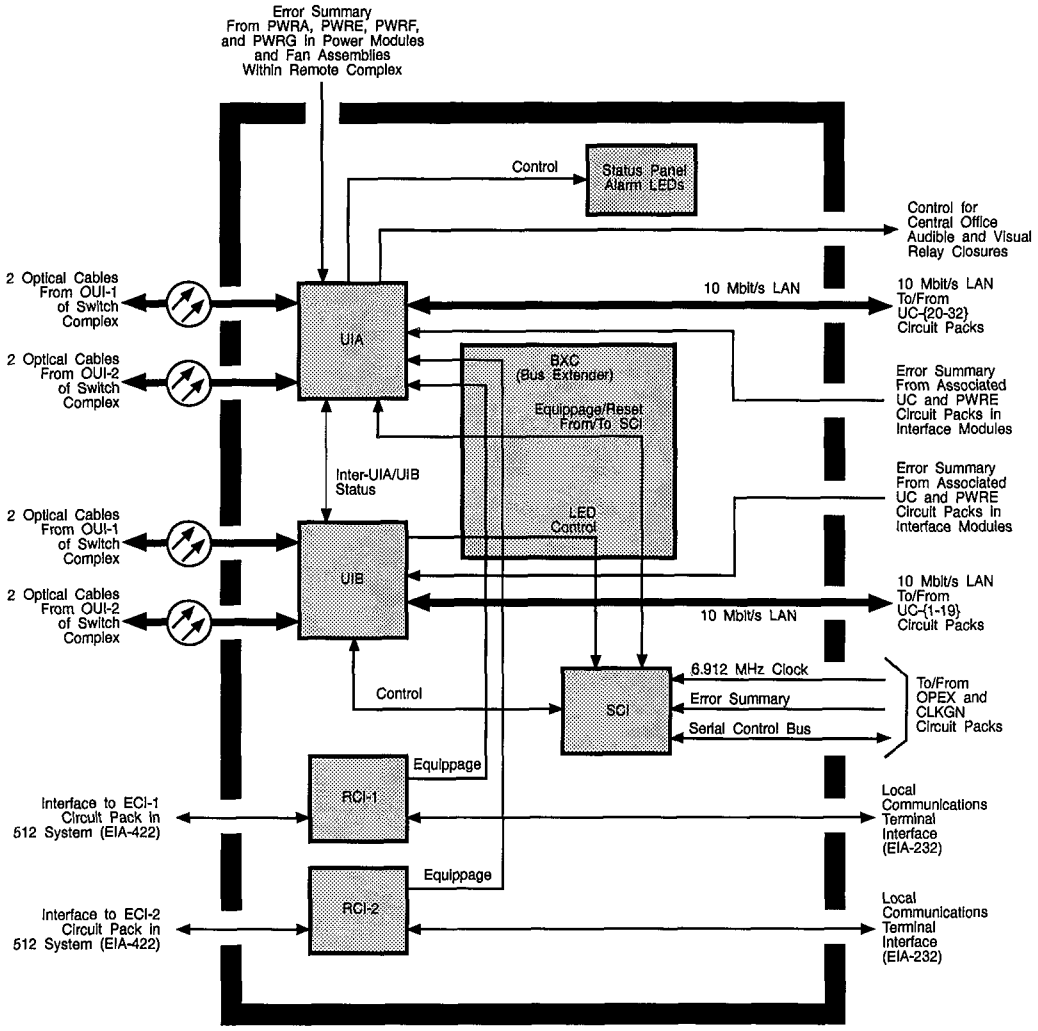



Figure 5-6. **Remote Unit Interface (RUI) Module Block Diagram**

## Remote Communications Interface (RCI)

The optional RCI circuit pack is a direct circuit pack replacement for the ECI circuit pack in the RUI Module. It provides the RS232-to-RS422 conversion required at the Remote Complex. The RCI is connected to a communications terminal, via the TTY connectors on the status panel or at the rear of the RUI Module, and provides the RS232 Snider protocol.

The RCI circuit pack provides a communications terminal at the Remote Complex. This is important when the Remote Complex is located out-of-sight from the Switch Complex and any collocated interface bays.

## Switch Controller Interface (SCI)

The Switch Communications Interface (SCI) provides the communication and maintenance interfaces between the UIA/UIB circuit packs and the OPEX Module circuit packs using a serial bus comprising information from the system bus (control, data, and status). The SCI receives a 6.912-MHz clock from the CLKGN circuit pack in the OPEX Module to provide timing for the serial bus to the OPEX Module.

# Switch Input/Output (SWIO), Switch Center Stage (SWCS), and Optical Extension (OPEX) Modules

The Switch Input/Output (SWIO) and Switch Center Stage (SWCS) Modules make up the switch matrix. The switch matrix is a 3-stage, nonblocking, redundant space switch. The SWIO and SWCS Modules perform the DS1, DS3, STS1, and VT1.5 cross-connection functions. The Optical Extension (OPEX) Module optically extends the N-rate signals to/from the Remote Complex interface modules from/to the SWIO Module in the Switch Complex.

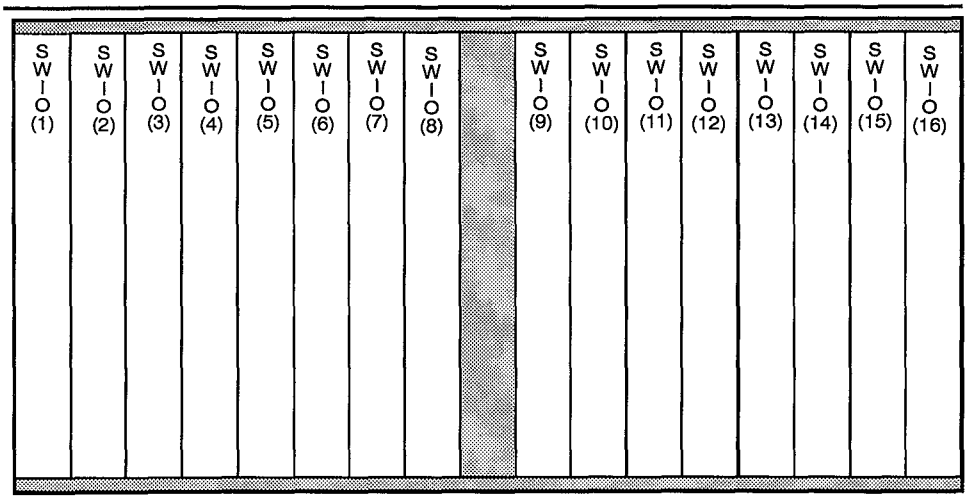
For systems with Remote Complex(es), the corresponding SWIO Modules require new Optical SWIO (OSWIO) circuit packs to support Capacity Expanded frames and/or Optical Remoting. Each SWIO Module houses 16 OSWIO circuit packs. The two SWIO Modules within a Switch Bay must contain either all SWIO circuit packs or all OSWIO circuit packs (and their associated blank covers); circuit pack types can not be mixed.

## Switch Input/Output (SWIO) Module

The SWIO Module (Figure 5-7) provides the input and output switch stages of the cross-connect network (Switch Matrix), the clock and sync signals (received from CLKGN), and error summary information. In Remote Complex configurations the N-rate signals to/from the interface modules are optically extended from/to the OSWIO circuit packs contained in the SWIO Module by the OPEX circuit packs contain in the OPEX Module. Table 5-4 lists the circuit packs contained in the SWIO Module.

## Switch Center Stage (SWCS) Module

The SWCS Module (Figure 5-8) contains twice the number of center stage switch paths as input and output ports. This feature provides the nonblocking capabilities of the switch. Two fully-equipped SWCS Modules are required. Table 5-5 lists the circuit packs contained in the SWCS Module.




**Note:** Numbers in parentheses are circuit pack position in module. The OSWIO circuit packs are addressed as SWIO locations by the software.

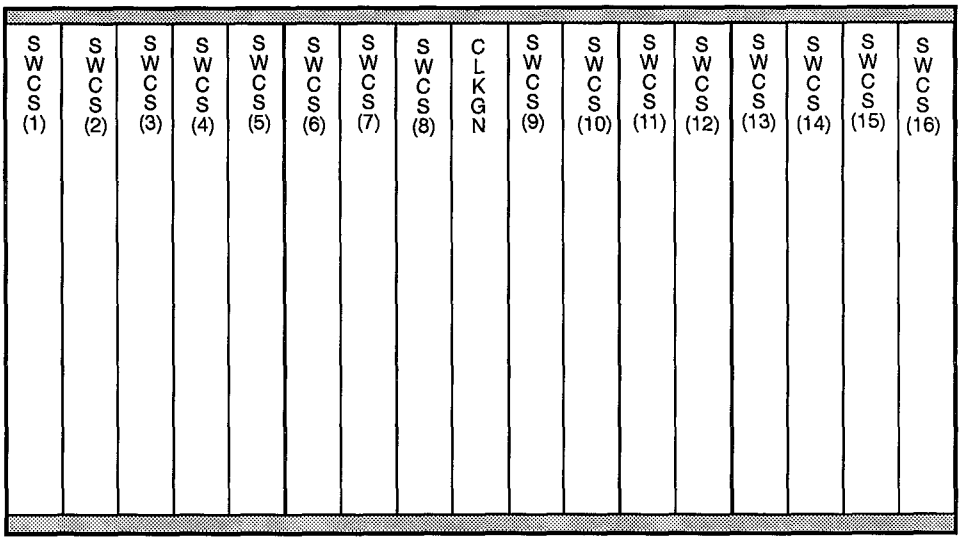
Figure 5-7. **SWIO Module**

Table 5-4. **SWIO Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| OSWIO | Switch Input/Output | 0*-16 (installed in pairs) |
| Apparatus Blank (Double-width) | Filler Assembly | 8**-0 (installed over a pair of circuit pack slots) |

* At least one SWIO Module must be equipped with at least two OSWIO circuit packs. An empty SWIO Module must be equipped with eight Apparatus Blanks or an assembly cover.

** A SWIO Module can contain eight Apparatus Blanks, provided one or more of the SWIO Modules contain at least two SWIO/OSWIO circuit packs.




**Note:** Numbers in parentheses are circuit pack position in module.

Figure 5-8. **SWCS Module**

Table 5-5. **SWCS Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| SWCS3 | Switch Center Stage 3 | 16 |
| CLKGN4 | Clock Generator 4 | 1 |

## Optical Extension (OPEX) Module

The OPEX Module (Figure 5-9) uses the shelf hardware and backplane of the existing DACS IV-2000 (256) Switch Module. Two OPEX Modules are shown in Figure 5-9 to distinguish the differences in addressing of the OPEX circuit packs. All the SWIO circuit packs within the (256) Switch Module are replaced with OPEX circuit packs or filler blanks. The SWCS circuit packs and the lower tier CLKGN circuit pack within the (256) Switch Module are replaced with cover assemblies.

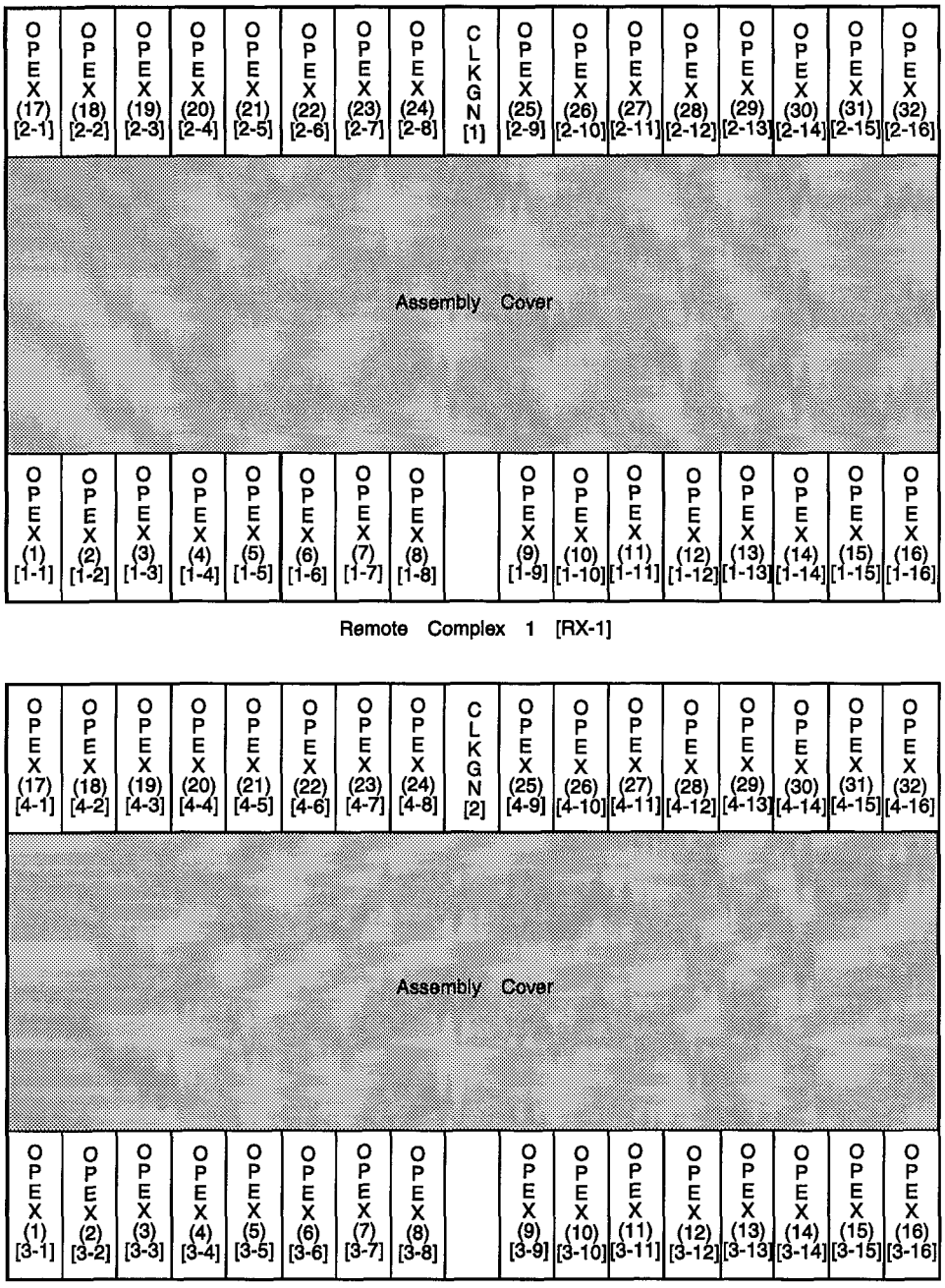
The OPEX Module is used to optically extend the N-rate signals from the Remote Complex interface modules to the Switch Complex. The fiber-optic cables from the OPEX circuit packs terminate on Optical Switch Input/Output (OSWIO) circuit packs in the Switch Complex.

Table 5-6 lists the circuit packs contained in the OPEX Module.

Table 5-6. **OPEX Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| OPEX | Optical Extension 1 | 2-32* |
| CLKGN3 | Clock Generator 3 | 1 (upper tier) |
| AWR-type | Filler Assembly | 32-2* |

* At least two OPEX circuit packs must be installed. Any empty OPEX circuit pack slots must be equipped with AWR-type Filler Assemblies.




**Note:** Numbers within brackets indicate the software location; numbers in parentheses indicate the actual physical location.

Figure 5-9. **OPEX Module**

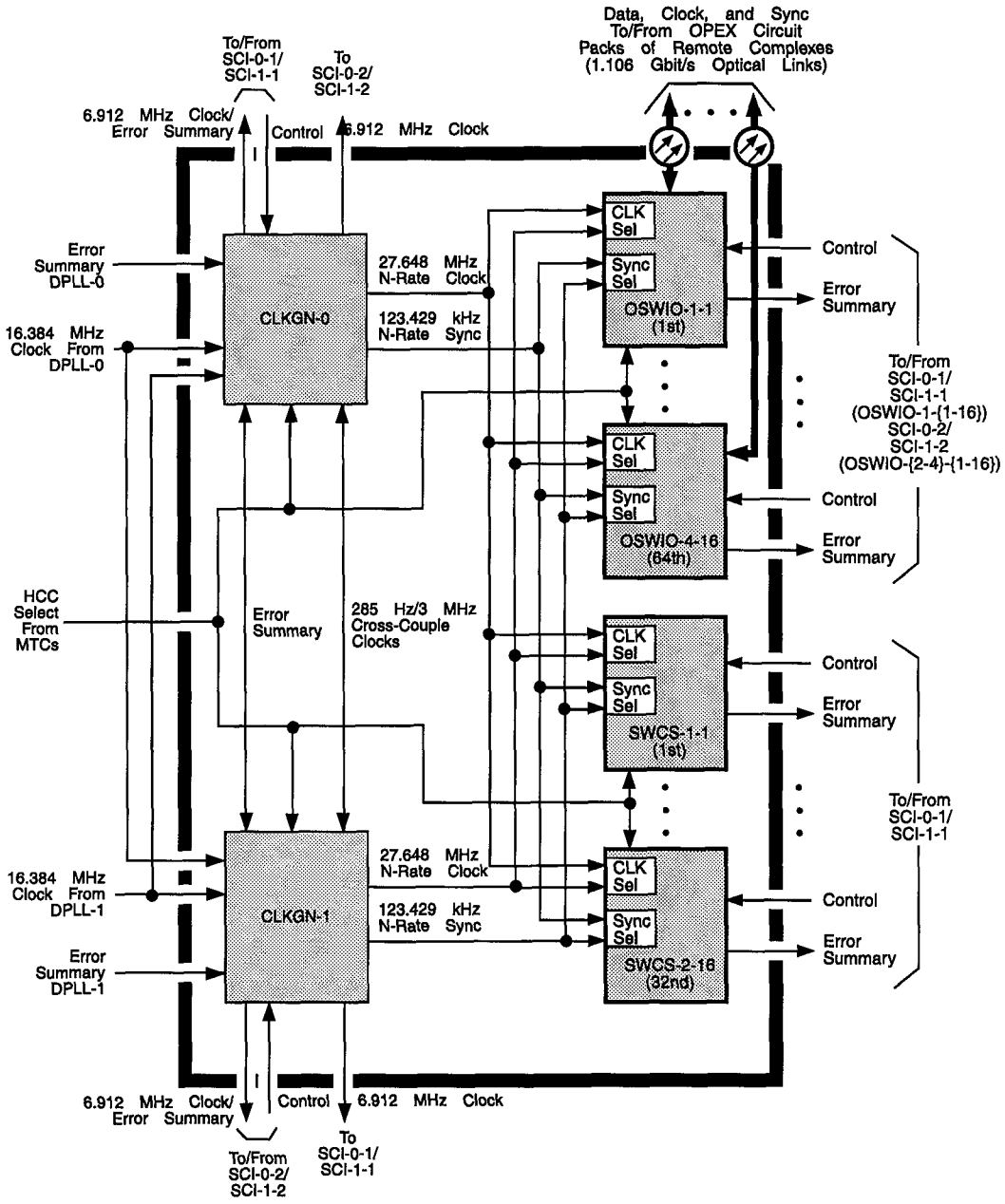
Figure 5-10 shows detailed block diagrams of the SWIO, SWCS, and OPEX Modules. The SWIO and SWCS Modules make up the non-blocking three-stage switch. The OPEX Module optically extends the N-rate signals to/from the Remote Complex interface Modules. Sheet 1 of Figure 5-10 shows the clocking/synchronization and control functions of the SWIO and SWCS Modules. Sheet 2 of Figure 5-10 shows the clocking/synchronization and control functions of the OPEX Module. Sheet 3 of Figure 5-10 shows the switching (cross-connection) functions and N-rate signal extension to the interface modules. The circuit packs and their functions are described in the following sections.

## Optical Extension (OPEX)

The OPEX circuit packs provide the extension of the N-rate, the clock, and the sync signals from the switch matrix to the Remote Complex interface modules. In addition, error summary information from the OPEX circuit packs is provided to the SCI circuit pack of the RUI Module. The OPEX circuit packs provide the extension of input and output interface module N-rate signals:

- At the input side:
  - — The OPEX and associated OSWIO and CLKDR circuit packs (and the interconnecting fiber) are in the same protection group. When an OSWIO circuit pack is protected, the OPEX and CLKDR circuit packs and optical link are protected as well.
  - — The OPEX circuit pack receives traffic-carrying signals (referred to as N-rate signals) from Remote Complex interface modules through N-rate cables and multiplexes these signals into a 1.106-Gbits/s signal. The 1.106-Gbits/s signal is sent to the input stage of the switch matrix (that is, the OSWIO circuit pack) over an optic-fiber cable.
- At the output side the OPEX circuit pack receives a 1.106-Gbits/s signal, demultiplexes the 1.106-Gbits/s signal into 16 service and 16 protection N-rate signals, and sends the N-rate signals to the interface modules through the N-rate cables.

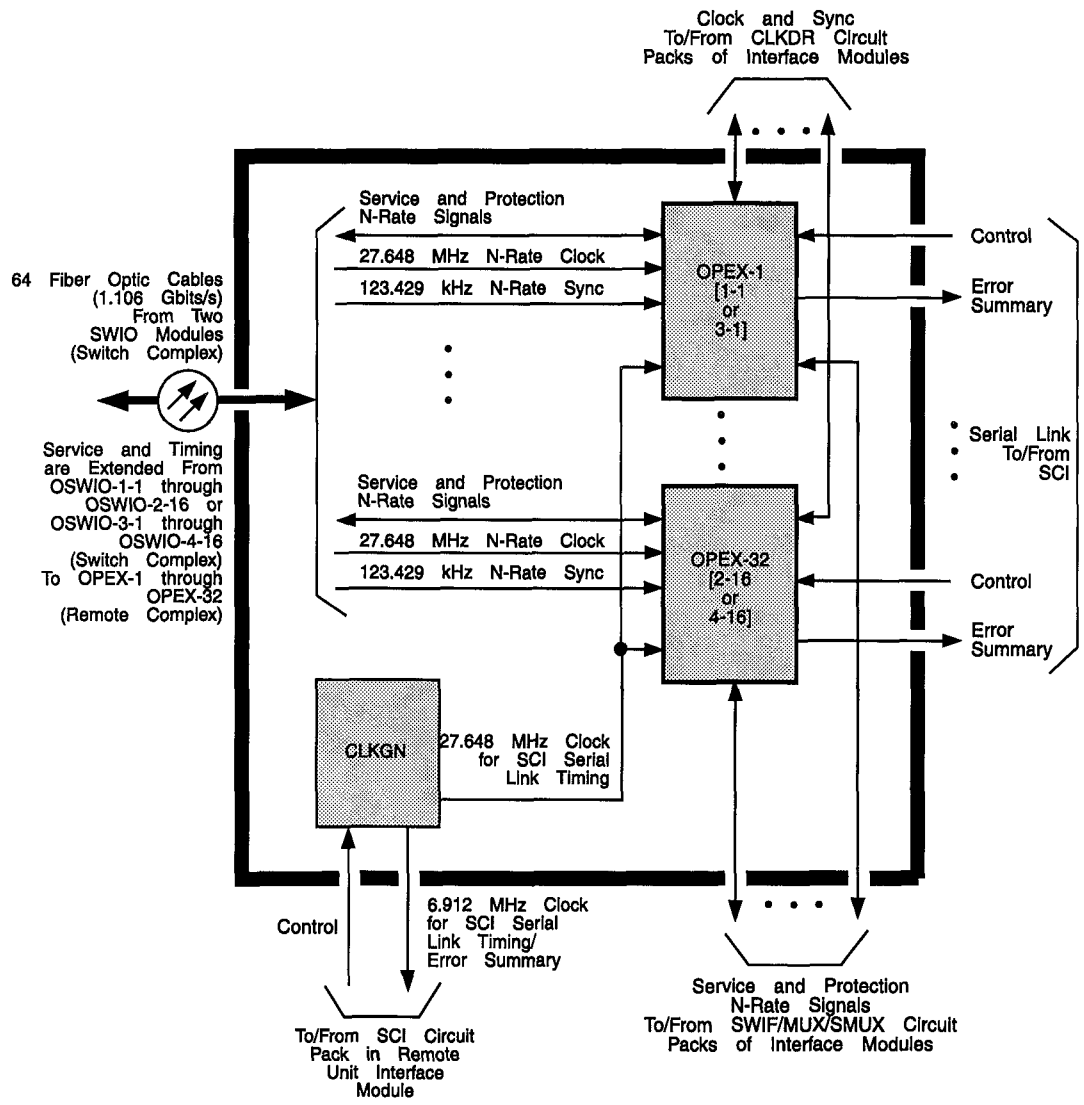
Both the incoming and outgoing signals handled by an OPEX circuit pack are switched to protection if either the input or output portion of the circuit pack fails. Service and protection signals are fed to pairs of OSWIO circuit packs to provide 1-to-1 redundant protection. There are 32 OPEX circuit packs in a fully loaded Remote Complex. If fewer than 32 OPEX circuit packs are present, AWR-type filler assemblies must be inserted into vacant circuit pack slots.




**Notes:**
CLK Sel = Clock select
Sync Sel = N-rate synchronizer select

**SWIO and SWCS Modules Timing/Synchronization and Control**

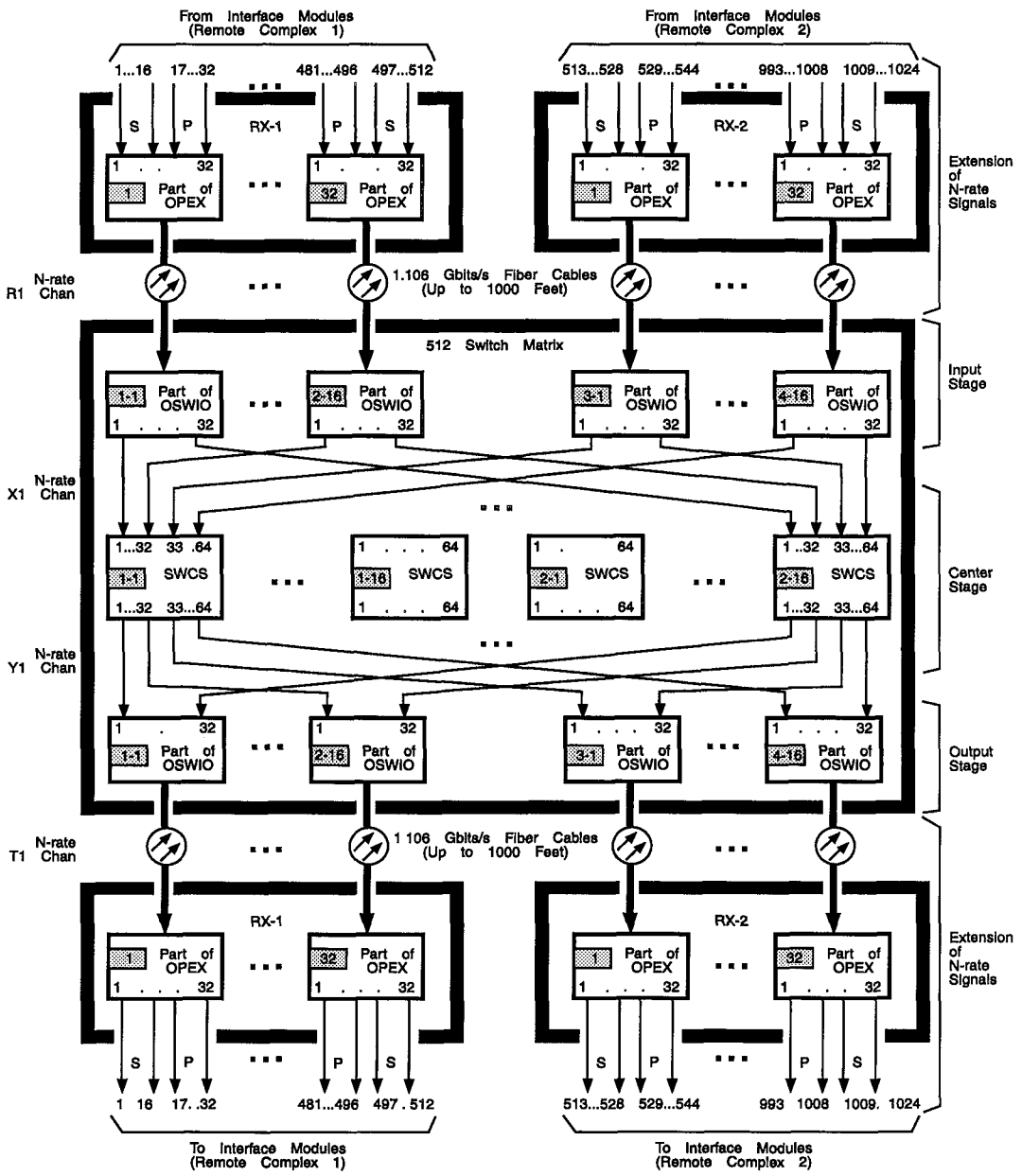
Figure 5-10. **SWIO, SWCS, and OPEX Modules Block Diagram (Sheet 1 of 3)**




**Notes:**
CLK Sel = Clock select
Sync Sel = N-rate synchronizer select

**OPEX Module Timing/Synchronization and Control**

Figure 5-10. **SWIO, SWCS, and OPEX Modules Block Diagram (Sheet 2 of 3)**




**Notes:**
SRV - Service
PROTN - Protection
Chan - Channel

**3-Stage Nonblocking Space Switch Matrix with N-rate Signals Extended to Interface Modules**

Figure 5-10. **SWIO, SWCS, and OPEX Module Block Diagram (Sheet 3 of 3)**

## Optical Switch Input/Output (OSWIO)

The OSWIO circuit packs provide the input and output switch stages of the cross-connect network. The OSWIO circuit packs receive clock and synchronizer signals from the CLKGN circuit packs of the SWCS Module and sends these signals to the CLKDR circuit packs in the interface modules through the OPEX circuit packs. N-rate signals from the interface modules are received over optic fibers from the OPEX circuit packs. In addition, error summary information is sent to the SCI circuit packs of the HCC Module. The OSWIO circuit packs provide the input and output stages of the 3-stage switch:

- At the input stage:
  - — The OSWIO and associated OPEX and CLKDR circuit packs (and the interconnecting fiber) are in the same protection group. When an OSWIO is protected, the OPEX and CLKDR circuit packs and optical link is protected as well.
  - — The OSWIO circuit pack receives the 1.106-Gbits/s signal from the OPEX circuit pack (R1 Channel), demultiplexes the 1.106-Gbits/s signal into 16 service and 16 protections signals, and sends them to the SWCS circuit packs (X1 Channel). Each OSWIO circuit pack has 32 output ports, one connected to an input port on each of the 32 SWCS circuit packs. These connections form the X1 Channel to the Switch Center Stage. However, if an OSWIO circuit pack fails, the main controller (SCI circuit pack) directs its mate OSWIO circuit pack to process both sets of signals and send them to the SWCS circuit packs.
  - — The 32 N-rate signals handled by the OSWIO circuit pack in this protection operation contain 480 1.728-bits/s tributaries (32 x 15) capable of directing each of these signals to a different destination. The OSWIO circuit pack contains a 480 x 480 switch matrix.
- At the output stage the OSWIO circuit pack receives cross-connected signals from the SWCS circuit packs (Y1 Channel), multiplexes these signals into a 1.106-Gbits/s signal (T1 Channel), and sends the 1.106-Gbits/s signal to the OPEX circuit pack.

Both the incoming and outgoing signals handled by an OSWIO circuit pack are switched to protection if either the input or output portion of the circuit pack fails. Service and protection signals are fed to pairs of OSWIO circuit packs to provide 1-to-1 redundant protection. There are 64 SWIO/OSWIO circuit packs in a fully loaded Switch Complex. If fewer than 64 SWIO/OSWIO circuit packs are present, double-width cover assemblies must be used over vacant circuit pack slots. SWIO Modules associated with a Switch Bay can contain only SWIO or OSWIO circuit packs. SWIO and OSWIO circuit packs can not be mixed in a Switch Bay.

## Switch Center Stage (SWCS)

The Switch Center Stage (SWCS) provides the center stage for the cross-connect network. The SWCS receives timing and error summary information from both Switch Complex CLKGN circuit packs and N-rate signals from the input stage of the OSWIO circuit packs (X1 Channel). The SWCS circuit packs cross-connect the N-rate signals and provide N-rate signals to the output stage of the OSWIO circuit packs (Y1 Channel).

The switch capacity of the SWCS circuit packs is the same as the input and output stages of the OSWIO circuit packs (that is, 896 x 896). SWCS circuit packs do not function in pairs. SWCS circuit pack number 2-16 serves as protection for the other 31 SWCS circuit packs providing protection on a 1-to-31 basis [refer to the section titled "Switch Protection Group" (page 2-119) for additional information on protection]. All SWCS circuit packs must be installed in the two SWCS Modules.

## Clock Generator (CLKGN) of the SWCS Module

The CLKGN circuit packs in the SWCS Modules provide the N-rate clock and synchronization signals to the OSWIO and SWCS circuit packs. The CLKGN circuit pack generates the N-rate clock (27.648 MHz) and the N-rate synchronizing (123.429 KHz) signals to the SWCS and OSWIO circuit packs by either using a stable on-board 16.384-MHz clock reference (stand-alone mode [asynchronous]) or using a 16.384-MHz clock reference received from the Synchronizer Module (synchronous mode). The clock and synchronizing signals also go through the OSWIO (and OPEX) circuit packs to the CLKDR circuit packs in the Remote Complex interface modules.

CLKGN circuit packs are provisioned as Active and Standby (providing 1-to-1 protection). The active and standby CLKGN circuit packs are cross-coupled to minimize the phase skew between the clock sides.

The CLKGN circuit packs provide the SCI circuit packs in the High-Capacity Controller Module with a 6.912-MHz clock. (SCI-0-1/SCI-1-1 provides control for CLKGN-0 and SCI-0-2/SCI-1-2 provides control for CLKGN-1.) The SCI circuit packs provide the CLKGN circuit packs with a data, address, and status interface to the main controller for alarm reporting and provisioning operations.

## Clock Generator (CLKGN) of the OPEX Module

The CLKGN circuit pack in the OPEX Module provides a timing reference for the SCI circuit pack in the RUI Module and for the OPEX circuit packs in the OPEX Module to support the serial communication interface. The CLKGN of the OPEX Module provides a 6.912-MHz reference to the SCI circuit pack in the RUI Module.

## AWR-type Filler Assembly (OPEX Module)

An AWR-type Filler Assembly must be installed in empty OPEX circuit pack slots to keep out dust and foreign objects and to maintain proper air flow from the fan assembly at the bottom of the OPEX Bay.

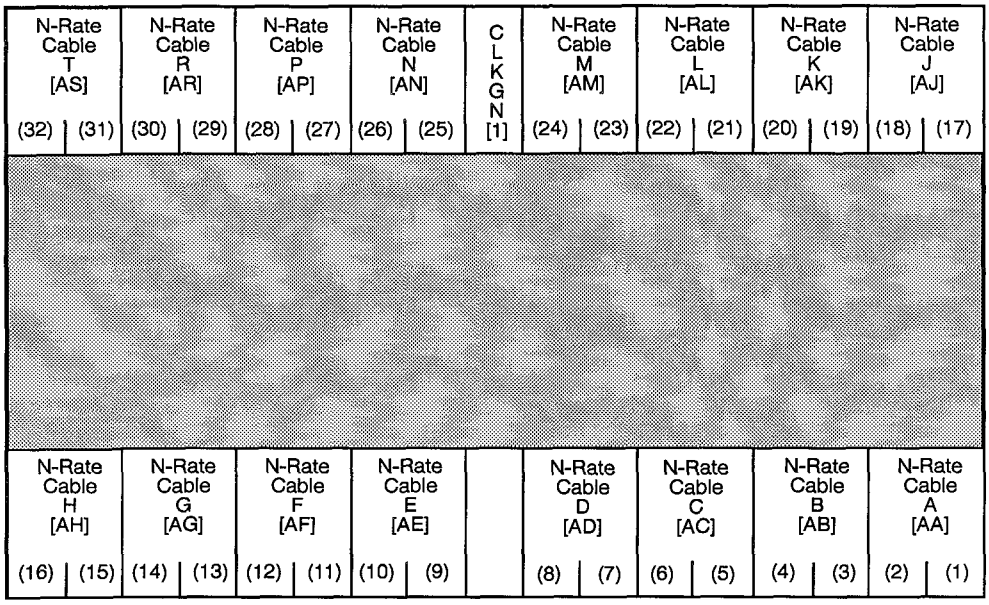
## Double-Width Cover Assembly (SWIO Module)

A double-width cover assembly must be installed over unused SWIO/OSWIO circuit pack slots to keep out dust and foreign objects and to maintain proper air flow from the fan assembly at the bottom of the Switch Bay. Each cover assembly covers a pair of SWIO/OSWIO circuit pack slots.

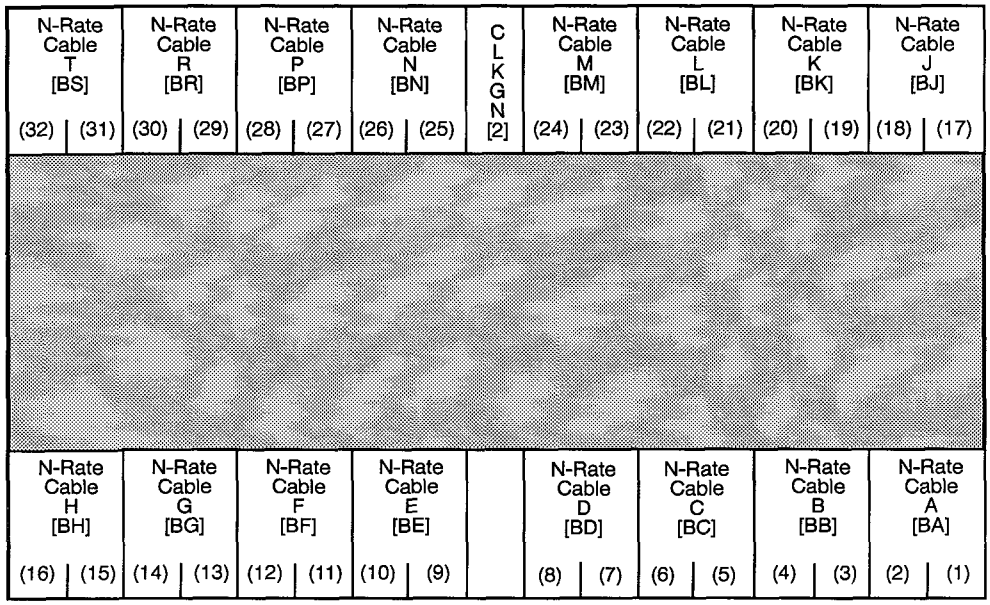
## N-Rate Cable Designations for Remote Interface Bays

The OPEX Module backplanes connect the OPEX circuit packs to the power, ground, and control buses (see Figure 5-11) of the Remote Complex. The OPEX Module is connected to the DS1, DS3, or STS1 Interface Modules by the backplane pin fields and cables associated with each OPEX circuit pack. These cables are referred to as N-rate cables and are designated A through T. The software renames these designations as AA through AS for Remote Complex 1 (RX-1) and are designated BA through BS for Remote Complex 2 (RX-2).

Each N-rate cable is associated with an OPEX circuit pack pair and 16 cables designated J1 through J16. For additional information on N-rate cables, refer to the section titled "N-rate Cables for Remote Complex Interface Bays" (page 3-33).




Remote Complex 1 [RX-1] (Rear of OPEX Bay)



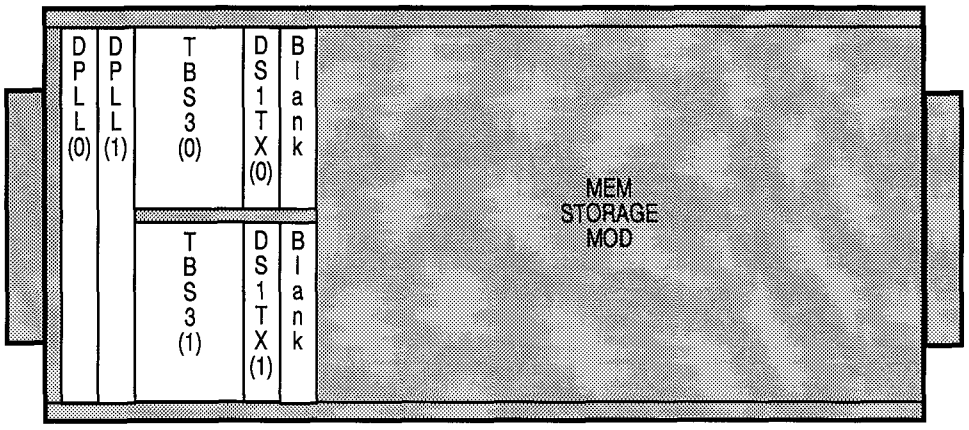

Remote Complex 2 [RX-2] (Rear of OPEX Bay)

**Note:** Numbers within brackets indicate the software location; numbers in parentheses indicate the actual physical location.

Figure 5-11. **N-Rate Cable Designations for Remote Complexes**

## Synchronizer (SYNC) Module

The Synchronizer (SYNC) Module (Figure 5-12) provides the timing signals to the CLKGN circuit packs in the SWCS Module for distribution within the switch matrix to the interface modules (through the OPEX circuit packs) within the DACS IV-2000. The synchronizer operates in phase-locked mode using one of the two DS1 input references from the Building Integrated Timing Supply (BITS) in the Central Office and has a Stratum 3 holdover capability in the event both the input references fail. Table 5-7 lists the circuit packs contained in the Synchronizer Module.




**Note:** Number in parentheses is circuit pack position number in module.

Figure 5-12. **Synchronizer Module**

Table 5-7. **Synchronizer Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| DPLL1 or DPLL2* | Digital Phase Lock Loop 1 or 2 | 2 |
| DS1TX1 or DS1TX2* | DS1 Timing Extractor 1 or 2 | 2 |
| TBS31 or TBS32* | Time Base Stratum 3, 1 or 2 | 2 |
| AWS-type | Blank Filler Assembly | 2 |

* Version 2 circuit packs contain red ALM and green ACT LEDs. The same version must be used on both Synchronizer sides.

Figure 5-13 shows a detailed block diagram of the Synchronizer Module. The functions provided by the circuit packs within the Synchronizer Module are described in the following sections.

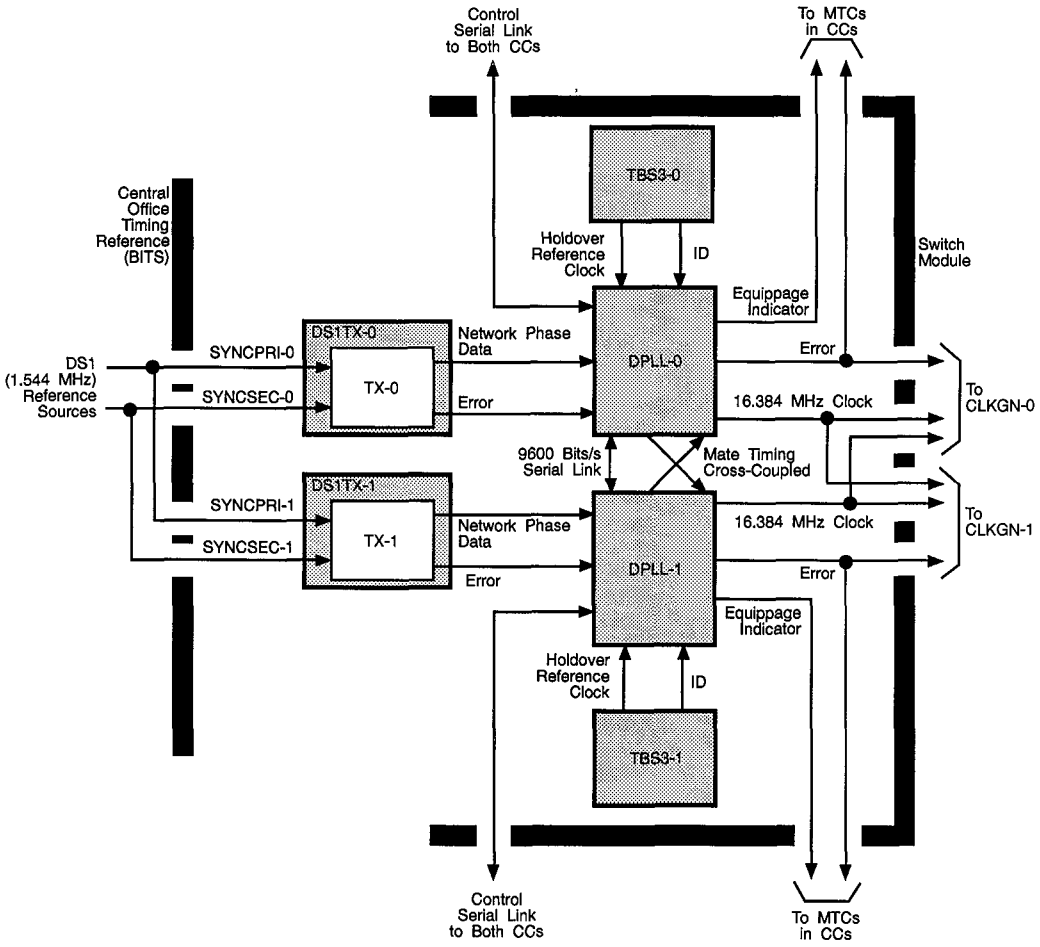



Figure 5-13. **Synchronizer Module Block Diagram**

## DS1 Timing Extractor (DS1TX)

The DS1 Timing Extractor (DS1TX) extracts timing information from up to two incoming DS1 reference signals (1.544-MHz ± 12 ppm), designated SYNCPRI and SYNCSEC, and provides line error monitors and phase detector circuitry to enable the DPLL circuit packs to lock their frequency synthesizer circuitry to one of the two 1.544-Mb/s digital links.

The line error monitors include a digital interface framer device for monitoring the signal failure activity (frame alignment, CRC-6, and loss of frame) on each of the two DS1 reference inputs. If an error occurs, the processor on the DPLL circuit pack is interrupted, indicating DS1 reference signal failure. The phase detector circuitry converts the bipolar DS1 signal to a dual-rail, 100% duty cycle, TTL compatible signal and extracts the 1.544-MHz clock.

The DS1TX circuit packs can be provisioned to interface with line formats of AMI or B8ZS and framing formats of superframe (SF) or extended superframe (ESF) on a reference basis. You can also monitor loss-of-signal and end-of-range parameters. Refer to the `ED-EQPT` command in the *DACS IV-2000 (512) Release 5.0 Commands and Messages* manual (AT&T 365-340-902).

## Time Base Stratum 3 (TBS3)

The Time Base Stratum 3 (TBS3) contains a precision fixed-frequency oscillator and associated circuitry to provide a stable 5-MHz reference frequency, and a low-level communications link to provide the stable reference frequency required by the DPLL circuit packs' frequency synthesizer circuitry to the DPLL circuit packs. When the DPLL circuit pack enters the holdover mode of operation or when the Synchronizer Module is operated in a stand-alone application, the TBS3 circuit packs determine the output clock stability. The TBS3 circuit pack is compatible with the Stratum 3 of the North American Synchronization Network.

The TBS3 circuit packs and their associated DPLL circuit packs provide the output clock signals. If the TBS3 circuit pack enters an OOS state, its associated DPLL circuit pack enters the OOS-FEF state. After corrective maintenance is performed on the TBS3 circuit pack, both the TBS3 and DPLL circuit packs are put back into service at the same time

## Digital Phase Lock Loop (DPLL)

Digital Phase Locked Loop (DPLL) circuit pack receives network phase information that has been derived from reference inputs to the DS1TX circuit packs. The DPLL circuit packs process the phase information to provide the 16.384-MHz master clock (which is synchronized to the digital network) and send timing information to each CLKGN circuit pack in the Switch Matrix.

Both DPLL circuit packs are cross-coupled and phase aligned to the same BITS reference input. The DPLL circuit packs are provided with serial communication links to the High Capacity Controller Module (control complex circuitry) and its mate DPLL circuit pack. In addition, the DPLL circuit packs provide alarm and circuit pack installation information (for all equipment associated with the DPLL circuit pack's SYNC side) to the MTC circuit packs in the HIgh Capacity Controller Module and alarm information to the CLKGN circuit packs in the Switch Matrix. The error and circuit pack installation information is used for autonomous switching of circuit packs and/or timing references and alarm reports.

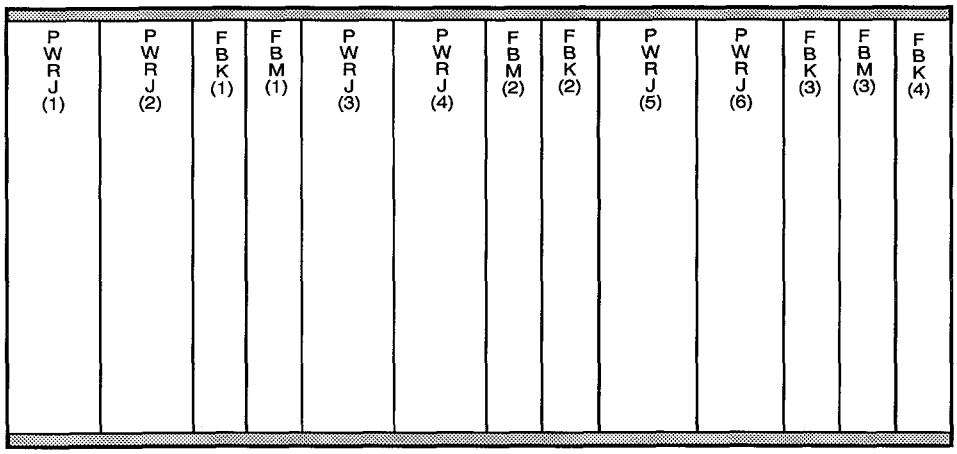
The DPLL circuit packs can operate in one of the following four modes:

- Normal (steady state condition) — provides for maximum jitter filtering phase-locked to the incoming reference signal
- Fast — provides loop time constraints that allow fast lock to the reference input(s)
- Holdover — is entered when a failure occurs, and the output frequency is maintained at the last known good frequency setting
- Free-Run — fixes the output frequency at a rate that is related to the frequency of the clock reference oscillator.

The DPLL circuit packs and their associated TBS3 circuit packs provide the output clock signals. If the DPLL circuit pack enters an OOS state, its associated TBS3 circuit pack enters the OOS-FEF state. After corrective maintenance is performed on the DPLL circuit pack, both the DPLL and TBS3 circuit packs are put back into service at the same time.

## Switch Power (SW PWR) Module

The Switch Power (SW PWR) Module (Figure 5-14) provides +5V and -5V power and fuse protection for the Switch Input/Output, Switch Center Stage, High-Capacity Controller, and Synchronizer Modules. Table 5-8 lists the circuit packs contained in the Switch Power Module.




**Note:** Number in parentheses is circuit pack position number in module.

Figure 5-14. **Switch Power Module**

Table 5-8. **Switch Power Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PWRJ | Power J | 6 |
| FBK | Fuse Board K | 4 |
| FBM | Fuse Board M | 3 |

Figure 5-15 shows a detailed block diagram of the Switch Power Module. The functions provided by the circuit packs within the Switch Power Module are described in the following sections.

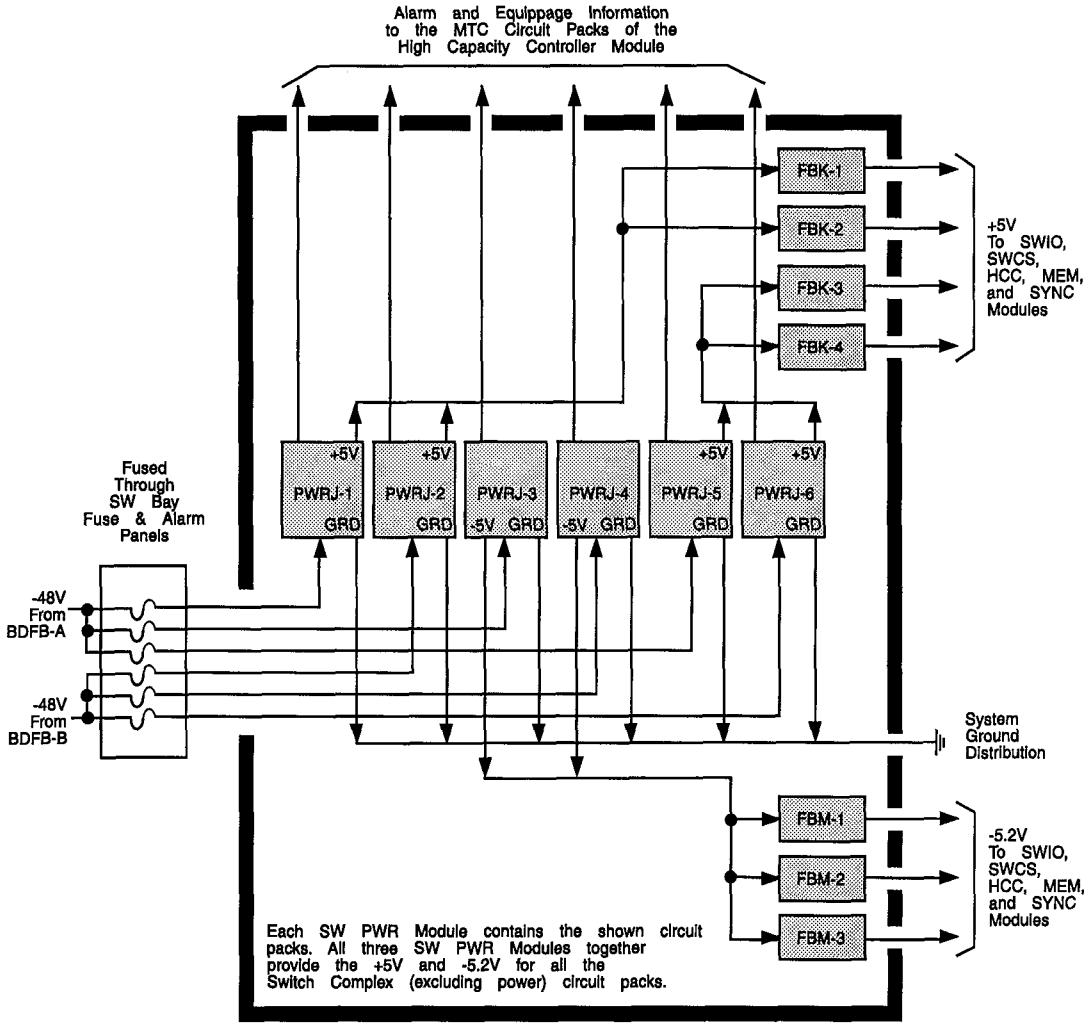



Figure 5-15. **Switch Power Module Block Diagram**

## Power J (PWRJ)

In Remote Complexes, Power Modules 1 and 3 require higher-rated PWRJ (568B) circuit packs to support the increased current demand of OSWIO circuit packs. Because of the power distribution scheme, eight of the twelve power circuit packs (PWRJ-{1,3}-{1,2,5,6}) within Power Modules 1 and 3 must be replaced if at least one Remote Complex is provisioned. As a result, the addition of a second Remote Complex does not require PWRJ circuit pack replacement.

The Power J (PWRJ) circuit packs (power circuit packs in each Switch Power Module) receive -48V power (fuse protected through the Switch Bay Fuse and Alarm Panels) from the Battery Distribution Feeder Boards (BDFBs) and provide +5V and -5.2V power to the SWIO, SWCS, HCC, and SYNC Modules. The PWRJ power circuit packs provide the low-voltage power to common busses that are distributed to the DACS IV-2000. Alarm and equipment information is supplied to the MTC circuit packs of the High-Capacity Controller Module from each PWRJ circuit pack.

The PWRJ circuit packs contained in the three Switch Power Modules are configured into nine groups of two PWRJ circuit packs. One BDFB provides -48V power to one of the PWRJ circuit packs in each group and the other BDFB provides -48V power to the other PWRJ circuit pack within a group. Each PWRJ circuit pack is capable of providing the current load for the entire PWRJ circuit pack group in the event of a failure affecting its mate. Table 5-9 identifies the nine PWRJ groups, the circuit packs power by the PWRJ group, and the voltage and current loads of each PWRJ group.

Two sets of test points ($V_L$+/$V_L$- and $I_L$+/$I_L$-) on each PWRJ circuit pack are provided to measure output voltage and output current, respectively. The test points labelled $V_L$+/$V_L$- are used to measure output voltage. The output voltage for SW PWR Modules 1 through 3, PWRJ circuit packs 1, 2, 5, and 6 is +5.1V ± 5%. The output voltage for PWRJ circuit packs 3 and 4 is -5.3V ± 5%. The test points labelled $I_L$+/$I_L$- are used to measure output current in terms of millivolts. To obtain the current measurement, divide the reading at $I_L$+/$I_L$- by 10 to determine the current in amperes. For example, a reading of 200 mV indicates a current of 20 amperes. Each PWRJ circuit pack can supply an output current of 106 amperes.

## Fuse Board K (FBK) and Fuse Board M (FBM)

Fuse Board K (FBK) is equipped with 77-type fuses and provides fuse protection for the +5V power supply to the Switch Complex (Main Controller and Switch Bays) circuit packs.

Fuse Board M (FBM) is equipped with 78-type fuses and provides fuse protection for the -5V power supply to the Switch Complex circuit packs.

Table 5-9. **PWRJ Circuit Pack Groups, Output Voltage Loads, and Current Loads — Remote Complexes**

| PWRJ Circuit Pack Group | Current Load Description | | Output Voltage | Maximum Current Load† |
|---|---|---|---|---|
| | Circuit Pack Location* | Amp Load | | |
| **Switch Power Module 1 (SW PWR MOD 1)** | | | | |
| PWRJ-1-1<br>PWRJ-1-2 | SWIO-1-{1-16} | 72.0A | 4.845V (min)<br>5.355V (max) | 102.2A |
| | SWIO-3-{1-6} | 27.0A | | |
| | SYNC-0 | 3.23A | | |
| PWRJ-1-3<br>PWRJ-1-4 | SWIO-1-{1-16} | 25.7A | -5.035 (max)<br>-5.565 (min) | 52.1A |
| | SWIO-3-{1-16} | 25.7A | | |
| | SYNC-0 | 0.64A | | |
| PWRJ-1-5<br>PWRJ-1-6 | SWIO-3-{7-16} | 45.0A | 4.845V (min)<br>5.355V (max) | 98.0A |
| | HCC-0 | 53.0A | | |
| **Switch Power Module 2 (SW PWR MOD 2)** | | | | |
| PWRJ-2-1<br>PWRJ-2-2 | SWCS-1-{1-16}, CLKGN-0 | 75.0A | 4.845V (min)<br>5.355V (max) | 83.5A |
| | PRI-1, SEC | 8.5A | | |
| PWRJ-2-3<br>PWRJ-2-4 | SWCS-1-{1-16}, CLKGN-0 | 45.29A | -5.035 (max)<br>-5.565 (min) | 90.6A |
| | SWCS-2-{1-16}, CLKGN-1 | 45.29A | | |
| PWRJ-2-5<br>PWRJ-2-6 | SWCS-2-{1-16}, CLKGN-1 | 75.0A | 4.845V (min)<br>5.355V (max) | 79.0A |
| | PRI-2 | 4.0A | | |
| **Switch Power Module 3 (SW PWR MOD 3)** | | | | |
| PWRJ-3-1<br>PWRJ-3-2 | SWIO-2-{1-16} | 72.0A | 4.845V (min)<br>5.355V (max) | 102.2A |
| | SWIO-4-{1-6} | 27.0A | | |
| | SYNC-1 | 3.23A | | |
| PWRJ-3-3<br>PWRJ-3-4 | SWIO-2-{1-16} | 25.7A | -5.035 (max)<br>-5.565 (min) | 52.1A |
| | SWIO-4-{1-16} | 25.7A | | |
| | SYNC-1 | 0.64A | | |
| PWRJ-3-5<br>PWRJ-3-6 | SWIO-4-{7-16} | 45.0A | 4.845V (min)<br>5.355V (max) | 98.0A |
| | HCC-1 | 53.2A | | |

* Failure of both PWRJ circuit packs within a group causes the associated circuit packs to lose service.

† For PWRJ-{1,3}-{1,2,5,6}, 4.5A per OSWIO circuit pack not installed are deducted from the maximum current load. For PWRJ-{1,3}-{3,4}, 1.61A per OSWIO circuit pack not installed are deducted from the maximum current load. For example, using PWRJ-1-{1,2} with an empty SWIO Mod 3, the current load is 75.2A (102.2 minus 27).

# Optical Extension Power (OPEX PWR) Module

The Optical Extension Power (OPEX PWR) Module (Figure 5-16) receives -48V power from the Battery Distribution Feeder Board(s) (BDFB). The fuse boards receive -5V from the Auxiliary Power Module. Seven power feeders and seven returns are terminated at the OPEX Bay and provide power for the entire Remote Complex. Table 5-10 lists the circuit packs contained in the OPEX Power Module.

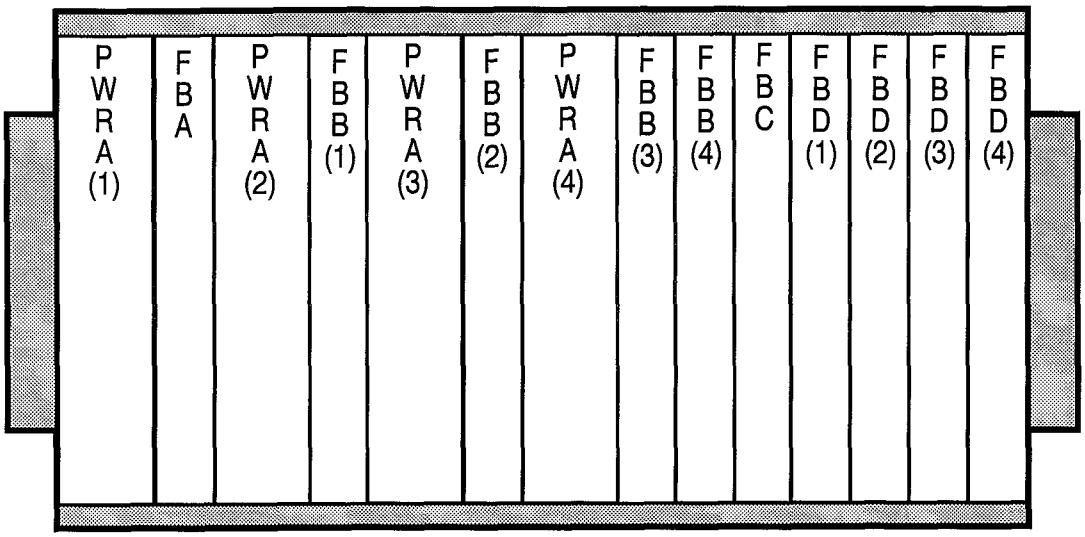



Figure 5-16. **OPEX Power Module**

Table 5-10. **OPEX Power Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PWRA | Power A | 4 |
| FBA | Fuse Board A | 1 |
| FBB | Fuse Board B | 4 |
| FBC | Fuse Board C | 1 |
| FBD | Fuse Board D | 4 |

Figure 5-17 shows a detailed block diagram of the OPEX Power Module. The functions provided by the circuit packs within the OPEX Power Module are summarized in the following sections.

## Power A (PWRA)

The PWRA circuit pack provides +5V power to the Optical Extension Module. The four PWRA power circuit packs provide the low-voltage power to common busses that are distributed to the Remote Complex. If a single PWRA power circuit pack fails, the remaining PWRA power circuit packs are sufficient to support low-voltage power to the common busses. Alarm and equipage information is supplied to the UIA circuit pack of the RUI Module from each PWRA circuit pack.

Each PWRA circuit pack receives -48V power from one of the Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse and Alarm Panel located in the OPEX Bay

## Fuse Board A (FBA) and Fuse Board B (FBB)

These five fuse boards (one FBA and four FBBs) are equipped with 77-type fuses and provide fuse protection for the +5V power supply to the Optical Extension Module.

## Fuse Board C (FBC) and Fuse Board D (FBD)

These five fuse boards (one FBC and four FBDs) are equipped with 78-type fuses and provide fuse protection for the -5V power supply to the Optical Extension Module.

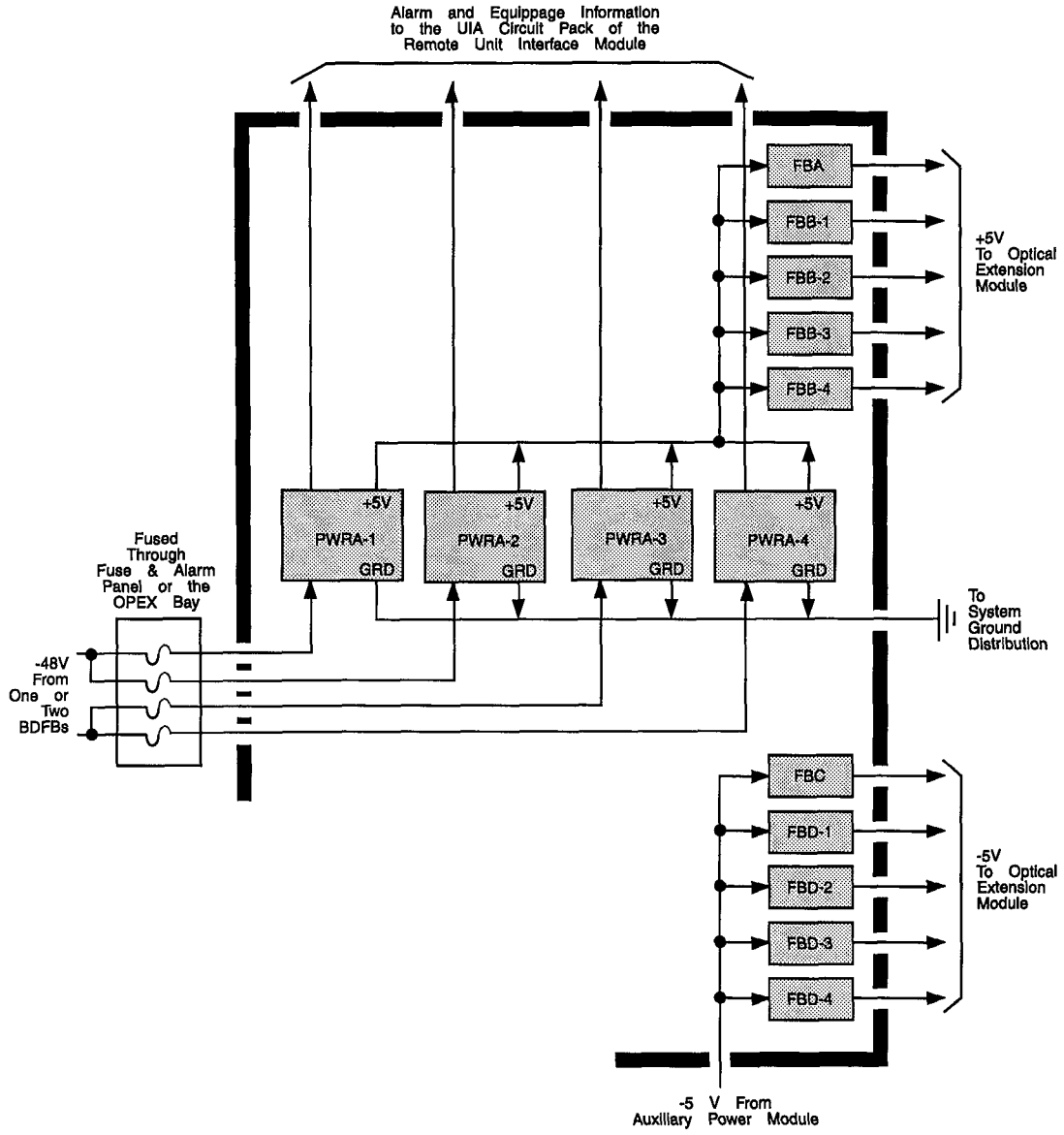



Figure 5-17. **OPEX Power Module**

# Remote Unit Interface Power (RUI PWR) Module

The Remote Unit Interface Power (RUI PWR) Module (Figure 5-18) replaces the Redundant Controller Power (RC PWR) Module and provides power to the RUI Module. Table 5-11 lists the circuit packs contained in the RUI Power Module.

Figure 5-19 shows a detailed block diagram of the RUI Power Module.The functions provided by the circuit packs within the RUI Power Module are summarized in the following sections.

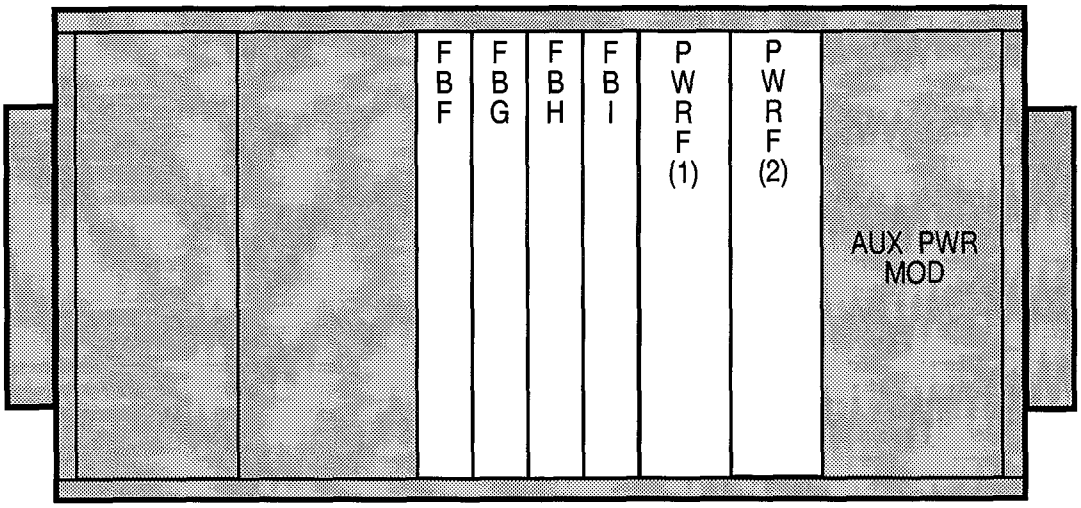
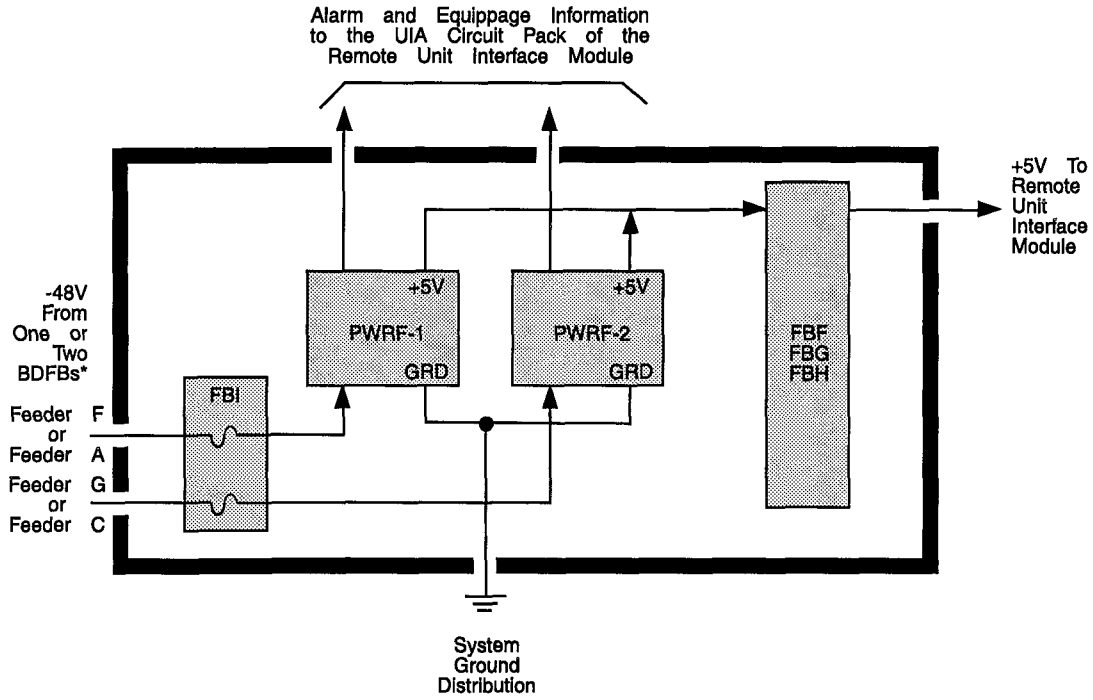



Figure 5-18. **RUI Power Module**

Table 5-11. **RUI Power Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PWRF | Power F | 2 |
| FBF | Fuse Board F | 1 |
| FBG | Fuse Board G | 1 |
| FBH | Fuse Board H | 1 |
| FBI | Fuse Board I | 1 |




* When using one BDFB, feeders F and G supply power to the RUI Power Module. When using two BDFBs, feeders A (fuse A1) and C (fuse C1) supply power to the RUI Power Module. If fuse A1 fails, -48V power to PWRF-1 is lost. Likewise, if fuse C1 fails, -48V power to PWRF-2 is lost.

Figure 5-19. **RUI Power Module Block Diagram**

## Power F (PWRF)

The PWRF circuit pack provides power to the Remote Unit Interface (RUI) Module. Each PWRF circuit pack receives -48V power from one of the Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse Board I (FBI).

## Fuse Board F (FBF), Fuse Board G (FBG), and Fuse Board H (FBH)

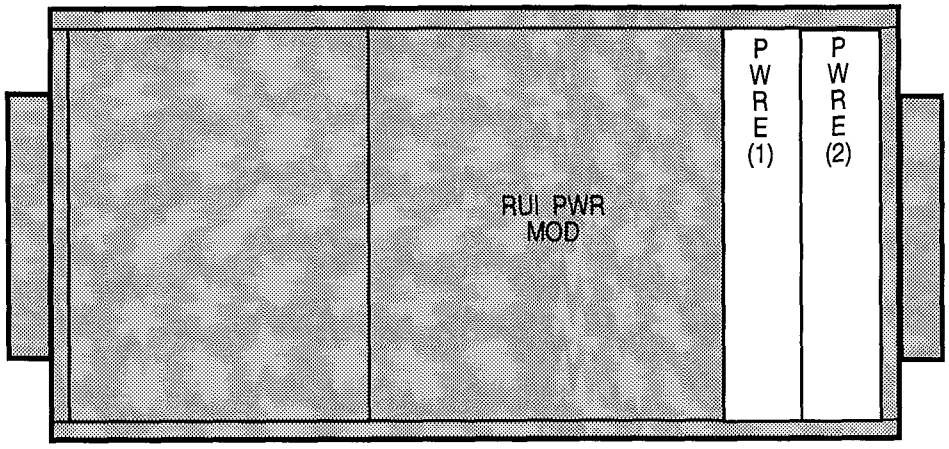
These fuse boards provide fuse protection for the +5V power supply to the Remote Unit Interface Module.

### Fuse Board I (FBI)

The FBI circuit pack provides fuse protection for power feeders connected directly to the RUI PWR Module.

## Auxiliary Power (AUX PWR) Module

The Auxiliary Power (AUX PWR) Module provides the -5V power for the OPEX Module. Figure 5-20 shows the circuit pack locations in the Auxiliary Power Module. Table 5-12 lists the Auxiliary Power Module circuit packs, their functions, and quantity.




**Note:** Number in parentheses is circuit pack position number in module.

Figure 5-20. **Auxiliary Power Module**

Table 5-12. **Auxiliary Power Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PWRE3 | Power E3 | 2 |

Figure 5-21 shows a detailed block diagram of the Auxiliary Power Module. Power E (PWRE) supplies -5V power to the OPEX Module through the -5V 78-type fuses located in the OPEX Power Module. Each PWRE circuit pack provides redundant power for its mate circuit pack. Alarm and equipage information is supplied to the UIA circuit pack of the Remote Unit Interface (RUI) Module from each PWRE circuit pack.

### Power E (PWRE)

Each PWRE circuit pack receives -48V power from one of the Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse and Alarm Panel located in the OPEX Bay.

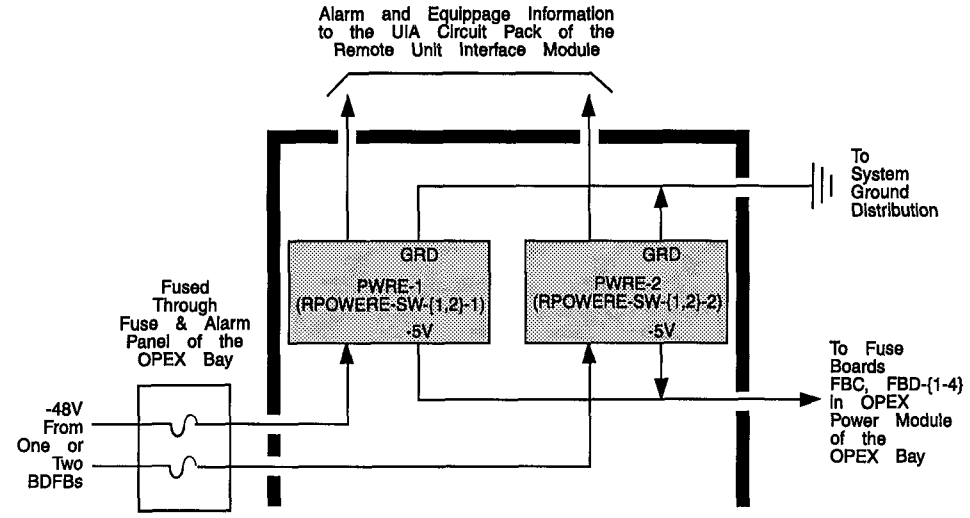



Figure 5-21. **Auxiliary Power Module Block Diagram (Remote Complex)**

## Remote Complex Configuration Circuit Packs

Table 5-13 lists the circuit pack equipment for Remote Complex configurations. Included in Table 5-13 are circuit packs used in the Switch Complex and the OPEX Bay for Remote Complex configurations.

Table 5-13. **Circuit Pack Equipment for Remote Complex Configurations**

| Functional Name | Circuit Pack or Equipment Code | Used In | Number Required | See Note |
|---|---|---|---|---|
| AWR-type filler assembly | 846103760 | OPEX Mod | As required | 1 |
| AWS-type filler assembly | 846960664 | SYNC Mod | 2 | |
| Apparatus blank cover | 847055563 | SWIO Mod | As required | 2 |
| BXC1 (Bus Extender C 1) | AWP20 | RUI Mod | 1 | |
| CLKGN3 (Clock Generator 3) | AWR11 | OPEX Mod | 1 (upper tier) | |
| CLKGN4 (Clock Generator 4) | ERA6B | SWCS Mod | 1 per module | 3 |
| CPU3 (Central Processing Unit 3) | ERA2 | HCC Mod | 2 | |
| DPLL1/DPLL2 (Digital Phase Lock Loop 1/2) | AWP9B/AWP15 | SYNC Mod | 2 | 4 |
| DS1TX1/DS1TX2 (DS1 Timing Extractor 1/2) | AWS5/AWS9 | SYNC Mod | 2 | 4 |
| ECI6 (Enhanced Communications Interface 6) | ERA1 | HCC Mod | 2 | 5 |
| FBA (Fuse Board A) | ED2C962-30 | OPEX PWR Mod | 1 | |
| FBB (Fuse Board B) | ED2C960-30 | OPEX PWR Mod | 4 | |
| FBC (Fuse Board C) | ED2C963-30 | OPEX PWR Mod | 1 | |
| FBD (Fuse Board D) | ED2C961-30 | OPEX PWR Mod | 4 | |
| FBF (Fuse Board F) | ED9C051-30 | RUI PWR Mod | 1 | |
| FBG (Fuse Board G) | ED9C052-30 | RUI PWR Mod | 1 | |
| FBH (Fuse Board H) | ED9C053-30 | RUI PWR Mod | 1 | |
| FBI (Fuse Board I) | ED9C055-30 | RUI PWR Mod | 1 | |
| FBJ (Fuse Board J) | ERE2 | MEM Mod | 1 | |
| FBK (Fuse Board K) | ERD1 | SW PWR Mod | 4 | |
| FBL (Fuse Board L) | ERE3 | MEM Mod | 1 | |
| FBM (Fuse Board M) | ERD2 | SW PWR Mod | 3 | |

Table continued on next page; notes are listed at end of table.

Table 5-13. **Circuit Pack Equipment for Remote Complex Configurations (Continued)**

| Functional Name | Circuit Pack or Equipment Code | Used In | Number Required | See Note |
|---|---|---|---|---|
| MTC4 (Maintenance Interface 4) | ERA9 | HCC Mod | 4 | 6 |
| OPEX1 (Optical Extension 1) | ERW3 | OPEX Mod | 2-32 | 7 |
| OSWIO1 (Optical Switch Input/Output 1) | ERY1 | SWIO Mod | 0-16 | 7,8 |
| OUI1 (Optical Unit Interface 1) | ERT1 | HCC Mod | 2 | 9 |
| PRI4 (Primary off-line storage 4) | ERB2 | MEM Mod | 2 | |
| PWRA (Power A) | 552A (standard)<br>566A (duplex) | OPEX PWR Mod | 4 | |
| PWRF (Power F) | 427AA/427AB | RUI PWR Mod | 2 | |
| PWRG (Power G) | 428AB | MEM Mod | 2 | |
| PWRJ (Power J) | 568A or<br>568B | SW PWR Mod | 6 per module | 10 |
| RCI1 (Remote Communications Interface 1) | AWP19 | RUI Mod | 2 | 11 |
| SCI3 (Switch Communications Interface 3) | AWR2C | RUI Mod | 1 | |
| SCI4 (Switch Communications Interface 4) | ERA8 | HCC Mod | 4 | |
| SEC4 (Secondary off-line storage 4) | ERB3 | MEM Mod | 1 | |
| SSC4 (Secondary Storage Controller 4) | ERA7 | HCC Mod | 2 | |
| STPNL1 (Status Panel 1) | ED-9C049-30 | RUI Mod | 1 | |
| STPNL2 (Status Panel 2) | ED-9C138-30 | HCC Mod | 1 | |
| SWCS3 (Switch Center Stage 3) | ERA5 | SWCS Mod | 16 | 12 |
| SWIO2 (Switch Input/ Output 2) | ERA4 | SWIO Mod | 0-16 | 7,8 |

Table continued on next page; notes are listed at end of table.

Table 5-13. **Circuit Pack Equipment for Remote Complex Configurations (Continued)**

| Functional Name | Circuit Pack or Equipment Code | Used In | Number Required | See Note |
|---|---|---|---|---|
| TBS31/TBS32 (Time Base Stratum 3 1/2) | AWS3/AWS8 | SYNC Mod | 2 | 4 |
| UIA1 (Unit Interface A 1) | ERW1 | RUI Mod | 1 | |
| UIB1 (Unit Interface B 1) | ERW2 | RUI Mod | 1 | |

Notes:

1. The AWR-type filler assemblies are installed in the OPEX Module in place of OPEX (ERW3) circuit packs when the OPEX Module is not equipped with the full complement of 32 OPEX circuit packs.
2. The blank apparatus covers (double width) are installed in the SWIO Module in place of SWIO (ERA4) or OSWIO (ERY1) circuit packs when the four SWIO Modules are not equipped with the full complement of 64 SWIO/OSWIO circuit packs.
3. Must use two identical CLKGN4 circuit packs (slots labeled CLKGN in the SWCS Modules).
4. Version 2 synchronizer circuit packs replace version 1 circuit packs for new systems. Existing systems can use either version circuit packs. Version 1 and 2 circuit packs can not be mixed within the same SYNC Module.
5. Two ECI6 circuit packs can exist; the administrative links associated with each circuit pack are 1-1 through 1-8 for ECI-1, and 2-1 through 2-8 for ECI-2.
6. Must use two identical MTC4 circuit packs (slots labeled MTC in the HCC Module).
7. No SWIO or OSWIO circuit packs can be contained in an SWIO Module provided at least one SWIO Module contains two SWIO or OSWIO circuit packs.
8. The SWIO, OSWIO, and OPEX circuit packs are installed in pairs. SWIO and OSWIO circuit packs can not be mixed within the same Switch Bay.
9. OUI1 circuit packs can be used in a collocated arrangement; however, UI3 circuit packs cannot be present if at least one Remote Complex is provisioned.
10. For systems with at least one Remote Complex, SW PWR Modules 1 and 3 must be equipped with eight new PWRJ (568B) circuit packs (that is, PWRJ-{1,3}-{1,2,5,6}). For systems with only collocated interfaces, SW PWR Modules 1 and 3 can have either version of PWRJ circuit packs (that is, 568A or 568B). SW PWR Module 2 can be equipped with either version of PWRJ circuit packs (that is, 568A or 568B).
11. Two RCI1 circuit packs can exist; the administrative link associated with RCI-1 is 1-7 or 1-8 and the administrative link associated with RCI-2 is 2-7 or 2-8.
12. Two identical SWCS Modules are required.

# Interface Bay Hardware

# 6

## Contents


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# Interface Bay Hardware

# 6

The interface bays provide the interface between the DACS IV-2000 and the incoming and outgoing facilities or network elements.

DS1 Interface Modules connect signals at the DS1 rate. Up to 8 DS3 equivalents are supported, plus one protection DS3 equivalent.

DS3 Interface Modules connect signals at the DS3 rate. Two shelf sizes are available: the Interface-16 supports 15 DS3 equivalents plus one protection DS3 equivalent, and the Interface-32 supports 31 DS3 equivalents plus one protection DS3 equivalent. Support of DS3 clear-channel signaling is available in the DS3 Clear-Channel Interface-16 Module.

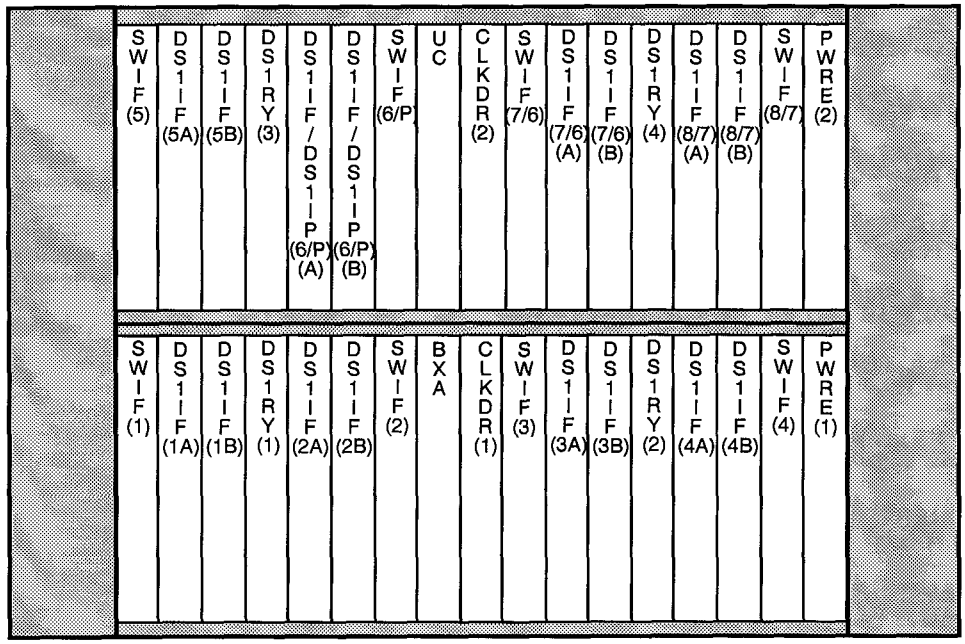
STS-1 Interface Modules connect signals at the STS-1 and VT1.5 rates. Up to 15 STS-1 equivalents are supported, plus one protection STS-1 equivalent. You cannot mix interface types (DS1/DS3/STS1) within the same shelf. The DACS IV-2000 interface modules are listed below:

- DS1 Interface (DS1 INTFC) Module
- DS1 Interface-Protection (DS1 INTFC-P) Module
- DS3 Interface-32 (DS3 INTFC-32) Module
- DS3 Interface-16 (DS3 INTFC-16) Module
- Enhanced DS3 Interface-16 (ENH DS3 INTFC-16) Module
- DS3 Clear-Channel Interface-16 (DS3CC INTFC-16) Module
- STS1 Interface-16 (STS1 INTFC-16) Module.

Each of these modules is described in the following sections.

## DS1 Interface Modules

DS1 interface modules (Figure 6-1) provide the interface for incoming and outgoing DS1 facilities or network elements. These modules accept DS1 signals (in a format that is compatible with a DSX-1) and switch these signals to and from the Switch Module. There are two types of DS1 interface modules, DS1 Interface and DS1 Interface-Protection.




**Note**: Number in parentheses is circuit pack position number on module. For entries with slashes (/), the entry before the slash corresponds to the DS1 Interface Module and the entry after the slash corresponds to the DS1 Interface-Protection Module.

Figure 6-1. **DS1 Interface/Interface-Protection Module**

The DS1 Interface consists of eight working groups, all used for service. The DS1 Interface-Protection consists of eight working groups, seven used for service and one used to provide protection for all working groups within the associated Interface Bay. A DS1 Interface Module must always be connected to a DS1 Interface-Protection Module for protection purposes. The protection group in the DS1 Interface-Protection Module protects the seven working groups in that module along with the eight working groups in the other DS1 Interface Modules that are connected to it. Up to three DS1 Interface Modules can be connected to a DS1 Interface-Protection module for this purpose, giving a maximum protection ratio of 1 to 31.

Table 6-1 lists the circuit packs contained in a DS1 Interface Module; Table 6-2 lists the circuit packs contained in a DS1 Interface-Protection Module.

Table 6-1. **DS1 Interface Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC4/UC4B* | Unit Controller 4 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| SWIF1 or SWIF2 | Switch Interface 1<br>Switch Interface 2<br>(SWIF2 circuit packs are required for the DS1 performance monitoring option.) | 1 to 8 |
| PMGR1 | Performance Monitor Test Signal Generator Receiver 1<br>(Optional; used for DS1 Performance Monitoring feature and replaces SWIF circuit packs.) | 0 to 8 |
| DS1RY1 | DS1 Relay 1 | 4 |
| DS1IF1 | DS1 Interface 1<br>(Installed in pairs.) | 2 to 16 |
| CLKDR2 | Clock Distributor 2 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped SWIF and DS1IF circuit pack slots of provisioned or non-provisioned DS1 Interface Modules associated with a provisioned DS1 Interface-Protection Module.) | 21 to 1 |

* UC4 circuit packs are required for collocated interface modules. UC4B circuit packs are required in Remote Complex interface modules.

Table 6-2. **DS1 Interface-Protection Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC4/UC4B* | Unit Controller 4 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| SWIF1 or SWIF2 | Switch Interface 1<br>Switch Interface 2<br>(SWIF2 circuit packs are required for the DS1 performance monitoring option.) | 1 to 8<br>(1 provisioned as SWIF-P) |
| PMGR1 | Performance Monitor Test Signal Generator Receiver 1<br>(Optional: used for DS1 Performance Monitoring feature and replaces SWIF circuit packs.) | 0 to 7 |
| DS1RY1 | DS1 Relay 1 | 4 |
| DS1IF1 | DS1 Interface 1<br>(Installed in pairs.) | 2 to 14 |
| DS1IP1 | DS1 Interface (Protection) 1 | 2 |
| CLKDR2 | Clock Distributor 2 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped SWIF and DS1IF circuit pack slots in a provisioned DS1 Interface-Protection Module.) | 19 to 1 |

* UC4 circuit packs are required for collocated interface modules. UC4B circuit packs are required in Remote Complex interface modules.

The functions of a DS1 Interface Module and the relationship existing in a DS1 protection group (all DS1 Interface Modules contained in a DS1 or STS1/DS3/DS1 Interface Bay) are described in the following sections.

## DS1 Timing/Synchronization, Control, and Power

Figure 6-2 (depicts the collocated) and Figure 6-3 (depicts the Remote Complex) are block diagrams of the timing/synchronization, control, and power distribution within a DS1 Interface or DS1 Interface-Protection Module for collocated and remote configurations, respectively. The functions provided by the circuit packs are described in the following sections.

**NOTE:**
In the following sections, the descriptions for the SWIO circuit packs also pertain to the OSWIO/OPEX[1] circuit packs.

### Power E (PWRE)

The PWRE circuit pack supplies +5V power to the other circuit packs within the associated DS1 Interface Module. Each PWRE circuit pack can supply power for the entire DS1 Interface Module if required due to PWRE circuit pack failure. Error summary information is provided to the MTC circuit packs in collocated interface bays, or to the UIA or UIB circuit packs in the Remote Complexes. Alarm and power indication LEDs are controlled by the UC circuit pack.

Each PWRE circuit pack is supplied -48V power from one or both Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse and Alarm Panel located in the Fuse and Alarm Bays for collocated interface modules or the Fuse and Alarm Panel located in the OPEX Bay for Remote Complex interface modules.

### Unit Controller (UC)

The UC circuit pack monitors the DS1 Interface Module hardware to detect and isolate faults and to monitor facilities. The UC circuit pack communicates (providing control) with other DS1 interface module circuit packs over 6.176-Mb/s serial control links. Other inputs to the UC allow for error summary of all circuit packs within the DS1 Interface Module. Outputs from the UC control the LEDs associated with other DS1 Interface Module circuit packs. The UC communicates (system control) with the main controller over the 10-Mb/s LAN. Software for the UC circuit pack is also downloaded from the main controller (the system disk) over the 10-Mbs/s LAN. The UC provides error summary information to and receives reset signals from the MTC (UIA or UIB) circuit packs. In addition, the UC provides protection switch control through the DS1IF, DS1IP, and DS1RY circuit packs.

**NOTE:**
Use the UC4 circuit pack in collocated configurations; use the UC4B circuit pack for Remote Complex configurations.

1. For remote interface modules, the N-rate signals are extended to the OSWIO circuit packs through OPEX circuit packs and associated optical fiber cables. OPEX circuit packs do not perform any switching functions.

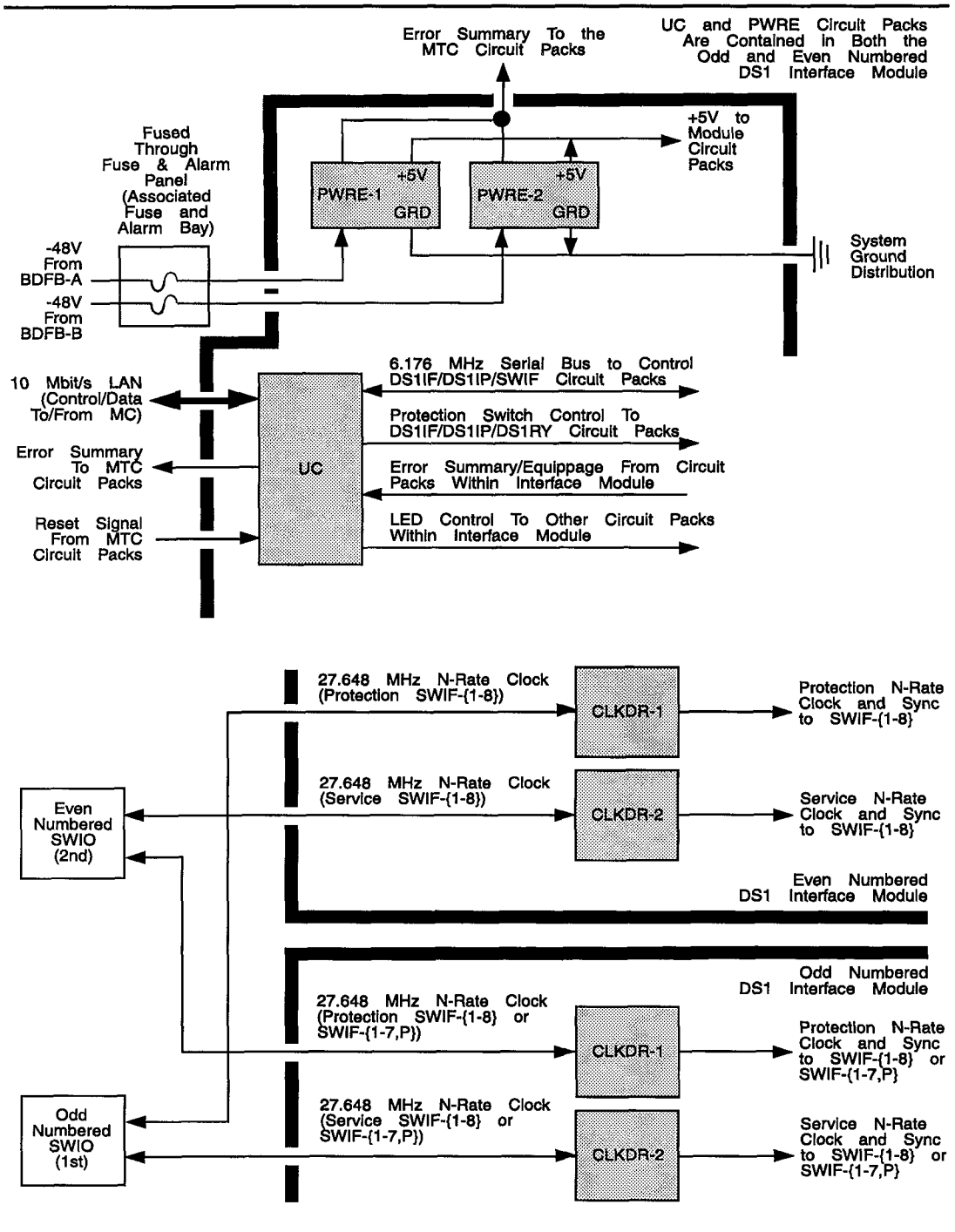



Figure 6-2. **DS1 Interface Module Block Diagram - Control (Collocated Interface Modules)**

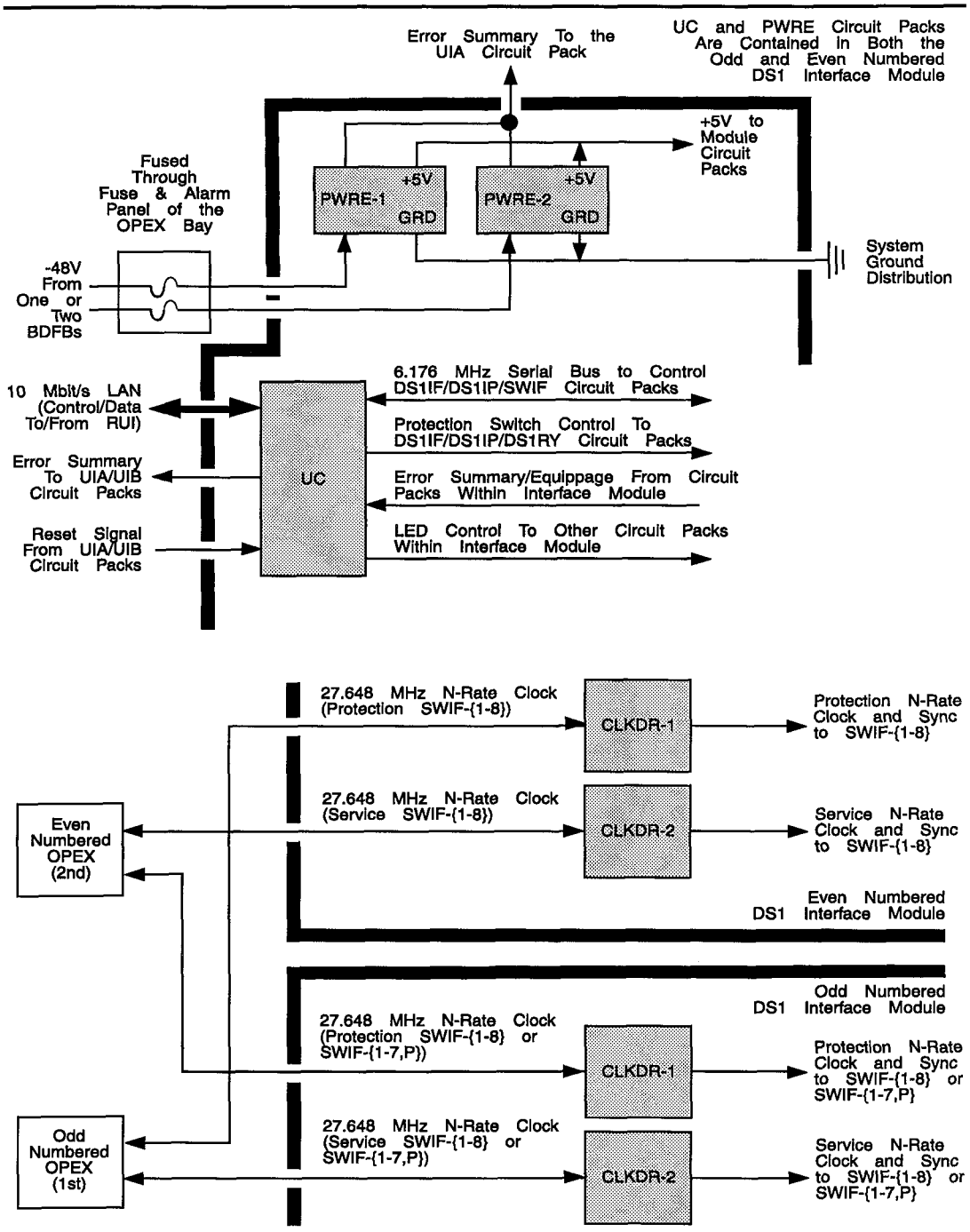



Figure 6-3. **DS1 Interface Module Block Diagram - Control (Remote Complex Interface Modules)**

## Clock Distributor (CLKDR)

The CLKDR circuit pack and its associated SWIO (or OSWIO) circuit pack provide N-rate synchronization for the SWIF circuit packs. The CLKDR circuit packs receive N-rate clock (27.648-MHz) and N-rate synchronizing (123.429-KHz) signals from SWIO (or OSWIO) circuit packs in the Switch Complex (over the N-rate cable) and distribute these signals to the SWIF circuit packs. One CLKDR circuit pack provides service timing signals to the eight SWIF circuit packs, and the other CLKDR circuit pack provides protection timing signals to the same eight SWIF circuit packs. In addition, the CLKDR circuit pack reclocks the N-rate clock and synchronizing signals and sends them back to the SWIO (or OSWIO) circuit packs (over the N-rate cable).

A SWIO (or OSWIO/OPEX) circuit pack pair [two adjacent SWIO (or OSWIO/OPEX) circuit packs, the first odd-numbered and the second even-numbered] provide service for 16 equivalent DS3 signals (the OPEX circuit pack extends the N-rate signals to the OSWIO circuit pack). DS1 Interface Modules provide for eight DS3 equivalent signals, and DS1 Interface-Protection Modules provide for seven service and one protection DS3 equivalent signals. Therefore, one SWIO (or OSWIO/OPEX) circuit pack pair services two DS1 Interface Modules or one DS1 Interface and one DS1 Interface-Protection Modules. Therefore, separate CLKDR circuit packs provide service and protection timing signals to the SWIF circuit packs.

In this configuration, two CLKDR circuit packs (one from each DS1 Interface Module) are associated with each SWIO (or OSWIO/OPEX) circuit pack, unlike the DS3 and STS1 Interface Modules where only one CLKDR circuit pack is associated with each SWIO (or OSWIO/OPEX) circuit pack. CLKDR circuit packs within DS1 Interface Modules do not provide a typical 1-to-1 protection arrangement in that two CLKDR circuit packs are used to provide service and protection signals where one CLKDR circuit pack in a DS3 or STS1 Interface Module provides the same capabilities. For DS1 Interface Modules, special care must be taken when performing maintenance on SWIO/CLKDR (or OSWIO/OPEX/CLKDR) circuit pack combinations [one SWIO (or OSWIO/OPEX) circuit pack and two CLKDR circuit packs].

The bottom half of Figure 6-2 (or Figure 6-3) shows the timing signal distribution from the SWIO (or OSWIO/OPEX) circuit pack pair to the CLKDR circuit packs of the two adjacent DS1 Interface Modules (the bottom one is odd-numbered and the top one is even-numbered). Under normal conditions (no failures or protection switches), the odd-numbered DS1 Interface Module's N-rate signals and CLKDR-2 is serviced by the odd-numbered SWIO (or OSWIO/OPEX) circuit pack (1st). The even-numbered DS1 Interface Module's N-rate signals and CLKDR-2 is serviced by the even-numbered SWIO (or OSWIO/OPEX) circuit pack (2nd). The SWIF circuit packs within a DS1 Interface Module normally receive timing from CLKDR-2.

The odd-numbered SWIO (or OSWIO/OPEX) circuit pack provides protection timing signals to the even-numbered DS1 Interface Module's CLKDR-1 circuit pack, and the even-numbered SWIO (or OSWIO/OPEX) circuit pack provides protection timing signals to the odd-numbered DS1 Interface Module's CLKDR-1 circuit pack.

If, for example, the odd-numbered SWIO (or OSWIO circuit pack is unable to provide service for any reason, all service in the odd-numbered DS1 Interface Module is switched to the even-numbered SWIO (or OSWIO) circuit pack. In this case, the even-numbered SWIO (or OSWIO) circuit pack is carrying the service (16 service DS1 groups or 15 service DS1 groups and 1 DS1 protection group) for both DS1 Interface Modules.

At the same time, CLKDR-2 of the odd-numbered DS1 Interface Module no longer provides timing. Instead CLKDR-1 provides the timing. The opposite is true if the even-numbered SWIO (or OSWIO) circuit pack is unable to provide service.

Tables 6-3 and 6-4 list the CLKDR circuit packs that provide timing (service) to the DS1 Interface Modules, given the status of the associated SWIO/OSWIO/OPEX circuit packs in collocated or Remote Complex interface modules, respectively. If it becomes necessary to replace a CLKDR circuit pack in a DS1 Interface Module, the status of the associated SWIO/OSWIO/OPEX circuit pack must be determined. If the associated SWIO/OSWIO/OPEX circuit pack is carrying service (active), manual commands must be entered to switch service to its mate circuit pack.

Table 6-3. **DS1 Interface Module — SWIO CLKDR Interworkings (Collocated Interface Modules)**

| SWIO Status | Traffic-Carrying CLKDR Circuit Packs | Standby CLKDR Circuit Packs |
|---|---|---|
| Odd SWIO Active<br>Even SWIO Active | Odd CLKDR-2<br>Even CLKDR-2 | Odd CLKDR-1<br>Even CLKDR-1 |
| Odd SWIO Active<br>Even SWIO Protected | Odd CLKDR-2<br>Even CLKDR-1 | Odd CLKDR-1<br>Even CLKDR-2 |
| Odd SWIO Protected<br>Even SWIO Active | Odd CLKDR-1<br>Even CLKDR-2 | Odd CLKDR-2<br>Even CLKDR-1 |

Table 6-4. DS1 Interface Module — OSWIO/OPEX CLKDR Interworkings (Remote Complexes)

| SWIO Status | Traffic-Carrying CLKDR Circuit Packs | Standby CLKDR Circuit Packs |
|---|---|---|
| Odd OSWIO/OPEX Active<br>Even OSWIO/OPEX Active | Odd CLKDR-2<br>Even CLKDR-2 | Odd CLKDR-1<br>Even CLKDR-1 |
| Odd OSWIO/OPEX Active<br>Even OSWIO/OPEX Protected | Odd CLKDR-2<br>Even CLKDR-1 | Odd CLKDR-1<br>Even CLKDR-2 |
| Odd OSWIO/OPEX Protected<br>Even OSWIO/OPEX Active | Odd CLKDR-1<br>Even CLKDR-2 | Odd CLKDR-2<br>Even CLKDR-1 |

## DS1 Transmission

Figure 6-4 is a block diagram of the transmission paths within a DS1 Interface or DS1 Interface-Protection Module. The functions provided by the circuit packs are described in the following sections.

### DS1 Interface (DS1IF)

The DS1IF circuit pack terminates 14 two-way DS1 signals (1.544-Mbs/s). The format of the DS1 signals can be either alternate mark inversion (AMI) or bipolar with 8-zero substitution (B8ZS), selected on a per-port basis (refer to Chapter 5 in the *DACS IV-2000 (512) Release 5.0 Operations and Maintenance* manual [AT&T 365-340-901] for information on provisioning DS1 facilities). The following blocks are used to process DS1 signals in the receive direction:

- Digital Signal Interface — receives 14 DS1 bipolar signals and converts them to unipolar signals. In addition, the DS1 signals are routed to the Protection Relays circuitry. The functions performed are:
    1. Receive fourteen DS1 bipolar signals
    2. Extract clock
    3. Regenerate and retime data
    4. Detect and count bipolar violations (BPVs)
    5. Convert bipolar signals to unipolar signals; decode AMI or B8ZS format
    6. Shutdown clock if there is a loss of incoming signal with no internal loopback (LPBKI) set.

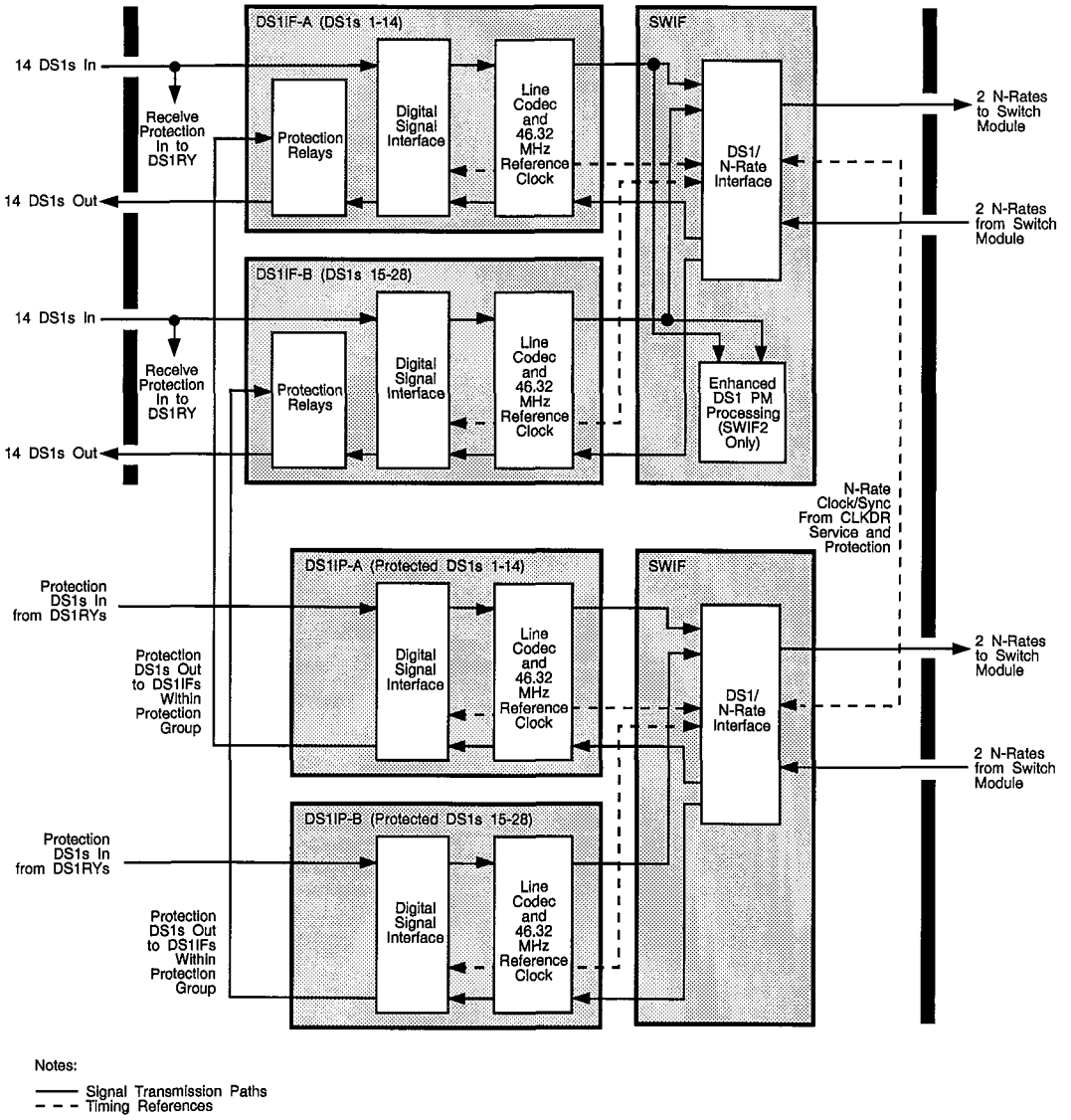



Figure 6-4. **DS1 Interface Module Block Diagram (Transmission Paths)**

In addition, provide for DS1 internal loopback (LPBKI, loopback from transmit to receive side) and DS1 line loopback (LPBKL, loopback from receive to transmit side).

- Protection Relays — connect the DS1IF to the receive side of the DS1RY circuit packs. The DS1RY circuit pack bridges two DS1 interface groups to the DS1 protection bus that is routed to the DS1IP circuit packs. Refer to the section titled "DS1 Protection Bus" (page 6-15) for more information.
- Line Codec and 46.32-MHz Reference Clock — receives 14 DS1 unipolar signals from the Digital Signal Interface and modifies and outputs signals to the SWIF circuit pack. The functions performed are:
    1. Receive 14 unipolar DS1 signals from the Digital Signal Interface circuitry
    2. Detect loss-of-clock (LOC)
    3. Autonomously insert AIS signal during an LOC condition
    4. Insert test data (1011000) toward the SWIF circuit pack
    5. Detect test data from the Digital Signal Interface circuitry.
    6. Detect test data from the Digital Signal Interface circuitry.

The following blocks are used to process DS1 signals in the transmit direction:

- Line Codec and 46.32-MHz Reference Clock — receives fourteen DS1 unipolar signals from the SWIF circuit pack and synchronizes the data to the DS1 rate and output to the Digital Signal Interface circuitry. The functions performed are:
    1. Receive 14 unipolar DS1 signals from the SWIF circuit pack
    2. Generate 1.544-MHz DS1 clock to synchronize data to the DS1 rate
    3. Detect loss-of-clock (LOC)
    4. Detect loss-of-data (AMI mode only)
    5. Detect test data (1011000) from the SWIF circuit pack
    6. Insert AIS signal, if provisioned to do so
    7. Autonomously insert AIS signal during an LOC condition
    8. Autonomously insert AIS signal during a loss-of-data condition in the AMI mode.
- Digital Signal Interface — receives 14 DS1 bipolar signals and converts them to unipolar signals. In addition, the DS1 signals are routed to the Protection Relays circuitry. The functions performed are:
    1. Receive 14 unipolar DS1 signals from the Line Codec and 46.32-MHz Reference Clock circuitry
    2. AMI or B8ZS coding (software controlled or through hardware switches)
    3. Equalize output waveform to meet the DS1 template specification (software controlled or through hardware switches)

4. Convert unipolar signal to bipolar signal
5. Provide for DS1 internal loopback (LPBKI, loopback from transmit to receive side) and DS1 line loopback (LPBKL, loop back from receive to transmit side).

- Protection Relays— connects the DS1IF to the transmit side of the DS1RY circuit packs. The DS1RY circuit pack bridges two DS1 interface groups to the DS1 protection bus that is routed to the DS1IP circuit packs. The protection relay determines if the DS1 signals are output from the DS1IF or DS1IP circuit pack. Refer to the section titled "DS1 Protection Bus" (page 6-15) for more information.

### Switch Interface (SWIF)

The SWIF circuit pack sends and receives N-rate signals (27.648-Mb/s) to and from the Switch Module. The following blocks are used to process DS1 signals in the receive direction:

- DS1/N-Rate Interface — multiplexes the 28 DS1 signals into two service and two protection N-rate signals and sends the N-rate signals to the Switch Module. The functions performed are:
  1. Receive 28 DS1 signals from the two associated DS1IF/DS1IP circuit packs and multiplex into 28 N-rate channels on the two N-rate signals
  2. Generate and insert stuff channel parity over the DS1
  3. Generate and embed N-rate parity over the 16-bit N-rate data block
  4. Generate two N-rate balanced signals (upper and lower) and drive both service and protection interfaces
  5. Monitor service and protection N-rate clock
  6. Monitor N-rate sync for the 123-kHz sync information
  7. Monitor and generate DS1 AIS.
- Enhanced DS1 PM Processing (SWIF2 circuit pack contained in an DS1 interface group only) — processes the information received from the DS1/N-Rate Interface circuitry (in the receive direction only) to allow collection of enhanced DS1 performance monitoring data for dedicated full-time monitoring. No DS1 performance monitoring data is collected for protected DS1 signals.

The following blocks are used to process DS1 signals in the transmit direction:

- DS1/N-Rate Interface — demultiplexes the received cross-connected N-rate signals from the Switch Module into 28 DS1 signals. The lower DS1 signals (1-14) are output to the DS1IF/DS1IP circuit pack designated A, and the upper DS1 signals (15-28) are output to the DS1IF/DS1IP circuit pack designated B. The functions performed are:
    1. Receive service and protection balanced CMOS clock and sync from backplane
    2. Monitor service and protection N-rate clock
    3. Monitor service and protection N-rate sync for 123-kHz sync information
    4. Perform N-rate clock and sync protection switching under software control
    5. Receive service and protection N-rate data sets (upper and lower) and perform protection switching under software control
    6. Monitor service and protection N-rate data inputs for N-rate parity errors
    7. Demultiplex N-rate channels to DS1 signals, monitor each DS1 stuff channel parity for errors to maintain cross-connect, and output the lower 14 DS1 signals (1-14) to the DS1IF/DS1IP circuit pack designated A and the upper 14 DS1 signals (15-28) to the DS1IF/DS1IP circuit pack designated B.

### DS1 Interface Protection (DS1IP)

The DS1IP circuit pack provides protection for DS1IF circuit packs within an interface protection group (that is, all DS1 interface groups within the same interface bay). DS1IP circuit packs perform the same functions as DS1IF circuit packs (except for protection relay and hardware switch functions) when active. In a DS1 Interface Bay, protection for DS1 facilities is provided on a 1-to-31 basis. In a STS1/DS3/DS1 Interface Bay protection for DS1 facilities is provided on a 1-to-15 basis.

### Performance Monitor Generator/Receiver (PMGR)

The PMGR circuit pack allows bridged access DS1 performance monitoring. PMGR circuit packs replace SWIF circuit packs (except protection group SWIF).

## DS1 Protection Bus

Figure 6-5 is a block diagram of the protection bus within a DS1 protection group (that is, all DS1 Interface and DS1 Interface-Protection Modules within a interface bay). The functions provided by the circuit packs are described in the following sections.

### DS1 Interface (DS1IF)

The DS1IF circuit packs contain protection relays, which when activated allow for the 14 DS1 signals to be processed by the associated DS1IP circuit pack. The 30 DS1IF circuit packs within a STS1/DS3/DS1 Interface Bay or the 62 DS1IF circuit packs within a DS1 Interface Bay are bridged together in pairs (for example DS1IF-1A/DS1IF-2A and DS1IF-1B/DS1IF-2B) and routed to DS1RY circuit packs (8 in STS1/DS3/DS1 Interface Bays and 16 in DS1 Interface Bays).

### DS1 Relay (DS1RY)

The DS1RY circuit pack provides protection relays for two DS1 Interface Groups and routes the DS1 signals to the DS1IP circuit packs. Each DS1RY circuit pack serves two DS1 interface groups. Each of the 56 DS1 signals received by the two interface groups is also bridged to be received by the DS1RY circuit pack. If a DS1IF or a SWIF circuit pack fails, the UC/DS1IF directs the DS1RY circuit pack to send the 28 affected DS1 signals to the protection group and activates the associated protection relays within the DS1IF circuit packs within the failed DS1 interface group allowing the affected DS1 signals to be protected.

### DS1 Interface Protection (DS1IP)

The DS1IP circuit pack provides protection for DS1IP circuit packs within an interface protection group (that is, all DS1 interface groups within the same interface bay). The DS1RY circuit packs are directed to select the appropriate interface group by the UC and/or DS1IF circuit packs when protection for DS1 signals is needed. In a DS1 Interface Bay, protection for DS1/SWIF circuit packs is provided on a 1-to-31 basis. In a STS1/DS3/DS1 Interface Bay protection for DS1/SWIF circuit packs is provided on a 1-to-15 basis.

### Bus Extender A (BXA)

The BXA circuit packs installed in empty DS1IF and SWIF circuit pack slots to provide proper termination of DS1 signals and to keep out dust and foreign matter.

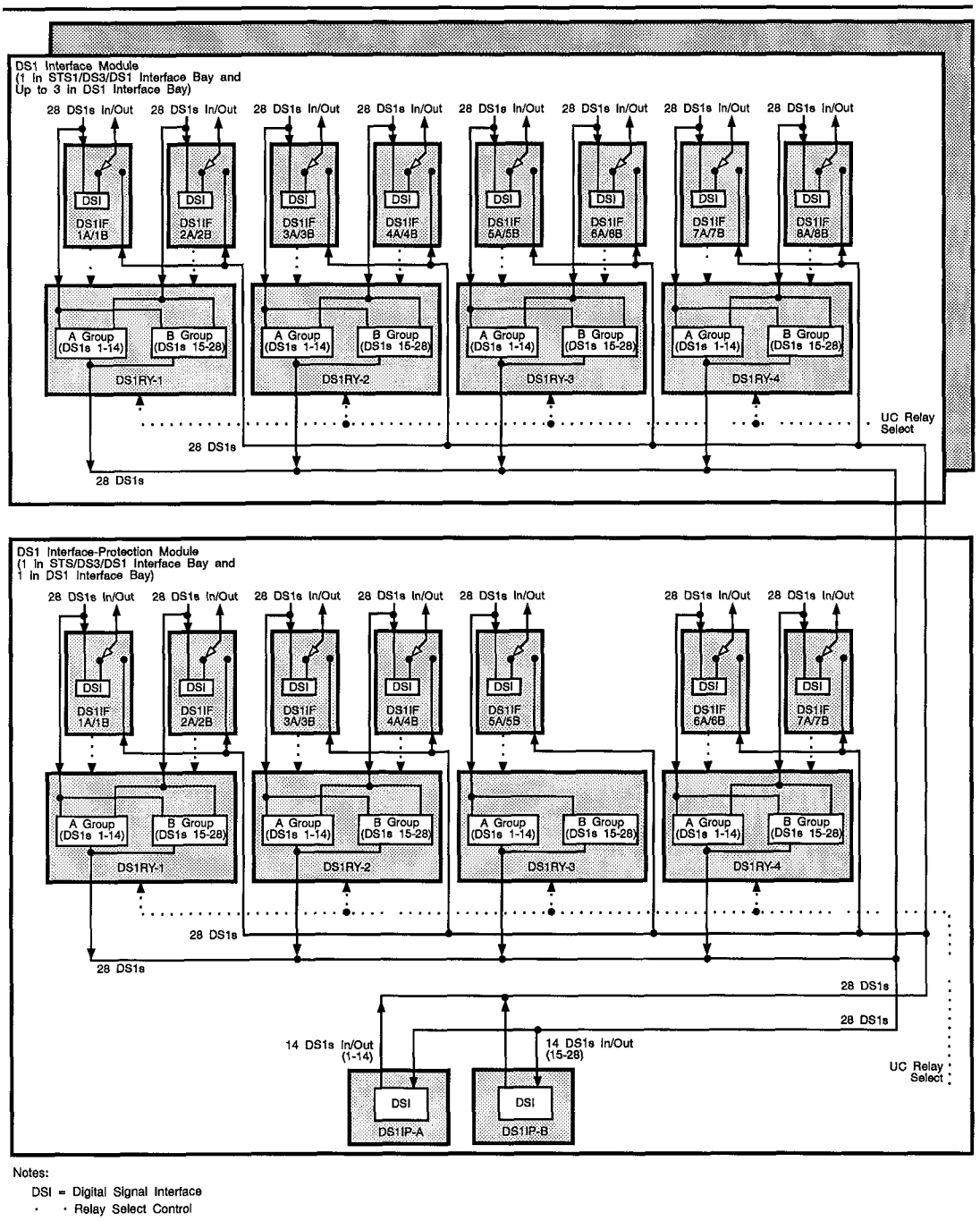


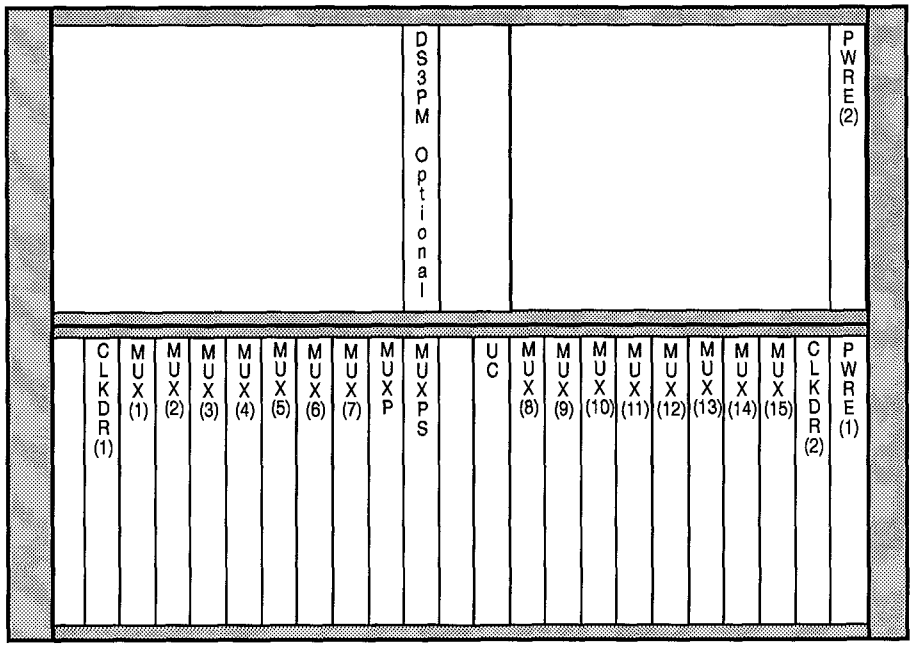

Figure 6-5. **DS1 Interface Module Block Diagram (Protection Bus)**

# DS3 Interface Modules

DS3 interface modules provide the interface for incoming and outgoing DS3 facilities or network elements. These modules accept DS3 signals (in a format compatible with a DSX-3) and switch these signals to and from the Switch Module.

The DS3 interface modules are described in the following sections.

- DS3 Interface-16 (DS3 INTFC-16) Module, Enhanced DS3 Interface-16 (ENH DS3 INTFC-16), and DS3 Clear-Channel Interface-16 (DS3CC INTFC-16) Modules — each supports 15 MUX circuit packs and one MUXP circuit pack (protection ratio of 1-to-15). Figure 6-6 represents each DS3 Interface-16 module, while Table 6-5 lists the circuit packs in the DS3 INTFC-16 Module, Table 6-6 lists the circuit packs in the ENH DS3 INTFC Module, and Table 6-7 lists the circuit packs in the DS3CC INTFC Module.




**Notes:**

Number in parentheses is circuit pack position number on module.

To implement DS1 performance monitoring features within a DS3 Interface-16 Module, one to fourteen MUX circuit packs are replaced with PMGR circuit packs. PMGR circuit packs cannot be used in the Enhanced DS3 or DS3 Clear-Channel Interface-16 Modules.

DS3PM2 circuit packs can only be installed in collocated DS3 Interface Modules. DS3PM circuit packs can not be used in Remote Complex interface modules.

Figure 6-6. **DS3 Interface-16 Module**

Table 6-5. **DS3 Interface-16 Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC4/UC4B* | Unit Controller 4 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| MUX1<br>MUX2 | Multiplexer 1<br>Multiplexer 2<br>(MUX2 circuit packs are required for enhanced DS3 performance monitoring and remote multiplexer communications features.) | 1 to15 |
| PMGR1 | Performance Monitor Test Signal Generator Receiver 1<br>(Optional; used for DS1 Performance Monitoring feature and replaces MUX circuit packs.) | 0 to 14 |
| MUXP1 or<br>MUXP2 | Multiplexer (Protection) 1<br>Multiplexer (Protection) 2 | 1 |
| MUXPS1 | Multiplexer Protection Switch 1 | 1 |
| DS3PM2† | DS3 Performance Monitor 2<br>(Optional, used for DS3 Performance Monitoring reporting to GTP) | 0 or 1 |
| CLKDR2 | Clock Distributor 2 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped MUX and DS3PM circuit pack slots. Provides proper termination for the interoffice DS3 signals.) | 15 to 0 |

* UC4 circuit packs are required for collocated interface modules. UC4B circuit packs are required in Remote Complex interface modules.

† DS3PM2 circuit packs can only be installed in collocated DS3 Interface Modules. DS3PM circuit packs can not be used in Remote Complex interface modules.

Table 6-6. **ENH DS3 Interface-16 Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC4/UC4B* | Unit Controller 4 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| MUX2<br>MUX3 | Multiplexer 2<br>Multiplexer 3 | 0 to 15<br>0 to 15 |
| MUXP3 | Multiplexer (Protection) 3 | 1* |
| MUXPS1 | Multiplexer Protection Switch 1 | 1 |
| DS3PM2† | DS3 Performance Monitor 2<br>(Optional, used for DS3 Performance Monitoring reporting to GTP) | 0 or 1 |
| CLKDR2 | Clock Distributor 2 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped MUX and DS3PM circuit pack slots. Provides proper termination for the interoffice DS3 signals.) | 15 to 0 |

* UC4 circuit packs are required for collocated interface modules. UC4B circuit packs are required in Remote Complex interface modules.

† DS3PM2 circuit packs can only be installed in collocated DS3 Interface Modules. DS3PM circuit packs can not be used in Remote Complex interface modules.

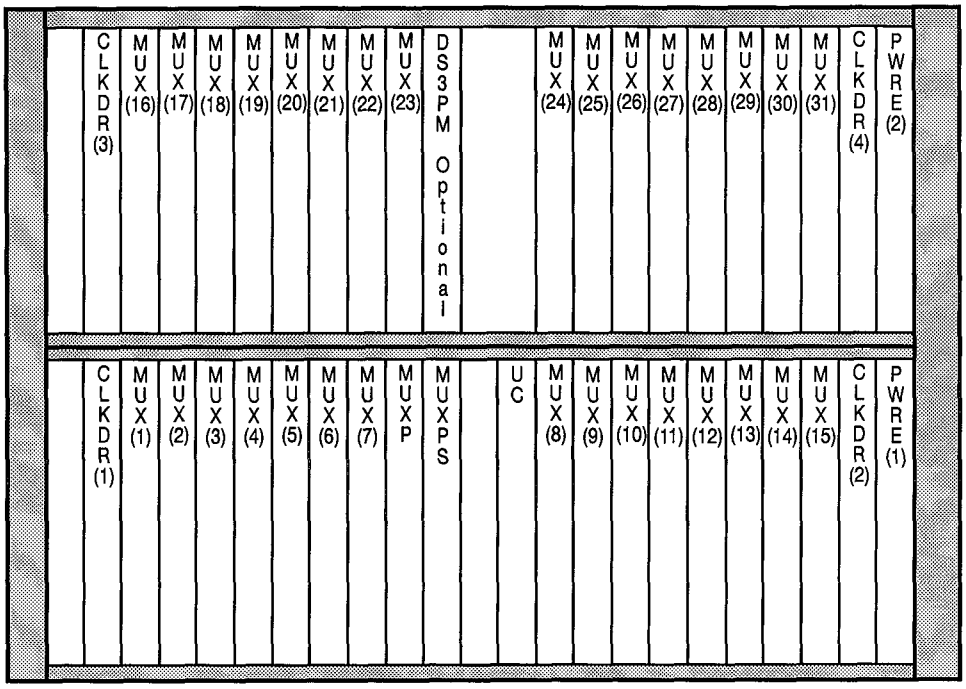
Table 6-7. **DS3CC Interface-16 Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC4/UC4B* | Unit Controller 4 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| MUX3 | Multiplexer 3 | 1 to 15 |
| MUXP3 | Multiplexer (Protection) 3 | 1 |
| MUXPS1 | Multiplexer Protection Switch 1 | 1 |
| DS3PM2† | DS3 Performance Monitor 2<br>(Optional, used for DS3 Performance Monitoring reporting to GTP) | 0 or 1 |
| CLKDR2 | Clock Distributor 2 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA2 | Bus Extender A2<br>(Inserted into unequipped MUX and DS3PM circuit pack slots. Provides proper termination for the interoffice DS3 signals.) | 15 to 0 |

* UC4 circuit packs are required for collocated interface modules. UC4B circuit packs are required in Remote Complex interface modules.

† DS3PM2 circuit packs can only be installed in collocated DS3 Interface Modules. DS3PM circuit packs can not be used in Remote Complex interface modules.

- DS3 Interface-32 (INTFC-32) Module — supports 31MUX circuit packs and one MUXP circuit pack (protection ratio of 1 to 31). Figure 6-7 shows a DS3 Interface-32 module, while Table 6-8 lists its circuit packs.




**Notes:**

Number in parentheses is circuit pack position number on module.

To implement DS1 performance monitoring features, one to sixteen MUX circuit packs are replaced with PMGR circuit packs. For more information on DS1 performance monitoring configurations, refer to the section titled "DS1 PM Hardware" later in this chapter.

DS3PM2 circuit packs can only be installed in collocated DS3 Interface Modules. DS3PM circuit packs can not be used in Remote Complex interface modules.

Figure 6-7. **DS3 Interface-32 Module**

Table 6-8. **DS3 Interface-32 Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC4/UC4B* | Unit Controller 4 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| MUX1<br>MUX2 | Multiplexer 1<br>Multiplexer 2<br>(MUX2 circuit packs are required for enhanced DS3 performance monitoring and remote multiplexer communications features.) | 1 to 31 |
| PMGR1 | Performance Monitor Test Signal Generator Receiver 1<br>(Optional; used for DS1 Performance Monitoring feature and replaces MUX circuit packs.) | 0 to 16 |
| MUXP1 or<br>MUXP2 | Multiplexer (Protection) 1<br>Multiplexer (Protection) 2 | 1 |
| MUXPS1 | Multiplexer Protection Switch 1 | 1 |
| DS3PM2† | DS3 Performance Monitor 2<br>(Optional, used for DS3 Performance Monitoring reporting to GTP) | 0 or 1 |
| CLKDR2 | Clock Distributor 2 | 4 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped MUX and DS3PM circuit pack slots. Provides proper termination for the interoffice DS3 signals.) | 31 to 0 |

* UC4 circuit packs are required for collocated interface modules. UC4B circuit packs are required in Remote Complex interface modules.

† DS3PM2 circuit packs can only be installed in collocated DS3 Interface Modules. DS3PM circuit packs can not be used in Remote Complex interface modules.

The following sections describe the functions of a DS3 Interface Module and the relationship existing in a DS3 protection group (all MUX circuit packs contained in a DS3 Interface-16 or Interface-32 Module).

## DS3 Timing/Synchronization, Control, and Power

Figures 6-8 and 6-9 show detailed block diagrams of the timing/synchronization, control, and power distribution within a DS3 Interface-16 or DS3 Interface-32 Module for collocated and remote configurations, respectively. The functions provided by the circuit packs are described in the following sections.

**NOTE:**
In the following sections, the descriptions for the SWIO circuit packs also pertain to the OSWIO/OPEX[1] circuit packs.

### Power E (PWRE)

The PWRE circuit pack supplies +5V power to the other circuit packs within the associated DS3 Interface Module. Each PWRE circuit pack can supply power for the entire DS3 Interface Module, if required due to PWRE circuit pack failure. Error summary information is provided to the MTC circuit packs in collocated interface bays or the UIA or UIB circuit pack in the Remote Complex. Alarm and power indication LEDs are controlled by the UC circuit pack.

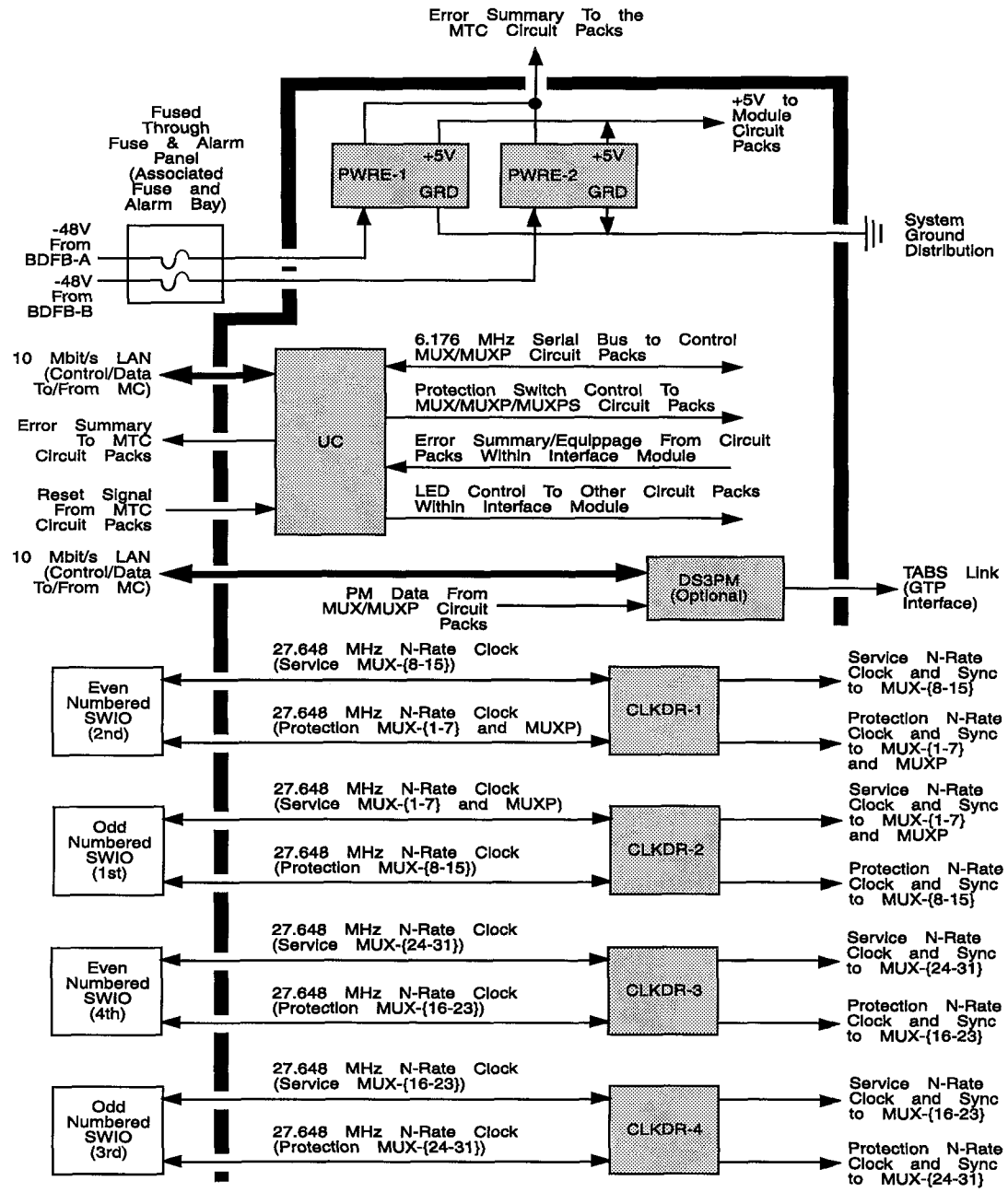
Each PWRE circuit pack is supplied -48V power from one of two Battery Distribution Feeder Boards (BDFB), which are fuse protected through the Fuse and Alarm Panel located in the Fuse and Alarm Bays for collocated interface modules or the Fuse and Alarm Panel located in the OPEX Bay for Remote Complex interface modules.

### Unit Controller (UC)

The UC circuit pack monitors the DS3 Interface Module hardware to detect and isolate faults and to monitor facilities. The UC circuit pack communicates (providing control) with other DS3 Interface Module circuit packs over 6.176-Mb/s serial control links. Other inputs to the UC allow for error summary of all circuit packs within the DS3 Interface Module. Outputs from the UC control the LEDs associated with other DS3 Interface Module circuit packs. The UC communicates (system control) with the Main Controller over the 10-Mb/s LAN. Software for the UC circuit pack is also downloaded from the Main Controller (the system disk or optical disk) over the 10-Mb/s LAN. The UC provides error summary information to, and receives reset signals from, the MTC (UIA or UIB) circuit packs. In addition, the UC provides protection switch control through the MUX, MUXP, and MUXPS circuit packs.

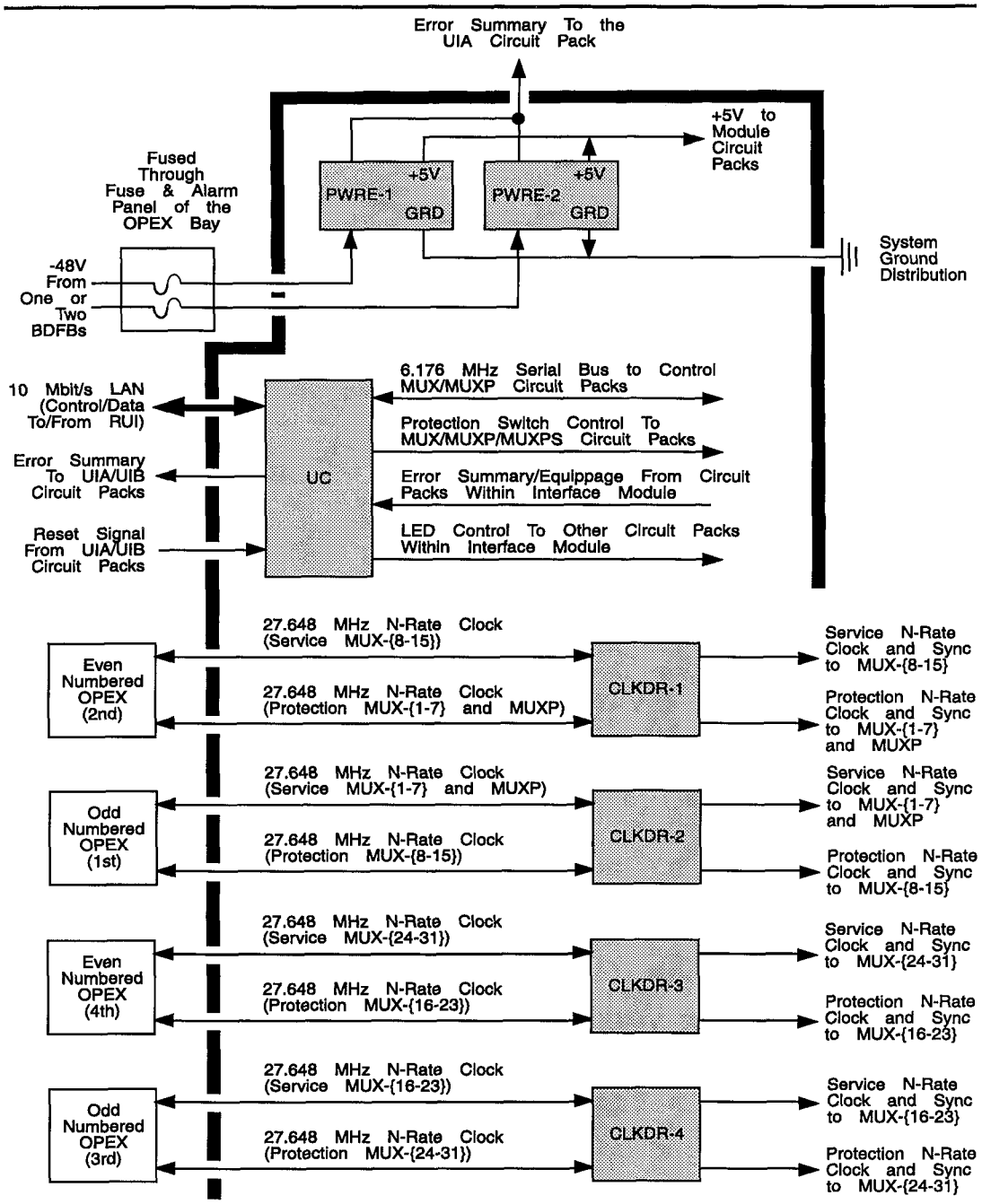
**NOTE:**
Use the UC4 circuit pack in collocated configurations; use the UC4B circuit pack for Remote Complex configurations.

1. For remote interface modules, the N-rate signals are extended to the OSWIO circuit packs through OPEX circuit packs and associated optical fiber cables. OPEX circuit packs do not perform any switching functions.




**Note:** CLKDR-3 and CLKDR-4 are contained in DS3 Interface-32 Modules only. DS3PM2 circuit packs can only be used in collocated DS3 Interface Modules. DS3PM2 circuit packs can not be used in Remote Complex interface modules.

Figure 6-8. **DS3 Interface Module Block Diagram - Control (Collocated Interface Modules)**




**Note:** CLKDR-3 and CLKDR-4 are contained in DS3 Interface-32 Modules only.

Figure 6-9. **DS3 Interface Module Block Diagram - Control (Remote Complex Interface Modules)**

## Clock Distributor (CLKDR)

The CLKDR circuit pack, and its associated SWIO (or OSWIO) circuit pack provides N-rate synchronization for the MUX circuit packs. The CLKDR circuit packs receive N-rate clock (27.648-MHz) and N-rate synchronizing (123.429-KHz) signals from SWIO (or OSWIO) circuit packs in the Switch Complex (over the N-rate cable) and distribute these signals to the MUX circuit packs.

Two CLKDR circuit packs are used to distribute service and protection timing signals for a DS3 Interface-16 Module and the lower shelf of a DS3 Interface-32 Module. An additional two CLKDR circuit packs are required in a DS3 Interface-32 Module to distribute service and protection timing signals to the upper shelf. Each CLKDR circuit pack distributes service signals to eight MUX/MUXP circuit packs and distributes protection signals to the other MUX/MUXP circuit packs within the same shelf. In addition, the CLKDR circuit packs reclocks the N-rate clock and synchronizing signals and sends them back to the SWIO (or OSWIO) circuit packs (over the N-rate cable).

A SWIO (or OSWIO/OPEX) circuit pack pair [two adjacent SWIO (or OSWIO/OPEX) circuit packs, the odd-numbered and the even-numbered] provide service for 16 DS3 signals (the OPEX circuit pack extends the N-rate signals to the OSWIO circuit pack). DS3 Interface-16 Modules provide 15 service signals and 1 protection DS3 signal and DS3 Interface-32 Modules provide 31 service signals and 1 protection DS3 signal. Therefore, one SWIO (or OSWIO/OPEX) circuit pack pair is needed for a DS3 Interface-16 Module, and two SWIO (or OSWIO/OPEX) circuit pack pairs are needed for a DS3 Interface-32 Module. Therefore, each CLKDR circuit pack provides eight service and eight protection timing signals to MUX/MUXP circuit packs. In this configuration, one CLKDR circuit pack is associated with each SWIO (or OSWIO/OPEX) circuit pack (providing for a typical 1-to-1 protection arrangement), unlike the DS1 Interface Modules where two CLKDR circuit packs are associated with each SWIO (or OSWIO/OPEX) circuit pack. For DS3 Interface Modules, special care must be taken when performing maintenance on SWIO (or OSWIO/OPEX) and CLKDR circuit pack pairs.

The bottom half of Figure 6-8 (or Figure 6-9) shows the timing signal distribution from the SWIO (or OSWIO/OPEX) circuit pack pair to the CLKDR circuit packs of a single DS3 Interface-16 or a single DS3 Interface-32 Module. Under normal conditions (no failures or protection switches) for both DS3 Interface-16 and DS3 Interface-32 Modules, CLKDR-2 is serviced by the first odd-numbered SWIO (or OSWIO/OPEX) circuit pack (1st) and CLKDR-1 is serviced by the first even-numbered SWIO (or OSWIO/OPEX) circuit pack (2nd). In addition, for DS3 Interface-32 Modules, CLKDR-4 is serviced by the second odd-numbered SWIO (or OSWIO/OPEX) circuit pack (3rd) and CLKDR-3 is serviced by the second even-numbered SWIO (or OSWIO/OPEX) circuit pack (4th). MUX circuit packs 8-15 normally receive timing from CLKDR-1, and MUX circuit packs 1-7 and the MUXP circuit pack normally receive timing from CLKDR-2. In addition, for DS3 Interface-32 Modules, MUX circuit packs 24-31 normally receive timing form CLKDR-3, and MUX circuit packs 16-23 receive timing from CLKDR-4.

If, for example, the first odd-numbered SWIO (or OSWIO) circuit pack is unable to provide service for any reason, all service for MUX circuit packs 1-7 and the MUXP circuit pack is switched to the first even-numbered SWIO (or OSWIO) circuit pack. In this case, the first even-numbered SWIO (or OSWIO) circuit pack is carrying the service (15 service MUX circuit packs and 1 protection MUXP circuit pack) for an entire bottom shelf. At the same time, CLKDR-2 no longer provides timing. Instead CLKDR-1 provides the timing for the entire bottom shelf of a DS3 Interface Module. The opposite is true if the first even-numbered SWIO (or OSWIO) circuit pack is unable to provide service. In a DS3 Interface-32 Module, CLKDR-3 and CLKDR-4 are unaffected by a failure of the first or second SWIO (or OSWIO) circuit pack.

Tables 6-9 and 6-11 lists the CLKDR circuit packs that provide timing (service) to the DS3 Interface-32 Module, given the status of the associated SWIO/OSWIO/ OPEX circuit packs in collocated or Remote Complex interface modules. Tables 6-10 and 6-12 lists the CLKDR circuit packs that provide timing (service) to the DS3 Interface-16 Module, given the status of the associated SWIO/OSWIO/ OPEX circuit packs in collocated or Remote Complex interface modules. If it becomes necessary to replace a CLKDR circuit pack in a DS3 Interface Module, the status of the associated SWIO/OSWIO/OPEX circuit pack must be determined. If the associated SWIO/OSWIO/OPEX circuit pack is carrying service (active), manual commands must be entered to switch service to its mate circuit pack.

Table 6-9. DS3 Interface-32 Module — SWIO/CLKDR Interworkings (Collocated Interface Modules)

| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted | CLKDR-3 Circuit Pack Fails or is Extracted | CLKDR-4 Circuit Pack Fails or is Extracted |
|---|---|---|---|---|
| 1st SWIO Active<br>2nd SWIO Active | Service hits on MUX-{8-15} | Service hits on MUX-{1-7} and MUXP | No effect | No effect |
| 1st SWIO Active<br>2nd SWIO Protected | No effect | Service outage on MUX-{1-15} and MUXP | No effect | No effect |
| 1st SWIO Protected<br>2nd SWIO Active | Service outage on MUX-{1-15} and MUXP | No effect | No effect | No effect |
| 3rd SWIO Active<br>4th SWIO Active | No effect | No effect | Service hits on MUX-{24-31} | Service hits on MUX-{16-23} |
| 3rd SWIO Active<br>4th SWIO Protected | No effect | No effect | No effect | Service outage on MUX-{16-31} |
| 3rd SWIO Protected<br>4th SWIO Active | No effect | No effect | Service outage on MUX-{16-31} | No effect |

Table 6-10. DS3 Interface-16 Module — SWIO/CLKDR Interworkings (Collocated Interface Modules)

| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted |
|---|---|---|
| 1st SWIO Active<br>2nd SWIO Active | Service hits on MUX-{8-15} | Service hits on MUX-{1-7} and MUXP |
| 1st SWIO Active<br>2nd SWIO Protected | No effect | Service outage on MUX-{1-15} and MUXP |
| 1st SWIO Protected<br>2nd SWIO Active | Service outage on MUX-{1-15} and MUXP | No effect |

Table 6-11. **DS3 Interface-32 Module — OSWIO/OPEX/CLKDR Interworkings (Remote Complex Interface Modules)**

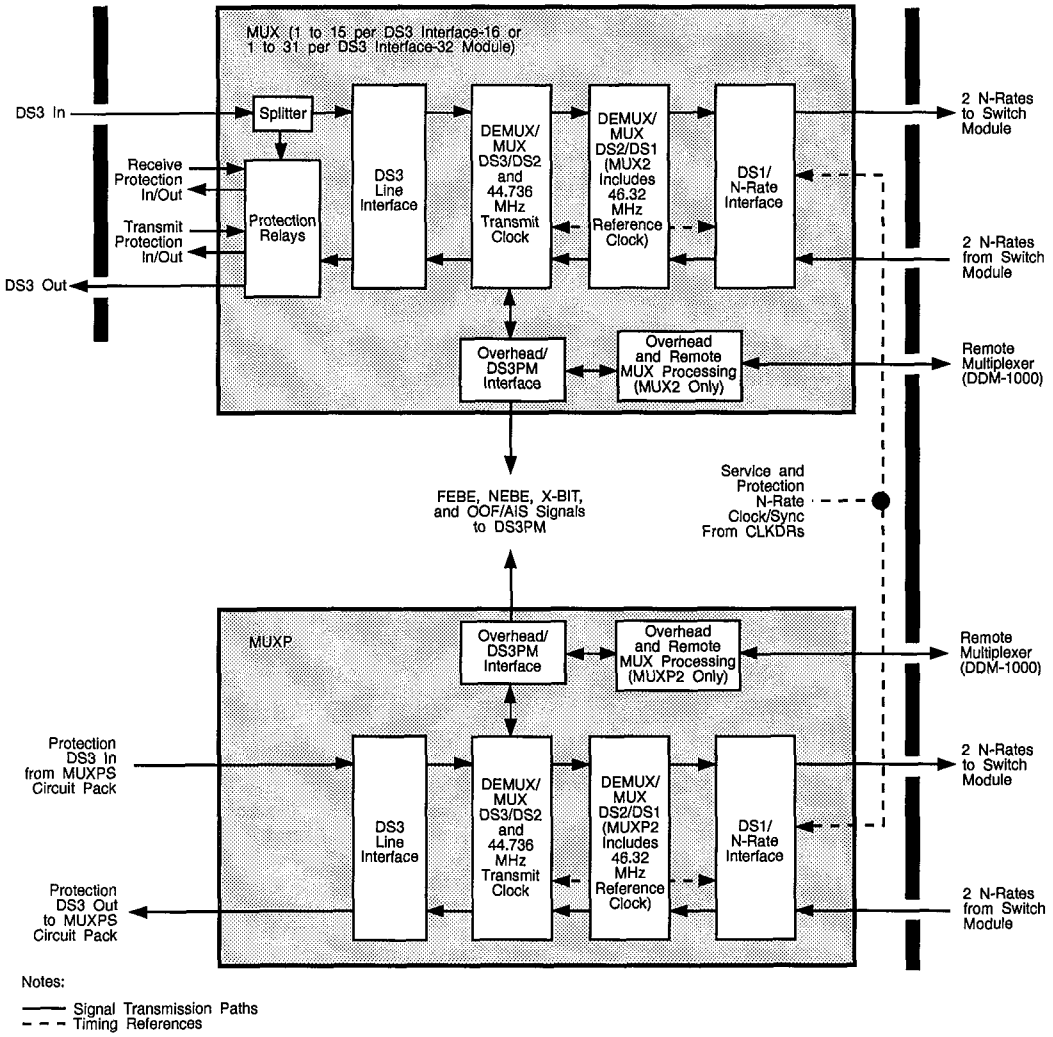
| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted | CLKDR-3 Circuit Pack Fails or is Extracted | CLKDR-4 Circuit Pack Fails or is Extracted |
|---|---|---|---|---|
| 1st OSWIO/OPEX Active<br>2nd SWIO Active | Service hits on MUX-{8-15} | Service hits on MUX-{1-7} and MUXP | No effect | No effect |
| 1st OSWIO/OPEX Active<br>2nd OSWIO/OPEX Protected | No effect | Service outage on MUX-{1-15} and MUXP | No effect | No effect |
| 1st OSWIO/OPEX Protected<br>2nd OSWIO/OPEX Active | Service outage on MUX-{1-15} and MUXP | No effect | No effect | No effect |
| 3rd OSWIO/OPEX Active<br>4th OSWIO/OPEX Active | No effect | No effect | Service hits on MUX-{24-31} | Service hits on MUX-{16-23} |
| 3rd OSWIO/OPEX Active<br>4th OSWIO/OPEX Protected | No effect | No effect | No effect | Service outage on MUX-{16-31} |
| 3rd OSWIO/OPEX Protected<br>4th OSWIO/OPEX Active | No effect | No effect | Service outage on MUX-{16-31} | No effect |

Table 6-12. **DS3 Interface-16 Module — OSWIO/OPEX/CLKDR Interworkings (Remote Complex Interface Modules)**

| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted |
|---|---|---|
| 1st OSWIO/OPEX Active<br>2nd OSWIO/OPEX Active | Service hits on MUX-{8-15} | Service hits on MUX-{1-7} and MUXP |
| 1st OSWIO/OPEX Active<br>2nd OSWIO/OPEX Protected | No effect | Service outage on MUX-{1-15} and MUXP |
| 1st OSWIO/OPEX Protected<br>2nd OSWIO/OPEX Active | Service outage on MUX-{1-15} and MUXP | No effect |

## DS3 Transmission

Figure 6-10 shows a block diagram of the transmission path within a MUX1 or MUX2 circuit pack. Figure 6-11 in the section titled "Multiplexer 3 (MUX3)" (page 6-34) shows a block diagram of the transmission path within a MUX3 circuit pack. The functions provided by the circuit packs are described in the following sections.




**Note:** DS3PM2 circuit packs can only be used in collocated DS3 Interface Modules. DS3PM2 circuit packs can not be used in Remote Complex interface modules.

Figure 6-10. **DS3 Interface Module (MUX1 and MUX2) Block Diagram (Transmission Paths)**

## Multiplexer (MUX1 or MUX2)

The MUX1 or MUX2 circuit pack terminates two-way DS3 (44.736-Mb/s) facilities. The following blocks are used to process a DS3 signal in the **receive** direction:

- Splitter — receives a DS3 bipolar signal and splits the signal by diverting half the power to the DS3 Line Interface circuitry and half the power to the Protection Relay circuitry.
- Protection Relays — connects the MUX to the receive protection bus daisy-chain. The receive daisy-chain connects each MUX circuit pack to the MUXP circuit pack through the MUXPS circuit pack. Refer to the next section titled "Protection Bus" for more information.
- DS3 Line Interface — extracts clock and converts the 50% duty cycle bipolar DS3 signal, received from the Splitter circuitry, into a 100% duty cycle dual-rail signal. The extracted clock and converted signal is sent to the DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock circuitry.
- DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock — demultiplexes the DS3 signal, received from the DS3 Line Interface circuitry into seven DS2 signals and sends the DS2 signals to the DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock circuitry. The functions performed are:
  1. Receive DS3 signal from the DS3 Line Interface circuitry
  2. Code B3ZS and M13 or C-bit parity format; dual-rail to single-rail signal conversion
  3. Detect LOS.
- Overhead and Remote MUX Processing (MUX2 circuit packs only) — processes the information received from the DEMUX/MUX DS3/DS2 circuitry and sends the processed information to a remote multiplexer (for example, the DDM-1000).
- DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock — demultiplexes the seven DS2 signals into 28 DS1 signals. In addition, clock circuitry is provided that is used to source a 1.544-MHz clock used by the DS1/N-Rate Interface circuitry. The functions performed are:
  1. Receive seven DS2 signals from the DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock circuitry and demultiplex into 28 DS1 signals
  2. Generate 1.544-MHz DS1 reference clock and send to the DS1/N-Rate Interface circuitry.

- DS1/VT/N-Rate Interface — multiplexes the 28 DS1 signals into two service signals and two protection N-rate signals and sends the N-rate signals to the Switch Module. The functions performed are:

    1. Receive 28 DS1 signals from the DEMUX/MUX DS2/DS1 and 44.32-MHz Reference Clock circuitry and multiplex into 28 N-rate channels on the two N-rate signals
    2. Generate and insert stuff-channel parity over the DS1
    3. Generate and embed N-rate parity over the 16-bit N-rate data block
    4. Generate two N-rate balanced signals (upper and lower) and drive both service and protection interfaces
    5. Monitor service and protection N-rate clock
    6. Monitor N-rate sync for the 123-kHz sync information
    7. Monitor and generate DS1 AIS.

  The following blocks are used to process the two N-rate signals received from the Switch Module in the transmit direction:

- DS1/N-Rate Interface — demultiplexes the received cross-connected N-rate signals from the Switch Module into 28 DS1 signals. The functions performed are:

    1. Receive service and protection balanced CMOS clock and sync from backplane
    2. Monitor service and protection N-rate clock
    3. Monitor service and protection N-rate sync for 123-kHz sync information
    4. Perform N-rate clock and sync protection switching under software control
    5. Receive service and protection N-rate data sets (upper and lower) and perform protection switching under software control
    6. Monitor service and protection N-rate data inputs for N-rate parity errors
    7. Demultiplex N-rate channels to DS1 signals, monitor each DS1 stuff channel parity for errors to maintain cross-connect, and output 28 DS1 signals to the DEMUX/MUX DS1/DS1 and 46.32-MHz Reference Clock circuitry
    8. Insert DS1 AIS.

- DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock — multiplexes the 28 DS1 signals into seven DS2 signals. In addition, clock circuitry is provided that is used to source a 1.544-MHz clock used by the DS1/N-Rate Interface circuitry.The 28 DS1signals are received from the DS1/N-Rate Interface circuitry and multiplexed into seven DS2 signals
- Overhead and Remote MUX Processing (MUX2 and MUX3 circuit packs only) — processes the information received from the remote multiplexer (if provisioned to do so) and sends the information to the Overhead/DS3PM Interface circuitry. (DS3PM circuit packs can only be used in collocated DS3 Interface Modules.)
- DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock — multiplexes the seven DS2 signals, received from the DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock circuitry into one DS3 signal and sends the DS3 signal to the DS3 Line Interface circuitry. In addition, clock circuitry is used to generate the 44.736-MHz DS3 clock reference used to generate the DS3 signal for transmission. This interface can also:
    1. Receive seven DS2 signals from the DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock circuitry
    2. Receive overhead information from the Overhead/DS3PM Interface circuitry
    3. Generate the 44.736-MHz DS3 transmit clock
    4. Convert single-rail signal to dual-rail signal
    5. Encode DS3 signal to M13 or C-bit parity format and B3ZS format
    6. Clock duty cycle correction.
- Overhead/DS3PM Interface — demultiplexes the DS3 overhead and distributes the information for processing.The function provided is demultiplex the FEBE, NEBE, AIS, and X-BIT information from the overhead link and transmit it to the DS3PM circuit pack and CILINKs in the associated interface module. (DS3PM circuit packs can only be used in collocated DS3 Interface Modules.)
- DS3 Line Interface — converts the dual-rail signal received from the DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock circuitry into a bipolar DS3 signal. This signal is output directly or through a jumper selectable line buildout (LBO) circuit to the Protection Relays circuitry.
- Protection Relays — connects the MUX to the transmit protection bus daisy-chain. The transmit daisy-chain connects each MUX circuit pack to the MUXP circuit pack through the MUXPS circuit pack. In addition, the protection relay determines if the DS3 signal is output from the MUX or MUXP circuit pack. Refer to the next section titled "DS3 Protection Bus" (page 6-37) for more information.

## Multiplexer 3 (MUX3)

The MUX3 circuit pack processes the DS3 signal in one of the following two modes:

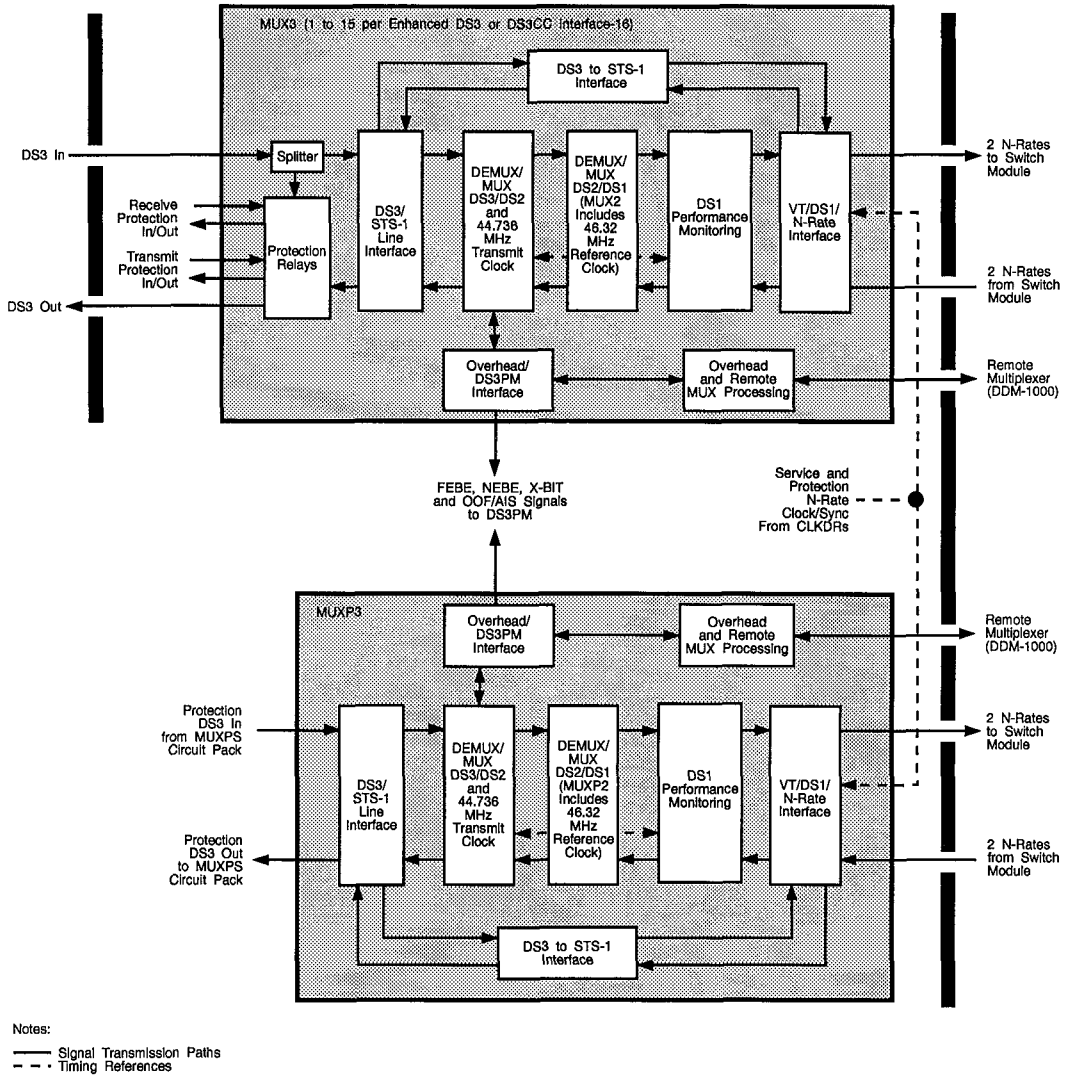
- 28 DS1 tributaries (provisioned in the DS1 mode)
- A DS3 clear-channel signal (provisioned in the CC mode)

In DS1 mode the MUX3 circuit pack performs the same functions as described above with the addition in the receive and transmit direction of the DS1 performance monitoring circuitry before/after the VT/DS1/N-rate interface circuitry (refer to Figure 6-11). The DS1 performance monitoring circuitry provides for collection of full-time performance monitoring data of individual DS1 tributaries of a DS3 signal.

In CC mode the MUX3 circuit pack performs the functions described in the following paragraphs (refer to Figure 6-11).

The functions performed in the receive direction are:

- DS3/STS-1 Line Interface — extracts clock and converts the 50% duty cycle bipolar DS3 signal, received from the Splitter circuitry, into a 100% duty cycle dual-rail signal. The extracted clock and converted signal is sent to the DS3 to STS-1 Interface.
- DS3 to STS-1 Interface — maps the dual-rail signal received from the DS3/STS-1 Line Interface into an STS-1 SPE. It adds stuff and overhead bits to the STS-1 signal to obtain the STS-1 payload. It also generates the associated STS-1 clock and frame synch and passes the resulting STS-1 signal to the DS3/VT/N-rate Interface. The functions performed are:
    1. Input dual rail DS3 and 51.840 MHz clock signals
    2. Provide DS3 receive output loopback to transmit input
    3. Monitor and reports B3ZS violations on the incoming DS3
    4. Provide AIS substitution capabilities
    5. Add overhead information to DS3 data to form the STS-1 signal
    6. Generate STS-1 data and frame sync outputs.




**Note:** DS3PM2 circuit packs can only be used in collocated DS3 Interface Modules. DS3PM2 circuit packs can not be used in in Remote Complex interface modules.

Figure 6-11. **DS3 Interface Module (MUX3) Block Diagram (Transmission Paths)**

- DS1/VT N-Rate Interface — converts the STS-1 signals into two service signals and two protection N-rate signals and sends the N-rate signals to the Switch Module. This interface also:
    1. Receives the STS-1 signal from the DS3 to STS-1 Interface and 51.840-MHz Reference Clock circuitry
    2. Monitors interdevice C1 parity over the incoming STS-1 (cc-SPE) data
    3. Detects and report loss of 51.840 MHz clock signal
    4. Generates and embed the CRC-6 over the STS-1 stream
    5. Bit interleaves the serial STS-1 stream and map to 30 N-rate channels.
- Overhead and Remote MUX Processing — processes the information received from the DEMUX/MUX DS3/DS2 circuitry and sends the processed information to a remote multiplexer (for example, the DDM-1000).

The functions performed in the transmit direction are:

- DS1/VT N-Rate Interface — interfaces and converts the N-rate signal to the STS-1 and DS1 signal formats. It interfaces the N-rate signals and performs N-rate data and timing protection switching. The STS-1 clock and sync signals are passed to the DS3 to STS-1 Interface. This interface also:
    1. Receives input service and protection clock and sync signals from the backplane
    2. Monitors service and protection clock and sync signals
    3. Performs N-rate clock and sync protection switching
    4. Monitors service and protection data input for N-rate parity errors
    5. Bit interleaves serial N-rate data to generate STS-1 signal
    6. Generates CRC-6 over the STS-1.
- DS3 to STS-1 Interface — receives the STS-1 clock and sync signals and map to the DS3 rate. The overhead information is removed from the STS-1 signal and a DS3 integrity check provides monitoring and parity correction for the DS3 output. B3ZS coding is added to the signal which is passed to the DS3/STS-1 Line Interface. This interface also:
    1. Receives STS-1 clock and sync signals
    2. Interprets H1 and H2 bytes for start of SPE
    3. Terminates path overhead information
    4. STS-1 loopback provides transmit clock and frame sync
    5. Provides AIS detection and insertion
    6. Provides parity correction

7. Generates 2-rail B3ZS encoded signal.

- DS3/STS-1 Line Interface — drives the DS3 output from the DS3 to STS-1 Interface. It also performs integrated pulse shaping and B3ZS encoding/ decoding for the DS3 signal

### Multiplexer Protection

Multiplexer Protection provides protection for MUX circuit packs within an interface protection group (that is, all MUX circuit packs within the same interface module). MUXP circuit packs perform the same functions as MUX circuit packs (except for signal splitting and protection relay functions) when active. MUXP circuit packs are hard-wired with the LBO set to `OUT` (MUXPS has switchable LBO). In a DS3 Interface-32 Module, protection is provided for MUX circuit packs on a 1-to-31 basis. In a DS3 Interface-16 Module, protection is provided for MUX circuit packs on a 1-to-15 basis.

### Performance Monitor Generator/Receiver (PMGR)

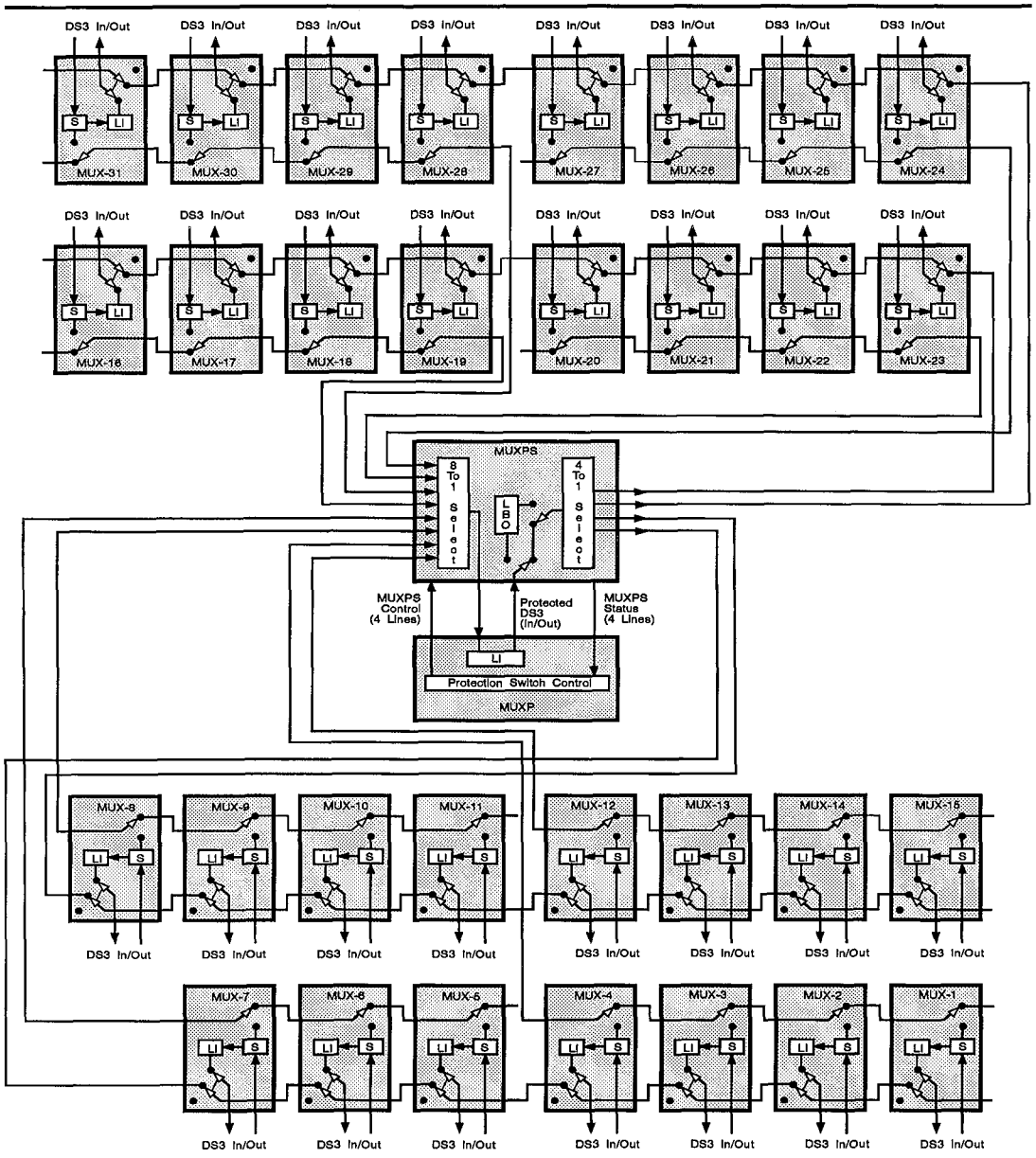
The Performance Monitor Generator/Receiver (PMGR) circuit pack is an optional circuit pack that can only be used in DS3 Interface-16, DS3 Interface-32, and DS1 Interface Modules. The PMGR circuit pack enables bridged access DS1 performance monitoring. PMGR circuit packs replace MUX circuit packs. When inserted, PMGR circuit packs maintain the DS3 protection bus integrity. For more information on performance monitoring, refer to the section titled "Performance Monitoring" (page 2-57) and "DS1 Performance Monitoring Hardware" (page 6-59).

## DS3 Protection Bus

Figure 6-12 is a block diagram of the protection bus within a DS3 protection group (that is, all MUX circuit packs within a DS3 Interface Module). The functions provided by the circuit packs are described in the following sections.

### Multiplexer (MUX)

The MUX circuit packs contain protection relays, which when activated allow for a DS3 signal to be processed by the MUXP circuit pack. The 15 MUX circuit packs within a DS3 Interface-16 module or the 31 MUX circuit packs within a DS3 Interface-32 Module are daisy-chained together and routed to the MUXPS circuit pack.




**Notes:**

S = Signal Splitter
LI = DS3 Line Interface
LBO = Line Buildout

For DS3 Interface-16 Modules, only four of the receive select lines and two of the transmit select lines of the MUXPS circuit pack are needed. When BXA or PMGR1 circuit packs are inserted for MUX circuit packs, the daisy-chain connectors (receive and transmit paths) are maintained.

Figure 6-12. **DS3 Interface Module Block Diagram (Protection Bus)**

### Bus Extender A (BXA)

The BXA circuit pack is installed in empty MUX circuit pack slots to provide protection bus integrity (that is, maintain the daisy-chain) and to keep out dust and foreign matter.

### Multiplexer Protection Switch (MUXPS)

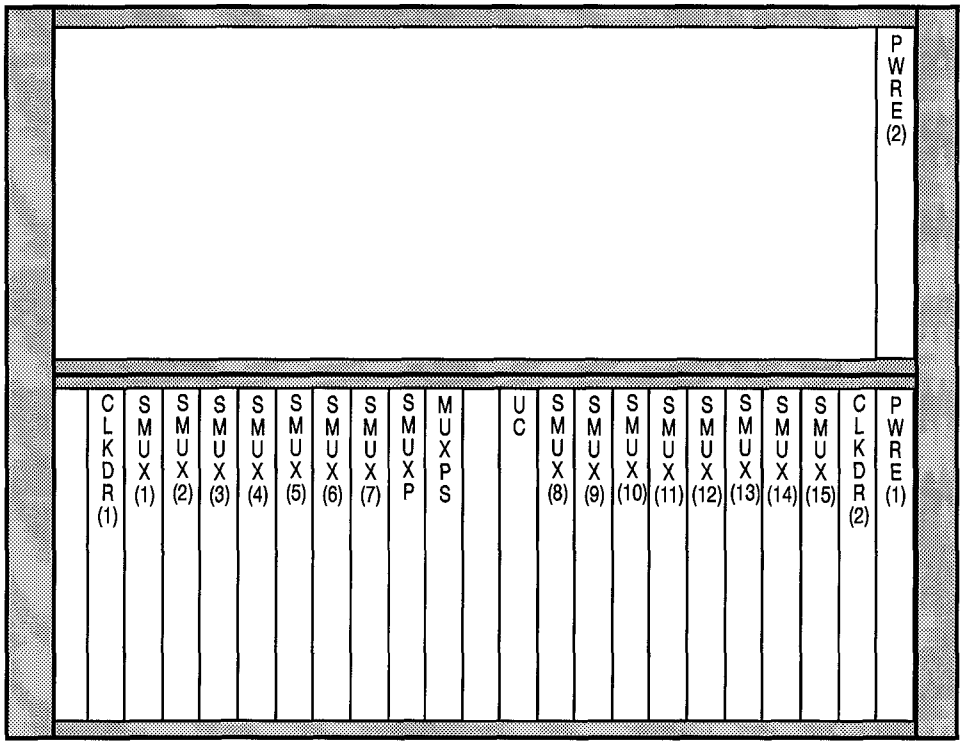
The MUXPS circuit pack terminates the receive and transmit protection daisy-chains of the MUX circuit packs and routes the DS3 signals to the MUXP circuit pack. In the receive direction, four groups of MUX circuit packs (DS3 Interface-16 Modules) or eight groups of MUX circuit packs (DS3 Interface-32 Modules) are daisy-chained together and routed to the MUXPS circuit pack. In the transmit direction, two groups of MUX circuit packs (DS3 Interface-16 Modules) or four groups of MUX circuit packs (DS3 Interface-32 Modules) are daisy-chained together and routed to the MUXPS circuit pack. Control from the UC/MUXP circuit packs selects the appropriate groups when necessary. If a MUX circuit pack fails, the UC directs the MUXP and MUXPS circuit packs to send the affected DS3 signal to the MUXP circuit pack and activates the associated protection relays within the failed MUX circuit pack, allowing the affected DS3 signal to be protected. The MUXPS LBO setting is determined by the failed MUX circuit pack.

### Multiplexer Protection (MUXP)

The MUXP circuit pack provides protection for MUX circuit packs within an interface protection group (that is, all MUX circuit packs within the same interface module). The MUXP circuit pack selects the appropriate daisy-chain group when directed by the UC circuit pack to provide protection for a DS3 signal. Status lines from the MUXPS circuit pack provide state information of the MUXPS circuit pack to the MUXP. In a DS3 Interface-16 Module, the MUXP circuit pack provides protection for MUX circuit packs on a 1-to-15 basis, and in a DS3 Interface-32 Module, the MUXP circuit pack provides protection for MUX circuit packs on a 1-to-31 basis.

# STS1 Interface Module

STS1 Interface-16 Modules provide the interface for incoming and outgoing EC-1 facilities or network elements. These modules accept STS-1 signals (in a format compliant with the SONET requirements) and switch these signals to and from the Switch Module. Figure 6-13 shows the circuit pack locations in the STS1 Interface-16 Module. Table 6-13 lists the STS1 Interface-16 Module circuit packs, their functions, and quantity.




**Note:** Numbers in parentheses is circuit pack position number on module.

Figure 6-13. **STS1 Interface-16 Module**

Table 6-13. **STS1 Interface Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC4/UC4B* | Unit Controller 4 (must be inserted into UC circuit pack slots or multiple alarms can occur) | 1 |
| SMUX1 | SONET Multiplexer 1 | 1 to 15 |
| SMUXP1 | SONET Multiplexer (Protection) 1 | 1 |
| MUXPS1 | Multiplexer Protection Switch 1 | 1 |
| CLKDR2 | Clock Distributor 2 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped SMUX circuit pack slots.) | 14 to 0 |

* UC4 circuit packs are required for collocated interface modules. UC4B circuit packs are required in Remote Complex interface modules.

The following sections describe the functions of an STS1 Interface-16 Module and the relationship existing in an STS1 protection group (all SMUX circuit packs contained in an STS1 Interface-16 Module).

## STS1 Timing/Synchronization, Control, and Power

Figures 6-14 and 6-15 show detailed block diagrams of the timing/synchronization, control, and power distribution within an STS1 Interface-16 Module for collocated and remote interface bays, respectively. The functions provided by the circuit packs are summarized in the following sections.

**NOTE:**
In the following sections, the descriptions for the SWIO circuit packs also pertain to the OSWIO/OPEX[1] circuit packs.

1. For remote interface modules, the N-rate signals are extended to the OSWIO circuit packs through OPEX circuit packs and associated optical fiber cables. OPEX circuit packs do not perform any switching functions.

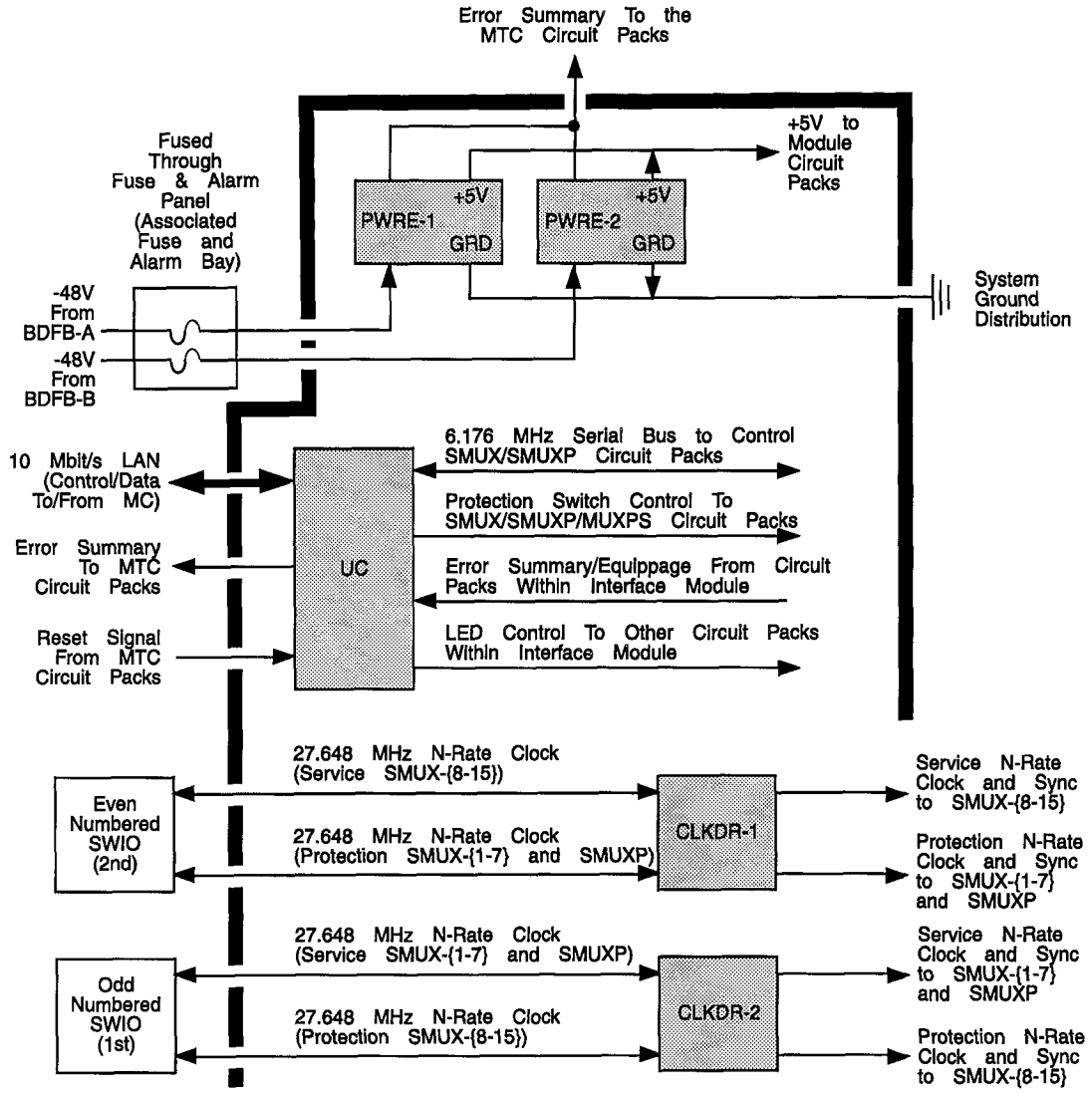



Figure 6-14. **STS1 Interface-16 Module Block Diagram - Control (Collocated Interface Modules)**

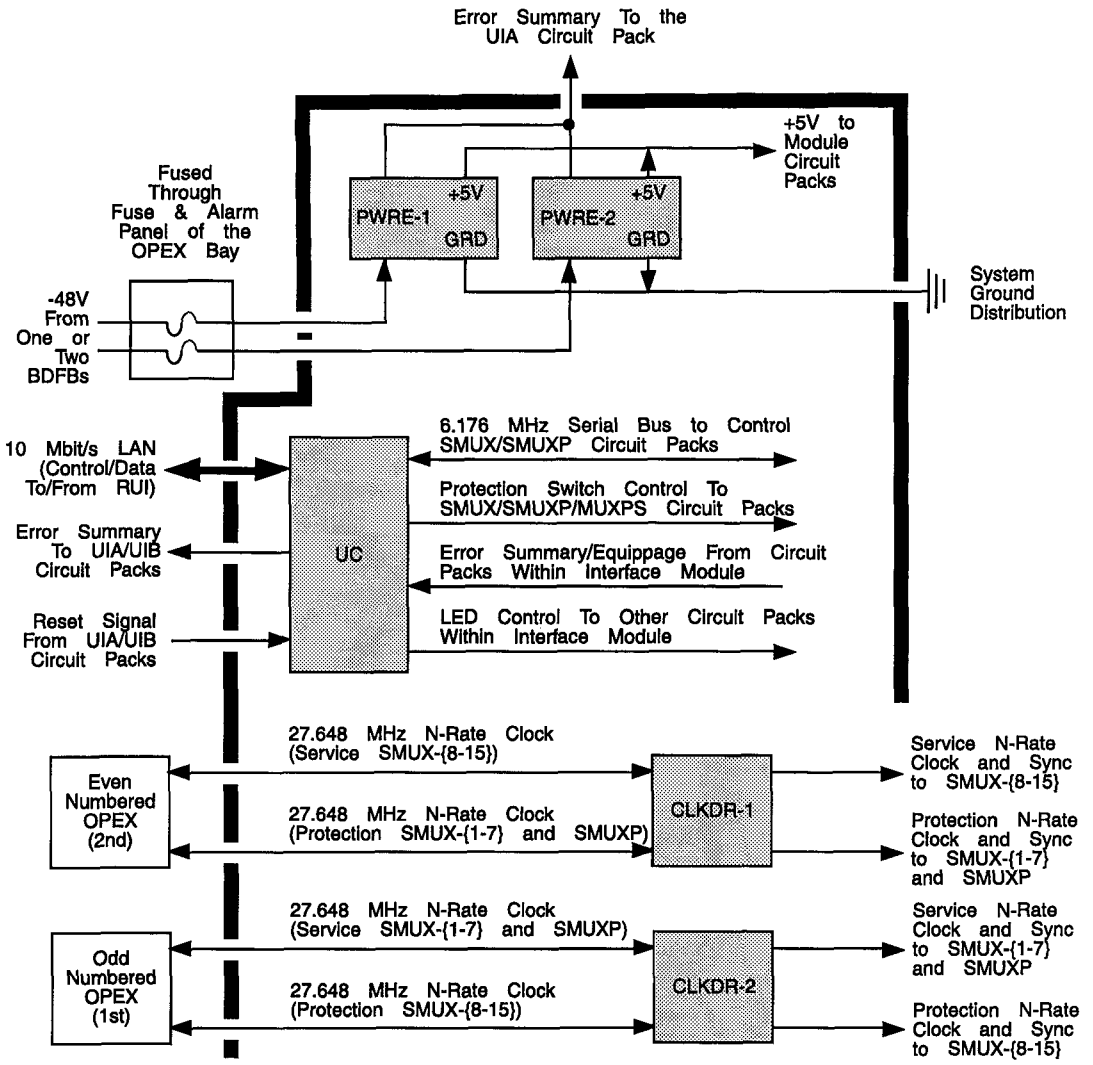



Figure 6-15. **STS1 Interface-16 Module Block Diagram - Control (Remote Complex Interface Modules)**

### Power E (PWRE)

The PWRE circuit pack supplies +5V power to the other circuit packs within the associated STS1 Interface-16 Module. Each PWRE circuit pack can supply power for the entire STS1 Interface-16 Module, if required due to PWRE circuit pack failure. Error summary information is provided to the MTC circuit packs in collocated interface bays, or to the UIA or UIB circuit packs in the Remote Complexes. Alarm and power indication LEDs are controlled by the UC circuit pack. Alarm and power indication LEDs are controlled by the UC circuit pack.

Each PWRE circuit pack is supplied -48V power from one or both Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse and Alarm Panel located in the Fuse and Alarm Bays for collocated interface modules or the Fuse and Alarm Panel located in the OPEX Bay for Remote Complex interface modules.

### Unit Controller (UC)

The UC monitors the STS1 Interface-16 Module hardware to detect and isolate faults and to monitor facilities. The UC circuit pack communicates (providing control) with other STS1 Interface-16 Module circuit packs over 6.176-Mb/s serial control links. Other inputs to the UC allow for error summary of all circuit packs within the STS1 Interface-16 Module. Outputs from the UC control the LEDs associated with other STS1 Interface-16 Module circuit packs. The UC communicates (system control) with the Main Controller over the 10-Mb/s LAN. Software for the UC circuit pack is also downloaded from the Main Controller (the system disk or optical disk) over the 10-Mb/s LAN. The UC provides error summary information to, and receives reset signals from, the MTC (or UIA/UIB) circuit packs. In addition, the UC provides protection switch control through the SMUX, SMUXP, and MUXPS circuit packs.

**NOTE:**
Use the UC4 circuit pack for collocated configurations; use the UC4B circuit pack for Remote Complexes.

### Clock Distributor (CLKDR)

The CLKDR circuit pack, and its associated SWIO (or OSWIO) circuit pack provides N-rate synchronization for the SMUX circuit packs. The CLKDR circuit packs receive N-rate clock (27.648-MHz) and N-rate synchronizing (123.429 KHz) signals from SWIO (or OSWIO) circuit packs in the Switch Complex (over the N-rate cable) and distribute these signals to the SMUX circuit packs.

Two CLKDR circuit packs are used to distribute service and protection timing signals for an STS1 Interface-16 Module. Each CLKDR circuit pack distributes service signals to eight SMUX/SMUXP circuit packs and distributes protection signals to the other SMUX/SMUXP circuit packs within the same shelf. In addition,

the CLKDR circuit packs reclocks the N-rate clock and synchronizing signals and sends them back to the SWIO (or OSWIO) circuit packs (over the N-rate cable).

A SWIO (or OSWIO/OPEX) circuit pack pair [two adjacent SWIO (or OSWIO/OPEX) circuit packs, the odd-numbered and the even-numbered] provide service for 16 STS-1 signals (the OPEX circuit pack extends the N-rate signals to the OSWIO circuit pack). STS1 Interface-16 Modules provide 15 service signals and 1 protection STS-1 signal. Therefore, one SWIO (or OSWIO/OPEX) circuit pack pair is needed for an STS1 Interface-16 Module. Therefore, each CLKDR circuit pack provides eight service and eight protection timing signals to SMUX/SMUXP circuit packs. In this configuration, one CLKDR circuit pack is associated with each SWIO (or OSWIO/OPEX) circuit pack (providing for a typical 1-to-1 protection arrangement), unlike the DS1 Interface Modules where two CLKDR circuit packs are associated with each SWIO (or OSWIO/OPEX) circuit pack. For STS1 Interface Modules, special care must be taken when performing maintenance on SWIO (or OSWIO/OPEX) and CLKDR circuit pack pairs.

The bottom half of Figure 6-14 (or Figure 6-15) shows the timing signal distribution from the SWIO (or OSWIO/OPEX) circuit pack pair to the CLKDR circuit packs of a single STS1 Interface-16 Module. Under normal conditions (no failures or protection switches) for STS1 Interface-16 Modules, CLKDR-2 is serviced by the odd-numbered SWIO (or OSWIO/OPEX) circuit pack (1st) and CLKDR-1 is serviced by the even-numbered SWIO (or OSWIO/OPEX) circuit pack (2nd). SMUX circuit packs 8-15 normally receive timing from CLKDR-1, and SMUX circuit packs 1-7 and the SMUXP circuit pack normally receive timing from CLKDR-2.

If, for example, the odd-numbered SWIO (or OSWIO circuit pack is unable to provide service for any reason, all service for SMUX circuit packs 1-7 and the SMUXP circuit pack is switched to the even-numbered SWIO (or OSWIO) circuit pack. In this case, the even-numbered SWIO (or OSWIO) circuit pack is carrying the service (15 service SMUX circuit packs and 1 protection SMUXP circuit pack) for an entire STS1 Interface-16 Module. At the same time, CLKDR-2 no longer provides timing. Instead CLKDR-1 provides the timing for the entireSTS1 Interface-16 Module. The opposite is true if the even-numbered SWIO (or OSWIO) circuit pack is unable to provide service.

Tables 6-14 and 6-15 list the CLKDR circuit packs that provide timing (service) to the STS1 Interface-16 Module, given the status of the associated SWIO/OSWIO/OPEX circuit packs in collocated or Remote Complex interface modules. If it becomes necessary to replace a CLKDR circuit pack in an STS1 Interface-16 Module, the status of the associated SWIO/OSWIO/OPEX circuit pack must be determined. If the associated SWIO/OSWIO/OPEX circuit pack is carrying service (active), manual commands must be entered to switch service to its mate circuit pack.

Table 6-14. **STS1 Interface-16 Module — SWIO/CKLDR Interworkings (Collocated Interface Module)**

| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted |
|---|---|---|
| Odd SWIO Active<br>Even SWIO Active | Service hits on SMUX-{8-15} | Service hits on SMUX-{1-7} and SMUXP |
| Odd SWIO Active<br>Even SWIO Protected | No effect | Service outage on SMUX-{1-15} and SMUXP |
| Odd SWIO Protected<br>Even SWIO Active | Service outage on SMUX-{1-15} and SMUXP | No effect |

Table 6-15. **STS1 Interface-16 Module — OSWIO/OPEX/CKLDR Interworkings (Remote Complex Interface Module)**

| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted |
|---|---|---|
| Odd OSWIO/OPEX Active<br>Even OSWIO/OPEX Active | Service hits on SMUX-{8-15} | Service hits on SMUX-{1-7} and SMUXP |
| Odd OSWIO/OPEX Active<br>Even OSWIO/OPEX Protected | No effect | Service outage on SMUX-{1-15} and SMUXP |
| Odd OSWIO/OPEX Protected<br>Even OSWIO/OPEX Active | Service outage on SMUX-{1-15} and SMUXP | No effect |

## STS1 Transmission

Figure 6-16 is a block diagram of the transmission paths within an STS1 Interface-16 Module. The functions provided by the circuit packs are described in the following sections.

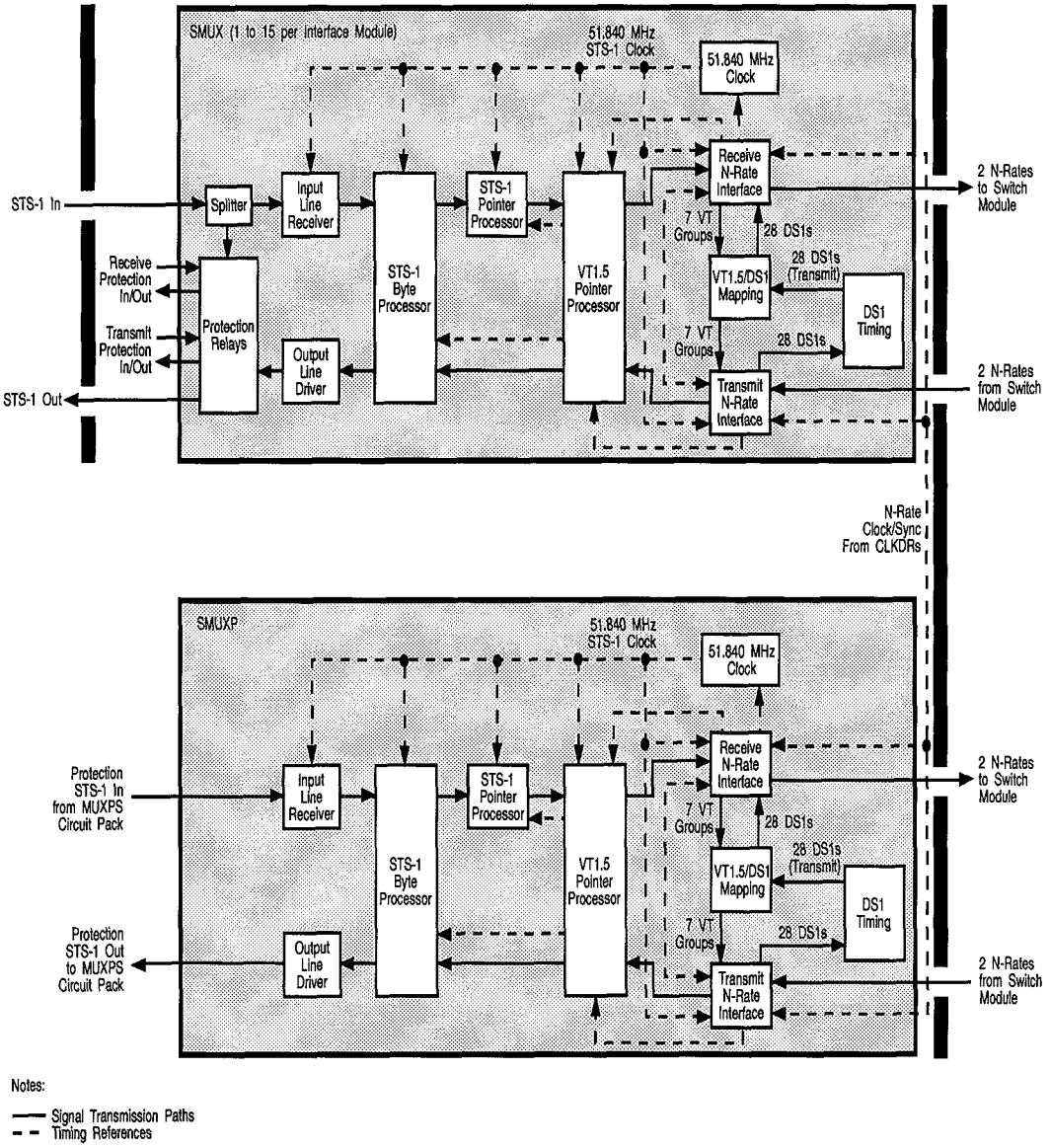



Figure 6-16. **STS1 Interface-16 Module Block Diagram (Transmission Paths)**

## SONET Multiplexer (SMUX)

The SMUX circuit pack terminates two-way EC-1 (51.840-Mb/s) facilities. The internal structure of the SMUX circuit packs is defined by the following functional blocks:

- 51.840-MHz Clock — generates the 51.840-MHz clock used on the SMUX circuit pack. The 51.840-MHz clock is derived from the 27.648-MHz N-Rate clock received from the CLKDR circuit packs. To generate the 51.840-MHz clock, the Transmit N-Rate Interface circuitry divides the 27.648-MHz N-Rate clock to generate a 1.728-MHz reference clock, and receives a buffered version of the 51.840-MHz oscillator output and divides that down to 1.728-MHz. The two generated 1.728-MHz reference signals received by the 51.840-MHz Clock circuitry, are inputted to a phase detector and locked together by a phase lock loop. This locks the 51.840-MHz clock to the selected 27.648-MHz N-Rate clock (that is, the 51.840-MHz clock is totally dependent on the N-Rate clock frequency). Finally, the 51.840-MHz clock is buffered and distributed to the Receive and Transmit N-Rate Interface, the VT1.5 Pointer Processor, the STS-1 Pointer Processor, and the STS-1 Byte Processor circuitry. In addition, a single ended 51.840-MHz clock is sent to the Input Line Receiver circuitry as a reference.

  The following blocks are used to process an STS-1 signal received from an EC-1 facility in the receive direction:

- Splitter — receives an STS-1 bipolar signal and splits the signal by diverting half the power to the Input Line Receiver circuitry and half the power to the Protection Relay circuitry.
- Protection Relays — connects the SMUX to the receive protection bus daisy-chain. The receive daisy-chain connects each SMUX circuit pack to the SMUXP circuit pack through the MUXPS circuit pack. Refer to the section titled "STS1 Protection Bus" (page 6-57) for more information.
- Input Line Receiver — extracts clock and converts the 50% duty cycle bipolar signal into a 100% duty cycle dual-rail signal from the bipolar STS-1 signal received from the Splitter circuitry. The extracted clock and converted signal is sent to the STS-1 Byte Processor circuitry.
- STS-1 Byte Processor — terminates the transport overhead portion of the STS-1 signal. The functions performed are:

  1. B3ZS decoding, dual-rail to single rail signal conversion
  2. LOS detection
  3. STS-1 descrambling
  4. STS-1 A1A2 framing and OOF/LOF detection
  5. B2 parity monitoring
  6. Generate receive path AIS
  7. FERF monitoring

8. Line AIS detection.

In addition, when operating an STS-1 line loopback, the transmit output is looped back to the receive input.

- STS-1 Pointer Processor — removes the STS-1 SPE and rebuilds a basic STS-1 frame structure to be output to the VT1.5 Pointer Processor circuitry. The functions performed are:

  1. Receive balanced CMOS line data, sync, and clock from the STS-1 Byte Processor circuitry
  2. Monitor interdevice C1 parity over the incoming Line STS-1 data
  3. Detect and report loss of line clock and sync
  4. Detect path AIS
  5. Perform STS-1 SPE synchronization through pointer processing
  6. Monitor pointer justifications
  7. Report New Data Flag (NDF)
  8. Build new STS-1 frame including insertion of A1A2 bytes based on the system frame sync received from the VT1.5 Pointer Processor circuitry
  9. Generate new H1H2 pointer values based on the system frame sync received from the VT1.5 Pointer Processor circuitry
  10. Insert STS-1 path AIS
  11. Detect and report loss of system clock and sync.

- VT1.5 Pointer Processor — operates in one of two modes: STS-1 clear or VT1.5 mode.

  In the STS-1 clear mode, the incoming STS-1 signal is passed through to the Receive N-Rate Interface unaltered. Path overhead monitoring can take place.

  In the VT1.5 mode, the VT1.5 Pointer Processor circuitry performs VT pointer processing analogous to the STS-1 pointer processing done in the STS-1 Pointer Processor circuitry except on the 28 VT1.5 signals embedded in the received STS-1 payload. The functions performed in the VT1.5 mode are:

  1. Receive balanced CMOS line data, sync, and clock from the STS-1 Pointer Processor circuitry
  2. Monitor interdevice C1 parity over the incoming line STS-1 data
  3. Detect and report loss of line clock and sync
  4. Detect path AIS
  5. Perform STS-1 pointer interpretation to find the STS-1 SPE

6. Terminate STS-1 path overhead
7. Monitor and count B3 parity errors
8. Detect STS-1 path FEBE
9. Generate VT1.5 path AIS on outgoing VT1.5 signals
10. Perform VT1.5 SPE synchronization through pointer processing
11. Monitor VT1.5 pointer justifications
12. Report STS-1 and VT1.5 NDF
13. Build new STS-1 frame including insertion of A1A2 bytes based on system frame sync received from the Receive N-Rate Interface circuitry
14. Generate new H1H2 pointer values based on the system frame sync received from the Receive N-Rate Interface circuitry
15. Insert STS-1 path AIS
16. Detect and report loss of system clock and two 8-kHz sync.

    In addition, the VT1.5 Pointer Processor circuitry generates the 1-second Timebase Sync counter used for performance monitoring measurements.

- Receive N-Rate Interface — converts the received signal to two N-rate signals, which are sent to the Switch Module. The Receive N-Rate Interface supports three input signal format modes: STS-1 (cc-SPE), VT1.5(cc-SPE), and DS1. Both service and protection N-rate groups are supported. The Receive N-Rate Interface also performs N-rate clock and sync protection switching and sources switch and cross-connect maintenance information. The functions performed are:

  1. Receive balanced CMOS data from the VT1.5 Pointer Processor circuitry
  2. Monitor interdevice C1 parity over the incoming STS-1 data
  3. Detect and report loss of system 51.840-MHz clock
  4. Source two 8-kHz modulated sync clocks to the VT1.5 Pointer Processor circuitry
  5. In the STS-1(cc-SPE) mode:
     - — Generate CRC-6 over the STS-1 stream and embed in C1 byte to maintain cross-connect integrity through the Switch Module
     - — Bit disinterleave serial STS-1 stream and map to 30 of the 32 N-rate channels.
  6. In the VT1.5(cc-SPE) and DS1 mode:

- Demultiplex the STS-1 signal into 28 VT1.5 channels
- Generate seven 6.912 Mb/s VT-group signals compatible with the VT1.5/DS1 Mapping circuitry from the 28 VT1.5 channels
- Output VT-group signals along with VT-group clock and sync to the VT1.5/DS1 Mapping circuitry
- Generate parity over VT-group data.

7. In the VT1.5(cc-SPE) mode:
   - Map individual VT1.5(cc-SPE) signals to individual N-rate channels (this mapping uses up to 28 of the 32 total channels on the two N-rate signals)
   - Generate parity over the VT multiframe and embed in the V4 byte.
8. In the DS1 mode:
   - Receive 28 DS1 signals and map any number to individual N-rate channels (DS1 signals map up to 28 of the 32 total channels on the two N-rate signals)
   - Generate and insert stuff channel parity over the DS1
   - Generate X-bit value to be used for cross-connect maintenance.
9. Generate and embed N-rate parity over the 16 bit N-rate data block
10. Generate two N-rate balanced signals (upper and lower) and drive both service and protection interfaces
11. Monitor service and protection N-rate clock
12. Monitor N-rate sync for both 123-kHz sync and embedded 285 Hz gapped sync information
13. Monitor and generate DS1 AIS.

- VT1.5/DS1 Mapping — receives VT-group data signals from the Receive N-Rate Interface circuitry, terminates the VT1.5 path overhead and maps DS1 signals from VT1.5 signals. The functions performed are:
  1. Receive VT-group data signal from the Receive N-Rate Interface circuitry
  2. Monitor VT-group parity over data
  3. Monitor loss of VT-group clock and sync
  4. Demultiplex VT-group signal into four VT1.5 signals
  5. Perform pointer interpretation on VT1.5 signals to find SPE
  6. Terminate VT path overhead

7. Monitor and count VT1.5 BIP-2 parity
8. Monitor for VT FEBE
9. Monitor VT path yellow
10. Detect VT path AIS
11. Extract DS1 from VT SPE
12. Insert DS1 AIS and AIS clock
13. Smooth DS1 data and clock through CMOS DS1 clock and data to the Receive N-Rate Interface circuitry.

The following blocks are used to process the two N-rate signals received from the Switch Module in the transmit direction:

- Transmit N-Rate Interface — converts the received cross-connected N-rate signals from the Switch Module to the STS-1 signal format. The Transmit N-Rate Interface supports three signal format modes: STS-1 (cc-SPE), VT1.5(cc-SPE), and DS1.N-rate data and timing protection switching is performed. The Transmit N-Rate Interface also performs switch and cross-connect maintenance functions and is used as the core timing source (in conjunction with the 51.840-MHz oscillator) for the SMUX circuit pack (that is, generates all internal timing and sync references from the 27.648-MHz service N-rate clock received from the CLKDR circuit packs). The functions performed are:

  1. Receive service and protection balanced CMOS clock and sync from backplane
  2. Monitor service and protection N-rate clock
  3. Monitor service and protection N-rate sync for both 123-kHz sync and 285 Hz gapped sync information
  4. Perform N-rate clock and sync protection switching under software control
  5. Receive service and protection N-rate data sets (upper and lower) and perform protection switching under software control
  6. Monitor service and protection N-rate data inputs for N-rate parity errors
  7. In the STS-1(cc-SPE) mode:
     - — Bit interleave the two serial N-rate data streams (except for parity bit position) and generate STS-1 signal
     - — Generate CRC-6 over the STS-1 stream, compare to embedded value in C1 byte, and monitor for errors to maintain cross-connect integrity through the switch.

8. In the VT1.5(cc-SPE) mode:
   - — Map individual N-rate channels to VT1.5(cc-SPE) signals (this mapping uses up to 28 of the 32 total channels on the two N-rate signals)
   - — Extract and monitor V4 parity.
9. In the DS1 mode:
   - — Demap N-rate channel to DS1 signal, monitor each DS1 stuff channel parity for errors to maintain cross-connect, and output up to 28 CMOS DS1 signals (data and clock) to the DS1 Timing circuitry
   - — Monitor stuff channel parity
   - — Monitor X-channel for cross-connect maintenance.
10. In the VT.15(cc-SPE) and DS1 modes:
    - — Output VT-group clock and sync to the VT1.5/DS1 Mapping circuitry
    - — Receive seven 6.912 Mb/s VT-group signals from the VT1.5/DS1 mapping circuitry and demultiplex each VT-group into four VT1.5 signals
    - — Monitor parity over VT-group data and report errors
    - — Multiplex 28 VT1.5 channels into STS-1 SPE and build STS-1 frame with H1H2 pointers around the SPE.
11. Generate and insert interdevice C1 parity into STS-1 signal
12. Output balanced CMOS STS-1 data and two 8-kHz sync references to the VT1.5 Pointer Processor circuitry
13. Divide down 51.840-MHz STS-1 system clock from oscillator to 1.728-MHz and output to the Receive N-Rate Interface and 51.840-MHz Clock circuitry
14. Divide down selected service 27.648-MHz N-rate clock to 1.728-MHz reference and output to the Receive N-Rate Interface and 51.840-MHz Clock circuitry
15. Insert DS1 or VT1.5 AIS
16. Insert all zeros DS1.

- DS1 Timing — destuffs the N-rate channel rate to recover the DS1 data. The destuffing process leaves gaps in the DS1 data stream which are removed before converting to a VT1.5 signal. The DS1 Timing circuitry receives gapped data and clock signals from the Transmit N-Rate Interface circuitry, buffers the gapped data, and clocks it out on the smoothed clock to the VT1.5/DS1 Mapping circuitry. Each DS1 Timing half services and performs signal maintenance on 14 DS1 signals. The functions performed are:
    1. Receive DS1 clock and data from the Transmit N-Rate Interface circuitry
    2. Detect and report loss of DS1 clock on each DS1 input
    3. Detect "stuck ats" on DS1 data inputs
    4. Perform DS1 clock and data smoothing on each channel
    5. Output smoothed DS1 clock and data to the VT1.5/DS1 Mapping circuitry
    6. Receive and monitor DS1 test signal.
- VT1.5/DS1 Mapping — receives 28 DS1 data and clock signals from the DS1 Timing circuitry, maps DS1 signals to VT1.5 signals, and generates the VT path overhead. The functions performed are:
    1. Receive DS1 clock and data from the DS1 Timing circuitry
    2. Monitor and detect DS1 loss of clock
    3. Monitor DS1 input
    4. Autonomous insertion of DS1 AIS into VT1.5
    5. Stuff DS1 and map into VT1.5 SPE
    6. Insert VT path overhead
    7. Generate BIP-2 parity
    8. Insert VT FEBE
    9. Insert VT path yellow
    10. Generate VT pointers and build a VT1.5 signal based on VT-group sync from Transmit N-Rate Interface circuitry
    11. Multiplex four VT1.5 signals into a VT-group serial stream
    12. Generate VT-group parity and inset into VT-group serial stream
    13. Output VT-group signal to the Transmit N-Rate Interface circuitry.

- VT1.5 Pointer Processor — operates in one of two modes: STS-1 clear or VT1.5 mode.

  In the STS-1 clear mode, the incoming STS-1 signal is passed through to the STS-1 Byte Processor circuitry unaltered. Path overhead monitoring can take place.

  In the VT1.5 mode, the VT1.5 Pointer Processor circuitry inserts STS-1 path overhead on the STS-1 data received from the Transmit N-Rate Interface circuitry. The functions performed in the VT1.5 mode are:

  1. Receive balanced 51.840-Mbs/s data, and two modulated 8-kHz sync references from the Transmit N-Rate Interface circuitry
  2. Monitor interdevice C1 parity over the incoming STS-1 data
  3. Monitor loss of clock and sync
  4. Insert STS-1 path overhead
  5. Generate B3 parity
  6. Insert STS-1 path FEBE
  7. Insert STS-1 path yellow
  8. Insert STS-1 path AIS source balanced CMOS 2-kHz sync and data to the Receive N-Rate Interface circuitry with embedded interdevice C1 parity.

  In addition the VT1.5 Pointer Processor circuitry generates the one-second Timebase Sync counter used for performance monitoring measurements.

- STS-1 Byte Processor — generates the transport overhead portion of the STS-1 signal. The functions performed are:

  1. Receive balanced 51.840-Mbs/s data, clock, and sync from the VT1.5 Pointer Processor circuitry
  2. Monitor interdevice C1 parity over the incoming STS-1 data
  3. Insert A1A2 bytes
  4. Insert C1 byte value = 00001111
  5. Generate and insert B1 parity
  6. Generate and insert B2 parity
  7. Generate and insert line FERF
  8. Generate path AIS
  9. Source APS in K1K2 bytes
  10. Pass remaining transport overhead or force to 00000000
  11. Scramble STS-1 signal

12. Convert single rail signal to dual-rail signal
13. Encode STS-1 signal to B3ZS format
14. Clock duty-cycle correction.

In addition, when operating an STS-1 line loopback, the receive input is looped back to the transmit output.

- Output Line Driver — converts the dual-rail signal received from the STS-1 Byte Processor circuitry into a bipolar STS-1 signal. This signal is output directly or through a jumper-selectable line buildout (LBO) circuit to the Protection Relays circuitry.
- Protection Relays — connects the SMUX to the transmit protection bus daisy-chain. The transmit daisy-chain connects each SMUX circuit pack to the SMUXP circuit pack through the MUXPS circuit pack. In addition, the protection relay determines if the STS-1 signal is output from the SMUX or SMUXP circuit pack. Refer to the next section titled "Protection Bus" for more information.

## SONET Multiplexer Protection (SMUXP)

The SMUXP circuit pack provides protection for SMUX circuit packs within an interface protection group (that is, all SMUX circuit packs within the same interface module). When active, SMUXP circuit packs perform the same STS-1 transmission functions as SMUX circuit packs (except for signal splitting and protection relay functions). In an STS1 Interface-16 Module, protection is provided for STS-1 facilities on a 1-to-15 basis.

## STS1 Protection Bus

Figure 6-17 is a block diagram of the protection bus within an STS1 protection group (that is, all SMUX circuit packs within an STS1 Interface-16 Module). The functions provided by the circuit packs are described below.

### SONET Multiplexer (SMUX)

The SMUX circuit pack contains protection relays, which when activated allow for an STS-1 signal to be processed by the SMUXP circuit pack. The 15 SMUX circuit packs within an STS1 Interface-16 Module are daisy-chained together and routed to the MUXPS circuit pack.

### Bus Extender A (BXA)

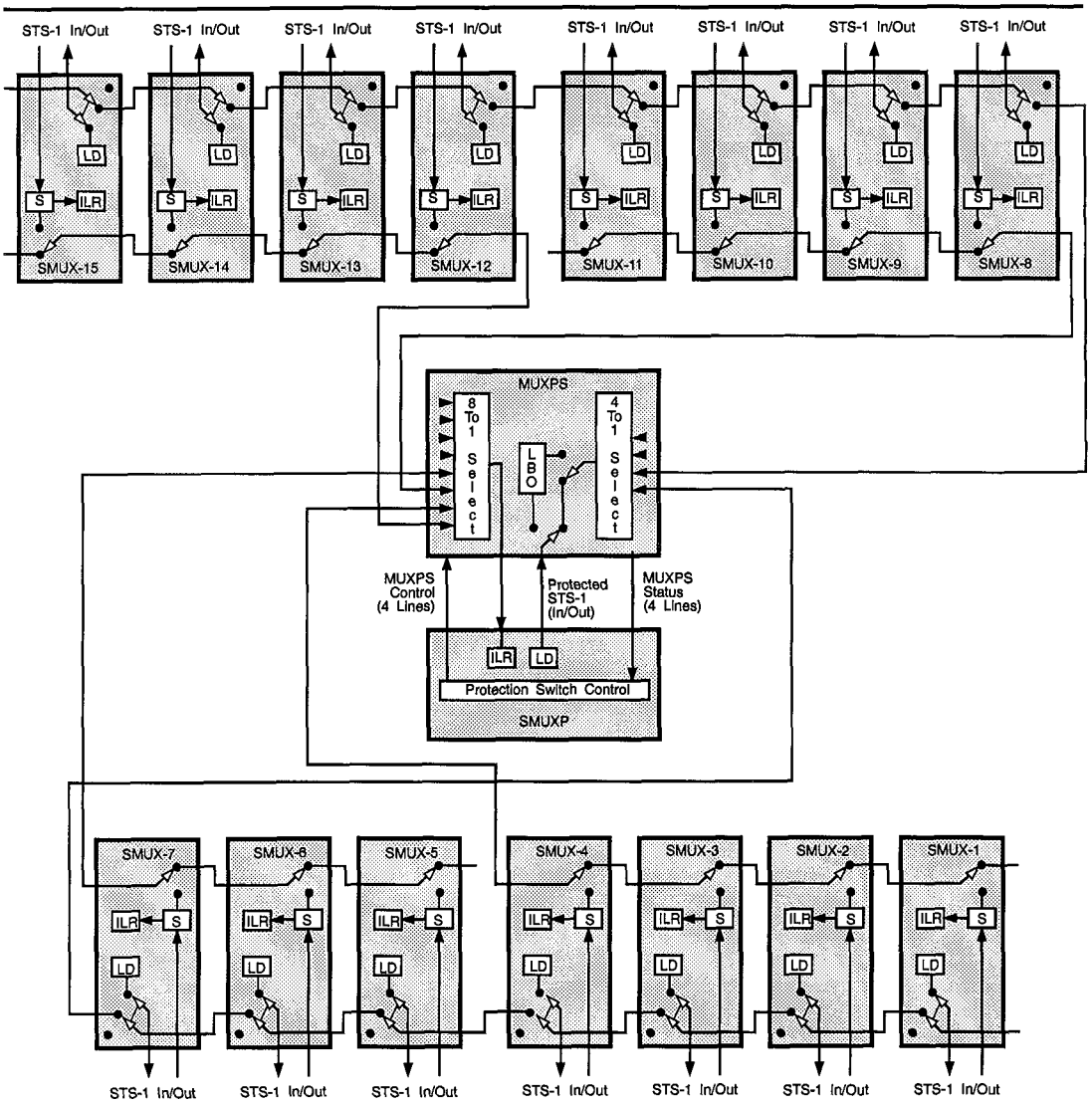
The BXA circuit pack is installed in empty SMUX circuit pack slot to provide protection bus integrity (that is, maintain the daisy-chain) and to keep out dust and foreign matter.

### Multiplexer Protection Switch (MUXPS)

The MUXPS circuit pack terminates the receive and transmit protection daisy-chains of the SMUX circuit packs and routes the STS-1 signals to the SMUXP circuit pack. In the receive direction, four groups of SMUX circuit packs are daisy-chained together and routed to the MUXPS circuit pack. In the transmit direction, two groups of SMUX circuit packs are daisy-chained together and routed to the MUXPS circuit pack. Control from the UC/SMUXP circuit packs selects the appropriate groups when necessary. If an SMUX circuit pack fails, the UC directs the SMUXP and MUXPS circuit packs to send the affected STS-1 signal to the SMUXP circuit pack and activates the associated protection relays within the failed SMUX circuit pack, allowing the affected STS-1 signal to be protected. The MUXPS LBO setting is determined by the failed SMUX circuit pack.

### SONET Multiplexer Protection (SMUXP)

The SMUXP circuit pack provides protection for SMUX circuit packs within an interface protection group (that is, all SMUX circuit packs within the same interface module). The SMUXP circuit pack selects the appropriate daisy-chain group when directed by the UC circuit pack to provide protection for an STS-1 signal. Status lines from the MUXPS circuit pack provide state information of the MUXPS circuit pack to the SMUXP. In an STS1 Interface-16 Module, the SMUXP circuit pack provides protection for EC-1 facilities (STS-1 signals) on a 1-to-15 basis.




**Notes:**

ILR = Input Line Receiver
S = Signal Splitter
LD = Output Line Driver
LBO = Line Buildout

For STS-1 Interface Modules, only four of the receive select lines and two of the transmit select lines of the MUXPS circuit pack are needed. When BXA circuit packs are inserted for SMUX circuit packs, the daisy-chain connections (receive and transmit paths) are maintained.

Figure 6-17. **STS1 Interface-16 Module Block Diagram (Protection Bus)**

# DS1 Performance Monitoring Hardware

The DACS IV-2000 can support different hardware configurations to allow for the following three options of DS1 performance monitoring:

- Dedicated Full-Time Monitoring
- Camp-On Full-Time Monitoring
- Scanned Monitoring.

Due to interface module configuration constraints, the number of PMGR circuit packs per interface module is limited by the following factors:

- UC4 circuit pack memory (scanned performance monitoring has a higher demand on memory than full-time/camp-on performance monitoring)
- Only one PMGR circuit pack can be provisioned to perform scanned performance monitoring per SWIO/OSWIO circuit pack pair.

Table 6-16 lists the maximum number of PMGR circuit packs in each interface module type for given performance monitoring mode combinations.

Table 6-16. **Maximum PMGR Circuit Packs per Interface Module**

| Interface Module Type | Performance Monitoring Mode | |
|---|---|---|
| | Scan | Dedicated Full-Time/ Camp-On Full-Time |
| DS3 Interface-32 | 0 | 16 |
| | 1 | 8 |
| | 2 | 2 |
| DS3 Interface-16 | 0 | 15 |
| | 1 | 8 |
| DS1 Interface | 0 | 8 |
| | 1/0* | 7 |
| DS1 Interface-Protection | 0 | 7 |
| | 1/0† | 6 |

* Zero if there is a scanned performance monitoring PMGR circuit pack in the DS1 Interface or Interface-Protection Module associated with the same SWIO/OSWIO circuit pack pair.

† Zero if there is a scanned performance monitoring PMGR circuit pack in the DS1 Interface Module associated with the same SWIO/OSWIO circuit pack pair.

The following sections describe the hardware configurations necessary to accommodate the different options of DS1 performance monitoring (including PMGR circuit pack usage).

## Dedicated Full-Time Monitoring

Dedicated Full-Time Monitoring uses one of the following two circuit packs:

- The SWIF2 circuit pack monitors a group of 28 DS1 signals associated with the SWIF2 circuit pack's two DS1IF circuit packs.
- The MUX3 circuit pack monitors a group of 28 DS1 tributaries associated with the DS3 signal demultiplexed by the MUX3 circuit pack.

This option is generally employed when all or a large fraction of the incoming DS1 facilities or DS1 tributaries require full-time monitoring. Figure 6-18 shows these configurations.

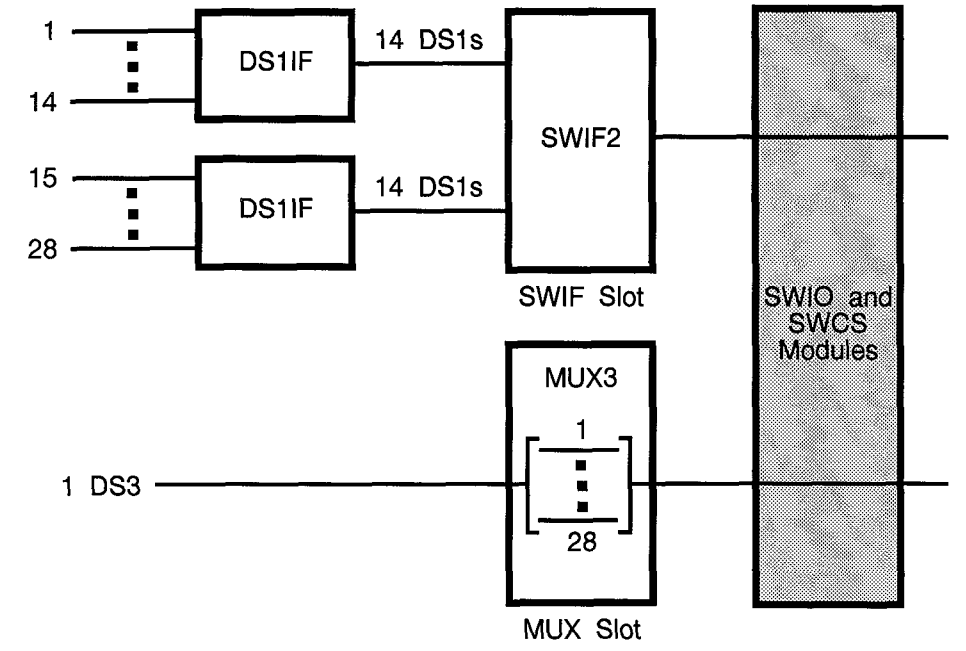



Figure 6-18. **Dedicated Full-Time DS1 PM Using SWIF2 or MUX3 Circuit Pack**

To implement the dedicated full-time mode for DS1 facilities, SWIF2 circuit packs are required for the DS1 interface groups that are going to be monitored. Any number of SWIF circuit pack slots (except protection SWIF slots) can be equipped with a SWIF2 circuit pack with no loss of switching capacity and constraints on number of PMGR circuit packs used for other modes of DS1 performance monitoring. Performance-monitoring data is not collected when a DS1 interface group is being protected by the DS1 protection group. Procedures for changing SWIF1 circuit packs are in the *DACS IV-2000 (512) Release 5.0 Operations and Maintenance* manual (AT&T 365-340-901).

To implement the dedicated full-time mode for DS1 tributaries of DS3 signals terminating on MUX3 circuit packs, only Enhanced or DS3CC Interface Modules can be used.

## Camp-On Full-Time Monitoring

Camp-on Full-Time Monitoring uses the PMGR circuit pack and monitors any DS1 signal not already monitored in the dedicated full-time option. This option is generally employed when you desire to perform selected full-time monitoring facilities or DS1 tributaries within DS3 (MUX1 or MUX2 circuit packs) or EC-1 facilities. Figure 6-19 shows this type of configuration.

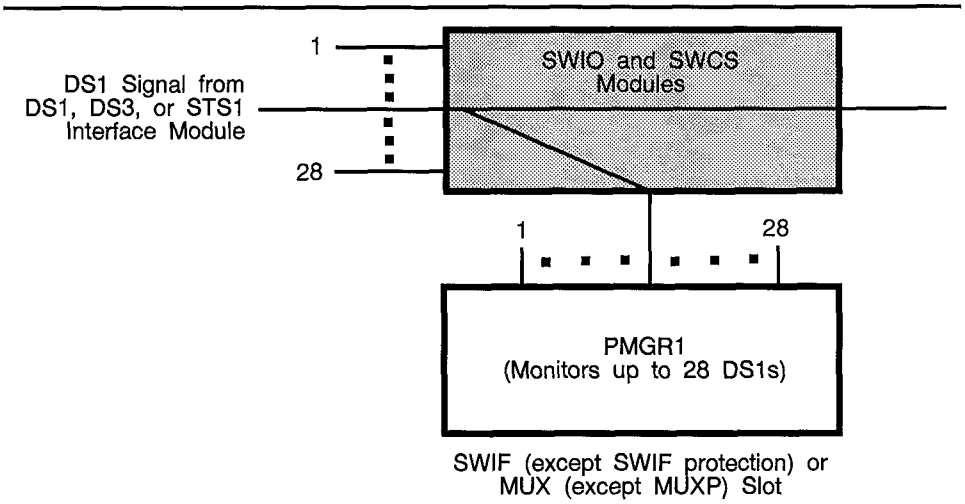



Figure 6-19. **Camp-On Full-Time DS1 PM**

To implement the camp-on full-time mode for DS1 facilities or DS1 tributaries within a DS3 facility, insert PMGR1 circuit packs into SWIF or MUX (except protection SWIF or MUXP) circuit pack slots (except Enhanced DS3 Interface-16 and DS3 Clear-Channel Interface-16 Modules). When using SWIF circuit pack slots, the associated DS1IF circuit pack slots must contain either DS1IF or BXA circuit packs. Switching capacity is decreased by 28 DS1 signals for each PMGR1 circuit pack used. In addition, depending on your configuration of camp-on full-time and scanned monitoring, the number of PMGR1 circuit packs used for the camp-on full-time mode can be limited. The following constraints (summarized in Table 6-16) apply:

- No scanned monitoring used:
  - — DS1 Interface Modules — up to 8 PMGR1 circuit packs
  - — DS1 Interface-P Modules — up to 7 PMGR1 circuit packs
  - — DS3 Interface-16 Modules — up to 15 PMGR1 circuit packs
  - — DS3 Interface-32 Modules — up to 16 PMGR1 circuit packs
- Scanned monitoring used:
  - — Pair of DS1 Interface Modules associated with the SWIO circuit pack pair scan monitored by a PMGR circuit pack — up to 15/14 PMGR1 circuit packs for camp-on full-time mode
  - — DS3 Interface-16 Module using PMGR circuit for scanned monitoring SWIO circuit pack pair — up to 8 PMGR1 circuit packs for camp-on full-time mode
  - — DS3 Interface-32 Module using one PMGR circuit for scanned monitoring SWIO circuit pack pair (either MUX-{1-15} or MUX-{16-31}) — up to 8 PMGR1 circuit packs for camp-on full-time mode
  - — DS3 Interface-32 Module using two PMGR circuit for scanned monitoring both SWIO circuit pack pairs (MUX-{1-15} and MUX-{16-31}) — up to 2 PMGR1 circuit packs for camp-on full-time mode.

## Scanned Monitoring

Scanned monitoring is provided when the performance health of the DS1 signal is desired but when full-time monitoring is not required. This mode is the most cost-effective mode provided by the DACS IV-2000, as one PMGR circuit pack can monitor up to 420 DS1 signals within the same switch I/O pair (each of the 28 ports associated with a PMGR circuit packs can scan up to 15 DS1 signals). Figure 6-20 shows this type of configuration.

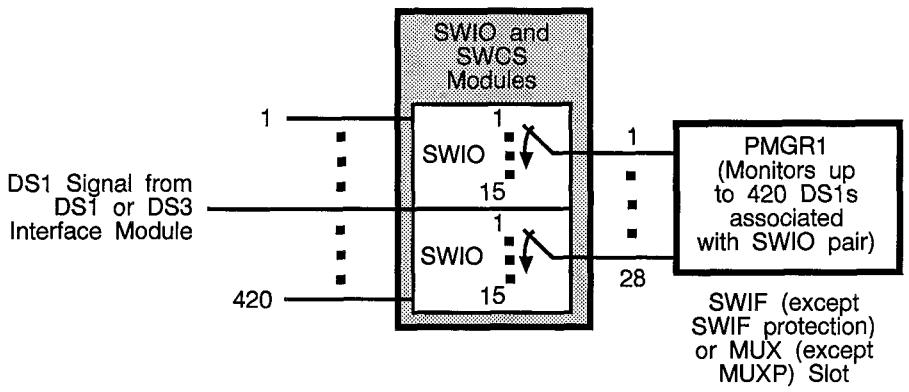



Figure 6-20. **Scanned DS1 PM**

To implement the scanned mode for DS1 facilities or DS1 tributaries within DS3 facilities, PMGR1 circuit packs are required to be inserted into SWIF (except protection SWIF) or MUX (except MUXP) circuit pack slots (except Enhanced Interface-16 and DS3CC Interface-16 Modules). When using SWIF circuit pack slots, the associated DS1IF circuit pack slots must contain either DS1IF or BXA circuit packs. Switching capacity is decreased by 28 DS1 signals for each PMGR1 circuit pack used. Only one PMGR1 circuit pack can be used for scanned monitoring per SWIO circuit pack pair. That is, one PMGR1 circuit pack can be used for each pair of DS1 Interface Modules (upper pair or lower pair within an DS1 or STS1/DS3/DS1 Interface Bay), one PMGR1 circuit pack per DS3 Interface-16 Modules, and up to two PMGR1 circuit packs per DS3 Interface-32 Modules (one for MUX-{1-15} and one for MUX-{16-31}). In addition, the constraint on the number of PMGR1 circuit packs used for scanned monitoring depends on the number of PMGR1 circuit packs used for bridged access or camp-on monitoring. Scanned monitoring can not be done for DS1s within VT1.5s of EC-1 facilities or for Enhanced DS3 Interface-16 or DS3CC Interface-16 Modules.

The procedure for provisioning PMGR circuit packs is in the Chapter 5 of the *DACS IV-2000 (512) Release 5.0 Operations and Maintenance* manual (AT&T 365-340-901).

## Interface Bay Circuit Packs

Table 6-17 lists the circuit pack equipment for the interface bays for both collocated and Remote Complex configurations. Only circuit packs used in interface bays are listed in Table 6-17.

Table 6-17. **Circuit Pack Equipment for the Interface Bays**

| Functional Name | Circuit Pack or Equipment Code | Used In | Number Required | See Note |
|---|---|---|---|---|
| BXA1 (Bus Extender 1) | AKM64 | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod<br>DS3CC INTFC-16 Mod<br>ENH DS3 INTFC-16 Mod<br>STS1 INTFC-16 Mod | As required | 1 |
| CLKDR2 (Clock Distributor 2) | AKM90 | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod<br>DS3CC INTFC-16 Mod<br>ENH DS3 INTFC-16 Mod<br>STS1 INTFC-16 Mod | 2<br>2<br>2<br>4<br>2<br>2<br>2 | |
| DS1IF1 (DS1 Interface 1) | AKM46B | DS1 INTFC Mod<br>DS1 INTFC-P Mod | 0-16<br>0-14 | 2,3,5<br>2,3,5 |
| DS1IP1 (DS1 Interface Protection 1) | AKM47 | DS1 INTFC-P Mod | 2 | |
| DS1RY1 (DS1 Relay 1) | AKM48 | DS1 INTFC Mod<br>DS1 INTFC-P Mod | 4 | |
| DS3PM2 (DS3 Performance Monitor 2) [optional] | AKM89 | DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod<br>DS3CC INTFC-16 Mod<br>ENH DS3 INTFC-16 Mod | 0 or 1 | 2,6 |
| MUX1 (Multiplexer 1) | AKM52B | DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod | 1-15<br>1-31 | 2,4<br>2,4 |
| MUX2 (Multiplexer 2) | AKM68B | DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod<br>ENH DS3 INTFC-16 Mod | 1-15<br>1-31<br>0-15 | 2,4<br>2,4<br>2,4,7 |
| MUX3 (Multiplexer 3) | AKM91 | ENH DS3 INTFC-16 Mod<br>DS3CC INTFC-16 Mod | 0-15<br>1-15 | 2,4,7<br>2,4 |

Table continued on next page; notes are listed at end of table.

Table 6-17. **Circuit Pack Equipment for the Interface Bays (Continued)**

| Functional Name | Circuit Pack or Equipment Code | Used In | Number Required | See Note |
|---|---|---|---|---|
| MUXP1 (Multiplexer Protection 1) | AKM55 | DS3 INTFC-16 Mod<br>DS3 INTFC-31 Mod | 1 | 4 |
| MUXP2 (Multiplexer Protection 2) | AKM70 | DS3 INTFC-16 Mod<br>DS3 INTFC-31 Mod<br>ENH DS3 INTFC-16 Mod | 1 | 4,8 |
| MUXP3 (Multiplexer Protection 3) | AKM92 | ENH DS3 INTFC-16 Mod<br>DS3CC INTFC-16 Mod | 1 | 4,8 |
| MUXPS1 (Multiplexer Protection Switch 1) | AKM53 | DS3 INTFC-16 Mod<br>DS3 INTFC-31 Mod<br>ENH DS3 INTFC-16 Mod<br>DS3CC INTFC-16 Mod<br>STS1 INTFC-16 Mod | 1 | |
| PMGR1 (Performance Monitor Generator/Receiver 1) [optional] | AKM66 | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod | 0-8<br>0-7<br>0-14<br>0-16 | 9<br>9<br>9<br>9 |
| PWRE3 (Power E3) | 556B/556C | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-31 Mod<br>ENH DS3 INTFC-16 Mod<br>DS3CC INTFC-16 Mod<br>STS1 INTFC-16 Mod | 2 | |
| SMUX1 (SONET Multiplexer 1) | AKM84 | STS1 INTFC-16 Mod | 1-15 | 2,4 |
| SMUXP1 (SONET Multiplexer Protection 1) | AKM85 | STS1 INTFC-16 Mod | 1 | 4 |

Table continued on next page; notes are listed at end of table.

Table 6-17. **Circuit Pack Equipment for the Interface Bays (Continued)**

| Functional Name | Circuit Pack or Equipment Code | Used In | Number Required | See Note |
|---|---|---|---|---|
| SWIF1/SWIF2<br>(Switch Interface 1/2) | AKM49/AKM50 | DS1 INTFC Mod<br>DS1 INTFC-P Mod | 0-8<br>1-8 | 2,3,10<br>2,3,10 |
| UC4/UC4B<br>(Unit Controller 4/4B) | AKM88/AKM88B | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-31 Mod<br>ENH DS3 INTFC-16 Mod<br>DS3CC INTFC-16 Mod<br>STS1 INTFC-16 Mod | 1 | 11 |

Notes:

1. The BXA1 circuit packs are installed in unused DS1IF, SWIF, MUX, DS3PM, and SMUX circuit pack slots. They must not be installed in any other circuit pack slots (that is, UC, CLKDR, DS1RY, MUXPS, PWRE, and protection [DS1IP, SWIF-P, MUXP, and SMUXP] circuit pack slots).
2. Unused DS1IF, SWIF (not protection), MUX, DS3PM, and SMUX circuit pack slots must contain BXA circuit packs.
3. One protection group and at least one service group of circuit packs within an interface bay must be installed.
4. One protection and at least one service circuit pack must be installed.
5. Must be installed in adjacent pairs.
6. DS3PM2 circuit packs can only be used in collocated DS3 Interface Modules. DS3PM2 circuit packs can not be used in Remote Complex interface modules.
7. An Enhanced DS3 Interface-16 Module must contain at least one MUX2 or MUX3 circuit pack.
8. A MUXP3 circuit pack is required in a DS3 Interface Module that contains at least one MUX3 circuit pack.
9. PMGR circuit packs are installed in SWIF (not protection) or MUX circuit pack slots. PMGR circuit packs can not be installed in Enhanced DS3 Interface-16, DS3 Clear-Channel Interface-16, or STS1 Interface-16 Modules.
10. SWIF2 circuit packs are required for full-time DS1 performance monitoring of DS1 Interface Modules.
11. UC4 (AKM88) circuit packs are required for collocated interface modules. UC4B (AKM88B) circuit packs are required for Remote Complex interface modules.

# Power and Miscellanous Hardware

# 7

## Contents


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# Contents

# Power and Miscellaneous Hardware

# 7

This chapter describes the DACS IV-2000 power distribution and the following miscellaneous hardware:

- Fan Assemblies
- BNC Connectors
- EMC Enclosures
- System Power and Fusing.

## Fan Assemblies

Fan assemblies ED-2C816-30 and ED-2C906-30 are used to cool vertically mounted assemblies only in the OPEX Bay. Fan assemblies ED-9C130-30 ED-9C130-30 and WP-92310,L4 are used to cool vertically mounted assemblies in the Switch Bay, Main Controller, OPEX Bay, and the following interface bays: ENH DS1, STS1/DS3, or ENH STS1/DS3, and ENH STS1/DS3/DS1 Interface Bays.

### ED-2C816-30 and ED-2C906-30 Fans

Figure 7-1 shows fan assemblies ED-2C816-30 and ED-2C906-30, which are used to cool vertically mounted assemblies only in the OPEX bay (not in the any other bay). Each fan assembly consists of three horizontally mounted fans along with a filter and control switches and indicators. You must keep the air intake (under the assembly) free of obstructions. You must also inspect the filter (and change if necessary) at recommended intervals. An autonomous message

(REPT FAN FILTER), generated after the recommended filter replacement interval of 91 days has occurred, reminds you that the fan filter needs to be replaced. This message must be acknowledged with the ENT-FAN-FILTER command when the fan filter is changed. The input operating voltage range of the assembly is -40.5 to -60 Vdc at approximately 1.57A.

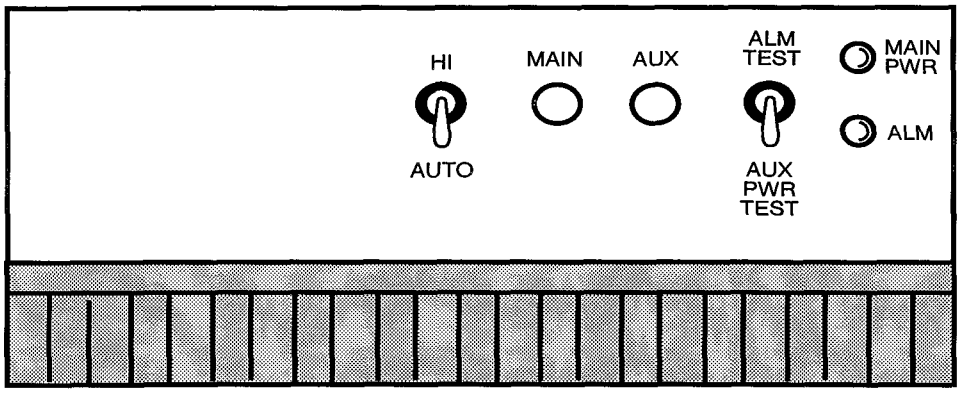



Figure 7-1. **ED-2C816-30 and ED-2C906-30 Fans**

The front panel of the fan assembly contains the following switches and indicators:

- A two-position toggle switch labeled HI/AUTO. When the switch is in the AUTO position, a controller causes the fans to operate at reduced speed when the ambient air temperature is below 90°F. For a temperature of 90° F or higher, the fans automatically go to full speed operation. When the switch is in the HI position, the fans operate continuously at maximum speed.
- MAIN and AUX power circuit breakers
- A three-position spring-loaded toggle test switch labeled ALM TEST/AUX PWR TEST with the center position as off. When the switch is held to the ALM TEST position, input power is cut off to one fan causing the ALM LED indicator to light. The remaining two fans shift to high speed (if not already operating at high speed). When the switch is held to the AUX PWR TEST position the MAIN input power is overridden, forcing auxiliary power operation. This action causes the ALM indicator to light, the MAIN PWR indicator to go off, and all three fans to switch to high speed (if not already operating at high speed).
- A green LED labeled MAIN PWR to indicate that main power is available to the fan assembly.
- A red LED labeled ALM to indicate power or fan failure.

## ED-9C130-30 and WP-92310,L4 Fans

Figure 7-2 shows fan assemblies ED-9C130-30 and WP-92310,L4 which are used to cool vertically mounted assemblies in the Switch Bay, Main Controller, OPEX Bay, and the following interface bays: ENH DS1, STS1/DS3, or ENH STS1/DS3, and ENH STS1/DS3/DS1 Interface Bays. Each fan assembly consists of three horizontally mounted fans along with a filter and control switches and indicators. You must keep the air intake (under the assembly) free of obstructions. When the minor FILTER alarm LED on the fan assembly turns on, the fan filter must be replaced. After replacing the fan filter and pressing the RESET button, the FILTER alarm LED turns off. The input operating voltage range of the assembly is -40.5 to -60 Vdc at approximately 1.57A.

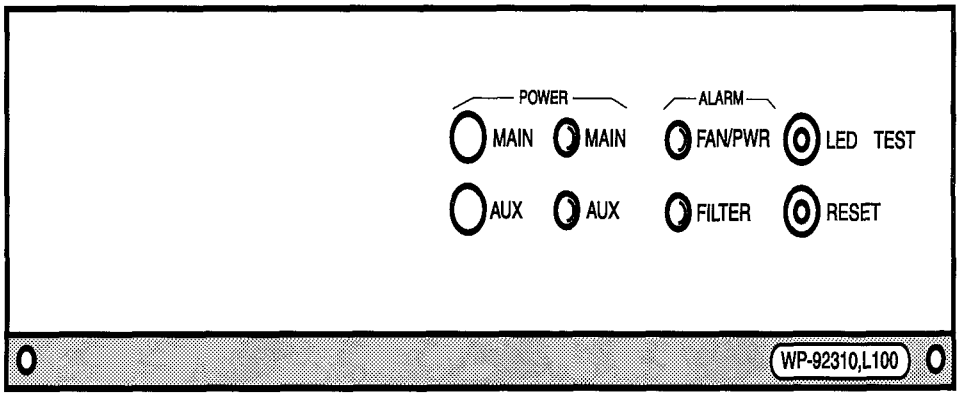



Figure 7-2. **ED-9C130-30 and WP-92310,L4 Fans**

The front panel of the fan assembly contains the following buttons and indicators:

- MAIN and AUX power circuit breakers
- Two green LEDs labeled MAIN and AUX; when lit, indicate main or auxiliary power is available to the fan assembly.
- A red LED labeled FAN/PWR; when lit, indicates a power or fan failure.
- A yellow LED labeled FILTER; when lit, indicates the fan filter needs replacing.
- A push button labeled LED TEST. Press this button to check the operation of the fan assembly LEDs.
- A push button labeled RESET. Press this button to clear an alarm and return the fan assembly to normal operation, after clearing an alarm associated with the fan assembly.

## BNC Connectors

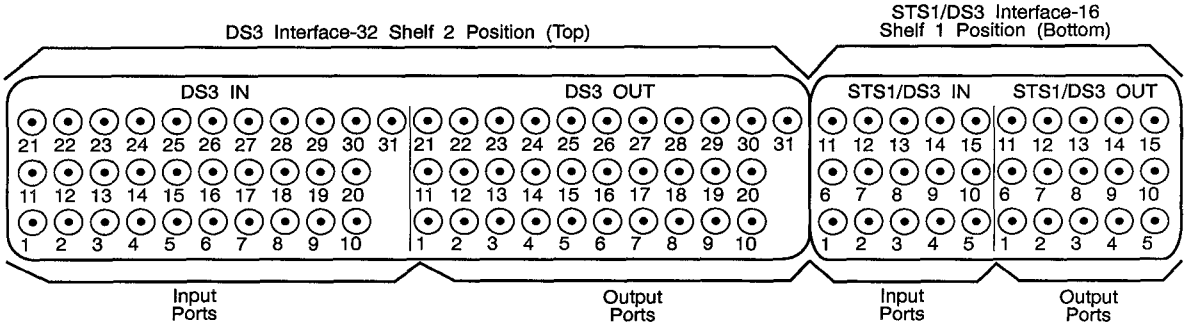
The DACS IV-2000 can be equipped with BNC connectors on STS1/DS3/DS1, STS1/DS3, and DS3 Interface Bays. These connectors provide the DACS IV-2000 with easy access to/from EC1 and DS3 facilities. BNC connectors, when provided are located at the top of the interface bay and are accessed from the rear of the bay lineup. BNC connectors are provided for each input and output port associated with MUX and SMUX circuit packs contained in STS1 and/or DS3 Interface Modules.

Figure 7-3 shows the different types of BNC connector panels for each of the STS1/DS3/DS1, STS1/DS3, and DS3 Interface Bays. The BNC connectors are panel-stamped to identify which connector is associated with the corresponding MUX/SMUX input/output port (that is, DS3 Interface-32 Module connectors are numbered 1 through 31 and STS1/DS3 Interface-16 Module connectors are numbered 1 through 15). In addition, Figure 7-3 associates the group of BNC connectors with its interface module shelf position.

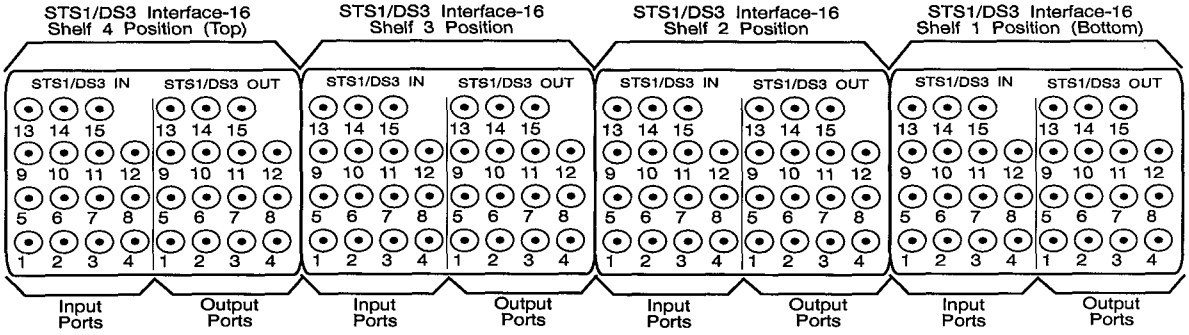
## EMC Enclosures

The DACS IV-2000 meets the electromagnetic compatibility (EMC) FCC criteria and the electrostatic discharge (ESD) requirements specified in Bellcore TR-NWT-001089. Enclosures must be ordered with any new frame and cannot be field retrofitted.

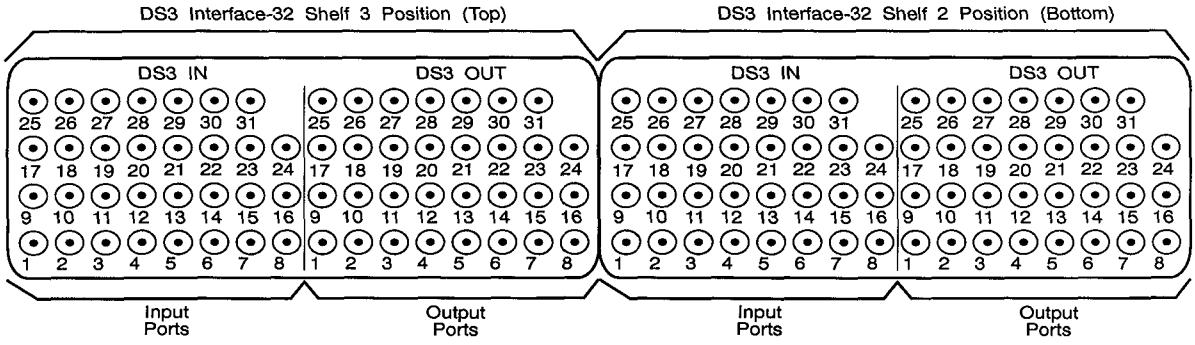
ESD grounding connections are provided on the front and rear of each bay and you are required to use wrist straps while handling the equipment.




**A. STS1/DS3/DS1 Interface Bay**




**B. STS1/DS3 Interface Bay**




**C. DS3 Interface Bay**

Figure 7-3. **BNC Connector Panels**

# Power

The DACS IV-2000 power and duplex power information for collocated and remote complexes is described in the following sections.

## Switch Complex and Collocated Interface Bays Configuration

The DACS IV-2000 Switch Complex and collocated interface bays operates with two Lineage® 2000 (or equivalent) battery plants, Battery Distribution Feeder Board (BDFB) A and B (-48 Vdc nominal) in the central office environment with collocated interface bays. Each BDFB supplies four power buses in each fuse and alarm panel in the Switch Bays and four power buses in the fuse and alarm panel in the Fuse and Alarm Bays. BDFB A supplies power buses AA through AD and BDFB B supplies power buses BA through BD. All feeders have four connections to the fuse and alarm panels.

The two BDFBs provide duplication of the power supply (Figure 7-4) and allow the system to operate in the event one battery plant fails.

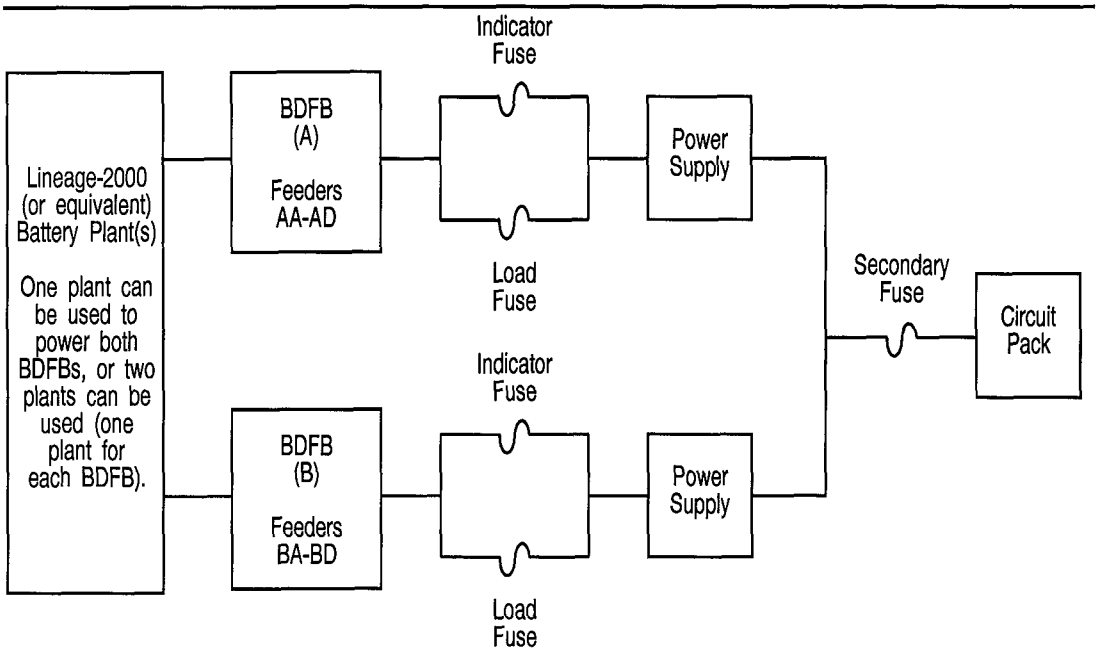



Figure 7-4. **Fuse Interconnection (Switch Complex and Collocated Interface Bays)**

## Remote Complexes

The DACS IV-2000 Remote Complex is configured to accept two power supply arrangements, standard or duplex. The standard configuration consists of one Battery Distribution Feeder Board (BDFB) powered from a single Lineage 2000 (or equivalent) battery plant. The duplex configuration consists of two BDFBs powered from one or two Lineage 2000 (or equivalent) battery plants.

## Standard Power Configuration

In the standard configuration (Figure 7-5), the DACS IV-2000 Remote Complex operates with a Lineage 2000 (or equivalent) battery plant (-48 Vdc nominal) in a central office environment supplying power to a single BDFB. Seven power feeders and seven returns are terminated at the OPEX Bay and provide power for the entire Remote Complex. The feeders are designated by the loads they serve: A, B, C, D, E, F, and G. Each load is fused separately.

- Feeders A, B, C, D, and E (connected through the Fuse and Alarm Panel) supply power to the facility interface bays, the OPEX PWR Module, and the fan assemblies.
- Feeders F and G (connected directly to the RUI PWR Module) supply power to the RUI PWR Module.

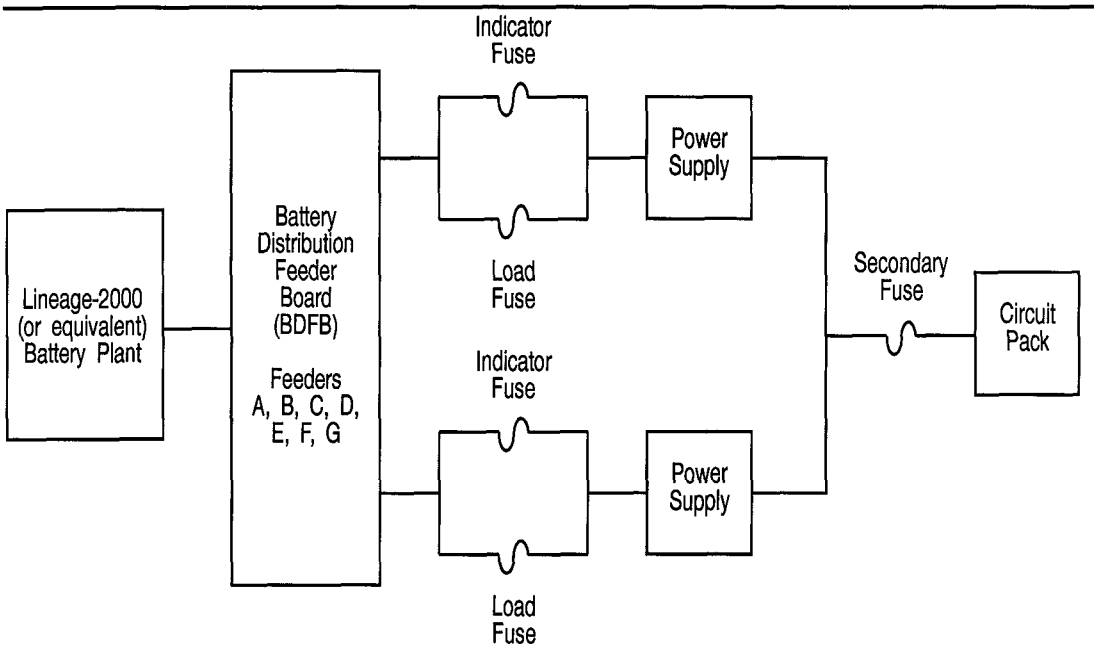



Figure 7-5. **Standard Power Fuse Interconnection (Remote Complex)**

## Duplex Power Configuration

The duplex power feature configuration (Figure 7-6), provides compatibility with the "red and blue" central office power distribution being deployed in the AT&T Network, and with other power-distribution arrangements. The duplex power feature uses one or two -48V diverse power plants. (A diverse power plant is one that does not share common components, such as rectifiers, batteries, BDFBs, and cable racks.)

Twelve power feeders (A1 through F1 and A2 through F2) and twelve returns are terminated at the OPEX Bay and provide power for the entire Remote Complex. The red battery plant supplies A, B, and E; the blue battery plants supplies C, D, and F. All power feeders are connected to the Fuse and Alarm Panel.

When the Remote Complex is powered using two battery plants, the following requirements apply:

- Power feeders to the Remote Complex must be placed in two groups to allow connection to two separate BDFBs.
- Two battery plants (red and blue) are required.
- Feeders A, B, and E are fed from the red battery plant; feeders C and D are fed from the blue battery plant.

Loss of one battery plant or one group of feeders connected to that plant does not cause any loss of service (except where there is only one battery plant supplying power).

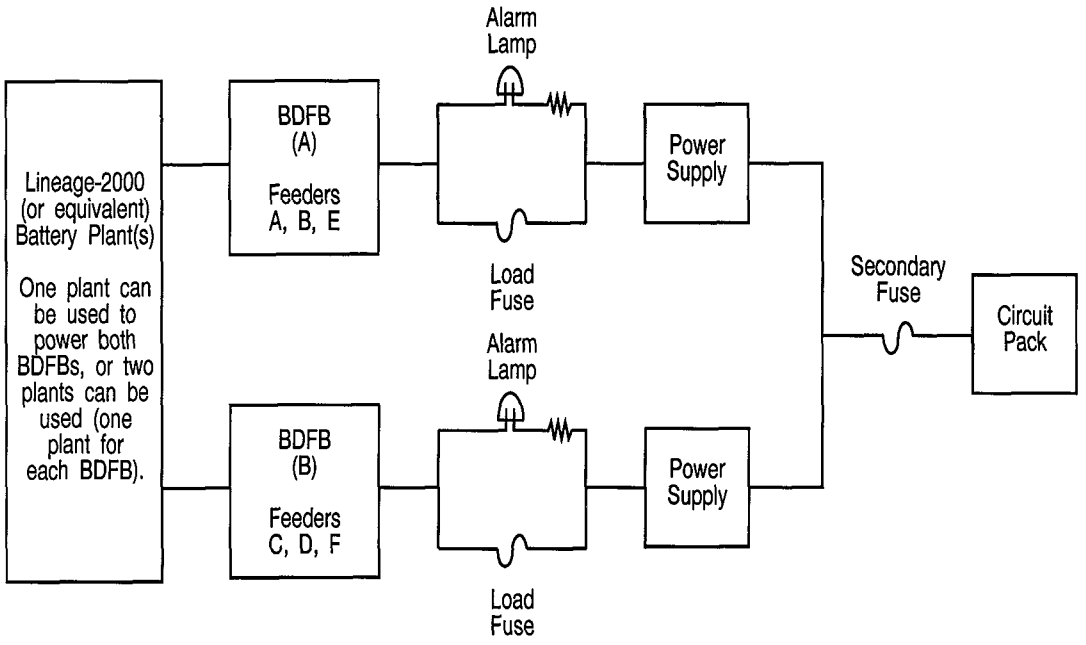



Figure 7-6. **Duplex Power Fuse Interconnection (Remote Complex)**

## Power Circuit Packs

The following sections describe the power circuit packs in the Switch Complex, OPEX Bay, and Interface Bays.

### Switch Complex

The three types of power circuit packs in the DACS IV-2000 Switch Complex are PWRE, PWRG, and PWRJ. These power circuit packs convert the -48 Vdc service from the BDFBs into voltage levels required by the system.

Fuse boards, along with the PWRJ power circuit packs for the SWIO, SWCS, HCC, and MEM Modules, are located in the Switch Power Modules. The PWRJ power circuit packs provide +5V and -5V power and are interconnected by a dedicated printed backplane. The power circuit pack outputs are placed on power buses connected to the SWIO, SWCS, HCC, and MEM Modules by local cables.

Two PWRG power circuit packs the Memory Storage Module provide +12V power to the PRI4 and SEC4, and +12V and -12V power to the ECI6 circuit packs. Fuses for these circuit packs are provided by fuse boards located in the Memory Storage Module.

### Optical Extension Bay

There are three types of power circuit packs in the Optical Extension (OPEX) Bay. These are PWRA, PWRE, and PWRF. These power circuit packs convert the -48V service from the BDFB(s) into levels usable by the system.

The Remote Unit Interface (RUI) Module has two dedicated PWRF power circuit packs (contained in the RUI Power Module), which provide power to the printed backplane power buses. The RUI Module circuit packs are connected to, and receive power, from these backplane power buses. Fuses for RUI Module circuit packs are provided by fuse boards located in the RUI Power Module.

Fuse boards, along with the PWRA power circuit packs for the OPEX Module, are located in the OPEX Power Module. The Auxiliary Power Module contains two PWRE circuit packs that provide power for the OPEX Module through fuses in the OPEX Power Module. These power circuit packs are interconnected by a dedicated printed backplane. The power circuit pack outputs are placed on power buses connected to the OPEX Module by local cables.

### Interface Bays

Each DS1, DS3, or STS1 Interface Module contains two PWRE circuit packs. These circuit packs provide +5V power to the module backplane power buses and to the Interface Module circuit packs. Each circuit pack is fused internally and draws power from the power buses.

## Fuses

### Switch Complex and Collocated Interface Bays

Tables 7-1 and 7-2 relate DACS IV-2000 Switch Complex and collocated interface bay fuses for the bays, interface modules, and shelves to their physical location on the Fuse and Alarm panels (see Figure 7-7 and 7-8) in the Switch and Fuse and Alarm Bays.

Tables 7-3, 7-4, and 7-5 relates the secondary fuses (see Figure 7-9) contained in the three Switch Power Modules to their associated circuit pack.

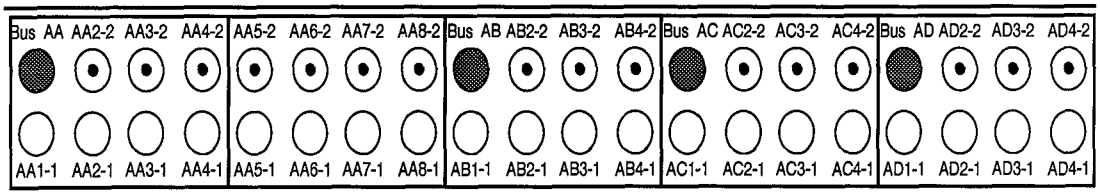
Figure 7-10 shows the location of the fuses in the Memory Storage Module fuses boards.

### Remote Complexes

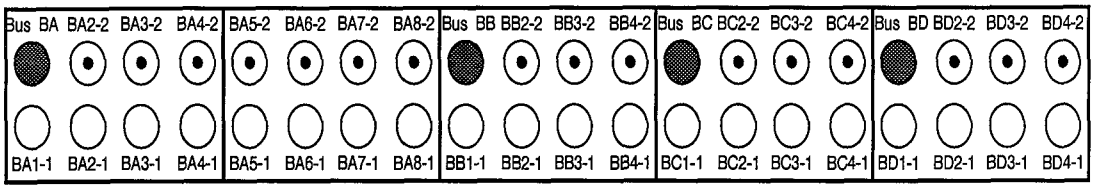
Figure 7-11 (standard power feed) and Figure 7-12 (duplex power feed) show the main fuse panel. Tables 7-6 and 7-7 relate DACS IV-2000 Remote Complex fuses for the power circuit packs in the OPEX Bay and interface modules to their physical location on the fuse and alarm panel at the top of the OPEX Bay.

Figure 7-13 shows the secondary fuse arrangement on the Remote Complex. Table 7-8 relates the secondary fuses contained in the OPEX Power Module to their associated circuit pack.

Figure 7-14 shows the location of the fuses in the RUI Power Module fuse boards FBF, FBG, FBH, and FBI. The associated equipment is panel stamped by each fuse.




**A. Fuse Panel in Bay Position 11**




**B. Fuse Panel in Bay Position 13**

**Note:** Fuses for all power buses come in pairs with the load fuse labeled with *-1* and the indicator fuse labeled with *-2*.

Figure 7-7. **Main Fuse Panels (Switch Bays)**

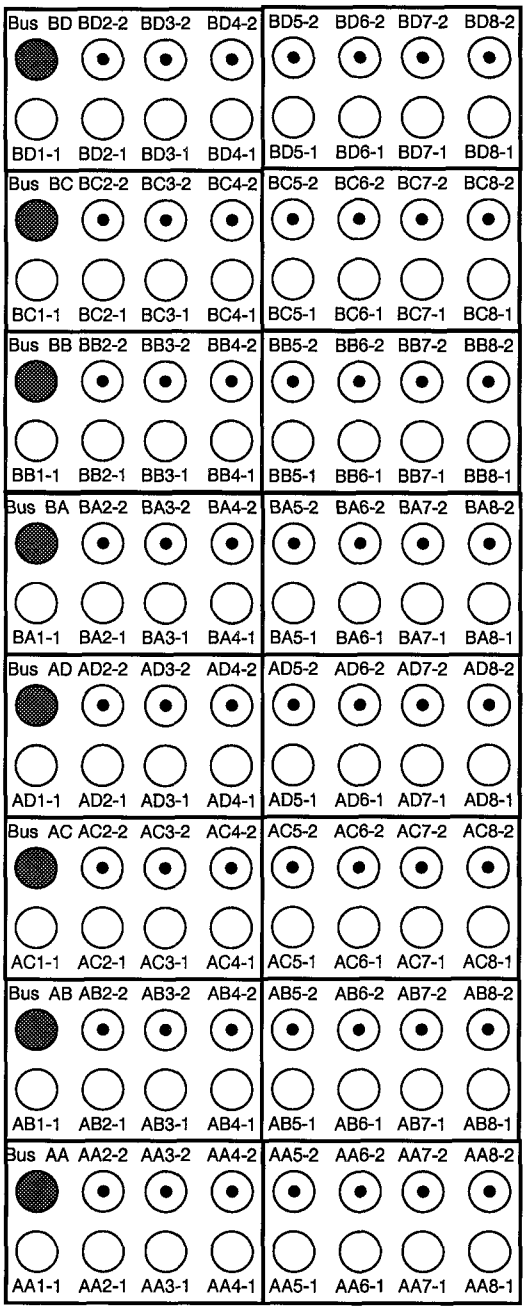
Table 7-1. **Fuse Chart for Switch Bays (Bays 11 and 13)**

**Switch Power Module PWRJ Circuit Packs**

| SW PWR Module | PWR Circuit Pack | | | | | |
|---|---|---|---|---|---|---|
| | PWRJ-1 | PWRJ-2 | PWRJ-3 | PWRJ-4 | PWRJ-5 | PWRJ-6 |
| 3 | AD2 | BD2 | AD3 | BD3 | AD4 | BD4 |
| 2 | AC2 | BC2 | AC3 | BC3 | AC4 | BC4 |
| 1 | AB2 | BB2 | AB3 | BB3 | AB4 | BB4 |

| MEM Module PWRG Circuit Packs | | Fan Assemblies | | |
|---|---|---|---|---|
| PWR Circuit Pack | Fuse | Bay | Main | Auxiliary |
| PWRG-1 | AA2 | 11 | AA4 | BA4 |
| PWRG-2 | BA2 | 12 | AA6 | BA6 |
| | | 13 | AA5 | BA5 |

**Note:** All load fuses for the PWRJ circuit packs are 20 A and load fuses for PWRG circuit packs and fan assemblies are 10 A. All indicator fuses are 0.5 A.



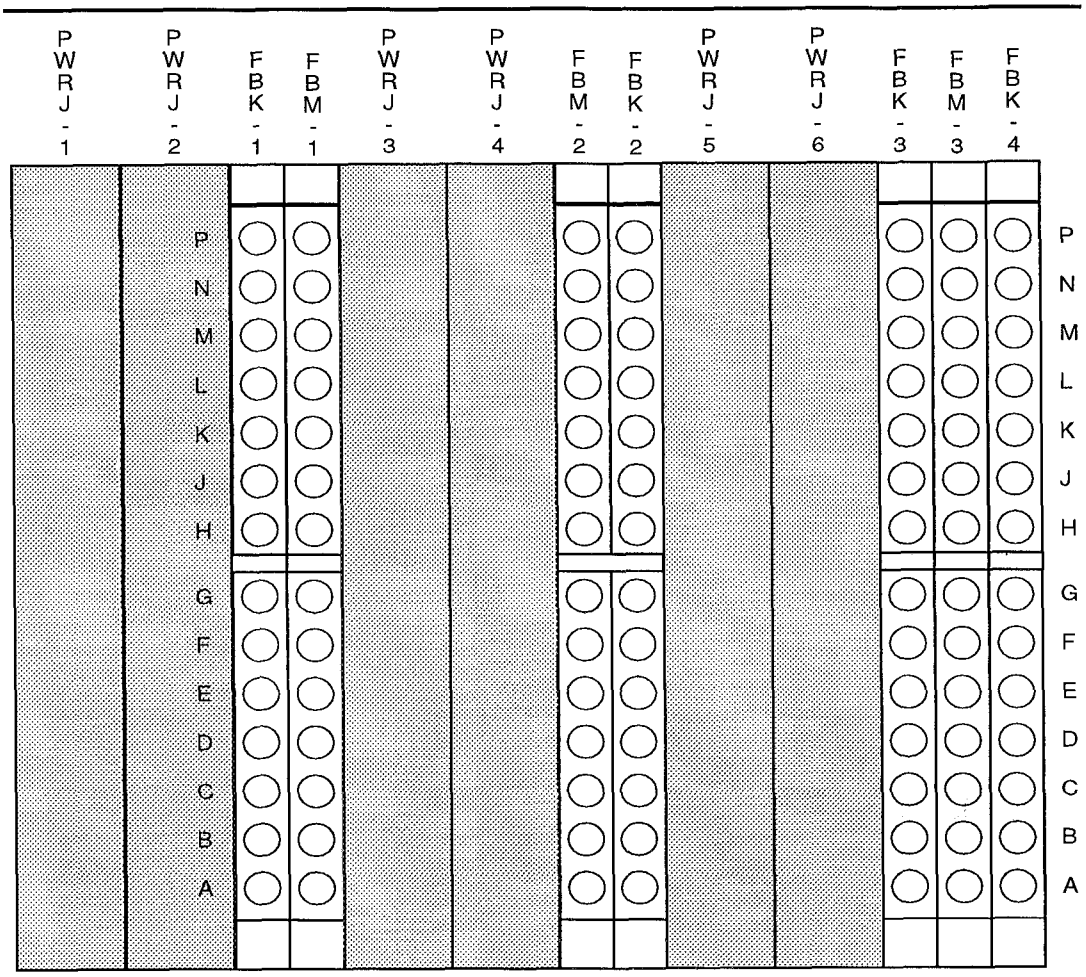

**Note:** Fuses for all power buses come in pairs with the load fuse labeled with *-1* and the indicator fuse labeled with *-2*.

Figure 7-8. **Main Fuse Panel (Fuse and Alarm Bays)**

Table 7-2. **Fuse Chart for Fuse and Alarm Bays (Bays 5, 10, 14, and 19)**

| Shelf | PWR Circuit Pack | Fuse Panel in Bay 5 | | | | Fuse Panel in Bay 10 | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bay 1 | Bay 2 | Bay 3 | Bay 4 | Bay 6 | Bay 7 | Bay 8 | Bay 9 |
| 4 | PWRE-2 | BD2 | BC3 | BD4 | BC5 | BD2 | BC3 | BD4 | BC5 |
| | PWRE-1 | AD2 | AC3 | AD4 | AC5 | AD2 | AC3 | AD4 | AC5 |
| 3 | PWRE-2 | BC2 | BD3 | BC4 | BD5 | BC2 | BD3 | BC4 | BD5 |
| | PWRE-1 | AC2 | AD3 | AC4 | AD5 | AC2 | AD3 | AC4 | AD5 |
| 2 | PWRE-2 | BB2 | BA3 | BB4 | BA5 | BB2 | BA3 | BB4 | BA5 |
| | PWRE-1 | AB2 | AA3 | AB4 | AA5 | AB2 | AA3 | AB4 | AA5 |
| 1 | PWRE-2 | BA2 | BB3 | BA4 | BB5 | BA2 | BB3 | BA4 | BB5 |
| | PWRE-1 | AA2 | AB3 | AA4 | AB5 | AA2 | AB3 | AA4 | AB5 |
| Fan | Main | AD6 | AC6 | AB6 | AA6 | AD6 | AC6 | AB6 | AA6 |
| | Auxiliary | BD6 | BC6 | BB6 | BA6 | BD6 | BC6 | BB6 | BA6 |
| Shelf | PWR Circuit Pack | Fuse Panel in Bay 14 | | | | Fuse Panel in Bay 19 | | | |
| | | Bay 15 | Bay 16 | Bay 17 | Bay 18 | Bay 20 | Bay 21 | Bay 22 | Bay 23 |
| 4 | PWRE-2 | BC5 | BD4 | BC3 | BD2 | BC5 | BD4 | BC3 | BD2 |
| | PWRE-1 | AC5 | AD4 | AC3 | AD2 | AC5 | AD4 | AC3 | AD2 |
| 3 | PWRE-2 | BD5 | BC4 | BD3 | BC2 | BD5 | BC4 | BD3 | BC2 |
| | PWRE-1 | AD5 | AC4 | AD3 | AC2 | AD5 | AC4 | AD3 | AC2 |
| 2 | PWRE-2 | BA5 | BB4 | BA3 | BB2 | BA5 | BB4 | BA3 | BB2 |
| | PWRE-1 | AA5 | AB4 | AA3 | AB2 | AA5 | AB4 | AA3 | AB2 |
| 1 | PWRE-2 | BB5 | BA4 | BB3 | BA2 | BB5 | BA4 | BB3 | BA2 |
| | PWRE-1 | AB5 | AA4 | AB3 | AA2 | AB5 | AA4 | AB3 | AA2 |
| Fan | Main | AA6 | AB6 | AC6 | AD6 | AA6 | AB6 | AC6 | AD6 |
| | Auxiliary | BA6 | BB6 | BC6 | BD6 | BA6 | BB6 | BC6 | BD6 |

**Note.** All load fuses are 10 A and all indicator fuses are 0.5 A.




**Note:** A blown fuse is indicated by a lit red LED.

Figure 7-9. **Switch Power Module Secondary Fuses (FBK and FBM)**

Table 7-3. **Secondary Fuse Chart for SW PWR MOD 1 (Bottom of Bay 12)**

| Location | Type 77H (4A), Type 77J (7.5A), and Type 77E (15A) Fuses for +5V Supply | | | |
|---|---|---|---|---|
| | FBK-1 | FBK-2 | FBK-3 | FBK-4 |
| P | SWIO-1-14 (77J) | PWRJ-1-1† (SNSEPAX) | NC (77J) | NC (77E) |
| N | SWIO-1-13 (77J) | PWRJ-1-2† (SNSEPBX) | NC (77J) | NC (77H) |
| M | SWIO-1-12 (77J) | SWIO-1-16 (77J) | SWIO-3-16 (77J) | +5V STPNL‡ (77H |
| L | SWIO-1-11 (77J) | SWIO-1-15 (77J) | SWIO-3-15 (77J) | +5V LED* (77H) |
| K | SWIO-1-10 (77J) | +5V SYNC-0 (77J) | SWIO-3-14 (77J) | MTC-0-2 (77J) |
| J | SWIO-1-9 (77J) | NC (77J) | SWIO-3-13 (77J) | MTC-0-1 (77J) |
| H | SWIO-1-8 (77J) | NC (77J) | SWIO-3-12 (77J) | UI-0 (77E) |
| G | SWIO-1-7 (77J) | NC (77J) | SWIO-3-11 (77J) | SCI-0-2 (77E) |
| F | SWIO-1-6 (77J) | SWIO-3-6 (77J) | SWIO-3-10 (77J) | SCI-0-1 (77E) |
| E | SWIO-1-5 (77J) | SWIO-3-5 (77J) | SWIO-3-9 (77J) | CPU-0 (77J) |
| D | SWIO-1-4 (77J) | SWIO-3-4 (77J) | SWIO-3-8 (77J) | SSC-0 (77J) |
| C | SWIO-1-3 (77J) | SWIO-3-3 (77J) | SWIO-3-7 (77J) | ECI-1 (77E) |
| B | SWIO-1-2 (77J) | SWIO-3-2 (77J) | NC (77J) | PWRJ-1-6† (SNSEPBZ) |
| A | SWIO-1-1 (77J) | SWIO-3-1 (77J) | NC (77J) | PWRJ-1-5† (SNSEPAZ) |

| Location | Type 78H (4A) Fuses for -5V Supply | | |
|---|---|---|---|
| | FBM-1 | FBM-2 | FBM-3 |
| P | SWIO-1-14 (78H) | NC (78H) | NC (78H) |
| N | SWIO-1-13 (78H) | NC (78H) | NC (78H) |
| M | SWIO-1-12 (78H) | SWIO-1-16 (78H) | SWIO-3-16 (78H) |
| L | SWIO-1-11 (78H) | SWIO-1-15 (78H) | SWIO-3-15 (78H) |
| K | SWIO-1-10 (78H) | -5V SYNC-0 (78H) | SWIO-3-14 (78H) |
| J | SWIO-1-9 (78H) | NC (78H) | SWIO-3-13 (78H) |
| H | SWIO-1-8 (78H) | NC (78H) | SWIO-3-12 (78H) |
| G | SWIO-1-7 (78H) | NC (78H) | SWIO-3-11 (78H) |
| F | SWIO-1-6 (78H) | SWIO-3-6 (78H) | SWIO-3-10 (78H) |
| E | SWIO-1-5 (78H) | SWIO-3-5 (78H) | SWIO-3-9 (78H) |
| D | SWIO-1-4 (78H) | SWIO-3-4 (78H) | SWIO-3-8 (78H) |
| C | SWIO-1-3 (78H) | SWIO-3-3 (78H) | SWIO-3-7 (78H) |
| B | SWIO-1-2 (78H) | SWIO-3-2 (78H) | PWRJ-1-4† (SNSEPBY) |
| A | SWIO-1-1 (78H) | SWIO-3-1 (78H) | PWRJ-1-3† (SNSEPAY) |

* - Provides fused power to LEDs of CC-0 circuit packs
† - Power sensory strap (does not carry load voltages, only sensory voltages). These straps must not be extracted. The sensory straps are provided by a Type 77H fuse.
‡ - CC-0 status panel fuse
NC - Not Connected (Spare)

Table 7-4. **Secondary Fuse Chart for SW PWR MOD 2 (Middle of Bay 12)**

| Location | Type 77H (4A) and Type 77J (7.5A) Fuses for +5V Supply | | | |
|---|---|---|---|---|
| | **FBK-1** | **FBK-2** | **FBK-3** | **FBK-4** |
| P | SWCS-1-13 (77J) | PWRJ-2-1† (SNSEPAX) | PRI-1 (77H) | NC (77J) |
| N | SWCS-1-12 (77J) | PWRJ-2-2† (SNSEPBZ) | SEC (77H) | NC (77J) |
| M | SWCS-1-11 (77J) | SWCS-1-16 (77J) | NC (77H) | NC (77J) |
| L | SWCS-1-10 (77J) | SWCS-1-15 (77J) | SWCS-2-16 (77J) | NC (77J) |
| K | SWCS-1-9 (77J) | SWCS-1-14 (77J) | SWCS-2-15 (77J) | NC (77J) |
| J | SWCS-1-8 (77J) | NC (77H) | SWCS-2-14 (77J) | NC (77J) |
| H | SWCS-1-7 (77J) | SWCS-2-7 (77J) | SWCS-2-13 (77J) | NC (77J) |
| G | SWCS-1-6 (77J) | SWCS-2-6 (77J) | SWCS-2-12 (77J) | NC (77J) |
| F | SWCS-1-5 (77J) | SWCS-2-5 (77J) | SWCS-2-11 (77J) | NC (77J) |
| E | SWCS-1-4 (77J) | SWCS-2-4 (77J) | SWCS-2-10 (77J) | NC (77J) |
| D | SWCS-1-3 (77J) | SWCS-2-3 (77J) | SWCS-2-9 (77J) | NC (77H) |
| C | SWCS-1-2 (77J) | SWCS-2-2 (77J) | SWCS-2-8 (77J) | NC (77H) |
| B | SWCS-1-1 (77J) | SWCS-2-1 (77J) | +5V LED* (77H) | PWRJ-2-6† (SNSEPBZ) |
| A | CLKGN-0 (77H) | CLKGN-1 (77H) | PRI-2 (77H) | PWRJ-2-5† (SNSEPAZ) |

| Location | Type 78H (4A) and Type 78E (15A) Fuses for -5V Supply | | |
|---|---|---|---|
| | **FBM-1** | **FBM-2** | **FBM-3** |
| P | SWCS-1-13 (78H) | NC (78H) | NC (78H) |
| N | SWCS-1-12 (78H) | NC (78H) | NC (78H) |
| M | SWCS-1-11 (78H) | SWCS-1-16 (78H) | NC (78H) |
| L | SWCS-1-10 (78H) | SWCS-1-15 (78H) | SWCS-2-16 (78H) |
| K | SWCS-1-9 (78H) | SWCS-1-14 (78H) | SWCS-2-15 (78H) |
| J | SWCS-1-8 (78H) | NC (78H) | SWCS-2-14 (78H) |
| H | SWCS-1-7 (78H) | SWCS-2-7 (78H) | SWCS-2-13 (78H) |
| G | SWCS-1-6 (78H) | SWCS-2-6 (78H) | SWCS-2-12 (78H) |
| F | SWCS-1-5 (78H) | SWCS-2-5 (78H) | SWCS-2-11 (78H) |
| E | SWCS-1-4 (78H) | SWCS-2-4 (78H) | SWCS-2-10 (78H) |
| D | SWCS-1-3 (78H) | SWCS-2-3 (78H) | SWCS-2-9 (78H) |
| C | SWCS-1-2 (78H) | SWCS-2-2 (78H) | SWCS-2-8 (78H) |
| B | SWCS-1-1 (78H) | SWCS-2-1 (78H) | PWRJ-2-4† (SNSEPBY) |
| A | CLKGN-0 (78E) | CLKGN-1 (78E) | PWRJ-2-3† (SNSEPAY |

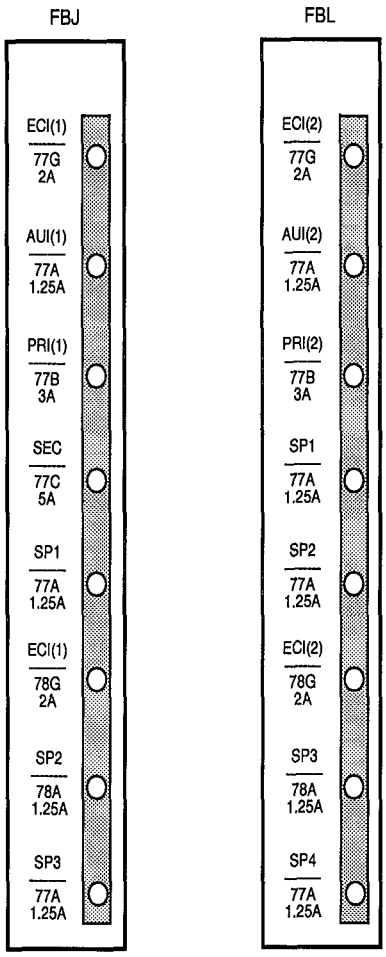
* - Provides fused power to LEDs of Memory Module circuit packs
† - Power sensory strap (does not carry load voltages, only sensory voltages). These straps must not be extracted. The sensory straps are provided by a Type 77H fuse.
NC - Not Connected (Spare)

Table 7-5. **Secondary Fuse Chart for SW PWR MOD 3 (Top of Bay 12)**

| Location | Type 77H (4A), Type 77J (7.5A), and Type 77E (15A) Fuses for +5V Supply | | | |
|---|---|---|---|---|
| | **FBK-1** | **FBK-2** | **FBK-3** | **FBK-4** |
| P | SWIO-2-14 (77J) | PWRJ-3-1† (SNSEPAX) | NC (77J) | NC (77E) |
| N | SWIO-2-13 (77J) | PWRJ-3-2† (SNSEPBZ) | NC (77J) | NC (77H) |
| M | SWIO-2-12 (77J) | SWIO-2-16 (77J) | SWIO-4-16 (77J) | +5V STPNL‡ (77H) |
| L | SWIO-2-11 (77J) | SWIO-2-15 (77J) | SWIO-4-15 (77J) | +5V LED* (77H) |
| K | SWIO-2-10 (77J) | +5V SYNC-1 (77J) | SWIO-4-14 (77J) | MTC-1-2 (77J) |
| J | SWIO-2-9 (77J) | NC (77J) | SWIO-4-13 (77J) | MTC-1-1 (77J) |
| H | SWIO-2-8 (77J) | NC (77J) | SWIO-4-12 (77J) | UI-1 (77E) |
| G | SWIO-2-7 (77J) | NC (77J) | SWIO-4-11 (77J) | SCI-1-2 (77E) |
| F | SWIO-2-6 (77J) | SWIO-4-6 (77J) | SWIO-4-10 (77J) | SCI-1-1 (77E) |
| E | SWIO-2-5 (77J) | SWIO-4-5 (77J) | SWIO-4-9 (77J) | CPU-1 (77J) |
| D | SWIO-2-4 (77J) | SWIO-4-4 (77J) | SWIO-4-8 (77J) | SSC-1 (77J) |
| C | SWIO-2-3 (77J) | SWIO-4-3 (77J) | SWIO-4-7 (77J) | ECI-2 (77E) |
| B | SWIO-2-2 (77J) | SWIO-4-2 (77J) | NC (77J) | PWRJ-3-6† (SNSEPBZ) |
| A | SWIO-2-1 (77J) | SWIO-4-1 (77J) | NC (77J) | PWRJ-3-5† (SNSEPAZ) |

| Location | Type 78H (4A) Fuses for -5V Supply | | |
|---|---|---|---|
| | **FBM-1** | **FBM-2** | **FBM-3** |
| P | SWIO-2-14 (78H) | NC (78H) | NC (78H) |
| N | SWIO-2-13 (78H) | NC (78H) | NC (78H) |
| M | SWIO-2-12 (78H) | SWIO-2-16 (78H) | SWIO-4-16 (78H) |
| L | SWIO-2-11 (78H) | SWIO-2-15 (78H) | SWIO-4-15 (78H) |
| K | SWIO-2-10 (78H) | -5V SYNC-1 (78H) | SWIO-4-14 (78H) |
| J | SWIO-2-9 (78H) | NC (78H) | SWIO-4-13 (78H) |
| H | SWIO-2-8 (78H) | NC (78H) | SWIO-4-12 (78H) |
| G | SWIO-2-7 (78H) | NC (78H) | SWIO-4-11 (78H) |
| F | SWIO-2-6 (78H) | SWIO-4-6 (78H) | SWIO-4-10 (78H) |
| E | SWIO-2-5 (78H) | SWIO-4-5 (78H) | SWIO-4-9 (78H) |
| D | SWIO-2-4 (78H) | SWIO-4-4 (78H) | SWIO-4-8 (78H) |
| C | SWIO-2-3 (78H) | SWIO-4-3 (78H) | SWIO-4-7 (78H) |
| B | SWIO-2-2 (78H) | SWIO-4-2 (78H) | PWRJ-3-4† (SNSEPBY) |
| A | SWIO-2-1 (78H) | SWIO-4-1 (78H) | PWRJ-3-3† (SNSEPAY |

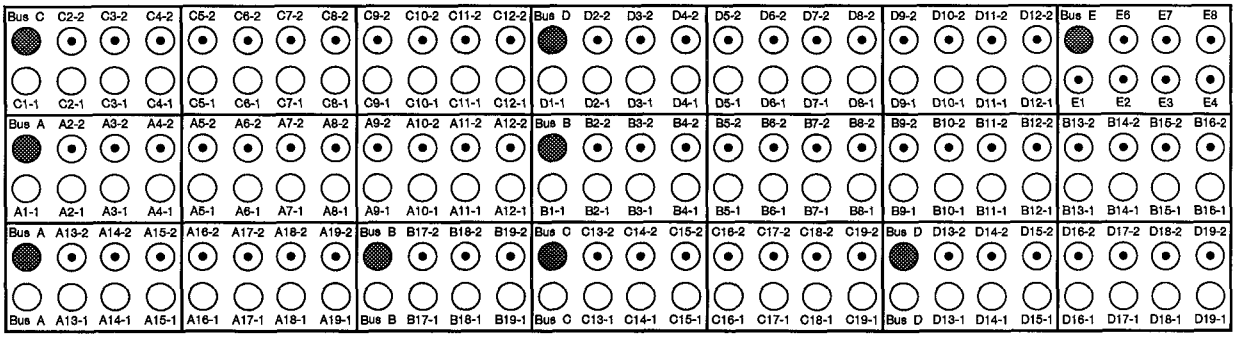
* - Provides fused power to LEDs of CC-1 circuit packs
† - Power sensory strap (does not carry load voltages, only sensory voltages). These straps must not be extracted.
‡ - CC-1 status panel fuse
NC - Not Connected (Spare)




**Notes:**

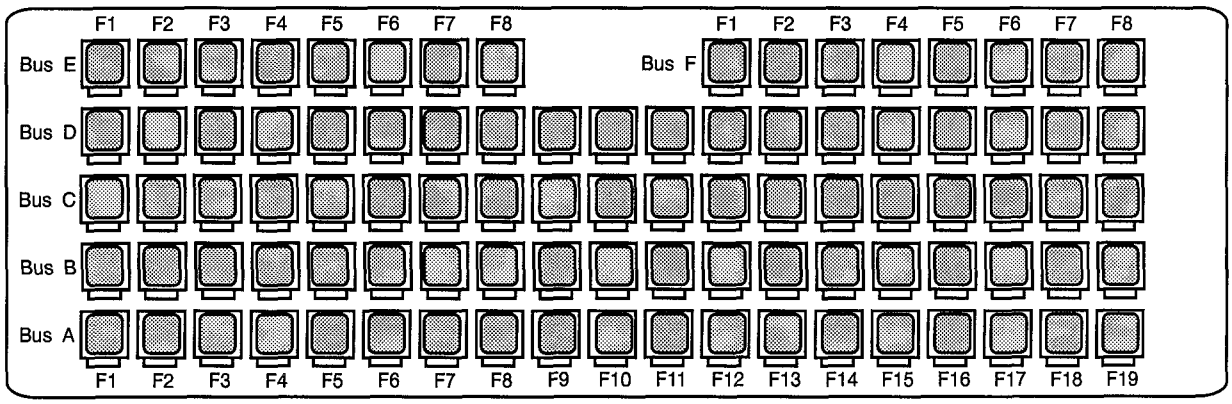
- Numbers in parentheses are circuit pack position numbers in the High-Capacity and Memory Storage Modules. Fuse ratings are listed below the circuit pack identifier and fuse type (77X or 78X label).
- The 2A fuses associated with the ECI circuit packs are for +12V and -12V supplied to the CILINKs. When these fuses blow, communication with the CILINKs can be interrupted.
- The 5A fuse for the SEC disk drive is for the +12V supply.
- The 3A fuses for the PRI disk drives are for the +12V supply.
- The labels SP1, SP2, SP3, and SP4 denote spare fuses that are not connected to any circuit pack.

Figure 7-10. **Memory Storage Module Fuses (FBJ and FBL)**




**Note:** Fuses for power buses A, B, C, and D come in pairs, the load fuse labeled "-1" and the indicator fuse labeled "-2". Fuses for power bus E are not paired (one load and one indicator); they are all indicator fuses.

Figure 7-11. **ED-2C940-30 Fuse and Alarm Panel (OPEX Bay)**




**Note:** Fuses A1, A2, B2, C1, C2, and D2 are rated at 12A, fuse D1 is rated at 2A, and all other fuses are rated at 10A. All fuses have a red alarm lamp to indicate failure. Fuse B1 is not connected.

Figure 7-12. **ED-9C114-30 Fuse and Alarm Panel (OPEX Bay)**

Table 7-6. **Fuse Chart Remote Complex Interface Bays (Bays 1-4 and 6-9)**

| Shelf | PWR Circuit Pack | Bay 1 | Bay 2 | Bay 3 | Bay 4 | Bay 6 | Bay 7 | Bay 8 | Bay 9 |
|---|---|---|---|---|---|---|---|---|---|
| **Standard Power (ED-2C940-30 Fuse Panel)** | | | | | | | | | |
| 4 | PWRE-2 | C17 | D14 | D4 | D10 | C12 | D6 | B15 | C19 |
| | PWRE-1 | A17 | C15 | B4 | C10 | B12 | B6 | C8 | A19 |
| 3 | PWRE-2 | D16 | D13 | C4 | B10 | D12 | C6 | B8 | D18 |
| | PWRE-1 | A16 | A14 | A4 | A10 | A12 | A6 | A8 | C18 |
| 2 | PWRE-2 | B18 | C14 | D3 | C9 | D11 | D5 | C7 | D19 |
| | PWRE-1 | A15 | B17 | C3 | B9 | B11 | C5 | B7 | A18 |
| 1 | PWRE-2 | D15 | C13 | B3 | D9 | C11 | B5 | D7 | D17 |
| | PWRE-1 | C16 | A13 | A3 | A9 | A11 | A5 | A7 | B19 |
| Fan | Main | — | A16 | B18 | A17 | C19 | D17 | D19 | — |
| | Auxiliary | — | D16 | D15 | C17 | C19 | D17 | D19 | — |
| **Note:** All load fuses are 10A and all indicator fuses are 0.5A. | | | | | | | | | |
| **Duplex Power (ED-9C114-30 Fuse Panel)** | | | | | | | | | |
| 4 | PWRE-2 | F4 | D14 | D4 | D10 | D12 | D6 | D17 | F8 |
| | PWRE-1 | E4 | B14 | B4 | B10 | B12 | B6 | B8 | E8 |
| 3 | PWRE-2 | F3 | C14 | C4 | C10 | C12 | C6 | C8 | F7 |
| | PWRE-1 | E3 | A14 | A4 | A10 | A12 | A6 | A8 | E7 |
| 2 | PWRE-2 | D15 | D13 | D3 | D9 | D11 | D5 | D7 | D18 |
| | PWRE-1 | B15 | B13 | B3 | B9 | B11 | B5 | B7 | B18 |
| 1 | PWRE-2 | F2 | C13 | C3 | C9 | C11 | C5 | C7 | F6 |
| | PWRE-1 | E2 | A13 | A3 | A9 | A11 | A5 | A7 | E6 |
| Fan | Main | E1 | A15 | A16 | B16 | B19 | A19 | A18 | E5 |
| | Auxiliary | F1 | C15 | C16 | D16 | D19 | C19 | C18 | F5 |
| **Note:** All fuses are 10A with a red alarm lamp to indicate failure. | | | | | | | | | |

Table 7-7. **Fuse Chart OPEX Bay (Bay 5)**

**Standard Power (ED-2C940-30 Fuse Panel)**

| Auxiliary Power PWRE | | OPEX Power PWRA | | | | Fan Assembly | |
|---|---|---|---|---|---|---|---|
| 1 | 2 | 1 | 2 | 3 | 4 | Main | Auxiliary |
| B14 | D8 | A2 | B2 | C2 | D2 | E6 | B13-2 |

**Note:** Fuses A2-1, B2-1, C2-1, and D2-1 are 12A and fuses B14-1 and D8-1 are 10A. Fuses A2-2, B2-2, B14-2, C2-2, D2-2, and D8-2 (indicator fuses) are 0.5A. The fan assembly fuses E6 and B13-2 are indicator fuses rated at 5A.

**Duplex Power (ED-9C114-30 Fuse Panel)**

| Auxiliary Power PWRE | | OPEX Power PWRA | | | | Fan Assembly | |
|---|---|---|---|---|---|---|---|
| 1 | 2 | 1 | 2 | 3 | 4 | Main | Auxiliary |
| B14 | D8 | A2 | B2 | C2 | D2 | A17 | C17 |

| RUI Power Module PWRF Circuit Packs | | Header Designation Aseembly Fuse |
|---|---|---|
| PWR Circuit Pack | Fuse | |
| PWRF-1 | A1 | D1 |
| PWRF-2 | C1 | |

**Note:** Fuses A1, A2, B2, C1, C2, and D2 are 12A, fuses B14 and D8 are 10A, fuses A17 and C17 are 5A, and fuse D1 is 2A. All fuses have a red alarm lamp to indicate failure.

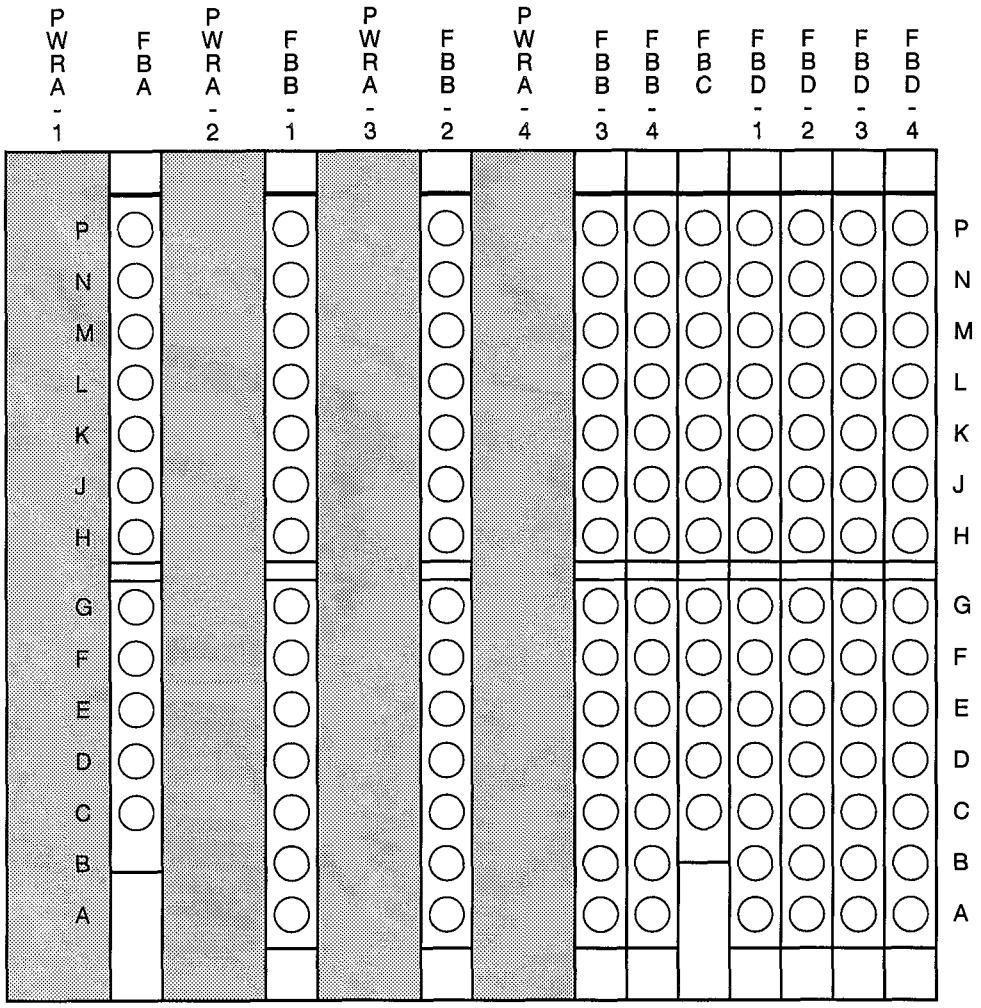
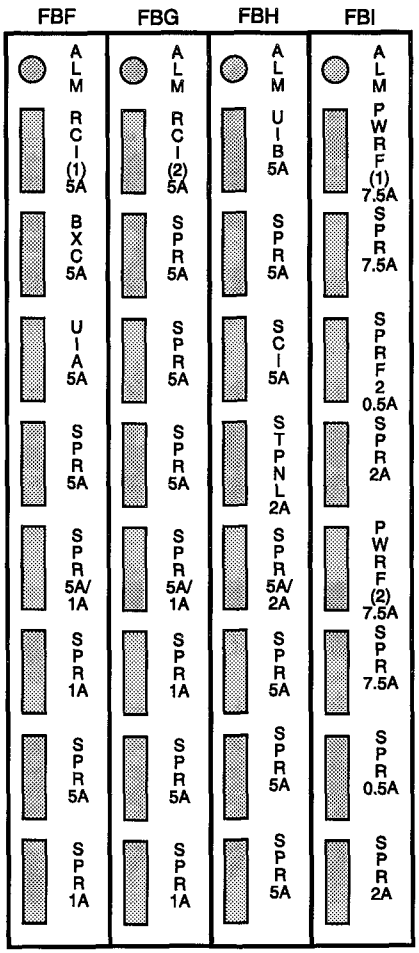



Figure 7-13. **OPEX Power Module Secondary Fuses (FBA, FBB, FBC, and FBD)**

Table 7-8. **Secondary Fuse Chart for Remote Complex**

| Location * | Type 77D (10A) Fuse for +5V Supply | | | | |
|---|---|---|---|---|---|
| | **FBA** | **FBB-1** | **FBB-2** | **FBB-3** | **FBB-4** |
| P | OPEX-11 | NA | NA | OPEX-21 | NA |
| N | OPEX-10 | NA | NA | OPEX-20 | NA |
| M | OPEX-9 | NA | NA | OPEX-19 | OPEX-32 |
| L | NA | NA | NA | OPEX-18 | OPEX-31 |
| K | OPEX-8 | NA | NA | OPEX-17 | OPEX-30 |
| J | OPEX-7 | NA | NA | NA | OPEX-29 |
| H | OPEX-6 | NA | NA | NA | OPEX-28 |
| G | OPEX-5 | NA | NA | NA | OPEX-27 |
| F | OPEX-4 | NA | NA | NA | OPEX-26 |
| E | OPEX-3 | OPEX-16 | NA | NA | OPEX-25 |
| D | OPEX-2 | OPEX-15 | NA | NA | CLKGN |
| C | OPEX-1 | OPEX-14 | NA | NA | OPEX-24 |
| B | - | OPEX-13 | NA | NA | OPEX-23 |
| A | - | OPEX-12 | NA | NA | OPEX-22 |
| **Location** | **Type 78J (7.5A) Fuse for -5V Supply** | | | | |
| | **FBC** | **FBD-1** | **FBD-2** | **FBD-3** | **FBD-4** |
| P | OPEX-11 | NA | NA | OPEX-21 | NA |
| N | OPEX-10 | NA | NA | OPEX-20 | NA |
| M | OPEX-9 | NA | NA | OPEX-19 | OPEX-32 |
| L | NA | NA | NA | OPEX-18 | OPEX-31 |
| K | OPEX-8 | NA | NA | OPEX-17 | OPEX-30 |
| J | OPEX-7 | NA | NA | NA | OPEX-29 |
| H | OPEX-6 | NA | NA | NA | OPEX-28 |
| G | OPEX-5 | NA | NA | NA | OPEX-27 |
| F | OPEX-4 | NA | NA | NA | OPEX-26 |
| E | OPEX-3 | OPEX-16 | NA | NA | OPEX-25 |
| D | OPEX-2 | OPEX-15 | NA | NA | CLKGN |
| C | OPEX-1 | OPEX-14 | NA | NA | OPEX-24 |
| B | - | OPEX-13 | NA | NA | OPEX-23 |
| A | - | OPEX-12 | NA | NA | OPEX-22 |

OPEX circuit pack physical locations are mapped into software as follows OPEX-{1-16} to OPEX-{1,3}-{1-16} and OPEX-{17-32} to OPEX-{2,4}-{1-16}




**Notes:**

- Numbers in parentheses are circuit pack position numbers in the High Capacity and Memory Storage Modules. Fuse ratings are listed below the circuit pack identifier and fuse type (77X or 78X label).
- The 2 amp fuses associated with the ECI circuit packs are for +12V and -12V supplied to the CILINKs. When these fuses blow, communication with the CILINKs can be interrupted.
- The 5A fuse for the SEC disk drive is for the +12V supply.
- The 3A fuses for the PRI disk drives are for the +12V supply.
- The labels SP1, SP2, SP3, and SP4 denote spare fuses that are not connected to any circuit pack.

Figure 7-14. **RUI Power Module Fuses (FBF, FBG, FBH, and FBI)**

# User Interfaces

# 8

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# Contents

# User Interfaces

# 8

The DACS IV-2000 provides user interfaces that allow you to issue commands to control system operations. This same user interface provides a mechanism that delivers messages regarding changes in system status.

## Commands and Messages

The DACS IV-2000 supports a message set (previously called Message Set 2[1]) that is compatible with Transaction Language (TL)1, Issue 4. This message set provides alarm, provisioning, administration, and maintenance (including test access and performance monitoring) commands and messages. This message set also provides support for communication with Bellcore's Operations Systems/ Intelligent Network Elements (OPS/INE) and Network Monitoring and Analysis (NMA) OSs.

The format of the DACS IV-2000 commands and messages follows the CCITT MML Standards and Recommendations from Bellcore. The dialog procedure used to enter commands follows the methodology given in Bellcore TR-TSY-000824.

1. Message Set 1 is not supported for Release 3.0 and later.

Messages can be issued either in response to a command (manual response) or to report a change in the state of the system due to autonomous actions (autonomous messages). Manual responses fall into two categories:

- Normal responses — indicating completion of a command, including data associated with the completion of the command.
- Error responses — indicating that the command was not successfully completed, including the reason for denial.

Messages have two formats, as follows:

- Human-machine — provides information over the administrative links that craft personnel can interpret.
- Machine-machine — provides additional parsable information that can be used by operations systems to further clarify and supplement information provided by the human-machine messages.

## Dialog Mode

Associated with each user (User ID) in the DACS IV-2000 is a parameter called dialog mode. The value of this parameter determines whether a particular session with the system is handled as human-machine or machine-machine. The dialog modes of operation are:

- MENU/prompt mode — provides the human-machine operation. Users enter this mode by typing a question mark at the command prompt (<). The menu/prompt mode provides three menu levels (called Activity Menus) that allow users to select an activity from the first (and possibly second) menu level and a command (verb-modifier) from the second (or possibly third) level. Figure 8-1 shows the basic menu/prompt mode structure. Details of the human-machine interactions and Activity Menus are given in Appendix B of the *DACS IV-2000 (512) Release 5.0 Commands and Messages* manual (AT&T 365-340-902).
- COMMAND-line mode — provides the machine-machine operation. This mode can also be used by experienced users who have knowledge of the command structure. When using this mode, commands are selected and parameters entered within a single line [a backslash (\) followed by a carriage-return (<cr>) is considered a single line of input].

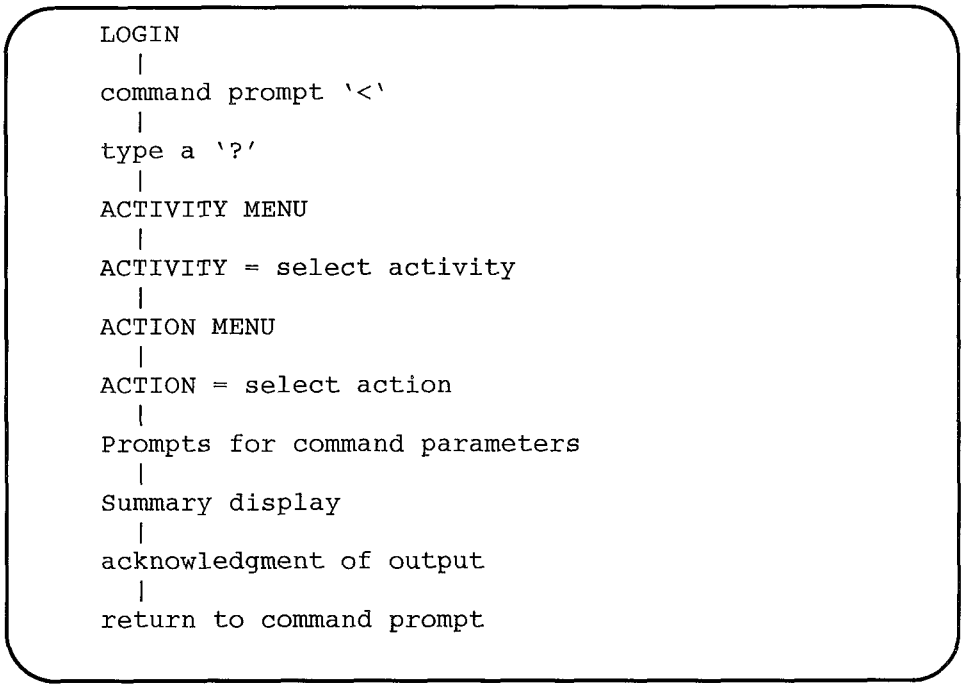



Figure 8-1. **Menu/Prompt Mode Structure**

## Message Screening

There are two message-screening parameters that users can set. One governs the amount of information that is sent over a link when no one is logged into the DACS IV-2000. The other governs the amount of information that is sent to a user who is logged into the DACS IV-2000. Each link and each user can be provisioned for a message screening value. These values need not be the same.

Virtual circuits associated with a link all share the same message screening value. The value of the message screening that is set for a user overrides the value set for the link when a user logs into the DACS IV-2000 (the link takes on the value set for the User ID). When a user logs into the DACS IV-2000 over a virtual circuit and the other virtual circuits of that link have no one logged in over them, the value of message screening for the user who logged on to the virtual circuit is used, and the other virtual circuits continue to use the value of message screening defined for the link.

The **ENT-SECU-USER** or **ED-SECU-USER** commands are used to set the user message screening values, and the **ED-PRMTR-LINK** command is used to set or change the link message screening value.

The message screening values and their definitions are as follows:

- INPUT — specifies that the User ID (UID) or link receives responses to its own input commands.
- AUTO — specifies that the UID or link receives responses to its own input commands and autonomous messages except `REPT DBCHG` messages due to manual command input.
- ALL — specifies that the UID or link receives responses to its own input messages, autonomous messages except `REPT DBCHG` messages due to manual command input, and responses to input commands from other UIDs.
- DBAUTO — specifies that the UID or link receives responses to its own input messages and autonomous messages including `REPT DBCHG` messages due to manual command input.
- DBALL — specifies that the UID or link receives responses to its own input messages, autonomous messages including `REPT DBCHG` messages due to manual command input, and responses to input commands from users (UIDs) links.

## Command Verification

Each UID is assigned a user type, either Human or Machine. This user type is checked when a user enters a command. If the command is potentially service-affecting or may prevent access to the DACS IV-2000 for an extended period of time and the user type is Human, the DACS IV-2000 displays a warning message and requests that the user verify the command. This warning message is displayed in both the Menu and Command dialog modes. The warning message is not displayed if the user type is Machine. The warning message is placed in the Review of Parameter Responses menu after the parameter responses and before the `EXECUTE COMMAND? [YES/NO/MODIFY]` prompt.

# System Addressing

Within the input commands, there are two levels of addressing. The first level consists of the target identifier (TID) parameter, and the second level is the entity identifier (EID) parameter.

## TID Addressing

The TID uniquely identifies the target DACS IV-2000. This parameter is set by the input command `ED-NE`. It can optionally be specified in any input command, and is always printed on all output messages. The 11-character CLLI[1] code is the recommended value for the TID. If the CLLI code for a DACS IV-2000 is not unique, the CLLI code can be augmented with additional characters for a total of 18 characters. If communications are point-to-point between the user and the DACS IV-2000, the TID is not necessary.

## EID Addressing

The EID identifies either equipment, facility, or link locations. For the most part, the equipment domain is used with command names ending with the `EQPT` modifier. The facility domain is used with command names ending with the `T1`, `T3`, `EC1`, or `VT1` modifier. The CILINK domain is used with command names ending in the `LINK` modifier. However, some command entries allow mixing of these domains.

## Equipment Addressing

An equipment domain address is a combination of a physical description and a logical address. The first component of the address is the physical description (SSC, SCI, etc.). If necessary, a hierarchic logical address is appended to the physical description (for example, `UC-16` identifies the unit controller in unit 16).

## Facility Addressing

Addressing within the facility domain also follows a hierarchic scheme, which is shown in Table 8-1. For VT1.5 ports or DS1 ports associated with an SMUX circuit pack, the user is provisioned (`ENT-SECU-USER` or `ED-SECU-USER` commands) to use one of two numbering schemes: DS1/VT1.5 port numbering or VT1.5 group numbering.

1. COMMON LANGUAGE is a registered trademark and CLEI, CLLI, CLCI, and CLFI are trademarks of Bell Communications Research, Inc.

Table 8-1. **EID Facility Addressing**

| Facility | Address DS1/DS3/ EC-1/VT1.5 Port Numbering {unit number}-{slot number}-{port number} | Address VT1.5 Group Numbering {unit number}-{slot number}-{group number}-{port number} |
|---|---|---|
| DS1 Interface Module DS1 Port | {1-64}-{1-8}-{1-28} | |
| DS1 Interface-P Module DS1 Port | {1-64}-{1-7}-{1-28} | |
| DS3 Interface-32 Module DS1 Port | {1-64}-{1-31}-{1-28} | |
| DS3 Interface-16 Module DS1 Port | {1-64}-{1-15}-{1-28} | |
| Enhanced DS3 Interface-16 Module DS1 Port | {1-64}-{1-15}-{1-28} | |
| DS3 Clear-Channel Interface-16 Module DS1 Port | {1-64}-{1-15}-{1-28} | |
| STS1 Interface-16 Module DS1 Port | {1-64}-{1-15}-{1-28} | {1-64}-{1-15}-{1-7}-{1-4} |
| DS3 Interface-32 Module DS3 Port | {1-64}-{1-31} | |
| DS3 Interface-16 Module DS3 Port | {1-64}-{1-15} | |
| Enhanced DS3 Interface-16 Module DS3 Port | {1-64}-{1-15} | |
| DS3 Clear-Channel Interface-16 Module DS3 Port | {1-64}-{1-15} | |
| STS1 Interface-16 Module DS3 Port | {1-64}-{1-15} | |
| STS1 Interface-16 Module VT1.5 Port | {1-64}-{1-15}-{1-28} | {1-64}-{1-15}-{1-7}-{1-4} |
| STS1 Interface-16 Module EC-1 Port | {1-64}-{1-15} | |

The DS1 Ports are all DS1 signals that enter the system, either as a DS1, a DS1 within a DS3, or as a DS1 within a VT1.5. The DS1 Interface Ports are the subset of DS1 Ports that enter the system as DS1 facilities. The VT1.5 Ports are tributaries of the EC-1 Ports. The DS3 Ports are DS3 facilities that enter the system. The EC-1 Ports are EC-1 facilities that enter the system. DS1, DS3, EC-1, and VT1.5 Ports can also be addressed by module name (for example, `UNIT-1`). DS1 ports can also be addressed by interface group name (for example, `DS1GRP-2`).

## DS1/DS3/EC-1/VT1.5 Port Numbering

All DS3, EC-1, and DS1 (not associated with SMUX circuit packs) ports must use the port numbering scheme. VT1.5 and DS1 (associated with SMUX circuit packs) ports can be addressed using port numbering when the user is provisioned for VT1.5 port numbering (three-part address). DS1/VT1.5 Port addressing has the form (DS3/EC-1 Ports have the same form except the port number is omitted):

{unit number}-{slot number}-{port number}

where:

- **Unit Number** — is the number of the interface module that supports the port.
- **Slot Number** (physical slot location occupied by a MUX, SMUX, or SWIF circuit pack) — is the DS3 or EC-1 equivalent within the interface module. The DS3 equivalent corresponds to either a MUX circuit pack that supports one DS3, or to a SWIF circuit pack that supports 28 DS1s. The EC-1 equivalent corresponds to the SMUX circuit pack that supports one STS-1. The range of numbers associated with these elements is related to the DACS IV-2000 architecture.
- **Port Number** (for DS1 Ports and VT1.5 Ports) — is one of the 28 DS1 port within the DS3/EC-1 equivalent or one of 28 VT1.5 ports within the EC-1 equivalent.

Leading zeroes are not permitted when addressing equipment and facilities in a parameter (for example, `MUX-01-05` and `16-07-12` are not valid addresses).

## VT1.5 Group Numbering

VT1.5 and DS1 (associated with SMUX circuit packs) ports can be addressed using VT1.5 group numbering when the user is provisioned for VT1.5 group numbering (four-part address). VT1.5 Group Numbering addressing has the form:

{unit number}-{slot number}-{group number} -{port number}

where:

- **Unit Number** — is the number of the interface module that supports the port.
- **Slot Number** (physical slot location occupied by an SMUX circuit pack) — is the EC-1 equivalent within the STS1 Interface-16 Module. The EC-1 equivalent corresponds to the SMUX circuit pack that supports one STS-1 signal. The range of numbers associated with these elements is related to the DACS IV-2000 architecture.

- **Group Number** — is one of the seven VT groups within the EC-1 equivalent.
- **Port Number** — is one of the four DS1/VT1.5 ports within the specified VT group.

Leading zeroes are not permitted when addressing equipment and facilities in a parameter (for example, `16-12-07-02` is not a valid address).

### Link Addressing

Addressing within the link domain consists of a single format:

```
CILINK-{1,2}-{1-8}
```

which indicates a physical link on the ECI circuit pack and is generically known as a communications interface link (CILINK).

## Security Interface

Access to the DACS IV-2000 is restricted to authorized users for security purposes through the security interface. The security interface consists of user login IDs and associated passwords, and user privilege codes. Input command priorities are established through the use of user priority levels.

### User ID Passwords

To allow access to the DACS IV-2000, the system administrator creates valid UIDs (logins) and their associated passwords. These UID/password pairs allow users to access the DACS IV-2000 to perform administrative, operational, provisioning, and maintenance functions.

Valid UIDs consist of one to ten characters. Allowable characters are letters (A-Z, a-z), decimal digits (0-9), and *special legal characters* (- . # % +). Valid passwords consist of six to eight characters. At least two of the characters must be non-alphabetic characters with at least one character being a *special legal character.* Password characters are letters (A-Z, a-z), decimal digits (0-9), and *special legal characters* (# % +). The first character of the password must be a letter.

The DACS IV-2000 allows the current set of UIDs and their associated passwords even if they do not adhere to the above rules. However, when creating new passwords, they must follow the above rules.

## User Privilege Codes

Restricting access to information stored in a DACS IV-2000 database to those who need access is an effective security strategy to preserve the integrity of the database. This strategy grants the smallest set of privileges necessary to perform tasks.

To assist in this restrictive access, UIDs are assigned User Privilege Codes. User Privilege Codes are made up of User Community Functional Categories (UCFC) and User Community Authorization Levels (UCAL) pairs. These components of security management are described in Appendix E of the *DACS IV-2000 Release 5.0 Commands and Messages* manual (AT&T 365-340-902).

## User/Superuser Priority Levels

The five levels of user login input commands priority (UCPL) are defined as: 5 (highest), 4, 3, 2, and 1 (lowest). There are no restrictions for assignment of priority levels to user logins; however, it is suggested the operation system support user logins that are provisioned for the highest priority level.

Only a superuser (UCFC/UCAL = S5) can change all parameters for all users. A user with a UCFC/UCAL of S1 can change the following parameters only: his own password, Message Screening, Dialogue Mode, and User Type. For a superuser, the Old Password field is checked against the current password only if it is given. If the superuser specifies the old password in the CHG-LGN command, that password must be validated. The last superuser cannot reduce the UCFC/UCAL below S5.

Characteristics of a superuser (UCFC/UCAL = S5) are as follows:

- The only user that can edit a user's UCFC/UCAL pair
- Must enter their password when changing their login; however, this is not necessary when changing other users' logins
- Has permission to create and delete a user login
- Can log out other users from a working session
- Is able to retrieve parameters associated with all user logins
- Can execute RTRV-SECU-AUD and DLT-SECU-AUD commands.

Passwords can be changed more than once in a login session. All changes to passwords take effect immediately. To change passwords you must use the password that you changed to, not the password that you logged in with. When you alter your own login parameters, the old password must be supplied. If the old password is used, even when optional, it is checked.

Non-superusers are able to retrieve privilege parameters associated with their own logins only.

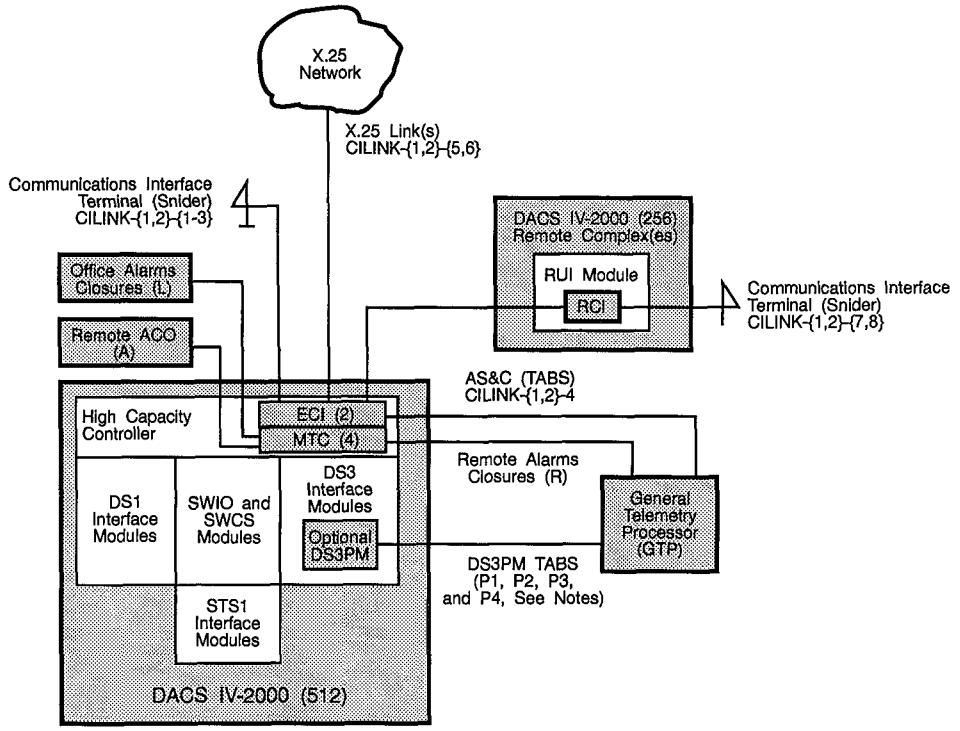
## Links

The DACS IV-2000 provides 16 administrative links (CILINKs) to interface with Operations Systems (OSs) using a X.25 network (CILINK-{1,2}-{5,6}) and communications interface terminals (CITs) using Snider protocol (CILINK-{1,2}-{1-3,7,8}). CILINK-{1,2}-{7,8} are used as CIT links at the Remote Complexes.

The administrative links are used to access all the features and functions of the system, both locally and remotely. It also provides alarm closures and a remote reset function to local and remote offices. In addition, a separate optional OS interface can be used to provide path performance monitoring information for DS3s that are provisioned with the C-bit parity format.

TABS links (CILINK-{1,2}-4) are provided for communications with a General Telemetry Processor (GTP). The system designates one ECI circuit pack as the master and the other ECI circuit pack as the slave (on a system reset ECI-1 is designated the master). For example, when using a GTP on a TABS link, the GTP must be connected to ECI-1 (CILINK-1-4) in the initial installation. ECI-1 becomes the slave only when it fails and is restored (`RST-EQPT` command) without resetting the frame. When ECI-1 fails, ECI-2 becomes the master and the GTP connection must be moved to ECI-2 (CILINK-2-4) if your office procedures do not require a system reset when ECI-1 fails; otherwise, the GTP connection remains on CILINK-1-4 and a system reset is performed after replacing ECI-1.

Figure 8-2 and Table 8-2 summarize the interfaces provided by the DACS IV-2000.




**Notes:**

1. One to four P links (collocated interface bays only).
2. Up to eight DS3PMs per link.
3. Up to 32 DS3PMs per DACS IV-2000 system.

Figure 8-2. **System Interfaces**

Table 8-2. **Link Interfaces**

| Interface (Figure 8-2) | Physical | Baud | Electrical | Functional |
|---|---|---|---|---|
| CILINK 1-1† and 2-1 | EIA-232-D | 1200, 2400, 4800, 9600, and 19200 Default: 9600* | EIA-232-D | Async. Snider |
| CILINK 1-2 and 2-2 | EIA-449 | 1200, 2400, 4800, and 9600 Default: 2400* | EIA-423 | Async. Snider |
| CILINK 1-3 and 2-3 | EIA-449 | 1200, 2400, 4800, 9600, and 19200 Default: 9600* | EIA-423 | Async. Snider |
| CILINK 1-4 and 2-4 | EIA-449 | 1200, 2400, 4800, and 9600 Default: 2400* | EIA-485 | TABS point-to-point AS&C |
| CILINK 1-5, 1-6, 2-5, and 2-6 | EIA-449 | 1200, 2400, 4800, and 9600 Default: 9600* | EIA-423 | Sync. X.25 or Async. Terminal Interface with external PAD |
| CILINK 1-7, 1-8, 2-7, and 2-8 | EIA-232-D | 1200, 2400, 4800, 9600, and 19200 Default: 9600* | EIA-232-D | Async. Snider |
| P1, P2, P3, and P4 (optional) | Connector | 2400 | RS-485 | TABS Async. multipoint DS3PM |
| Local Alarm Closures (L) | Wirewrap | - | Closures | Local alarms (Visual and Audible) |

Footnotes are at the end of this table.

Table continued on next page.

Table 8-2. **Link Interfaces (Continued)**

| Interface (Figure 8-2) | Physical | Baud | Electrical | Functional |
|---|---|---|---|---|
| Remote Alarm Closures (R) | Wirewrap | - | Closures | Remote alarms (GTP) |
| Remote ACO (A) | Wirewrap | - | Closures | Remote ACO |

**Notes:**

* When provisioning CILINKs, it is recommended that the baud rate default values be used.

† CILINK-1-1 can be hardware provisionable for a default of 1200 or 9600 baud.

1. All EIA-423 links are interoperable with EIA-232-D via the use of the suggested adapters. For Snider links DACS IV-2000-to-terminal communication, it is suggested the ED-2C646,G1 adapter be used. For Snider links DACS IV-2000-to-OS via modem communication, it is suggested the ED-2C646,G2 adapter be used.
2. Links 1-2 and 2-2 are electrically compatible with the EIA-232-D (see Note 1) standard up to 4800 baud. Links 1-3 and 2-3 are electrically compatible with the EIA-232-D standard up to 9600 baud. These links may operate with the EIA-232-D above these data rates; however, the 4-percent rise time specification of EIA-232-D is violated.
3. To supply internal timing for the X.25 links, the ED-2C646,G7 adapter must be used and the baud rate is fixed at 9600. All baud rates can be used with an external timing source.

Sixteen administrative links on two ECI6 circuit packs support the operations, administration, maintenance, and provisioning functions. They are:

- CILINKs 1-1 through 1-3, 1-7, 1-8, 2-1 through 2-3, 2-7, and 2-8 are asynchronous links (convertible to RS-232 with an optional passive adapter). CILINKs 1-1 and 2-1 supports the local communications interface terminal (CIT) for the switch complex and collocated interface bays, CILINKs 1-7, 2-7, 1-8, and 2-8 support the CIT for the remote complexes, and CILINKs 1-2, 1-3, 2-2, and 2-3 support remote terminals and OSs such as 2A Switching Control Center System (2ASCCS) or 2BSCCS using the SCCS AI (asynchronous interface, also called Snider) protocol. These Snider interfaces operate at 300, 1200, 2400, 4800, 9600, or 19200 (1-2, 2-1, 1-3, 2-3, 1-7, 2-7, 1-8, and 2-8 only) baud.
- CILINKs 1-4 and 2-4 can be provisioned as asynchronous TABS links operating at 2400 baud or Snider links.
- CILINKs 1-5, 1-6, 2-5, and 2-6 can be provisioned to use either the synchronous X.25 protocol or asynchronous Snider protocol with the addition of an external Packet Assembler and Disassembler (PAD) device. Each X.25 link supports CCITT MML on as many as four virtual circuits. The synchronous interfaces operate at up to 9600 baud as determined by the external devices.

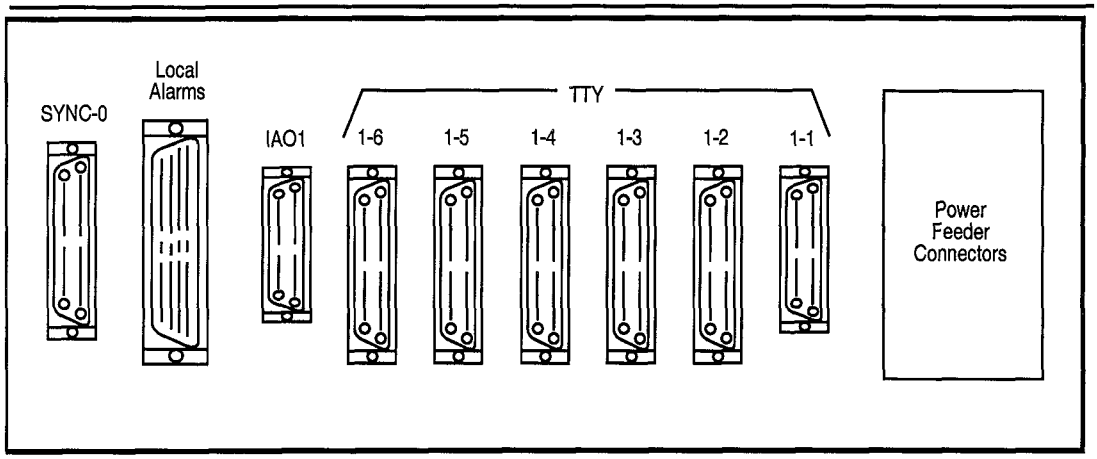
Two additional links (labelled IAO at the rear of the Switch Bays and LAN on the Switch Complex status panel) are for DACSlink connections.

All CILINKs support the message set (TL1, Issue 4) for communication with Bellcore's, Operations Systems/Intelligent Network Elements (OPS/INE) and Network Monitoring and Analysis (NMA) OSs.

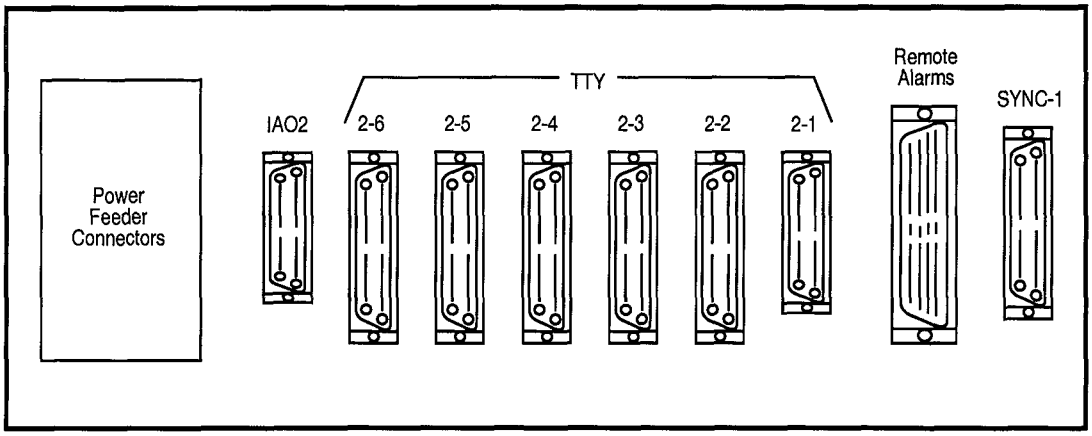
The optional DS3PM multipoint asynchronous interface (P1, P2, P3, and P4) (collocated interface bays only) operates at 2400 baud. A general telemetry processor (GTP) remote processor can be connected to these links and interfaced to a modem over an E2A or compatible data link to the telemetry OS. These links provide DS3 path performance data to telemetry-based OSs.

Figure 8-3 shows the location of the CILINK TTY connectors at the rear of the two Switch Bays (Bays 11 and 13) of the Switch Complex.

Figure 8-4 shows the location of the CILINK TTY connectors at the rear of the Remote Unit Interface Module of a Remote Complex.



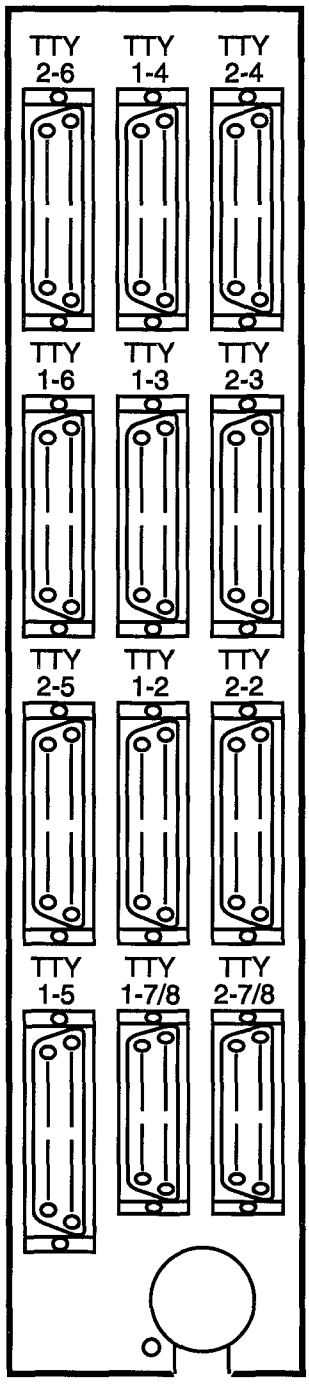

**A. Top Panel of Switch Bay in Bay Position 11**




**B. Top Panel of Switch Bay in Bay Position 13**

**Note:** TTY connectors IAO1 and IAO2 are used for DACSlink connections.

Figure 8-3. **CILINK, Alarms and Synchronizer Connectors at the Rear of the Switch Bays**




**Note:** Only the links labelled TTY 1-7/8 and TTY 2-7/8 are used. Links {1,2}-{2-6} are unused.

Figure 8-4. **CILINK Connectors at the Rear of the RUI Module**

## Indicators and Switches

All circuit packs (except version 1 Synchronizer, BXA, and BXC circuit packs) have a red LED indicator for trouble isolation. The LEDs flash on and off at one-second intervals on circuit packs that have input DS1, DS3, STS-1, and VT1.5 signal failures. The LEDs stay on for internal circuit pack failures. The normal LED condition is off. In addition to the LED alarm indication, `REPT ALM` messages are generated for all system circuit pack and facility failures.

Power circuit packs have green LEDs that indicate normal operation. They also have a red LED for trouble isolation as described above.

Switch Complex CLKGN circuit packs have green LEDs to indicate active CLKGN. All control complex circuit packs (CPU/MTC/SSC/SCI/UI) have green LEDs to indicate the on-line control complex.

The disk drives (PRI and SEC) have both green and red LEDs. The green LED indicates that the disk drive is operating and the red LED indicates that the disk has been manually removed from service or has failed.

The ECI circuit packs have green LEDs to indicate the ECI is in service.

The Switch Complex status panel (Figure 8-5) has seven equipment indicators. They are:

- CR (critical)— is red and signals a critical alarm condition.
- MJ (major) — is red and signals a major alarm condition.
- MN (minor) — is yellow and signals a minor alarm condition.
- ABN (abnormal) — reserved for future use.
- ACO — is green and shows that the audible alarms for the Switch Complex and collocated interface bays have been silenced (ACO switch activated).
- MC FAIL — is a red processor major alarm and signals a failure in the HCC module.
- FE (far end) — reserved for future use.

The Remote Complex status panel (Figure 8-6) has eight equipment indicators. They are:

- CRITICAL — is red and signals a critical alarm condition.
- MAJOR — is red and signals a major alarm condition.
- MINOR — is yellow and signals a minor alarm condition.
- ABNORMAL — reserved for future use.
- LOCAL ACO — is green and shows that the audible alarms for the Remote Complex have been silenced (ACO switch activated).

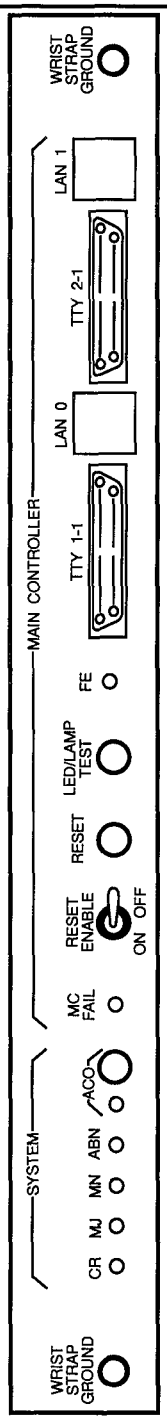



Figure 8-5. **Status Panel — Switch Complex**

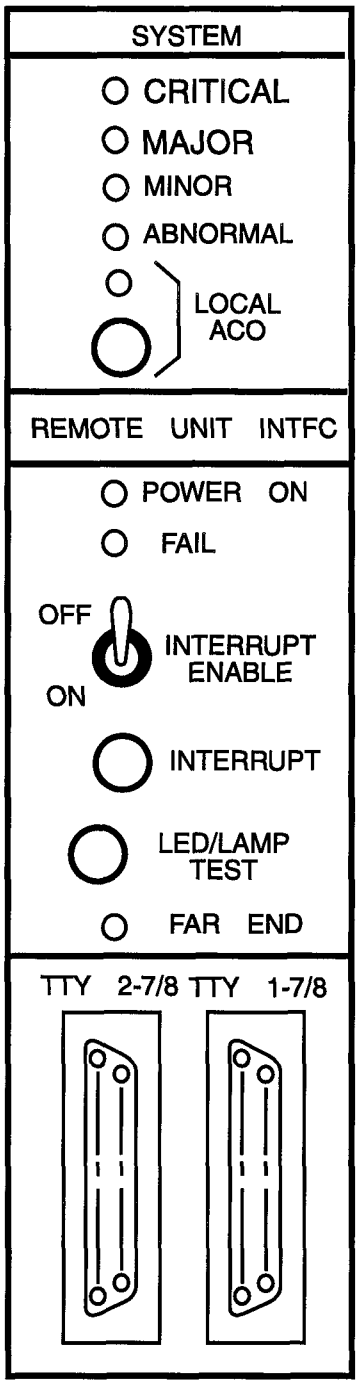



Figure 8-6. **Status Panel — Remote Complexes**

- POWER ON — is green and signals that power is present at the status panel.
- FAIL — is a red processor major alarm and signals a failure in the Remote Unit Interface (RUI) Module.
- FAR END — reserved for future use.

When the main controller (MC) is in the OOS-MCOND state and if the MTC circuit pack of the active control complex (CC) is extracted, the MJ and MC FAIL alarm LEDs on the status panel and the header designation assembly (HDA) light, and remain lit until a system reset is performed.

## Equipment Control Switches

The Switch Complex and each Remote Complex contains its own status panel. The following sections describe the controls for each type of status panel.

### Switch Complex Status Panel

The Switch Complex status panel (Figure 8-5) in the DACS IV-2000 (512) Main Controller Bay has four momentary contact switches used for equipment control. They are:

- ACO (alarm cutoff) — silences the audible alarms associated with the Switch Complex and collocated interface bays when pressed.
- LED/LAMP TEST — tests the operation of the LEDs/lamps in the DACS IV-2000 Switch Complex and Remote Complexes. This function is performed on a per-shelf basis in sequential order. Pressing this switch is equivalent to entering the `EX-EQPT` command. If the system is busy executing another command, there is a delay before the LEDs light. When this switch is pressed, the LEDs on the High Capacity Controller Module, status panel (except FE LED), Switch Power Modules, SWCS and SWIO circuit packs, and provisioned interface modules are lit on a module- by- module basis. Fan Assembly and Header Designation Assembly LEDs are also exercised as part of the system LED test function.
- RESET — resets the DACS IV-2000. The RESET switch starts the reset function when operated simultaneously with the RESET ENABLE switch. This combination allows the main controller to be booted manually. Requiring simultaneous operation of the RESET and RESET ENABLE switches helps prevent the reset function from being initiated accidentally.

**⚠ CAUTION:**
*Any jacks connected to LAN 0 and LAN 1 on the status panel must be removed before executing the reset.*

- RESET ENABLE — See RESET above.

The Switch Complex status panel also has two TTY connectors (TTY1-1 and TTY2-1) that allow the communications interface terminal (CIT) to be used from the front of the frame. Twelve administrative link connectors are located on the back of the Switch Complex. In addition, two connectors labelled LAN 0 and LAN 1 are reserved.

**⚠ CAUTION:**
*Never connect terminals to the same TTY jack on the Status Panel and the TTY jack at the rear of the Switch Complex (for example, never connect terminals to both jacks for TTY1-1 at the same time).*

### Remote Complex Status Panel

The Remote Complex status panel (Figure 8-6) in the Remote Unit Interface (RUI) Module has four momentary contact switches used for equipment control. They are:

- LOCAL ACO (alarm cutoff) — silences the audible alarms associated with the Remote Complex when pressed.
- LED/LAMP TEST — tests the operation of the LEDs/lamps in the Remote Complex. This function is performed on a per-shelf basis in sequential order. Pressing this switch is equivalent to entering the `EX-EQPT::RX-[1,2];` command. If the system is busy executing another command, there is a delay before the LEDs light. When this switch is pressed, the LEDs on the OPEX, RUI, RUI Power, OPEX Power, and AUX Power Module circuit packs, and provisioned interface modules are lit on a module by module basis. Fan Assembly LEDs are also exercised as part of the system LED test function.
- INTERRUPT — interrupts the Remote Complex. The INTERRUPT switch starts the interrupt function when operated simultaneously with the INTERRUPT ENABLE switch. This combination allows the Remote Unit Interface to be booted manually. Requiring simultaneous operation of the INTERRUPT and INTERRUPT ENABLE switches helps prevent the interrupt function from being initiated accidentally.
- INTERRUPT ENABLE — See INTERRUPT above.

The Remote Complex status panel also has two TTY connectors (TTY1-7/8 and TTY2-7/8) that allow a communications interface terminal (CIT) to be used at the Remote Complex. CILINK-1-7 and CILINK-2-7 are used for Remote Complex 1 and CILINK-1-8 and CILINK-2-8 are used for Remote Complex 2.

**⚠ CAUTION:**
*Never connect terminals to the same TTY jack on the Status Panel and the TTY jack at the rear of the RUI Module (for example, never connect terminals to both jacks for TTY1-7/8 at the same time).*

### EMC Enclosure Header Alarm Indicators

With the EMC option for the DACS IV-2000, the entire front of the system is covered with EMI doors to reduce electromagnetic interference. Because of this, the visual alarm indicators are only visible when viewed straight on. In addition to the EMI doors, this feature provides the following Header Designation Assemblies (HDA) [refer to Figure 8-7] to house the additional alarm indicators:

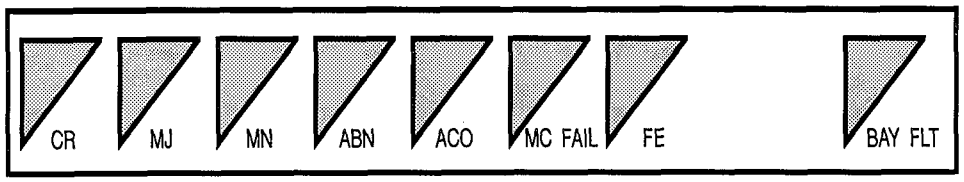
- Main Controller Bay HDA — duplicates MC FAIL, CR, MJ, MN, ABN, ACO, and FE alarm indicators from the status panel and provides a red Bay Fault (BAY FLT) LED indicator that indicates an equipment failure within the Main Controller Bay.
- Switch Bay HDA — contains four green power bus LED indicators for the -48V power feeds and a red BAY FLT LED indicator. The green LEDs, when lit, indicate power is available; when off, they indicate the associated power bus feed has failed. The BAY FLT indicator lights when any circuit pack within the bay has failed.
- Fuse and Alarm Bay HDA — contains eight green power bus LED indicators for the -48V power feeds and a red BAY FLT LED indicator. The green LEDs, when lit, indicate power is available; when off, they indicate the associated power bus feed has failed. The BAY FLT indicator lights when any fuse in the fuse panel is blown or any PWRE circuit pack in the associated interface bay has failed.
- Facility Interface Bay HDA — contains a red BAY FLT LED indicator. The BAY FLT indicator lights when any circuit pack within the bay fails.

## Local and Remote Alarm Connectors

The DACS IV-2000 provides connectors that allow access to the central office alarm system. Table 8-3 identifies the pins associated with the Switch Complex alarm connectors and Table 8-4 identifies the pins associated with the Remote Complex alarm connectors. Both tables are provided as reference information only. The connections from the DACS IV-2000 to the central office alarm system are made at installation or when the DACS IV-2000 frame is relocated. This access provides for:

- Central office audible and visual alarms for the DACS IV-2000
- Remote monitoring and resetting of the DACS IV-2000.

The Switch Complex local alarm connector (Figure 8-3) is located on the back of Bay 11 (top panel) next to the CILINK connectors associated with ECI-1. The remote alarm connector is located on the back of Bay 13 (top panel) next to the CILINK connectors associated with ECI-2. Under normal operations, the alarm connectors do not need to be accessed. The Remote Complex local alarm




**Note:** ABN and FE are reserved for future use.

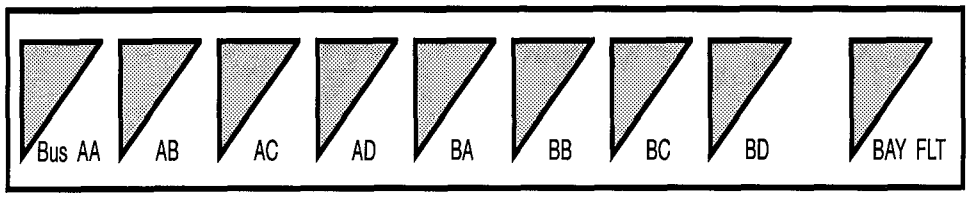
**A. Main Controller Bay**



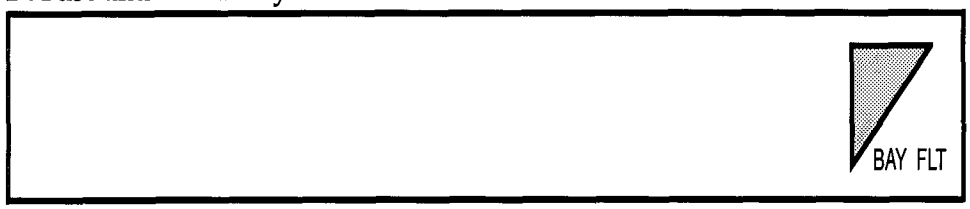

**B. Switch Bay 1**




**C. Switch Bay 2**




**D. Fuse and Alarm Bay**




**E. Interface Bay**

Figure 8-7. **Header Designation Assemblies**

terminal strip (Figure 8-8) is located at the top of the OPEX Bay above the fuse and alarm panel. In order to access the terminal strip, the cover plate must be removed. Under normal operations and in procedures contained in this manual, the terminals do not need to be accessed.

Table 8-3. Switch Complex Alarm Connector Pin Assignments

| Terminal (-24 Volt) | Terminal (-48 Volt) | System Signal |
|---|---|---|
| **Local Office Alarms (Back of Bay 11)** | | |
| 13 | 13 | Minor Audible Alarm Return |
| 14 | 32 | Minor Audible alarm |
| 11 | 11 | Major Audible Alarm Return |
| 12 | 30 | Major Audible Alarm |
| 9 | 9 | Critical Audible Alarm Return |
| 10 | 28 | Critical Audible Alarm |
| 5 | 5 | Minor Visual Alarm Return |
| 6 | 24 | Minor Visual alarm |
| 3 | 3 | Major Visual Alarm Return |
| 4 | 22 | Major Visual Alarm |
| 1 | 1 | Critical Visual Alarm Return |
| 2 | 20 | Critical Visual Alarm |
| 7 | 7 | Processor Major Visual Alarm Return |
| 8 | 26 | Processor Major Visual Alarm |
| **Remote Alarms (Back of Bay 13)** | | |
| 11 | 11 | Remote Minor Alarm Return |
| 12 | 30 | Remote Minor Alarm |
| 9 | 9 | Remote Major Alarm Return |
| 10 | 28 | Remote Major Alarm |
| 7 | 7 | Remote Critical Alarm Return |
| 8 | 26 | Remote Critical Alarm |
| 13 | 13 | Remote Processor Major Alarm Return |
| 14 | 32 | Remote Processor Major Alarm |
| 5 | 5 | Remote ID Return |
| 6 | 24 | Remote ID |
| 15 | 15 | Remote ACO Return |
| 16 | 34 | Remote ACO |

**Notes:**

1. All terminal locations not listed are not used.
2. Cables for connections to remote ACO, remote alarm, and local office alarm in the central office are not supplied with the DACS IV-2000 frame.

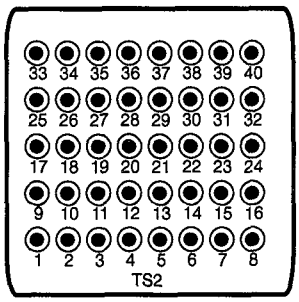



Figure 8-8. **Remote Complex Office and Telemetry Alarm Terminals**

Table 8-4. **Remote Complex Terminal Strip Point Connections**

| Terminal | System Signal | Central Office Connection |
|---|---|---|
| 1 | Major Visual Alarm | Local Office Alarm |
| 2 | Major Visual Alarm Return | Local Office Alarm |
| 5 | Remote Reset B | Remote Alarm |
| 6 | Remote Reset A | Remote Alarm |
| 9 | Remote Major Alarm | Remote Alarm |
| 10 | Remote Major Alarm Return | Remote Alarm |
| 11 | Minor Audible Alarm | Local Office Alarm |
| 12 | Minor Audible Alarm Return | Local Office Alarm |
| 13 | Remote Processor Major Alarm | Remote Alarm |
| 14 | Remote Processor Major Alarm Return | Remote Alarm |
| 17 | Processor Major Visual Alarm | Local Office Alarm |
| 18 | Processor Major Visual Alarm Return | Local Office Alarm |
| 19 | Remote ID | Remote Alarm |
| 20 | Remote ID Return | Remote Alarm |
| 21 | Minor Visual Alarm | Local Office Alarm |
| 22 | Minor Visual Alarm Return | Local Office Alarm |
| 27 | Critical Visual Alarm | Local Office Alarm |
| 28 | Critical Visual Alarm Return | Local Office Alarm |
| 29 | Major Audible Alarm | Local Office Alarm |
| 30 | Major Audible Alarm Return | Local Office Alarm |
| 33 | Remote Critical Alarm | Remote Alarm |
| 34 | Remote Critical Alarm Return | Remote Alarm |

Table continued on next page. See notes at end of table.

Table 8-4. **Remote Complex Terminal Strip Point Connections (Continued)**

| Terminal | System Signal | Central Office Connection |
|---|---|---|
| 35 | Critical Audible Alarm | Local Office Alarm |
| 36 | Critical Audible Alarm Return | Local Office Alarm |
| 37 | Remote Minor Alarm | Remote Alarm |
| 38 | Remote Minor Alarm Return | Remote Alarm |

**Notes:**

1. All terminal locations not listed are not used.
2. Cables for connections to remote reset, remote alarm, local office alarm, and the BITS timing references in the central office are not supplied with the DACS IV-2000 frame.

## SYNC-0 and SYNC-1 Connectors

The DACS IV-2000 provides connectors (see Figure 8-3) that allow access to the central office Building Integrated Timing Supply (BITS) timing reference signals. Table 8-5 identifies the pins associated with the BITS synchronous timing reference connectors, and is provided as reference information. The connections from the DACS IV-2000 to the central office BITS are made at installation or when the DACS IV-2000 frame is relocated. This access provides for:

- Central office local timing reference signals for the DACS IV-2000
- Central office remote timing reference signals for the DACS IV-2000.

The SYNC-0 connector is located on the back of Bay 11 (top panel) next to the Local Alarms connector. The SYNC-1 connector is located on the back of Bay 13 (top panel) next to the Remote Alarms connector. Under normal operations, the SYNC connectors do not need to be accessed.

Table 8-5. Synchronizer Connector Pin Connections

| Connector Pins | Timing Reference Signal | Central Office Connection |
|---|---|---|
| **BITS Timing Reference to Synchronizer Side 0 (Back of Bay 11)** | | |
| 1 through 8 | Reserved for Future Use | - |
| 9 through 20 | Not Connected | - |
| 21 | SYNCPRI (Tip) | BITS Reference |
| 22 | SYNCPRI (Ring) | BITS Reference |
| 23 | SYNCSEC (Tip) | BITS Reference |
| 24 | SYNCSEC (Ring) | BITS Reference |
| **BITS Timing Reference to Synchronizer Side 1 (Back of Bay 12)** | | |
| 1 through 8 | Reserved for Future Use | - |
| 9 through 20 | Not Connected | - |
| 21 | SYNCPRI (Tip) | BITS Reference |
| 22 | SYNCPRI (Ring) | BITS Reference |
| 23 | SYNCSEC (Tip) | BITS Reference |
| 24 | SYNCSEC (Ring) | BITS Reference |

# Technical Specifications

# A

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# Technical Specifications

# A

This appendix describes the technical specifications that must be considered when engineering the DACS IV-2000 (512) Release 5.0 into a network. It provides technical specifications for the following areas:

- Interface
- System Performance
- Power
- Physical
- Environmental
- Availability and Reliability.

## Interface Specifications

This section describes the transmission interface specifications, the alarm and control specifications, and the command and message specifications for the DACS IV-2000.

## Transmission Characteristics

The transmission interface characteristics of the DACS IV-2000 include the port capacity, signal characteristics, signal impairments, and cable characteristics. Each of these areas is addressed in this section, and the particular specifications and requirements associated with each area are included.

### Port Capacity

Port capacity defines the number of DS1, DS3, and/or STS-1 ports that can be terminated on the DACS IV-2000 and is a function of the number and types of interface bays. The maximum configurations include:

- 13,888 DS1 ports for an arrangement consisting of all DS1 ports (496 equivalent DS3s)
- 496 DS3 ports for an arrangement consisting of all DS3 ports
- 480 STS-1 ports for an arrangement consisting of all STS-1 ports.

Bay arrangements include:

- A collocated arrangement, in which the Switch Complex and the interface bays are physically and electrically connected
- A remoted arrangement, in which the Switch Complex and up to half the interface bay capacity (one Remote Complex) are physically separated up to 1000 cable feet and optically connected
- A second remoted arrangement, in which two Remote Complexes are optically connected to the Switch Complex.

The port capacities of the DACS IV-2000 (512) are summarized in Table A-1.

Table A-1. **Port Capacity**

| Item | Value |
|---|---|
| Maximum System Capacity | 496 DS3-equivalent input and output interface ports |
| Maximum DS1 Port Capacity | 13,888 input and output DS1 interface ports |
| Maximum DS3 Port Capacity | 496 input and output DS3 interface ports |
| Maximum STS1 Port Capacity | 480 input and output STS1 interface ports |

## Signal Characteristics

The transmission interfaces to the DACS IV-2000 are DSX-3, DSX-1, and STSX-1 compatible facilities or network elements.

### DS3 Signal

The DACS IV-2000 accepts incoming DS3 signals at the specified line rate of 44.736 Mbps with the specified B3ZS line code. Acceptable signal formats are asynchronous M13 or C-bit parity. (See Table A-2.)

Table A-2. **DS3 Signal Characteristics**

| Item | Value |
|---|---|
| Frame Format | M13/C-bit parity; unframed (MUX3 only) |
| DS3 Line Rate | 44.736 Mbps ±20 ppm |
| Line Code | B3ZS |
| Test Load Impedance | 75Ω ±5% resistive, unbalanced |

### DS1 Signal

The DACS IV-2000 accepts incoming DS1 signals at the specified line rate of 1.544 Mbps with the specified AMI or B8ZS line code. (See Table A-3.) The DACS IV-2000 is fully transparent to the DS1 bit stream; that is, all overhead and payload bytes are passed through unchanged.

Table A-3. **DS1 Signal Characteristics**

| Item | Value |
|---|---|
| DS1 Line Rate | 1.544 Mbps ±130 ppm |
| Line Code | AMI or B8ZS |
| Test Load Impedance | 100Ω ±5% resistive, balanced |

### STS-1 Signal

The DACS IV-2000 accepts incoming STS-1 signals at the specified line rate of 51.84 Mbps with the B3ZS line code. (See Table A-4.)

Table A-4. **STS-1 Signal Characteristics**

| Item | Value |
|---|---|
| STS-1 Signal Format | Conforms to TA-NWT-000253 |
| STS-1 Line Rate | 51.84 Mbps ±4.6 ppm |
| Line Code | B3ZS |
| Duty Cycle (measured at output cable terminals) | Nominal 50%, RZ pulse with 1.03V (±10%) peak output amplitude |
| Frame Synchronous Scrambling | Conforms to TA-NWT-000253 |
| Wideband Power Level (measured at 450 ft) | -2.7 dBm to 4.7 dBm |

## Signal Impairments

The requirements related to signal impairments in electronic digital signal cross-connect equipment are specified in Bellcore TA-NWT-000233, *Wideband and Broadband Digital Cross-Connect Systems Generic Criteria* (Issue 1, November 1993) and TA-NWT-001339, *General Reliability Requirements for Digital Cross-Connect Systems* (Issue 1, November 1993). The requirements applicable to the DACS IV-2000 are summarized in the following paragraphs.

### DS3 Signal

The jitter accommodation (tolerance) requirement for a DS3 signal input is specified in terms of the amount of sinusoidal jitter (peak-to-peak) that must be accommodated versus the frequency of that jitter. The DACS IV-2000 meets the jitter accommodation requirements for a DS3 signal given in Figure 7 of Bellcore TR-TSY-000009, *Asynchronous Digital Multiplexer Requirements and Objectives* (Issue 1, May 1986) and Figure 7-2 of Bellcore TR-NWT-000499, *Transport Systems Generic Requirements (TSGR): Common Requirements* (Issue 4, Revision 1, April 1992). The DACS IV-2000 does not generate more than 0.01 unit interval (timeslots) of rms jitter with a high-pass measurement filter with 12-Hz cutoff frequency.

The peak signal-to-rms noise (S/N) power ratio for an all-ones pattern measured over the bandwidth of the digital signal in the DACS IV-2000 is greater than 46 dB

on any digital output line signal. The return loss at a half-bit rate (normal cross-connection) measured at the input of a cross-connection in the DACS IV-2000 is greater than 18 dB. (The cross-connection must be properly terminated when making this measurement.)

The DACS IV-2000 provides more than 46-dB (measured at 22.368 MHz) isolation between any two DS3 output ports.

The DS1-to-DS3 nominal transmission delay (normal cross-connection) through the DACS IV-2000 is less than 25 μs for AMI-coded DS1 inputs and less than 29.5 μs for B8ZS-coded DS1 inputs. The DS3-to-DS3 nominal transmission delay (normal cross-connection) through the DACS IV-2000 is less than 23 μs.

The DACS IV-2000 provides an operational bit error rate (BER) of less than $10^{-10}$ per cross-connect path across the system regardless of the number of other cross-connections established. The DS3 signal impairment specifications are shown in Table A-5 (MUX2 circuit pack) and Table A-6 (MUX3 circuit pack).

Table A-5. **DS3 Signal Impairment Specifications (MUX2 Circuit Pack)**

| Item | Value |
|---|---|
| Jitter Accommodation | Conforms to TR-TSY-000009 (Figure 7) and TR-NWT-000499 (Figure 7-2) |
| Jitter Generation | < 0.01 UI |
| Signal-to-Noise Power Ratio | > 46 dB for all-ones signal pattern |
| Return Loss at 22.368 MHz (normal cross-connection) | >18 dB |
| Crosstalk | > 46 dB isolation between any two DS3 output ports |
| Transmission Signal Delay DS1 to DS3 (normal cross-connection) | < 25 μs (AMI), < 29.5 μs (B8ZS) |
| Transmission Signal Delay DS3 to DS3 | < 23 μs |
| Bit Error Rate (BER/cross-connect path) | $< 1 \times 10^{-10}$ |

Table A-6. DS3 Signal Impairment Specifications (MUX3 Circuit Pack)

| Item | Value |
|---|---|
| Jitter Accommodation | TR-NWT-000499, Issue 5 (Figure 7-1) |
| Jitter Generation | < 0.4 UI |
| Jitter Transfer | TA-NWT-000253, Issue 8 (Figure 5-13) |
| Bit-Error Rate | $< 1 \times 10^{-10}$ |
| Transmission Signal Delay DS3 Clear-Channel | 16 µs |
| Transmission Signal Delay DS3 Clear-Channel in DS1 Mode | 27 µs |
| Transmission Signal Delay Enhanced DS3 Interface | 27 µs |

## DS1 Signal

The jitter accommodation (tolerance) requirement for a DS1 signal input is specified in terms of the amount of sinusoidal jitter (peak-to-peak) the signal accommodates versus the frequency of that jitter. The DACS IV-2000 meets the jitter accommodation requirements for a DS1 signal given in Figure 7 of Bellcore TR-TSY-000009, *Asynchronous Digital Multiplexer Requirements and Objectives* (Issue 1, May 1986) and Figure 7-2 of Bellcore TR-NWT-000499, *Transport Systems Generic Requirements (TSGR): Common Requirements* (Issue 4, Revision 1, April 1992). The DACS IV-2000 does not generate more than 0.3 UI (timeslots) of rms jitter or more than 1 UI of peak-to-peak jitter over a 10-Hz to 40-kHz jitter spectrum in the absence of input jitter.

The peak signal-to-rms noise (S/N) power ratio for an all-ones pattern measured over the bandwidth of the digital signal in the DACS IV-2000 is greater than 46 dB on any digital output line signal. The return loss at a half-bit rate (normal cross-connection) measured at the input of a cross-connection in the frame is greater than 18 dB. (The cross-connection must be properly terminated when making this measurement.) The DACS IV-2000 provides more than 46-dB (measured at 772 kHz) isolation between any two DS1 output ports.

The DS1-to-DS1 nominal transmission delay (normal cross-connection) through the DACS IV-2000 is less than 27.5 μs for AMI-coded DS1 inputs/outputs and less than 37 μs for B8ZS-coded DS1 inputs/outputs. The nominal DS1 line loopback transmission delay is less than 3 μs.

The DACS IV-2000 provides an operational BER of less than $10^{-10}$ per cross-connect path across the system regardless of the number of other cross-connections established.

The DS1 signal impairment specifications are shown in Table A-7.

Table A-7. **DS1 Signal Impairment Specifications**

| Item | Value |
|---|---|
| Jitter Accommodation | Conforms to TR-TSY-000009 (Figure 7) and TR-NWT-000499 (Figure 7-2) |
| Jitter Generation (rms) | < 0.3 UI |
| Jitter Generation (peak-to-peak) | < 1.0 UI |
| Signal-to-Noise Power Ratio | > 46 dB for all ones signal pattern |
| Return Loss at 772 kHz (normal cross-connection) | >18 dB |
| Crosstalk | > 46 dB isolation between any two DS1 output ports |
| Transmission Signal Delay DS1 to DS1 (normal cross-connection) | < 27.5 μs (AMI), < 37 μs (B8ZS) |
| Transmission Signal Delay DS1 Line Loopback | < 3.0 μs |
| Bit Error Rate (BER/cross-connect path) | $< 1 \times 10^{-10}$ |

### STS-1 Signal

The jitter accommodation (tolerance) requirement Ifor an STS-1 signal input is specified in terms of the amount of sinusoidal jitter (peak-to-peak) that must be accommodated versus the frequency of that jitter. The DACS IV-2000 meets the jitter accommodation requirements for an STS-1 signal given in Bellcore GR-253-CORE, *SONET Transport Systems: Common Generic Criteria (A Module of TSGR, FR-NWT-000440)* (Issue 8, October 1993). The DACS IV-2000 does not generate more than 0.01 UI (timeslots) of rms jitter with a high-pass measurement filter with a 12-kHz cutoff frequency.

The STS-1 signal impairment specifications are shown in Table A-8.

Table A-8. **STS-1 Signal Impairment Specifications**

| Item | Value |
|---|---|
| Jitter Accommodation | Conforms to TA-NWT-000253 |
| Jitter Transfer (terminating DS1 signals on STS1 interfaces) | Conforms to TA-NWT-000253 |
| Jitter Amplitude (terminating DS1 signals on STS1 interfaces) | < 5 UI peak-to-peak |
| Jitter Generation (rms) | < 0.01 UI |

## Cable Characteristics

Various cables and connectors are available for interconnecting the DACS IV-2000 to a DSX-1, DSX-3, or STSX-1, or directly to other network elements.

### Optical Interface Cable and Connectors

All optical transmission cables are single-mode. All optical control cables are multi-mode. The maximum cable distance between the Switch Complex and a remoted interface bay is 1000 feet. All connectors are SC-type.

## DS3 Interface Electrical Cable and Connectors

The DACS IV-2000 supports both overhead and underfloor cable distribution. The DS3 interface cable and connector specifications are shown in Table A-9.

Table A-9. **DS3 Cable and Connector Specifications**

| Item | Value |
|---|---|
| Maximum Distance to DSX-3 (KS-19224-type cable) | 150 ft |
| Maximum Distance to DSX-3 (734-type cable) | 450 ft |
| Maximum Distance to DSX-3 (735-type cable) | 250 ft |
| Maximum Distance to DS3 NE (KS-19224-type cable) | 300 ft |
| Maximum Distance to DS3 NE (734-type cable) | 900 ft |
| Maximum Distance to DS3 NE (735-type cable) | 500 ft |
| DS3 Connector Type (982-type) at the DACS IV-2000 | 2x4 |
| DS3 Connector Type (BNC) at the DACS IV-2000 | connectorized |

## DS1 Interface Electrical Cable and Connectors

The DACS IV-2000 supports both overhead and underfloor cable distribution. The DS1 interface cable and connector specifications are shown in Table A-10.

Table A-10. **DS1 Cable and Connector Specifications**

| Item | Value |
|---|---|
| Maximum Distance to DSX-1 (600-type cable) | 655 ft |
| Maximum Distance to DSX-1 (1249-type cable*) | 450 ft |
| Maximum Distance to DS1 NE (600-type cable) | 1310 ft |
| Maximum Distance to DS1 NE (1249- or 2249-type cable*) | 900 ft |
| DS1 Connector Type (963P/T) or Wirewrap at the DACS IV-2000 | 2x14 (in)<br>1x28 (out) |
| DS1 Connector Type at DSX-1 | wirewrap |

* 1249 is preferred for overhead installation; 2249 is required for underfloor installation.

### STS1 Interface Electrical Cable and Connectors

The DACS IV-2000 supports both overhead and underfloor cable distribution. The STS1 interface cable and connector characteristics are shown in Table A-11

Table A-11. **STS1 Interface Cable and Connector Characteristics**

| Item | Value |
|---|---|
| Maximum Distance to STS1 NE (735-type cable or equivalent) | 500 ft |
| Maximum Distance to STSX-1 (735-type cable or equivalent) | 250 ft |
| Maximum Distance to STS1 NE (734-type cable or equivalent) | 900 ft |
| Maximum Distance to STSX-1 (734-type cable or equivalent) | 450 ft |
| STS1 Connector Type (982-type) at the DACS IV-2000 | 2x4 |
| STS1 Connector Type (BNC) at the DACS IV-2000 | connectorized |

## Alarm and Control Specifications

The alarm and control interfaces for the DACS IV-2000 consist of office and remote alarms, communications, telemetry, and operations systems (OSs). Each of these interfaces is addressed in this section, and the particular specifications and characteristics associated with each interface are included.

### Office and Remote Alarms

The DACS IV-2000 has seven office alarm outputs: Critical Audible, Critical Visual, Major Audible, Major Visual, Minor Audible, Minor Visual, and Main Controller Failure Visual. Contact closures for visual alarms remain latched until the failure is cleared.

The DACS IV-2000 provides a set of relay closures for critical, major, and minor alarms, which can be picked up by a remote telemetry system in the local office and sent to the appropriate OS.

All alarm contacts are rated as follows: maximum current (1.0 ampere), maximum voltage (48 volts), and maximum volt-amperage (20 volt-amperes).

The activation of the alarms is delayed to avoid calling the technician to respond to transient errors of short duration. The alarm delay is programmable over a range of 1 to 30 seconds. The alarm delay operates on all audible and visual office alarm outputs, including major and minor visual indicators, autonomous messages, and OS (telemetry) alarm points. The OS status points associated with the delayed alarm points are similarly delayed.

The office and telemetry alarm types and requirements for the DACS IV-2000 are shown in Table A-12.

Table A-12. **Office and Telemetry Alarms and Requirements**

| Item | Value |
|---|---|
| Local Office Audible Alarms | Critical, Major, Minor |
| Local Office Visual Alarms | Critical, Major, Minor, MC Fail |
| Remote Telemetry Alarms | Critical, Major, Minor, MC Fail, Remote Indicator |
| Alarm Contact Closure Rating | 1.0A, 48V, 20 VA (max) |
| Alarm Delay (non-SONET facilities and equipment) | 1 to 30 sec (default 10 sec) |
| Alarm Clear Delay (non-SONET facilities and equipment) | 1 to 20 sec (default 10 sec) |
| Soak Time – Alarm Onsets (SONET facilities) | 1 to 30 sec (default 2 sec) |
| Soak Time – Alarm Clears (SONET facilities) | 1 to 20 sec (default 10 sec) |
| GTP Poll Time | 10 to 60 sec (default 20 sec) |

## Communications and OS Interfaces

The link characteristics for the communications and OS interfaces for the DACS IV-2000 are shown in Table A-13.

Table A-13. **Link Characteristics**

| Interface | Physical | Baud | Electrical | Functional |
|---|---|---|---|---|
| CILINK 1-1 and 2-1 | EIA-232-D | 1200, 2400, 4800, 9600, and 19200 Default: 9600 | EIA-232-D | Async. Snider |
| CILINK 1-2 and 2-2 | EIA-449 | 1200, 2400, 4800, and 9600 Default: 2400 | EIA-423 | Async. Snider |
| CILINK 1-3 and 2-3 | EIA-449 | 1200, 2400, 4800, 9600, and 19200 Default: 9600 | EIA-423 | Async. Snider |
| CILINK 1-4 and 2-4 | EIA-449 | 1200, 2400, 4800, and 9600 Default: 2400 | EIA-485 | TABS point-to-point AS&C |
| CILINK 1-5, 1-6, 2-5, and 2-6 | EIA-449 | 1200, 2400, 4800, and 9600 Default: 9600 | EIA-423 | Sync. X.25 or Async. Terminal Interface with external PAD |
| CILINK 1-7, 1-8, 2-7, and 2-8 | EIA-232-D | 1200, 2400, 4800, 9600, and 19200 Default: 9600 | EIA-232-D | Async. Snider |

Notes:

1. All EIA-423 links are interoperable with EIA-232-D via the use of the suggested adapters. For Snider links DACS IV-2000-to-terminal communication, it is suggested the ED-2C646,G1 adapter be used. For Snider links DACS IV-2000-to-OS via modem communication, it is suggested the ED-2C646,G2 adapter be used.
2. Links 1-2 and 2-2 are electrically compatible with the EIA-232-D (see Note 1) standard up to 4800 baud. Links 1-3 and 2-3 are electrically compatible with the EIA-232-D standard up to 9600 baud. These links may operate with the EIA-232-D above these data rates; however, the 4-percent rise time specification of EIA-232-D is violated.
3. To supply internal timing for the X.25 links, the ED-2C646,G7 adapter must be used and the baud rate is fixed at 9600. All baud rates can be used with an external timing source.

## Protocols

The interface protocol for Links 1-1, 1-2, 1-3, 1-7, 1-8, 2-1, 2-2, 2-3, 2-7, and 2-8 is asynchronous Snider, which is defined in Bellcore TR-NWT-000064, LATA Switching Systems Generic Requirements (LSSGR), and FSD 35-08-0100, *SPCS (Stored Program Control Systems) OS Interface, SCCS (Switching Control Center System), Asynchronous Interface.*

The message interface protocol for Links 1-4 and 2-4 (TABS) is specified in Compatibility Bulletin #149, *Maintenance Standards for Digital Transmission Systems* (Issue 4).

The synchronous Links 1-5, 1-6, 2-5, and 2-6 operate up to 9600 baud. The message interface protocol for the four links is X.25 as verified with Bellcore TR-NWT-001213, *Objectives for the Maintenance User Interface of Switching Systems and Transport Systems* (Issue 1, March 1992) or asynchronous terminal interface with the use of an external PAD.

The network layer for the synchronous links is X.25. The DACS IV-2000 meets the CCITT X.25 1984 specification and has been verified with Bellcore TR-NWT-001213, *Objectives for the Maintenance User Interface of Switching Systems and Transport Systems* (Issue 1, March 1992).

## TABS Link Specifications

The DACS IV-2000 has a TABS port as an electrical interface to a telemetry-based OS. The electrical interface specifications are given in Compatibility Bulletin #149, *Maintenance Standards for Digital Transmission Systems* (Issue 4). The interface can be connected to the monitoring equipment on a point-to-point basis. The interface operates at 1200 to 9600 baud.

All alarm and status indications available over the communications interface link are also available over the TABS telemetry link. (Note that the mapping between communications and telemetry interfaces is not on a one-to-one basis.) The only control functions available over the telemetry links are protection switches and locks, and CLKGN circuit pack switches.

## X.25 Link Specifications

The DACS IV-2000 has two synchronous EIA-449/EIA-423 ports for electrical interfaces to message-based OSs. The physical interface specifications are given in EIA Standard EIA-449 (November 1977). The synchronous links have the unbalanced voltage signals of EIA-423. The functions that can be performed over the synchronous links depend on the OS. The links can be converted to an asynchronous terminal interface with the use of an external PAD.

## Command and Message Specifications

**NOTE:**
In previous releases, the DACS IV-2000 supported Message Sets 1 and 2. The DACS IV-2000 (512) starting with Release 3.0 supports one message set, formerly Message Set 2.

The DACS IV-2000 message interface is compatible with two operations systems from Bellcore: the Operations Systems/Intelligent Network Elements (OPS/INE) and Network Monitoring and Analysis (NMA). This message set, commonly known as Transaction Language 1, Issue 4, is based on the Bellcore Special Reports, Technical Advisories, and Technical References listed in Table A-14.

Table A-14. **Command and Message Specifications**

| Document Number | Specification |
|---|---|
| SR-STS-001665 | *Network Monitoring and Analysis Generic Network Element Interface Support* (Issue 2, December 1992) |
| SR-STS-001578 | *OPS/INE Generic Interface Support* (Issue 2, December 1992) |
| TA-NWT-000199 | *Specification of Memory Administration Messages at the OS/NE Interface* (Issue 7, January 1993) |
| TA-NWT-000200 | *Specification of System Maintenance Messages at the OS/NE Interface* (Issue 5, December 1990) |
| TR-NWT-000811 | *OTGR: Operations Application Messages - TL1 Message Index* (Issue 2, May 1992) |
| TR-NWT-000818 | *OTGR Section 6.1: Network Maintenance: Access and Testing - Generic Test Architecture* (Issue1, November 1992) |
| TR-NWT-000833 | *OTGR: Operations Application Messages Network Maintenance: Generic Requirements for Network Element and Transport Surveillance Messages, Section 12.3* (Issue 5, Revision 2, April 1993) |
| TR-NWT-000835 | *OTGR: Operations Application Messages - Network Element (NE) Security Parameter Administration Messages, Section 12.5* (Issue 3, Revision 1, May 1991) |

# System Performance Specifications

The system capabilities and performance specifications for the DACS IV-2000 cover switch types and capacity, cross-connection capabilities, boot time, fault tolerance and protection, and frame indicators and controls. Each of these areas is addressed in this section, and the particular specifications and requirements associated with each area are included.

## Switch Type and Capacity

All cross-connect-related functions in the DACS IV-2000 are accomplished via a nonblocking, 3-stage, space-division switch. Nonblocking here implies that access to any or all of the free paths through the switch is never denied so that a connection from an input port to an output port can always be completed.

The capacity of the DACS IV-2000 is 14,336 input and output switch ports (512 equivalent DS3 signals).

## Cross-Connect Capability

The DACS IV-2000 supports four types of cross-connections:

- One-way
- Two-way
- Bridge
- Roll.

The execution time for a command depends on the type of command; speed and status of the administrative links; activities in the DACS IV-2000; and the status of the equipment in the system needed to make the connection.

The cross-connect command to the DACS IV-2000 can be one-way or two-way. The cross-connect setup time specification includes the time from which the system receives the command to the time the connection is made; it does not include the output message. The time to set up a one-way or two-way cross-connection is less than 1 second.

The DACS IV-2000 can bridge any existing connection by cross-connecting the input port to a second output port without affecting service (that is, the existing cross-connect path is not affected). The time to set up a bridge is less than 1 second.

A tail-end switch occurs when an existing cross-connect path is disconnected and a new cross-connection is made at the tail-end of a facility. The in-service rolling operation requires that a tail-end switch be made in less than 2 ms. In executing the tail-end switch (command), the DACS IV-2000 does not cause more than a

2-ms interruption in the transmission signal (error-free transmission is established within 2 ms).

A one-way signal split of an existing cross-connect path between an input port and an output port is accomplished by rerouting the input port signal to a test output port and cross-connecting the signal from the test input port to the output port. The DACS IV-2000 does not cause more than a 2-ms interruption in the signal appearing at the output port (error-free transmission is established within 2 ms).

The original cross-connect path is established automatically when the split function is disabled. In establishing the original cross-connection, the system does not cause more than a 2-ms interruption in the signal appearing at the output port (error-free transmission is established within 2 ms).

The cross-connect capabilities of the DACS IV-2000 are shown in Table A-15.

Table A-15. **Cross-Connect Capabilities**

| Cross-Connect Procedures | Value |
|---|---|
| One-way Cross-Connect Setup Time | < 1 sec (DS1, VT1.5)<br>< 3 sec (STS-1/DS3 clear-channel) |
| Two-way Cross-Connect Setup Time | < 1 sec (DS1, VT1.5)<br>< 3 sec (STS-1/DS3 clear-channel) |
| Bridge Setup Time | < 1 sec (DS1, VT1.5)<br>< 3 sec (STS-1DS3 clear-channel) |
| Rolling (Signal Interruption Time) | < 2 ms (DS1, VT1.5)<br>< 3 ms (STS-1/DS3 clear-channel) |
| One-way Signal Split (Signal Interruption Time) | < 2 ms (DS1, VT1.5)<br>< 3 ms (STS-1/DS3 clear-channel) |

## Boot Time

The system boot time is the elapsed time from the moment a system reset request is made to the moment the system is ready for an input command. The boot time includes the downloading of all the system programs and the latest cross-connect maps from the hard disk to the appropriate controllers. If the information on the hard disk has been corrupted, additional time is required to restore the information to the hard disk from a backup optical disk before the DACS IV-2000 can be booted. The memory update procedures conform to Bellcore TA-NWT-000199, *Specification of Memory Administration Messages at the OS/NE Interface* (Issue 7, January 1993).

The boot time specifications for the DACS IV-2000 are shown in Table A-16. (Boot times for the collocated and remote systems do not differ significantly.)

Table A-16. **Boot Time Specifications (Collocated Systems)**

| | Value |
|---|---|
| **Procedure** | **Collocated** |
| Cold Boot (from hard disk) | < 15 min |
| Cold Boot (from backup optical disk) | < 15 min |
| Restart (MC, ECI) | < 5 min |
| Memory Administration | Conforms to TA-NWT-000199 |

## Fault Tolerance and Protection

The DACS IV-2000 can isolate a fault to the facility or equipment, and can isolate the fault to the equipment circuit-pack level.

The DACS IV-2000 provides two provisionable BER alarm thresholds for input signals. The high category shows failures at $10^{-3}$, and the low category shows failures at $10^{-9}$. If the facility connects to a MUX2 circuit pack (DS3), an SWIF2 circuit pack (DS1), or an SMUX circuit pack (STS1), you can choose from the following bit error rate thresholds: $10^{-3}$, $10^{-4}$, $10^{-5}$, $10^{-6}$,$10^{-7}$, $10^{-8}$, or $10^{-9}$ errors per second. At the local office, the incoming signal failures are indicated at the threshold you have specified (major, minor, or no alarm).

Any single hard equipment failure (a nontransient failure that can cause interruption in the transmission path) in the DACS IV-2000 is protected, and the protection switching capability restores error-free transmission within 60 ms from the moment such a failure occurs. Following a correct protection switch around a failed circuit pack and after the failed circuit pack is replaced by a new circuit pack, the health of this new circuit pack is checked. Service is automatically restored to this new circuit pack from the protection circuit pack. The automatic restoration time is the elapsed time between the replacement of a circuit pack and the restoration of service to this new circuit pack. The automatic restoration time is less than 10 seconds. The automatic restoration does not cause more than a 60-ms interruption in the transmission path.

The DACS IV-2000 automatically supplies DS1 IDLE (unframed all ones), STS-1 AIS, and VT1.5 AIS signals to the output ports (toward facilities/DSX-3) to drive facilities that are not cross-connected through the DACS IV-2000. When an existing cross-connect path is disconnected, a DS1 IDLE, STS-1 AIS, or VT1.5 AIS signal is substituted at the output port in less than 3 ms.

The fault tolerance and protection specifications for the DACS IV-2000 are shown in Table A-17.

Table A-17. **Fault Tolerance and Protection Specifications**

| Item | Value |
|---|---|
| Cross-Connect Path Monitoring | Continuous |
| Input Signal Alarm, BER Threshold (DS1, DS3, and STS1 interfaces) | $10^{-3}$, $10^{-4}$, $10^{-5}$,$10^{-6}$,$10^{-7}$,$10^{-8}$,$10^{-9}$ |
| Input Signal Failure Alarm | Major, Minor, or No Alarm |
| Input Signal Failure Visual Indication | ALM (flashes at 1-sec intervals) |
| DS1 AIS Substitution Time | < 3 ms |
| STS-1 AIS Substitution Time | < 3 ms |
| VT1.5 AIS Substitution Time | < 3 ms |
| Protection Switching Time | < 60 ms |
| Automatic Restoration Time | < 10 sec |

## Frame Indicators and Controls

Frame indicators and controls are provided in both the Switch Complex and the Remote Complexes.

Seven visual equipment indicators are provided on the Switch Complex status panel (contained in the Main Controller Bay):

- CR (Critical) signals a critical alarm condition; red
- MJ (Major) signals a major alarm condition; red
- MN (Minor) signals a minor alarm condition; yellow
- ABN (Abnormal) is reserved for future use
- ACO (Alarm Cutoff) signals that the audible alarms have been turned off (ACO switch activated); green
- MC FAIL (Main Controller failure) is a processor major alarm that signals a failure in the High-Capacity Controller Module; red; (256) and (512) are not optically connected to a (512)
- FE (Far End) is reserved for future use.

The Remote Complex contains:

- CRITICAL signals a critical alarm condition
- MAJOR signals a major alarm condition
- MINOR signals a minor alarm condition
- ABNORMAL is reserved for future use
- LOCAL ACO (Local Alarm Cutoff) shows that the audible alarms for the Remote Complex have been silenced (ACO switch activated)
- POWER ON signals that power is present at the status panel
- FAIL signals a failure in the Remote Unit Interface (RUI) Module
- FAR END is reserved for future use.

All circuit packs, except those in the version one Synchronizer Module, have a red LED to aid in problem identification. (In addition, the ECI circuit packs have green LEDs to indicate the ECI is in service.) The LED is mounted so that it is visible while the circuit pack is in the equipment. The LED is controlled by a main/unit controller so that it can be illuminated even if the circuit pack it is mounted in is defective. In addition to the red LEDs, alarm messages are generated for all circuit-pack failures.

For the DS1, DS3, and STS1 interface circuit packs and version two DS1TX circuit packs, the LED indicators flash continuously at 1-second intervals on circuit packs that have input signal failures, and remain on for failures in the circuit packs themselves. (Circuit-pack failure indicators have a minimum duration of two seconds, to distinguish them from incoming signal failures.) The power circuit packs activate their respective LEDs when a fault exists. Because the power circuit pack failure LED is powered from the primary power supply, it lights even when there is a loss of logic level power.

There are four controls (momentary-action, pushbutton, or toggle switches) located on the Switch Complex status panel. They are:

- LED/LAMP TEST tests all LEDs
- RESET initiates the system reset function when operated simultaneously with the RESET ENABLE switch
- RESET ENABLE inhibits the reset function from being activated accidentally
- ACO turns off the office audible alarms.

There are four controls (momentary-action, pushbutton, or toggle switches) located on the Remote Complex status panel. They are:

- LED/LAMP TEST tests all LEDs
- INTERRUPT initiates the interrupt function of the Remote Complex when operated simultaneously with the INTERRUPT ENABLE switch
- INTERRUPT ENABLE inhibits the reset function from being activated accidentally
- LOCAL ACO turns off the office audible alarms.

The alarm selection criteria for the DACS IV-2000 conform to Bellcore TR-TSY-000191, *Alarm Indication Signal Requirements and Objectives* (Issue 1, May 1986).

The alarm indications for maintenance support in the DACS IV-2000 are summarized in Table A-18.

Table A-18. **Visual Indicators**

| Indicator | Value or Specification |
|---|---|
| System Visual Indicators (Switch Complex) | CR, MJ, MN, ACO, MC FAIL |
| System Visual Indicators (Remote Complex) | CRITICAL, MAJOR, MINOR, LOCAL ACO, POWER ON, FAIL |
| Circuit Pack Failure Visual Indicator | ALM (2-sec minimum duration); red LED lit |
| Protection Bus Active Visual Indicator | Green LED lit on MUXPS or DS1RY |
| Primary and Secondary Disk Active Visual Indicator (when disk is spinning) | Green LED lit |
| Power Feed Status Visual Indicator | Green LED lit |
| System Controls (Switch Complex) | LED TEST, RESET/RESET ENABLE, and ACO |
| System Controls (Remote Complex) | LED TEST, INTERRUPT/INTERRUPT ENABLE, and LOCAL ACO |
| Power Bus Failure Indicator | BUS AA, AB, AC, AD, BA, BB, BC, BD |
| Power Unit Failure Visual Indicator | ALM; red LED lit |
| Alarm Selection Criteria | Conforms to TR-TSY-000191 |
| CPU (Control Complex) Active Visual Indicator | Green LED lit |
| Active CLKGN Visual Indicator | Green LED lit |
| Version Two Synchronizer Active Visual Indicator | Green LED lit |

# Power Specifications

Two sets of power requirements for the DACS IV-2000 are addressed in this section, one for the DACS IV-2000 (512) Switch Module and collocated interface bays and one for the Remote Complexes [converted to DACS IV-2000 (256) frames].

- For power information regarding a collocated configuration, see the *Floor Plan Data* (FPD 801-500-168-15)
- For power information regarding a singularly powered Remote Complex, see the *Floor Plan Data* (FPD 801-500-168-8)
- For power information regarding Remote Complexes with duplex power, see the *Floor Plan Data* (FPD 801-500-168-21).

## Switch Complex and Collocated Interface Bays

The DACS IV-2000 (512) operates with one or two Lineage® 2000 (or equivalent) battery plants (-48 Vdc nominal) in a central office environment, which supply power to one or two battery distribution feeder boards (BDFBs). BDFB-A supplies power buses AA through AD, and BDBF-B supplies power buses BA though BD to the Switch Complex and collocated interface bays. All feeders have four connections to the fuse and alarm panels.

The two BDFBs enable duplication of the power supply to the system to operate in the event one battery plant fails (except where there is only one battery plant).

## Remote Complex

The DACS IV-2000 Remote Complexes are configured to accept two power supply arrangements: standard or duplex. The standard configuration consists of one BDFB powered from a single Lineage 2000 (or equivalent) battery plant. The standard configuration was the only configuration available for (256) systems up to Release 4.0. The Release 4.0 and 5.0 (256) systems include an option for duplex power. The duplex configuration allows the Remote Complex to be powered from one or two Lineage 2000 (or equivalent) battery plants.

### Standard Power Configuration

In the standard configuration, the Remote Complexes operate with a Lineage 2000 (or equivalent) battery plant (-48 Vdc nominal) in a central office environment.

Seven power feeders and seven returns are terminated at the OPEX Bay and provide power for the entire Remote Complex. The feeders are designated by the loads they serve: A, B, C, D, E, F, and G. Each load is fused separately.

- Feeders A, B, C, D, and E (connected through the Fuse and Alarm Panel) supply power to the facility interface bays, the OPEX PWR Module, and the fan assemblies.
- Feeders F and G (connected directly to the RUI PWR Module) supply power to the RUI PWR Module.

## Duplex Power Configuration

The duplex power feature provides compatibility with the "red and blue" central office power distribution being deployed in the AT&T Network, and with other power-distribution arrangements. The duplex power feature uses one or two -48V diverse power plants. (A diverse power plant is one that does not share common components, such as rectifiers, batteries, BDFBs, and cable racks.)

Twelve power feeders (A1 through F1 and A2 through F2) and twelve returns are terminated at the OPEX Bay and provide power for the entire Remote Complex. The red battery plant supplies A, B, and E; the blue battery plants supplies C, D, and F. All power feeders are connected to the Fuse and Alarm Panel.

When the Remote Complex is powered using two battery plants, the following requirements apply:

- Power feeders to the Remote Complex must be placed in two groups to allow connection to two separate BDFBs.
- Two battery plants (red and blue) are required.
- Feeders A, B, and E are fed from the red battery plant; feeders C and D are fed from the blue battery plant.

Loss of one battery plant or one group of feeders connected to that plant does not cause any loss of service (except where there is only one battery plant supplying power).

## Power Dissipation

The power dissipation of the DACS IV-2000 bays conforms to Bellcore TR-NWT-000063, *Network Equipment-Building System (NEBS) Generic Equipment Requirements* (Issue 5, September 1993).

The power specification requirements for fully equipped bays with an input voltage range of -40.5V to -60V are shown in Table A-19.

Table A-19. **Power Dissipation**

| Bay | Value | |
|---|---|---|
| | Collocated System | System with Remote Complex |
| Switch Complex (Main Controller, two Switch Bays) | 4909 watts | 5400 watts |
| OPEX Bay | — | 1000 watts |
| Enhanced DS1 Interface Bay | 685 watts | 685 watts |
| DS3 Interface Bay | 597 watts | 597 watts |
| Enhanced STS1/DS3 Interface Bay | 1144 watts | 1144 watts |
| Enhanced STS1/DS3/DS1 Interface Bay | 911 watts | 911 watts |

**Notes:**

1. These values conform to TR-NWT-000063, *Network Equipment-Building Systems (NEBS) Generic Equipment Requirements* (Issue 5, September 1993).

# Physical Specifications

The physical specifications for the DACS IV-2000 are shown in Table A-20. The floor load from the frames (excluding cable distribution system) averaged across the associated floor area does not exceed 115 lb/ft$^2$.

Table A-20. **Physical Characteristics**

| Item | Value |
|---|---|
| Framework Type | Network Bay |
| Physical Dimensions Collocated arrangement | Up to 23 bay positions, or 21 standard bays: 26 in. (W) x 84 in. (H) x 12 in. (D) |
| Physical Dimensions Remote Complex | Up to 9 standard bay positions: 26 in. (W) x 84 in. (H) x 12 in. (D) |
| Fuse and Alarm Bay | 13 in. (W) x 84 in. (H) x 12 in. (D); 200 lb. |
| Switch Complex (Main Controller, two Switch Bays) | 2090 lb. |
| OPEX Bay | 450 lb. |
| Enhanced DS1 Interface Bay | 450 lb. |
| DS3 Interface Bay | 450 lb. |
| Enhanced STS1/DS3 Interface Bay | 450 lb. |
| Enhanced STS1/DS3/DS1 Interface Bay | 450 lb. |
| Floor Load (excluding cable distribution) | Conforms to TR-NWT-000063 |
| Maintenance Aisle, Front (minimum width) | 30 in. |
| Wiring Aisle, Rear (minimum width) | 24 in. |
| Maximum Shipping Size (packaged) | 90 in. (W) x 100 in. (H) x 46 in. (D) |

# Environmental Specifications

The environmental specifications for the DACS IV-2000 include the thermal characteristics; handling and transportation requirements; and earthquake, acoustical noise, electromagnetic compatibility (EMC), and electrostatic discharge (ESD) specifications. These environmental specifications conform to Bellcore TR-NWT-000063 *Network Equipment-Building System (NEBS) Generic Equipment Requirements (Issue 5, September 1993)* and TR-NWT-001089, *Electromagnetic Compatibility and Electrical Safety Generic Criteria for Network Telecommunications Equipment* (Issue 2, June 1993).

## Ambient Characteristics

The DACS IV-2000 remains operational within the following room ambient temperature and humidity limits.

Room ambient refers to conditions at a location 5 feet above the floor and 15 inches in front of the equipment. Short term refers to a period of not more than 72 consecutive hours and a total of not more than 15 days in one year. Relative humidity must be less than 68 percent for ambient temperatures above 95°F. At the short-term emergency condition of 120°F, the relative humidity must be below 20 percent.

The DACS IV-2000 remains operational when installed in central offices located from 200 feet below sea level to 13,000 feet above sea level.

The DACS IV-2000 environmental characteristics are summarized in Table A-21.

Table A-21. **Environmental Characteristics**

| Item | Value |
|---|---|
| Normal Operating Temperature Range | +40° to +100°F (4.4° to 37.8°C) |
| Minimum Short-Term Temperature | +35°F (1.6°C) |
| Maximum Short-Term Temperature | +120°F (48.8°C) |
| Maximum Rate of Temperature Change | 15°F (8.4°C) per hour |
| Operating Relative Humidity | 20 to 55% |
| Minimum Short-Term Relative Humidity | 10% |
| Maximum Short-Term Relative Humidity | 80% and < 0.024 lb of water/lb of dry air |

Table continued on next page.

Table A-21. **Environmental Characteristics (Continued)**

| Item | Value |
|---|---|
| Operational Altitude | From 200 ft below to 13,000 ft above sea level |
| Equipment Cooling | Forced Convection |
| Fire Resistance and Dust | Conforms to TR-NWT-000063 |
| Standard Heat Dissipation | Conforms to TR-NWT-000063 |

## Handling and Transportation

The DACS IV-2000 meets the shock, vibration, temperature, and relative humidity requirements specified in TR-NWT-000063, *Network Equipment-Building System (NEBS) Generic Equipment Requirements* (Issue 5, September 1993) for handling and transportation. (See Table A-22.)

Table A-22. **Handling and Transportation Specifications**

| Item | Value |
|---|---|
| Vibration and Shock Design Criteria | Conforms to TR-NWT-000063 |
| Temperature for Transportation/ Storage | Conforms to TR-NWT-000063 |
| Relative Humidity for Transportation/ Storage | Conforms to TR-NWT-000063 |
| Altitude for Storage/Shipment | Up to 40,000 ft, conforming to TR-NWT-000063 |

## Earthquake, Acoustical Noise, EMI, and ESD

The DACS IV-2000 meets the earthquake and office vibration criteria for zone 4 earthquake protection specified in TR-NWT-000063, Issue 5. It meets the acoustical noise limits specified for CO indoor telephone equipment in TR-NWT-000063, *Network Equipment-Building System (NEBS) Generic Equipment Requirements* (Issue 5, September 1993).

The design techniques for the DACS IV-2000 minimize emissions for an open frame design. The objective is to conform to the emission and immunity EMC limits as outlined in Part 15, Subpart J, of the FCC rules for Class A Computing Devices; see TR-NWT-000063, *Network Equipment-Building System (NEBS)*

*Generic Equipment Requirements* (Issue 5, September 1993) and TR-NWT-001089, *Electromagnetic Compatibility and Electrical Safety Generic Criteria for Network Telecommunications Equipment* (Issue 2, June 1993).

The DACS IV-2000 is designed to meet the ESD requirements specified in TR-NWT-001089, *Electromagnetic Compatibility and Electrical Safety Generic Criteria for Network Telecommunications Equipment* (Issue 2, June 1993).

ESD grounding connections are provided on the front and rear of each bay, and the use of wrist straps is required. EMI enclosures are required for the DACS IV-2000 to be fully compliant with EMC limits and ESD requirements.

The earthquake, acoustical noise, EMC, and ESD specifications are shown in Table A-23.

Table A-23. **Earthquake, Acoustical Noise, EMC, and ESD Specifications**

| Item | Value |
|---|---|
| Earthquake and Office Vibration | Conforms to TR-NWT-000063 |
| Acoustical Noise Limits under Normal Operating Temperatures | < 60 dBA<br>Conforms to TR-NWT-000063 |
| Electromagnetic Compatibility (EMC) with EMI Enclosures | Conforms to TR-NWT-001089, Part 15, Subpart J, *Class A Computing Devices* |
| Electrostatic Discharge (ESD) with EMI Enclosures | Conforms to TR-NWT-001089 |

# Availability and Reliability Specifications

Availability and reliability can be defined in terms of the following three components, which are described in this section and summarized in Table A-23.

- Mean time between failures
- Mean time between maintenance activities for the equipment
- Quality and reliability of the software.

## Mean Time Between Failures

Mean Time Between Failures (MTBF) indicates the frequency of service-affecting failures within the DACS IV-2000. The specifications are greater than 9000 years per DS3/STS1 and greater than 17,000 years per DS1. The outage time is less than 0.013 minute per year per DS3/STS1, and less than 0.007 minute per year per DS1, as specified in Bellcore TA-NWT-000233, *Wideband and Broadband Digital Cross-Connect Systems Generic Criteria* (Issue 1, November 1993) and TA-NWT-001339, *General Reliability Requirements for Digital Cross-Connect Systems* (Issue 1, November 1993).

## Mean Time Between Maintenance Activities

Reliability is specified in terms of Mean Time Between Maintenance Activities (MTBMA), which indicates the frequency of failures within the DACS IV-2000. This is a measurement of how often a maintenance activity occurs and includes both service-affecting and non-service-affecting failures. The MTBMA is greater than 3000 hours for a fully equipped DACS IV-2000 standard bay. The MTBMA specified in Table A-24 is for fully equipped standard bays and depends on bay type. The MTBMA, MTBF, and outage time are based on 2 hours Mean Time To Repair (MTTR) as specified in Bellcore TA-NWT-000233, *Wideband and Broadband Digital Cross-Connect Systems Generic Criteria* (Issue 1, November 1993) and TA-NWT-001339, *General Reliability Requirements for Digital Cross-Connect Systems* (Issue 1, November 1993).

## Software Quality and Reliability

The software quality criteria conform to Bellcore TR-TSY-000179, *Software Quality Program Generic Requirements* (SQPR) (Issue 2, June 1993).

The software reliability criteria conform to Bellcore TA-TSY-000282, *Software Reliability and Quality Acceptance Criteria (SRQAC)* (Issue 1, December 1986).

The reliability prediction procedures conform to Bellcore TR-NWT-000332, *Reliability Prediction Procedure For Electronic Equipment* (Issue 4, December 1992).

Table A-24. **Availability and Reliability Specifications**

| Item | Value | |
|---|---|---|
| | Collocated System | System with One Remote Complex |
| MTBF (per DS1) | 17,000 years | 17,000 years |
| MTBF (per DS3/STS1) | 9000 years | 9000 years |
| Outage Time (per DS1) | 0.0107 min/year; better than TA-NWT-001339 | 0.0339 min/year; better than TA-NWT-001339 |
| Outage Time (per DS3) | 0.0167 min/year; better than TA-NWT-001339 | 0.0397 min/year; better than TA-NWT-001339 |
| Outage Time (per DS3/STS1 to DS3/STS1) | 0.0173 min/year; better than TA-NWT-001339 | 0.0405 min/year; better than TA-NWT-001339 |
| Outage Time (per STS1) | 0.0167 min/year; better than TA-NWT-001339 | 0.0399 min/year; better than TA-NWT-001339 |
| MTBMA Switch Bay (fully equipped) | 5840 hours | 5840 hours |
| MTBMA STS1/DS3 Interface Bay (fully equipped) | 4112 hours | 4112 hours |
| MTBMA STS1/DS3/DS1 Interface Bay (fully equipped) | 3793 hours | 3793 hours |
| MTBMA DS1 Interface Bay (fully equipped) | 5211 hours | 5211 hours |
| MTBMA STS1/DS3 Interface Bay (fully equipped) | 4112 hours | 4112 hours |
| MTTR | 2 hours | 2 hours |
| Reliability Prediction Procedure | Conforms to TR-NWT-000332 | Conforms to TR-NWT-000332 |

# Alarm, Scan, and Control Points

# B

## Contents


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# Contents

# Alarm, Scan, and Control Points

# B

This appendix is provided to describe the interface between the DACS IV-2000 and telemetry operations systems (OSs). The AS&C points are used with administrative links (CILINKs 1-4 and 2-4). CILINKs 1-4 and 2-4 support the TABS (telemetry asynchronous block serial) protocol as defined in AT&T Compatibility Bulletin No. 149 entitled *Maintenance Standards for Digital Transmission Standards, Issue 3.* TABS protocol uses a polling format between the telemetry system and the DACS IV-2000 with the telemetry system initiating all communications by sending a request message to the DACS IV-2000 during each poll cycle. The system responds by sending the surveillance (or scan) point to the telemetry remote. The TABS protocol supports both point-to-point and multipoint architectures. CILINKs 1-4 and 2-4 are used as a dedicated links. When using a General Telemetry Processor (GTP), the GTP must be connected to link 4 of the master ECI circuit pack at all times. If both ECI circuit packs are available, ECI-1 is the master ECI on system reset.

## Types of AS&C Points

Point is a term which is used to describe a single element of binary information. Physically, an AS&C point can be a single bit position in a serial telemetry message or it can be a discrete relay contact closure. Functionally, three distinct classes of AS&C points exist as follows:

- Alarm Points — provide the telemetry remote with information concerning alarm conditions existing within the DACS IV-2000. This information is available as both dedicated binary bit positions in the telemetry messages (sent by the DACS IV-2000 to the telemetry remote) and also as a set of discrete relay closures.
- Scan Points — provide the telemetry remote with status information concerning the DACS IV-2000. This information is available as dedicated binary bit positions in the telemetry messages (sent by the DACS IV-2000 to the telemetry remote).
- Control Points — provide the telemetry remote with operational control of certain aspects of the DACS IV-2000. This information is available as dedicated binary bit positions in the telemetry messages (received by the DACS IV-2000 from the telemetry remote).

## Alarm Points via Relay Closures

Alarm points are provided, through relay closures, to telemetry remote equipment accepting discrete inputs (for example, the General Telemetry Processor [GTP]). The relay closures provide the same alarm information to the OS as is available locally through the office alarms. The DACS IV-2000 software supports relay closures for critical, major, and minor alarms. The conditions for activating each type of alarm point are:

- Critical Alarm (CR) — is set on the occurrence of a severe, service-affecting condition which requires immediate corrective action regardless of time-of-day or day-of-the-week.
- Major Alarm (MJ) — is set whenever there are one or more service-affecting failures or whenever failures which can mask service-affecting failures (for example, main controller failures).
- Minor Alarm (MN) — is set whenever there are one or more non-service-affecting failures exist, or when certain manually initiated functions (for example, manual protection switches are in effect).

## Scan and Control Displays

The serial telemetry data is broken down into logical groups of 64 points each, called *displays*. This grouping, in general, conforms to the manner in which the data is shown on a terminal, with one display presenting a single terminal screen full of data. There are two types of displays:

- Scan — transmitted by the DACS IV-2000, consists of combinations of alarm and scan points. Scan point indications for momentary conditions (for example, an intermittent failure) are stretched to a minimum duration of

20 seconds to ensure that the conditions are sensed by the telemetry system. The 64th scan point in a display is reserved to indicate to the telemetry remote that serial link errors have occurred.

- Control — received by the DACS IV-2000, consists of control points from a remote site. Through the use of control points, certain aspects of system operation can be controlled by a remote site.

The DACS IV-2000 has the flexibility to support three levels of display sets:

- Summary — providing system level alarms and status identifying:
  - — Type of equipment or facility failure
  - — Presence of a protection switch or of a inhibition of protection switching (that is, lock-out) in a specific type of module

  This set does not indicate the specific facilities, equipment, or modules affected. The primary application for the summary set is as a backup source of alarm data when a message Operations System [OS] (for example, SCCS) is used as the primary source of alarm data.
- Detailed — providing expanded information which identifies the particular module(s) experiencing a problem and usually containing information to isolate a failure to the circuit pack level. This set also allows remote control of manual protection switching and the inhibition or the locking of protection switching. Selecting the detailed set automatically includes the transmission of the summary set.
- Extended Facility — providing additional circuit pack and interface port information, particularly on the DS1 facility level, on the VT1.5 facility level, on out-of-frame (OOF) conditions on DS2s within DS3 facilities, on DS3 input format mismatches, and on EC-1 facility conditions. For STS1 (modules 1-32), DS3 (modules 9-32), and DS1 (modules 33-64) Interface Modules there are control points included in the extended facility set. In addition, for DS3 (modules 9-32) and DS1 (modules 33-64) Interface Modules and Switch Input/Output (modules 3 and 4) Modules, the extended facility set includes detailed set information (scan and control points). Selecting the extended facility set automatically includes the transmission of the summary and detailed sets. The choice of alarm sets is made by you when the telemetry link (CILINK-1-4 and CILINK-2-4) is provisioned. The display sets are described in the following sections.

## Summary Display Set

The summary display set provides the OS with data on the severity of the failure and the type of module that indicates the failure. Failures are identified as either non-service affecting (NSA) or service affecting (SA) as specified in Bell Communications Research TA-NWT-000474, Issue 1, or without an indication of the specific facilities affected or the circuit packs responsible for the failure. The main controller failure (MC:FAIL or OOS) point indicates failure(s) in the control complexes (CCs) circuit packs are preventing the execution of system control functions. The point HCC:FAIL or OOS indicates a failure with CC-0 and/or CC-1. Failure of one of the ECI circuit packs is indicated by ECI:FAIL or OOS. Failures of the primary (PRI) and secondary (SEC) backup memories or the secondary storage controller (SSC) are indicated with separate alarm points and are therefore not included in the MC FAIL alarm point. The `SYNC Reference:FAIL NSA` point indicates the presence of a NSA failure of one or both synchronizer timing references.

Scan points indicate if any protection groups are switched to protection or have protection locked (either manually or as a result of an autolock). The type of module is specified, but not the specific protection group affected. If the equipment is in an abnormal state as a result of a manual control (for example, locking or forcing of protection switching), this is indicated by setting a scan point for *manual function initiated.* Failure of any frame audit that results in an autonomous message over the Snider and X.25 links also sets the Frame Audit Failure scan point for one polling cycle.

No control points are associated with the summary set. Table B-1 lists the summary set scan points.

Table B-1. **Summary Display Set Scan Points**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 0 | 1 | A | MC Fail or OOS |
| | 2 | A | PRI Fail or OOS |
| | 3 | A | SEC Fail or OOS |
| | 4 | A | MC/OPEX/RUI Power Fail SA |
| | 5 | A | MC/OPEX/RUI Power Fail NSA |
| | 6 | A | Clock Hardware Fail SA |
| | 7 | A | Clock Hardware Fail NSA |
| | 8 | A | SWCS Fail SA |
| | 9 | A | SWCS Fail NSA |
| | 10 | A | SWIO/OPEX Fail SA |
| | 11 | A | SWIO/OPEX Fail NSA |
| | 12 | A | DS1 Interface Module UC Fail or OOS |
| | 13 | A | DS1 Interface Module Power Fail |
| | 14 | A | HCC/RUI Fail or OOS |
| | 15 | A | DS1 Interface Module CLKDR Fail SA |
| | 16 | A | DS1 Interface Module CLKDR Fail NSA |
| | 17 | A | DS1IF/SWIF/DS1RY Fail SA |
| | 18 | A | DS1IF/SWIF/PMGR1 Fail NSA |
| | 19 | A | Incoming DS3/STS-1 Fail |
| | 20 | A | Multiple Incoming DS3/STS-1 Fail |
| | 21 | A | DS3/STS1 Interface Module UC Fail or OOS |
| | 22 | A | DS3/STS1 Interface Module Power Fail |
| | 23 | A | ECI Fail or OOS |
| | 24 | A | DS3/STS1 Interface Module CLKDR Fail SA |
| | 25 | A | DS3/STS1 Interface Module CLKDR Fail NSA |
| | 26 | A | MUX/SMUX Fail SA |

* A = Alarm
S = Scan

† There is one display per system.

Table continued on next page.

Table B-1. **Summary Display Set Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 0 | 27 | A | MUX/PMGR1/SMUX Fail NSA |
| | 28 | A | Fan Fail |
| | 29 | A | Switch Module Manual Function Initiated |
| | 30 | A | DS1 Interface Module Manual Function Initiated |
| | 31 | A | DS3/STS1 Interface Module Manual Function Initiated |
| | 32 | A | Time of Day Clock Fail |
| | 33 | S | SWCS Protection Switch Active |
| | 34 | S | SWCS Protection Switch Locked |
| | 35 | S | SWCS Protection Switch Auto-Locked |
| | 36 | S | SWIO Protection Switch Active |
| | 37 | S | SWIO Protection Switch Locked |
| | 38 | S | SWIO Protection Switch Auto-Locked |
| | 39 | A | SYNC Reference Fail NSA |
| | 40 | S | DS1IF Protection Switch Active |
| | 41 | S | DS1IF Protection Switch Locked |
| | 42 | S | DS1IF Protection Switch Auto-Locked |
| | 43 | S | Incoming DS1 Fail |
| | 44 | S | Multiple Incoming DS1s Fail |
| | 45 | - | Unassigned |
| | 46 | S | MUX/SMUX Protection Switch Active |
| | 47 | S | MUX/SMUX Protection Switch Locked |
| | 48 | S | MUX/SMUX Protection Switch Auto-Locked |
| | 49 | S | CILINK-{1,2}-{7,8} OOS or Lock-Out |
| | 50 | S | CILINK-1-4 OOS or Lock-Out |
| | 51 | S | Transfer to SEC Fail |

* A = Alarm
S = Scan

† There is one display per system.

Table continued on next page.

Table B-1. **Summary Display Set Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 0 | 52 | A | Frame Audit Fail |
| | 53 | S | CILINK-1-1 OOS or Lock-Out |
| | 54 | S | CILINK-1-2 OOS or Lock-Out |
| | 55 | S | CILINK-1-3 OOS or Lock-Out |
| | 56 | S | CILINK-1-5 OOS or Lock-Out |
| | 57 | S | CILINK-1-6 OOS or Lock-Out |
| | 58 | S | CILINK-2-1 OOS or Lock-Out |
| | 59 | S | CILINK-2-2 OOS or Lock-Out |
| | 60 | S | CILINK-2-3 OOS or Lock-Out |
| | 61 | S | CILINK-2-4 OOS or Lock-Out |
| | 62 | S | CILINK-2-5 OOS or Lock-Out |
| | 63 | S | CILINK-2-6 OOS or Lock-Out |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There is one display per system.

## Detailed Display Set

Most applications that use the telemetry AS&C points as the primary source of maintenance data need more detail than is provided by the summary set. The following paragraphs describe the functions provided by the detailed AS&C points and include tables with the specific scan and control points needed for each product.

Most equipment failures are identified by the specific affected circuit pack. The failures are specified as either NSA or SA as specified in Bell Communications Research TA-NWT-000474, Issue 1. An NSA alarm indicates the failure of a circuit pack that does not affect service, such as a controller, or a failure that resulted in a successful protection switch to restore service. In the latter case, a scan point is provided to indicate the state of the protection switch. SA alarms indicate failures that result in service being lost.

The DACS IV-2000 can distinguish between equipment failures and incoming facility failures. Incoming DS3 failures are assigned individual alarm points, while incoming DS1 failures are indicated by a multiple scan point that specifies the affected module but not the individual DS1.

Terminating DS3 facilities have four alarm points[1] per DS3. The first alarm point indicates a loss-of-signal (LOS) or high bit error rate (BER) condition. The BER can be determined through either bipolar violations (BPVs), which is the default, or by monitoring DS3 parity errors. The alarm point is set when the BER exceeds the threshold of $10^{-3}$ (default) through $10^{-9}$ as provisioned. The second alarm point indicates an out-of-frame (OOF) condition. Under LOS or when the BER is high enough to cause an OOF, both alarm points are set. The other two alarm points indicate detection of incoming DS3 alarm indication signal (AIS) and detection of incoming DS3 idle signal.

The DS1 facilities associated with the DS1 Interface Module have two scan points indicating that one or more of the incoming DS1 signals to the module have either an LOS condition or a BER that exceeds the threshold of $10^{-3}$ (default) through $10^{-9}$ as determined by monitoring BPVs.

Control points allow manual protection switching of individual circuit packs and permit inhibiting (lockout) protection switching. Three controls are provided:

- Make protection switch — transfers service to the protection circuit pack if it is available and good and locks it in that state. This control has no effect if service on the indicated circuit pack is already on protection, if protection is unavailable, or if protection is inhibited (locked).
- Lock protection — inhibits service from being transferred to the protection circuit pack. In this state, no automatic switch to protection occurs if the service circuit pack is diagnosed as bad.
- Unlock protection — allows manual or automatic protection switching on the indicated circuit pack. If a manual protection switch has been made on a *good* circuit pack, the unlock control allows the DACS IV-2000 to release the switch. No control point is provided to force a circuit pack into the unprotected state if it is in the protected state and diagnosed as bad.

For each control, a corresponding scan point is provided to allow verification that the action specified by the control was completed.

Tables B-2 through B-14 define the scan and control points required for each module or assembly of the DACS IV-2000. Scan points are divided by type into alarm and scan points, and alarm points are further designated as either NSA or SA.

## HCC, SYNC, SWIO, SWCS, RUI, and OPEX Modules

Tables B-2 and B-3 list the detailed High Capacity Controller, Synchronizer, Switch Input/Output, Switch Center Stage, Remote Unit Interface, and Optical Extension Module scan and control points, respectively.

1. An additional alarm point is provided in the extended display set for DS3 format mismatches. Refer to the section titled "Extended Facility Display Sets" (page B-29) for more information on the extended display sets.

Table B-2. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Scan Points**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1 | A | MC Fail |
| | 2 | A | PRI-1 Fail |
| | 3 | A | SEC Fail |
| | 4 | A | OPEX-1 Power Fail SA |
| | 5 | A | OPEX-1 Power Fail NSA |
| | 6 | A | RUI-1 Power Fail NSA |
| | 7 | A | CLKGN Fail SA |
| | 8-9 | A | CLKGN-{0,1} Fail NSA |
| | 10 | A | Frame Audit Fail |
| | 11 | A | Fan-1 Fail |
| | 12-27 | A | SWIO-1-{1-16} Fail NSA |
| | 28-43 | A | SWIO-2-{1-16} Fail NSA |
| | 44 | A | Switch Module Manual Function Initiated |
| | 45 | A | Time of Day Clock 1 Fail |
| | 46 | A | CC-1 Fail or OOS |
| | 47 | A | Time of Day Clock 2 Fail |
| | 48 | A | CC-0 Fail or OOS |
| | 49 | S | CILINK-1-7 OOS-MTCE |
| | 50-51 | S | CLKGN-{0,1} Active |
| | 52 | S | CILINK-1-7 OOS-FLT, Protocol, or Lock-Out |
| | 53 | S | Transfer to SEC Fail |
| | 54 | S | CILINK-1-1 OOS-MTCE |
| | 55 | S | CILINK-1-2 OOS-MTCE |
| | 56 | S | CILINK-1-3 OOS-MTCE |
| | 57 | S | CILINK-1-5 OOS-MTCE |

* A = Alarm
S = Scan

† There are six displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-2. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 58 | S | CILINK-1-6 OOS-MTCE |
| | 59 | S | CILINK-1-4 OOS-MTCE |
| | 60-61 | A | ECI-{1,2} Fail or OOS |
| | 62-63 | S | SYNC-{0,1} Active |
| | 64 | - | Reserved |
| 2 | 1-16 | A | SWIO--1-{1-16} Fail SA |
| | 17-32 | A | SWIO--2-{1-16} Fail SA |
| | 33 | A | SWCS-1-16 Fail SA |
| | 34-39 | S | CILINK-1-{1-6} OOS-FLT, Protocol, or Lock-Out |
| | 40-45 | S | CILINK-2-{1-6} OOS-MTCE |
| | 46-51 | S | CILINK-2-{1-6} OOS-FLT, Protocol, or Lock-Out |
| | 52 | A | TBS3 Fail SA |
| | 53-54 | A | TBS3-{0,1} Fail NSA |
| | 55 | A | DPLL Fail SA |
| | 56-57 | A | DPLL-{0,1} Fail NSA |
| | 58-59 | - | Unassigned |
| | 60 | S | CILINK-1-8 OOS-MTCE |
| | 61 | S | CILINK-1-8 OOS-FLT, Protocol, or Lock-Out |
| | 62 | - | Unassigned |
| | 63 | A | PRI-2 Fail or OOS |
| | 64 | - | Reserved |
| 3 | 1-16 | S | SWIO-1-{1-16} Protection Switch Active |
| | 17-32 | S | SWIO-2-{1-16} Protection Switch Active |
| | 33-35 | A | Fan-{2-4} Fail |

* A = Alarm
S = Scan

† There are six displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-2. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 3 | 36 | A | Fan-6 Fail |
| | 37-38 | A | DS1TX-{0,1} Fail NSA |
| | 39 | S | CILINK-2-7 OOS-MTCE |
| | 40 | S | CILINK-2-7 OOS-FLT, Protocol, or Lock-Out |
| | 41 | A | SYNCPRI-0 (DS1TX-0) Primary Reference Fail NSA |
| | 42 | A | SYNCSEC-0 (DS1TX-0) Secondary Reference Fail NSA |
| | 43 | A | SYNCPRI-1 (DS1TX-1) Primary Reference Fail NSA |
| | 44 | A | SYNCSEC-1 (DS1TX-1) Secondary Reference Fail NSA |
| | 45 | S | CILINK-2-8 OOS-MTCE |
| | 46 | S | CILINK-2-8 OOS-FLT, Protocol, or Lock-Out |
| | 47 | A | SYNC Mode Fail NSA |
| | 48-50 | A | Fan-{7-9} Fail |
| | 51-53 | A | Fan-{11-13} Fail |
| | 54-57 | A | Fan-{15-18} Fail |
| | 58-61 | A | Fan-{20-23} Fail |
| | 62-63 | S | Reserved |
| | 64 | - | Reserved |
| 4 | 1-16 | S | SWIO Pair {1-16} Protection Switch Auto-Locked |
| | 17-48 | S | SWIO-{1-32} Protection Switch Locked |
| | 49 | A | MC OOS-MCOND |
| | 50-51 | A | CC-{0,1} OOS-MTCE |

* A = Alarm
S = Scan

† There are six displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-2. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 4 | 52 | A | PRI-1 OOS-MTCE |
| | 53 | - | Reserved |
| | 54 | A | PRI-2 OOS-MTCE |
| | 55-56 | - | Reserved |
| | 57-58 | A | RUI-{1,2} OOS-FLT |
| | 59-60 | A | RUI-{1,2} OOS-MTCE |
| | 61-62 | A | RUI-{1,2} OOS-FEF |
| | 63 | - | Unassigned |
| | 64 | - | Reserved |
| 5 | 1-15 | A | SWCS-1-{1-15} Fail SA |
| | 16-31 | A | SWCS-2-{1-16} Fail SA |
| | 32-47 | A | SWCS-1-{1-16} Fail NSA |
| | 48-63 | A | SWCS-2-{1-16} Fail NSA |
| | 64 | - | Reserved |
| 6 | 1 | S | SWCS Protection Auto-Locked |
| | 2-17 | S | SWCS-1-{1-16} Protection Switch Active |
| | 18-32 | S | SWCS-2-{1-15} Protection Switch Active |
| | 33-48 | S | SWCS-1-{1-16} Protection Switch Locked |
| | 49-63 | S | SWCS-2-{1-15} Protection Switch Locked |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are six displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table B-3. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Control Points**

| Display † | Point No. | Description |
|---|---|---|
| 1 | 1-2 | CLKGN-{0,1} Make CLKGN Active |
| | 3-4 | SYNC-{0,1} Make SYNC Active |
| | 5 | SYNCPRI-0 Make Timing Reference Active |
| | 6 | SYNCSEC-0 Make Timing Reference Active |
| | 7-22 | SWIO-4-{1-16} Make Protection Switch |
| | 23 | SYNCPRI-1 Make Timing Reference Active |
| | 24 | SYNCSEC-1 Make Timing Reference Active |
| | 25-63 | Unassigned |
| | 64 | Reserved |
| 2 | 1-16 | SWIO-1-{1-16} Make Protection Switch |
| | 17-32 | SWIO-2-{1-16} Make Protection Switch |
| | 33-48 | SWIO-3-{1-16} Make Protection Switch |
| | 49-63 | Unassigned |
| | 64 | Reserved |
| 3 | 1 | SWIO-1-1 Lock Protection |
| | 2 | SWIO-1-1 Unlock Protection |
| | 3 | SWIO-1-2 Lock Protection |
| | 4 | SWIO-1-2 Unlock Protection |
| | 5 | SWIO-1-3 Lock Protection |
| | 6 | SWIO-1-3 Unlock Protection |
| | 7 | SWIO-1-4 Lock Protection |
| | 8 | SWIO-1-4 Unlock Protection |
| | 9 | SWIO-1-5 Lock Protection |
| | 10 | SWIO-1-5 Unlock Protection |
| | 11 | SWIO-1-6 Lock Protection |
| | 12 | SWIO-1-6 Unlock Protection |
| | 13 | SWIO-1-7 Lock Protection |

† There are five displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-3. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| | 14 | SWIO-1-7 Unlock Protection |
| | 15 | SWIO-1-8 Lock Protection |
| | 16 | SWIO-1-8 Unlock Protection |
| | 17 | SWIO-1-9 Lock Protection |
| | 18 | SWIO-1-9 Unlock Protection |
| | 19 | SWIO-1-10 Lock Protection |
| | 20 | SWIO-1-10 Unlock Protection |
| | 21 | SWIO-1-11 Lock Protection |
| | 22 | SWIO-1-11 Unlock Protection |
| | 23 | SWIO-1-12 Lock Protection |
| | 24 | SWIO-1-12 Unlock Protection |
| | 25 | SWIO-1-13 Lock Protection |
| | 26 | SWIO-1-13 Unlock Protection |
| 3 | 27 | SWIO-1-14 Lock Protection |
| | 28 | SWIO-1-14 Unlock Protection |
| | 29 | SWIO-1-15 Lock Protection |
| | 30 | SWIO-1-15 Unlock Protection |
| | 31 | SWIO-1-16 Lock Protection |
| | 32 | SWIO-1-16 Unlock Protection |
| | 33 | SWIO-2-1 Lock Protection |
| | 34 | SWIO-2-1 Unlock Protection |
| | 35 | SWIO-2-2 Lock Protection |
| | 36 | SWIO-2-2 Unlock Protection |
| | 37 | SWIO-2-3 Lock Protection |
| | 38 | SWIO-2-3 Unlock Protection |
| | 39 | SWIO-2-4 Lock Protection |
| | 40 | SWIO-2-4 Unlock Protection |

† There are five displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-3. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| 3 | 41 | SWIO-2-5 Lock Protection |
| | 42 | SWIO-2-5 Unlock Protection |
| | 43 | SWIO-2-6 Lock Protection |
| | 44 | SWIO-2-6 Unlock Protection |
| | 45 | SWIO-2-7 Lock Protection |
| | 46 | SWIO-2-7 Unlock Protection |
| | 47 | SWIO-2-8 Lock Protection |
| | 48 | SWIO-2-8 Unlock Protection |
| | 49 | SWIO-2-9 Lock Protection |
| | 50 | SWIO-2-9 Unlock Protection |
| | 51 | SWIO-2-10 Lock Protection |
| | 52 | SWIO-2-10 Unlock Protection |
| | 53 | SWIO-2-11 Lock Protection |
| | 54 | SWIO-2-11 Unlock Protection |
| | 55 | SWIO-2-12 Lock Protection |
| | 56 | SWIO-2-12 Unlock Protection |
| | 57 | SWIO-2-13 Lock Protection |
| | 58 | SWIO-2-13 Unlock Protection |
| | 59 | SWIO-2-14 Lock Protection |
| | 60 | SWIO-2-14 Unlock Protection |
| | 61 | SWIO-2-15 Lock Protection |
| | 62 | SWIO-2-15 Unlock Protection |
| | 63 | SWIO-2-16 Lock Protection |
| | 64 | Reserved |
| 4 | 1-16 | SWCS-1-{1-16} Switch to Protection |
| | 17-32 | SWCS-2-{1-16} Switch to Protection |
| | 33-63 | Unassigned |

† There are five displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-3. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| 4 | 64 | Reserved |
| 5 | 1 | SWCS-1-1 Lock Protection |
| | 2 | SWCS-1-1 Unlock Protection |
| | 3 | SWCS-1-2 Lock Protection |
| | 4 | SWCS-1-2 Unlock Protection |
| | 5 | SWCS-1-3 Lock Protection |
| | 6 | SWCS-1-3 Unlock Protection |
| | 7 | SWCS-1-4 Lock Protection |
| | 8 | SWCS-1-4 Unlock Protection |
| | 9 | SWCS-1-5 Lock Protection |
| | 10 | SWCS-1-5 Unlock Protection |
| | 11 | SWCS-1-6 Lock Protection |
| | 12 | SWCS-1-6 Unlock Protection |
| | 13 | SWCS-1-7 Lock Protection |
| | 14 | SWCS-1-7 Unlock Protection |
| | 15 | SWCS-1-8 Lock Protection |
| | 16 | SWCS-1-8 Unlock Protection |
| | 17 | SWCS-1-9 Lock Protection |
| | 18 | SWCS-1-9 Unlock Protection |
| | 19 | SWCS-1-10 Lock Protection |
| | 20 | SWCS-1-10 Unlock Protection |
| | 21 | SWCS-1-11 Lock Protection |
| | 22 | SWCS-1-11 Unlock Protection |
| | 23 | SWCS-1-12 Lock Protection |
| | 24 | SWCS-1-12 Unlock Protection |
| | 25 | SWCS-1-13 Lock Protection |
| | 26 | SWCS-1-13 Unlock Protection |

† There are five displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-3. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| | 27 | SWCS-1-14 Lock Protection |
| | 28 | SWCS-1-14 Unlock Protection |
| | 29 | SWCS-1-15 Lock Protection |
| | 30 | SWCS-1-15 Unlock Protection |
| | 31 | SWCS-1-16 Lock Protection |
| | 32 | SWCS-1-16 Unlock Protection |
| | 33 | SWCS-2-1 Lock Protection |
| | 34 | SWCS-2-1 Unlock Protection |
| | 35 | SWCS-2-2 Lock Protection |
| | 36 | SWCS-2-2 Unlock Protection |
| | 37 | SWCS-2-3 Lock Protection |
| | 38 | SWCS-2-3 Unlock Protection |
| | 39 | SWCS-2-4 Lock Protection |
| 5 | 40 | SWCS-2-4 Unlock Protection |
| | 41 | SWCS-2-5 Lock Protection |
| | 42 | SWCS-2-5 Unlock Protection |
| | 43 | SWCS-2-6 Lock Protection |
| | 44 | SWCS-2-6 Unlock Protection |
| | 45 | SWCS-2-7 Lock Protection |
| | 46 | SWCS-2-7 Unlock Protection |
| | 47 | SWCS-2-8 Lock Protection |
| | 48 | SWCS-2-8 Unlock Protection |
| | 49 | SWCS-2-9 Lock Protection |
| | 50 | SWCS-2-9 Unlock Protection |
| | 51 | SWCS-2-10 Lock Protection |
| | 52 | SWCS-2-10 Unlock Protection |
| | 53 | SWCS-2-11 Lock Protection |

† There are five displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-3. **Detailed Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| 5 | 54 | SWCS-2-11 Unlock Protection |
| | 55 | SWCS-2-12 Lock Protection |
| | 56 | SWCS-2-12 Unlock Protection |
| | 57 | SWCS-2-13 Lock Protection |
| | 58 | SWCS-2-13 Unlock Protection |
| | 59 | SWCS-2-14 Lock Protection |
| | 60 | SWCS-2-14 Unlock Protection |
| | 61 | SWCS-2-15 Lock Protection |
| | 62 | SWCS-2-15 Unlock Protection |
| | 63 | SWCS-2-16 Lock Protection |
| | 64 | Reserved |

† There are five displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

## DS1 Interface Modules

Tables B-4 and B-5 list the detailed scan and control points, respectively, for each DS1 Interface and DS1 Interface-Protection Module. The same points are used for both the DS1 Interface and DS1 Interface-Protection Modules. Detailed display sets for modules 33-64 are part of the extended displays sets.

Table B-4. **Detailed Display Set (DS1 INTFC Module) — Scan Points**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1 | A | Power Circuit Pack(s) Fail |
| | 2 | - | Unassigned |
| | 3 | A | UC Fail or OOS |
| | 4 | A | CLKDR Fail SA |
| | 5-6 | A | CLKDR-{1,2} Fail NSA |
| | 7-22 | A | DS1IF-{1-16} Fail SA |
| | 23-38 | A | DS1IF-{1-16} Fail NSA |
| | 39-46 | A | SWIF-{1-8} Fail SA |
| | 47-54 | A | SWIF/PMGR-{1-8} Fail NSA |
| | 55-58 | A | DS1RY-{1-4} Fail SA |
| | 59 | A | SWIO/SWCS Module Manual Function Initiated |
| | 60-63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1 | S | DS1 Incoming Fail |
| | 2 | S | Multiple DS1s Incoming Fail |
| | 3 | - | Unassigned |
| | 4-19 | S | DS1IF-{1-16} Protection Switch Active |
| | 20-35 | S | DS1IF-{1-16} Protection Switch Locked |
| | 36 | S | DS1IF Protection Switch Auto-Locked |
| | 37-63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are two displays per DS1 Interface Module

Table B-5. **Detailed Display Set (DS1 INTFC Module) — Control Points**

| Display † | Point No. | Description |
|---|---|---|
| | 1 | Unassigned |
| | 2 | DS1IF-{1A,1B} Switch to Protection |
| | 3 | Unassigned |
| | 4 | DS1IF-{2A,2B} Switch to Protection |
| | 5 | Unassigned |
| | 6 | DS1IF-{3A,3B} Switch to Protection |
| | 7 | Unassigned |
| | 8 | DS1IF-{4A,4B} Switch to Protection |
| | 9 | Unassigned |
| | 10 | DS1IF-{5A,5B} Switch to Protection |
| | 11 | Unassigned |
| | 12 | DS1IF-{6A,6B} Switch to Protection |
| | 13 | Unassigned |
| 1 | 14 | DS1IF-{7A,7B} Switch to Protection |
| | 15 | Unassigned |
| | 16 | DS1IF-{8A,8B} Switch to Protection |
| | 17-19 | Unassigned |
| | 20 | DS1IF-{1A,1B} Lock Protection |
| | 21 | DS1IF-{1A,1B} Unlock Protection |
| | 22-23 | Unassigned |
| | 24 | DS1IF-{2A,2B} Lock Protection |
| | 25 | DS1IF-{2A,2B} Unlock Protection |
| | 26-27 | Unassigned |
| | 28 | DS1IF-{3A,3B} Lock Protection |
| | 29 | DS1IF-{3A,3B} Unlock Protection |
| | 30-31 | Unassigned |
| | 32 | DS1IF-{4A,4B} Lock Protection |

† There is one display per DS1 Interface Module

Table continued on next page.

Table B-5. **Detailed Display Set (DS1 INTFC Module) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| 1 | 33 | DS1IF-{4A,4B} Unlock Protection |
| | 34-35 | Unassigned |
| | 36 | DS1IF-{5A,5B} Lock Protection |
| | 37 | DS1IF-{5A,5B} Unlock Protection |
| | 38-39 | Unassigned |
| | 40 | DS1IF-{6A,6B} Lock Protection |
| | 41 | DS1IF-{6A,6B} Unlock Protection |
| | 42-43 | Unassigned |
| | 44 | DS1IF-{7A,7B} Lock Protection |
| | 45 | DS1IF-{7A,7B} Unlock Protection |
| | 46-47 | Unassigned |
| | 48 | DS1IF-{8A,8B} Lock Protection |
| | 49 | DS1IF-{8A,8B} Unlock Protection |
| | 50-64 | Unassigned |

† There is one display per DS1 Interface Module

## DS3 Interface Modules

The same points are assigned to the DS3 Interface-16 or DS3 Interface-32 Modules, except that the points referring to MUX number 17-32 or CLKDR number 3-4 are not needed for the DS3 Interface-16 Modules. MUX-16 (DS3 Interface-16 Modules) and MUX-32 (DS3 Interface-32 Modules) refer to the MUXP circuit packs. These points are always set to 0 in the DS3 Interface-16 Module displays. Tables B-6 and B-7 list the required scan and control points, respectively. In addition to equipment failures, alarm points are required to indicate incoming DS3 facility alarms. These points specify whether the DS3 is OOF or if there is a LOS or BER exceeding the selected threshold (either $10^{-3}$ or $10^{-6}$). Detailed display sets for modules 9-32 are part of the extended display sets.

Table B-6. **Detailed Display Set (DS3 INTFC Module) — Scan Points**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1 | A | Power Circuit Pack(s) Fail |
| | 2 | - | Unassigned |
| | 3 | A | UC Fail SA |
| | 4-7 | A | CLKDR-{1-4} Fail SA |
| | 8-11 | A | CLKDR-{1-4} Fail NSA |
| | 12 | A | MUXPS Fail SA |
| | 13 | - | Reserved |
| | 14 | A | DS3 Interface Manual Function Initiated |
| | 15-18 | - | Unassigned |
| | 19-49 | S | MUX-{1-31} Protection Switch Active |
| | 50-63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1 | S | MUX Protection Switch Auto-Locked |
| | 2-32 | S | MUX-{1-31} Protection Switch Locked |
| | 33-63 | A | DS3 Signal-{1-31} ID Error |
| | 64 | - | Reserved |
| 3 | 1-31 | A | MUX-{1-31} Fail SA |
| | 32-62 | A | MUX/PMGR-{1-32} Fail NSA |
| | 63 | A | MUX-32 (MUXP) Fail NSA |
| | 64 | - | Reserved |
| 4 | 1-31 | A | Incoming DS3 Signal-{1-31} LOS/BER |
| | 32-62 | A | Incoming DS3 Signal-{1-31} OOF |
| | 63 | A | MUX-32 (MUXP) Fail SA |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are five displays per DS3 Interface Module

Table continued on next page.

Table B-6. **Detailed Display Set (DS3 INTFC Module) — Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 5 | 1-31 | A | Incoming DS3 Signal-{1-31} AIS Detected |
| | 32-62 | A | Incoming DS3 Signal-{1-31} Idle Detected |
| | 63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are five displays per DS3 Interface Module

Table B-7. **Detailed Display Set (DS3 INTFC Module) — Control Points**

| Display † | Point No. | Description |
|---|---|---|
| 1 | 1 | Unassigned |
| | 2-32 | MUX-{1-31} Switch to Protection |
| | 33-64 | Unassigned |
| 2 | 1 | MUX-1 Lock Protection |
| | 2 | MUX-1 Unlock Protection |
| | 3 | MUX-2 Lock Protection |
| | 4 | MUX-2 Unlock Protection |
| | 5 | MUX-3 Lock Protection |
| | 6 | MUX-3 Unlock Protection |
| | 7 | MUX-4 Lock Protection |
| | 8 | MUX-4 Unlock Protection |
| | 9 | MUX-5 Lock Protection |
| | 10 | MUX-5 Unlock Protection |
| | 11 | MUX-6 Lock Protection |
| | 12 | MUX-6 Unlock Protection |
| | 13 | MUX-7 Lock Protection |
| | 14 | MUX-7 Unlock Protection |
| | 15 | MUX-8 Lock Protection |

† There are two displays per DS3 Interface Module

Table continued on next page.

Table B-7. Detailed Display Set (DS3 INTFC Module) — Control Points (Continued)

| Display † | Point No. | Description |
|---|---|---|
| | 16 | MUX-8 UnLock Protection |
| | 17 | MUX-9 Lock Protection |
| | 18 | MUX-9 Unlock Protection |
| | 19 | MUX-10 Lock Protection |
| | 20 | MUX-10 Unlock Protection |
| | 21 | MUX-11 Lock Protection |
| | 22 | MUX-11 Unlock Protection |
| | 23 | MUX-12 Lock Protection |
| | 24 | MUX-12 Unlock Protection |
| | 25 | MUX-13 Lock Protection |
| | 26 | MUX-13 Unlock Protection |
| | 27 | MUX-14 Lock Protection |
| | 28 | MUX-14 Unlock Protection |
| 2 | 29 | MUX-15 Lock Protection |
| | 30 | MUX-15 Unlock Protection |
| | 31 | MUX-16 Lock Protection |
| | 32 | MUX-16 Unlock Protection |
| | 33 | MUX-17 Lock Protection |
| | 34 | MUX-17 Unlock Protection |
| | 35 | MUX-18 Lock Protection |
| | 36 | MUX-18 Unlock Protection |
| | 37 | MUX-19 Lock Protection |
| | 38 | MUX-19 Unlock Protection |
| | 39 | MUX-20 Lock Protection |
| | 40 | MUX-20 Unlock Protection |
| | 41 | MUX-21 Lock Protection |
| | 42 | MUX-21 Unlock Protection |

† There are two displays per DS3 Interface Module

Table continued on next page.

Table B-7. **Detailed Display Set (DS3 INTFC Module) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| | 43 | MUX-22 Lock Protection |
| | 44 | MUX-22 Unlock Protection |
| | 45 | MUX-23 Lock Protection |
| | 46 | MUX-23 Unlock Protection |
| | 47 | MUX-24 Lock Protection |
| | 48 | MUX-24 Unlock Protection |
| | 49 | MUX-25 Lock Protection |
| | 50 | MUX-25 Unlock Protection |
| | 51 | MUX-26 Lock Protection |
| | 52 | MUX-26 Unlock Protection |
| 2 | 53 | MUX-27 Lock Protection |
| | 54 | MUX-27 Unlock Protection |
| | 55 | MUX-28 Lock Protection |
| | 56 | MUX-28 Unlock Protection |
| | 57 | MUX-29 Lock Protection |
| | 58 | MUX-29 Unlock Protection |
| | 59 | MUX-30 Lock Protection |
| | 60 | MUX-30 Unlock Protection |
| | 61 | MUX-31 Lock Protection |
| | 62 | MUX-31 Unlock Protection |
| | 63-64 | Unassigned |

† There are two displays per DS3 Interface Module

# Extended Display Sets

## HCC, SYNC, SWIO, SWCS, RUI and OPEX Modules

For the DACS IV-2000 (512), additional detailed scan and control display sets are provided in the extended display sets. These additional scan and control points are provided for the additional SWIO circuit packs. Tables B-8 and B-9 list the additional detailed High Capacity Controller, Synchronizer, Switch Input/Output, Switch Center Stage, Remote Unit Interface, and Optical Extension Module scan and control points, respectively.

Table B-8. **Extended Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Scan Points**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1-16 | A | SWIO-3-{1-16} Fail NSA |
| | 17-32 | A | SWIO-4-{1-16} Fail NSA |
| | 33-48 | A | SWIO-3-{1-16} Fail SA |
| | 49-63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1-16 | A | SWIO-4-{1-16} Fail SA |
| | 17-32 | S | SWIO-3-{1-16} Protection Switch Active |
| | 33-48 | S | SWIO-4-{1-16} Protection Switch Active |
| | 49-63 | - | Unassigned |
| | 64 | - | Reserved |
| 3 | 1-16 | S | SWIO-3-{1-16} Protection Switch Locked |
| | 17-32 | S | SWIO-4-{1-16} Protection Switch Locked |
| | 33-48 | S | SWIO-2-{1-16} Protection Switch Auto-Locked |
| | 49-63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are seven displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-8. Extended Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Scan Points (Continued)

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| | 1-16 | S | SWIO-3-{1-16} Protection Switch Auto-Locked |
| | 17-32 | S | SWIO-4-{1-16} Protection Switch Auto-Locked |
| | 33 | S | SWCS-2-16 Protection Switch Active |
| | 34 | S | SWCS-2-16 Protection Switch Locked |
| | 35 | A | PWRJ-1-{1,2} Fail NSA |
| | 36 | A | PWRJ-1-{1,2} Fail SA |
| | 37 | A | PWRJ-1-{3,4} Fail NSA |
| | 38 | A | PWRJ-1-{3,4} Fail SA |
| | 39 | A | PWRJ-1-{5,6} Fail NSA |
| | 40 | A | PWRJ-1-{5,6} Fail SA |
| | 41 | A | PWRJ-2-{1,2} Fail NSA |
| 4 | 42 | A | PWRJ-2-{1,2} Fail SA |
| | 43 | A | PWRJ-2-{3,4} Fail NSA |
| | 44 | A | PWRJ-2-{3,4} Fail SA |
| | 45 | A | PWRJ-2-{5,6} Fail NSA |
| | 46 | A | PWRJ-2-{5,6} Fail SA |
| | 47 | A | PWRJ-3-{1,2} Fail NSA |
| | 48 | A | PWRJ-3-{1,2} Fail SA |
| | 49 | A | PWRJ-3-{3,4} Fail NSA |
| | 50 | A | PWRJ-3-{3,4} Fail SA |
| | 51 | A | PWRJ-3-{5,6} Fail NSA |
| | 52 | A | PWRJ-3-{5,6} Fail SA |
| | 53 | A | PWRG Fail NSA |
| | 54 | A | PWRG Fail SA |

* A = Alarm
S = Scan

† There are seven displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table continued on next page.

Table B-8. **Extended Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 4 | 55 | A | OPEX-2 Power Fail SA |
| | 56 | A | OPEX-2 Power Fail NSA |
| | 57 | A | RUI-2 Power Fail NSA |
| | 58-59 | A | RX-{1,2} Fan Fail |
| | 60-63 | - | Unassigned |
| | 64 | - | Reserved |
| 5 | 1-16 | A | OPEX-1-{1-16} Fail SA |
| | 17-32 | A | OPEX-2-{1-16} Fail SA |
| | 33-48 | A | OPEX-3-{1-16} Fail SA |
| | 49-63 | - | Unassigned |
| | 64 | - | Reserved |
| 6 | 1-16 | A | OPEX-4-{1-16} Fail SA |
| | 17-32 | A | OPEX-1-{1-16} Fail NSA |
| | 33-48 | A | OPEX-2-{1-16} Fail NSA |
| | 49-63 | - | Unassigned |
| | 64 | - | Reserved |
| 7 | 1-16 | A | OPEX-3-{1-16} Fail NSA |
| | 17-32 | A | OPEX-4-{1-16} Fail NSA |
| | 33-63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are seven displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

Table B-9. Extended Display Set (HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules) — Control Points

| Display † | Point No. | Description |
|---|---|---|
| 1 | 1-16 | SWIO-3-{1-16} Lock Protection |
| | 17-32 | SWIO-4-{1-16} Lock Protection |
| | 33-64 | Unassigned |
| | 64 | Reserved |
| 2 | 1-16 | SWIO-3-{1-16} Unlock Protection |
| | 17-32 | SWIO-4-{1-16} Unlock Protection |
| | 33 | SWIO-2-16 Unlock Protection |
| | 34 | SWCS-2-16 Unlock Protection |
| | 35-63 | Unassigned |
| | 64 | Reserved |

† There are two displays for the HCC/SYNC/SWIO/SWCS/RUI/OPEX Modules.

## Extended Facility Display Sets

The detailed scan points described previously are not always sufficient to identify the specific facility affected by a failure. In particular, incoming DS1 failures are specified by a single scan point for a DS1 Interface Module that can interface with up to 224 DS1 signals. The extended set provides the telemetry remote with increased information concerning incoming DS1 failures, and incoming DS3 OOF and format mismatches.

The extended facility scan and control points listed in Tables B-10, B-11, B-12, B-13, and B-14 overcome the limitations of the detailed AS&C set previously described. Even with the addition of the scan points, failures relating to outgoing DS1 and DS3 facilities are not identified to the specific affected facility.

### DS1 Facilities

A single scan point is provided for each incoming DS1 signal. This point indicates whenever the specified DS1 signal exceeds the BPV error threshold of $10^{-3}$ through $10^{-9}$ or is in an LOS condition. Table B-10 lists these scan points. These scan points require four additional displays for each DS1 Interface Module.

Table B-10. **Extended Display Set (DS1 INTFC Module) — Scan Points**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1-56 | S | Incoming DS1 Signal-{1-56} Fail |
| | 57-63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1-56 | S | Incoming DS1 Signal-{57-112} Fail |
| | 57-63 | - | Unassigned |
| | 64 | - | Reserved |
| 3 | 1-56 | S | Incoming DS1 Signal-{113-168} Fail |
| | 57-63 | - | Unassigned |
| | 64 | - | Reserved |
| 4 | 1-56 | S | Incoming DS1 Signal-{169-224} Fail |
| | 57-63 | - | Unassigned |
| | 64 | - | Reserved |

* S = Scan

† There are four displays per DS1 Interface Module.

## DS3 Facilities

For each service MUX circuit pack in a DS3 Interface Module, one alarm point is provided to indicate signal format mismatches (M13 or CBIT) and seven alarm points are provided to indicate DS2 signals within the incoming DS3 facility that are OOF. Table B-11 lists these points. These scan points require four additional displays for each DS3 Interface Module.

In addition to the above points, MUX3 circuit packs also have one alarm point is provided to indicate signal label match failures (SLMF) and one alarm point each for DS1 tributaries within a DS3 signal for OOF, BER, AIS, YEL, DLI, and DLN conditions. Table B-12 lists these points. These scan points require four additional displays for each DS3 Interface Module.

Table B-11. **Extended Display Set (DS3 INTFC Module, All MUX Circuit Packs) — Scan Points**

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1-7 | A | DS3 1, DS2-{1-7} OOF |
| | 8-14 | A | DS3 2, DS2-{1-7} OOF |
| | 15-21 | A | DS3 3, DS2-{1-7} OOF |
| | 22-28 | A | DS3 4, DS2-{1-7} OOF |
| | 29-35 | A | DS3 5, DS2-{1-7} OOF |
| | 36-42 | A | DS3 6, DS2-{1-7} OOF |
| | 43-49 | A | DS3 7, DS2-{1-7} OOF |
| | 50-56 | A | DS3 8, DS2-{1-7} OOF |
| | 57-63 | A | DS3 9, DS2-{1-7} OOF |
| | 64 | - | Reserved |
| 2 | 1-7 | A | DS3 10, DS2-{1-7} OOF |
| | 8-14 | A | DS3 11, DS2-{1-7} OOF |
| | 15-21 | A | DS3 12, DS2-{1-7} OOF |
| | 22-28 | A | DS3 13, DS2-{1-7} OOF |
| | 29-35 | A | DS3 14, DS2-{1-7} OOF |
| | 36-42 | A | DS3 15, DS2-{1-7} OOF |
| | 43-49 | A | DS3 16, DS2-{1-7} OOF |
| | 50-56 | A | DS3 17, DS2-{1-7} OOF |
| | 57-63 | A | DS3 18, DS2-{1-7} OOF |
| | 64 | - | Reserved |
| 3 | 1-7 | A | DS3 19, DS2-{1-7} OOF |
| | 8-14 | A | DS3 20, DS2-{1-7} OOF |
| | 15-21 | A | DS3 21, DS2-{1-7} OOF |
| | 22-28 | A | DS3 22, DS2-{1-7} OOF |
| | 29-35 | A | DS3 23, DS2-{1-7} OOF |
| | 36-42 | A | DS3 24, DS2-{1-7} OOF |

* A = Alarm

† There are four displays per DS3 Interface Module.

Table continued on next page.

Table B-11. **Extended Display Set (DS3 INTFC Module, All MUX Circuit Packs) — Scan Points (Continued)**

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 3 | 43-49 | A | DS3 25, DS2-{1-7} OOF |
| | 50-56 | A | DS3 26, DS2-{1-7} OOF |
| | 57-63 | A | DS3 27, DS2-{1-7} OOF |
| | 64 | - | Reserved |
| 4 | 1-7 | A | DS3 28, DS2-{1-7} OOF |
| | 8-14 | A | DS3 29, DS2-{1-7} OOF |
| | 15-21 | A | DS3 30, DS2-{1-7} OOF |
| | 22-28 | A | DS3 31, DS2-{1-7} OOF |
| | 29-59 | A | DS3 Signal-{1-31} Format Mismatch |
| | 60-63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm

† There are four displays per DS3 Interface Module.

Table B-12. **Extended Display Set (DS3 INTFC Module, MUX3 Additional Points) — Scan Points**

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1-31 | A | DS3 Signal-{1-31} SLMF |
| | 32-62 | A | DS3 Signal-{1-31} DS1-{1-28} OOF |
| | 63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1-31 | A | DS3 Signal-{1-31} DS1-{1-28} BER |
| | 32-62 | A | DS3 Signal-{1-31} DS1-{1-28} AIS |
| | 63 | - | Unassigned |
| | 64 | - | Reserved |
| 3 | 1-31 | A | DS3 Signal-{1-31} DS1-{1-28} YEL |
| | 32-62 | A | DS3 Signal-{1-31} DS1-{1-28} DLI |

* A = Alarm

† There are four displays per DS3 Interface Module.

Table continued on next page.

Table B-12. **Extended Display Set (DS3 INTFC Module, MUX3 Additional Points) — Scan Points (Continued)**

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 3 | 63 | - | Unassigned |
| | 64 | - | Reserved |
| 4 | 1-31 | A | DS3 Signal-{1-31} DS1-{1-28} DLN |
| | 32-63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm

† There are four displays per DS3 Interface Module.

## STS1 Interface Module AS&C Points

All AS&C points for STS1 Interface Modules are provided as extended alarm sets. Alarm, scan, and control points are provided for equipment associated with STS1 Interface Modules. In addition, for each incoming STS-1 facility to a SMUX circuit pack, eight alarm points (120 alarm points for each SMUX circuit pack) are provided to indicate:

- Loss of signal or high bit error rate (LOS/T-BERL)
- Loss of frame (LOF)
- Loss of pointer (LOP)
- Line alarm indication signal (AISL)
- Path alarm indication signal (AISP)
- Path yellow (YEL)
- Far-end remote failure (FERF)
- Signal label match failure (SLMF)

For a VT1.5 tributary signal within an EC-1 facility, the following points are provided:

- Fifteen alarm points to identify one or more VT LOP condition(s)
- Fifteen status points to identify one or more VT path yellow condition(s) has been detected on an upstream tributary failure

Tables B-13 and B-14 list the extended set scan and control points, respectively.

Table B-13. **Extended Display Set (STS1 INTFC Module) — Scan Points**

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1 | A | Power Circuit Pack Fail |
| | 2 | - | Unassigned |
| | 3 | A | UC Fail SA |
| | 4-5 | A | CLKDR-{1,2} Fail SA |
| | 6-7 | A | CLKDR-{1,2} Fail NSA |
| | 8 | A | MUXPS Fail SA |
| | 9 | A | STS1 Interface Manual Function Initiated |
| | 10-14 | - | Unassigned |
| | 15-29 | S | SMUX-{1-15} Protection Switch Active |
| | 30 | S | SMUX Protection Switch Auto-Locked |
| | 31-45 | S | SMUX-{1-15} Protection Switch Locked |
| | 46-60 | - | Reserved |
| | 61-63 | | Unassigned |
| | 64 | - | Reserved |
| 2 | 1-15 | A | SMUX-{1-15} Fail SA |
| | 16 | A | SMUX-16 (SMUXP) Fail SA |
| | 17-31 | A | SMUX-{1-15} Fail NSA |
| | 32 | A | SMUX-16 (SMUXP) Fail NSA |
| | 33-47 | A | Incoming STS-1 Signal-{1-15} LOF/T-BERL |
| | 48-62 | A | Incoming STS-1 Signal-{1-15} LOF |
| | 63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are five displays per STS1 Interface-16 Module.

Table continued on next page.

Table B-13. **Extended Display Set (STS1 INTFC Module) — Scan Points (Continued)**

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 3 | 1-15 | A | Incoming STS-1 Signal-{1-15} LOP |
| | 16-30 | A | Incoming STS-1 Signal-{1-15} AISL |
| | 31-45 | S | Incoming STS-1 Signal-{1-15} AISP |
| | 46-60 | S | Incoming STS-1 Signal-{1-15} YEL |
| | 61-63 | - | Unassigned |
| | 64 | - | Reserved |
| 4 | 1-15 | S | Incoming STS-1 Signal-{1-15} FERF |
| | 16-30 | A | Incoming STS-1 Signal-{1-15} SLMF |
| | 31-63 | - | Unassigned |
| | 64 | - | Reserved |
| 5 | 1-15 | A | STS1-{1-15}, VT1.5-{1-28} VT LOP |
| | 16-30 | S | STS1-{1-15}, VT1.5-{1-28} VT AISP |
| | 31-45 | S | STS1-{1-15}, VT1.5-{1-28} VT YEL |
| | 46-63 | - | Unassigned |
| | 64 | - | Reserved |

A = Alarm
S = Scan

† There are five displays per STS1 Interface-16 Module.

Table B-14. **Extended Display Set (STS1 INTFC Module) — Control Points**

| Display† | Point No. | Description |
|---|---|---|
| 1 | 1 | Unassigned |
| | 2-16 | SMUX-{1-15} Make Protection Switch |
| | 17 | SMUX-1 Lock Protection |
| | 18 | SMUX-1 Unlock Protection |
| | 19 | SMUX-2 Lock Protection |
| | 20 | SMUX-2 Unlock Protection |

† There is one display per STS1 Interface-16 Module.

Table continued on next page.

Table B-14. Extended Display Set (STS1 INTFC Module) — Control Points (Continued)

| Display† | Point No. | Description |
|---|---|---|
| 1 | 21 | SMUX-3 Lock Protection |
| | 22 | SMUX-3 Unlock Protection |
| | 23 | SMUX-4 Lock Protection |
| | 24 | SMUX-4 Unlock Protection |
| | 25 | SMUX-5 Lock Protection |
| | 26 | SMUX-5 Unlock Protection |
| | 27 | SMUX-6 Lock Protection |
| | 28 | SMUX-6 Unlock Protection |
| | 29 | SMUX-7 Lock Protection |
| | 30 | SMUX-7 Unlock Protection |
| | 31 | SMUX-8 Lock Protection |
| | 32 | SMUX-8 Unlock Protection |
| | 33 | SMUX-9 Lock Protection |
| | 34 | SMUX-9 Unlock Protection |
| | 35 | SMUX-10 Lock Protection |
| | 36 | SMUX-10 Unlock Protection |
| | 37 | SMUX-11 Lock Protection |
| | 38 | SMUX-11 Unlock Protection |
| | 39 | SMUX-12 Lock Protection |
| | 40 | SMUX-12 Unlock Protection |
| | 41 | SMUX-13 Lock Protection |
| | 42 | SMUX-13 Unlock Protection |
| | 43 | SMUX-14 Lock Protection |
| | 44 | SMUX-14 Unlock Protection |
| | 45 | SMUX-15 Lock Protection |
| | 46 | SMUX-15 Unlock Protection |
| | 47-63 | Unassigned |
| | 64 | Reserved |

† There is one display per STS1 Interface-16 Module.

# Display Requirements

The number of displays required depends on the choice of AS&C set and on the configuration of the system. The following paragraphs discuss the total number of displays required for each of the three AS&C sets previously described.

## Summary AS&C Points

The summary set consists of a single scan display.

## Detailed and Extended AS&C Points

Tables B-15 (scan points) and B-16 (control points) list the number of displays required for each module and, for each module type, how many modules can be equipped in a single system. Although the maximum number of DS3 Interface Modules is 32 and the maximum number of DS1 Interface Modules is 64, the switch is limited to a capacity of 512/496 DS3/STS-1 equivalents and, therefore, the number of DS1 Interface Modules must be reduced by 4 for each DS3 Interface-32 Module and by 2 for each DS3 Interface-16 or STS1 Interface-16 Module in the system.

The maximum number of displays (detailed and extended) is 360. For example, a DACS IV-2000 configuration of 8 STS1 Interface-16 Modules, 8 DS3 Interface-32 Modules, and 16 DS1 Interface Modules uses 13 displays for the High Capacity Controller, Synchronizer, Switch Input/Output, Switch Center Stage, Switch Power, Remote Unit Interface, and Optical Extension Modules, 40 displays for the 8 STS1 Interface-16 Modules, 104 displays for the 8 DS3 Interface-32 Modules, and 96 displays for the 16 DS1 Interface Modules for a total of 253 displays. In normal practice, only changed displays are transmitted, and this greatly reduces the number of displays sent in any given polling interval. Displays for modules that are not equipped are not sent in response to a *Scan All* or *Scan Changed Displays*, but are indicated by a gap in the response.

The DACS IV-2000 can be equipped in a variety of configurations with different combinations of DS1, DS3, and STS1 interfaces. The configuration with the most displays has 64 DS1 Interface Modules and no DS3 Interface or STS1 Interface Modules and requires 70 detailed displays (6 for the High Capacity Controller, Switch Input/Output, Switch Center Stage, Synchronizer, Switch Power, Remote Unit Interface, and Optical Extension Modules and 64 for the first 32 DS1 Interface Modules).

Table B-15. **Number of Scan Point Displays**

| Module Type | Maximum Modules | Number of Displays per Module | |
|---|---|---|---|
| | | Detailed | Extended |
| HCC, SYNC, SWIO, SWCS, RUI, and OPEX Modules | 1 | 6 | 7 |
| DS1 Interface Module (1-32) | 32 | 2 | 4 |
| DS1 Interface Module (33-64) | 32 | 0 | 6 |
| DS3 Interface Module [MUX1/ MUX2/MUX3] (1-8) | 8 | 5 | 4 |
| DS3 Interface Module [MUX1/ MUX2/MUX3] (9-32) | 24 | 0 | 9 |
| DS3 Interface Module [MUX3 additional points] (1-32) | 32 | 0 | 4 |
| STS1 Interface Module (1-32) | 32 | 0 | 5 |

Table B-16. **Number of Control Point Displays**

| Module Type | Maximum Modules | Number of Displays per Module | |
|---|---|---|---|
| | | Detailed | Extended |
| HCC, SYNC, SWIO, SWCS, RUI, and OPEX Modules | 1 | 5 | 2 |
| DS1 Interface Module (1-32) | 32 | 1 | 0 |
| DS1 Interface Module (33-64) | 32 | 0 | 1 |
| DS3 Interface Module (1-8) | 8 | 2 | 0 |
| DS3 Interface Module (9-32) | 24 | 0 | 2 |
| STS1 Interface Module (1-32) | 32 | 0 | 1 |

## Display Numbering

Table B-17 lists the AS&C display numbering assignments.

Table B-17. **Scan Point Display Numbering**

| Scan Display | Control Display | Module |
|---|---|---|
| 0 | - | Summary (entire system) |
| 1-6 | 1-5 | High Capacity Controller Module,<br>Synchronizer Module,<br>Switch Input/Output Module,<br>Switch Center Stage,<br>Switch Power Module,<br>Remote Unit Interface Module, and<br>Optical Extension Module |
| 7-11 | 7-8 | DS3 Interface 1 |
| 12-16 | 12-13 | DS3 Interface 2 |
| 17-21 | 17-18 | DS3 Interface 3 |
| 22-26 | 22-23 | DS3 Interface 4 |
| 27-31 | 27-28 | DS3 Interface 5 |
| 32-36 | 32-33 | DS3 Interface 6 |
| 37-41 | 37-38 | DS3 Interface 7 |
| 42-46 | 42-43 | DS3 Interface 8 |
| 47-48 | 48 | DS1 Interface 1 |
| 49-50 | 50 | DS1 Interface 2 |
| 51-52 | 52 | DS1 Interface 3 |
| 53-54 | 54 | DS1 Interface 4 |
| 55-56 | 56 | DS1 Interface 5 |
| 57-58 | 58 | DS1 Interface 6 |
| 59-60 | 60 | DS1 Interface 7 |
| 61-62 | 62 | DS1 Interface 8 |
| 63-64 | 64 | DS1 Interface 9 |
| 65-66 | 66 | DS1 Interface 10 |
| 67-68 | 68 | DS1 Interface 11 |
| 69-70 | 70 | DS1 Interface 12 |

Table continued on next page.

Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 71-72 | 72 | DS1 Interface 13 |
| 73-74 | 74 | DS1 Interface 14 |
| 75-76 | 76 | DS1 Interface 15 |
| 77-78 | 78 | DS1 Interface 16 |
| 79-80 | 80 | DS1 Interface 17 |
| 81-82 | 82 | DS1 Interface 18 |
| 83-84 | 84 | DS1 Interface 19 |
| 85-86 | 86 | DS1 Interface 20 |
| 87-88 | 88 | DS1 Interface 21 |
| 89-90 | 90 | DS1 Interface 22 |
| 91-92 | 92 | DS1 Interface 23 |
| 93-94 | 94 | DS1 Interface 24 |
| 95-96 | 96 | DS1 Interface 25 |
| 97-98 | 98 | DS1 Interface 26 |
| 99-100 | 100 | DS1 Interface 27 |
| 101-102 | 102 | DS1 Interface 28 |
| 103-104 | 104 | DS1 Interface 29 |
| 105-106 | 106 | DS1 Interface 30 |
| 107-108 | 108 | DS1 Interface 31 |
| 109-110 | 110 | DS1 Interface 32 |
| 111-119 | - | Unused |
| 120-123 | - | DS3 Interface 1 Extended Facilities |
| 124-127 | - | DS3 Interface 2 Extended Facilities |
| 128-131 | - | DS3 Interface 3 Extended Facilities |
| 132-135 | - | DS3 Interface 4 Extended Facilities |
| 136-139 | - | DS3 Interface 5 Extended Facilities |
| 140-143 | - | DS3 Interface 6 Extended Facilities |
| 144-147 | - | DS3 Interface 7 Extended Facilities |
| 148-151 | - | DS3 Interface 8 Extended Facilities |

Table continued on next page.

Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 152-155 | - | DS1 Interface 1 Extended Facilities |
| 156-159 | - | DS1 Interface 2 Extended Facilities |
| 160-163 | - | DS1 Interface 3 Extended Facilities |
| 164-167 | - | DS1 Interface 4 Extended Facilities |
| 168-171 | - | DS1 Interface 5 Extended Facilities |
| 172-175 | - | DS1 Interface 6 Extended Facilities |
| 176-179 | - | DS1 Interface 7 Extended Facilities |
| 180-183 | - | DS1 Interface 8 Extended Facilities |
| 184-187 | - | DS1 Interface 9 Extended Facilities |
| 188-191 | - | DS1 Interface 10 Extended Facilities |
| 192-195 | - | DS1 Interface 11 Extended Facilities |
| 196-199 | - | DS1 Interface 12 Extended Facilities |
| 200-203 | - | DS1 Interface 13 Extended Facilities |
| 204-207 | - | DS1 Interface 14 Extended Facilities |
| 208-211 | - | DS1 Interface 15 Extended Facilities |
| 212-215 | - | DS1 Interface 16 Extended Facilities |
| 216-219 | - | DS1 Interface 17 Extended Facilities |
| 220-223 | - | DS1 Interface 18 Extended Facilities |
| 224-227 | - | DS1 Interface 19 Extended Facilities |
| 228-231 | - | DS1 Interface 20 Extended Facilities |
| 232-235 | - | DS1 Interface 21 Extended Facilities |
| 236-239 | - | DS1 Interface 22 Extended Facilities |
| 240-243 | - | DS1 Interface 23 Extended Facilities |
| 244-247 | - | DS1 Interface 24 Extended Facilities |
| 248-251 | - | DS1 Interface 25 Extended Facilities |
| 252-255 | - | DS1 Interface 26 Extended Facilities |
| 256-259 | - | DS1 Interface 27 Extended Facilities |
| 260-263 | - | DS1 Interface 28 Extended Facilities |
| 264-267 | - | DS1 Interface 29 Extended Facilities |

Table continued on next page.

Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 268-271 | - | DS1 Interface 30 Extended Facilities |
| 272-275 | - | DS1 Interface 31 Extended Facilities |
| 276-279 | - | DS1 Interface 32 Extended Facilities |
| 280-284 | 280-281 | DS3 Interface 9 |
| 285-289 | 285-286 | DS3 Interface 10 |
| 290-294 | 290-291 | DS3 Interface 11 |
| 295-299 | 295-296 | DS3 Interface 12 |
| 300-304 | 300-301 | DS3 Interface 13 |
| 305-309 | 305-306 | DS3 Interface 14 |
| 310-314 | 310-311 | DS3 Interface 15 |
| 315-319 | 315-316 | DS3 Interface 16 |
| 320-323 | - | DS3 Interface 9 Extended Facilities |
| 324-327 | - | DS3 Interface 10 Extended Facilities |
| 328-331 | - | DS3 Interface 11 Extended Facilities |
| 332-335 | - | DS3 Interface 12 Extended Facilities |
| 336-339 | - | DS3 Interface 13 Extended Facilities |
| 340-343 | - | DS3 Interface 14 Extended Facilities |
| 344-347 | - | DS3 Interface 15 Extended Facilities |
| 348-351 | - | DS3 Interface 16 Extended Facilities |
| 352-355 | 355 | STS1 Interface 1 |
| 356-359 | 359 | STS1 Interface 2 |
| 360-363 | 363 | STS1 Interface 3 |
| 364-367 | 367 | STS1 Interface 4 |
| 368-371 | 371 | STS1 Interface 5 |
| 372-375 | 375 | STS1 Interface 6 |
| 376-379 | 379 | STS1 Interface 7 |
| 380-383 | 383 | STS1 Interface 8 |
| 384-387 | 387 | STS1 Interface 9 |
| 388-391 | 391 | STS1 Interface 10 |

Table continued on next page.

Table B-17. Scan Point Display Numbering (Continued)

| Scan Display | Control Display | Module |
|---|---|---|
| 392-395 | 395 | STS1 Interface 11 |
| 396-399 | 399 | STS1 Interface 12 |
| 400-403 | 403 | STS1 Interface 13 |
| 404-407 | 407 | STS1 Interface 14 |
| 408-411 | 411 | STS1 Interface 15 |
| 412-415 | 415 | STS1 Interface 16 |
| 416 | - | STS1 Interface 1 Extended Facilities |
| 417 | - | STS1 Interface 2 Extended Facilities |
| 418 | - | STS1 Interface 3 Extended Facilities |
| 49 | - | STS1 Interface 4 Extended Facilities |
| 420 | - | STS1 Interface 5 Extended Facilities |
| 421 | - | STS1 Interface 6 Extended Facilities |
| 422 | - | STS1 Interface 7 Extended Facilities |
| 423 | - | STS1 Interface 8 Extended Facilities |
| 424 | - | STS1 Interface 9 Extended Facilities |
| 425 | - | STS1 Interface 10 Extended Facilities |
| 426 | - | STS1 Interface 11 Extended Facilities |
| 427 | - | STS1 Interface 12 Extended Facilities |
| 428 | - | STS1 Interface 13 Extended Facilities |
| 429 | - | STS1 Interface 14 Extended Facilities |
| 430 | - | STS1 Interface 15 Extended Facilities |
| 431 | - | STS1 Interface 16 Extended Facilities |
| 432-433 | 433 | DS1 Interface 33 |
| 434-435 | 435 | DS1 Interface 34 |
| 436-437 | 437 | DS1 Interface 35 |
| 438-439 | 439 | DS1 Interface 36 |
| 440-441 | 441 | DS1 Interface 37 |
| 442-443 | 443 | DS1 Interface 38 |
| 444-445 | 445 | DS1 Interface 39 |

Table continued on next page.

Table B-17. Scan Point Display Numbering (Continued)

| Scan Display | Control Display | Module |
|---|---|---|
| 446-447 | 447 | DS1 Interface 40 |
| 448-449 | 449 | DS1 Interface 41 |
| 450-451 | 451 | DS1 Interface 42 |
| 452-453 | 453 | DS1 Interface 43 |
| 454-455 | 455 | DS1 Interface 44 |
| 456-457 | 457 | DS1 Interface 45 |
| 458-459 | 459 | DS1 Interface 46 |
| 460-461 | 461 | DS1 Interface 47 |
| 462-463 | 463 | DS1 Interface 48 |
| 464-465 | 465 | DS1 Interface 49 |
| 466-467 | 467 | DS1 Interface 50 |
| 468-469 | 469 | DS1 Interface 51 |
| 470-471 | 471 | DS1 Interface 52 |
| 472-473 | 473 | DS1 Interface 53 |
| 474-475 | 475 | DS1 Interface 54 |
| 476-477 | 477 | DS1 Interface 55 |
| 478-479 | 479 | DS1 Interface 56 |
| 480-481 | 481 | DS1 Interface 57 |
| 482-483 | 483 | DS1 Interface 58 |
| 484-485 | 485 | DS1 Interface 59 |
| 486-487 | 487 | DS1 Interface 60 |
| 488-489 | 489 | DS1 Interface 61 |
| 490-491 | 491 | DS1 Interface 62 |
| 492-493 | 493 | DS1 Interface 63 |
| 494-495 | 495 | DS1 Interface 64 |
| 496-499 | - | DS1 Interface 33 Extended Facilities |
| 500-503 | - | DS1 Interface 34 Extended Facilities |
| 504-507 | - | DS1 Interface 35 Extended Facilities |
| 508-511 | - | DS1 Interface 36 Extended Facilities |

Table continued on next page.

Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 512-515 | - | DS1 Interface 37 Extended Facilities |
| 516-519 | - | DS1 Interface 38 Extended Facilities |
| 520-523 | - | DS1 Interface 39 Extended Facilities |
| 524-527 | - | DS1 Interface 40 Extended Facilities |
| 528-531 | - | DS1 Interface 41 Extended Facilities |
| 532-535 | - | DS1 Interface 42 Extended Facilities |
| 536-539 | - | DS1 Interface 43 Extended Facilities |
| 540-543 | - | DS1 Interface 44 Extended Facilities |
| 544-547 | - | DS1 Interface 45 Extended Facilities |
| 548-551 | - | DS1 Interface 46 Extended Facilities |
| 552-555 | - | DS1 Interface 47 Extended Facilities |
| 556-559 | - | DS1 Interface 48 Extended Facilities |
| 560-563 | - | DS1 Interface 49 Extended Facilities |
| 564-567 | - | DS1 Interface 50 Extended Facilities |
| 568-571 | - | DS1 Interface 51 Extended Facilities |
| 572-575 | - | DS1 Interface 52 Extended Facilities |
| 576-579 | - | DS1 Interface 53 Extended Facilities |
| 580-583 | - | DS1 Interface 54 Extended Facilities |
| 584-587 | - | DS1 Interface 55 Extended Facilities |
| 588-591 | - | DS1 Interface 56 Extended Facilities |
| 592-595 | - | DS1 Interface 57 Extended Facilities |
| 596-599 | - | DS1 Interface 58 Extended Facilities |
| 600-603 | - | DS1 Interface 59 Extended Facilities |
| 604-607 | - | DS1 Interface 60 Extended Facilities |
| 608-611 | - | DS1 Interface 61 Extended Facilities |
| 612-615 | - | DS1 Interface 62 Extended Facilities |
| 616-619 | - | DS1 Interface 63 Extended Facilities |
| 620-623 | - | DS1 Interface 64 Extended Facilities |
| 624-628 | 624-625 | DS3 Interface 17 |

Table continued on next page.

Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 629-633 | 629-630 | DS3 Interface 18 |
| 634-638 | 634-635 | DS3 Interface 19 |
| 639-643 | 639-640 | DS3 Interface 20 |
| 644-648 | 644-645 | DS3 Interface 21 |
| 649-653 | 649-650 | DS3 Interface 22 |
| 654-658 | 654-655 | DS3 Interface 23 |
| 659-663 | 659-660 | DS3 Interface 24 |
| 664-668 | 664-665 | DS3 Interface 25 |
| 669-673 | 669-670 | DS3 Interface 26 |
| 674-678 | 674-675 | DS3 Interface 27 |
| 679-683 | 679-680 | DS3 Interface 28 |
| 684-688 | 684-685 | DS3 Interface 29 |
| 689-693 | 689-690 | DS3 Interface 30 |
| 694-698 | 694-695 | DS3 Interface 31 |
| 699-703 | 699-700 | DS3 Interface 32 |
| 704-707 | - | DS3 Interface 17 Extended Facilities |
| 708-711 | - | DS3 Interface 18 Extended Facilities |
| 712-715 | - | DS3 Interface 19 Extended Facilities |
| 716-719 | - | DS3 Interface 20 Extended Facilities |
| 720-723 | - | DS3 Interface 21 Extended Facilities |
| 724-727 | - | DS3 Interface 22 Extended Facilities |
| 728-731 | - | DS3 Interface 23 Extended Facilities |
| 732-735 | - | DS3 Interface 24 Extended Facilities |
| 736-739 | - | DS3 Interface 25 Extended Facilities |
| 740-743 | - | DS3 Interface 26 Extended Facilities |
| 744-747 | - | DS3 Interface 27 Extended Facilities |
| 748-751 | - | DS3 Interface 28 Extended Facilities |
| 752-755 | - | DS3 Interface 29 Extended Facilities |
| 756-759 | - | DS3 Interface 30 Extended Facilities |

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Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 760-763 | - | DS3 Interface 31 Extended Facilities |
| 764-767 | - | DS3 Interface 32 Extended Facilities |
| 768-771 | 771 | STS1 Interface 17 |
| 772-775 | 775 | STS1 Interface 18 |
| 776-779 | 779 | STS1 Interface 19 |
| 780-783 | 783 | STS1 Interface 20 |
| 784-787 | 787 | STS1 Interface 21 |
| 788-791 | 791 | STS1 Interface 22 |
| 792-795 | 795 | STS1 Interface 23 |
| 796-799 | 799 | STS1 Interface 24 |
| 800-803 | 803 | STS1 Interface 25 |
| 804-807 | 807 | STS1 Interface 26 |
| 808-811 | 811 | STS1 Interface 27 |
| 812-815 | 815 | STS1 Interface 28 |
| 816-819 | 819 | STS1 Interface 29 |
| 820-823 | 823 | STS1 Interface 30 |
| 824-827 | 827 | STS1 Interface 31 |
| 828-831 | 831 | STS1 Interface 32 |
| 832 | - | STS1 Interface 17 Extended Facilities |
| 833 | - | STS1 Interface 18 Extended Facilities |
| 834 | - | STS1 Interface 19 Extended Facilities |
| 835 | - | STS1 Interface 20 Extended Facilities |
| 836 | - | STS1 Interface 21 Extended Facilities |
| 837 | - | STS1 Interface 22 Extended Facilities |
| 838 | - | STS1 Interface 23 Extended Facilities |
| 839 | - | STS1 Interface 24 Extended Facilities |
| 840 | - | STS1 Interface 25 Extended Facilities |
| 841 | - | STS1 Interface 26 Extended Facilities |
| 842 | - | STS1 Interface 27 Extended Facilities |

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Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 843 | - | STS1 Interface 28 Extended Facilities |
| 844 | - | STS1 Interface 29 Extended Facilities |
| 845 | - | STS1 Interface 30 Extended Facilities |
| 846 | - | STS1 Interface 31 Extended Facilities |
| 847 | - | STS1 Interface 32 Extended Facilities |
| 848-854 | 848-849 | High Capacity Controller Module, Synchronizer Module, Switch Input/Output Module, Switch Center Stage Module, Switch Power Module, Remote Uint Interface Module, and Optical Extension Module |
| 855-858 | - | DS3 Interface 1 Extended Facilities (Additional MUX3 Points) |
| 859-862 | - | DS3 Interface 2 Extended Facilities (Additional MUX3 Points) |
| 863-866 | - | DS3 Interface 3 Extended Facilities (Additional MUX3 Points) |
| 867-870 | - | DS3 Interface 4 Extended Facilities (Additional MUX3 Points) |
| 871-874 | - | DS3 Interface 5 Extended Facilities (Additional MUX3 Points) |
| 875-878 | - | DS3 Interface 6 Extended Facilities (Additional MUX3 Points) |
| 879-882 | - | DS3 Interface 7 Extended Facilities (Additional MUX3 Points) |
| 883-886 | - | DS3 Interface 8 Extended Facilities (Additional MUX3 Points) |
| 887-890 | - | DS3 Interface 9 Extended Facilities (Additional MUX3 Points) |
| 891-894 | - | DS3 Interface 10 Extended Facilities (Additional MUX3 Points) |
| 895-898 | - | DS3 Interface 11 Extended Facilities (Additional MUX3 Points) |

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Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 899-902 | - | DS3 Interface 12 Extended Facilities (Additional MUX3 Points) |
| 903-906 | - | DS3 Interface 13 Extended Facilities (Additional MUX3 Points) |
| 907-910 | - | DS3 Interface 14 Extended Facilities (Additional MUX3 Points) |
| 911-914 | - | DS3 Interface 15 Extended Facilities (Additional MUX3 Points) |
| 915-918 | - | DS3 Interface 16 Extended Facilities (Additional MUX3 Points) |
| 919-922 | - | DS3 Interface 17 Extended Facilities (Additional MUX3 Points) |
| 923-926 | - | DS3 Interface 18 Extended Facilities (Additional MUX3 Points) |
| 927-930 | - | DS3 Interface 19 Extended Facilities (Additional MUX3 Points) |
| 931-934 | - | DS3 Interface 20 Extended Facilities (Additional MUX3 Points) |
| 935-938 | - | DS3 Interface 21 Extended Facilities (Additional MUX3 Points) |
| 939-942 | - | DS3 Interface 22 Extended Facilities (Additional MUX3 Points) |
| 943-946 | - | DS3 Interface 23 Extended Facilities (Additional MUX3 Points) |
| 947-950 | - | DS3 Interface 24 Extended Facilities (Additional MUX3 Points) |
| 951-954 | - | DS3 Interface 25 Extended Facilities (Additional MUX3 Points) |
| 955-958 | - | DS3 Interface 26 Extended Facilities (Additional MUX3 Points) |
| 959-962 | - | DS3 Interface 27 Extended Facilities (Additional MUX3 Points) |
| 963-966 | - | DS3 Interface 28 Extended Facilities (Additional MUX3 Points) |

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Table B-17. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 967-970 | - | DS3 Interface 29 Extended Facilities (Additional MUX3 Points) |
| 971-974 | - | DS3 Interface 30 Extended Facilities (Additional MUX3 Points) |
| 975-978 | - | DS3 Interface 31 Extended Facilities (Additional MUX3 Points) |
| 979-982 | - | DS3 Interface 32 Extended Facilities (Additional MUX3 Points) |

# Glossary

## A

**Absent (ABS)**
The circuit pack or a blank circuit pack is not in the associated slot.

**Active (ACT)**
The circuit pack or module is in service, not protected. If it is a traffic-carrying circuit pack or module, it is carrying traffic.

**Alarm**
An indication that a failure has occurred within a piece of equipment and/or a transmission facility.

**Alarm Cutoff (ACO)**
A button on the Status Panel used to silence audible alarms. Audible alarms can also be silenced using the `OPR-ACO-ALL` command.

**Alarm Delay**
Specifies the alarm delay (in seconds) for software-detected alarm conditions. Initial value is 10 seconds.

**Alarm Indication Signal (AIS)**
A signal transmitted downstream if the incoming signal is defective.

**Alarm, Scan, and Control (AS&C) Points**
Interface between the DACS IV-2000 and telemetry operations systems (OSs).

**All-Ones Signal**
Signal that is defined to contain all ones. AIS is an example of an all-ones signal.

**Alphanumeric Characters**
Letters and digits.

**Alternate Mark Inversion (AMI)**
A DS1 line code in which alternate one bits are positive and negative, but zero substitution is not used.

**ASCII Characters**
Letters, digits, and symbols used in the American Standard Code for Information Interchange.

**Attribute**
Alarm indication level: critical, major, minor, or no alarm.

**Autolock**
When the system autolocks a circuit pack, it switches to protection and forbids return to the working circuit pack even if the trouble clears. This is caused by multiple protection switches on that circuit pack in a short time period.

**Autolock Numbers of Switches**
This parameter is the number of times that the system restores a circuit pack to service (after intermittent failures) in a given autolock switching interval before the circuit pack is autolocked.

**Autolock Release Time**
The number of hours between times when the system automatically releases autolock.

**Autonomous**
An action performed by the system without direction by you.

**Auto-provisioning**
Put into the provisioned state automatically by the system.

**Available (AVAIL)**
Circuit pack or interface module is not provisioned and not assigned in the database. The circuit pack or interface module is not monitored by the system

# B

**B3ZS**
Bipolar with 3-zero substitution; a DS3 or STS-1 line code.

**B8ZS**
Bipolar with 8-zero substitution; a DS1 line code.

**Battery Distribution Feeder Board (BDFB)**
Lineage 2000 (or equivalent) battery plant (-48 Vdc nominal) used to supply power to the DACS IV-2000. New Release 4.0 frame orders use two BDFBs (red and blue power feeds), while existing frames software upgraded to Release 4.0 use one BDFB

**Baud Rate**
Transmission rate (bits per second) on a link.

**BER Metric**
Specifies the metric for calculating bit error rate at a DS3 interface port. Options are bipolar variation (BPV) or parity (PTY). The initial value is BPV.

**Bipolar Variation**
A variation of the alternating +1, -1 pattern in a 3-level code.

**Bit Error Rate (BER) Threshold**
Point at which an alarm is issued for bit errors.

**Blank (BLK)**
Circuit pack slot containing a bus extender (blank) circuit pack.

**Blue Code**
Same as alarm indication signal (AIS).

**Boot**
To transfer contents of backup memory into the system's working memory.

**Bridge**
To take a signal from a single input port and connect it to multiple output ports.

**Broadcast**
To take a signal from a single input port and connect it to multiple output ports.

**Byte**
Usually refers to a group of eight consecutive binary digits, but sometimes used for bit groups of other sizes.

# C

**Call Redirect**
Autonomous action taken when the ECI circuit pack that an X.25 network is connected to fails. A call redirect takes up to 2 minutes to complete and switches the X.25 network to the working ECI circuit pack.

**Capacity Expansion**
Feature that allows customers to minimize the number of DACS IV-2000 frames needed in larger offices by absorbing up to two DACS IV-2000 (256) systems into the Switch Complex of a DACS IV-2000 (512) system.

**C-bit Parity**
Parity checks on blocks of data are used to detect bits in error. C-bit parity is a DS3 format specified by ANSI T1.107 that supports near-end and far-end path performance monitoring, contains far-end alarm/control, and three end-to-end overhead communications channels.

**Clear (CL)**
The state where an alarm condition no longer exists.

**Clear-Channel**
A channel in which all bandwidth is used, with no overhead bits.

**Collocated**
A standalone system in which the interface bays are electrically and physically connected to the Switch Complex.

**Command Mode**
One of two modes used to communicate with the DACS IV-2000. This mode involves entering commands directly into the system without any prompts.

**Communication Interface Link (CILINK)**
Access port that allows users or operations systems (OSs) to communicate with the DACS IV-2000.

**Condition**
The type of alarm failure, such as internal and loss of signal.

**Conference**
To take a signal from a single input port and connect it to multiple output ports.

**Control Cable ID**
Specifies the controller cable (J cable) identification associated with an interface module or a DS3 performance monitor (DS3PM) circuit pack.

**Control Complex (CC)**
A set of circuit packs (CPU/MTC/SSC/SCI/UI) that provide all control functions for the DACS IV-2000. For the redundant controller, two control complexes are provided for increased reliability of the main controller.

**Critical (CR)**
Alarm that indicates a severe, service-affecting condition.

**Cross-Connect**
Hardware used to interconnect line-terminating equipment, multiplexers, and other equipment, allowing access to these facilities and having the ability to change these facilities as required.

**Crosstalk**
An unwanted signal induced into one transmission line from another transmission line.

**Current Value**
In the dialog mode, indicates that the current value of a parameter is used by the system unless you direct otherwise.

# D

**Database**
A record of cross-connections, status of circuit packs and facilities, and other data.

**Default**
A value the system automatically uses for a parameter if the you do not specify a value.

**Delimiter**
A punctuation mark (colon or comma) used to separate two parameters in an input message.

**Demultiplexer**
An electronic device used with a multiplexed signal for recovering signals combined within it and restoring the distinct individual channels of these signals.

**Diagnose**
To test a circuit pack.

**Display Number**
Specifies a TABS display number.

**Double Ampersand (&&)**
Specifies multiple addressed ranges of equipment, links, or ports. For example, 1&&-6 means equipment/link/port locations 1 through 6.

**Driven**
A condition in which an interface with a connection is being monitored.

**DS1GRP**
A group of 28 DS1 ports in an SWIF, MUX, or SMUX [VT1.5(DS1) signals] circuit pack.

**DS1 Port**
Terminates a DS1 signal on a DS1IF (one of fourteen ports), as part of a DS3 signal on a MUX, or as part of an STS-1(VT1.5) signal on an SMUX circuit pack.

**DS1 Signal**
A logical signal with a data rate of 1.544 Mbps (ANSI T1.107). A DS1 signal is produced by combining 192 payload bits and one framing bit; for example, 24 DS0 signals (eight bits per DS0) can be combined with one framing bit, thereby transmitting 193 bits per frame.

**DS2 Signal**
A logical signal with a data rate of 6.312 Mbps (ANSI T1.107). A DS2 signal is produced by combining seven DS1 signals.

**DS3 Clear-Channel Interface-16 Module**
A DS3 Interface-16 Module that contains one to fifteen MUX3 circuit packs, one MUXP3 circuit pack, and no MUX2 circuit packs.

**DS3 Equivalent**
The second item in the address of a port. It refers either to a MUX circuit pack or to an SWIF circuit pack, either of which handles 28 DS1 signals.

**DS3 Format**
Specifies the line format of a DS3 interface port. The initial value is M13, the common multiplexer format.

**DS3 Idle Signal**
A signal that can be optionally applied to any DACS IV-2000 output port that is not cross-connected to any input port. This signal lets downstream network elements know that the facility is operating normally even though the DACS IV-2000 is not sending a normal DS3 signal.

**DS3 Interface Port**
Specifies a DS3 port on a MUX circuit pack. If the value UNIT is given, it indicates all the DS3 interface ports in that DS3 Interface Module.

**DS3 Signal**
A logical or electrical B3ZS signal with a data rate of 44.736 Mbps (ANSI T1.107). For the DACS IV-2000, a traffic-carrying DS3 signal is either framed or unframed (MUX3 only). A framed signal is made up of 28 DS1 signals and control bits used for synchronization and other purposes. The DS3 signal consists of a succession of masterframes approximately 106 µs long. Each masterframe contains seven subframes, each of which consists of eight data blocks. A data block contains one control bit and 84 data bits, with three data bits coming from each of the 28 DS1 signals that make up the DS3 signal. An unframed DS3 is any DS3 conformant to electrical specifications in ANSI T1.102-1994.

**DSX-1, 2, 3**
Digital cross-connect used to interconnect equipment, provide patch capability, and provide test access at the DS1, DS2, or DS3 level.

**Duplex Entity**
A pair of circuit packs in which one is active and the other is in hot standby (clock generators).

**Duplicate Control Complex**
A set of circuit packs (CPU/MTC/SSC/SCI/UI) that provides all control functions for the DACS IV-2000. For the high capacity-controller, the main controller functions are duplicated by the two Control Complexes.

# E

**Echo**
To display an input at a terminal. (A user ID is echoed, but a password is not.)

**Electrical Carrier 1 (EC-1)**
The industry standard nomenclature for an electrical STS-1 signal.

**Electromagnetic Compatibility (EMC)**
A measure of equipment tolerance to external electromagnetic fields.

**Electromagnetic Interference (EMI)**
Interference generated in a circuit by electromagnetic radiation energy coupling.

**Electrostatic Discharge (ESD)**
Static electrical energy potentially harmful to circuit packs and humans.

**Enhanced Bay**
An interface bay containing seismic bay framework.

**Enhanced DS3 Interface-16 Module**
A DS3 Interface-16 Module that contains at least one MUX3 circuit pack and one MUXP3 circuit pack in addition to one or more MUX2 circuit packs.

**Enter**
To provision a circuit pack or interface module by a command, not automatically by the system.

**Entity**
A specific piece of hardware (such as a circuit pack, memory device, or communications link) that has been assigned a name recognized by the system.

**Entity Identifier**
The name used by the system to refer to a circuit pack, memory device, or communications link.

**Equalizer**
A circuit adjustment used to maintain signal strength within desired limits.

**Equipped (EQPT)**
The circuit pack or interface module is in the system database and physically in the frame, but is not yet provisioned.

# F

**Facility**
A one-way or two-way circuit connected to the DACS IV-2000 that carries a transmission signal (such as a DS1 or STS-1 signal).

**Far-end**
Equipment not associated with the DACS IV-2000 frame currently being communicated with over the CILINKs.

**Fault**
The circuit pack has a hard (not temporary) fault and can not provide its normal function.

**Forced**
A traffic-carrying circuit pack (either service or protection) has been deliberately locked into a service-providing state by a manual command despite being bad.

**Frame**
The smallest repetitive block of digital data being transmitted (for example, 193 bits in a DS1 signal, which contains twenty-four 8-bit bytes and a synchronizing frame bit). Also refers to an assembly of equipment units, such as a DACS IV-2000 frame.

# G

**Grooming**
Rearrangement of DS1/VT1.5 signals in DS3/STS-1 signals.

**Group Numbering Method**
The numbering method using the combination of the VT1.5 group and the VT1.5 port for DS1 and VT1.5 signals within STS1 interface modules.

# H

**Hardware ID**
Specifies the hardware identification (type and version) of a circuit pack.

**Header**
The first line of a message.

**Header Date**
Specifies the current date as YYMMDD, where YY is the last two digits of the year, MM is the month, and DD is the day of the month.

**Header Time**
Specifies the current time of day as HHMMSS, where HH is the hour (00 to 23), MM is the minute, and SS is the second.

**Hierarchy**
An orderly ranking or sequence of elements, such as that of menus presented at a terminal.

**Hit**
A momentary disruption of service.

**Hot Standby**
A circuit pack ready for fast, automatic placement into operation to replace an active circuit pack.

# I

**Idle**
An output port is idle if it is not cross-connected to an input port.

**Idle Code**
A signal that is transmitted downstream automatically from an idle output port; it can also be transmitted downstream by a manual command from a cross-connected output port. The DS1 idle code (the same as DS1 alarm indication signal) consists of all ones.

**Input Status**
The input signal status of a DS1, DS3, VT1.5, or STS1 interface port, which can be:

- DRVN (driven) — indicates that a valid signal is expected at the Port, the Port is being monitored for incoming failures, and no incoming failures are currently detected.
- NDRVN (not driven) — indicates that no valid signal is expected at the Port, and the port is not monitored for failures. If the port is formatted, Performance Monitoring data is accumulated.
- INIT (initialized) — is used for an initialized (unset) value (in this case, the port is considered not driven until a valid signal is detected, at which time it becomes DRVN).
- QRSS (quasi-random signal source) — is used to indicate that the DS1 signal is provisioned as the QRSS source for the system. Only one Input Port can be designated as the QRSS Port at any given time. Attempting to specify QRSS for more than one port is denied.

**In-Service**
A state in which the circuit pack is performing normal service functions, in either active or standby mode.

**Intertie**
A facility interface between two DACS IV-2000 systems.

# J

**Jitter**
Short-term variations in timing properties of a digital signal.

# L

**Line**
A transmission medium, together with the associated equipment, required to provide the means of transporting information between two consecutive network elements; one network element originates the line signal and the other terminates the line signal.

**Line Buildout (LBO)**
An attenuating (signal-reducing) element used to keep DS3 or STS-1 output signal strength within desired limits. The line buildout setting for MUX or SMUX circuit packs includes:

- IN — the line buildout is in use, reducing the output signal strength
- OUT — the line buildout is not in use
- INIT — initialized (unset)

**Line Code Type**
Specifies the code type for a DS1 port terminating in a DS1 circuit pack, B8ZS or AMI.

**Line Layer**
The third layer of the standard SONET signal, used for reliable transport of the path layer payload and its overhead across the physical medium. The added overhead is accessed at points where STS signals are formed or terminated. Both lower layers (the photonic and section layers) exist to provide transport for this layer.

**Link ID**
The location and type of a user interface link.

**Literal Character**
A letter, digit, or symbol that is entered in a command. The first hyphen in UNIT-{1-64} is a literal character; the braces and the second hyphen are not literal characters.

**Location**
An identifier for a specific circuit pack, interface module, interface port, or communications link.

**Loopback (LPBK)**
A circuit arrangement that causes a received signal to be returned to its source.

**Loopback State**
Specifies the state of a DS1, VT1.5, or STS1 port loopback:

- LPBKL (line loopback) — loops the signal from an input port to the corresponding output port in the same circuit pack by a connection in the circuit pack
- LPBKT (terminal loopback) — loops the signal from an input port to the corresponding output port in the same circuit pack by a cross-connection in the Switch Module
- LPBKI (internal loopback) — loops the signal from an output port to the corresponding input port of the same circuit pack.

# M

**M13**
A standard format used for DS3 signals, produced by a DS1-to-DS3 multiplexer.

**Major (MJ)**
Indicates a service-affecting failure, main or unit controller failure, or power supply failure.

**Maintenance Condition (MCOND)**
A circuit pack state in which some normal service functions are suspended, either because of a problem or to perform special functions (copy memory) that can not be performed while normal service is being provided.

**Mapped**
Cross-connected.

**Memory Class**
One of two types of memory in the DACS IV-2000: PROG (software release) or DBASE (database).

**Memory Data**
Specifies the data (eight hexadecimal digits) associated with a memory type.

**Memory Location**
Specifies the equipment, DS1 interface port, DS3 MUX port, or STS1 SMUX port location associated with a memory type.

**Memory Type**
Specifies the memory device, which may be:

- WKG — working (system) random access memory
- PRI — primary backup (disk)
- SEC — secondary backup (optical disk).

**Menu/Prompt Mode**
One of two modes used to communicate with the DACS IV-2000. When operating in this mode, the system lets you choose commands from menus and then prompts you for information to complete the command.

**Minor (MN)**
Indicates a non-service-affecting equipment or facility failure.

**Multiplexer**
An electronic device that allows two or more signals to pass over one communications circuit.

**Multipoint Address**
Specifies the Layer 2 (multipoint) address used on a TABS link.

# N

**Near-end**
Equipment associated with the DACS IV-2000 frame that is currently being communicated with over the CILINKs.

**Network Element**
A DACS IV-2000 frame is an example of a network element.

**Notification Code**
The notification code for alarm and status conditions, which includes:

- MJ — major alarm
- MN — minor alarm
- NA — indicates no alarm (status only)
- CL — cleared alarm.

**NOVAL (no value)**
In dialog mode, it indicates that no value is used for this parameter unless you enter one.

**N-Rate Cable**
A cable that carries an N-rate signal (27.648 Mbps), which includes 14 DS1 signals, half of an STS-1(cc-SPE) signal, or 14 STS-1(VT1.5) signals and timing information. There are four N-rate cable groups:

- R1 — from SWIF, MUX, or SMUX to SWIO (or OSWIO)
- X1 — from SWIO (or OSWIO) to SWCS
- Y1 — from SWCS to SWIO (or OSWIO)
- T1 — from SWIO (or OSWIO) to SWIF, MUX, or SMUX.

# O

**Optical Extension (OPEX)**
Circuit pack, module, and bay that allow one or two DACS IV-2000 (256) systems to be optically connected to a DACS IV-2000 (512) Switch Complex.

**Optical Remoting**
The optional feature in which optical fibers and circuit packs connect interface bays. Optical Remoting is used to accomplish capacity expansion.

**Optical Unit Interface (OUI)**
A circuit pack in the High-Capacity Controller that extends the LAN distribution and error summary functions to the Unit Controller and power circuit packs in the interface modules of a Remote Complex.

**Outage**
A disruption of service that lasts for more than 1 second.

**Out-Of-Service (OOS)**
The circuit pack is not providing its normal service function (removed from service or protected) either because of a system problem or because it has been removed from service manually.

**Output Mode**
Specifies what is being transmitted from a DS1, VT1.5, or STS1 output port. The modes are:

- NORM — normal cross-connected data
- TERM (terminated) — idle code
- AIS — alarm indication signal
- QRSS (quasi-random signal source) — an externally generated DS1 test signal, assumed to be quasi-random.

The initial value is NORM.

# P

**Parity Check**
A check that tests whether the number of ones (or zeros) in an array of binary bits is odd or even; used to determine that the received signal is the same as the transmitted signal.

**Path**
A logical connection between the point at which a standard frame format for the signal at the given rate is assembled, and the point at which the standard frame format for the signal is disassembled.

**Path Layer**
The highest of the four layers of a standard SONET signal, used to transport services between path-terminating network elements. Examples of such services include DS1s, DS3s (synchronous and asynchronous), and video signals.

**Path Overhead (POH)**
Informational bytes assigned to, and transported with, the payload until the payload is demultiplexed.

**Payload Pointer**
The pointer that shows the location of the beginning of the synchronous payload envelope (SPE).

**Photonic Layer**
The lowest of the four layers in a standard SONET signal, used to convert STS signals and OC (optical carrier) signals.

**Poll Timing**
Specifies (in seconds) how often the system expects a poll request from a remote telemetry on a TABS link.

**Port**
The point of access on an interface circuit pack that connects the DACS IV-2000 to a DS1, DS3, or STS-1 signal.

**Port Numbering Method**
The numbering method using the sequence of 1 to 28 VT1.5 or VT1.5(DS1) signals within an STS-1 signal.

**Primary Line**
The second line in an output message.

**Program**
The software that directs the operation of the main controller and other frame elements.

**Protocol**
Detailed format and procedures used for transmitting digital data.

**Protocol Type**
Indicates the protocol supported on an interface link.

**Provision**
To set parameters to establish the environment required for correct interaction of hardware, software, and peripherals.

**Provisioned (PROV)**
The circuit pack is ready to perform its intended function. A provisioned circuit pack can be active (ACT), in-service (IS), standby (STBY), provisioned out-of-service (POS), or out-of-service (OOS).

**Pulse Code Modulation (PCM)**
The process by which analog signals are sampled, quantized, and coded into a digital bit stream.

# Q

**Quasi-random Signal Source (QRSS)**
Equipment that generates a specific, reproducible but complicated digital test signal that resembles a normal traffic-carrying DS1 signal.

# R

**Red-lined**
A circuit that is given special protection against unintentional disconnection.

**Released**
If an input port, it is not under test access; if an output port, it is not cross-connected to an input port under test access.

**Remote Complex**
A system in which the interface bays are optically connected but not physically connected in the Switch Complex.

**Remote Unit Interface (RUI)**
The Remote Unit Interface Module is located in a shelf in the OPEX bay. This module replaces the 256 Redundant Controller Module in capacity-expansion applications. The RUI supports the Remote Complex fiber interface to the Optical Unit Interface in the Switch Complex Main Controller.

**Return to Zero**
A code form having two information states termed zero and one and having a third state or an at-rest condition to which the signal returns during each period.

**Rollover**
Operation used when the transmission facility between the system and an upstream system is to be replaced.

# S

**Section**
The portion of a transmission facility, including terminating points, between:

- a terminal network element and a line-terminating network element, or
- two line-terminating network elements.

A terminating point is the point, after single regeneration, at which performance monitoring is done.

**Section Layer**
The second of the four levels in a standard SONET signal, used to transport an STS frame across a physical medium. This layer uses the photonic layer to form the physical transport.

**Sequential Numbering Method**
The numbering method using the sequence of 1 to 28 VT1.5 or VT1.5(DS1) signals within an STS-1 signal.

**Side Switch**
The autonomous action taken when the active Control Complex (CC) fails. A side switch takes up to 5 minutes to complete and switches the standby CC to the active state.

**Single Ampersand (&)**
Specifies multiple addressed equipment, links, or ports. For example, 1&-5 means equipment/link/port locations 1 and 5.

**Snider**
Protocol (message format) used on administrative links.

**Software ID**
Number that provides the software version information for the system. The software ID contains:

- a 1-digit number that indicates the software release
- a 2-digit number that indicates the point release
- a 3-digit number that indicates the issue of the point release
- one letter that indicates the load of the software release.

**Split**
Test access state in which an incoming signal is cross-connected to the receiver of a test set rather than to a previously connected output port, and a signal from the transmitter of the test set is cross-connected to the previously connected output port.

**Standby (STBY)**
The circuit pack is in service but is not providing service functions. It is ready to be used to replace a similar circuit pack either by protection or by duplex switching.

**State**
The state of a circuit pack indicates whether it is defective or normal (ready for normal use).

**STSX-1**
Digital cross-connect used to interconnect equipment, provide patch capability, and provide test access at the STS-1 level.

**STS1 Interface Port**
Specifies an STS1 port on an SMUX circuit pack.

**STS Envelope Capacity**
Bandwidth within, and aligned to, the STS frame that carries the STS SPE.

**STS Path Overhead**
Nine evenly distributed path overhead bytes per 125 µs starting at the first byte of the STS SPE. STS path overhead provides for communications between the point of assembly of an STS SPE and its point of disassembly.

**STS Payload Capacity**
The maximum bandwidth within the STS SPE that is available for payload.

**STS Synchronous Payload Envelope (STS SPE)**
A 125-µs frame structure composed of STS path overhead and bandwidth for payload.

**STS Transport Overhead**
The overhead (informational bytes that contain the line and section overhead) added to the STS SPE for transmission.

**STS-1 Signal**
The basic building block signal in the SONET standard. An STS-1 signal has a data rate of 51.84 Mbps. An STS-1 signal frame consists of 90 columns and 9 rows of 8-bit bytes, for a total of 810 bytes (6480 bits) for a frame length of 125 µs. The first three columns of an STS-1 signal are the transport overhead, which contains overhead bytes of section (nine bytes) and line (eighteen bytes) layers. The remaining 87 columns of 9 rows of bytes (783 bytes) make up the STS-1 envelope capacity.

**Subrate**
In the Digital Data System, a data bit rate that is 2.4, 4.8, or 9.6 kbps.

**Synchronous**
The essential characteristic of time scales or signals such that their corresponding significant instances occur at precisely the same average rate.

**Synchronous Network**
The synchronization of transmission systems with synchronous payloads to a master (network) clock that can be traced to a reference clock.

**Synchronous Payload**
Payloads that can be derived from a network transmission signal by removing integral numbers of bits from every frame; that is, no variable bit-stuffing-rate adjustments are required to fit the payload in the transmission signal.

# T

**T1**
Transmission carrier system at the rate of 1.544 Mbps (same as DS1 signal).

**T2**
Transmission carrier system at the rate of 6.312 Mbps (same as DS2 signal).

**T3**
Transmission carrier system at the rate of 44.736 Mbps (same as DS3 signal).

**Terminated**
Output mode in which idle code is transmitted downstream.

**Test Access**
Allows the DACS IV-2000 the ability to apply and monitor test signals in accordance with Bellcore TA-TSY-000203.

**Test Mode**
Specifies the test access mode.

**Test Signal Identification (TSID)**
Unique name given to a DS1 test signal

**Tributary**
One of the 28 DS1 (1.544 Mbps) channels in a DS3 (44.736 Mbps) signal or one of 28 VT1.5 (1.728 Mbps) channels in an STS-1 (51.84 Mbps) signal.

# U

**User Community Authorization Level (UCAL)**
Specifies the user authorization level: 5 identifies a super user (system administrator); 1 identifies an ordinary user.

**Unit**
An interface module; the term is sometimes used instead of entity or subassembly.

**Unit Type**
Specifies the type of interface module:

- 32DS3 — for DS3 Interface-32 Module
- 16DS3 — for DS3 Interface-16 Module
- 16EDS3 — for Enhanced DS3 Interface-16 Module
- 16DS3CC — for DS3 Clear-Channel (DS3CC) Interface-16 Module
- 16STS1 — for STS1 Interface-16 Module
- DS1 — for DS1 Interface Module
- DS1P — for DS1 Interface-Protection Module.

# V

**Virtual Tributary (VT)**
A structure designed for transporting and switching some STS-1 payloads.

**Volatile Memory**
Type of memory that is lost if electrical power to it is interrupted.

**VT1.5 Port**
Terminates a VT1.5 signal that is part of an STS-1 signal on an SMUX circuit pack.

**VT1.5 Tributary**
A SONET logical signal with a data rate of 1.728 Mbps. In the 9-row structure of the STS-1 SPE, a VT1.5 occupies three columns. VT-structured STS-1 SPEs are divided into seven VT groups. Each VT group occupies twelve columns of the 9-row structure and, for VT1.5s, contains four VTs per group.

**VT Envelope Capacity**
Bandwidth within, and aligned to, the VT Superframe that is available for the VT SPE.

**VT Group**
A 9-row by 12-column structure (108 bytes) that carries one or more VTs of the same size. Seven VT groups (756 bytes) are byte-interleaved within the VT-organized SPE.

**VT Path Overhead**
One path overhead byte per 500 µs located at the first byte of the VT SPE. VT path overhead provides for communication between the point of assembly of the VT SPE and the point of its disassembly.

**VT Payload Capacity**
The maximum bandwidth within the VT SPE that is available for payload.

**VT Superframe**
The VT is organized into a 500-µs superframe structure overlaid on, and aligned to, a 125-µs STS1 SPE. Contained within this structure is the VT payload pointer and the VT SPE.

**VT Synchronous Payload Envelope (VT SPE)**
A 500-µs frame structure carried by the VT, composed of VT path overhead and bandwidth for payload. The envelope is contained within the VT envelope capacity and can have any alignment with respect to it.

# W

**Wideband Digital Cross-Connect System (WDCS)**
A digital cross-connect system that interfaces any one or combinations of SONET, DS3, and DS1 signals and has the basic functionality of cross-connecting at the floating SONET Virtual Tributary 1.5 (VT1.5) or the DS1 level. A SONET WDCS is a DCS that cross-connects at the VT1.5 level and provides SONET signal multiplexing and termination. A DCS 3/1 is a DCS that cross-connects at the DS1 level and provides DS3 multiplexing and termination.

**Wideband Loopback**

The connection of a VT1.5 [VT1.5(cc-SPE) or VT1.5(DS1)] tributary from an incoming STS-1 facility to the outgoing direction of the same facility. This type of loopback differs from a line loopback in that the signal being looped back is not at the line rate, and it is necessary to modify the VT pointer bits to perform the loopback. The DACS IV-2000 implements the wideband loopback as a terminal loopback (the loopback point is in the cross-connect network).

# Acronyms

## Numerics

| | |
|---|---|
| 2ASCCS | 2A Switching Control Center System |
| 2BSCCS | 2B Switching Control Center System |

## A

| | |
|---|---|
| A | Ampere |
| ABN | Abnormal |
| ABS | Absent |
| AC | Alternating Current |
| ACO | Alarm Cutoff |
| ACPWR | AC Power |
| ACT | Active |
| ADM | Add-Drop Multiplixer |
| AI | Asynchronous Interface |
| AIS | Alarm Indication Signal |
| AISFRAMED | Alarm Indication Signal Framed |
| AISL | Alarm Indication Signal, Line |
| AISP | Alarm Indication Signal, Path |
| AISS | Alarm Indication Signal Seconds |
| AISUNFRAMED | Alarm Indication Signal, Unframed |
| ALLDS2OOF | All DS2 Out-of-Frame |
| ALLDS2SOOF | All DS2s within DS3 Signal Out-of-Frame |
| ALLREFFAIL | All Timing References Failed |
| ALW | Allow |
| AMI | Alternate Mark Inversion |
| AS&C | Alarm, Scan, and Control |
| ATTR | Attribute |
| AUTO | Automatic |
| AUX | Auxiliary |
| AVAIL | Available |

## B

| | |
|---|---|
| B3ZS | Bipolar with 3-Zero Substitution |
| B8ZS | Bipolar with 8-Zero Substitution |
| BDFB | Battery Distribution Feeder Board |
| BEC | Block Error Count |
| BER | Bit Error Rate |
| BERL | Line Bit Error Rate |
| BESP | Bursty Errored Seconds, Path |
| BIP-8 | Bit Interleaved Parity-8 |
| BKUPMEMS | Backup Memory Secondary Failure |
| BLK | Blank |
| BNC | Bayonet Navy Connector |
| BOC | Bell Operating Company |
| BPV | Bipolar Variation |
| BXA | Bus Extender A |

## C

| | |
|---|---|
| CANC | Cancel |
| CB | Compatibility Bulletin |
| CC | Control Comple<br>Control Complex |
| cc | Clear Channel |
| CCITT | International Telegraph and Telephone Consultative Committee |
| CD | Compact Disk |
| CE | Capacity Expansion |
| CILINK | Communications Interface Link |
| CIT | Communications Interface Terminal |
| CL | Clear |
| CLKDR | Clock Distributor |
| CLKGN | Clock Generator |
| CMOS | Complementary Metal Oxide Semiconductor |
| COM | Common |
| COMPL | Complete |
| CONTBUS | Control Bus Failure |
| CP-BITS | Copy of Parity Bits |
| CPU | Central Processing Unit |
| CPY | Copy |
| CR | Critical |
| CRC | Cyclic Redundancy Code |
| CRS | Cross-Connect |
| CRT | Circuit |
| CSS | Controlled Slipped Seconds |
| CVL | Code Violations, Line |
| CVP | Code Violations, Path |

## D

| | |
|---|---|
| DACS | Digital Access Cross-Connect System |
| DBCHG | Database Change |
| dc | Direct Current |
| DISC | Disconnect |
| DLI | Data Link Inaccessable |
| DLN | Data Link Not Responding |
| DPLL | Digital Phase Lock Loop |
| DPLL2 | Digital Phase Lock Loop 2 |
| DRVN | Driven |
| DS1 | Digital Signal, Level 1 |
| DS1IF | DS1 Interface |
| DS1IP | DS1 Interface Protection |
| DS1RY | DS1 Relay |
| DS1TX | DS1 Timing Extractor |
| DS1TX2 | DS1 Timing Extractor 2 |
| DS2 | Digital Signal, Level 2 |
| DS3 | Digital Signal, Level 3 |
| DS3cc | DS3 Clear-Channel Cross-Connection |
| DS3FRMTMISMATCH | DS3 Format Mismatch |
| DS3PM | DS3 Performance Monitoring |
| DSX | Digital Signal Cross-Connect |
| DSX-1 | Digital Signal Cross-Connect, Level 1 |
| DSX-3 | Digital Signal Cross-Connect, Level 3 |
| DTAU | Digital Test Access Unit |
| DTLCH | Data Latch Error |

## E

| | |
|---|---|
| EC-1 | Electrical Carrier, Level 1 |
| ECI | Enhanced Communications Interface |
| EMC | Electromagetic Compatibility |
| EMI | Electromagnetic Interference |
| ENT | Enter |
| EOR | End-of-Range |
| EQPT | Equipment<br>Equipment<br>Equipped |
| ERRANAL | Error Analysis |
| ESA | Errored Seconds Type A |
| ESB | Errored Seconds Type B |
| ESD | Electrostatic Discharge |
| ESF | Extended Superframe |
| ESL | Errored Seconds, Line |
| ESP | Errored Seconds, Path |
| EVT | Event |
| EX | Exercise |
| EXJIT | Excessive Jitter |
| EXPHR | Excessive Phase Error |
| EXTERR | Error Detected External to System |
| EXZ | Excessive Zeros |

## F

| | |
|---|---|
| FANAUX | Fan Auxilliary |
| FANFILTER | Fan Filter |
| FANMAIN | Fan Main |
| FBE | Framing Bit Error |
| FCC | Federal Communications Commission |
| FE | Far-End |
| FEAC | Far-End Alarm and Control |
| FEBE | Far-End Block Error |
| FEF | Family of Equipment Failure |
| FERF | Far-End Receive Failure |
| FLT | Fault |
| FMA-BITS | F and M Bits Adjusted |
| FMN-BITS | F and M Bits Nonadjusted |
| FRD | Security Violation has Occurred |
| FRQOF | Frequency Offset Error |
| FS & ALM | Fuse and Alarm |
| FSNLN | Frequency Synthesizer Loss of Energy |
| FSTO | Phase Lock Loop Fast Start Time-out |

## G

| | |
|---|---|
| GRP | Group |
| GTP | General Telemetry Processor |

## H

| | |
|---|---|
| HCC | High-Capacity Controller |
| HDA | Header Designation Assembly |
| HI | High |

## I

| | |
|---|---|
| ICTLR | Interrupt Controller Error |
| ID | Identication |
| IDMISMATCH | Indicates DS3 Path ID Mismatch |
| IDUNREADABLE | Indicates an unreadable DS3 Path ID |
| IHRER | Interrupt Holding Register Error |
| IMPROPBLK | Improper Blank |
| IMPROPRMVL | Improper Removal |
| INC | Incoming |
| INE | Intelligent Network Elements |
| INH | Inhibit |
| INHSWPR | Inhibit Switch to Protection |
| INHSWWKG | Inhibit Switch to Working |
| INIT | Initialized |
| INT | Internal |
| INTFC | Interface |

## L

| | |
|---|---|
| LAN | Local Area Network |
| LBO | Line Buildout |
| LCV | Line Code Violations |
| LERDF | Line Error Detector Failure |
| LOC | Loss-of-Clock |
| LOCL | Local |
| LOF | Loss-of-Frame |
| LOOPE | Loop E |
| LOOPF | Loop F |
| LOP | Loss-of-Pointer |
| LOS | Loss-of-Signal |
| LOSS | Loss-of-Signal Seconds |
| LPBK | Loopback |
| LPBKI | Internal Loopback |
| LPBKL | Line Loopback |
| LPBKM | DS1 Tributary Loopback |
| LPBKT | Terminal Loopback |

## M

| | |
|---|---|
| MAN | Manual |
| MC | Main Controller |
| MCOND | Maintenance Condition |
| MEM | Memory |
| MHz | Mega Hertz |
| MINC | Mulitple Incoming |
| MJ | Major |
| MML | Human-Machine Language |
| MN | Minor |
| MONE | Monitor E |
| MONEF | Monitor E F |
| MONF | Monitor F |
| ms | Millisecond |
| MTC | Maintenance |
| MTCE | Maintenance |
| MUX | Multiplexer |
| MUXP | Multiplexer Protection |
| MUXPS | Multiplexer Protection Switch |

## N

| | |
|---|---|
| NA | No Alarm<br>Not Available |
| NDF | New Data Flag |
| NDRVN | Not Driven |
| NE | Network Element |
| NMA | Network Monitoring Analysis |
| NORM | Normal |
| NOVAL | No Value |
| NSA | Non-Service Affecting |

## O

| | |
|---|---|
| OC | Optical Carrier |
| OC-12 | Optical Carrier, Level 12 |
| OC-3 | Optical Carrier, Level 3 |
| OC-48 | Optical Carrier, Level 48 |
| OOF | Out-of-Frame |
| OOFS | Out-of-Frame Seconds |
| OOS | Out-of-Service |
| OPEX | Optical Extension |
| OPS | Operations Systems |
| OPS/INE | Operations System/Intelligent Network Element |
| OR | Optical Remoting |
| OS | Operations System |
| OSWIO | Optical Switch Input/Output |
| OUI | Optical Unit Interface |

## P

| | |
|---|---|
| PAD | Packet Assembler and Disassembler |
| PCM | Pulse Code Modulation |
| PFLCH | Phase/Frequency Latch Error |
| PHSTP | Phase Step Error |
| PLL | Phase Lock Loop |
| PMGR | Performance Monitoring Generator/Receiver |
| PMREP | Performance Monitoring Report |
| POH | Path Overhead |
| POS | Provisioned Out-of-Service |
| PRI | Primary Storage |
| PRTL | Partial |
| PSET#1 | Parameter Set 1 |
| PSET#2 | Parameter Set 2 |
| PSHLN | Phase Shifter Output Loss-of-Energy |
| PTE | Path Terminating Equipment |
| PTY | Parity |
| PWR | Power |
| PWRA | Power A |
| PWRE | Power E |
| PWRF | Power F |
| PWRG | Power G |
| PWRJ | Power J |

## Q

| | |
|---|---|
| QRSS | Quasi-Random Signal Source |

## R

| | |
|---|---|
| RAM | Random Access Memory |
| RAMER | RAM Error |
| RBOC | Regional Bell Operating Company |
| RCI | Remote Communications Interface |
| RL | Retry Later |
| RLS | Release |
| RMS | Remote Management System |
| ROLL | Rollover |
| ROM | Read-Only Memory |
| ROMER | ROM Error |
| RST | Restore |
| RTRV | Retrieve |
| RTV | Real-Time Violation |
| RUI | Remote Unit Interface |
| RX | Remote Complex |

## S

| | |
|---|---|
| SA | Service Affecting |
| SARTS | Switched Access Remote Testing System |
| SBIT | DS3 Stuff Bit Protocol |
| SBITFAIL | S Bits Failure |
| SCCS | Switching Control Center System |
| SCHED | Schedule |
| SCI | Switch Communications Interface |
| SEC | Secondary Storage |
| SEFS | Severly Errored Frame Seconds |
| SESL | Severly Errored Seconds, Line |
| SESP | Severly Errored Seconds, Path |
| SF | Superframe |
| SLMF | Signal Label Match Failure |
| SLS | Slipped Seconds (see CSS) |
| SMUX | SONET Multiplexer |
| SMUXP | SONET Multiplexer Protection |
| SONET | Synchronous Optical Network |
| SPE | Synchronous Payload Envelope |
| SPLTA | Split A |
| SPLTB | Split B |
| SPLTE | Split E |
| SPLTEF | Split E F |
| SPLTF | Split F |
| SRV | Service |
| SSC | Secondary Storage Controller |
| SSS | Secondary Storage Subsystem |
| STBY | Standby |
| STPNL | Status Panel |
| STS-1 | Synchronous Transport Signal, Level 1 |
| SW | Switch |
| SWCS | Switch Center Stage |
| SWIF | Switch Interface |
| SWIO | Switch Input/Output |
| SWSLMF | Switch Signal Label Match Failure |
| SYNC | Synchronizer |
| SYNCCLK | Synchronizer Clock Failure |
| SYNCFRNG | Synchronizer Transitioned to Free-Running Mode |
| SYNCFST | Synchronizer Transitioned to Fast-Start Mode |

| | |
|---|---|
| SYNCHLDOVR | Synchronizer Transitioned to Holdover Mode |
| SYNCN | Synchronizer |
| SYNCPRI | Primary Timing Reference |
| SYNCSEC | Secondary Timing Reference |
| SYPLN | Sync Pulse Generator Loss-of-Energy |

## T

| | |
|---|---|
| T+BER | Bit Error Rate Threshold Exceeded |
| TA | Technical Advisory |
| TABS | Telemetry Asynchronous Block Serial |
| TACC | Test Access |
| TAP | Test Access Port |
| TB | Time Base (TBS3) |
| TBCOLD | Time Base Oven Cold |
| T-BER | Bit Error Rate Threshold |
| T-BERL | Line Bit Error Rate Threshold |
| TBIOER | Time Base Communication Error |
| TBLEN | Time Base Strobe Loss-of-Energy |
| TBNDF | Time Base Strobe Energy Detector Failure |
| TBS3 | Time Base Stratum 3 |
| TCA | Threshold Crossing Alert |
| TERM | Terminated |
| TH | Threshold |
| TL1 | Transaction Language 1 |
| TMAS | Transport Maintenance Administration System |
| TNM | Total Network Management |
| TODC | Time-of-Day Clock |
| TOPROTN | To Protection |
| TOWKG | To Working |
| TPA | Errored Seconds, Type A |
| TPB | Errored Seconds, Type B |
| TPC | Errored Seconds, Type C |
| TR9 | TR-TSY-000009 Remote Multiplexer |
| TRANSID | Transport Self-Identification |
| TRBER | High Bit Error Rate |
| TRMNBER | Minor Bit Error Rate |
| TSID | Test Signal Identification |
| TSTF | Tests Failed |
| TTY | Terminal Typewritter |
| TX | Timing Extractor (DS1TX) |

## U

| | |
|---|---|
| UART | Universal Asynchronous Receiver/ Transmitter |
| UAS | Unavailable Seconds |
| UC | Unit Controller |
| UCAL | User Community Authorization Level |
| UI | Unit Interface |
| UIA | Unit Interface A |
| UIB | Unit Interface B |
| UNF | Unframed |
| UPC | User Privilege Code |
| URTER | UART Error |

## V

| | |
|---|---|
| V | Volt |
| Vdc | Volts direct current |
| VT | Virtual Tributary |
| VT1.5 | Virtual Tributary, Level 1.5 |

## W

| | |
|---|---|
| WDCS | Wideband Digital Cross-Connect System |
| WRNGPWR | Wrong PWRJ circuit packs installed |

## X

| | |
|---|---|
| X1LEN | Synchronizer 1 ms Cross-Couple Loss-of-Energy |
| X3LEN | Synchronizer 30 ms Cross-Couple Loss-of-Energy |
| XCOOL | Synchronizer Cross-Couple Out-of-Lock Error |
| XCRTV | Synchronizer Cross-Couple Real-Time Violation Error |
| XCSUM | Synchronizer Cross-Couple Summary Error |
| XFLRG | Synchronizer Cross-Couple Fast Lock Range Error |
| XFQOF | Synchronizer Cross-Couple Frequency Offset Error |
| XLKDN | Synchronizer Cross-Couple Communication Link Error |

## Y

| | |
|---|---|
| YEL | Yellow Signal |

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