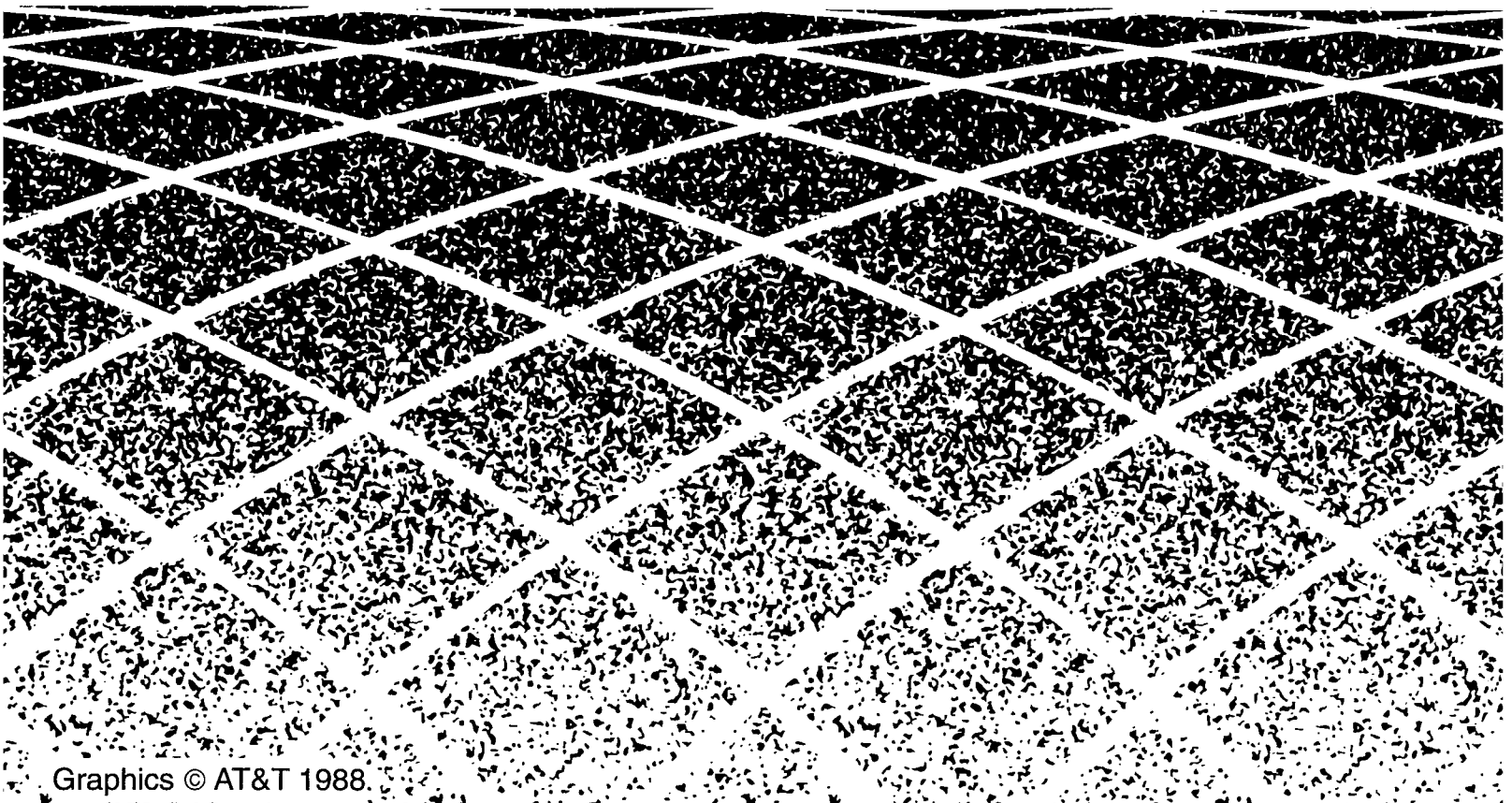
AT&T 365-340-700
April, 1995

# DACS IV-2000 (256) Digital Access and Cross-Connect System IV-2000 Release 4.0

## Reference Manual



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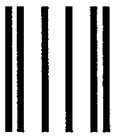

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# Preface

## Purpose

This manual provides detailed, functional descriptions of the system architecture, hardware, software, configurations, and features for the DACS IV-2000 (256) Release 4.0.

New features described in this manual include enhancements to the Synchronizer Module and the Secondary Storage Subsystem, visual indication for circuit packs that have been manually switched to protection, as well as a new configuration for duplex power input.

## Audience

This manual is intended for network planners, administrators, maintenance engineers, and technical personnel who require an in-depth knowledge of the DACS IV-2000.

## Document Summary

The parts of this document are summarized below:

- **Preface** includes the purpose, the audience, and a summary of this document. It also lists referenced and related documents and ordering instructions.
- **Chapter 1 - Introduction** offers a brief overview of the AT&T 2000 family of transmission products and an overview of the DACS IV-2000 and its benefits.
- **Chapter 2 - System Features** details major features of the DACS IV-2000.
- **Chapter 3 - Hardware** describes the major components of the DACS IV-2000, which are the equipment bays, modules, and circuit packs.
- **Chapter 4 - User Interfaces** describes the format of commands and messages, system addressing, user passwords, user/superuser privileges, administrative links, and indicators and switches for the DACS IV-2000.
- **Appendix A - Technical Specifications** contains technical specifications of the DACS IV-2000.
- **Appendix B - Alarm, Scan, and Control Points** contains information describing the interface between the DACS IV-2000 and telemetry operating systems (OSs).
- **Glossary** gives definitions of terms used in the DACS IV-2000 documents.
- **Acronyms** gives definitions of acronyms used in this document.
- **Index** gives page locations of information used in this document.

## Print Conventions

The following print conventions are used in this manual.

- *Italic* type is used for documentation titles, primarily AT&T customer documents and Bell Communications Research (Bellcore) technical references, technical advisories, and ANSI standards
- `Constant Width Bold` type is used for information you input, primarily commands
- `Constant Width` is used for information the system outputs, primarily messages.

# Referenced Documents

Table 2 is a list of Bellcore documents referenced in this document, providing additional technical information, specifications or other supporting data.

Table 1. **Bellcore Reference Documents**

| Document Number | Document Title |
|---|---|
| TR-TSY-000009 | *Asynchronous Digital Multiplexer Requirements and Objectives* (Issue 1, May 1986) |
| TR-NWT-000063 | *Network Equipment-Building System (NEBS) Generic Equipment Requirements (A Module of LSSGR, FR-NWT-000064 and of TSGR, FR-NWT-000440)* (Issue 5, September 1993) |
| FR-NWT-000064 | *LATA Switching Systems Generic Requirements (LSSGR): 1993 Edition* (Issue 93, February 1993) |
| TR-TSY-000179 | *Software Quality Program Generic Requirements (SQPR) (A Module of ROGR, FR-NWT-000796)* (Issue 2, June 1993) |
| TR-TSY-000191 | *Alarm Indication Signal Requirements and Objectives (A Module of TSGR, FR-NWT-000440)* (Issue 1, May 1986) |
| TA-NWT-000199 | *Specification of Memory Administration Messages at the OS/NE Interface* (Issue 7, January 1993) |
| TA-NWT-000200 | *Specification of System Maintenance Messages at the OS/NE Interface* (Issue 5, December 1990) |
| TR-NWT-000233 | *Wideband and Broadband Digital Cross-Connect Systems Generic Criteria* (Issue 3, November 1993) |
| TA-TSY-000241 | *Electronic Digital Signal Cross-Connect (EDSX) System Generic Requirements and Objectives (Issue 4, July 1989)* |
| TR-NWT-000253 | *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria (A Module of TSGR, FR-NWT-000440)* (Issue 8, October 1993) |
| TR-TSY-000282 | *Software Reliability and Quality Acceptance Criteria (SRQAC) (A Module of ROGR, FR-NWT-000796)* (Issue 1, December 1986) |

Table continued on next page.

Table 1. **Bellcore Reference Documents (Continued)**

| Document Number | Document Title |
|---|---|
| TR-NWT-000332 | *Reliability Prediction Procedure for Electronic Equipment (A Module of ROGR, FR-NWT-000796)* (Issue 5, September 1992) |
| TR-NWT-000499 | *Transport Systems Generic Requirements (TSGR): Common Requirements (A Module of TSGR, FR-NWT-000440)* (Issue 4, Revision 1, April 1992) |
| TR-NWT-000811 | *OTGR: Operations Application Messages - TL1 Message Index* (Issue 2, May 1992) |
| TR-NWT-000818 | *OTGR Section 6.1: Network Maintenance: Access and Testing - Generic Test Architecture* (Issue 1, November 1992) |
| TR-TSY-000820 | *OTGR: Network Maintenance: Transport Surveillance - Generic Digital Transmission Surveillance, Section 10.1 (A Module of OTGR, FR-NWT-000439)* (Issue 2, February 1988) |
| TR-TSY-000824 | *OTGR: User System Interface User System Access, Section 10.1 (A Module of OTGR, FR-NWT-000439)* (Issue 2, February 1988) |
| TR-NWT-000833 | *OTGR: Operations Application Messages Network Maintenance: Generic Requirements for Network Element and Transport Surveillance Messages, Section 12.3 (A Module of OTGR, FR-NWT-000439)* (Issue 5, Revision 2, April 1993) |
| TR-NWT-000835 | *OTGR: Operations Application Messages - Network Element (NE) Security Parameter Administration Messages, Section 12.5 (A Module of OTGR, FR-NWT-000439)* (Issue 3, Revision 1, May 1991) |
| TR-NWT-001089 | *Electromagnetic Compatibility and Electrical Safety Generic Criteria for Network Telecommunications Equipment (A Module of LSSGR, FR-NWT-000064 and TSGR, FR-NWT-000440)* (Issue 2, June 1993) |
| TR-NWT-001213 | *Objectives for the Maintenance User Interface of Switching Systems and Transport Systems (Issue1, March 1992)* |
| TR-NWT-001244 | *Clocks for the Synchronized Network: Common Generic Criteria (Issue 1, June 1993)* |

Table continued on next page.

Table 1. **Bellcore Reference Documents (Continued)**

| Document Number | Document Title |
|---|---|
| TA-NWT-001339 | *General Reliability Requirements for Digital Cross-Connect Systems* (Issue 1, November 1993) |
| SR-STS-001578 | *OPS/INE Generic Interface Support* (Issue 2, December 1992) |
| SR-STS-001665 | *Network Monitoring and Analysis Generic Network Element Interface Support* (Issue 2, December 1992) |

Table 2 is a list of ANSI standards referenced in this document, providing additional technical information, specifications or other supporting data.

Table 2. **American National Standards Institute Documents**

| Document Number | Document Title |
|---|---|
| ANSI T1.105 | *Digital Hierarchy - Optical Interface Rates and Formats Specifications (SONET) - 1991* |
| ANSI T1.107 | *Telecommunications - Digital Hierarchy - Supplement to Formats Specifications (Synchronous Digital Data Format); Supplement T1.107A - 1990, Supplement T1.107B - 1991 (ESCA)* |
| ANSI T1.107a | *Telecommunications - Digital Hierarchy - Supplement to Formats Specifications (Synchronous Digital Data Format); Supplement T1.107A - 1990, Supplement T1.107B - 1991 (ESCA)* |
| ANSI T1.403 | *Carrier-to-Customer Installation - DS1 Metallic Interface* |
| ANSI T1M1.3 | *These are standards in draft form, dealing with telecommunications maintenance/performance issues.* |

## Related Documents

The following documents provide additional information about the DACS IV-2000 and can be ordered after the general availability date of this release:

- *DACS IV-2000 (256) Release 4.0 Operations and Maintenance*
  AT&T 365-340-701

  This manual provides detailed procedures for daily operations, trouble-clearing procedures, and routine maintenance of the DACS IV-2000 (256).

- *DACS IV-2000 (256) Release 4.0 Commands and Messages*
  AT&T 365-340-702

  This manual gives a description of each command and its associated output response messages, including error codes. The appendices include command name, parameter, and state modifier acronym tables, activity menus, user privilege codes, state names, and state diagrams.

- *DACS IV-2000 (256) Release 4.0 Quick Reference Job Aids*
  AT&T 365-340-703

  These aids are produced on laminated sheets and contain command names, error codes, fuse locations, test access, port addressing, loopbacks, and monitored parameter default and range values.

- *DACS IV-2000 (256) Release 4.0 Applications, Planning, and Ordering*
  AT&T 365-340-704

  This guide is designed for network planners, account representatives, account executives, and engineers. It contains descriptions of DACS IV-2000 features, applications, and ordering information.

- *DACS IV-2000 (256) Release 4.0 Software Release Description*
  AT&T 365-340-705

  This document contains upgrade procedures for the new software release. It relates status of problems fixed in previous releases, and operating issues for the current software release. (This document can not be ordered as a stand-alone item; it only accompanies the software.)

## Electronic Documentation

AT&T DACS IV-2000 customer documentation is available on CD-ROM. Consult your AT&T account executive for details.

## Ordering Documents

To order copies of documents available for this release, send or call in an order using the title and its associated 9-digit document number as provided above:

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# Introduction

# 1

## Contents

# Contents

# Introduction

# 1

The DACS IV-2000 (256) Release 4.0 is a software-based, high-capacity, digital cross-connect system that merges cross-connect and multiplexer functions. It helps manage DS1, DS3, and EC-1[1] (and in the future OC-3) facilities more efficiently by automating network route restoration, remote service and facility provisioning, and remote surveillance and test access. Its software-controlled cross-connect facility allows centralization and automation of operation, administration, maintenance, and provisioning functions.

The DACS IV-2000 can terminate DS1, DS3, and STS-1 signals and can cross-connect DS1, STS-1, and VT1.5 signals from transmission facilities or from DS1, DS3, and/or STS-1 based network elements. All cross-connections are done at the 1.728 Mbits/s signal level. In the case of an STS-1 clear-channel Synchronous Payload Envelope (cc-SPE) signal, a group of 30 1.728 Mbits/s are used. DS3 signals are demultiplexed within the DACS IV-2000 into 28 DS1 signals to access the switch network. Each STS-1 signal is either cross-connected as a clear-channel STS-1 signal or is demultiplexed as 28 VT1.5 tributaries, which can be cross-connected as VT1.5 or DS1 signals.

A wide range of termination mixes is supported by the system architecture. The number of ports allocated to DS1, DS3, or EC-1 terminations depends on the particular application. The extreme cases are when all of the ports are allocated for DS1 signals (6944 DS1s), DS3 signals (248 DS3s), or STS-1 signals (240 STS-1s).

The DACS IV-2000 accommodates SONET interfaces (STS-1 signals) to support SONET-to-SONET cross-connections as well as providing a gateway between asynchronous and SONET networks.

1. Electrical Carrier-1 (EC-1) is the industry standard nomenclature for an electrical STS-1 signal.

The equipment architecture reduces start-up configuration costs, provides modular growth capability, and allows for reduced floor space. These benefits allow the DACS IV-2000 to be deployed economically in any size office.

## AT&T 2000 Product Family

AT&T is focused on a carefully planned and growing product family designed to provide total network solutions. The 2000 Product Family complies with the SONET standard and builds on items that customers have found necessary to build an efficient and successful network. It includes single-ended maintenance features and in-service upgrade capabilities. The system's modular design allows graceful in-service upgrades to accommodate both synchronous and asynchronous network communications.

The AT&T 2000 product family includes:

- FT-2000 OC-48 Lightwave System — a high-capacity, synchronous digital transmission system.
- DDM-2000 OC-3/OC-12 Multiplexer — a low-capacity, synchronous digital transmission system. The DDM-2000 OC-3/OC-12 multiplexer is designed for loop feeder or interoffice applications.
- DACS III-2000 Cross-Connect System — a software-based, high-capacity, digital cross-connect system that automates many functions performed by manual DSX-3 cross-connect frames.
- DACS IV-2000 Cross-Connect System — a software-based, high-capacity, digital cross-connect system that merges cross-connect and multiplexer functions. It provides interfaces at the STS-1/DS3/DS1 signal rates and cross-connects at the STS-1/VT1.5/DS1 signal levels.
- DACScan®-2000 Controller — a workstation that automates control over diversely located network elements, such as the DACS III-2000 and DACS IV-2000 cross-connect systems.
- SLC®-2000 Access System — a system that supports standard switch interfaces such as TR08 and TR303, as well as standard feeder interfaces at DS1 and SONET OC-3 rates.
- Business Remote Terminal-2000 (BRT-2000) — a terminal that provides access for businesses through sophisticated fiber-optic telecommunications equipment.

# System Overview

This section gives an overview of the DACS IV-2000 by describing the system functionality and architecture.

## System Functionality

The following sections explain the DACS IV-2000 in terms of system capacity, signal types and how they function within the system, and the manner in which cross-connections, bridging, grooming, and monitoring are performed.

### System Capacity

The electronic digital switch in a fully equipped DACS IV-2000 can cross-connect any of the following signal types:

- A maximum of 6944 DS1 signals
- A maximum of 240 STS-1 signals
- A maximum of 6720 VT1.5 tributaries of STS-1 signals
- Various combinations of the above (not exceeding the switch capacity of 6944 DS1/6720 VT1.5/240 STS-1).

A wide range of termination mixes is supported by the system architecture. The number of ports allocated to DS1, DS3, and STS-1 terminations depends on the application in use. In extreme cases, all ports are allocated for DS1 (6944 DS1s), DS3 (248 DS3s), or STS-1 (240 STS-1s) signals.

### Signal Types

The DACS IV-2000 can process the following signal types: Digital Signal, level 1 (DS1); Digital Signal, level 3 (DS3); Synchronous Transport Signal, level 1 (STS-1); and Virtual Tributary, level 1.5 (VT1.5).

#### DS1 Signal

A DS1 is a logical signal with a data rate of 1.544 Mbit/s (ANSI T1.107). A DS1 signal is produced by combining 24 DS0 signals (8 bits per DS0) and one synchronizing bit, thereby transmitting 193 bits per frame.

DS1 signals can arrive at the frame in any of three ways:

- On DS1 transmission facilities
- As tributaries (components) on DS3 transmission facilities
- As tributaries [VT1.5(DS1)] on Electrical Carrier-1 (EC-1) facilities.

## DS3 Signals

A DS3 signal is a logical or electrical Bipolar with Three-Zero Substitution (B3ZS) signal with a data rate of 44.736 Mb/s (ANSI T1.107). A traffic-carrying DS3 signal is made up of 28 DS1 signals and control bits used for synchronization and other purposes. The DS3 signal consists of a succession of masterframes approximately 106 μs long. Each masterframe contains seven subframes, each of which consists of eight data blocks. A data block contains one control bit and 84 data bits, with three data bits coming from each of the 28 DS1 signals that make up the DS3 signal.

Network elements (NEs), such as the DACS IV-2000, use the control bits to demultiplex the DS3 signals and determine whether to add stuff bits to maintain synchronization of the DS3 signals. DS3 signals arrive at the frame as DS3 facilities.

## STS-1 Signals

An STS-1 is the basic building block signal in the SONET standard ANSI T1.105 and Bellcore TR-TSY-000253. An STS-1 signal has a data rate of 51.84 Mb/s. An STS-1 signal frame consists of 90 columns and 9 rows of 8-bit bytes, for a total of 810 bytes (6480 bits) for a frame length of 125 μs. The first three columns of an STS-1 signal are the transport overhead, which contain overhead bytes of section (9 bytes) and line (18 bytes) layers. The remaining 87 columns of 9 rows of bytes (783 bytes) carry the STS-1 synchronous payload envelope (SPE).

The first column of an SPE defines the STS-1 path overhead (POH), and the remaining columns are available for the payload. The STS-1 SPE can begin anywhere in the STS-1 envelope capacity. (Typically, an STS-1 SPE begins in one frame and ends in the next, although an STS-1 SPE can be wholly contained in one frame.)

The STS-1 payload pointer contained in the transport overhead defines the beginning of the STS-1 SPE. The STS-1 POH is associated with each payload and is used to communicate functions from the point where a service is mapped into the STS-1 SPE to its delivery point.

The DACS IV-2000 can process any of the following information supplied by an STS-1 SPE:

- STS-1 [Virtual Tributary, level 1.5 STS-1 (VT1.5)] — is an STS-1 signal in which the SPE contains 28 floating VT1.5 signals and access to the VT1.5s by the DACS IV-2000 is required. Virtual tributaries are used to transport sub-STS-1 payloads.
- STS-1 [clear channel SPE STS-1 (cc-SPE)] — is an STS-1 signal in which the SPE contents are arbitrary (that is, the SPE can contain 28 VT1.5s, one DS3cc, or some unspecified payload) and access to the payload by the DACS IV-2000 is not required.

STS-1 signals arrive at the frame as EC-1 facilities.

### VT1.5 Signals

A VT1.5 signal is a subrate of a SONET STS-1 logical signal and has a data rate of 1.728 Mb/s. In the 90-column, 9-row structure of the STS-1 SPE, a VT1.5 occupies 3 columns.

VT-structured STS-1 SPEs are divided into 7 VT groups. Each VT group occupies 12 columns of the 9-row structure. The 12-column VT group structure can accommodate four 3-column VT1.5s per group.

The floating mode of operation (supported by the DACS IV-2000) minimizes delay for distributed VT switching.

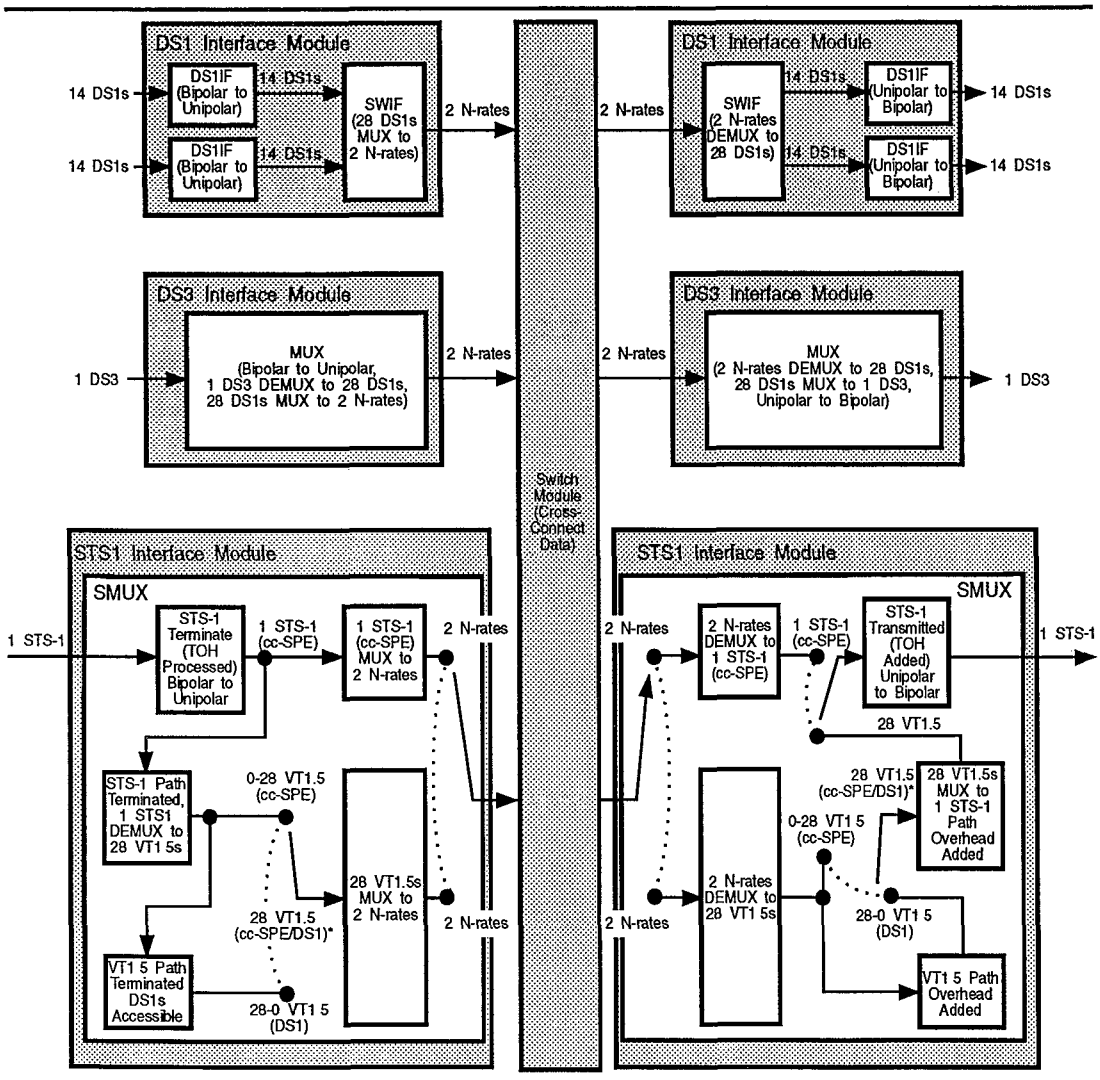
The DACS IV-2000 can accept the following VT1.5 mappings (signal formats are defined in the Bellcore TR-NWT-000253):

- VT1.5 clear-channel SPE (cc-SPE) — is a VT1.5 signal in which the SPE contents are arbitrary and access to the payload by the DACS IV-2000 is not required. VT1.5(cc-SPE) signals processed by the DACS IV-2000 must use the floating mode of operation. They can be mapped as:
  - — Asynchronous — clear channel transports that meet DSX-1 requirements [Bellcore TR-TSY-000499]
  - — Byte-synchronous — allows downstream SONET network elements direct identification and access to the 24 DS0 channels that are carried
  - — Bit-synchronous — special case mapping of a DS1 signal in the floating VT mode.
- VT1.5(DS1) — is a VT1.5 signal in which the SPE contains one DS1 signal and access to the DS1 signal is required by the DACS IV-2000. VT1.5(DS1) signals processed by the DACS IV-2000 must use the floating mode of operation and must be mapped as asynchronous.

VT1.5 signals can arrive at the frame only as tributaries of EC-1 facilities.

## Signal Paths

To support the different types of signals, the DACS IV-2000 provides DS1, DS3, and STS1 Interface Modules. These modules receive and process the signals, send them to the VT1.5/DS1 switch for cross-connection, regenerate the cross-connected signals, and transmit the signal downstream. Figure 1-1 shows the paths of different signal types (DS1, DS3, and STS-1) within the DACS IV-2000.




* VT1.5(cc-SPE) and VT1.5(DS1) are cross-connected on a per-tributary basis. The 28 tributaries that make up a STS-1 signal can contain a mix of VT1.5(cc-SPE) and VT1.5(DS1) signals totalling 28.

Figure 1-1. DS1, DS3, and STS-1 Signal Paths

## DS1 Signals

In the receive stage, 28 DS1 signals are received (see Figure 1-2) by a DS1 interface group (two DS1IF and one SWIF circuit packs) within a DS1 Interface Module. Each DS1IF circuit pack converts 14 DS1 signals from bipolar to unipolar and sends the signals to the SWIF circuit pack. The SWIF circuit pack multiplexes 28 DS1 signals into two N-rate signals (27.648 MHz) and sends the N-rate signals to the SWIO Module for cross-connection.

In the transmit stage, the SWIF circuit pack receives two N-rate signals containing cross-connected DS1 signals from a DS1, DS3, or STS1 Interface Module and demultiplexes the N-rate signals into 28 DS1 signals. Each DS1IF circuit pack receives 14 DS1 signals from the SWIF circuit pack, converts the signals from unipolar to bipolar, and transmits the 14 DS1 signals downstream.

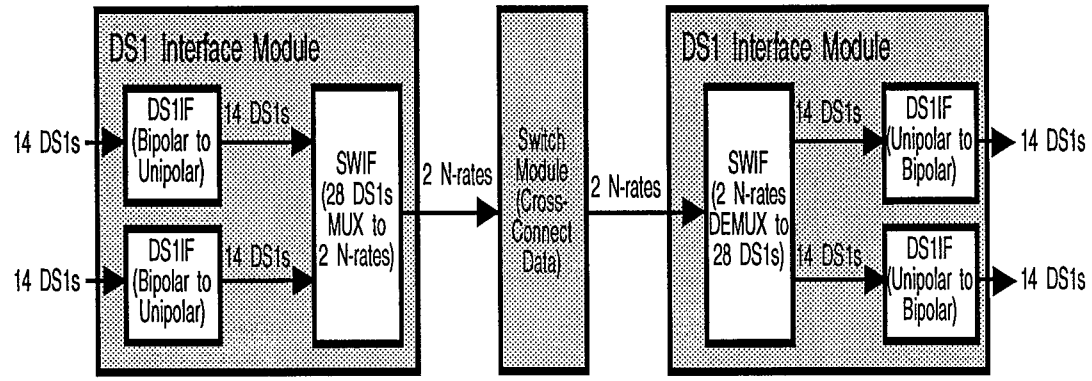



Figure 1-2. DS1 Signal Path via DS1 Interface Modules

### DS3 Signals

In the receive stage, a single DS3 signal is received by a MUX circuit pack within a DS3 Interface Module (see Figure 1-3). The MUX circuit pack converts the DS3 signal from bipolar to unipolar, demultiplexes the DS3 signal into 28 DS1 signals, multiplexes the 28 DS1 signals into two N-rate signals, and sends the N-rate signals to the SWIO Module for cross-connection.

In the transmit stage, the MUX circuit pack receives two N-rate signals containing cross-connected DS1 signals from a DS1, DS3, or STS1 Interface Module;, demultiplexes the N-rate signals into 28 DS1 signals; multiplexes the 28 DS1 signals into one DS3 signal; converts the DS3 signal from unipolar to bipolar; and transmits the DS3 signal downstream.

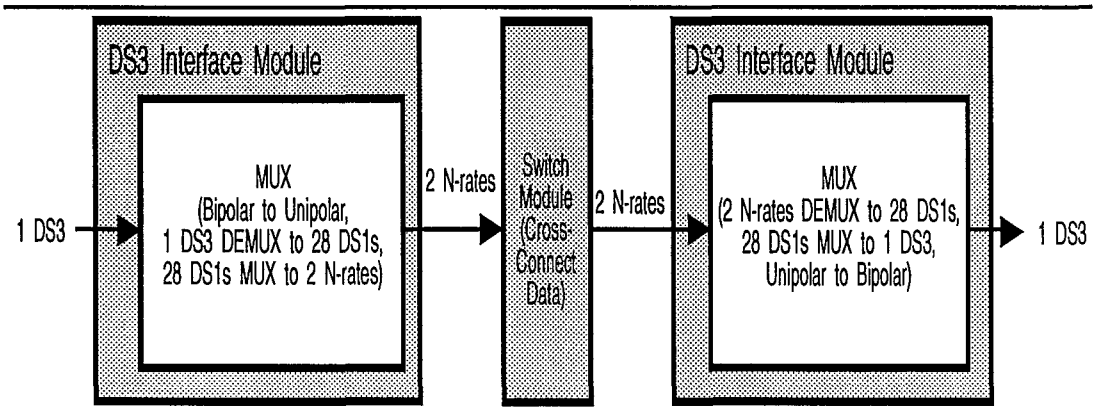
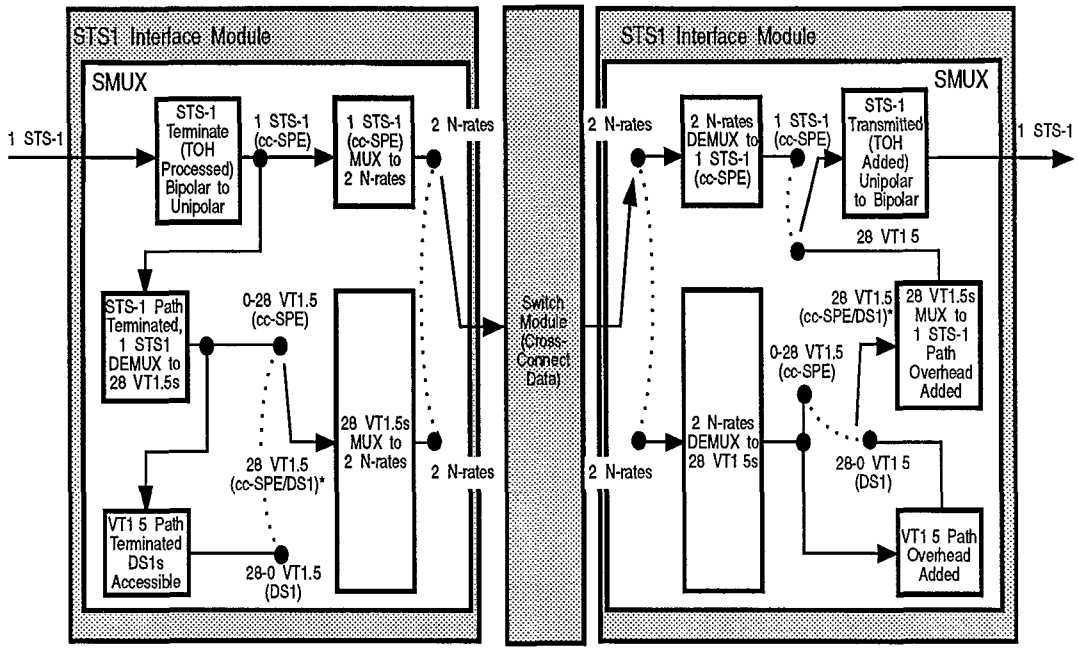



Figure 1-3. DS3 Signal Path via DS3 Interface Modules

### STS-1 Signals

In the receive stage, a single STS-1 signal is received by an SMUX circuit pack within an STS1 Interface Module (see Figure 1-4). The SMUX circuit pack terminates the transport overhead of the STS-1 signal and converts the STS-1 signal from bipolar to unipolar. Depending on the information to be cross-connected, the SMUX circuit pack performs the following functions:

- STS-1(cc-SPE) — the SMUX circuit pack demultiplexes the STS-1 signal into two N-rate signals and sends the N-rate signals to the SWIO Module for cross-connection. Cross-connecting an STS-1 signal as an STS-1(cc-SPE) signal preserves the path of the STS-1 signal through the DACS IV-2000.
- VT1.5(cc-SPE) — the SMUX circuit pack terminates the STS-1 path and demultiplexes the STS-1 signal into 28 VT1.5 tributaries. Each tributary that is to be cross-connected as a VT1.5(cc-SPE) signal receives no more processing before being multiplexed into two N-rate signals and sent to the SWIO Module for cross-connection. Cross-connecting VT1.5 tributaries as a VT1.5(cc-SPE) preserves the path of the VT1.5 tributary through the DACS IV-2000.




* VT1.5(cc-SPE) and VT1.5(DS1) are cross-connected on a per-tributary basis. That is, the 28 tributaries that make up a STS-1 signal can contain a mix of VT1.5(cc-SPE) and VT1.5(DS1) signals totalling 28.

Figure 1-4. **STS-1 Signal Path via STS1 Interface Modules**

- VT1.5(DS1) — the SMUX circuit pack terminates the STS-1 path and demultiplexes the STS-1 signal into 28 VT1.5 tributaries. Each tributary that is to be cross-connected as a VT1.5(DS1) signal has the VT1.5 path terminated so that the DS1 signal can be accessed before being multiplexed into two N-rate signals and sent to the SWIO Module for cross-connection. This allows the DACS IV-2000 to cross-connect DS1 signals to and from STS1 interfaces, providing the synchronous/asynchronous gateway.

In the transmit stage, the SMUX circuit pack receives two N-rate signals containing cross-connected signals from a DS1, DS3, or STS1 Interface Module for VT1.5(DS1) signals, or an STS1 Interface Module for STS-1(cc-SPE) and VT1.5(cc-SPE) signals. Depending on the type of signals received from the SWIO Module, the SMUX circuit pack performs the following functions:

- STS-1(cc-SPE) — the SMUX circuit pack multiplexes the N-rate signals into one STS-1 signal.
- VT1.5(cc-SPE) — the SMUX circuit pack demultiplexes the N-rate signals into 28 VT1.5 tributaries. For tributaries that are cross-connected as VT1.5(cc-SPE) tributaries, no other processing is performed before multiplexing the 28 VT1.5 tributaries that make up an STS-1 signal [combination of VT1.5(cc-SPE) and/or VT1.5(DS1)] into one STS-1 signal and adding the STS-1 path overhead.
- VT1.5(DS1) — the SMUX circuit pack demultiplexes the N-rate signals into 28 VT1.5 tributaries. For tributaries that are cross-connected as VT1.5(DS1) tributaries, the SMUX adds the VT1.5 path overhead before multiplexing the 28 VT1.5 tributaries that make up an STS-1 signal [combination of VT1.5(cc-SPE) and/or VT1.5(DS1)] into one STS-1 signal and adding the STS-1 path overhead.

After generating the STS-1 signal, the SMUX circuit pack adds the STS-1 transport overhead, converts the STS-1 signal from unipolar to bipolar, and transmits the STS-1 signal downstream. For detailed information on all functions performed by the various interface modules and circuit packs, refer to Chapter 3.

## Cross-Connection Capability

Because cross-connections are done at the DS1, VT1.5, or STS-1 signal level, each DS3 signal is demultiplexed into 28 DS1 signals before being sent to the switch matrix. Each STS-1 signal can be sent to the switch matrix as one STS-1(cc-SPE) signal or as a combination of 28 demultiplexed VT1.5(cc-SPE) and/or DS1 [VT1.5(DS1)] signals.

The SONET interface of the DACS IV-2000 can deliver an STS-1 SPE to the switch matrix to make an STS-1(cc-SPE) cross-connect; deliver a VT1.5 tributary to the switch matrix to make a VT1.5(cc-SPE) cross-connect; and deliver a DS1 to the switch matrix to make a DS1 cross-connect.

The STS-1(cc-SPE) and VT1.5(cc-SPE) signals are cross-connected between STS1 Interface Modules only. A DS1 signal can be cross-connected between DS1, DS3, or STS1 Interface Modules. This allows for both SONET-to-SONET and SONET-to-asynchronous signal interworking, thus achieving gateway functionality.

## Grooming and Bridging

A DS1 signal arriving at a DS1 port, a DS3 port, or an STS-1 port can be cross-connected to any output ports. This capability permits both grooming (rearrangement of DS1 components of DS3 or STS-1 signals) and adding or dropping DS1 components of DS3 or STS-1 signals. On the other hand, if none of the DS1 signals within a DS3 or STS-1 signal requires modification before being cross-connected, you can cross-connect all the tributaries of the DS3 or STS-1 signal with a single command.

Similarly, VT1.5 signals arriving as tributaries of an STS-1 signal can be groomed, added, or dropped the same way.

Bridging is the cross-connection of one input port to two output ports. This capability allows for test access to DS1, VT1.5, or STS-1 signals, and the rerouting of signals (temporarily or permanently) with only brief interruptions of service. DS1, VT1.5, and STS-1 signals can all be bridged by a single command.

## Fully Protected

If a traffic-carrying circuit pack in the DACS IV-2000 fails, the main controller automatically switches to a protection standby circuit pack and reports the failure. The frame also monitors the performance of its other subassemblies and the facilities it cross-connects. When appropriate, it activates alarms, issues failure reports, and sends alarm indication signals downstream.

## Performance Monitoring

With Release 4.0, performance-monitoring functions are available at the SONET interface, including the STS-1 section, line, and path parameters, and the VT1.5 path parameters. For more information on performance monitoring, refer to the section titled "Performance Monitoring" in Chapter 2.

## Controller Architecture

The DACS IV-2000 control architecture (Figure 1-5) is a distributed multiprocessor design that supports concurrent execution and performs real-time operations. The architecture consists of the following two systems:

- Redundant Controller System
  - — Two Control Complexes (CPU/MTC/SSC circuit packs)
  - — Switch Communications Interface
  - — Unit Interface
  - — Enhanced Communications Interface (ECI)
  - — Synchronizer Module
- Unit Controller System
  - — Unit Controllers
  - — Interface Circuit Packs
  - — DS3 Performance Monitoring (DS3PM) over a Telemetry Asynchronous Block Serial (TABS) protocol interface (optional).

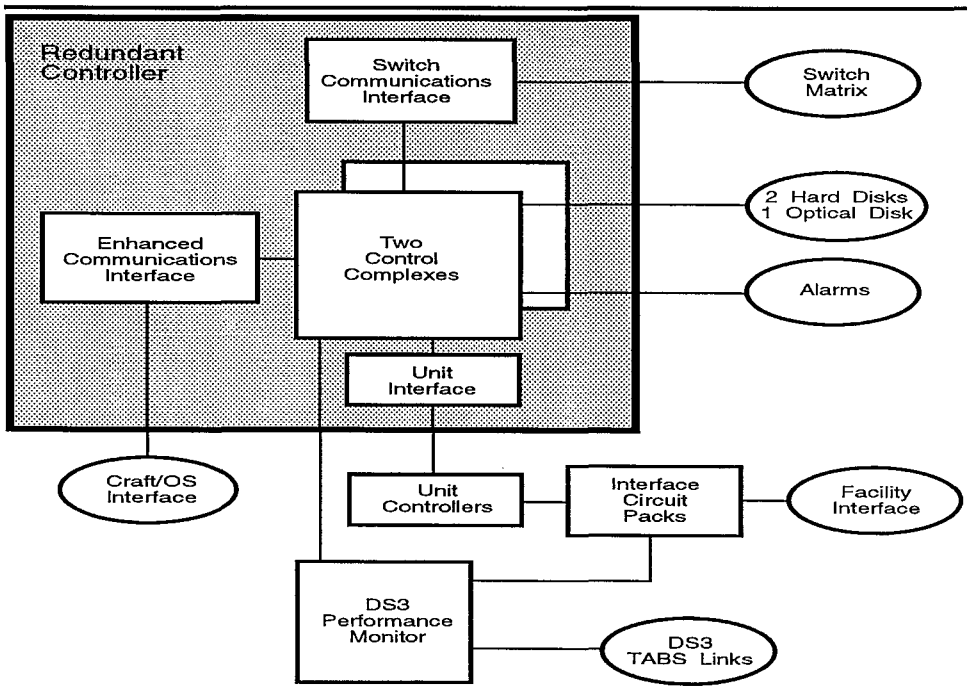



Figure 1-5. System Software Architecture

## Redundant Controller System

The central component of the redundant controller system are the two control complexes (CC). Each CC:

- Runs application software to perform all system administration functions including cross-connection, provisioning, test access, and synchronization for the SONET interfaces
- Serves as the central point of coordination for all system maintenance functions such as diagnostics, fault recovery, and alarms
- Performs all database management functions for the system, with the secondary storage controller providing the interface between the main processor and the nonvolatile storage devices (disk and optical drives).

The Enhanced Communications Interface (ECI) supports the user interface to the duplicated control complex. The ECI:

- Parses commands and generates messages to support the system interface languages: Transaction Language 1 (TL1), TABS and Telemetry Byte-Oriented Serial (TBOS).
- Provides the physical and electrical interfaces supporting synchronous (X.25) and asynchronous (Snider, telemetry) protocols.

The two ECI circuit packs can be configured to provide redundancy.

The DACS IV-2000 Release 4.0 contains a Synchronizer Module which accepts two external DS1 timing references. In the event of a timing reference failure, the synchronizer automatically switches to the secondary reference. If both references fail, the synchronizer operates in a stratum 3 holdover mode. The synchronizer is fully protected; if one synchronizer side fails, the system switches to the other side.

## Unit Controller System

The unit controllers (UCs) maintain the DACS IV-2000 redundant controller system facility interfaces. The UCs support the redundant controller by:

- Providing communications with the interface circuit packs
- Performing real-time maintenance functions, such as hardware fault detection.

Separate individual controllers on some of the enhanced interface circuit packs provide expanded real-time capabilities for features such as enhanced DS1, DS3, and SONET performance monitoring.

The optional DS3PM supports the TABS interface to the DS3 performance data.

**NOTE:**
The DS3PM is not required unless you are using TABS interface language.

## Hardware Architecture

The DACS IV-2000 hardware consists of an arrangement of two to nine equipment bays. Each equipment bay consists of modules, and each module consists of an equipment shelf and its associated circuit packs.

### Equipment Bays

The different types of bays are:

- Switch (SW) Bay — provides the control for the system, the fuses, the cross-connections, and the interbay cabling. This bay contains a fan assembly to provide cooling of the associated equipment.
- DS1 Interface (INTFC) Bay — provides the interface for up to 868 DS1 signals (equivalent to 31 DS3 signals). Air baffles are provided for equipment cooling.
- DS3 Interface (INTFC) Bay — provides the interface for up to 62 DS3 signals (equivalent to 1736 DS1 signals). Air baffles are provided for equipment cooling.
- STS1/DS3 Interface (INTFC) Bay — provides the interface for up to 60 DS3 or STS-1 signals (each DS3 is equivalent to 28 DS1 signals). This bay contains a fan assembly to provide equipment cooling.
- STS1/DS3/DS1 Interface (INTFC) Bay — provides the interface for:
  - — Up to 420 DS1 signals (equivalent to 15 DS3 signals) and
  - — Up to 46 DS3 signals (equivalent to 1288 DS1 signals) and no STS-1 signals, up to 31 DS3 signals (equivalent to 868 DS1 signals) and 15 STS-1 signals, or up to 30 STS-1 signals and no DS3 signals.

  Air baffles are provided for equipment cooling.

### Equipment Modules

The system bays contain modules made up of circuit packs to create the different functional segments of the DACS IV-2000. Figure 1-6 is a functional block diagram showing the main components of the DACS IV-2000.

The different types of modules and their main functions are:

- Redundant Controller (RC) Module — manages the user interface (administrative links), performs user specified functions, and coordinates database management, maintenance, and fault recovery operations. It also provides primary and secondary program and database backup capabilities and the means to load new software releases.

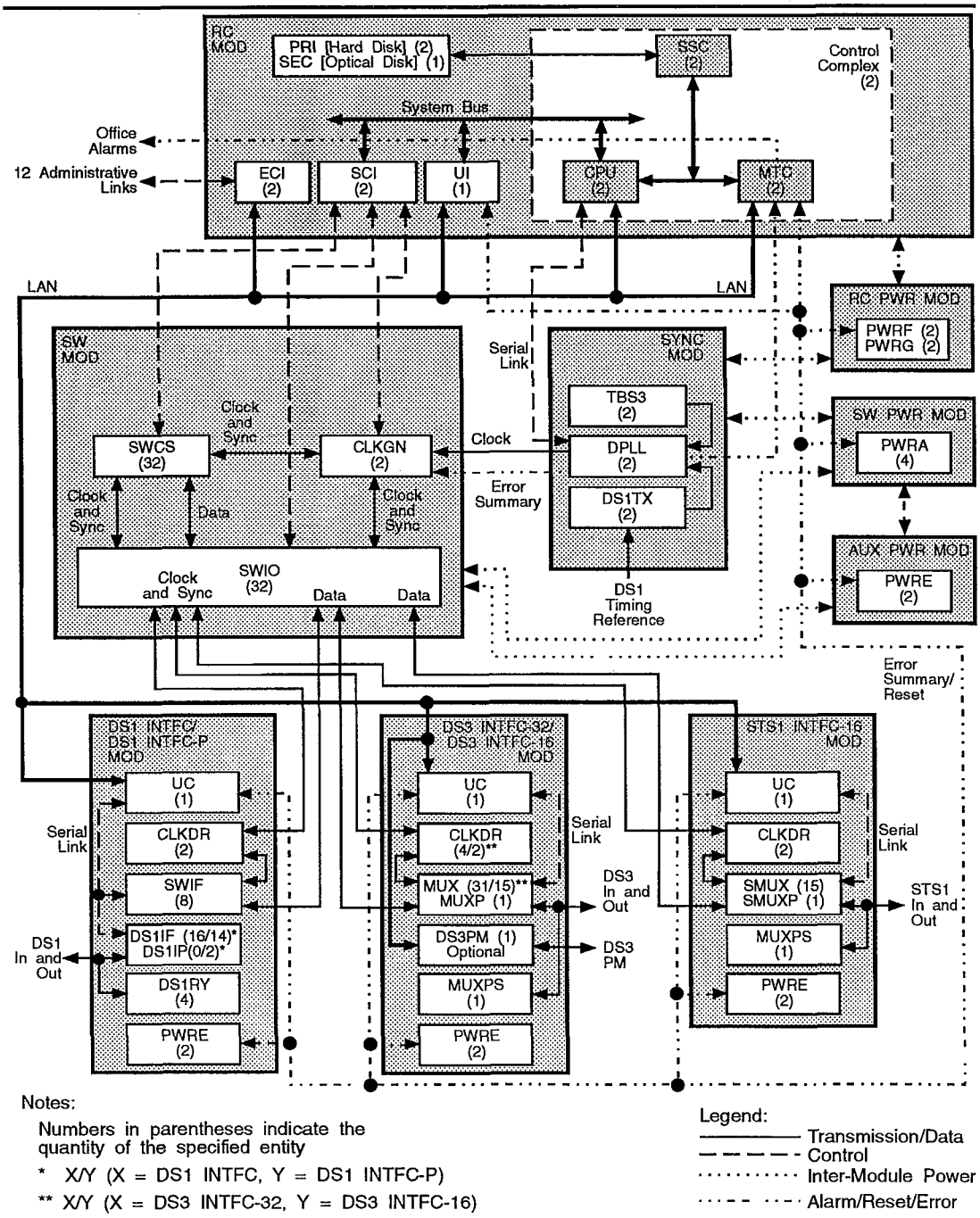



Figure 1-6. **DACS-IV 2000 (256) Release 4.0 Functional Block Diagram**

- Redundant Controller Power (RC PWR) Module — provides the +5 Vdc, +12 Vdc, and -12 Vdc power and fuse protection for the RC Module. This module also provides the -48 Vdc power to the SYNC Module.
- Synchronizer (SYNC) Module — generates the timing information for the DACS IV-2000.
- Switch (SW) Module — performs the DS1, STS-1, and VT1.5 cross-connection functions.
- Switch Power (SW PWR) Module — provides the +5 Vdc and fuse protection for the Switch Module and the fuse protection for the -5 Vdc power supplied by the AUX PWR Module. This module also provides the +5 Vdc power and -5 Vdc fuse protection for the SYNC Module.
- Auxiliary Power (AUX PWR) Module — provides the -5 Vdc power for the SW Module and the SYNC Module.
- DS1 Interface (INTFC) Module — provides up to 224 DS1interfaces for the incoming and outgoing facilities. This module accepts DS1 signals (in a format that is compatible with a DSX-1) and switches these signals to and from the Switch Input/Output Module. Protection for the interfaces of this module is provided by the DS1 Interface-Protection Module contained in the same DS1 Interface Bay.
- DS1 Interface-Protection (INTFC-P) Module — provides up to 196 DS1interfaces for the incoming and outgoing facilities. This module accepts DS1 signals (in a format that is compatible with a DSX-1) and switches these signals to and from the Switch Input/Output Module. This module provides protection for itself in addition to the other DS1 Interface Modules (up to three) within the same DS1 Interface Bay.
- DS3 Interface-16 (INTFC-16) Module — provides up to 15 DS3 interfaces with protection for incoming and outgoing DS3 facilities. These modules accept DS3 signals in a format compatible with a DSX-3 and switch the signals to and from the Switch Input/Output Module.
- DS3 Interface-32 (INTFC-32) Module — provides up to 31 DS3 interfaces with protection for incoming and outgoing DS3 facilities. These modules accept DS3 signals in a format compatible with a DSX-3 and switch the signals to and from the Switch Input/Output Module.
- STS1 Interface-16 (INTFC-16) Module — provides up to 15 interfaces with protection for incoming and outgoing STS-1 facilities. These modules accept STS-1 signals in a format compliant with the SONET specifications and switch the signals to and from the SWIO Module.

Each module in the system is equipped with circuit packs. These circuit packs are required to perform the functions of the system. The Redundant Controller, RC Power Module, Auxiliary Power, and Switch Power Modules, all located in the Switch Bay, are always fully equipped with the required circuit packs. The Switch Modules located in the Switch Bay and the DS1, DS3, and STS1 Interface Modules located in the interface bays are equipped with circuit packs as required, depending on service requirements. The Synchronizer Module in the Switch Bay must be fully equipped when used in systems supporting SONET interfaces.

Circuit packs are identified by functional name and circuit pack code. A suffix number after a circuit pack functional name indicates a series version. When there is no suffix number, a 1 is assumed. Higher series versions can be substituted in slots labeled for a lower series version but not the reverse. For example, a PWRE3 circuit pack can be substituted in a slot labeled PWRE, but a PWRE1 circuit pack cannot be substituted in a slot labeled PWRE2 or other higher series version.

# System Features

# 2

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# System Features

# 2

This chapter describes the capabilities of the DACS IV-2000 (256) Release 4.0. The new features are described first, followed by the existing features.

## New Features

The DACS IV-2000 (256) Release 4.0 offers the following new features:

- Enhanced Secondary Storage Subsystem
- Enhanced Synchronizer Module
- LED for Manual Protection Switch
- Duplex Power Feed (new frame orders; existing frames use standard power feed).

## Enhanced Secondary Storage Subsystem

The enhanced Secondary Storage Subsystem (SSS) consists of a Secondary Storage Controller (SSC), one per Control Complex (CC); two Primary Storage devices (PRI-1 and PRI-2); and a Secondary Storage device (SEC). For Release 4.0, the SSS incorporates a new architecture, which upgrades the existing SSS to the industry-standard Small Computer System Interface (SCSI) and improves the overall system performance of the SSS.

Functionally, the enhanced SSS is responsible for database backup and storage. With this release, the SSS includes two new hard disks and a removable optical disk to:

- Upgrade the volatile RAM memory to store relevant system information (such as switch settings and cross-connect map)
- Increase the primary nonvolatile memory (PRI-1 and PRI-2) to 248 Mbytes
- Enhance the SEC by replacing the tape drive with an optical disk drive, which:
  - — increases storage capacity to 128 Mbytes
  - — increases data access speed
  - — stores system database and the program control out of the equipment or off-site for backup purposes.

With the addition of the optical disk, you are positioned for growth; that is, you will be able to advance to Release 5.0 and beyond.

The enhanced SSS:

- Improves controller reliability
- Provides faster access and data transfer times
- Increases database capacity for future feature enhancements
- Improves input/output availability.

The increased input/output availability permits acceptance, processing, and execution of incoming commands even during manual or autonomous backups between the primary and secondary nonvolatile memory devices. Cross-connect commands can be executed during backups from working memory to the PRI disk drives.

The DACS IV-2000 Release 4.0 uses the industry-standard SCSI for both the primary and secondary nonvolatile memory storage devices.

The enhanced Secondary Storage Controller circuit packs (SSC5, PRI5, and SEC5) are fully compatible with the Redundant Controller shelf; that is, no hardware or wiring changes are required to accommodate these circuit packs. However, a new PWRF circuit pack (427AB) is needed to support the new SSS as well as new fuses. The Duplex power option requires a new PWRA circuit pack (566A). The SSC5, PRI5, and SEC5 circuit packs are pin-compatible with the SSC2, PRI2, and SEC2 circuit packs. They occupy the same physical space, size, and location as the SSS of Release 3.0.

## Enhanced Synchronizer Module

DACS IV-2000 synchronization (first introduced in Release 3.0) allows the DACS IV-2000 to act as a gateway between synchronous and asynchronous networks. The DACS IV-2000 Release 4.0 provides enhancements to the Synchronizer Module for improved compliance with Bellcore TR-NWT-001244 and TR-NWT-000253.

In addition to its previous capabilities, the Synchronizer Module now:

- Has LEDs on its circuit packs (version 2 only) to indicate an active or alarm state (see "Circuit Pack Alarms" later in this chapter)
- Supports field-upgradable firmware to minimize future hardware changes
- Offers improved lock-time performance
- Locks to an external reference when modulated with input jitter per TR-NWT-001244
- Generates major alarm on loss of all timing reference.

The synchronizer module should contain the same vintage (version one or version two) circuit packs on both side. However, to facilitate a smooth transition to version two, the software supports both version one circuit packs (DPLL1, DS1TX1, TBS31) and version two circuit packs (DPLL2, DS1TX2, TBS32). In normal operation, all circuit packs in the Synchronizer Module must be of the same version; otherwise, the synchronizer circuit packs cannot be restored via the `RST-EQPT` command. If circuit packs of the same version are on both synchronizer (SYNC) sides and the circuit packs are not in a failed state, no synchronizer hardware-related alarms appear on the system.

The DACS IV-2000 Release 4.0 provides error-free SONET transmission with version one circuit packs (DPLL1, DS1TX1, TBS31) on one SYNC side and version two circuit packs (DPLL2, DS1TX2, TBS32) on the other SYNC side, regardless of which SYNC side is active.

The intensity, arrangement, label position, and spacing for the LEDs comply with the requirements of Bellcore TR-TSY-000824.

## LED for Manual Protection Switch

To aid in identifying a circuit pack that has been manually switched to protection, this feature lights the red ALM LED on the interface or switch circuit packs (SWIF, MUX, SMUX, SWIO, or SWCS) when the circuit pack has been manually switched to protection. This is a provisionable feature.

When a manual protection switch has been performed, the red ALM LED on the circuit pack that was switched to protection is constantly lit for the duration of the protection switch. The output response to the command that was used to manually switch the circuit pack to protection contains a warning message that the red ALM LED on the protected circuit pack is lit as a result of this operation.

## Duplex Power Feed

Previous releases of the DACS IV-2000 (256) were powered by a single power plant through a Battery Distribution Feeder Board (BDFB). While existing DACS IV-2000 (256) frames upgraded to Release 4.0 are powered in this manner, the new duplex power feed capability, provided with new frame orders, ensures optimum reliability.

With the duplex power capability, the system receives power from one or two -48V diverse power plants at two BDFBs. (A diverse power plant is one that does not share common components, such as BDFBs, rectifiers, batteries, and cable racks.) All -48V power feeds from the BDFBs are fused separately at the fuse and alarm panel and connected to one of two independent central office battery plants in such a way that loss of one BDFB does not affect traffic or result in any loss of service.

For more information, see "Power Specifications" in Appendix A.

## Feature Description

The DACS IV-2000 (256) Release 4.0 supports the following features, which were introduced in previous releases:

- SONET Networking
- Upgrade
- Cross-Connections
- Special Service (Redlined) Connections
- DS1/STS-1/VT1.5 Facility Roll
- Loopbacks
- Test Access
- Link Association
- Performance Monitoring
- Redundant Controller
- Nonvolatile Backup Memory
- Alarm Reporting
- Deny Manual Unit Controller Removal
- Supported Operations Systems
- User and OS Interfaces
- Input Command Routing
- Facility Maintenance
- Facility Failure Detection
- Frame Maintenance
- Protection Switching Operations
- Automatic Restoration of Circuit Packs.

## SONET Networking

The DACS IV-2000 provides SONET networking, which is the ability to perform all of the functionality associated with SONET interconnection. The SMUX circuit pack terminates an EC-1 facility and allows for cross-connection of the entire STS-1 SPE, demultiplexing of VT1.5-based STS-1s and cross-connection of VT1.5s to other SONET interfaces, or cross-connection of DS1s. This same circuit pack also provides in-line performance monitoring of the SONET signal, including VT1.5 tributaries of the STS-1. Additional circuit packs are not required, and no deloading of switch capacity is required in order to accommodate the SONET performance-monitoring feature. The DACS IV-2000 also supports operational, maintenance, and administrative features necessary for full SONET networking capability.

### SONET Interface

The DACS IV-2000 is fully compliant with SONET STS-1 industry standards, allowing interconnections with AT&T's transmission equipment (DDM-2000 and FT-2000) and any other vendor equipment that meets these standards. The DACS IV-2000 provides for EC-1 SONET termination on STS1 interfaces. STS1 interfaces are housed in STS1/DS3 Interface-16 modules located in the STS1/DS3/DS1 bay or the STS1/DS3 bay. The STS1/DS3 bay can house up to four STS1/DS3 Interface-16 modules. The STS1/DS3/DS1 Interface Bay contains one DS1 Interface module, one DS1 Interface-Protection module, one DS3 Interface-32 module, and one STS1/DS3 Interface-16 module. (The DS3 Interface-32 module in the STS1/DS3/DS1 Bay can be replaced by an STS1 Interface-16 module; however, this results in a reduction of total system capacity, because 16 slots in the module must be left unequipped.)

The STS1/DS3 Interface-16 module can be equipped with either SMUX and SMUXP circuit packs to support STS-1 signals or MUX2 and MUX2P circuit packs to support DS3 signals. An STS1/DS3 Interface-16 module is dedicated to either STS1 or DS3 interfaces; this module does not support a mixture of STS1 and DS3 interfaces.

The capacity of the STS1/DS3 Interface-16 module is designed to support fifteen service circuit packs and one protection circuit pack. Each SMUX circuit pack terminates one EC-1 line and supports all of the SONET capabilities described in this chapter.

## Upgrade

You can upgrade from a DACS IV-2000 (256) Release 3.0 to a DACS IV-2000 Release 4.0. (You cannot move directly from a release prior to 3.0 to Release 4.0; you must first step to Release 3.0. The upgrade includes the in-service replacement of the Main Controller Module with the Redundant Controller Module equipped with the enhanced SSS.)

Any configuration of the Release 3.0 system can be upgraded to Release 4.0. The only hardware change required for the upgrade is replacement of the existing SSC, PRI, and SEC circuit packs with the corresponding circuit packs of the enhanced SSS. If SONET interfaces are used for Release 4.0, the Clock Generator and Synchronizer Module circuit packs must be upgraded.

The upgrade procedure includes conversion of the Release 3.0 database to the optical disk media used in Release 4.0.

## Cross-Connections

The DACS IV-2000 electronically cross-connects DS1, STS-1, and VT1.5 signals. The cross-connections are implemented with a three-stage space division switch. The DACS IV-2000 switch network is nonblocking and can perform the following types of cross-connections:

- STS-1(cc-SPE) signals between SONET interfaces (SMUX circuit packs). By cross-connecting STS-1(cc-SPE) signals, SONET end-to-end path connectivity is maintained through the DACS IV-2000.
- VT1.5 signals between SONET interfaces. VT1.5 end-to-end path connectivity is maintained through the DACS IV-2000 with this type of cross-connection.
- DS1 signals between SONET interfaces. DS1 signals are accessed by terminating the path of the VT1.5 signals and extracting the DS1 signal.
- DS1 gateway cross-connection between SONET and DS1/DS3 interfaces. These types of cross-connections provide the SONET/asynchronous gateway connection.
- DS1 signals between DS1/DS3 interfaces.

The DACS IV-2000 can perform one-way, two-way, bridged, and roll cross-connections. These functions can be performed on DS1, VT1.5, and STS-1 signals. The DACS IV-2000 implements cross-connections from commands received over one of the administrative links from either a local terminal or from a centralized operations center. In addition to implementing cross-connections, commands are provided for map retrieval. These commands are used to retrieve more data about input ports that are mapped to output ports. In addition, data can be retrieved about DS1 ports that are transmitting quasi-random signals.

## DS1 Cross-Connections

The DACS IV-2000 switch network can cross-connect up to 6,944 DS1 (240 equivalent DS3) one-way signals from terminating DS3, DS1, and STS-1 facilities and/or network elements.

The DACS IV-2000 can cross-connect a DS1 signal on any incoming port to any outgoing port. This allows DS1 grooming (the rearrangement of DS1 signals in DS3 signals and/or STS-1 signals) on the DS3 or STS-1 facilities without the need for back-to-back multiplexers. This feature also allows adding or dropping DS1 signals from outgoing or incoming DS3 or STS-1 facilities as well as DS1-to-DS1 cross-connections. Figure 2-1 shows these capabilities (for simplicity, only one-way cross-connections are shown).

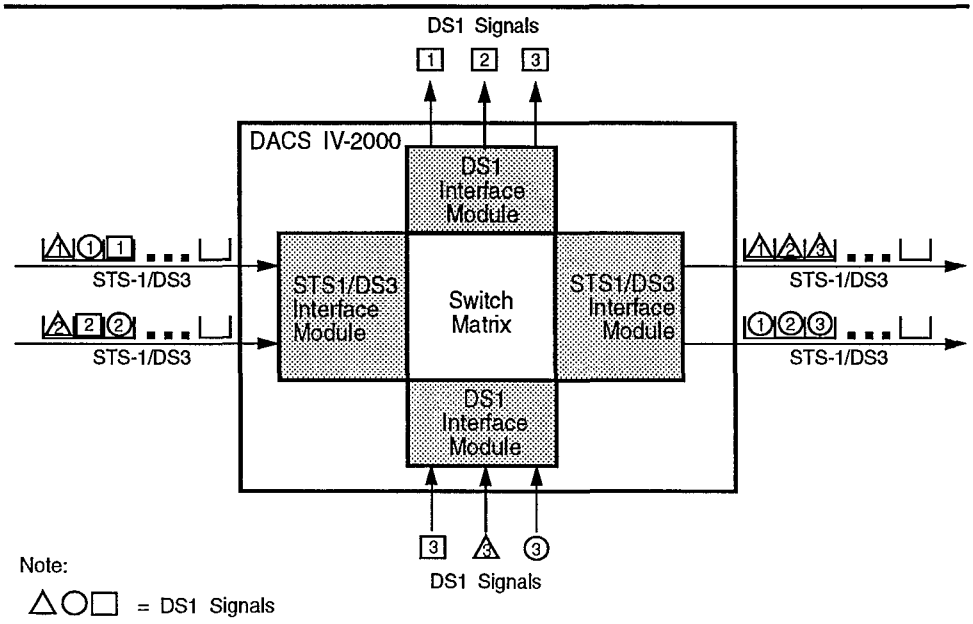
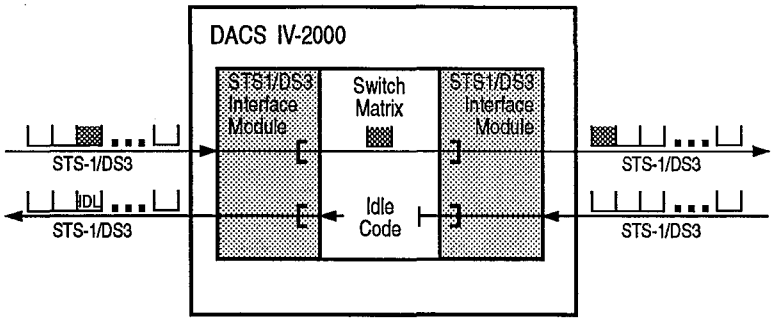



Figure 2-1. DS1 Cross-Connects (One-Way)

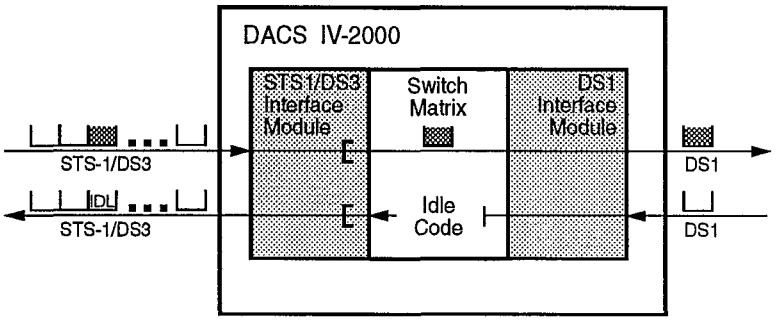
Three types of DS1 cross-connections are possible with the DACS IV-2000: One-Way, Two-Point DS1 cross-connect; Two-Way, Two-Point DS1 cross-connect; and Bridged DS1 cross-connect.

- One-Way, Two-Point DS1 Cross-Connection — Figure 2-2 shows the DACS IV-2000 can cross-connect one direction only of a two-point DS1 cross-connection. The corresponding DS1 in the other direction can be independently cross-connected or terminated with no cross-connection, in which case a DS1 idle code or other external generator signal pattern is transmitted on the unused DS1 facility. The DS1 idle code consists of unframed all ones.



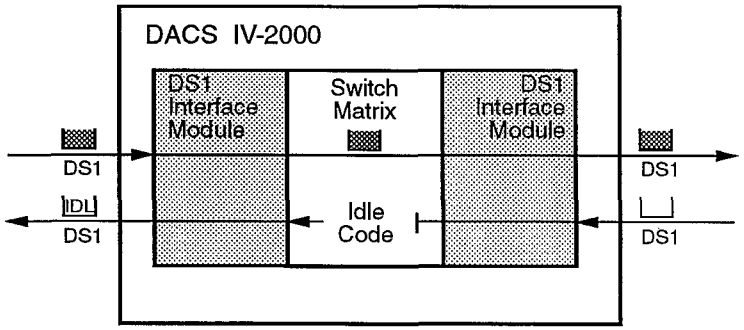

Notes:
IDL = DS1 Idle Code
⊣ = Termination
[ = MUX/DEMUX

**A. STS-1/DS3 to STS-1/DS3**




Notes:
IDL = DS1 Idle Code
⊣ = Termination
[ = MUX/DEMUX

**B. STS-1/DS3 to DS1**

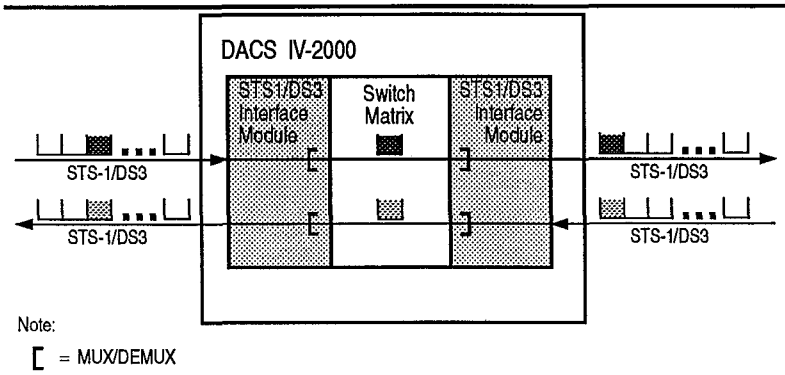



Notes.
IDL = DS1 Idle Code
⊣ = Termination

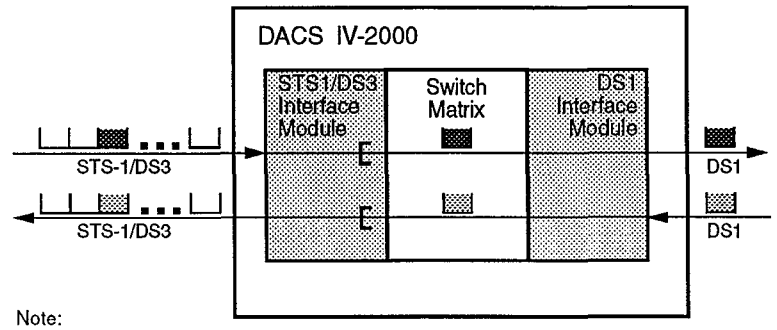
**C. DS1 to DS1**

Figure 2-2. **One-Way, Two-Point DS1 Cross-Connection**

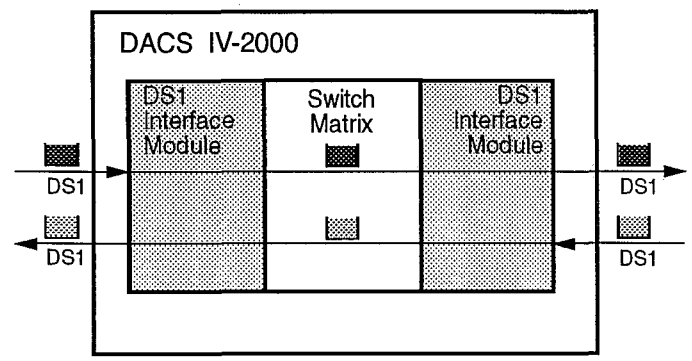
- Two-Way, Two-Point DS1 Cross-Connection — Figure 2-3 shows examples of a two-way, two-point DS1 cross-connection. With a single command, the DACS IV-2000 can cross-connect both directions of a DS1 signal on any incoming DS1, DS3, or STS-1 port to any outgoing DS1, DS3, or STS-1 port.




A. STS-1/DS3 to STS-1/DS3



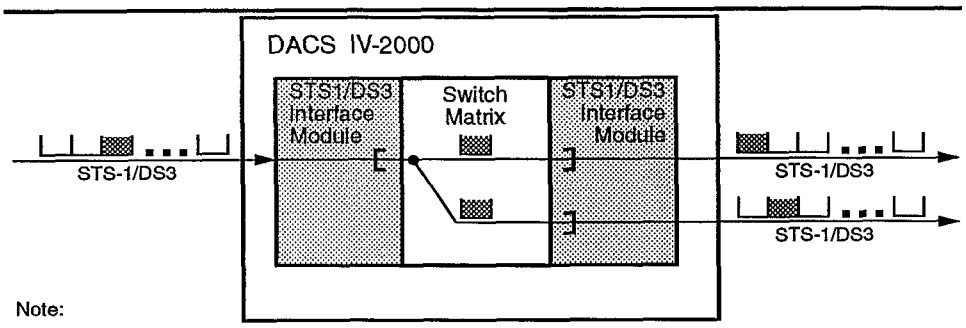

B. STS-1/DS3 to DS1



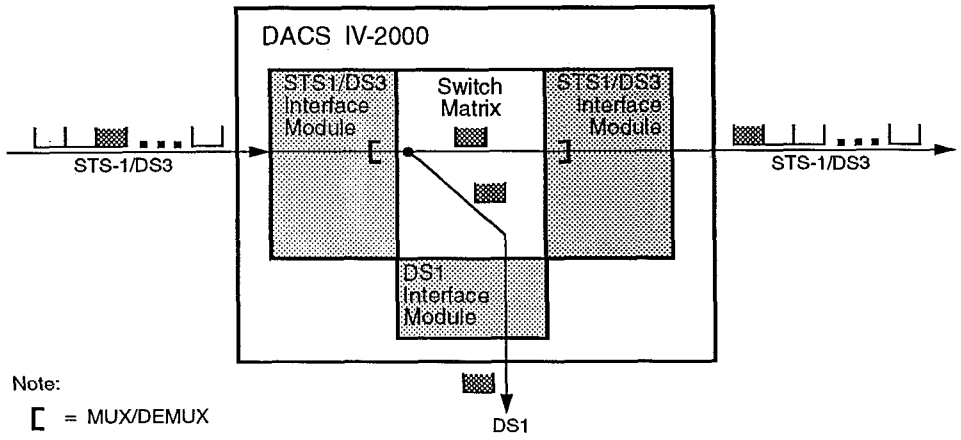

C. DS1 to DS1

Figure 2-3. Two-Way, Two-Point DS1 Cross-Connection

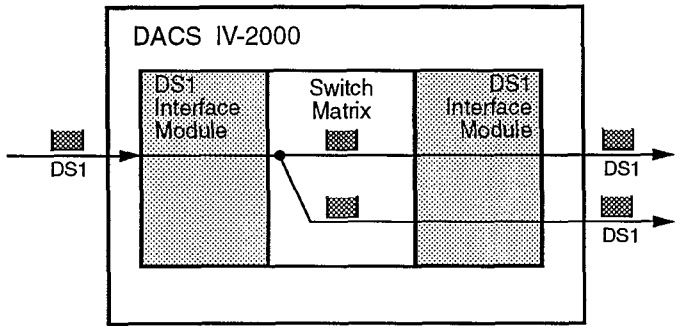
- Bridged DS1 Cross-Connection — Figure 2-4 shows examples of the DACS IV-2000 bridging existing DS1 connections by cross-connecting the DS1, DS3, or STS-1 input port of the existing connection to a second DS1, DS3, or STS-1 output port without affecting service in the existing path. This feature is used for DS1 facility rolling.




A. STS-1/DS3 to STS-1/DS3




B. STS-1/DS3 to DS1



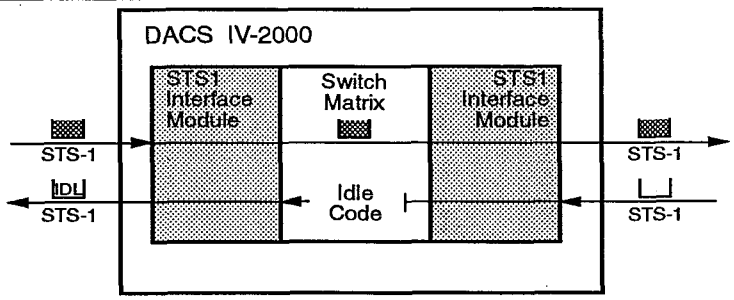

C. DS1 to DS1

Figure 2-4. Bridged DS1 Cross-Connections

## STS-1 Cross-Connections

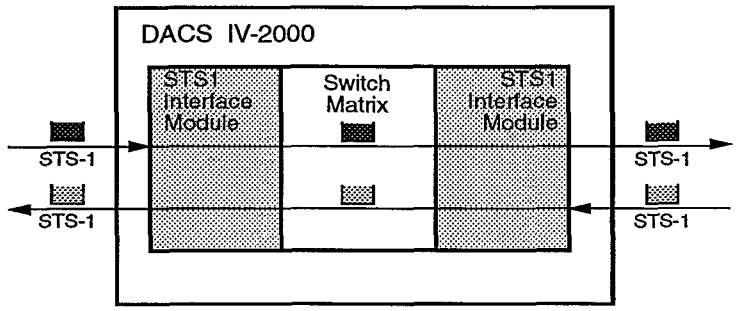
The DACS IV-2000 switch network can cross-connect up to 240 STS-1 signals from terminating EC-1 facilities and/or network elements. The DACS IV-2000 can cross-connect an STS-1 signal on any incoming STS1 port to any outgoing STS1 port. Three types of STS-1 cross-connections are possible with the DACS IV-2000:

- Two-Point STS-1 Cross-Connection, One-way — Figure 2-5A shows a one-way STS-1 cross-connect of a two-point cross-connection. The corresponding STS-1 signal in the other direction can be independently cross-connected or terminated with no cross-connection, in which case an STS-1 path Alarm Indication Signal (AIS) is transmitted on the unused EC-1 facility.
- Two-Point STS-1 Cross-Connection, Two-way — Figure 2-5B shows a two-way STS-1 cross-connection of a two-point cross-connection. A single command can cross-connect both directions of an STS-1 signal on any incoming STS1 port to any outgoing STS1 port.
- Bridged STS-1 Cross-Connection — Figure 2-5C illustrates how the DACS IV-2000 can bridge any existing STS-1 connection by cross-connecting the STS1 input port of the existing connection to a second STS1 output port without affecting service in the existing path. This feature allows for EC-1 facility rolling.

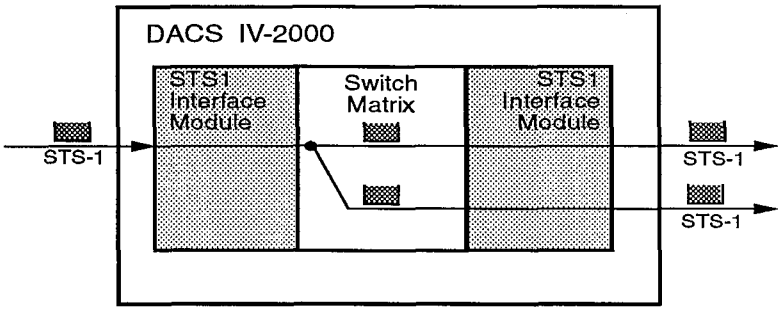



Notes:
IDL = STS-1 Path AIS
⊣ = Termination

**A. Two-Point, One-Way**




**B. Two-Point, Two-Way**



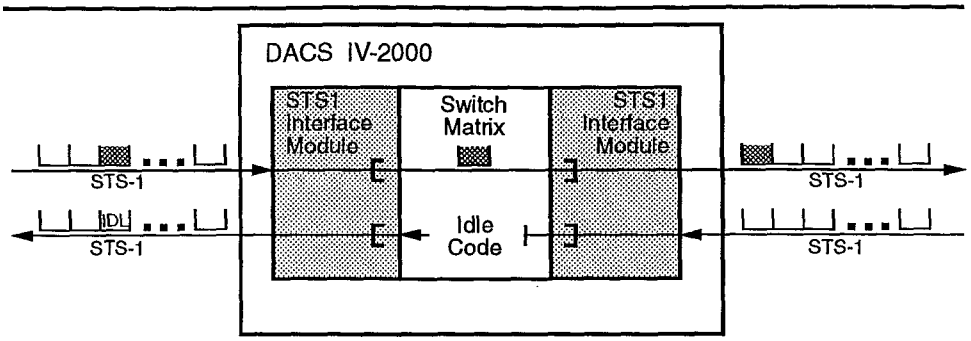

**C. Bridged Cross-Connection**

Figure 2-5. **STS-1 Cross Connections**

## VT1.5 Cross-Connections

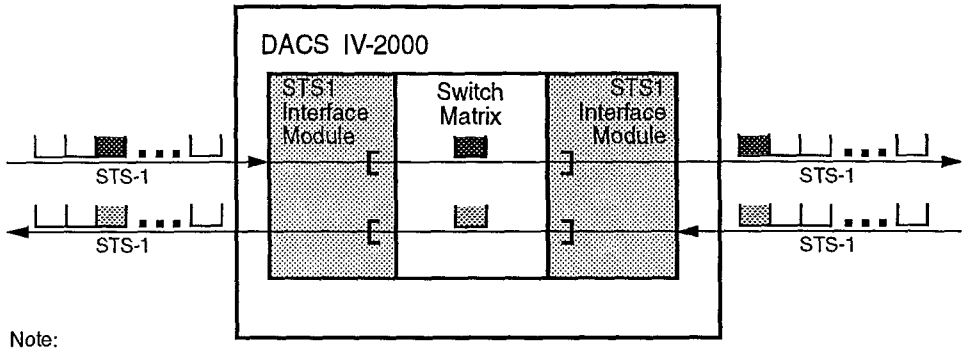
The DACS IV-2000 switch network can cross-connect up to 6720 VT1.5 one-way signals (240 equivalent STS-1signals) from terminating EC-1 facilities and/or network elements. The DACS IV-2000 can cross-connect a VT1.5 signal on any incoming STS1 port to any outgoing STS1 port. Three types of VT1.5 cross-connections are possible:

- Two-Point VT1.5 Cross-Connection, One-way — Figure 2-6A shows a one-way VT1.5 cross-connect of a two-point cross-connection. The corresponding VT1.5 signal in the other direction can be independently cross-connected or terminated with no cross-connection, in which case a VT path AIS is transmitted on the unused VT1.5 facility.
- Two-Point VT1.5 Cross-Connection, Two-way — Figure 2-6B shows a two-way VT1.5 cross-connection of a two-point cross-connection. A single command can cross-connect both directions of an VT1.5 signal on any incoming STS1 port to any outgoing STS1 port
- Bridged VT1.5 Cross-Connection — Figure 2-6C shows how the DACS IV-2000 can bridge any existing VT1.5 connection by cross-connecting the VT1.5 input port of the existing connection to a second VT1.5 output port without affecting service in the existing path. This feature allows for VT1.5 facility rolling.



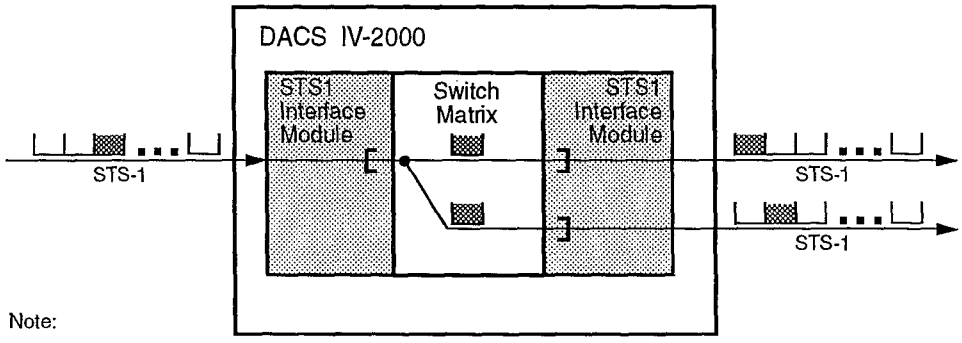

Notes:
IDL = VT Path AIS
⊣ = Termination
[ = MUX/DEMUX

**A. Two-Point, One-Way**




Note:
[ = MUX/DEMUX

**B. Two-Point, Two-Way**




Note:
[ = MUX/DEMUX

**C. Bridged Cross-Connection**

Figure 2-6. VT1.5 Cross-Connection

## DS1 and VT1.5 Mappings

The industry uses two methods to number DS1 signals within DS3 signals and VT1.5 signals within STS-1 signals. One method is to number the DS1/VT1.5 signals sequentially (1 through 28); and the other is to use the combination of the DS2/VT group and the DS1/VT1.5 port. Table 2-1 (DS1 signals) and Table 2-2 (VT1.5 signals) show the two numbering methods and their relationship with each other. The first column of each table shows the sequential numbering method, and the last two columns show the group/port numbering method. In the two tables, notice that DS1s within DS3s and VT1.5s within STS-1s are mapped to different DS2/VT groups and DS1/VT1.5 ports. In Table 2-1, DS2 group 1 is associated with DS1 signals 1 through 4, while in Table 2-2, VT group 1 is associated with VT1.5 signals numbered 1, 8, 15, and 22.

Network elements can use either numbering method. The DACS IV-2000 uses the 1 through 28 sequential numbering method. Add-drop multiplexers (ADMs), which generally associated a single low-speed circuit pack with four ports with a DS2/VT group, use the DS2/VT group and DS1/VT1.5 port numbering method.

When cross-connecting asynchronous and synchronous information from other network elements (such as the DDM-1000 or DDM-2000) that use the DS2/VT group and DS1/VT1.5 port numbering method, within the DACS IV-2000, the signal numbering methods for all network elements must be taken into consideration when setting up the `ENT-CRS-T1` command.

The following examples show how the numbering of signals is maintained for three different types of cross-connections through the DACS IV-2000:

- Example 1 shows an *asynchronous-to-asynchronous* (asynchronous) environment where the DACS IV-2000 receives a DS3 signal from one DDM-1000, cross-connects a DS1 signal within that DS3 to a DS1 signal within another DS3, and transmits the new DS3 signal to a second DDM-1000.
- Example 2 shows an *asynchronous-to-synchronous* (asynchronous gateway) environment where the DACS IV-2000 receives a DS3 signal from a DDM-1000, cross-connects a DS1 signal within that DS3 to a VT1.5(DS1) signal within an STS-1, and transmits that STS-1 signal to a DDM-2000.
- Example 3 shows a *synchronous-to-synchronous* (SONET) environment where the DACS IV-2000 receives an STS-1 signal from one DDM-2000, cross-connects a VT1.5(DS1) signal within that STS-1 to a VT1.5(DS1) signal within another STS-1, and transmits the new STS-1 signal to a second DDM-2000.

In the examples, the DSX-1 panels are used to show how the numbering of DS1 and VT1.5 signals corresponds when looking at both ends of the signal path. The same locations at the DSX-1 panels are used for each example. Note that the `ENT-CRS-T1` command differs depending on the cross-connection type used (asynchronous, asynchronous gateway, or SONET).

Table 2-3 summarizes the DS1 and VT1.5 mappings used in the examples.

Table 2-1. DS1 Signal Numbering Within DS3 Signals

| DS1s Within DS3 | DS2 Group | DS1 Port Within DS2 Group | DS1s Within DS3 | DS2 Group | DS1 Port Within DS2 Group |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 17 | 5 | 1 |
| 2 | | 2 | 18 | | 2 |
| 3 | | 3 | 19 | | 3 |
| 4 | | 4 | 20 | | 4 |
| 5 | 2 | 1 | 21 | 6 | 1 |
| 6 | | 2 | 22 | | 2 |
| 7 | | 3 | 23 | | 3 |
| 8 | | 4 | 24 | | 4 |
| 9 | 3 | 1 | 25 | 7 | 1 |
| 10 | | 2 | 26 | | 2 |
| 11 | | 3 | 27 | | 3 |
| 12 | | 4 | 28 | | 4 |
| 13 | 4 | 1 | | | |
| 14 | | 2 | | | |
| 15 | | 3 | | | |
| 16 | | 4 | | | |

Table 2-2. VT1.5 Signal Numbering Within STS-1 Signals

| VT1.5 Within STS-1 | VT Group | VT1.5 Port Within VT Group | VT1.5 Within STS-1 | VT Group | VT1.5 Port Within VT Group |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 15 | 1 | 3 |
| 2 | 2 | 1 | 16 | 2 | 3 |
| 3 | 3 | 1 | 17 | 3 | 3 |
| 4 | 4 | 1 | 18 | 4 | 3 |
| 5 | 5 | 1 | 19 | 5 | 3 |
| 6 | 6 | 1 | 20 | 6 | 3 |
| 7 | 7 | 1 | 21 | 7 | 3 |
| 8 | 1 | 2 | 22 | 1 | 4 |
| 9 | 2 | 2 | 23 | 2 | 4 |
| 10 | 3 | 2 | 24 | 3 | 4 |
| 11 | 4 | 2 | 25 | 4 | 4 |
| 12 | 5 | 2 | 26 | 5 | 4 |
| 13 | 6 | 2 | 27 | 6 | 4 |
| 14 | 7 | 2 | 28 | 7 | 4 |

Table 2-3. **Summary of DS1 and VT1.5 Mappings Between DACS IV-2000 and DDM-1000/2000**

| Asynchronous DACS IV-2000 to DDM-1000 | | Synchronous | | | |
|---|---|---|---|---|---|
| | | DACS IV-2000 | | DDM-2000 | |
| DS1s Within DS3 | DS2,DS1 | VT1.5s Within STS-1 | VT Group, VT | VT Group, VT | VT1.5s Within STS-1 |
| 1 | 1,1 | 1 | 1,1 | 1,1 | 1 |
| 2 | 1,2 | 2 | 2,1 | 1,2 | 8 |
| 3 | 1,3 | 3 | 3,1 | 1,3 | 15 |
| 4 | 1,4 | 4 | 4,1 | 1,4 | 22 |
| 5 | 2,1 | 5 | 5,1 | 2,1 | 2 |
| 6 | 2,2 | 6 | 6,1 | 2,2 | 9 |
| 7 | 2,3 | 7 | 7,1 | 2,3 | 16 |
| 8 | 2,4 | 8 | 1,2 | 2,4 | 23 |
| 9 | 3,1 | 9 | 2,2 | 3,1 | 3 |
| 10 | 3,2 | 10 | 3,2 | 3,2 | 10 |
| 11 | 3,3 | 11 | 4,2 | 3,3 | 17 |
| 12 | 3,4 | 12 | 5,2 | 3,4 | 24 |
| 13 | 4,1 | 13 | 6,2 | 4,1 | 4 |
| 14 | 4,2 | 14 | 7,2 | 4,2 | 11 |
| 15 | 4,3 | 15 | 1,3 | 4,3 | 18 |
| 16 | 4,4 | 16 | 2,3 | 4,4 | 25 |
| 17 | 5,1 | 17 | 3,3 | 5,1 | 5 |
| 18 | 5,2 | 18 | 4,3 | 5,2 | 12 |
| 19 | 5,3 | 19 | 5,3 | 5,3 | 19 |
| 20 | 5,4 | 20 | 6,3 | 5,4 | 26 |
| 21 | 6,1 | 21 | 7,3 | 6,1 | 6 |
| 22 | 6,2 | 22 | 1,4 | 6,2 | 13 |
| 23 | 6,3 | 23 | 2,4 | 6,3 | 20 |
| 24 | 6,4 | 24 | 3,4 | 6,4 | 27 |
| 25 | 7,1 | 25 | 4,4 | 7,1 | 7 |
| 26 | 7,2 | 26 | 5,4 | 7,2 | 14 |
| 27 | 7,3 | 27 | 6,4 | 7,3 | 21 |
| 28 | 7,4 | 28 | 7,4 | 7,4 | 28 |

### EXAMPLE 1: Asynchronous-to-Asynchronous Mapping

An example of asynchronous-to-asynchronous mapping is shown in Figure 2-7, where a DACS IV-2000 is used to cross-connect a DS1 signal within a DS3 signal between two DDM-1000 ADMs that accept DS1 signals from a DSX-1 panel.

- The DS1 signal labeled 7 (or DS1 port 3 of DS2 group 2 on the DSX-1 on the FROM side) is transmitted to the DS1 signal labeled 26 (or DS1 port 2 of DS2 group 7 on the DSX-1) on the TO side.
- The DDM-1000 on the FROM side accepts the DS1 signal on slot 2, port 3 (the mapping is the same as the DS2 group, DS1 port numbering). Using Table 2-3 column 2 for the value 2, 3 of DS2,DS1, the DS1 port from the DSX-1 maps into DS1 7 within the DS3 that is sent to the DACS IV-2000. The DACS IV-2000 cross-connects DS1 7 of the DS3 entering at MUX-17-1 to DS1 26 of the DS1 exiting at MUX-21-1 with the `ENT-CRS-T1::17-1-7:21-1-26;` command.
- The DS3 signal is sent to the DDM-1000 on the TO side, where DS1 26 is mapped to slot 7, port 2. Using column 1 of Table 2-3, the value 26 maps to the value 7,2 in column 2.
- Finally, the DS1 signal is accessed at the DSX-1 on the TO side as DS1 26 (or DS1 port 2 of DS2 group 7).

In this example, the DACS IV-2000 cross-connected the two asynchronous DS1 signals from the DSX-1 panels on a one-for-one basis; that is, DS1 7 on the FROM side is cross-connected to DS1 26 on the TO side.

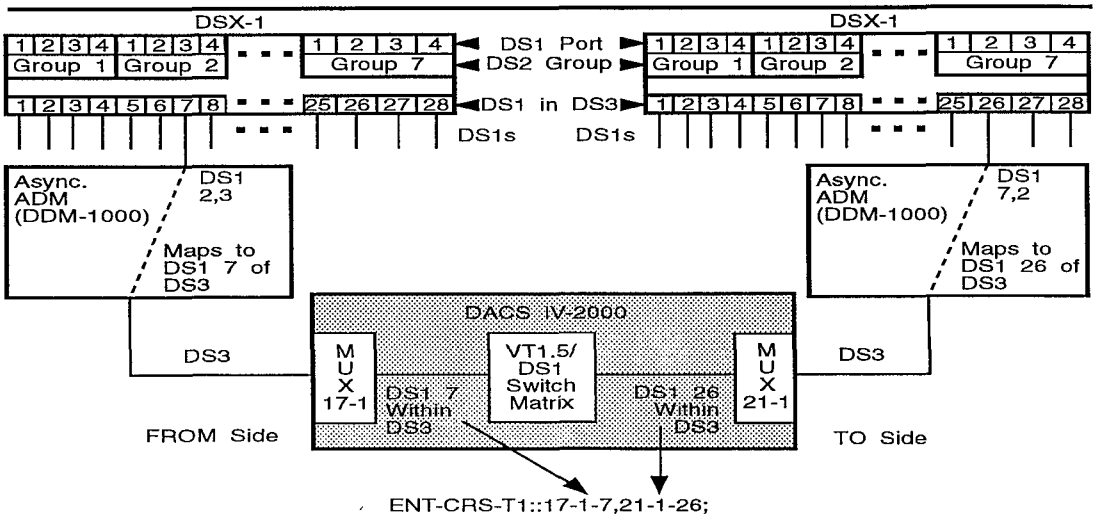



Figure 2-7. Asynchronous-to-Asynchronous Cross-Connection — TO/FROM Port Identification

**EXAMPLE 2: Asynchronous-to-Synchronous Mapping**

In Figure 2-8, a DACS IV-2000 is used to cross-connect a DS1 signal within a DS3 signal from an asynchronous ADM (DDM-1000) to a synchronous ADM (DDM-2000) via a VT1.5 signal within an STS-1 signal.

- The DS1 signal labeled 7 (or DS1 port 3 of DS2 group 2 on the DSX-1) on the FROM side is transmitted to the DS1 signal labeled 26 (or DS1 port 2 of DS2 group 7 on the DSX-1) on the TO side.
- The DDM-1000 on the FROM side accepts the DS1 signal on slot 2, port 3. Using Table 2-3 column 2 for the value 2,3 of DS2,DS1, the DS1 port from the DSX-1 maps into DS1 7 within the DS3 that is sent to the DACS IV-2000.
- Since the VT1.5 signal transmitted to the DDM-2000 on the TO side is mapped differently from the DS1 signal on the FROM side, using Table 2-3 column 5 for the value 7,2 (the DS1 signal at the DSX-1 on the TO side), the DACS IV-2000 must cross-connect the VT1.5 signal that to port 14.

Therefore (assuming that the DS3 enters the DACS IV-2000 at MUX-17-1 and the STS-1 exits at SMUX-22-1), the `ENT-CRS-T1::17-1-7:22-1-14;` command is used to cross-connect the DS1 at the DSX-1 on the FROM side to the DS1 at the DSX-1 at the TO side.

In this example, the DS1 at the DSX-1 on the TO side is mapped to VT1.5 14 within the STS-1 instead of DS1 26, because of the difference in the grouping of the signals.

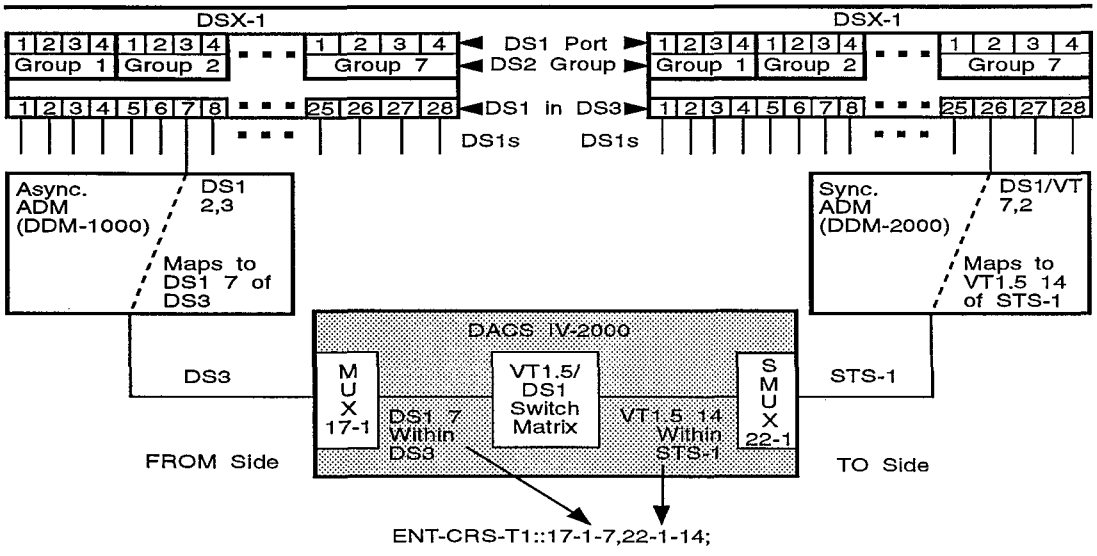



Figure 2-8. **Asynchronous-to-Synchronous Cross-Connection — TO/FROM Port Identification**

### EXAMPLE 3: Synchronous-to-Synchronous Mapping

In Figure 2-9, a DS1 signal from one DSX-1 is received by another DSX-1 that is transmitted to/from a DACS IV-2000 as a VT1.5 within an STS-1 signal through two synchronous ADMs (DDM-2000s).

- The DS1 signal labeled 7 (or DS1 port 3 of DS2 group 2 on the DSX-1) on the FROM side is transmitted to the DS1 signal labeled 26 (or DS1 port 2 of DS2 group 7 on the DSX-1) on the TO side.
- The DDM-2000 on the FROM side accepts the DS1 signal on slot 2, port 3. Since the DDM-2000 maps this DS1 into a VT1.5 signal, to determine the mapping, use column 5 of Table 2-3. The value 2,3 (VT group, VT) maps to VT1.5 16. Therefore, the DS1 from the DSX-1 on the FROM side is transmitted to the DACS IV-2000 as VT1.5 16 within the STS-1 received at SMUX-18-1.
- The VT1.5 signal transmitted to the DDM-2000 on the TO side is mapped using Table 2-3, column 5, for the value 7,2 (the DS1 signal at the DSX-1 on the TO side). Using SMUX-22-1 as the port the STS-1 is transmitted from, the DACS IV-2000 must cross-connect to VT1.5 14 of the STS-1 signal.

Therefore, the **`ENT-CRS-T1::18-1-16:22-1-14;`** command is used to cross-connect the DS1 at the DSX-1 on the FROM side to the DS1 at the DSX-1 at the TO side.

In this example, both VT1.5 signals at the DACS IV-2000 are mapped as different numbers than the DS1 signals in the first example.

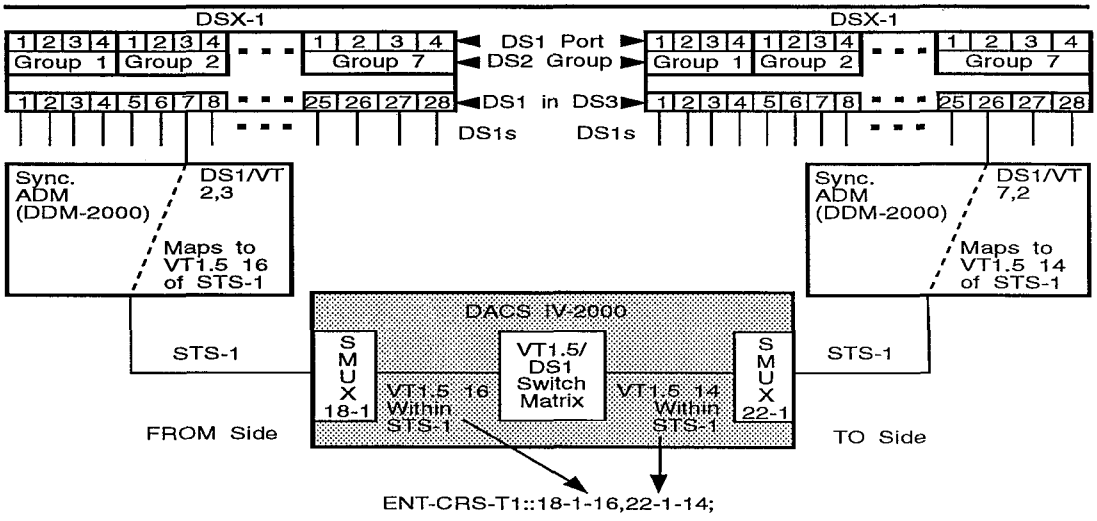



Figure 2-9. Synchronous-to-Synchronous Cross-Connection — TO/FROM Port Identification

## Special Service (Redlined) Connections

Circuits that are sensitive or require special care when being changed or deleted, should be made as a special service connection to prevent inadvertent changes in status. When entering cross-connections (one-way, two-way, and broadcast), the connection can be specified as a special service (redlined) connection (for example, 911 service or other sensitive connections). Connections specified as special service can only be deleted or modified if they are identified as a special service connection using the RDLD value in the Special Service Type parameter, or the YES value in the INCL parameter.

## DS1/STS-1/VT1.5 Facility Roll

The roll feature (rerouting) allows you to roll a facility from an existing path to a new path in service. This feature is useful for in-service rerouting of traffic to new systems. Rerouting can be temporary or permanent and can be between one-way or two-way cross-connections. Also, this feature can be used to roll service from one central office to another central office.

Facilities that can be rerouted:

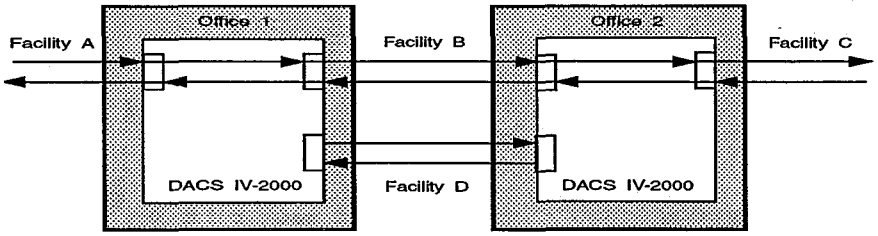
- A DS1 facility
- DS1 tributaries within DS3 facilities or EC-1 facilities
- All 28 DS1 tributaries of a DS3 facility (DS3 rerouting)
- EC-1 facilities and VT1.5 tributaries within EC-1 facilities.

The following two examples show how the roll feature can be used. The first example shows the rerouting of one facility to another facility between two central offices. The second example shows the rerouting of service to a common central office from two other central offices.

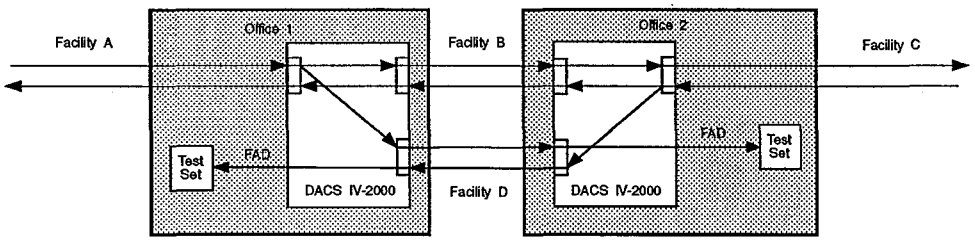
**EXAMPLE 1:**

Figure 2-10 shows how a facility is rerouted to another facility between two central offices. Rerouting of one facility to another facility involves coordination between two DACS IV-2000s as follows:

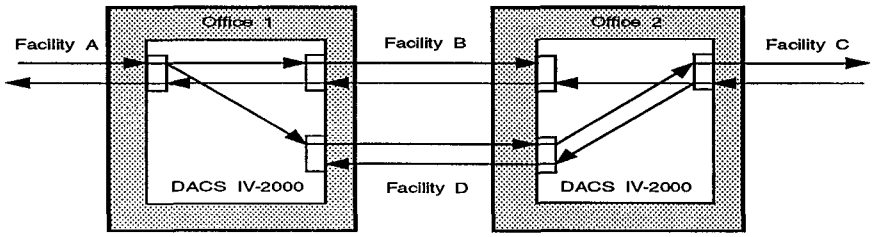
- In Figure 2-10A, Facility B is the original path between offices 1 and 2.
- In Figure 2-10B, a broadcast (bridge) cross-connection is established over Facility D from Office 1 to Office 2 and from Office 2 to Office 1. Test access can be performed to ensure that the signal over Facility D is being transmitted and received.
- In Figure 2-10C, after service over Facility D is tested, service is rolled in Office 2 from Facility B to Facility D.
- In Figure 2-10D, service is rolled in Office 1 from Facility B to Facility D.
- In Figure 2-10E, Facility B is taken out of service using `DLT-CONF` commanands.



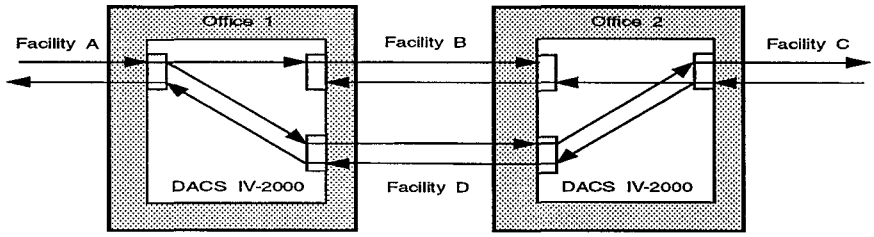

A. Existing Cross-Connections Over Original Facility



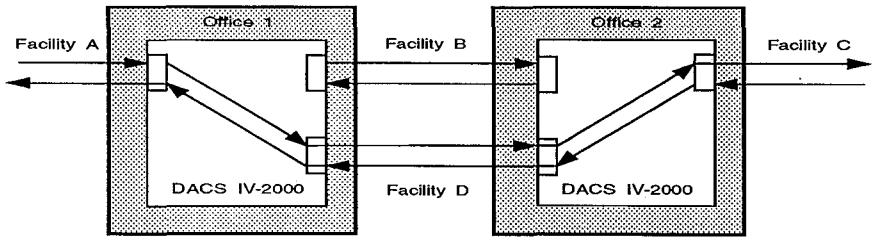

B. Establishing Broadcast Connection and Testing New Facility (Test Access)




C. Rolling Service Through Office 2 on New Facility)




D. Rolling Service Through Office 1 on New Facility



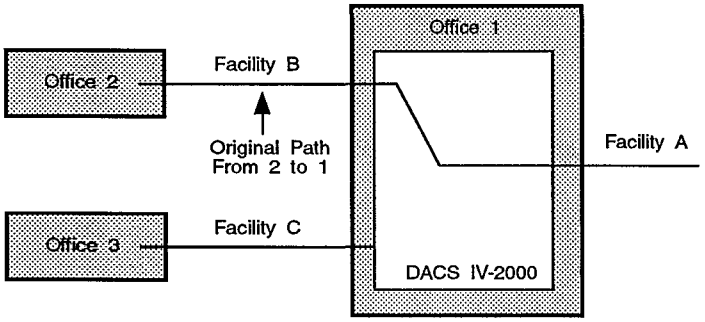

E. Taking Old Facility Out of Service (DLT-CONF Commands)

Figure 2-10. Facility Roll Between DACS IV-2000 Systems

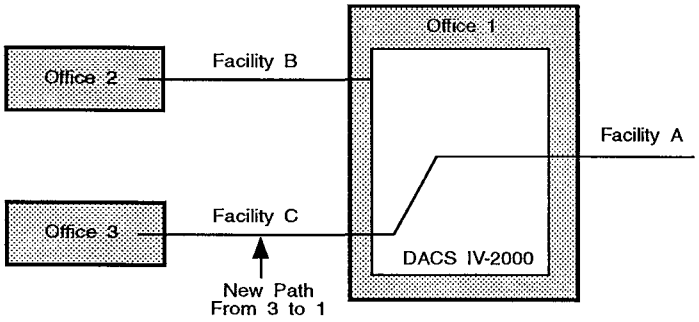
**EXAMPLE 2:**

Figure 2-11 shows how a facility is rerouted from one central office to another central office, with the new facility going to the same central office as the original facility. Rerouting of a facility in this manner involves the use of the **ENT-ROLL** command as follows:

- In Figure 2-11A, Facility B is the original transmission path between offices 1 and 2.
- Service is rolled (rerouted) from Office 3 through Facility C by entering the **ENT-ROLL** command on the DACS IV-2000 in Office 1 by using the port connected to Office 3 as the NEWFROM port (Figure 2-11B).




A. Existing Cross-Connection Between Two Central Offices




B. Rolling (Rerouting) Service From New Central Office With **ENT-ROLL** Command

Figure 2-11. Facility Roll Through One DACS IV-2000

## Loopbacks

The DACS IV-2000 provides DS1, DS3, STS-1, and VT1.5 loopback features that facilitate testing and trouble isolation.

The wideband loopback feature provides a loopback for VT1.5s within incoming STS-1 signals to be looped back through the switch (on a per-tributary basis) to the outgoing STS-1 of the same STS-1 signal. The STS-1 line loopback feature allows for connections of incoming STS-1 signals to the output direction, and maintains all incoming signal code and format violations and timing. Both loopback features are performed without changing any bits in the looped- back signal.

### DS1 Loopbacks

Loopbacks can be operated on a specified DS1 port or range of DS1 ports.

The following types of DS1 loopbacks are supported:

- LPBKL (Line Loopback) — loops the signal from the input port to the output port (towards the facility) at the DS1 Interface Module.
- LPBKT (Terminal Loopback) — loops the signal from the input port to the output port through the switch matrix in the switch module. DS1 terminal loopbacks are valid for DS1IF1, MUX1, MUX2, or SMUX1 circuit packs.
- LPBKI (Internal Loopback) — loops the signal from the output port to the input port (towards the switch) at the DS1 Interface Module.
- LPBKM (DS1 Tributary Loopback) — loops a DS1 tributary signal within a MUX2 circuit pack from the input port to the output port (toward the facility) at the DS3 Interface Module. DS1 tributary loopbacks are valid for either near-end or far-end on MUX2 circuit packs only.

Figure 2-12 shows examples of DS1 signal loopbacks.

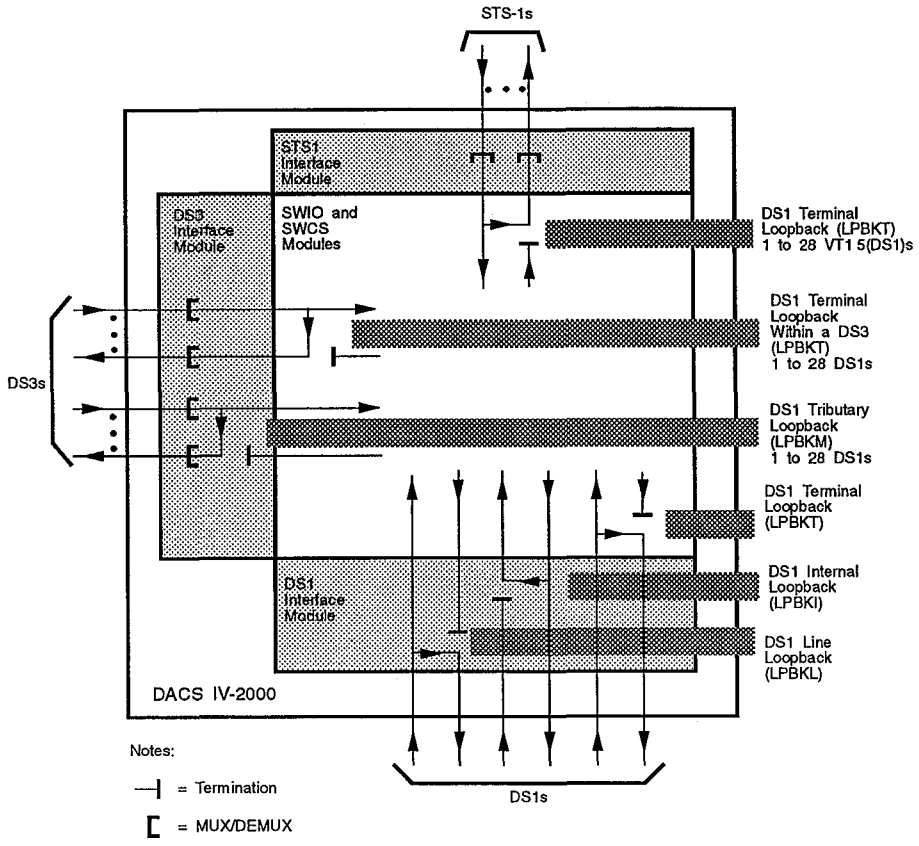



Figure 2-12. **DS1 Signal Loopbacks**

## DS3 Line Loopback

The DACS IV-2000 can loop back an incoming DS3 signal directly to the outgoing direction of the same port (see Figure 2-13). This loopback happens directly in the DS3 interface circuit pack (MUX2). This keeps the signal from entering the switch matrix and thus keeps the amount of hardware encountered to a minimum. Because the signal is not demultiplexed, it retains all its control bits, overhead bits, and bipolar violations. The DACS IV-2000 also preserves the timing of the looped-back signal. The only modification of the DS3 signal occurs when the system regenerates the signal to meet the specifications for an outgoing DS3 signal.

The DS3 line loopback can be activated using commands at an interface terminal connected to the DACS IV-2000. The loopback is also activated by embedded control in the DS3 bit stream provided by the C-bit parity format. This enhances the system's ability to perform trouble isolation within a digital network.

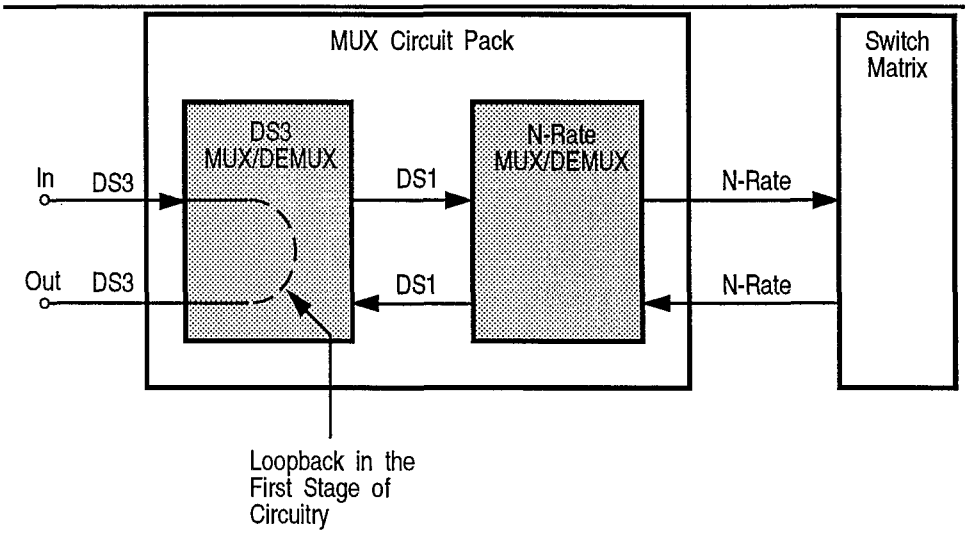



Figure 2-13. DS3 Line Loopback

## STS-1 Loopbacks

STS-1 loopbacks can be operated on a specified STS1 port or range of STS1 ports, either towards the facility or through the switch matrix of an STS1 Interface Module. STS-1 loopbacks can be one of the following two types:

- LPBKL (Line Loopback) — loops the signal from the input port to the output port (towards the facility) at the STS1 Interface Module.
- LPBKT (Terminal Loopback) — loops the signal from the input port to the output port through the switch matrix in the switch module. STS-1 terminal loopbacks are valid for the near end on SMUX circuit packs.

Figure 2-14 shows examples of a STS-1 loopbacks.

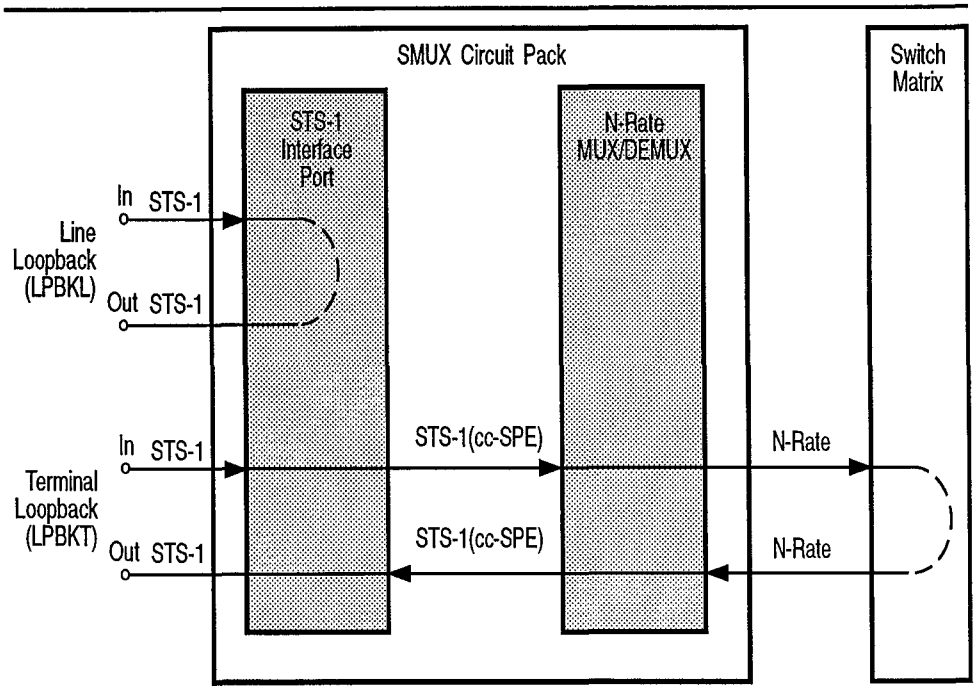



Figure 2-14. **STS-1 Line and Terminal Loopbacks**

## VT1.5 Loopbacks

VT1.5 loopbacks can be operated on a specified VT tributary of an STS-1 signal as a terminal loopback (LPBKT), which loops the VT1.5 signal from the input port to the output port through the switch matrix in the switch module. Figure 2-15 shows an example of a VT1.5 terminal loopback.

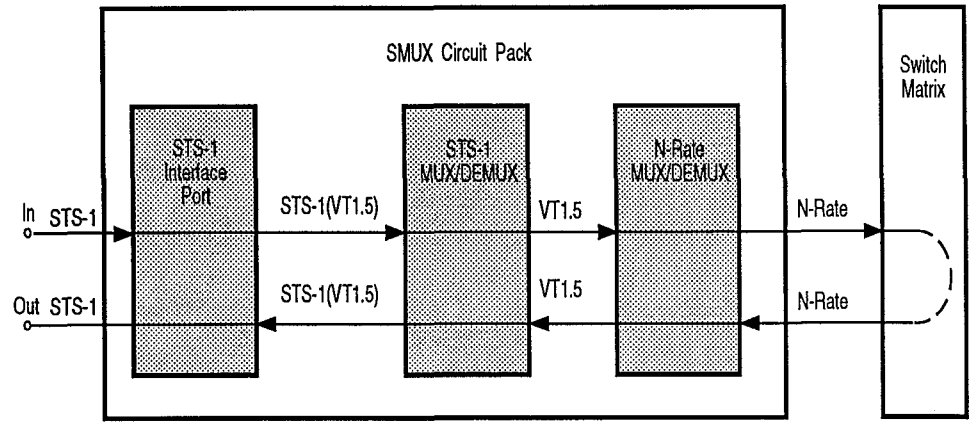



Figure 2-15. **VT1.5 Terminal Loopback**

## Test Access

The DACS IV-2000 supports all the DS1, VT1.5, and STS-1 test access modes specified in Bellcore TR-NWT-000818. The test access modes supported are MONE, MONF, SPLTA, SPLTB, SPLTE, SPLTF, LOOPE, LOOPF, MONEF, and SPLTEF. With these capabilities, the system can act as a digital test access unit (DTAU).

VT1.5 and STS-1 test access connections are accessed via the SONET interface. Individual VT1.5 tributaries must be accessed externally from an STS-1, for which test access is provided.

The ability to supply and monitor DS1, VT1.5, and STS-1 test signals, split connections, and perform loopbacks can simplify facility turnup and assist in trouble isolation.

Figure 2-16 shows the test-access naming conventions. The E-End and F-End are arbitrarily designated for a one-way or a two-way cross-connection.[1] For example, the E-End can be designated to correspond to a short-haul transmission path to equipment (such as a DACS III-2000) within the same Central Office; the

1. Traditionally E-End and F-End mean equipment end and facility end, respectively. However you can designate any port as E-End or F-End.

F-End can be designated to correspond to a long-haul transmission path to another Central Office. The E-End and F-End signals are terminated at DS1, DS3, or STS-1 Interface Modules.

Test access can be established at either the E-End or the F-End through a test-access port (TAP), which is also referred to as a facility access digroup (FAD).

The signal path through the frame from the E-End to the F-End is referred to as the A direction, and the signal path from the F-End to the E-End is the B direction. In a one-way cross-connection, the signal travels in the A direction. The In and Out designations indicate the direction to/from the E-End and F-End. After selecting designations of E-End and F-End, these designations must not change during the test-access session.

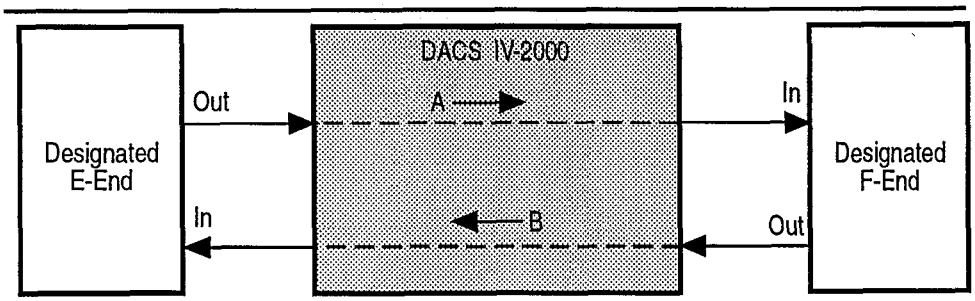



Figure 2-16. Test Access Conventions

Ten modes of test access are supported in the DACS IV-2000:

- MONE — The MONE mode of test access monitors the output of the E-End of an idle port, a one-way cross-connection, or a two-way cross-connection. It reads the incoming signal to the DACS IV-2000 in direction A.
- MONF — The MONF mode of test access monitors the output of the F-END of a two-way cross-connection. It reads the incoming signal to the DACS IV-2000 in direction B.
- MONEF — The MONEF mode of test access monitors both directions of a two-way cross-connection. This mode of test access requires two FADs. It reads the incoming signals to the DACS IV-2000 (the output from the E-End and F-End) in directions A and B.
- SPLTA — The SPLTA mode of test access splits the E-End (to FAD) to F-End (from FAD) connection of a one-way or two-way cross-connection to allow testing in the A direction.
- SPLTB — The SPLTB mode of test access splits the F-End (to FAD) to E-End (from FAD) connection of a two-way cross-connection to allow testing in the B direction.

- SPLTE — The SPLTE mode of test access splits the E-End to F-End of a one-way or two-way cross-connection to allow testing at the E-End. The incoming signal to the DACS IV-2000 in the A direction goes to the input of the FAD, and the output of the FAD is sent in the B direction.
- SPLTF — The SPLTF mode of test access splits the F-End to E-End of a two-way cross-connection to allow testing at the F-End. The incoming signal to the DACS IV-2000 in the B direction goes to the input of the FAD, and the output of the FAD is sent in the A direction.
- SPLTEF — The SPLTEF mode of test access splits both directions of a two-way cross-connection to allow testing at both the E-End and the F-End. This mode of test access requires two FADs. The incoming signal to the DACS IV-2000 in the A direction goes to the input of FAD-1, and the output of FAD-1 is sent in the B direction. The incoming signal to the DACS IV-2000 in the B direction goes to the input of FAD-2, and the output of FAD-2 is sent in the A direction.
- LOOPE — The LOOPE mode of test access establishes a terminal loopback on the E-End port and monitors the loopback signal. It reads the incoming signal to the DACS IV-2000 (output from the E-End) in the A direction.
- LOOPF — The LOOPF mode of test access establishes a terminal loopback on the F-End port and monitors the loopback signal. It reads the incoming signal to the DACS IV-2000 (output from the F-End) in the B direction.

In the following figures 2-17 through 2-26, three types of lines are used to illustrate the different connections. They are:

- Solid Line — represents the test access path up on the tested cross-connection
- Dotted Line — represents the continuation of an active cross-connection
- Dashed Line — represents one leg of a two-way cross-connection. If only a one-way cross-connection is active, the connection shown by the dashed line does not exist.

## Monitor Test Access

When creating DS1 monitor test-access connections, DS1 ports selected for E-End, F-End, and FAD can be on a DS1, DS3, or STS1 interface circuit pack. When creating VT1.5 and STS-1 monitor test-access connections, VT1.5 and STS1 ports can only be on STS1 interface circuit packs (SMUX).

### MONE Mode

The MONE mode of test access monitors the E-End of an idle port, a one-way cross-connection, or a two-way cross-connection. It reads the incoming signal in direction A.

In Figure 2-17, a monitor test-access connection is established from a testport located at port 1 of DS1GRP-15-1 to an idle port located at port 3 of DS1GRP-15-1. If the E-End is idle, the connections shown by the dotted and dashed lines are not present. If a one-way cross-connection exists from the E-End to the F-End, the connection shown by the dashed line is not present.

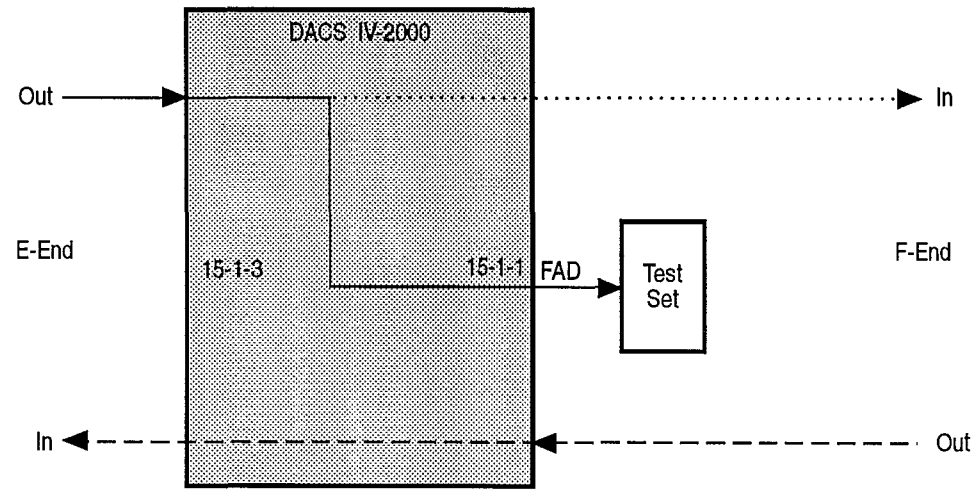



Figure 2-17. MONE Mode of Test Access

## MONF Mode

The MONF mode of test access monitors the F-End of a two-way cross-connection. It reads the incoming signal in direction B.

In Figure 2-18, a monitor test-access connection is established on the F-End of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport.

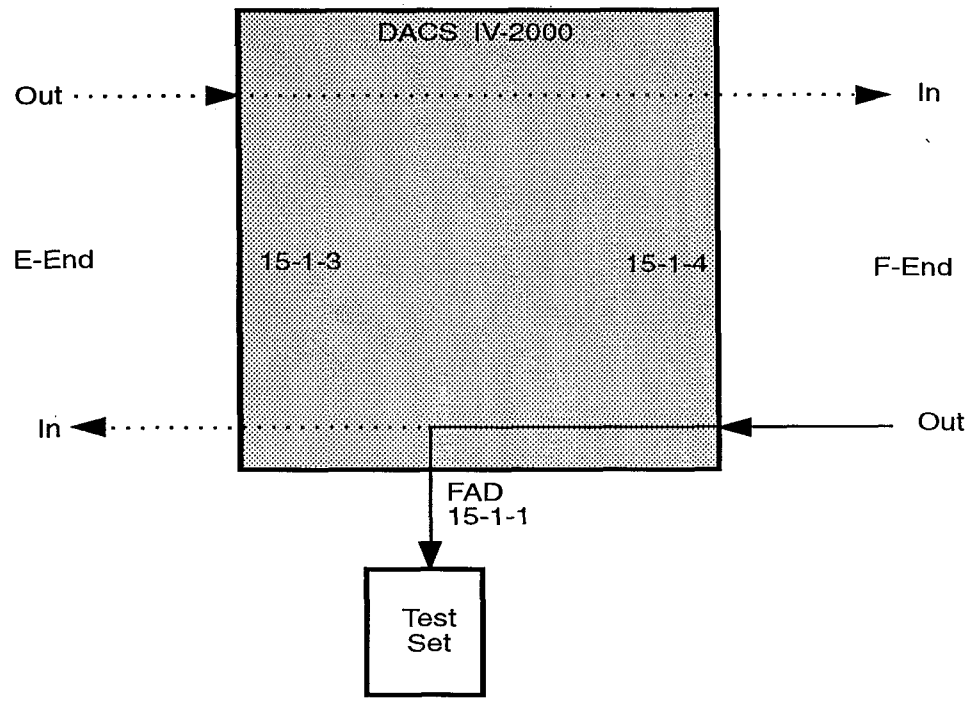



Figure 2-18. MONF Mode of Test Access

## MONEF Mode

The MONEF mode of test access monitors both directions of a two-way cross-connection. This mode of test access requires two FADs. It reads the incoming signals in directions A and B.

In Figure 2-19, a monitor test-access connection is established on both the E-End and the F-End of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Ports 1 and 2 of DS1GRP-15-1 as the testport. Only the odd-numbered port of the testport pair is specified in the test-access command and the MONEF mode of test access can only be established on a two-way cross-connection.

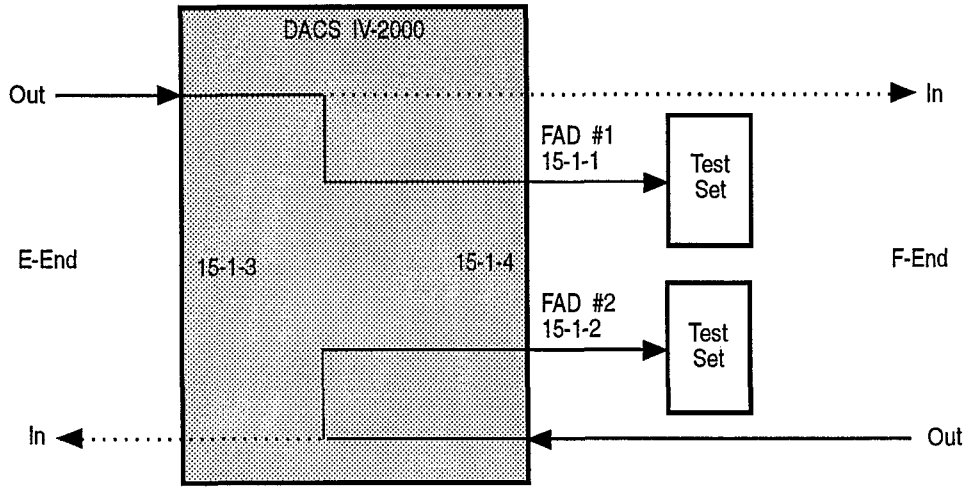



Figure 2-19. MONEF Mode of Test Access

## Split Test Access

When creating DS1 split test-access connections, DS1 ports selected for E-End, F-End, and FAD can be on a DS1, DS3, or STS1 interface circuit pack. When creating VT1.5 and STS-1 split test-access connections, VT1.5 and STS1 ports can only be on STS1 interface circuit packs (SMUXs).

### SPLTA Mode

The SPLTA mode of test access splits the E-End (to FAD) to F-End (from FAD) connection of a one-way or two-way cross-connection to allow testing in the A direction.

In Figure 2-20, a split test-access connection is established in the A direction on a one-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. On a one-way cross-connection from the E-End to the F-End, the connection shown by the dashed line is not present.

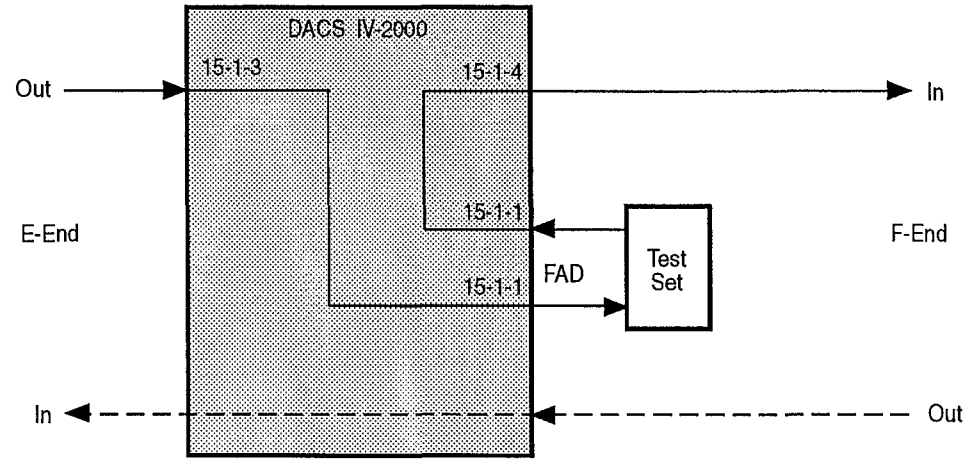



Figure 2-20. SPLTA Mode of Test Access

### SPLTB Mode

The SPLTB mode of test access splits the F-End (to FAD) to E-End (from FAD) connection of a two-way cross-connection to allow testing in the B direction.

In Figure 2-21, a split test-access connection is established in the B direction on a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport.

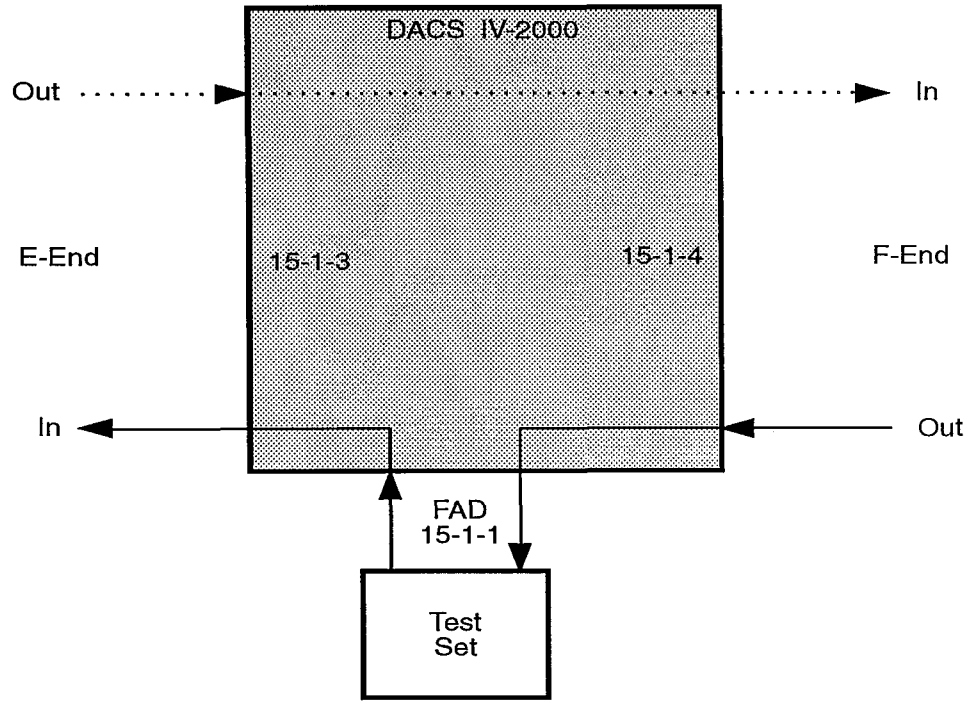



Figure 2-21. SPLTB Mode of Test Access

## SPLTE Mode

The SPLTE mode of test access splits the E-End to F-End of an idle port, a one-way cross-connection, or a two-way cross-connection to allow testing at the E-End. The incoming signal in the A direction goes to the input of the FAD, and the output of the FAD is sent in the B direction.

In Figure 2-22, a split test-access connection is established at the E-End of a one-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a Quasi-Random Signal Source (QRSS) or IDLE signal is sent to the F-End output port and to any other ports tied to the E-End input port. For a two-way cross-connection, the F-End input port is disconnected from the E-End output port during the test session. If a bridge is tied to the F-End input port, it is not affected. If the E-End port is idle, the signal paths represented by the dotted and dashed lines are not present. If a one-way cross-connection exists from the E-End to the F-End, the signal path represented by the dashed line is not present.

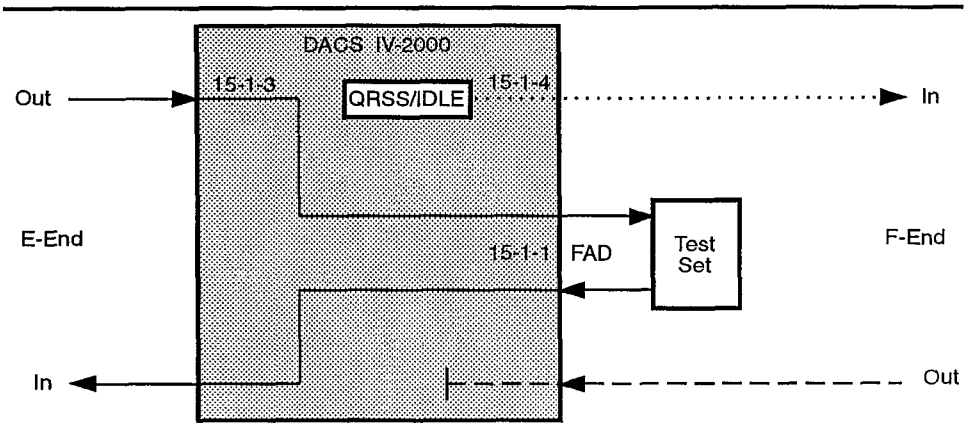



Figure 2-22. SPLTE Mode of Test Access

For DS1 SPLTE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5 and STS-1 SPLTE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

## SPLTF Mode

The SPLTF mode of test access splits the F-End to E-End of a two-way cross-connection to allow testing at the F-End. The incoming signal in the B direction goes to the input of the FAD and the output of the FAD is sent in the A direction.

In Figure 2-23, a split test-access connection is established at the F-End of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1 GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a QRSS or IDLE signal is sent to the E-End output port and to any other ports tied to the F-End input port unless the F-End port is idle. The E-End input port is disconnected from the F-End output port during the test session. If a bridge is tied to the E-End input port, it is not affected.

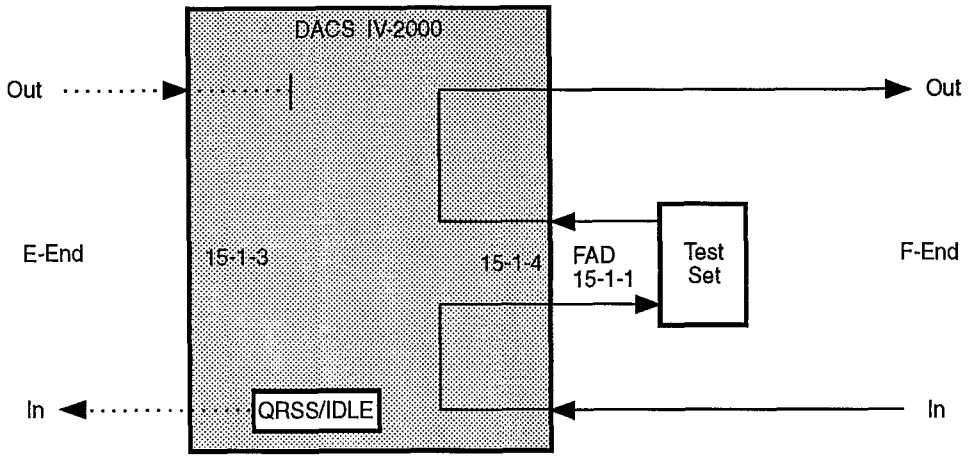



Figure 2-23. SPLTF Mode of Test Access

For DS1 SPLTF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5 and STS-1 SPLTF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

### SPLTEF Mode

The SPLTEF mode of test access splits both directions of a two-way cross-connection to allow testing at both the E-End and the F-End. This mode of test access requires two FADs. The incoming signal in the A direction goes to the input of FAD-1 and the output of FAD-1 is sent in the B direction. The incoming signal in the B direction goes to the input of FAD-2 and the output of FAD-2 is sent in the A direction.

In Figure 2-24, a split test-access connection is established on both the E-End and the F-End of a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Ports 1 and 2 of DS1GRP-15-1 as the testports.

Only the odd-numbered port of the testport pair is specified in the test-access command. The SPLTEF mode of test access can only be established on a two-way cross-connection.

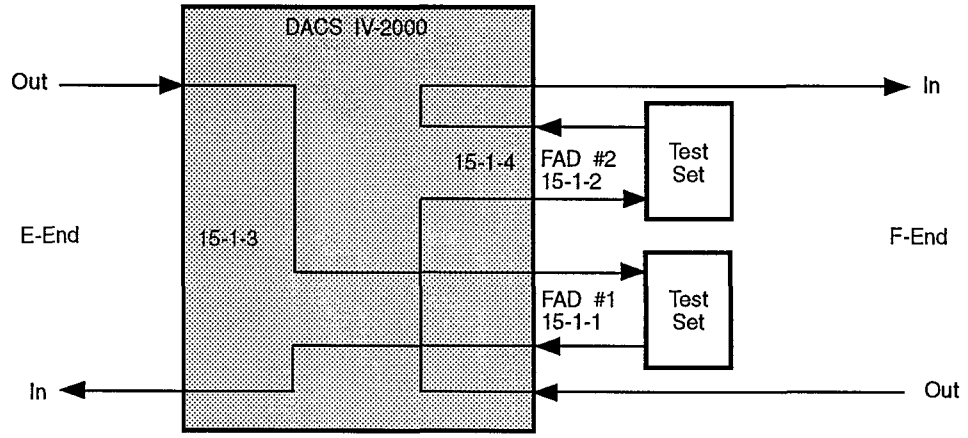



Figure 2-24. SPLTEF Mode of Test Access

## Loopback Test Access

When creating DS1 loopback test-access connections, DS1 ports selected for E-End, F-End, and FAD can be on a DS1, DS3, or STS1 interface circuit pack. When creating VT1.5 and STS-1 loopback test-access connections, VT1.5 and STS1 ports can only be on STS1 interface circuit packs (SMUX).

### LOOPE Mode

The LOOPE mode of test access establishes a terminal loopback on the E-End port and monitors the loopback signal. It reads the incoming signal in the A direction.

In Figure 2-25, a loopback test-access connection is established on a one-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a QRSS or IDLE signal is sent to the F-End output port The LOOPE mode can be established on either a one-way or a two-way cross-connection. For a two-way cross-connection, the F-End input port is disconnected from the E-End output port during the test session. If a bridge is tied to the F-End input port, it is not affected. If the E-End port is idle, the dotted and dashed connections are not present. If a one-way cross-connection exists from the E-End to the F-End, the signal path represented by the dashed line is not present.

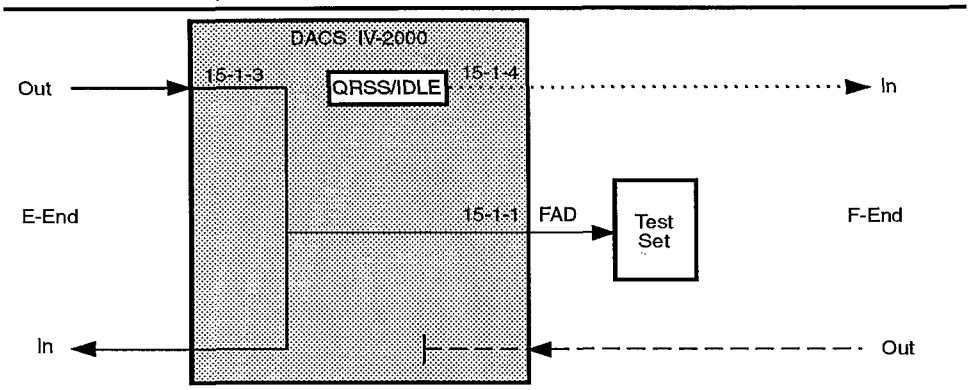



Figure 2-25. LOOPE Mode of Test Access

For DS1 LOOPE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5 and STS-1 LOOPE test access, the output mode of the F-End output port, along with any other output ports the E-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

### LOOPF Mode

The LOOPF mode of test access establishes a terminal loopback on the F-End port and monitors the loopback signal. It reads the incoming signal in the B direction.

In Figure 2-26, a loopback test-access connection is established on a two-way cross-connection from Port 3 of DS1GRP-15-1 to Port 4 of DS1GRP-15-1 using Port 1 of DS1GRP-15-1 as the testport. In this arrangement, a QRSS or IDLE signal is sent to the E-End output port. The E-End input port is disconnected from the F-End output port during the test session. If a bridge is tied to the F-End input port, it is not affected.

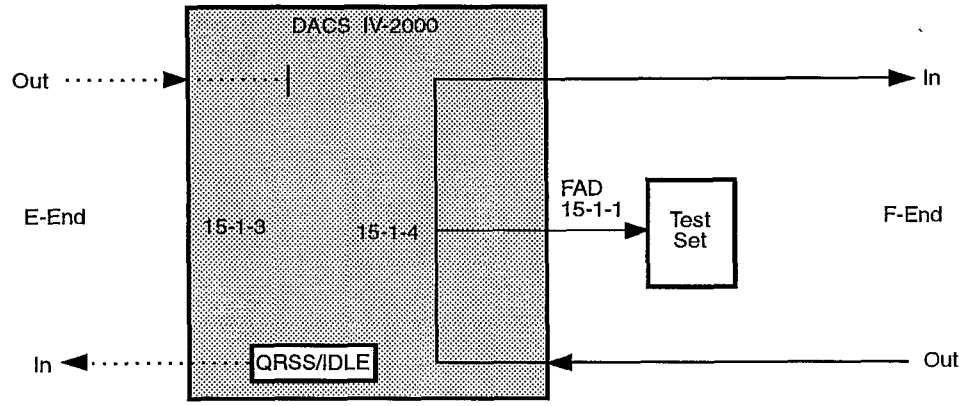



Figure 2-26. LOOPF Mode of Test Access

For DS1 LOOPF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the QRSS mode (if the ports are on DS1 and DS3 interface circuit packs and a QRSS source has been provisioned for the system) or to the IDLE mode. For VT1.5 and STS-1 LOOPF test access, the output mode of the E-End output port, along with any other output ports the F-End is transmitting to, is automatically set to the IDLE mode sending-path AIS.

## Link Association

When making test access and loopback connections, you can specify that the connection is associated with the user ID and link. When a connection is associated with the link, the connection is automatically disconnected or removed when the user that created the connection logs off. When a test access or loopback connection is made that is not associated with a link, when the user that created the connection logs off the connection remains until it is removed with a `DISC-TACC` (test access) or `RLS-LPBK` (loopbacks) command.

## Performance Monitoring

This section describes STS-1, VT1.5, DS1, and DS3 performance monitoring. The DACS IV-2000 provides DS1 and DS3 performance monitoring in accordance with Bellcore TR-TSY-000820. The DACS IV-2000 supports measurement and reporting of VT1.5 and STS-1 signal degradations in accordance with draft copies of the ANSI T1M1.3 standards. The following paragraphs provide a description of the performance-monitoring features.

### DS1 Performance Monitoring

The DS1 performance monitoring feature allows the DACS IV-2000 to monitor the health of DS1 facilities by collecting performance data for those facilities. The parameters that are monitored and measured to determine the health of a facility depend on the framing format and the performance monitoring option. The parameters that are monitored and measured also depend on whether near-end (monitored directly by the DACS IV-2000) or far-end (as updated by the upstream NTE) performance monitoring data are requested.

#### Framing Format

Framing format may be extended super frame, super frame, or unframed.

- Extended Super Frame (ESF) — Provides path performance monitoring using cyclic redundancy code (CRC) error checking to monitor the health of the incoming DS1 signal path. The CRC code checks for errors in all the bits of the DS1 signal. ESF format also provides a 4-kbit/s data link for communication between network elements connecting the DS1 facility which can be used to send Performance Report Messages as required by the ANSI T1.403 standard.
- Super Frame (SF) — Provides path performance monitoring using DS1 signal framing bits.
- Unframed (UNF) — Provides line performance monitoring for all DS1 signal formats coded with alternate mark inversion (AMI) or bipolar with 8-zero substitution (B8ZS). Line performance monitoring is performed using bipolar violation counts to monitor the received signal on the facility; this excludes the bipolar violations that are part of the B8ZS code.

#### Performance Monitoring Options

Performance monitoring option may be full time, camp-on, or scanned.

### Full-Time Monitoring

When using the full-time monitoring option, the software monitors the health of incoming DS1 facilities continuously. It supports both DS1s that terminate on DS1 interfaces and DS1 tributaries within a DS3. The DACS IV-2000 offers two types of full-time monitoring, dedicated and bridged.

- Dedicated full-time monitoring continuously checks the health of facilities terminating on a DS1 interface (DS1IF). Any of the 28 DS1s associated with the SWIF circuit pack can be provisioned for dedicated full-time performance monitoring. Dedicated full-time monitoring does not reduce the capacity of the DACS IV-2000.
- Bridged access full-time monitoring can continuously check the health of DS1 tributaries within a DS3 as well as DS1 facilities terminating on a DS1 interface (DS1IF). The DACS IV-2000 monitors these signals by bridging the DS1s to a performance monitoring generator and receiver (PMGR) circuit pack.

### Camp-on Monitoring

The camp-on monitoring option allows the DACS IV-2000 to monitor a specified DS1 or group of DS1s. The system provides two camp-on monitoring options: manual and automatic.

- Manual — Selected ports have a bridge of a DS1 signal passing through a SWIF or MUX to a port on a PMGR circuit pack; established using a command.
- Automatic — Occurs when the performance monitoring scanning option detects that a DS1 port has degraded service; that port is automatically connected to an available designated automatic camp-on port.

### Scanned Mode

This option is used to monitor DS1 signals not requiring full-time monitoring or is used when simpler and more cost-effective performance-monitoring measures are required. This option is ideal for checking general network and facility performance health, and is the most cost-effective DS1 performance-monitoring option offered by the DACS IV-2000. Using scanned monitoring, one PMGR circuit pack can monitor up to 420 DS1 signals, but can monitor only up to 28 DS1s when operating in the full-time or camp-on modes.

Scanned monitoring is accomplished by bridging 28 DS1 signals to the PMGR circuit pack. In the scanned option, up to 15 selected DS1 signals are monitored by a single port of the PMGR circuit pack in sequential order.

One scanning cycle for each group takes approximately 60 seconds, with about 50 seconds of that cycle actively monitoring the DS1 ports. If the maximum of 15 groups are monitored, then the time to revisit and rescan a DS1 group is 15 minutes. If only five are monitored, then the rescan cycle is five minutes. In the scan mode, all 420 DS1 signals associated with a particular pair of SWIO circuit packs can be sequentially monitored by the PMGR circuit pack, while only 28 DS1 signals of interface capacity are lost (a MUX or a SWIF circuit pack).

The PMGR circuit pack can occupy any MUX circuit pack slot (except the MUXP circuit pack slot) in the DS3 Interface Module and/or any SWIF circuit pack slot (except for the protection SWIF slot) in the DS1 Interface Module. When occupying a MUX circuit pack slot, the PMGR circuit pack has the ability to scan DS1 tributaries within a DS3 signal. One PMGR circuit pack can scan all the DS1 tributaries in a DS3 Interface-16 Module, while two PMGR circuit packs (one in the upper half of the module and the other in the lower half) are required in the DS3 Interface-32 Module. A PMGR circuit pack installed in a DS1 Interface Module (DS1 Interface or DS1 Interface-Protection) can scan all the DS1 signals in its module, as well as all the DS1 signals in the DS1 Interface Module (within a DS1 Interface Bay) associated with the SWIO circuit pack pair.

Scanned monitoring is available for ESF- and SF-framed DS1 tributaries within DS3 facilities as well as for similarly framed DS1 signals from DS1 facilities. Because the DACS IV-2000 monitors each DS1 signal for less than 100 percent of the time (varying with the number of DS1 groups scanned), it is not possible to gather as much detail about the DS1 performance as full-time monitoring. Scanned monitoring is not available for DS1 tributaries within EC-1 facilities. These signals must use manual camp-on monitoring.

### DS1 PM Mode Mixing

As described previously, the DACS IV-2000 provides three different DS1 performance-monitoring modes. These modes can be implemented independently or in unison. Any mix of modes can be in operation simultaneously, as dictated by the specific application.

Table 2-4 summarizes the DS1 performance-monitoring capabilities, the mixing and matching of modes, and the typical applications for each option. Restrictions to simplify administration of DS1 performance monitoring can be implemented. For example, full-time monitoring can be implemented for all incoming DS1 facilities and scanned monitoring for all DS1 tributaries of DS3 facilities. This is accomplished by using all SWIF2 circuit packs in the DS1 Interface Modules and by installing PMGR circuit packs in DS3 Interface Modules.

For hardware configuration information, including equipment constraints, refer to the section titled "DS1 Performance Monitoring Hardware" in Chapter 3.

Table 2-4. DS1 PM Summary

| Monitoring Characteristics | Monitoring Mode | | |
|---|---|---|---|
| | Dedicated Full-Time | Camp-on Full-Time | Scanned |
| DS1 Signals Monitored | DS1 Facilities | DS1 Facilities<br>DS1s on DS3 Facilities<br>DS1s on EC-1 Facilities | DS1 Facilities<br>DS1s on DS3 Facilities |
| Parameters Measured | See Table 2-5 | See Table 2-5 | See Table 2-5 |
| Formats Monitored | ESF, SF, and unframed | ESF and SF | ESF and SF |
| Monitoring Coverage | 28 DS1s associated with a SWIF2 | Any ESF-or SF-framed DS1s in the system except those using the dedicated monitoring method | Any ESF- or SF-framed DS1s associated with a PMGR (up to 420 DS1s) except for those using the dedicated monitoring method |
| Implementation | ■ SWIF2s monitor 28 assigned DS1s<br>■ Any mix of SWIF and SWIF2 circuit packs allowed in DS1 Interface Module | ■ PMGR occupies SWIF slot in DS1 Interface Module and/or MUX slot in DS3 Interface Module<br>■ PMGR can monitor any set of DS1s [from any interface module(s)] with any mix of full-time and camp-on<br>■ Any number of PMGRs allowed<br>■ Frame capacity reduced by 28 DS1s per PMGR | ■ DS1 Interface Module<br>— PMGR occupies SWIF slot<br>— 1 PMGR per pair of interface modules (SWIO pair)<br>■ DS3 Interface Module<br>— PMGR occupies MUX slot<br>— 1 PMGR per DS3 Interface-16 module<br>— 2 PMGRs per DS3 Interface-32 Module (1 in upper half and 1 in lower half)<br>■ Frame capacity reduced by 28 DS1s per PMGR |
| Typical Applications | ■ Full-time monitoring of all or large fraction of DS1 facilities | ■ Full-time monitoring of selected DS1s<br>■ Camp-on monitoring of selected DS1s to provide detailed examination of DS1s suspected of being of degraded quality | ■ Monitor performance health of any DS1s that do not require full-time monitoring |

## Monitored Parameters

The DACS IV-2000 monitors and reports both path and line performance parameters to verify that service-quality objectives specified in terms of these parameters are being met. Performance monitoring only occurs during available time because service-quality assessments cannot be determined during a period of service outage. From a service perspective, two important criteria must be verified:

- Availability of service, which is measured by the parameter UAS (Unavailable Seconds)
- Quality of service during available time, which is measured by the other performance-monitoring parameters.

In addition to the path and line parameters that are monitored and reported, the DACS IV-2000 can detect incoming trouble condition indicators on SF- and ESF-formatted DS1 signals.

### Near-End Path Parameters

Path performance-monitoring parameters apply only to ESF-formatted and SF-formatted signals. The path performance parameters are determined using the cyclic redundancy check (CRC-6) codes in the ESF format or using framing bit errors (FBE) in the SF format. The path parameters are listed below:

- Path Code Violation (CVP) — A count of CRC-6 violations in DS1 ESF- formatted signals or FBEs in DS1 SF formatted signals. A CRC-6 violation occurs when the received CRC-6 code is not identical to the locally calculated CRC-6 code. An FBE occurs when a frame bit error is received in the frame bit pattern of the SF formatted signal.
- Path Out-of-Frame Seconds (OOFS) — A count of out-of-frame (OOF) events occurring over the path. In measuring OOF events, an integration time of one second is used so that all the OOF events within that second are counted as one. An OOF event occurs when a density of two FBEs out of four consecutive frame bits are detected. An OOF defect is terminated when no FBEs occur within four or more consecutive frame bit positions.
- Path Errored Seconds (ESP) — A count of the seconds having at least one CVP or OOF (for ESF-formatted signals) or at least one FBE or OOF (for SF-formatted signals).
- Path Bursty Errored Seconds (BESP) — A count of one-second intervals with 2 to 319 CVPs and no OOFSs (for ESF-formatted signals) or one-second intervals with two to seven FBEs and no OOFSs (for SF-formatted signals). BESP is not monitored during scanned performance-monitoring mode.
- Path Severely Errored Seconds (SESP) — A count of one-second intervals with 320 or more CVPs or an OOF event (for ESF-formatted signals) or one-second intervals with eight or more FBEs or an OOFS (for SF-formatted signals).

- Unavailable Seconds (UAS) — A period of unavailable time beginning when an SESP occurs within 10 seconds or when an alarm indicating signal (AIS), loss-of-signal (LOS), or loss-of-frame (LOF) trouble condition is declared. Once unavailable, and if no failure is present, the DS1 path becomes available at the onset of 10 contiguous seconds with no SESPs.
- Path Degraded Minute (DM) — A service-related parameter that is defined on a frame-wide basis. Any available minute is considered a DM if it has all SESs removed and has more than the set threshold of CRC-6 violations. DMs do not apply to SF-formatted signals.

**Near-End Line Parameters**

DS1 line parameters only apply to DS1 signals that terminate on DS1 interface circuit packs in the DACS IV-2000. Line performance parameters are determined using bipolar violations. The line parameters are listed below:

- Line Code Violations (CVL) — are illegal bipolar violation (BPV) events. A BPV event for an AMI-coded DS1 signal is the occurrence of a pulse of the same polarity as the previous pulse. A BPV for a B8ZS-coded DS1 signal is the occurrence of a pulse of the same polarity as the previous pulse without being a part of the zero substitution code. This parameter is not monitored during an LOS condition. For unframed (UNF) DS1 signals interfacing with the DACS IV-2000, CVLs are used to determine the bit error rate (BER) of the incoming DS1 signal. Also, signals that are not being monitored by the full-time or camp-on mode have their BER thresholds estimated with CVL counting.
- Line Errored Seconds (ESL) — measures seconds during which at least one CVL has occurred.
- Line Severely Errored Seconds (SESL) — measures seconds with more than 1544 CVLs. This parameter is not monitored during a LOS condition.

**Far-End Path Parameters**

Far-end path parameters are only collected in the system by reading the extended super frame (ESF) data link. The performance parameters are not written by the DACS IV-2000 onto this data link.

The ANSI T1.403 standard specifies that the equipment that terminates an ESF DS1 facility monitors the performance of the incoming signal and transmits a performance report to the far-end once per second. The report contains performance data for each of the previous four one-second intervals. The DACS IV-2000 is capable of reading this report and maintaining a database of the far-end performance data.

The far-end path parameters are listed below:

- Severely Errored Frame Seconds (SEFS) — A count of one-second performance report message intervals received from the far-end, containing one or more Severely Errored Frame (SEF) events. An SEF event is the occurrence of two or more FBEs within a 0.75-ms window.

- Controlled Slipped Seconds (CSS) — A count of one-second performance report message intervals received from the far-end containing one or more controlled slip (CS) events. A CS is the replication or deletion of the 192 payload bits of a DS1 frame by a path terminating network element. A CS can be performed when a difference exists between the timing of a synchronous receiving terminal and the received signal intervals.
- Path Code Violation (CVP) — A count of far-end CRC-6 violations occurring during a defined accumulation period. Since far-end CRC-6 errors occurring during each second are reported to the near-end (not as exact counts, but in form), the far-end CVP parameter is accumulated as one of six groups: G1 = 1 CVPs, G2 = 5 CVPs, G3 = 10 CVPs, G4 = 100 CVPs, G5 = 319 CVPs, and G6 = 333 CVPs.
- Path Errored Seconds (ESP) — A count of 1-second performance-report message intervals containing one or more CVP events, one or more SEF events, or one or more CS events.
- Path Severely Errored Seconds (SESP) — A count of 1-second performance-report message intervals containing 320 or more CVP events or one or more SEF events.
- Path Bursty Errored Seconds (BESP) — A count of 1-second-performance report message intervals containing between 2 and 319 CVP events and no SEF events. BESP is not monitored during scanned performance-monitoring mode.
- Path Degraded Minute (DM) — A service-related parameter that is defined on a frame-wide basis. Any available minute is considered a DM if it has all SESs removed and has more than the set threshold of CRC-6 violations. DMs do not apply to SF formatted signals.
- Unavailable Seconds (UAS) — A period of unavailable time beginning when 10 consecutive seconds with an SESP are occurring or when an alarm indicating signal (AIS), loss-of-signal (LOS), or loss-of-frame (LOF) trouble condition is declared. Once unavailable, and if no failure is present, the DS1 path becomes available at the onset of 10 contiguous seconds with no SESPs.

### Parameter Measurements

The DACS IV-2000 performance monitoring accumulates measurements for the parameters listed in Table 2-5. This table shows those parameters that are measured given the options of full-time, camp-on, and scan performance monitoring in conjunction with line format and location.

Table 2-5. DS1 PM Parameters

| Location | Monitored Parameter | Full-Time | | | Camp-On | | | Scan | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | ESF | SF | UNF | ESF | SF | UNF | ESF | SF | UNF |
| Near-End | CVL | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| | ESL | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| | SESL | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| | CVP | ✓ | ✓ | - | ✓ | ✓ | - | ✓ | ✓ | - |
| | ESP | ✓ | ✓ | - | ✓ | ✓ | - | ✓ | ✓ | - |
| | BESP | ✓ | ✓ | - | ✓ | ✓ | - | - | - | - |
| | SESP | ✓ | ✓ | - | ✓ | ✓ | - | ✓ | ✓ | - |
| | OOFS | ✓ | ✓ | - | ✓ | ✓ | - | ✓ | ✓ | - |
| | DM | ✓ | - | - | ✓ | - | - | - | - | - |
| | UAS | ✓ | ✓ | - | | ✓ | - | - | - | - |
| Far-End | SEFS | ✓ | - | - | ✓ | - | - | ✓ | - | - |
| | CSS* | ✓ | - | - | ✓ | - | - | - | - | - |
| | ESP | ✓ | - | - | ✓ | - | - | ✓ | - | - |
| | SESP | ✓ | - | - | ✓ | - | - | ✓ | - | - |
| | CVP | ✓ | - | - | ✓ | - | - | - | - | - |
| | BESP | ✓ | - | - | ✓ | - | - | - | - | - |
| | DM | ✓ | - | - | ✓ | - | - | - | - | - |
| | UAS | ✓ | - | - | ✓ | - | - | - | - | - |

**Note:** ✓ Denotes parameter being monitored for the given performance-monitoring option and line format.

* This is SLS in previous releases.

Table 2-6 lists the default threshold levels for measured parameters in the full-time and camp-on performance-monitoring modes. Table 2-7 lists the default threshold levels for measured parameters in the scan performance-monitoring mode. Table 2-8 lists the range of threshold levels for measured parameters in the full-time and camp-on performance-monitoring modes. Table 2-9 lists the range of threshold levels for measured parameters in the scan performance-monitoring mode. Threshold levels are given for both short-interval (15-minute and hourly) accumulated data and for daily accumulated data. As indicated, the line performance parameters (CVL, ESL, and SESL) are valid only for the DS1s that terminate on the DACS IV-2000 through a DS1 interface circuit pack.

Table 2-6. **Default Thresholds for Full-Time, Camp-On, and Line DS1 Performance Monitoring Full-Time/Camp-On DS1 PM Defaults**

| Monitored Parameter | DS1 Framing Format | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Extended Super Frame | | | | Super Frame | | Unframed | |
| | Far-End* | | Near-End | | | | | |
| | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily |
| **Full Time (SWIF2 Based) and Camp-on (PMGR Based)** | | | | | | | | |
| CVP | 53184 | 132960 | 53184 | 132960 | 6615 | 16540 | - | - |
| ESP | 259 | 648 | 259 | 648 | 38 | 95 | - | - |
| BESP | 100 | 600 | 100 | 600 | 19 | 90 | - | - |
| SESP | 40 | 100 | 40 | 100 | 11 | 27 | - | - |
| OOFS | - | - | 7 | 17 | 7 | 17 | - | - |
| DM | 15 | 360 | 15 | 360 | - | - | - | - |
| UAS | 10 | 10 | 10 | 10 | 10 | 10 | - | - |
| SEFS | 7 | 17 | - | - | - | - | - | - |
| CSS | 7 | 17 | - | - | - | - | - | - |
| **Line (DS1IF Based)** | | | | | | | | |
| CVL† | - | - | 53360 | 133400 | 53360 | 133400 | 53360 | 133400 |
| ESL† | - | - | 259 | 648 | 259 | 648 | 259 | 648 |
| SESL† | - | - | 40 | 100 | 40 | 100 | 40 | 100 |

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

† Only applicable for DS1 signals terminating on DS1Interface Modules.

Table 2-7. **Default Thresholds for Scan (PMGR Based) DS1 Performance Monitoring Scan**

| Monitored Parameter | DS1 Framing Format | | | | | |
|---|---|---|---|---|---|---|
| | Extended Super Frame | | | | Super Frame | |
| | Far-End* | | Near-End | | | |
| | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily | 15 Min and Hourly | Daily |
| CVP | - | - | 1772 | 4432 | 177 | 443 |
| ESP | 8 | 21 | 8 | 21 | 1 | 3 |
| SESP | 1 | 3 | 1 | 3 | 1 | 3 |
| OOFS | - | - | 1 | 2 | 1 | 2 |
| SEFS | 1 | 2 | - | - | - | - |

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

Table 2-8. Threshold Value Ranges for Full-Time, Camp-On, and Line DS1 Performance Monitoring

| Monitored Parameter | Far-End* | | | Near-End | | |
|---|---|---|---|---|---|---|
| | 15 Min | Hourly | Daily | 15 Min | Hourly | Daily |
| **Full Time (SWIF2 Based) and Camp-on (PMGR Based)** | | | | | | |
| CVP | 0-2097152 | 0-8388608 | 0-134217728 | 0-2097152 | 0-8388608 | 0-134217728 |
| ESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| BESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| SESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| OOFS | - | - | - | 0-900 | 0-3600 | 0-65535 |
| DM | 0-15 | 0-60 | 0-1440 | 0-15 | 0-60 | 0-1440 |
| UAS | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| SEFS | 0-900 | 0-3600 | 0-65535 | - | - | - |
| CSS | 0-900 | 0-3600 | 0-65535 | - | - | - |
| **Line (DS1IF Based)** | | | | | | |
| CVL† | - | - | - | 0-2097152 | 0-8388608 | 0-134217728 |
| ESL† | - | - | - | 0-900 | 0-3600 | 0-65535 |
| SESL† | - | - | - | 0-900 | 0-3600 | 0-65535 |

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

† Only applicable for DS1 signals terminating on DS1Interface Modules.

Table 2-9. Threshold Value Ranges for Scan (PMGR Based) DS1 Performance Monitoring

| Monitored Parameter | Far-End* | | | Near-End | | |
|---|---|---|---|---|---|---|
| | 15 Min | Hourly | Daily | 15 Min | Hourly | Daily |
| CVP | - | - | - | 0-65535 | 0-65535 | 0-65535 |
| ESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| SESP | 0-900 | 0-3600 | 0-65535 | 0-900 | 0-3600 | 0-65535 |
| OOFS | - | - | - | 0-900 | 0-3600 | 0-65535 |
| SEFS | 0-900 | 0-3600 | 0-65535 | - | - | - |

* Far-end parameters are only applicable to Extended Super Frame (ESF) DS1 signals with ports provisioned for FENDNTE = ANSI.

The path performance parameters are determined using the cyclic CRC-6 codes in the ESF format or using FBE in the SF format. Line performance parameters are based on bipolar violations.

The monitoring time interval can be provisioned for the short accumulation period measured parameters to be either 15 minutes or 60 minutes. Daily accumulation period parameters are accumulated for 24-hour periods that begin at midnight. Data (for the 15- or 60-minute period) is stored for the preceding 24 hours, daily information is stored for seven days.

**Trouble Condition Reporting**

Facility alarm messages are generated if a LOS condition occurs or if the BER threshold is reached. The BER is based on BPVs, the framing bits of the SF format, or the CRC-6 bits of the ESF format. The BER can be set to a value in the range of $10^{-3}$ through $10^{-9}$ errors per second. In addition to reporting the LOS and BER alarms, the DACS IV-2000 reports incoming AIS, yellow alarm, and LOF status conditions.

Monitoring for BER threshold crossings is independent of performance monitoring. Therefore, the performance-monitoring feature does not have to be provisioned for the system to monitor the BER count. The system monitors the BER rate for the threshold levels $10^{-3}$ through $10^{-8}$ for SF-formatted signals or $10^{-3}$ through $10^{-9}$ for ESF-formatted signals.

If the BER count for a specific DS1 signal exceeds the threshold, the system sends a `REPT ALM T1` message and flashes the LED on the circuit pack, thereby terminating the DS1 signal.

## DS1 PM Data Reporting

The system database maintains running tallies of all the parameters monitored by the DS1 performance-monitoring hardware. When a parameter count is changed, data is collected based on the parameter and the collection interval previously selected. Each parameter has a predetermined threshold established by the system administrator. If a threshold is reached, the system generates a threshold crossing alert (TCA) message over the administrative links. Records of the processed performance-monitoring data are generated and may be retrieved. The system also provides the capability to schedule performance reports to be generated according to a pre-defined timetable. Schedules can be established for automatic performance reports and can specify:

- Starting time of the first report
- Interval between reports (can be set to a value in the range of 15 minutes to 24 hours for the 15-minute or 1-hour data, or from 1 to 7 days for the daily data)
- Facilities included in the report
- Parameters to be reported
- Monitoring time period covered by each report
- Total number of reports.

**NOTE:**
The current short interval (15-minute or 1 hour) and the current daily total DS1 path performance-monitoring data being collected is lost if:

- A circuit pack fails or is removed in a DS1 protection group (a pair of DS1IFs and SWIF circuit packs)
- A manual switch to protection in a DS1 protection group is made
- A PMGR1 circuit pack fails or is removed
- A UC2 circuit pack in a DS1 interface module and/or a module equipped with PMGR1 circuit packs is extracted, fails or is removed.

Failure of both hard disks (PRI) causes loss of the 7-day history of daily total DS1 performance-monitoring data for all monitored DS1 facilities on the DACS IV-2000.

Any unused ports being monitored, either full-time or scanned, should be provisioned as UNF. Since whole DS1 interface groups or the DS1 ports associated with MUXs can be monitored or scanned, unused ports are included in the monitoring process. Therefore, provisioning unused ports to UNF reduces the number of `REPT EVT T1` messages that are received at the CILINKs.

The system generates scheduled reports using the `REPT PM T1` message. To receive these reports, the administrative link(s) must meet the following conditions:

- The correct authorization code must be logged in.
- Message Screening must be set to **AUTO** or **ALL**.
- User Privilege Code (UPC) of **PM1**, **PM2**, **PM3**, **PM4**, or **PM5** must be used.

The `REPT PM T1` message reports DS1 performance information as scheduled in the **SCHED-PMREPT-T1** command.

## DS3 Performance Monitoring

DS3 performance monitoring provides the following:

- DS3 performance data based on path as well as line parameters
- Processed performance data in compliance with Bellcore TR-TSY-000820 and AT&T Compatibility Bulletin Number 149, *Maintenance Standards for Digital Transmission Systems, Issue 3* (CB149)
- Performance-monitoring data available on all message-based administrative links.

Except for the Copy of Parity Bits (CP-BIT) errors of the C-bit parity format, the DACS IV-2000 normally does not monitor the total path of the DS3 signal. This is because upstream equipment cleans up the signal before it reaches the DACS IV-2000. With enhanced performance monitoring, the system now monitors the F- and M-bits in the DS3 signal to provide DS3 path performance monitoring for the M13 line DS3 format. In addition, the DS3 path performance monitoring for the C-bit parity format is done by monitoring the CP-BITS errors.

### Monitored Parameters

The DACS IV-2000 processes performance data in compliance with CB-149 (PSET#1) and Bellcore TR-TSY-000820 (PSET#2). This applies to the M13 line and C-bit parity Bipolar Violations (BPV) formats, and to line monitoring (LCV and DS3 parity) and path monitoring (DS3 F- and M-bits, DS3 CP-BITS, and DS3 far-end block error bits).

The following performance BER metric parameters can be monitored:

Bipolar Violations (BPV); BPVs monitored but not stored
Parity (PTY)
Copy of Parity Bits (CP-BITS)
F and M Bits Adjusted (FMA-BITS)
F and M Bits Nonadjusted (FMN-BITS).

At any given time, only one primitive (BER metric parameter) can be monitored on a DS3 port. The CP-BITS primitive is valid only for the C-bit parity format (not for the M13 line format). In addition, the BER alarm threshold can be provisioned to any one of the following rates: $10^{-3}$, $10^{-4}$, $10^{-5}$, $10^{-6}$,$10^{-7}$, $10^{-8}$, or $10^{-9}$ errors per second.

With DS3 performance monitoring, the software reports all performance parameters and alarm conditions over any of the DACS IV-2000 administrative links. DS3 performance parameters monitored by the DACS IV-2000 are described below.

**NOTE:**
Removing a MUX2 circuit pack or failure of a MUX2 circuit pack causes the loss of all stored DS3 performance-monitoring data for the associated DS3 facility.

Table 2-10 summarizes the DS3 performance parameters that are monitored by the DACS IV-2000.

Table 2-10. DS3 PM Parameters

| Parameter Set | Path and Line Parameter |
|---|---|
| PSET#1<br>(CB149) | BEC<br>OOFS<br>TPA<br>TPB<br>TPC<br>UAS |
| PSET#2<br>(TR-TSY-000820) | CV<br>OOFS<br>ES<br>SES<br>UAS |

**Parameter Set #1**

The following are the performance monitored parameters specified by Compatibility Bulletin No. 149 requirements:

- Block Error Counts (BEC) — A count of M-frames received with at least one P-bit parity error, one F- and M-bit error, or one line code violation (LCV). A LCV event occurs when bipolar violations (BPV) or excessive zeros (EXZ) are detected. A BPV for a bipolar with 3-zero substitution (B3ZS)-coded DS3 signal is the occurrence of a pulse of the same polarity as the previous pulse without being part of the zero substitution code. An EXZ is the occurrence of any zero string length of 3 bits or more.
- Out-Of-Frame Seconds (OOFS) — A count of OOF events. An OOF event occurs when 3 out of 16 F-bit errors are received or when 2 errored M-bit patterns out of 4 M frames are received.
- Errored Seconds Type A (TPA) — A count of 1-second intervals with no OOF events and exactly one BEC.
- Errored Seconds Type B (TPB) — A count of 1-second intervals with no OOF events and between 1 and 44 BECs.
- Errored Seconds Type C (TPC) — A count of 1-second intervals with either an OOF event or 45 or more BECs.
- Unavailable Seconds (UAS) — Measures the time period that service is unavailable. The line is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, and no

failure is present, the path becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the line is unavailable.

PSET#1 performance parameters have settable thresholds for the current 15-minute interval and for the 96 15-minute (24 hours) rolling total. Their default values for the given time interval are shown in Table 2-11.

Table 2-11. **Monitored Parameters For PSET#1 (CB149) Counters — Register Size and Default Values**

| Parameter | Interval | | | |
|---|---|---|---|---|
| | Current 15 Minutes and Last 96 15-minute intervals | | 24-Hour Total† | |
| | Default | Range | Default | Range |
| Number of Block Errors (BEC)* | 4000 | 0-8458200 | 386500 | 0-811987200 |
| Errored Seconds A (TPA) | 30 | 0-900 | 90 | 0-65535 |
| Errored Seconds B (TPB) | 30 | 0-900 | 90 | 0-65535 |
| Errored Seconds C (TPC) | 20 | 0-900 | 60 | 0-65535 |
| Out-of-Frame Seconds (OOFS) | 10 | 0-900 | 30 | 0-65535 |
| Unavailable Seconds (UAS) | 30 | 0-900 | 90 | 0-65535 |

* MUX2 circuit pack only.

† The 24-hour total is the sum of the last 96 15-minutes rolling.

When these thresholds are reached, a corresponding TCA message is generated. These thresholds are modifiable, and if you do not specify a threshold crossing level, the DACS IV-2000 assumes the default value for that parameter. If the count of any of the above parameters exceeds the capacity of a specific register, the system pegs the register at the maximum value. The register reinitializes at the end of the data-collection interval after storing the data in memory.

The only allowed DS3 accumulation period for the PSET#1 parameters is the 15-minute interval, which is set during provisioning. A rolling window and a rolling total of the last 96 15-minute intervals are provided. A validity indicator provides an indication of whether data being sent to an operations system (OS) or administrative link is valid and covers the entire accumulation period. This indicator can have a value of `COMPL` (complete), `PRTL` (partial), or `NA` (not available).

### Parameter Set #2

The following are the performance-monitored parameters specified by Bellcore TR-TSY-000820 requirements:

- Coding Violations (CV) — A count of errors detected in an M-frame. M-frame errors are determined from line code violations (LCV), DS3 frame parity errors (P-bit or CP-bit errors), or DS3 F- and M-bit errors. A LCV event occurs when bipolar violations (BPV) or excessive zeros (EXZ) are detected. A BPV for a B3ZS-coded DS3 signal is the occurrence of a pulse of the same polarity as the previous pulse without being part of the zero substitution code. An EXZ is the occurrence of any zero string length of 3 bits or more.
- Out-Of-Frame Seconds (OOFS) — A count of OOF events. An OOF event occurs when 3 out of 16 F-bit errors are received or when 2 errored M-bit patterns out of 4 M frames are received.
- Errored Seconds (ES) — A count of 1-second intervals in which one or more CVs or one or more OOF events have occurred.
- Severely Errored Seconds (SES) — A count of 1-second intervals in which a BER greater than $10^{-6}$ or one or more OOF events have occurred.
- Unavailable Seconds (UAS) — Measures the time period that service is unavailable. The line is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, and no failure is present, the path becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the line is unavailable.

PSET#2 performance parameters have settable thresholds for the current 15-minute interval, the current 1-hour interval, and for the 1-day interval (96 15-minute or 24 1-hour intervals). Their default values are given in Table 2-12.

Table 2-12. **Monitored Parameters For PSET #2 (TR820) Counters — Register Size and Default Values.**

| Parameter | Interval | | | | | |
|---|---|---|---|---|---|---|
| | Current 15 Minutes | | Current 1 Hour* and Last 24 1-Hour Intervals | | Current Day* and Last 7 Days of daily totals | |
| | Default | Range | Default | Range | Default | Range |
| Coding Violations (CV) | 4000 | 0-8458200 | 16100 | 0-33832800 | 386500 | 0-811987200 |
| Errored Seconds (ES) | 40 | 0-900 | 40 | 0-3600 | 90 | 0-65535 |
| Severely Errored Seconds (SES) | 20 | 0-900 | 20 | 0-3600 | 60 | 0-65535 |
| Out-of-Frame Seconds (OOFS) | 10 | 0-900 | 10 | 0-3600 | 30 | 0-65535 |
| Unavailable Seconds (UAS) | 30 | 0-900 | 30 | 0-3600 | 90 | 0-65535 |

* Current hour is the sum of 15-minute intervals beginning on the hour and current day is the sum of hourly intervals beginning at midnight.

When these thresholds are reached, a corresponding TCA message is generated. These thresholds are modifiable, and if a threshold crossing level is not specified, the DACS IV-2000 assumes the default value for that parameter. If the count of any of the above parameters exceeds the capacity of a specific register, then the system pegs the register at the maximum value. The register reinitializes at the end of the data-collection interval after storing the data in the system memory.

### Data Reporting (DS3PM/TABS Option)

The DACS IV-2000 provides six parameters for reporting to the General Telemetry Processor (GTP) via the TABS links for both the near-end and far-end of the monitored C-bit formatted DS3 paths. These parameters are:

- Data Missing Indicator — when 0, indicates valid near-end or far-end performance-monitoring data. The other five parameters for this path were successfully calculated for the complete measurement interval. When 1, indicates invalid near-end or far-end performance-monitoring data, as occurs when a DS3 port is provisioned during a measurement interval and cannot be monitored for the entire interval. This parameter also can be set to 1 (for the far-end only) if a near-end OOF second occurred during the measurement interval, because the far-end parameter cannot be updated when the incoming signal is an error. An OOF event occurs when 3 out of 16 F-bit errors are received or when two errored M-bit patterns out of 4 M frames are received.
- Number of Detected Errors Counter — reflects the total near-end bit error (NEBE) or far-end bit error (FEBE) count for the measurement interval. Its final value does not exceed 563,880 ±5%, which is calculated by multiplying the maximum bit error counts per second (9,398 ±5%) by the number of seconds in the measurement interval (60).

  The near-end counter is set to 0 at the beginning of each measurement interval and is incremented by the contents of the NEBE counter at the end of each second. During AIS conditions, the NEBE counter is obtained from C-BITS in the incoming DS3 signal. During OOF and LOC conditions, the NEBE counter increments at its maximum rate.

  The far-end counter is set to 0 at the beginning of each measurement interval and is incremented by the contents of the FEBE counter at the end of each second, except that it is not incremented for a second during which a near-end OOF second occurs.

- OOF Seconds — includes a count and a status flag. The count is 0 at the beginning of each measurement interval and is incremented once every second for the near-end, if the near-end OOFAIS latch was set during that second. The counter is incremented every second for the far-end, if the following are true:
  - — The far-end OOFAIS (X-bit) latch is set, meaning that an OOF, LOS, or AIS condition occurred in the far-end processor's signal and was flagged using X-bit signaling
  - — The near-end OOFAIS latch is not set.

  The final value for this parameter does not exceed 60. The status flag reflects the state of the far-end OOFAIS (X-bit) latch after the last second in the measurement interval.
- Type A Errored Seconds Counter — gives the number of seconds during which one and only one error has occurred. This counter is 0 at the beginning of each measurement interval, and the final value does not exceed 60. This counter is incremented once after each second if the following are true:
  - — The OOFAIS latch is not set
  - — The BE counter equals 1
  - — For far-end only, the near-end OOFAIS latch is not set.
- Type B Errored Seconds Counter — gives the number of seconds during which errors have occurred but at an error rate of less than $10^{-6}$. The counter is 0 at the beginning of each measurement interval, and the final value does not exceed 60. It is incremented once after each second if the following are true:
  - — The OOFAIS latch is not set
  - — The BE counter is greater than 1 and less than or equal to 44
  - — For far-end only, the near-end OOFAIS latch is not set.
- Type C Errored Seconds Counter — reflects the number of seconds during the measurement interval that the near-end path was partially unusable (an error rate greater than $10^{-6}$). The final value of this parameter does not exceed 60. The counter is 0 at the beginning of each measurement interval and is incremented once after each second if the following are true:
  - — The OOFAIS latch is set
  - — The BE counter exceeds 44
  - — For far-end only, the near-end OOFAIS latch is not set.

## STS-1 and VT1.5 Performance Monitoring

The DACS IV-2000 provides SONET performance-monitoring capabilities for intermediate points on the STS-1 and VT1.5 paths as well as at termination points. In this way, the DACS IV-2000 provides a centralized point for monitoring the health of the SONET network.

For the VT1.5 path, near-end performance monitoring is provided by counting the Bit Interleaved Parity-2 (BIP-2) coding violations using V5 bits 1-2. From these counts, the DACS IV-2000 derives the VT1.5 PM parameters (Table 2-13).

For the STS-1 path, the DACS IV-2000 provides both near-end and far-end performance monitoring. Near-end STS-1 performance monitoring is accomplished by counting the BIP-8 coding violations using the B3 byte. These counts are used to derive the STS path performance monitoring parameters. The far-end parameters are derived by counting the FEBEs using bits 1 through 4 of the G1 byte.

In its implementation of the SONET networking feature, the DACS IV-2000 extends its performance-monitoring capabilities of asynchronous signals to SONET signals. Performance-monitoring thresholds in the DACS IV-2000 are selectable on a per-parameter, per-channel basis. TCA messages are generated when thresholds are reached. Performance-monitoring reports are available on both scheduled or demand basis. For the SONET signals, the DACS IV-2000 stores 15-minute bins for up to 8 hours, and performance-monitoring totals for the current and previous day.

**NOTE:**
If an SMUX circuit pack is removed or fails, all stored STS-1 and/or VT1.5 performance-monitoring data is lost.

### Monitored Parameters

This section lists the performance monitoring parameters.

The DACS IV-2000 monitors and reports section, line, and path-performance parameters to verify that service quality objectives specified in terms of these parameters are being met. Performance monitoring only occurs during available time because service-quality assessments cannot be determined during a period of service outage. From a service perspective, two important criteria must be verified:

- Availability of service, which is measured by the parameter Unavailable Seconds (UAS)
- Quality of service during available time, which is measured by the other performance-monitoring parameters.

Table 2-13. **STS-1/ VT1.5 PM Parameters**

| Monitored Parameter | | STS-1 | | | VT1.5 |
|---|---|---|---|---|---|
| | | Section | Line | Path | Path |
| Near-End | SEFS | ✓ | - | - | - |
| | LOSS | ✓ | - | - | - |
| | CV | - | ✓ | ✓ | ✓ |
| | ES | - | ✓ | ✓ | ✓ |
| | ESA | - | ✓ | ✓ | ✓ |
| | ESB | - | ✓ | ✓ | ✓ |
| | SES | - | ✓ | ✓ | ✓ |
| | AISS | - | ✓ | - | - |
| | ALS | - | - | ✓ | ✓ |
| | UAS | - | ✓ | ✓ | ✓ |
| Far-End | CV | - | - | ✓ | - |
| | ES | - | - | ✓ | - |
| | ESA | - | - | ✓ | - |
| | ESB | - | - | ✓ | - |
| | SES | - | - | ✓ | - |
| | UAS | - | - | ✓ | - |

Note: ✓ denotes monitoring is supported.

### Near-End Section Parameters

The following are the STS-1 section performance-monitoring parameters specified by the ANSI T1M1.3 requirements:

- Severely Errored Framing Seconds (SEFS) — The count of 1-second intervals containing one or more OOF events.
- Loss of Signal Seconds (LOSS) — The count of 1-second intervals containing one or more LOS defects. An LOS defect is the occurrence of no transitions on the incoming STS-1 signal (before descrambling) for a time period between 2.3 µs and 100 µs. The LOS defect is terminated after a 125-µs interval during which the LOS defect entry criteria is not met.

STS-1 section performance-monitoring parameter thresholds can be set for the current 15-minute interval and for the current day. Their default values for the given time interval are shown in Table 2-14.

**Near-End Line Parameters**

The following are the STS-1 line performance-monitoring parameters specified by the ANSI T1M1.3 requirements:

- Coding Violations (CV) — The count of the BIP errors detected at the line layer of the incoming STS-1 signal. The CV counter is incremented for each BIP error detected. That is, each line BIP-8 can detect up to eight errors per STS-1 frame, with each error incrementing the CV counter. CVs for the line layer are collected using the BIP-8s in the B2 byte located in the line overhead of each STS-1 signal.
- Errored Seconds (ES) — A count of 1-second intervals during which one or more CV or AIS defect occurred.
- Errored Seconds Type A (ESA) — A count of 1-second intervals during which exactly one line CV and no AIS defects occurred.
- Errored Seconds Type B (ESB) — A count of 1-second intervals during which more than one but less than the number of line CVs that cause an SES (the number of line CVs is set by the **SET-TH-NE** command, system default is 12, allowable range is 1 to 55) and no AIS defects occurred.
- Severely Errored Seconds (SES) — A count of 1-second intervals during which the number of line CVs set by the **SET-TH-NE** command is met or exceeded or during which one or more AIS defects occurred.
- Alarm Indication Signal Seconds (AISS) — A count of 1-second intervals containing one or more AIS defects. An AIS defect is the occurrence of a 111 pattern in bits 6, 7, and 8 of the K2 byte in five contiguous STS-1 frames. The AIS defect terminates when bits 6, 7, and 8 of the K2 byte do not contain the 111 pattern for five contiguous STS-1 frames.
- Unavailable Seconds (UAS) — measure the duration for which service is unavailable. The line is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, with no failure present, the line becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the line is unavailable.

STS-1 line performance-monitoring parameter thresholds can be set for the current 15-minute interval and for the current day. Default values for the given time intervals are shown in Table 2-14.

### Near-End STS-1 Path Parameters

The following are the STS-1 path performance-monitoring parameters specified by the ANSI T1M1.3 requirements:

- Coding Violations (CV) — The count of the BIP errors detected at the path layer of the incoming STS-1 signal. The CV counter is incremented for each BIP error detected. CVs for the path layer are collected using the BIP-8 in the B3 byte located in the path overhead of each STS-1 signal.
- Errored Seconds (ES) — A count of 1-second intervals during which one or more path CVs, AIS, or LOP defects occurred.
- Errored Seconds Type A (ESA) — A count of 1-second intervals during which exactly one path CV and no AIS or LOP defects occurred.
- Errored Seconds Type B (ESB) — A count of 1-second intervals during which more than one but less than the number of path CVs that cause a SES (the number of path CVs is set by the **SET-TH-NE** command [system default is 9, allowable range is 1 to 55]) occurred and no AIS defects occurred.
- Severely Errored Seconds (SES) — A count of 1-second intervals during which the number of path CVs set by the **SET-TH-NE** command is met or exceeded or during which one or more AIS defects occurred.
- Alarm Indication Signal/Loss of Pointer Seconds (ALS) — A count of 1-second intervals containing one or more AIS or LOP defects. An STS path AIS defect is the occurrence of all ones in bytes H1 and H2 in three contiguous STS-1 frames. The STS path AIS defect terminates when a valid STS pointer is detected with the New Data Flag (NDF) set to 1001 (inverted) for one frame or 0110 (normal) for three contiguous STS-1 frames. An LOP defect occurs when either a valid pointer is not detected in eight consecutive frames, or when eight consecutive frames are detected with the NDF set to 1001 without a valid concatenation indicator. The LOP defect is terminated when either a valid pointer with a normal NDF (set to 0110) or a valid concatenation indicator is detected for three contiguous frames.
- Unavailable Seconds (UAS) — measure the duration for which service is unavailable. The path is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, with no failure present, the path becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the path is unavailable.

STS-1 path performance-monitoring parameter thresholds can be set for the current 15-minute interval and for the current day. Default values for the given time intervals are shown in Table 2-14.

Table 2-14. STS-1 PM Thresholds

| Parameter Name | Accumulation Interval | | | |
|---|---|---|---|---|
| | 15 Minutes | | Day | |
| | Default | Range | Default | Range |
| **Section Performance-Monitoring Parameters (Near-End)** | | | | |
| SEFS | 10 | 0-900 | 100 | 0-86400 |
| LOSS | 10 | 0-900 | 100 | 0-86400 |
| **Path and Line Performance-Monitoring Parameters (Near-End)** | | | | |
| CV | 4666 | 0-46660 | 447900 | 0-4479000 |
| ES | 65 | 0-900 | 648 | 0-86400 |
| ESA | 65 | 0-900 | 648 | 0-86400 |
| ESB | 65 | 0-900 | 648 | 0-86400 |
| SES | 10 | 0-900 | 100 | 0-86400 |
| AISS (line only) | 10 | 0-900 | 100 | 0-86400 |
| ALS (path only) | 10 | 0-900 | 100 | 0-86400 |
| UAS | 10 | 0-900 | 100 | 0-86400 |
| **Path Performance-Monitoring Parameters (Far-End)** | | | | |
| CV | 4666 | 0-46660 | 447900 | 0-4479000 |
| ES | 65 | 0-900 | 648 | 0-86400 |
| ESA | 65 | 0-900 | 648 | 0-86400 |
| ESB | 65 | 0-900 | 648 | 0-86400 |
| SES | 10 | 0-900 | 100 | 0-86400 |
| UAS | 10 | 0-900 | 100 | 0-86400 |

### Far-End STS-1 Path Parameters

For valid far-end monitoring, far-end parameters are derived during 1-second intervals that contain no near-end LOP or AIS defects. For 1-second intervals that do contain near-end LOP or AIS defects, all far-end parameters are set to zero and the invalid data flag is raised. The far-end STS-1 path layer performance is conveyed back to the near-end STS-1 Path Terminating Equipment (PTE) through the path status (G1) byte. Bits 1 through 4 provide a STS-1 path FEBE indication and convey the count of interleaved bit blocks that have been detected in error by the path BIP-8 (byte B3) code. The STS-1 yellow alarm signal conveys the occurrence of AIS or LOP defects detected at the near-end.

Far-end STS-1 path parameters are derived from the STS-1 path FEBE indication and yellow alarm signal and are similar to STS-1 path performance parameters defined for the near-end STS-1 path.

When these thresholds are reached, a corresponding TCA message is generated. These thresholds are modifiable, and if you do not specify a threshold crossing level, the DACS IV-2000 assumes the default value for that parameter. If the count of any of the parameters in Table 2-14 exceeds the capacity of a specific register, the system pegs the register at the maximum value. The register reinitializes at the end of the data collection interval after storing the data in memory.

### Near-End VT1.5 Path Parameters

The following are the VT1.5 path performance-monitoring parameters specified by the ANSI T1M1.3 requirements:

- Coding Violations (CV) 1ecThe count of the BIP errors detected at the path layer of the incoming VT1.5 signal. The CV counter is incremented for each BIP error detected. CVs for the path layer are collected using the BIP-2 in the V5 overhead byte of the floating VT.
- Errored Seconds (ES) — A count of 1-second intervals during which one or more path CVs, AIS, or LOP defects occurred.
- Errored Seconds Type A (ESA) — A count of 1-second intervals during which exactly one path CV and no AIS or LOP defects occurred.
- Errored Seconds Type B (ESB) — A count of 1-second intervals during which more than one but less than the number of path CVs that cause a SES occurred and no AIS or LOP defects occurred. The number of path CVs is set by the **SET-TH-NE** command. System default is 4, allowable range is 1 to 20.
- Severely Errored Seconds (SES) — A count of 1-second intervals during which the number of path CVs set by the **SET-TH-NE** command is met or exceeded or during which one or more AIS or LOP defects occurred.

- Alarm Indication Signal/Loss of Pointer Seconds (ALS) — A count of 1-second intervals containing one or more AIS or LOP defects. An AIS defect is the occurrence of all ones in bytes V1 and V2 in three contiguous VT superframes. The AIS defect terminates when a valid VT pointer with a valid VT size is detected with the New Data Flag (NDF) set to 1001 (inverted) for one VT superframe, or 0110 (normal) for three contiguous VT superframes. An LOP defect occur when either a valid pointer is not detected in eight consecutive VT superframes, or when eight consecutive VT superframes are detected with the NDF set to 1001 without a valid concatenation indicator. The LOP defect is terminated when either a valid pointer with a normal NDF (set to 0110), or a valid concatenation indicator is detected for three contiguous VT superframes.
- Unavailable Seconds (UAS) — measure the duration for which service is unavailable. The path is unavailable from the onset of 10 contiguous SESs, or the onset of the condition leading to a failure. Once unavailable, with no failure present, the path becomes available at the onset of 10 contiguous seconds with no SESs. This parameter is the only parameter counted when the path is unavailable.

VT1.5 path performance-monitoring parameters have settable thresholds for current 15-minute interval and for the current day. The default values and ranges are shown in Table 2-15.

Table 2-15. VT1.5 PM Threshold

| Parameter Name | Accumulation Interval | | | |
|---|---|---|---|---|
| | 15 Min | | Day | |
| | Default | Range | Default | Range |
| CV | 156 | 0-16383 | 14930 | 0-1048575 |
| ES | 65 | 0-900 | 648 | 0-86400 |
| ESA | 65 | 0-900 | 648 | 0-86400 |
| ESB | 65 | 0-900 | 648 | 0-86400 |
| SES | 10 | 0-900 | 100 | 0-86400 |
| ALS | 10 | 0-900 | 100 | 0-86400 |
| UAS | 10 | 0-900 | 10 | 0-86400 |

When the thresholds are reached, a corresponding TCA message is generated. These thresholds are modifiable, and if you do not specify a threshold crossing level, the DACS IV-2000 assumes the default value for that parameter. If the count of any of the parameters in Table 2-15 exceeds the capacity of a specific register, the system pegs the register at the maximum value. The register reinitializes at the end of the data collection interval after storing the data in memory.

## Redundant Controller

The DACS IV-2000 is provided with two control complexes, which maximize control availability and reliability by providing redundancy in the critical parts of the Main Controller and autonomous recovery from controller failures. The following sections describe additional features provided with the Redundant Controller (RC) Module.

### Administrative Links

Two ECI circuit packs are provided, allowing for twelve administrative links (six per ECI circuit pack). The ECI circuit packs can provide administrative link redundancy by establishing separate links to critical operating systems from each ECI. The links are identified as CILINK-1-1 through CILINK-1-6 and CILINK 2-1 through CILINK 2-6.

### Redundant Power

Duplicated power circuit packs provide redundant power to the Redundant Controller Module circuit packs, thereby increasing reliability.

## Nonvolatile Backup Memory

The two hard disks are the primary (PRI) nonvolatile backup memory devices for the DACS IV-2000. All database changes are automatically recorded on the disks. A removable read/write optical disk is used to download new software and perform periodic, scheduled system database backups.

The DACS IV-2000 provides an option to enable automatic database backups from the primary backup medium to the secondary medium. Automatic database backups can be scheduled to execute once in a 24-hour period on selected days or on every day of the week. The disk database can also be manually backed up to the secondary disk.

## Alarm Reporting

The DACS IV-2000 provides three levels of alarms: critical, major, and minor.

- A critical alarm indicates a severe, service-affecting condition.
- A major alarm indicates a service-affecting failure, main or unit controller failure, or power supply failure.
- A minor alarm indicates an abnormal condition that is not service-affecting.

Alarms are reported in three places: in the central office (office alarms), in the remote maintenance center (remote alarms), and on the circuit packs (circuit pack alarms). The three types of alarms are described below.

### Office Alarms

The DACS IV-2000 provides the following local office alarm outputs:

- Critical audible
- Critical visual
- Major audible
- Major visual
- Minor audible
- Minor visual
- Main controller failure (processor major) visual.

Local status indicators are provided on the status panel. Detailed alarm information is provided over administrative links. Software-controlled alarms can be delayed to suppress spurious alarms. (The delay is programmable from 1 to 30 seconds.)

The alarm level of incoming DS1, DS3, and EC-1 facility failures can be changed on a per-port basis to major, minor, or no alarm.

Serial alarm, scan, and control (AS&C) telemetry points and parallel alarm closures are provided by the system.

An alarm cutoff (ACO) for turning off the audible alarms is provided both on the status panel and at a remote location (Table 2-16). Contact closures for visual alarms remain on until the condition causing the alarm is corrected.

## Remote Alarms

The DACS IV-2000 provides four remote alarms: critical, major, minor, and processor major, with local status indicators on the status panel circuit pack. Detailed alarm information is provided over administrative links. Software-controlled alarms can be delayed in order to suppress spurious alarms. (The delay is programmable from 1 to 30 seconds.).

Table 2-16. **DACS IV-2000 Alarm Indications/Switches**

| Indicators/Switches | Frame | Office | | |
|---|---|---|---|---|
| | Status Panel | Audible | Visual | Remote |
| CRITICAL indicator | X | X | X | X |
| MAJOR indicator | X | X | X | X |
| MINOR indicator | X | X | X | X |
| FAILURE (main controller failure) indicator | X | | X | X |
| ACO indicator | X | | | |
| ACO switch | X | | | X |
| Remote ID (active whenever CRITICAL, MAJOR, MINOR, or FAILURE alarm indicators are active) indicator | | | | X |

**Note:** ABNORMAL and FAR END are reserved for future use

The alarm level of incoming DS1, DS3, and EC-1 facility failures to major, minor, or no alarm can be changed on a per-port basis. The default alarm level for DS1 facilities is no alarm. The default alarm level for DS3 and EC-1 facilities is major.

AS&C telemetry points and parallel alarm closures and remote reset are provided by the system. The AS&C points are collected by a telemetry remote in the local office and transmitted to the appropriate operations system (OS).

## Circuit Pack Alarms

All circuit packs, except version 1 Synchronizer and BXA circuit packs, contain a red LED to aid in trouble isolation. Some circuit packs also contain a green LED to indicate that the circuit pack is active. The LED is mounted so that it is visible while the circuit pack is plugged into the equipment. The power supply circuit packs activate their respective red LEDs when a fault exists, and, because the LEDs are powered from the primary power supply, they light even if logic level power is lost. An alarm indication message is generated for each circuit pack failure.

The Synchronizer Module is a fully duplex module with each synchronizer side comprising three circuit packs: DS1TX (DS1 timing extractor), TBS3 (stratum 3 time base oscillator), and DPLL (digital phase lock loop). Each version 2 circuit pack has a green LED and a red LED.

- The red LED (labeled ALM) indicates circuit pack failures. The red LED on any synchronizer module circuit pack (DPLL, DS1TX, and TBS3) lights continuously while the circuit pack is in a failed condition.
  - — The red LED remains lit for the duration of the failure or two seconds, whichever is longer.
  - — The red LED on the DS1TX circuit pack blinks (1 second on, 1 second off) continuously when a reference failure exists on either timing link. The blinking starts immediately upon failure detection and continue as long as the reference failure exists. The blinking stops as soon as the failure is cleared and the reference is declared valid.
- The green LED (labeled ACT) indicates whether the circuit pack is active.
  - — For the DPLL and TBS3 circuit packs, the green LED remains lit while the circuit pack is active; that is, the circuit pack is on the active SYNC side. It is extinguished if the circuit pack is not active.
  - — For the DS1TX circuit pack, the green LED remains lit while the circuit pack is active; that is, the circuit pack is on the active SYNC side and the SYNC is either in normal or fast mode. It is extinguished if the circuit pack is not active.

**NOTE:**
Whenever the red LED on any synchronizer circuit pack is lit because of any circuit pack failure, the green LED on that circuit pack is extinguished and the circuit pack is removed from service.

## Alarm Conditions and Associated Alarm Levels

Table 2-17 shows alarm condition types and their associated definition for the DACS IV-2000 equipment and facility alarms. Table 2-18 lists the facility and equipment and alarm levels associated with a specific alarm condition.

Table 2-17. **Alarm Conditions**

| Alarm Condition Type | Definition |
|---|---|
| ACPWR | Indicates AC Power Failure detected |
| AIS | Indicates Alarm Indication Signal detected |
| AISFRAMED | Indicates a framed Alarm Indication Signal detected |
| AISL | Indicates Line Alarm Indication Signal detected |
| AISP | Indicates Path Alarm Indication Signal detected |
| AISUNFRAMED | Indicates an unframed Alarm Indication Signal detected |
| ALLDS2SOOF | Indicates all DS2s in a DS3 signal are out of frame |
| ALLREFFAIL | Indicates failure of all synchronizer timing references. |
| BKUPMEMS | Indicates backup to secondary nonvolatile memory failure detected. |
| COM | Indicates a common equipment failure detected |
| CONTBUS | Indicates control bus failure detected |
| DS1-AIS | Indicates DS1 Alarm Indication Signal detected |
| DS1IF | Indicates DS1 Interface equipment failure detected |
| DS3FRMTMISMATCH | Indicates DS3 Format Mismatch detected |
| DTLCH | Indicates Data Latch Error detected |
| EOR | Indicates End-of-Range Error detected |
| EXJIT | Indicates Excessive Jitter detected |
| EXPHR | Indicates Excessive Phase Error detected |

Table continued on next page.

Table 2-17. Alarm Conditions (Continued)

| Alarm Condition Type | Definition |
|---|---|
| EXTERR | Indicates error detected external to the DACS IV-2000 |
| FERF | Indicates Far End Receive Failure detected |
| FRD | Indicates security violation has occurred |
| FRQOF | Indicates Frequency Offset Error detected |
| FSNLN | Indicates Frequency Synthesizer Loss of Energy detected |
| FSTO | Indicates PLL Fast Start Time-out detected |
| ICTLR | Indicates Interrupt Controller Error detected |
| IDLE | Indicates Idle signal detected |
| IHRER | Indicates Interrupt Holding Register Error detected |
| IMPROPBLK | Indicates Improper blank circuit pack detected |
| IMPROPRMVL | Indicates Improper removal detected |
| INC | Indicates Incoming DS3 or DS1 failure detected |
| INHSWPR | Indicates Switch to protection equipment inhibited |
| INHSWWKG | Indicates Switch to working equipment inhibited |
| INT | Indicates Internal hardware fault or failure detected |
| LERDF | Indicates Line Error Detector Failure detected |
| LOF | Indicates Loss of frame detected |
| LOP | Indicates Loss of pointer detected |
| LOS | Indicates Loss of signal detected (equipment) |
| LSSIG | Indicates Loss of signal detected (facility) |
| MAN | Indicates Manually removed from service |
| MINC | Indicates Multiple Incoming detected |
| MUX | Indicates Multiplex equipment failure detected |

Table continued on next page.

Table 2-17. **Alarm Conditions (Continued)**

| Alarm Condition Type | Definition |
|---|---|
| OOF | Indicates Out of Frame detected |
| PFLCH | Indicates Phase/Frequency Readable Output Latch Error detected |
| PHSTP | Indicates Phase Step Error detected |
| PSHLN | Indicates Phase Shifter Output Loss of Energy detected |
| RAMER | Indicates RAM Error detected |
| ROMER | Indicates ROM Error detected |
| RTV | Indicates Real-time Violation detected |
| SBITFAIL | Indicates SBIT communications protocol Failure indicating that the far end is not responding to (acknowledging) near end SBIT protocol communication |
| SLMF | Indicates Signal Label Match Failure detected |
| SYNCCLK0 | Indicates detected failure is in Side 0 Clock Hardware |
| SYNCCLK1 | Indicates detected failure is in Side 1 Clock Hardware |
| SYNCFRNG | Indicates synchronizer has made a transition into free-running mode |
| SYNCFST | Indicates synchronizer has made a transition into fast-start mode |
| SYNCHLDOVR | Indicates synchronizer has made a transition into holdover mode |
| SYPLN | Indicates Sync Pulse Generator Loss of Energy detected |
| TBCOLD | Indicates Time Base Oven Cold |
| TBIOER | Indicates Time Base Communication Error detected |

Table continued on next page.

Table 2-17. **Alarm Conditions (Continued)**

| Alarm Condition Type | Definition |
|---|---|
| TBLEN | Indicates Time Base Strobe Loss of Energy detected |
| TBNDF | Indicates Time Base Strobe Energy Detector Failure detected |
| TODC | Indicates Time-of-Day Clock |
| T-BER | Indicates Bit Error Rate threshold exceeded |
| T-BERL | Indicates Line Bit Error Rate threshold exceeded |
| TRBER | Indicates High Bit-Error Rate on a Synchronization Timing Reference detected |
| TRMNBER | Indicates Minor Bit-Error Rate on a Synchronization Timing Reference detected |
| URTER | Indicates UART Error detected |
| X1LEN | Indicates Loss of Energy on 1 ms Synchronizer Crosscouple detected |
| X3LEN | Indicates Loss of Energy on 30 ms Synchronizer Crosscouple detected |
| XCOOL | Indicates Synchronizer Cross-couple Out-of-Lock Error detected |
| XCRTV | Indicates Synchronizer Cross-couple Real-time Violation Error detected |
| XCSUM | Indicates Synchronizer Cross-couple Summary Error detected |
| XFLRG | Indicates Synchronizer Cross-couple Fast Lock Range Error detected |
| XFQOF | Indicates Synchronizer Cross-couple Frequency Offset Error detected |
| XLKDN | Indicates Synchronizer Cross-couple Communication Link Error detected |
| YEL | Indicates Carrier Group Alarm, Yellow, incoming direction detected |

Table 2-18. **Alarms Associated With Equipment and Facilities**

| Entity | Alarm Condition Types | Alarm Levels |
|---|---|---|
| EC-1 Facilities | AISL, AISP, FERF, LOF, LOP, LOS, SLMF, T+BERL, YEL | MJ, MN, NA |
| T1 Facilities | Near-End: DS1-AIS, LOS, LSSIG, T+BER, YEL | MJ, MN, NA |
| | Far-End: INC, MINC | |
| T2 Facilities | Near-End: OOF | MJ, MN, NA |
| | Far-End: OOF | |
| T3 Facilities | Near-End: AIS (MUX1), AISFRAMED (MUX2), AISUNFRAMED (MUX2), ALLDS2SOOF (MUX2), DS3FRMTMISMATCH, IDLE, LSSIG, OOF, T+BER | MJ, MN, NA |
| | Far-End (MUX2): AIS, IDLE, INC, OOF, SBITFAIL, YEL | |
| VT1.5 Facilities | AISP, LOP, YEL | MJ, MN, NA |
| CLKDR1 | IMPROPRMVL, INT | MJ, MN |
| CLKGN3 | IMPROPRMVL, INT | MJ, MN |
| CPU2 | INT, MAN | MJ, MN, FAILURE |
| DPLL1/DPLL2 | DTLCH, EOR, EXPHR, FSNLN, FSTO, ICTLR, IHRER, INT, MAN, PFLCH, PSHLN, ROMER, RAMER, RTV, SYPLN, TBLEN, URTER, X1LEN, X3LEN, XCOOL, XCRTV, XCSUM, XFLRG, XFQOF, XLKDN | MJ |
| DS1IF1 | IMPROPBLK, IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| DS1IP1 | IMPROPRMVL, INT | MJ, MN |
| DS1RY1 | IMPROPRMVL, INT | MJ, MN |
| DS1TX1/ DS1TX2 | EXJIT, FRQOF, INT, LERDF, LOS, MAN, OOF, PHSTP, TBLEN, TBNDF | MJ, MN |
| DS3PM1 | INT, MAN | MN |

Table continued on next page.

Table 2-18. **Alarms Associated With Equipment and Facilities (Continued)**

| Entity | Alarm Condition Types | Alarm Levels |
|---|---|---|
| ECI3 | INT, MAN, TODC | MN |
| Fan Assembly | INT | MJ, MN |
| MTC3 | INT, MAN | INT, MAN |
| MUX1/MUX2 | Near-End: IMPROPBLK, IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| | Far-End (MUX2): ACPWR, COM, DS1IF, MUX | MJ, MN, NA |
| MUXP1/ MUXP2 | IMPROPRMVL, INT | MJ, MN |
| MUXPS1 | IMPROPRMVL, INT | MJ, MN |
| PMGR1 | IMPROPRMVL, INT | MN |
| PRI5 | INT, MAN | MJ, MN, FAILURE |
| PWRA | IMPROPRMVL, INT | MJ |
| PWRE1/ PWRE2/ PWRE3 | IMPROPRMVL, INT | MJ |
| PWRF | IMPROPRMVL, INT | MJ |
| PWRG | IMPROPRMVL, INT | MJ |
| SCI2 | INT, MAN | MJ, MN, FAILURE |
| SEC5 | INT, MAN | MN |
| SMUX1 | IMPROPBLK, IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| SMUXP1 | IMPROPRMVL, INT | MJ, MN |
| SSC5 | INT, MAN | MJ, MN, FAILURE |
| SWCS2 | IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |

Table continued on next page.

Table 2-18. Alarms Associated With Equipment and Facilities (Continued)

| Entity | Alarm Condition Types | Alarm Levels |
|---|---|---|
| SWIF1/SWIF2 | IMPROPBLK, IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| SWIO1 | IMPROPRMVL, INHSWPR, INHSWWKG, INT | MJ, MN |
| SYNCN | ALLREFFAIL,SYNCFRNG, SYNCFST, SYNCHLDOVR, SYNCPRI, SYNCSEC | MJ, MN |
| SYNCPRI | EXJIT, FRQOF, LOS, OOF, PHSTP | MJ, MN |
| SYNCSEC | EXJIT, FRQOF, LOS, OOF, PHSTP | MJ, MN |
| TBS31/TBS32 | FRQOF, INT, MAN, TBCOLD, TBLEN, TBIOER | MJ |
| UC2 | INT, MAN | MJ |
| UI2 | INT, MAN | MJ, FAILURE |

## Multiple Alarm Processing

This feature improves the correlation and readability of alarm report messages and enhances system performance. The Multiple Alarm Processing and Reporting feature collects multiple alarms that occur within one second into a single alarm message. This reduces system overhead, and makes alarm messages easier to read and interpret.

## RTRV-ALM-ALL Command

The **RTRV-ALM-ALL** command can be used to retrieve the active near-end T1, T2, T3, VT1.5, and EC-1 facility alarms, equipment alarms, and link alarms. The output message also indicates if the frame is in critical alarm.

## Alarm Clear Messages

For each alarm condition reported, a message is sent when the alarm is cleared regardless of any other active condition on the same report.

The DACS IV-2000 software provides a clear delay capability that specifies the length of time following a condition that has cleared before the associated alarm point is cleared and an alarm clear message is issued to indicate the cleared condition. The clear delay time is provisionable from 1 to 20 seconds. The alarm is cleared if the condition clears and remains cleared for the provisioned clear delay time.

## CB-149 Alarm Compliance

The DACS IV-2000 software provides a clear delay capability that specifies the length of time from the time a condition clears until the associated alarm point is cleared and a message is issued to indicate the cleared condition. The clear delay time is provisionable from 1 to 20 seconds. The alarm is cleared if the condition clears and remains clear for the provisioned clear delay time.

## Deny Manual Unit Controller Removal

You cannot manually request removal of a unit controller (UC) from service if any interface circuit pack in that unit is protected. Denying the removal of the UC when an interface circuit pack is protected prevents the interface circuit pack from being unprotected under certain situations.

## Supported Operations Systems

The DACS IV-2000 provides for communications with various Bellcore and AT&T Operations Systems (Figure 2-27). The DACS IV-2000 command message set complies with the current Bellcore TL1 specifications. This message set allows for communicating with Bellcore Operations System/Intelligent Network Element (OPS/INE) and Network Monitoring Analysis (NMA).

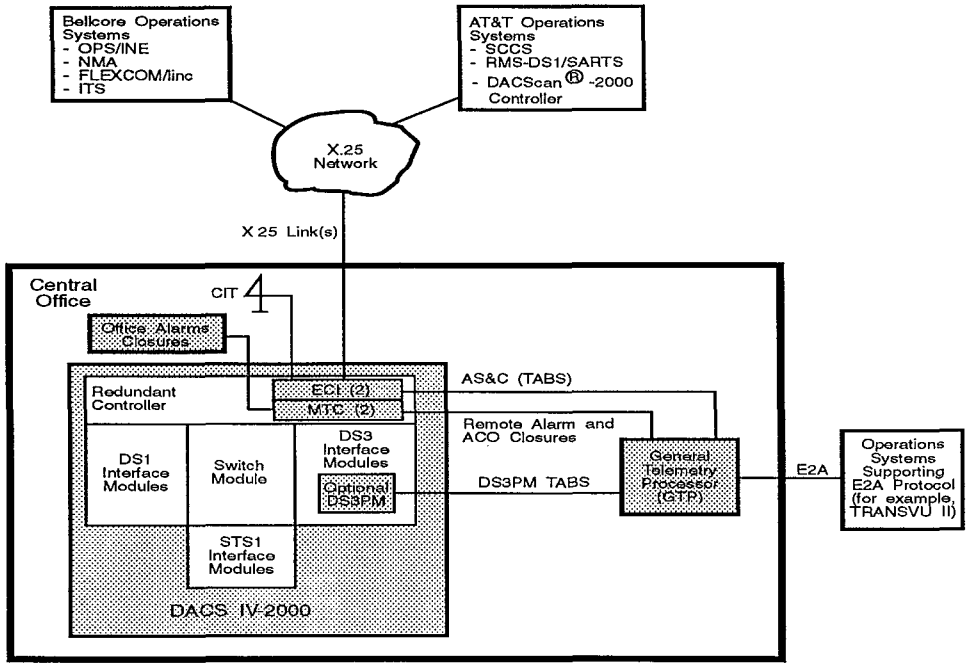



Figure 2-27. Supported Operations Systems

## Bellcore Operations Systems

The DACS IV-2000 can communicate with the following Bellcore Operations Systems (OSs):

- Facility and Equipment Planning System (FEPS) is used by capacity planners to plan equipment and facility usage and to forecast demand for new equipment and facilities.
- Trunks Integrated Record Keeping System (TIRKS) maintains a data-base of equipment and facilities in the interoffice network to design end-to-end circuits for service provisioning.
- Operations System/Intelligent Network Element (OPS/INE) implements cross-connects in the DACS IV-2000 based on information received from the provisioning system.
- Network Monitoring Analysis (NMA) collects alarms and performance-monitoring data from the DACS IV-2000.
- FLEXCOM/linc supports end-customer control of the DACS IV-2000.
- Integrated Test System (ITS) supports facility testing.

The interface to OPS/INE and NMA is through X.25 links to Bellcore's Operations Communications System (OCS).

In addition to the alarm data from the DACS IV-2000 that are sent to a central OS through TL1 messages, the remote MUX capabilities of the DACS IV-2000 support the communication of alarm data from a DDM-1000 (or any vendor's M13 multiplexer meeting Bellcore TR-TSY-000009 or ANSI T1.107 specifications) to an alarm monitoring OS such as NMA. Because of this capability, direct communication links to the remote M13 for alarm data are not required.

In order for the DACS IV-2000 Release 4.0 to interface with current Bellcore OSs and for full support of the Release 4.0 features, the following releases (or later) of the NMA, OPS/INE, and TIRKS software should be used:

NMA - Release 4.2
OPS/INE - Release 1.9
TIRKS - Release 16.2

## AT&T Operations Systems

The DACS IV-2000 can communicate with the following AT&T Operations Systems:

- DACScan®-2000 controller automates control over diversely located network elements, such as the DACS III-2000 and DACS IV-2000.
- Remote Measuring System-DS1/Switched Access Remote Testing System (RMS-DS1/SARTS) provides remote testing, executes access commands, and provides performance monitoring (on demand) by the DACS IV-2000.
- Switching Control Center System (SCCS) provides management and surveillance of network elements.
- Total Network Management (TNM) provides management and surveillance of network elements. TNM is a migration of the existing SCCS architecture to the AT&T Star Server® FT Release 2 fault-tolerant computer platform.

In order for the DACS IV-2000 to interface with current AT&T OSs and for full support of the current DACS IV-2000 features, the following releases (or later) of the DACScan-2000 Controller, RMS-DS1/SARTS, and SCCS/TNM software should be used:

DACScan-2000 Controller - Release 5.2 (available June 1995)
RMS-DS1/SARTS - Release 5.0.1.6
SCCS - Release 13.3
TNM - Release 4.0

## User and OS Interfaces

The user and OS interfaces of the DACS IV-2000 are used in the operations, administration, maintenance, and provisioning of the system. The interfaces are described in Chapter 4, "User Interfaces."

## Security

The DACS IV-2000 provides a security feature that offers secured access to the Main Controller (MC). This feature includes login and password protection, manual logout, and super-user access to administer logins for MC access. The super user can restrict the access of other users to only that subset of commands they need to do their job. For example, technicians I who only need to perform various system queries can be assigned user logins that restrict them from executing potentially service-affecting commands.

### Security Audit

To help system administrators determine if the security of the system has been compromised, the DACS IV-2000 provides a security audit feature to maintain a record of the following security-related events:

- User logins and all autonomous and manual user logouts
- Login creations, deletions, and changes
- Failed login attempts that result in a link lockout
- Input commands issued by a user with the incorrect security level
- Changes of the system time or date
- Edit link security parameters
- Delete security audit records.

The audit log maintains the most recent 100 security related events in nonvolatile memory.

## Message Screening

Five message screening values can be provisioned on a per-link and a per-user basis. When logged into a link, the user value has precedence over the link value. The five message screening values are:

- INPUT — specifies that the user or link receives responses to its own input commands.
- AUTO — specifies that the user or link receives responses to its own input commands and to autonomous messages except for report database change messages due to manual command input.
- ALL — specifies that the user or link receives responses to its own input commands, to autonomous messages except for report database change messages due to manual command input, and to responses to input commands from other users.
- DBAUTO — specifies that the user or link receives responses to its own input commands and to autonomous messages including report database change messages due to manual command input.
- DBALL — specifies that the user or link receives responses to its own input commands, to autonomous messages including report database change messages due to manual command input, and to input commands from other users.

## User Priority Levels

Super users can assign a priority level to a user's login so that commands entered by that user are processed according to the priority level assigned. When commands are entered over the administrative link, the software places each command in a queue. This allows the processor to execute each command one at a time. If a number of commands are in the queue, the processor executes them according to the priority assigned to the user who entered the command.

The five user priority levels are defined as 1 to 5, with 5 being the highest priority level. For example, if the queue contains three commands with the first two entered by a user with a priority level of 3 and the last command entered by a user with a priority of 4, then the processor executes the last command first. If two commands have the same priority, then the processor executes the commands in the order received. This feature is useful in circumstances that require immediate processing of commands, such as enabling cross-connections for restoration.

## Command Verification

The DACS IV-2000 has a command verification feature that reduces the chance of error. The software displays a warning message and requires a confirmation before allowing the processor to execute commands that can affect service or prevent access to the system for extended periods of time. After receiving the warning message, you have the option to modify, cancel, or execute the command. The system administrator can disable this feature for specified user logins, allowing the OS to operate unimpeded by command reviews and warning messages.

The expanded command verification warning messages also inform you when the execution of a `CPY-MEM` option takes longer than 10 minutes.

## X.25 Links

The DACS IV-2000 supports the X.25 Packet Assembler and Disassembler (PAD) and provides an X.25 Clear-to-Send detection.

### X.25 Packet Assembler and Disassembler

Using an external Packet Assembler and Disassembler, an X.25 link can be converted into multiple asynchronous terminal interfaces. The PAD can be used to connect asynchronous terminals to the system for local operation, or to modems for remote (networking) operation (see Figure 2-28). The recommended PAD is a MICOM® box Type 2 X.25 asynchronous PAD.

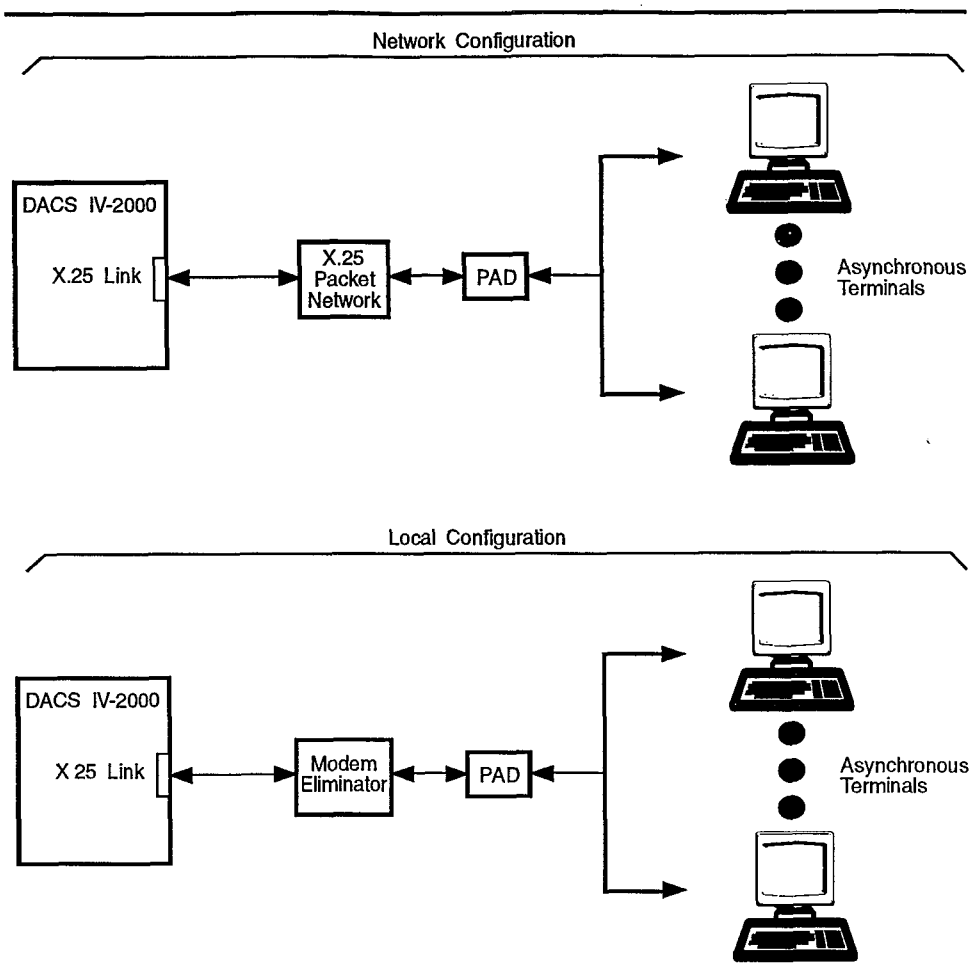



Figure 2-28. X.25 PAD Applications

## X.25 Flow Control

With the X.25 flow control feature, commands are never dropped because of full input buffers if the OSs have been suitably coded. Without the X.25 flow control feature, the DACS IV-2000 can not accept commands when the input buffers are full; it drops commands and sends back the input acknowledgment `RL` (retry later). With X.25 flow control, the DACS IV-2000 stops acknowledging X.25 commands when the input buffers are full. By not acknowledging commands, back pressure is applied through the X.25 network and stops the sending system from transmitting commands until the DACS IV-2000 is ready to accept them again.

## Input Command Routing

This feature allows input commands and acknowledgment codes from any administrative link at the DACS IV-2000 frame to be echoed to a specified link. Input commands and acknowledgment codes are echoed through autonomous messages (REPT LOCL IN). The following commands support this feature:

- **ACT-ECHO-LINK** activates echoing of input commands from the specified link to another link.
- **CANC-ECHO-LINK** cancels the echoing of input commands from the specified link to another link.
- **RTRV-ECHO-LINK** retrieves the status of echoing of input commands for the specified link.

## Facility Maintenance

Facility maintenance consists of monitoring incoming DS1, DS3, and STS-1 signals; generating alarms and messages when failures are detected; and auditing system security. Facility maintenance features provided by the DACS IV-2000 are described in this section.

### Application of Special Signals

The DACS IV-2000 automatically supplies a DS1, VT1.5, or STS-1 idle signal to the output ports to drive facilities through the switch. If all 28 DS1 tributaries in a DS3 are idle, the system can be provisioned to transmit a DS3 idle signal on the output port. When an incoming signal failure condition is detected at an input port of the switch, a DS1, VT1.5, or STS-1 AIS is supplied to the corresponding output port to replace the failed signal.

The DACS IV-2000 can be provisioned to provide a DS1 test signal supplied by an external test generator, such as a QRSS. One of the DACS IV-2000 DS1 ports must be connected to this generator. A command given to the system, using the broadcast capability of the switch matrix, makes this signal available to any outgoing DS1 port (DS1 or DS3 interface circuit pack). The QRSS can be substituted for normal DS1 data (via user command) when needed for test purposes.

The DACS IV-2000 can insert two special signals onto a specified outgoing facility without taking down the established cross-connection. This feature can be used for verification of facility routing or for testing. The two signals that can be applied are an idle (AIS) signal (unframed all ones) or a DS1 test signal from the external signal generator.

## DS3 AIS and IDLE Signals

If a DS3 facility fails before getting to an upstream network element (such as a DACS III-2000), that network element sends an alarm indication signal (AIS) over the facility to the DACS IV-2000. The AIS inhibits the DACS IV-2000 from generating misleading facility alarms and activates status indications along the path of the DS3 facility. Similarly, if a facility fails coming into the system, the system transmits an AIS to the next network element downstream.

A network element upstream (such as a DACS III-2000) supplies a DS3 idle signal on the DS3 facility if no other signal is connected to the facility at the network element. For example, a DS3 facility can be connected to an incoming port on the DACS IV-2000 coming from a DACS III-2000.

The DACS IV-2000 monitors incoming DS3 ports for DS3 AIS and idle signal. If the DACS IV-2000 detects either of these conditions, the software does the following:

- Inhibits incoming signal failure alarms
- Provides status indications through serial telemetry and over administrative links that indicate detection of AIS or Idle signals
- If AIS, indicates the type of DS3 AIS format.The system can detect two different formats of AIS. Bellcore TR-TSY-000191 specifies that DS3 AIS have valid DS3 framing, information bits set to a repeating `1010` pattern. An alternate CCITT DS3 AIS format specifies an unframed, all-ones signal.

For DS3 facilities requiring any of these capabilities, the MUX2 and MUXP2 circuit packs, respectively, must be used. For DS3 Interface-32 Modules, you must also use Unit Controller 2 (UC2) and Power E3 (PWRE3) circuit packs.

## DS1/DS3 AIS Signals

The DACS IV-2000 automatically supplies a DS1 idle signal (unframed all ones) to any output port that is not cross-connected through the DS1 switch (A DS1 idle signal is identical to a DS1 AIS signal). If all 28 DS1 tributaries in a DS3 are idle, the system can be provisioned to transmit a DS3 idle signal on the output port. If an incoming signal failure is detected at an input port of the DS1 switch, a DS1 (idle) AIS is supplied to the corresponding output port to replace the failed signal. The detection of signal loss, out-of-frame, or AIS on an incoming DS3 facility causes activation of DS1 AIS on all DS1 tributaries in the DS3 signal.

## Alarm Indication Signals

Alarm indication signals are generated to alert downstream equipment that a failure has been detected on upstream equipment. Refer to Bellcore TR-NWT-000253 for information on STS-1and VT1.5 signal formats. The following Alarm Indication Signal (AIS) indications are generated by the DACS IV-2000:

- STS-1 AIS Line (AISL) — is generated by section terminating equipment to alert the downstream line terminating equipment that a failure has been detected upstream when an AISL failure state on an incoming STS-1 signal is detected for five consecutive frames. AISL is detected as an all ones pattern in bits 6-8 of byte K2 of the STS-1 signal. The DACS IV-2000 only detects AISLs but does not generate AISLs.
- STS-1 AIS Path (AISP) — is generated by line terminating equipment to alert the downstream STS-1 path terminating equipment that a failure has been detected upstream. AISP is generated by setting bytes H1, H2, H3, and the entire STS-1 SPE to all ones.
- VT1.5 AIS Path (AISP) — is generated to alert the downstream VT1.5 path terminating equipment that a failure has been detected upstream when:
  - STS-1(VT1.5) signal — an LOS, LOF, AISL, STS-1 LOP, or STS-1 AISP failure state on an incoming STS-1(VT1.5) signal occurs. An VT1.5 AISP is generated in the downstream direction of all associated VT1.5(cc-SPE) tributaries.
  - VT1.5(cc-SPE) signal — a VT1.5 LOP failure state on any VT1.5(cc-SPE) tributary on an incoming STS-1(VT1.5) signal occurs.

  A VT1.5 AISP is generated by setting bytes V1-V4 and the entire VT1.5 SPE to ones.
- DS1 AIS (DS1, DS3, or STS1 interface) —unframed all-ones signal generated in the downstream direction caused by an upstream equipment failure.
  - DS1 interface — when a LOS or AIS failure state is entered on any associated incoming DS1 signal
  - DS3 interface — when a LOS or AIS failure state is entered on any associated DS1 tributary of an incoming DS3 signal
  - STS1 interface — when a VT1.5 LOP or VT1.5 AISP failure state is entered on any VT1.5(DS1) tributary of an incoming STS-1(VT1.5) signal.

### Yellow Signals

Yellow signals are sent by DS1/STS-1/VT1.5 path-terminating equipment to alert upstream DS1/STS-1/VT1.5 path-terminating equipment that a failure or AIS along the path has been detected and alarmed by the downstream DS1/STS-1/VT1.5 path terminating equipment. The STS-1 yellow signal is indicated by bit 5 of the G1 byte being set to 1. The VT1.5 yellow signal is indicated by bit 8 of the V5 byte being set to 1.

DS1 yellow alarm signals are detected and reported by the DACS IV-2000 on all ports provisioned to support DS1 performance monitoring. STS-1 and VT1.5 yellow alarm signals are detected and reported when received from upstream equipment.

### DS1 Quasi-Random Signals

The DACS IV-2000 can be provisioned to provide an outgoing DS1 signal supplied by an external signal generator. This signal can be quasi-random or another signal pattern. One of the DS1 ports must be connected to the external generator. A command given to the system (using the broadcast capability of the DACS IV-2000 switch matrix) makes this signal available to any outgoing DS1 port. The signal from the external generator is transmitted from all DS1 output ports that are provisioned with an output mode of `QRSS`.

## Facility Failure Detection

DS1, DS3, and STS1 ports are monitored for LOS and for BERs that exceed a user-selectable threshold of $10^{-3}$ through $10^{-9}$, (programmable on a per-port basis). DS3 ports are also monitored for the out-of-frame (OOF) condition. STS1 ports are also monitored for Loss of Frame (LOF), Loss of Pointer (LOP), Section Coding Violation (CV), Line CV, STS-1 Path CV, and VT1.5 Path CV. The STS-1 and VT1.5 Path CVs are gathered for performance monitoring only, and no maintenance signals are generated based on them.

BER is determined as follows:

- DS1 signals — by checking BPVs
- DS3 signals — by checking BPV or parity violations (your option)
- STS-1 signals — by checking bit interleaved parity (BIP).

The occurrence of any facility failure is indicated by a system alarm (Critical, Major, Minor, or no alarm, as provisioned); the appropriate facility failure reports over the administrative links; and a flashing LED on the interface circuit pack associated with the incoming signal.

### DS3 Mismatch Detection

Each DS3 port is provisioned for either an M13 or a C-Bit Parity signal type. In previous software releases, when a signal that was not in the provisioned format was received on a port, the DACS IV-2000 generated an alarm. The invalid signal was indicated by either one or more DS2 Out of Frame (DS2OOF) or All DS2 Out of Frame (ALLDS2OOF) alarms. With the DS3 Mismatch Detection feature, the system reports the invalid signal, identifies the source of the problem, and indicates that the invalid DS3 signal is due to a C-Bit Parity/M13 format mismatch. This feature requires that Multiplexer 2 (MUX2) circuit packs be installed in the DS3 interface module.

### Input Port Status

The input port status is provisioned in the DACS IV-2000 to mark all input ports as:

- Driven — a good signal is expected and an alarm occurs if the signal is bad.
- Not driven — no valid signal is expected at the port, and the port is not monitored for failures. If the port is formatted, Performance Monitoring data is accumulated.
- Initialized — the port is considered non-driven until a valid signal is detected, and, when a valid signal is received, status automatically changes to driven.
- QRSS — the DS1 signal is provisioned as the QRSS source for the system.

### Per-Frame Database Change Report

This feature allows the system to report database changes on a per-frame basis. This feature is provisionable at the frame level.

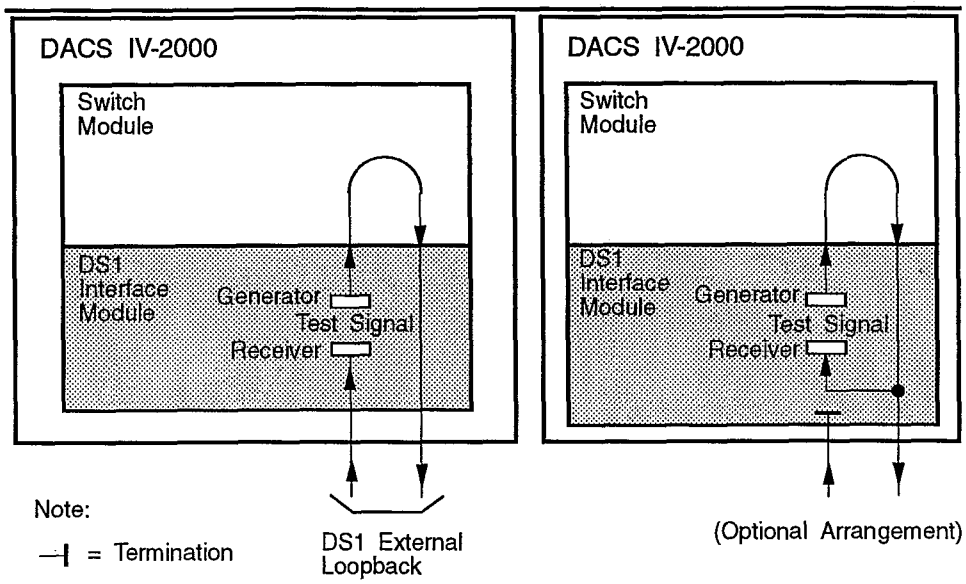
### Port Information Retrieval

The DACS IV-2000 provides a parameter for use when retrieving the status of provisioned ports. Ports are selectable that transmit normal signals, or transmit idle signals, or transmit AIS signals, or transmit a signal from an external DS1 generator.

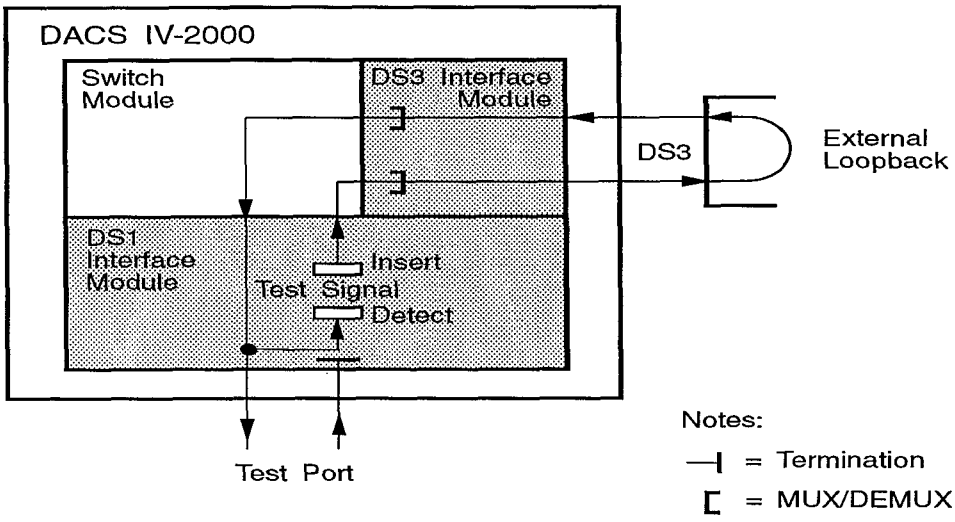
### Automated Facility Turnup Test

Built-in test signal generators and receivers in the DS1 Interface circuit paths can be used during facility turnup to test facility continuity. A new facility is looped back at the far end, a test signal is applied at the DS1 signal rate, and the presence of the looped-back signal is verified by the test receiver. The system must be equipped with a DS1 Interface Module to have this capability. DS1 and DS3 facilities can be tested, but DS3 facilities are tested as 28 DS1s on an individual

DS1 basis. Figure 2-29 provides examples of the automated facility turnup test. For additional information, refer to the section titled "External Cables" in Chapter 15 of the *DACS IV-2000 (256) Release 4.0 Operations and Maintenance* manual (AT&T 365-340-701).




**A. Automated Loopback Transmission Test on a DS1 Port**




**B. Automated Loopback Transmission Test on a DS3 Port**

Figure 2-29. **Automated Facility Turnup Test**

## Remote Multiplex Communication

The Remote Multiplex Communication feature enables the DACS IV-2000 to communicate with far-end multiplexers (that is, a DDM-1000 or any M13 multiplexer meeting the TR-TSY-000009 or ANSI TI.107 specifications) by using the DS3 overhead bits. This feature allows the following actions:

- Far-end loopback control
- Response to far-end loopback commands
- Signaling of alarm conditions to the far-end
- Generation of alarm/status messages on far-end conditions.

This feature supports the following protocols for communications with multiplexers at the far end of the DS3 facilities:

- DS3 X-bit signaling that indicates far-end DS3 alarm conditions
- DS2 X-bit signaling that indicates far-end DS2 out-of-frame condition
- DS1 loopback control using the DS2 C-bits as specified in Bellcore TR-TSY-000009 (**TR9** value used in **ED-T3** command)
- C-bit parity format far-end alarm and control link for control of DS1 and DS3 loopbacks and reporting of far-end facility and equipment alarm conditions (FEAC) as specified by ANSI T1.107a -1989 (**FEAC** value used in **ED-T3** command)
- S-bit (DS3 stuff bit) communications link used by AT&T DDM-1000 multiplexers for DS1 loopback operations and reporting equipment and facility failure conditions at the far and near ends (**SBIT** value used in **ED-T3** command).

Functions and protocols are specified on a per-port basis. This allows the DACS IV-2000 to match the capabilities of the far-end multiplexers.

For DS3 facilities requiring the remote multiplex communication feature, MUX2 and MUXP2 circuit packs are required. The **ED-T3** command is used to provision MUX2 circuit packs for use with the different remote multiplexer types (TR9, FEAC, or SBIT). In addition, the **SET-ATTR-EQPT**, **SET-ATTR-T1**, **SET-ATTR-T2**, and **SET-ATTR-T3** commands are used to set alarm notification levels associated with far-end equipment and facilities.

### DS3 X-Bit Signaling

The DS3 X-bits, when provisioning a MUX2 circuit pack for remote multiplexers, allow for the following communications functions:

- Transmit to the far-end equipment that the MUX2 circuit pack has detected a DS3 yellow alarm condition (LOF or AIS). The DACS IV-2000 issues a near-end `REPT ALM T3` message, indicating the DACS IV-2000 detected the LOF or AIS condition.

- Issue a REPT ALM T3 message with the condition type YEL when the MUX2 circuit pack has received indication of a DS3 yellow alarm condition from the far-end equipment.

### DS2 X-Bit Signaling

The DS2 X-bits, when provisioning a MUX2 circuit pack for remote multiplexers, allow for the following communications functions:

- Transmit to the far-end equipment that the MUX2 circuit pack has detected a DS2 OOF facility condition. The DACS IV-2000 issues a near-end REPT ALM T2 message, indicating the DACS IV-2000 detected the OOF condition.
- Issue a REPT ALM T2 message with the condition type OOF when the MUX2 circuit pack has received indication of a far-end DS2 OOF condition from the far-end equipment.

### TR9 Type Remote Multiplexers

Provisioning a MUX2 circuit pack for TR9 remote multiplexers allows for the following communications functions:

- Receive far-end requests to establish or release DS1 tributary loopbacks. A REPT DBCHG message is issued when the DACS IV-2000 establishes or releases a loopback due to a remote request.
- If a MUX2 circuit pack is not transmitting a DS3 Idle signal, request the far-end equipment to establish or release DS1 tributary loopbacks. Test equipment can be used to determine if the far-end equipment has established or released a loopback requested by the DACS IV-2000.

### FEAC Type Remote Multiplexers

Provisioning a MUX2 circuit pack for FEAC remote multiplexers allows for the following communications functions:

- Receive far-end requests (via 16-bit operation and object code words) to establish or release DS1 tributary loopbacks (1 or all 28 associated with the MUX2 circuit pack) or DS3 line loopbacks. A REPT DBCHG message is issued when the DACS IV-2000 establishes or releases a loopback due to a remote request.
- Request the far-end equipment (via generation of 16-bit operation and object code words) to establish or release DS1 tributary loopbacks (1 or all 28 loopbacks associated with the MUX2 circuit pack) or DS3 line loopbacks.

- Transmit to the far-end equipment (via generation of 16-bit operation code-word) that the DACS IV-2000 has detected an equipment or a facility failure. The alarm is declared on the DACS IV-2000 before being transmitted to the far-end. The following failures are reported to the far-end:
  - — Service-affecting DS3 equipment failures — diagnostic audit failures of DS3 hardware
  - — DS3 LOS or T+BER — failure condition received on incoming DS3 signal of MUX2 circuit pack communicating with the far end
  - — DS3 OOF, AIS, or IDLE received — conditions received (also includes DS2 OOF) on incoming DS3 signal of MUX2 circuit pack communicating with the far-end
  - — Non-service-affecting DS3 equipment failures — failure condition on MUX2 circuit pack communication with the far end
  - — Non-service-affecting common equipment failures — failure to SWIO, SWCS, CLKGN, PWRE, CLKDR, UC, SMUX, MUXP2, SWIF, or DS1IF circuit packs associated with the path of the MUX2 circuit pack communicating with the far-end
- Issue a `REPT ALM EQPT`, `REPT ALM T1`, `REPT ALM T2`, or `REPT ALM T3` message indicating a far-end equipment or facility failure has been received (via 16-bit operation code word) by the MUX2 circuit pack from the far-end. The follow alarm conditions are reported by the DACS IV-2000:
  - — MUX — indicates failures associated with far-end DS3 hardware equipment
  - — DS1IF — indicates failures associated with far-end DS1 hardware equipment
  - — COM — indicates failures associated with far-end equipment other than the DS3 hardware within the path of the DS3 signal
  - — AIS — indicates a DS3 AIS signal is received by the far end
  - — IDLE — indicates a DS3 IDLE signal is received by the far end
  - — INC — indicates a single DS1 LOS or T+BER signal is received by the far-end
  - — MINC — indicates multiple DS1 LOS and/or T+BER signals are received by the far end
  - — OOF — indicates DS3 or DS2 OOF condition is received by the far end

### SBIT Type Remote Multiplexers

Provisioning a MUX2 circuit pack for SBIT remote multiplexers allows for the following communications functions:

- Issue a `REPT ALM T3` with the alarm condition SBITFAIL when far-end high-speed acknowledgment packets are not received in response to far-end high-speed request packets. During an SBITFAIL condition, requests for operate or release far-end loopbacks are denied.
- Receive far-end requests to establish or release DS1 tributary loopbacks (1 or all 28 associated with the MUX2 circuit pack) or DS3 line loopbacks. A `REPT DBCHG` message is issued when the DACS IV-2000 establishes or releases a loopback due to a remote request.
- Request the far-end equipment to establish or release DS1 tributary loopbacks (1 or all 28 loopbacks associated with the MUX2 circuit pack). The far-end equipment acknowledges if the loopback is established or denied. If denied, the DACS IV-2000 issues a `REPT EVT T1` message with the condition type `DENYDS1LPCK`.
- Transmit to the far-end equipment that the DACS IV-2000 has detected an equipment or a facility failure. The alarm is declared on the DACS IV-2000 before being transmitted to the far-end. The following failures are reported to the far-end:
  - — Service-affecting DS3 equipment failures — diagnostic audit failures of DS3 hardware
  - — DS3 LOS or T+BER — failure condition received on incoming DS3 signal of MUX2 circuit pack communicating with the far end
  - — DS3 OOF, AIS, or IDLE received — conditions received (also includes DS2 OOF) on incoming DS3 signal of MUX2 circuit pack communicating with the far end
  - — Non-service-affecting DS3 equipment failures — failure condition on MUX2 circuit pack communication with the far end
  - — Non-service-affecting common equipment failures — failure to SWIO, SWCS, CLKGN, PWRE, CLKDR, UC, SMUX, MUXP2, SWIF, or DS1IF circuit packs associated with the path of the MUX2 circuit pack communicating with the far end

- Issue a `REPT ALM EQPT`, `REPT ALM T1`, `REPT ALM T2`, or `REPT ALM T3` message indicating a far-end equipment or facility failure has been received (via 16-bit operation code word) by the MUX2 circuit pack from the far-end. The follow alarm conditions are reported by the DACS IV-2000:
  - ACPWR — indicates the AC power feed in an unmanned loop cabinet has failed, and the far end is operating on backup battery power.
  - MUX — indicates non-service-affecting failures associated with far-end DS3 hardware equipment (for example, MUXR or ELIU of a DDM-1000)
  - DS1IF — indicates service or non-service-affecting failures associated with far-end DS1 hardware equipment (for example, a DS1 circuit pack of a DDM-1000)
  - COM — indicates non-service-affecting failures associated with far-end equipment other than the DS3 hardware within the path of the DS3 signal (for example, power, controller, telemetry circuit pack or a fan on a DDM-1000)
  - AIS — indicates a DS3 AIS signal is received by the far end. This is indicated by all seven DS2 signals being OOF.
  - IDLE — indicates a DS3 IDLE signal is received by the far end
  - INC — indicates a single DS1 LOS or T+BER signal is received by the far end
  - MINC — indicates multiple DS1 LOS and/or T+BER signals are received by the far end
  - OOF — indicates DS3 LOS or T+BER condition is received by the far end.

## Frame Maintenance

The features and capabilities of the frame maintenance mechanism are described in this section.

### Incorrect Secondary Disk Load Message

When an attempt is made to copy the database from secondary disk to primary disk, system identifiers (system type, system release, and TID) are compared to the system identifiers in memory (WKG). A warning message is generated if the identifiers differ, and the database transfer is not completed.

### AS&C Activation on Secondary Disk Failures

This feature facilitates remote operations by providing an Alarm, Surveillance, and Control (AS&C) point, which is activated whenever a `CPY-MEM` request to the secondary disk (SEC) fails. These failures may not be confined to failures of the secondary disk. The alarm points are held active until the DACS IV-2000 is polled at CILINK 1-4, or CILINK 2-4. After being polled, the alarm points are cleared. In addition, if a `REPT BKUP` message is issued with the status parameter set to `FAIL`, the AS&C points are set.

### Empty Primary Database Check

An empty database is defined as a database with no units provisioned, but otherwise correct. If the frame is instructed to boot a database with this characteristic, the boot fails and the MC is placed in the OOS-MCOND state. A failure message indicates the nature of the failure. (The state of the MC can be changed to IS, if necessary, after a successful boot.)

### Disk Verification

This feature automatically verifies and checks the system's ability to access the primary hard disks and the secondary optical disk at least once every fifteen minutes. This process detects and reports disk access failures.

### Fault Isolation and Reporting

The DACS IV-2000 can isolate a fault to the incoming facility or equipment. In the case of an equipment failure, the DACS IV-2000 identifies the failed circuit pack by lighting a red LED on the faceplate and generating alarms and administrative link messages.

### Protection Switching

The DACS IV-2000 automatically restores transmission upon detection of a service-affecting equipment failure by switching to a protection circuit pack within 60 ms.

### Fan Filter Replacement Indication

This feature provides a periodic autonomous message alerting you that the fan filter in the Switch Bay needs to be replaced. An autonomous message is generated when the recommended replacement period of 91 days has expired. The message must be acknowledged manually.

## Fan Assembly

Fan assemblies are provided in the Switch Bay and STS1/DS3 Interface Bays. The fan assemblies are used to cool the equipment modules. Each fan assembly consists of three horizontally mounted fans with a filter, and control switches and indicators. You must keep the air intake (under the assembly) free of obstructions and replace the fan filter on a routine basis. An autonomous message (`REPT FAN FILTER`) is generated (after the recommended filter replacement interval of 91 days has occurred) to remind you that the fan filter needs to be replaced. In addition, fan assemblies ED-9C130-30,G1 and ED-9C130-30,G2, causes the DACS IV-2000 to generate an alarm for a clogged filter condition (a minor FILTER alarm LED on the fan assembly turns on) and when sensing high preset temperature values. The `REPT FAN FILTER` message can be disabled if the system does not contain an ED-2C816-30,G1 or ED-2C906-30 fan assembly.

## BNC Connectors

The DACS IV-2000 can be equipped with BNC connectors that allow connections to DS3 and STS-1 facilities. BNC connector panels can be ordered with STS1/DS3/DS1, DS3, or STS1/DS3 Interface Bays. The BNC connector panel is provided as part of the electromagnetic compatibility (EMC) enclosure to meet the FCC Class A criteria for EMC, but can be provided optionally without the enclosure.

Advantages of the BNC connectors are:

- The coaxial connections are collected in a single place at a convenient and consistent location.
- A quick, positive connection/disconnection is provided.
- Risks are reduced when handling coaxial lines, since they are kept from the backplane areas.
- A more robust connection is available.
- The coaxial splice is eliminated because the 734A and 735A cables can be brought directly to the frame. The need to downsize to a smaller diameter is eliminated.
- Cable routing and precabling are facilitated. Cables can be pulled from either end with less risk, and if necessary, can be trimmed and re-terminated easily. This minimizes the excess slack problem.
- Standard industry-wide hardware is available, and such items as connectors, tools, and cabling, can be stocked as necessary.

### EMC Enclosures

When fitted with the optional EMC enclosures, the DACS IV-2000 meets the EMC FCC criteria and the electrostatic discharge (ESD) requirements specified in Bellcore TR-NWT-001089.

**NOTE:**
Enclosures must be ordered with any new frame and cannot be field retro-fitted.

With the EMC option to help eliminate electromagnetic interference, the entire front of the DACS IV-2000 is covered with EMC doors. Because of this, the visual alarm indicators are only visible when looked at straight on. However, the EMC enclosure provides a Header Designation Assembly (HDA) at the top the Switch Bay to house duplicate alarm indicators so they are fully visible to technicians (see section "EMC Enclosure Header Alarm Indicators" in Chapter 4).

## Protection Switching Operations

Protection switching does not take place when the main controller is out of service.

### Protection Groups

The DACS IV-2000 architecture divides the circuit packs associated with signal transmission (interfaces and switch matrix) into a number of protection groups. A single failure within a protection group is protected, but additional failures within a single protection group are not protected. Multiple failures occurring in multiple protection groups are protected independently within the individual protection groups.

### Interface Protection Groups

A DS3 interface protection group consists of a DS3 Interface Module (either a DS3 Interface-32 or DS3 Interface-16 Module). The protectable circuit pack in a DS3 interface protection group is the MUX circuit pack, which supports one DS3 facility. Each DS3 Interface-32 Module has 32 MUX equipment locations, with 31 of these locations used for service and one used for protection, giving a protection ratio of 1 to 31. Each DS3 Interface-16 Module has 16 MUX equipment locations, with 15 of these locations used for service and one used for protection, giving a protection ratio of 1 to 15.

A DS1 interface protection group consists of all the DS1 Interface Modules within the same bay. The protectable circuit pack in a DS1 interface protection group is a set of three circuit packs, two DS1IF circuit packs and a SWIF circuit pack, which in combination, support 28 DS1 facilities. Each DS1 Interface Module supports eight sets of these circuit packs. An STS1/DS3/DS1 Interface Bay has two DS1 Interface Modules. One DS1 Interface Module uses all eight sets of circuit packs for service. The second DS1 Interface Module uses seven sets of circuit packs for

service and one set for protection, thereby providing a 1 to 15 protection ratio. A DS1 Interface Bay has four DS1 Interface Modules. Three use all eight sets of circuit packs for service. The fourth uses seven sets for service and one for protection, thereby providing a 1 to 31 protection ratio.

An STS-1 interface protection group consists of an STS-1 Interface-16 Module. The protectable circuit pack in a STS-1 interface protection group is the SMUX circuit pack, which supports one STS-1 facility. Each STS1 Interface-16 Module has 16 SMUX equipment locations, with 15 of these locations used for service and one used for protection, giving a protection ratio of 1 to 15.

### Failures Within Interface Protection Groups

In an interface protection group, there is a single protection circuit pack and a single protection bus available, so only one protection switch can be performed at a time in that protection group. When a MUX, DS1IF, SWIF, or SMUX circuit pack is protected, relays on the circuit pack are used to switch traffic onto the protection bus, which reroutes the DS3, DS1, or STS-1 signals from that circuit pack to the protection circuit pack. This routing is alternatively performed by contacts on the backplane when a MUX, DS1IF, or SMUX circuit pack is removed from the slot. In order to maintain protection bus continuity, BXA circuit packs must be equipped in unprovisioned slots that are not equipped with MUX, DS1IF, SWIF, or SMUX circuit packs to provide correct protection bus operation.

When you pull a MUX, DS1IF, SWIF, or SMUX circuit pack, protection of another circuit pack in the same protection group can be dropped. In the case of a DS3, or STS-1 interface protection group, it depends on whether the first circuit pack is failed or extracted and the positions in which the circuit packs reside, as to whether or not the pulled circuit pack is protected. In the case of a DS1 interface protection group, no protection is provided until this situation is corrected.

### Failures Between Interface Protection Groups

The DACS IV-2000 protects a single failure in each interface protection group independently of failures in other interface protection groups.

### Switch Protection Group

The switch protection group consists of the SWIO and SWCS circuit packs in the Switch Module, and the associated CLKDR circuit packs in the interface modules. The protectable circuit pack in the switch protection group is either a SWIO/ CLKDR circuit pack combination or a SWCS circuit pack. There are 32 SWIO circuit packs, with each circuit pack used to half capacity under normal conditions. The SWIO circuit packs operate in pairs. When a SWIO is protected, its mate circuit pack uses spare capacity to assume the load of the protected circuit pack. There are also 32 SWCS circuit packs, but only 31 are needed to provide a nonblocking switch under normal conditions, with the 32nd circuit pack available to protect the others, giving a 1 to 31 protection ratio. Only one SWIO or SWCS

circuit pack can be protected at any given time (refer to the following section titled "Failures Within Switch Protection Group" for more information).

The CLKDR circuit packs in the DS1, DS3, or STS-1 Interface Modules are used to distribute clock from the SWIO circuit packs to the DS1, DS3, or STS-1 interface circuit packs. The failure of a CLKDR circuit pack, therefore, is treated by the system as if the associated SWIO circuit pack failed. Consequently, the switch protection group is extended to include the CLKDR circuit packs in the modules.

### Failures Within Switch Protection Group

When a SWIO or CLKDR circuit pack fails, it is protected by its mate circuit pack; for example, if SWIO-1 fails, SWIO-2 protects the signals to SWIO-1 and the CLKDR associated with SWIO-2 assumes the signals for the CLKDR associated with SWIO-1. In order to support the additional load that is switched onto the mate circuit pack, additional paths through the switch matrix are utilized, and these are provided by the spare 32nd SWCS circuit pack. The need for these paths precludes protecting multiple SWIO or SWCS circuit packs at the same time.

### Failures Between Switch and Interface Protection Groups

Protection switching in the switch protection group requires remapping connections (as many as 448 for a single circuit pack failure). To perform this within the required time interval, the system maintains prestored maps that are used to protect failures of SWIO and SWCS circuit packs. These prestored maps are updated whenever connections in the switch matrix are changed.

The DACS IV-2000 allows for protection of the switch while one or more interface protection groups are protected. It also allows for protection of one or more interface protection groups while the switch is protected. Due to the prestored map recalculations associated with protection switching, there can be a brief period of time after the protection of an interface group before the switch group can be protected.

### Operational Guidelines

The following operational guidelines must be followed:

- All unprovisioned DS1IF, MUX, and SMUX slots in an interface bay are equipped with a circuit pack, either an unused DS1IF, MUX, or SMUX circuit pack, or a BXA circuit pack.
- Do not pull unprotected circuit packs carrying traffic from the system.
- Never pull more than one failed circuit pack from one protection group.
- All failures in a protection group should be repaired before performing other maintenance activities in that group.

## System Operation Under Protection

The DACS IV-2000 allows for cross-connections, disconnections, test access, loopback functions, and changes to the output mode on all circuit packs while they are protected.

## Automatic Protection Switching

The DACS IV-2000 circuit packs do not protection switch automatically unless they are carrying traffic. This applies to DS1IF, SWIF, MUX, SMUX, and SWIO circuit packs, but it does not apply to SWCS circuit packs (because these circuit packs are not associated with specific facilities and because 31 of 32 center stage circuit packs must be available at all times to guarantee nonblocking).

## Manual Protection Switch

Using the manual protection switch command of either `SW-TOPROTN-EQPT` or `SW-TOWKG-EQPT` always locks the circuit pack in the state (protected or unprotected) to which it is switched. The result is equivalent to issuing an inhibit command (`INH-SW-EQPT`) while in the unprotected or protected state.

If a circuit pack is locked in the protected state, the command `SW-TOWKG-EQPT` causes the circuit pack to switch back to the working state and locks the circuit pack in this state. Therefore, the circuit pack is not subsequently in protection if a failure occurs.

To have the circuit pack revert to the unlocked working state, the `ALW-SW-EQPT` command should be used, which releases the lock and, if the circuit pack is good, automatically switches back to working. The `SW-TOPROTN-EQPT` command can be used on a circuit pack whether or not it is carrying traffic.

## LED for Manual Protection Switch

To aid in identifying a circuit pack that has been manually switched to protection, this feature lights the red ALM LED on the interface or switch circuit pack (SWIF, MUX, SWIO, SMUX, or SWCS) when the circuit pack has been manually switched to protection. This is a provisionable feature.

When a manual protection switch has been performed, the red ALM LED on the circuit pack that was switched to protection is constantly lit for the duration of the protection switch. The output response to the command that was used to manually switch the circuit pack to protection contains a warning message that the red ALM LED on the protected circuit pack is lit as a result of this operation.

## Autolock

A protectable circuit pack cycles through the following states in the protection switching process (assuming no manual locking occurs):

- good/working
- bad/working
- good/protected
- bad/protected.

Normally, the circuit pack is in the good/working state. When a failure occurs, the circuit pack transitions to bad/working. If protection switching is available, the circuit pack transitions to bad/protected. When the problem clears, the circuit pack transitions to good/protected, which is a transient state that is passed through as the circuit pack unprotects and returns to good/working. The state names associated with these four states are:

- ACT = good/working
- ACT-*xxx* = where *xxx* is one of the bad substates: FLT, ABS, BLK, TSTF, or FEF
- OOS-*xxx* = where *xxx* is one of the bad substates: FLT, ABS, BLK, TSTF, or FEF.

The autolock state protects against frequent cycling through the four states due to an intermittent problem. A circuit pack is put into the autolock state when it goes through this cycle *n* times within an *m*-minute period. All autolocks are autonomously released every *x* hours by the system. The values *n*, *m*, and *x* are user provisionable; the default (system initialization) values are:

*n* = 4 times

*m* = 10 minutes

*x* = 24 hours.

Autolock is automatically removed whenever the system is reset or whenever the *n*, *m*, or *x* value is changed; or it can be removed manually by command.

When a circuit pack is in the autolock state, the modifier, ERRANAL, is appended to its state name.

## Automatic Restoration of Circuit Packs

When a failed circuit pack is replaced, it is automatically returned to service if it passes all system diagnostic tests. This feature applies to all circuit packs except the redundant controller, synchronizer, and DS3PM circuit packs.

The UC and DS3PM circuit packs are automatically restored when the system is reset. The system may be reset by pushing the RESET button, issuing an initialization command, or performing a power-on restart.

# Hardware

# 3

## Contents

# Contents

# Hardware

# 3

The DACS IV-2000 hardware comprises one Switch Bay and from one to eight interface bays (containing DS1, DS3, and/or STS-1 Interface Modules). Each module consists of an equipment shelf and its associated circuit packs.

The switch contained in the DACS IV-2000 can accept 7168 input signals. However, 224 paths into the switch are from protection circuit packs, thus limiting the switch to 6944 traffic-carrying signals. A fully equipped system is capable of making 3472 two-way DS1 cross-connections.

## System Bays

Release 4.0 of the DACS IV-2000 (256) supports five types of system bays:

- Switch (SW) Bay — provides control for the system, fuses, the cross-connections, the switch matrix, and interbay cabling.
- DS1 Interface (INTFC) Bay — provides the interface for up to 868 DS1 signals (equivalent to 31 DS3 signals). This bay provides air baffles for cooling of the associated equipment.
- DS3 Interface (INTFC) Bay — provides the interface for up to 62 DS3 signals (equivalent to 1736 DS1 signals). This bay provides air baffles for cooling of the associated equipment.

- STS1/DS3/DS1 Interface (INTFC) Bay — provides the interface for:
  - — Up to 420 DS1 signals (equivalent to 15 DS3 signals) and
  - — Up to 46 DS3 signals (equivalent to 1288 DS1 signals) and no STS-1 signals, or up to 30 STS-1 signals and no DS3 signals.

  This bay provides air baffles for cooling of the associated equipment.
- STS1/DS3 Interface (INTFC) Bay — provides the interface for up to 60 DS3 and/or STS-1 signals (each DS3 is equivalent to 28 DS1 signals and each STS-1 is equivalent to 28 VT1.5 signals). This bay provides a fan assembly for cooling of the associated equipment.

Table 3-1 identifies the different types of bays and their associated equipment.

Table 3-1. System Bays and Associated Modules

| Bay | Module | Modules Per Bay |
|---|---|---|
| Switch (SW) | Redundant Controller (RC)<br>Redundant Controller Power (RC PWR)<br>Switch Power (SW PWR)<br>Auxiliary Power (AUX PWR)<br>Synchronizer (SYNC)<br>Switch (SW)<br>Fuse and Alarm (FS & ALM) Panel<br>Fan Assembly | 1<br>1<br>1<br>1<br>1<br>1<br>1<br>1 |
| DS1 Interface (INTFC) | DS1 Interface (INTFC)<br>DS1 Interface-Protection (INTFC-P) | 3<br>1 |
| DS3 Interface (INTFC) | DS3 Interface-32 (INFTC) | 2 |
| STS1/DS3/DS1 Interface (INTFC) | DS1 Interface (INTFC)<br>DS1 Interface-Protection (INTFC-P)<br>DS3 Interface-32 (INTFC-32)<br>DS3 Interface-16 (INTFC-16)<br>STS1 Interface-16 (INTFC-16) | 1<br>1<br>0 or 1*<br>0 or 1†<br>0-2*† |
| STS1/DS3 Interface (INTFC) | DS3 Interface-16 (INTFC-16)<br>STS1 Interface-16 (INTFC-16)<br>Fan Assembly | 0-4‡<br>0-4‡<br>1 |

* STS1/DS3/DS1 Interface Bays can be equipped with an STS1 Interface-16 Module in place of the DS3 Interface-32 Module. When doing so, the capacity of the DACS IV-2000 is decreased by 16 DS3 equivalent signals (per such conversion)

† STS1/DS3/DS1 Interface Bays can be equipped with either a DS3 Interface-16 or STS1 Interface-16 Module in the bottom shelf (STS1/DS3 Interface-16 shelf).

‡ STS1/DS3 Interface Bays can be equipped with any combination of DS3 Interface-16 and STS1 Interface-16 Modules totaling four.

Figures 3-1, 3-2, and 3-3 illustrate the physical association of bays, units (the shelf positions of interface modules), and interbay cables (refer to the section titled "Interbay Cabling" later in this chapter for more information) in a fully-equipped system with all DS1, DS3, or STS-1 interfaces, respectively. For example, using Figure 3-1, look at Unit 11, located in the third column of the second row. Thus:

- The first label in Unit 11 is SWIO 7. This represents the Switch Input/Output (SWIO) circuit pack in the Switch Module that is associated with Unit 11.
- The designation N-Rate D indicates half of an N-rate cable (labeled D) that connects this interface module to the Switch Module.
- The number 9 indicates the DS1 Interface-Protection Module (located in Unit 9) responsible for protection this interface module.
- Finally, the number J-7 shows the control cable for this interface module in the bay lineup.

Each unit shown in this sample configuration is labeled with the same information.

The unit numbers and control cable numbers shown are the same for any DACS IV-2000 configuration. The examples pictured in Figures 3-1, 3-2, and 3-3 are based on maximum DS1, DS3, and STS-1 configurations, but the same numbers are used for other configurations. Refer to the section titled "Unit Numbering" in this chapter for more information.

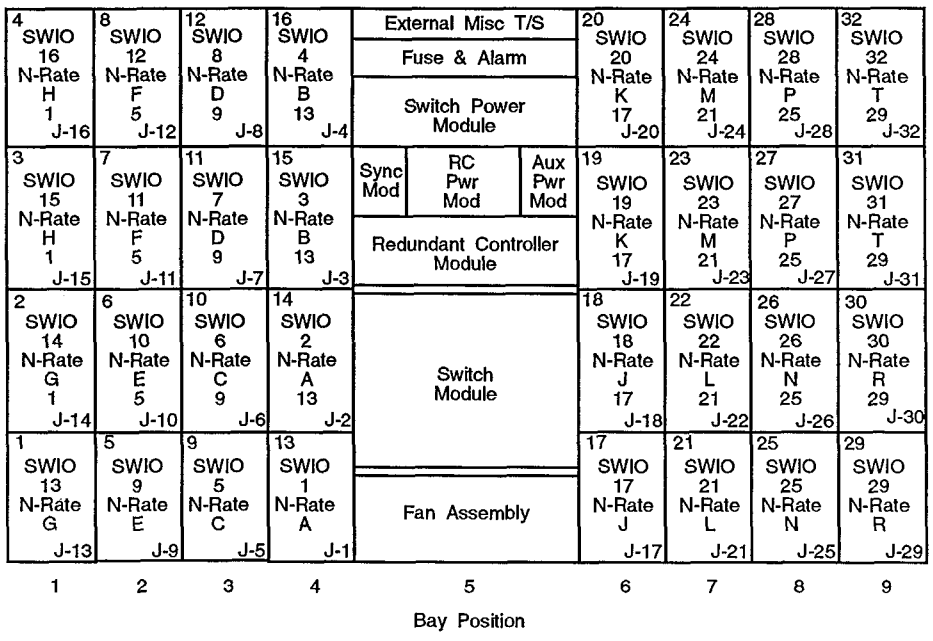
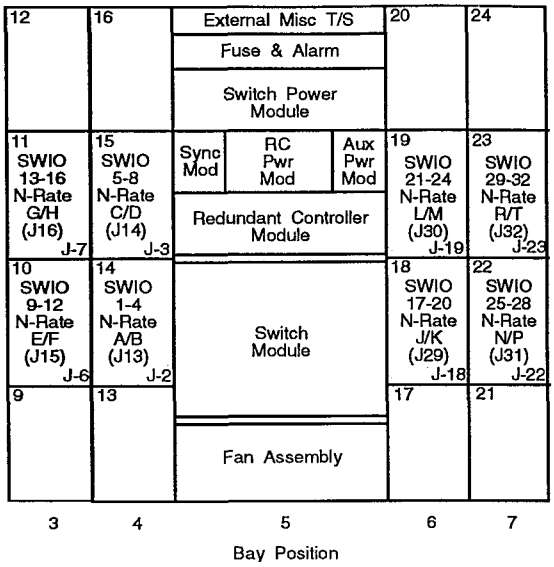



Figure 3-1. **Maximum Configuration of DS1 Interface Modules**




Note:

The J-Cable (control cable) ID shown in parentheses is the control cable for the optional DS3PM circuit pack. In the above figure, it is assumed each DS3 Interface-32 Module contains a DS3PM circuit pack.

Figure 3-2. **Maximum Configuration of DS3 Interface-32 Modules**

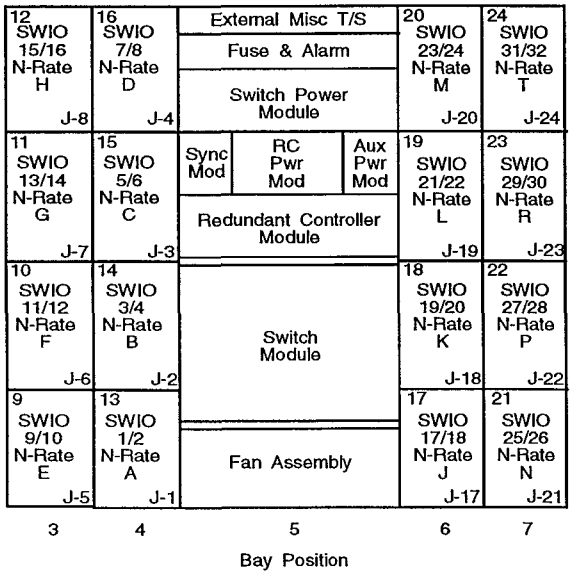
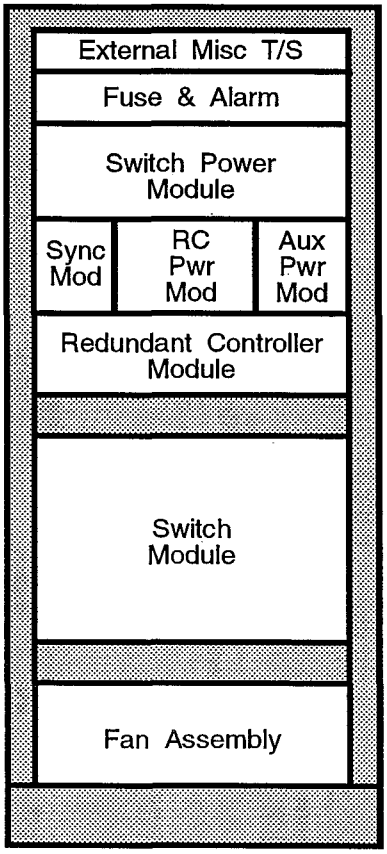



Figure 3-3. **Maximum Configuration of STS1 Interface-16 Modules**

## Bay Types

### Switch Bay

The Switch (SW) Bay (Figure 3-4) contains the Switch (SW) Module, the Switch Power (SW PWR) Module, the Auxiliary Power (AUX PWR) Module, the Redundant Controller (RC) Module, the Redundant Controller Power (RC PWR) Module, the Synchronizer (SYNC) Module, the fuse & alarm (FS & ALM) panel, and the fan assembly. The Switch Bay is the core of the DACS IV-2000 system, and is therefore required for any system configuration. All interplay cabling for the system is provided with the Switch Bay. This cabling is stored temporarily in the two cable end guard assemblies until the system is expanded to its maximum configuration. The Switch Bay is fuse-protected only for the equipment that is shipped initially. Dummy fuses are provided in all other fuse positions.

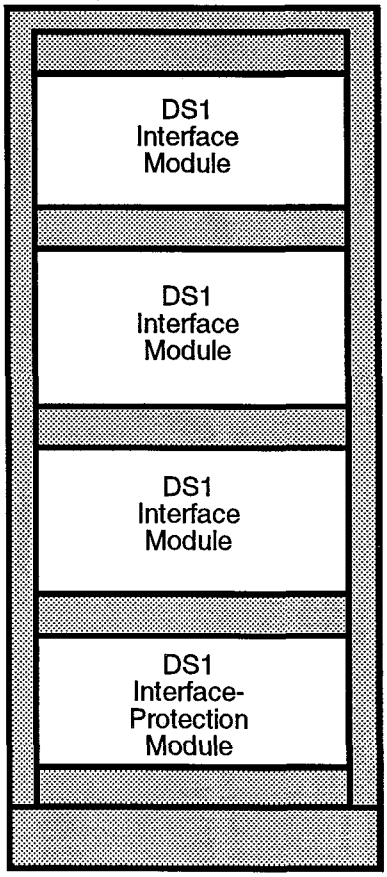



Front View

Figure 3-4. Switch Bay

## DS1 Interface Bay

The DS1 Interface (INTFC) Bay (Figure 3-5) contains three DS1 Interface Modules and one DS1 Interface-Protection Module. The DS1 Interface-Protection Module interfaces with up to 196 DS1 signals and each DS1 Interface Module interfaces with up to 224 DS1 signals. Consequently, each DS1 Interface Bay provides a capacity of up to 868 DS1 signals (31 equivalent DS3 signals). However, each PMGR1 circuit pack used for performance monitoring reduces the capacity by 28 DS1 signals. Protection for the DS1 Interface Bay is provided by the DS1 Interface-Protection Module. This module provides protection for itself, and up to three other DS1 Interface Modules. Protection for the bay is on a 1 to 31 basis.

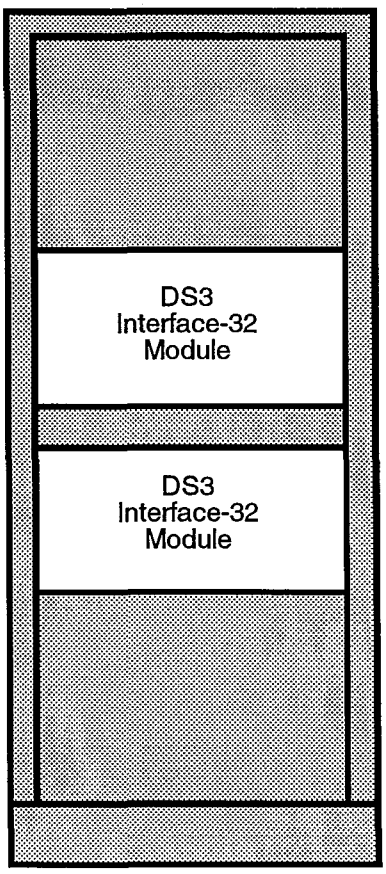



Front View

Figure 3-5. DS1 Interface Bay

## DS3 Interface Bay

The DS3 Interface (INTFC) Bay (Figure 3-6) contains two DS3 Interface-32 Modules. Each DS3 Interface-32 Module can be equipped to interface with up to 31 DS3 signals. Each bay provides a capacity of up to 62 DS3 signals. However, each PMGR1 circuit pack used for performance monitoring reduces the capacity by one DS3 signal. Protection for the DS3 Interface Bay is provided on an individual module basis. Each module provides protection for itself, and the protection is done on a 1 to 31 basis.

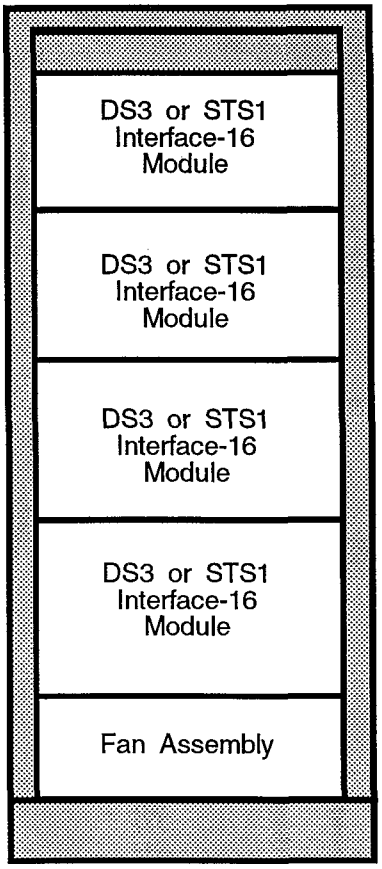



Front View

Figure 3-6. DS3 Interface Bay

## STS1/DS3 Interface Bay

The STS1/DS3 Interface (INTFC) Bay (Figure 3-7) contains four equipment shelves that can hold DS3 or STS1 Interface-16 Modules. Each DS3 Interface-16 Module can be equipped to interface with up to 15 DS3 signals, and each STS1 Interface-16 Module can be equipped to interface with up to 15 STS-1 signals. Each bay provides a capacity of up to 60 DS3 signals and/or STS-1 signals. Protection for the STS1/DS3 Interface Bay is provided on an individual module basis. Each module provides protection for itself, and the protection is done on a 1 to 15 basis.




Front View

Figure 3-7. STS1/DS3 Interface Bay

## STS1/DS3/DS1 Interface Bay

The STS1/DS3/DS1 Interface (INTFC) Bay (Figure 3-8) contains one DS1 Interface Module, one DS1 Interface-Protection Module, one DS3 Interface-32 module, and one DS3 Interface-16 or STS1 Interface-16 Module. The DS1 Interface and DS1 Interface-Protection Modules are identical to those in the DS1 Interface Bay and can be equipped to interface with up to 224 and 196 DS1 signals, respectively. The DS3 Interface-32 Module can be equipped to interface with up to 31 DS3 signals. The DS3 Interface-16 Module can be equipped to interface with up to 15 DS3 signals, while the STS1 Interface-16 Module can be equipped to interface with up to 15 STS-1 signals. Consequently, each STS1/DS3/DS1 Interface Bay provides a capacity of up to 46 DS3 signals and 420 DS1 signals (15 equivalent DS3 signals) when equipped with a DS3 Interface-16 Module. It can provide up to 31 DS3 signals, 15 STS-1 signals, and 420 DS1 signals when equipped with a STS1 Interface-16 Module. However, each PMGR1 circuit pack used for performance monitoring reduces the capacity by 28 DS1 signals in the DS1 Interface Modules or 1 DS3 signal in the DS3 Interface Modules. PMGR1 circuit packs cannot be used in STS1 Interface-16 Modules. Protection for the STS1/DS3/DS1 Interface Bay is provided in two ways:

- Protection for the DS3 and STS1 Interface Modules is on an individual module basis; the DS3 Interface-32 Module is protected on a 1 to 31 basis; and the DS3 and STS1 Interface-16 Module is protected on a 1 to 15 basis.
- The DS1 Interface-Protection Module provides protection for itself plus the DS1 Interface Module. This protection is provided on a 1 to 15 basis.

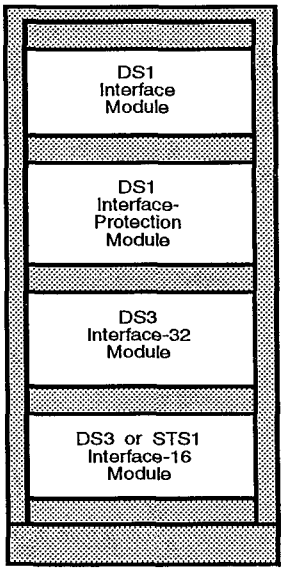



Figure 3-8. STS1/DS3/DS1 Interface Bay

## Bay Configurations

The flexibility provided by the modular design of the DACS IV-2000 allows for different initial bay configurations based on traffic requirements. It can later be expanded to a number of possible bay layouts for a fully configured system. The following sections discuss configuration alternatives.

The four basic types of DACS IV-2000 interface bays enable you to create many possible bay layouts for a fully-configured system. Figure 3-9 shows fully-configured systems and the typical order in which the systems are expanded. These configurations are not intended to limit the options, but rather represent the range of DS1 terminations, DS3 terminations, and Electrical Carrier-1 (EC-1)[1] terminations.

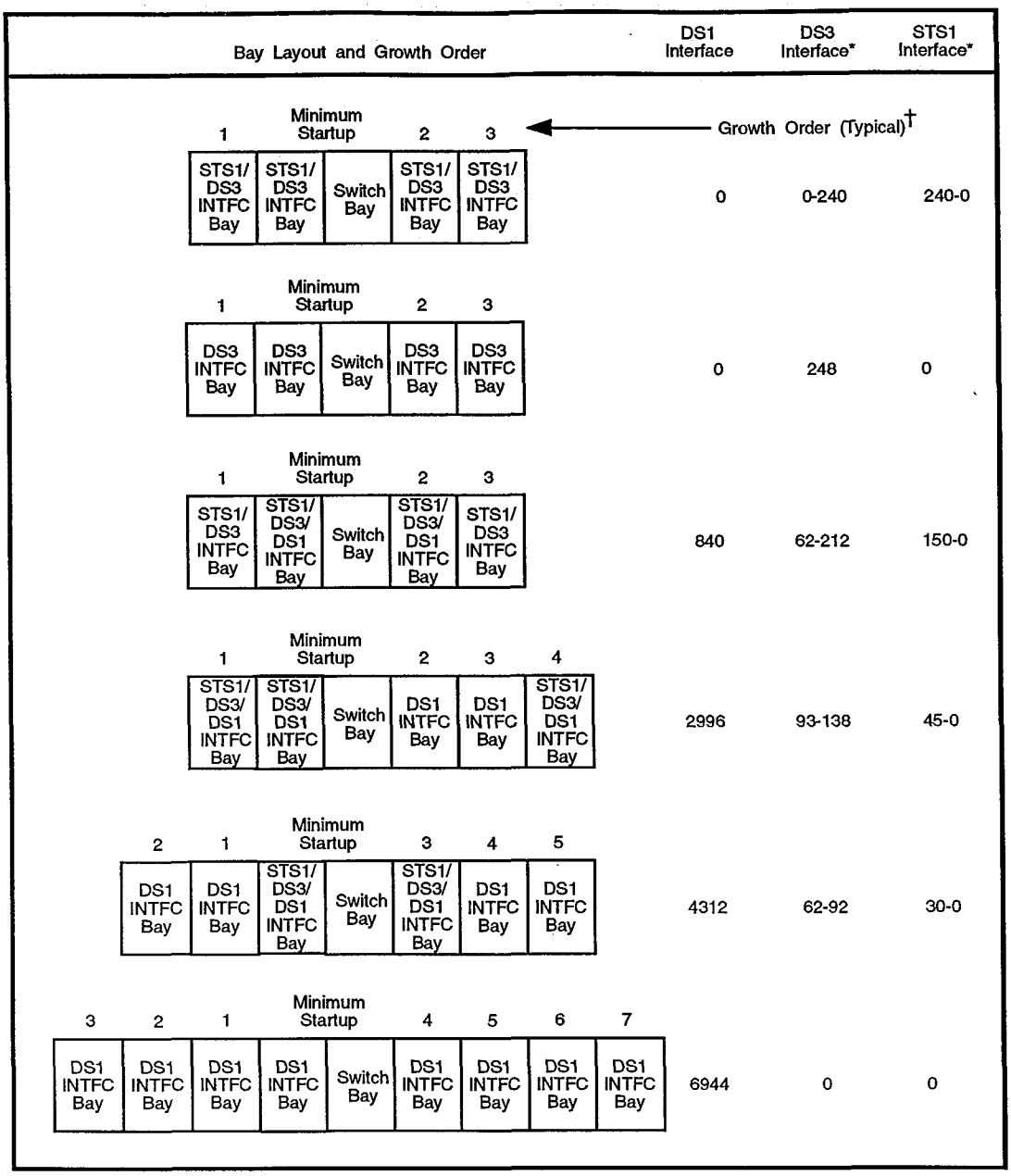
The DACS IV-2000 system can be configured to accommodate any changing DS1, DS3, and EC-1 facility needs over time under the cabling constraint that no more than 124/120 equivalent DS3s/STS-1s (including protection) can be connected on either side of the Switch (SW) Bay. Because of this cabling constraint, the Switch Bay is usually located at or near the center of the bay layout, as shown in Figure 3-9. A maximum of two STS1/DS3/DS1 Interface Bays, two DS3 Interface Bays or STS1/DS3 Interface Bays, or four DS1 Interface Bays can be located on either side of the Switch Bay.

When planning the bay layout, keep in mind that the capacity of a DS1 Interface Bay (32 equivalent DS3 signals) is half the capacity of an STS1/DS3/DS1 Interface Bay or a DS3 Interface Bay.

**NOTE:**
DS1 Interface Bays can be purchased separately, but must be installed in tandem with another DS1 Interface Bay before any other type interface bay can be added to the system.

For DS1 applications requiring thicker (22 gauge) cable, consider a Digital Systems Access Bay (DSAB) to eliminate potential cable congestion. For more information on a DSAB, refer to the *Digital Systems Access Bay (DSAB) System Reference Guide* (AT&T 365-301-135). When using DSAB bays, all interface circuit pack slots (DS1IF and SWIF) must be equipped with either SWIF/DS1IF or BXA circuit packs.

1. Electrical Carrier-1 (EC-1) is the industry standard nomenclature for an electrical STS-1 signal.




* The designation STS1/DS3/DS1 INTFC Bay indicates a standard configuration of 1 DS3 Interface-32, 1 DS3 Interface-16 or STS1 Interface-16, 1 DS1 Interface, and 1 DS1 Interface-Protection Module.

† Adjacent bays can be added to either the left or right side; the growth order shown is for typical growth.

Figure 3-9. **Sample System Configurations**

## Recommended Arrangements

### Bay Mounting

The DACS IV-2000 interface bays are 2 feet 2 inches wide, 7 feet high, 12 inches deep. The Switch Bay is 2 feet 2 inches wide, 7 feet high, and 13 inches deep. Both the Interface and the Switch Bays use the network bay framework. Equipment shelves that mount on these bays are factory installed. The only expansion that occurs is for additional circuit packs or growth bays.

The Switch Bay and STS1/DS3 Interface Bays have forced-air cooling while the DS1, DS3, and STS1/DS3/DS1 Interface Bays are cooled by free convection. The fan assembly at the bottom of the Switch and STS1/DS3 Interface Bays takes in air near the floor and exhausts it out the top rear of the bay. Unequipped circuit pack slots are not permitted. Functionally unused slots must either contain a circuit pack or be covered with filler assemblies. Heat baffles are used between the shelves on the interface bays to direct rising heat away from the circuit packs located above.

The initial or startup bay configuration consists of the Switch Bay, one interface bay, and two temporary cable end guard assemblies all bolted together as a unit for shipment. This initial configuration is 6 feet 6 inches wide. The Switch Bay is delivered with all its interbay cabling for maximum capacity. Consequently, the cable end guard assemblies are required to store and protect the cables until they are needed. The initial bays are bolted to the floor during installation.

When a growth interface bay is provided, the appropriate cable end guard assembly is moved to allow bay placement adjacent to the existing arrangement. The growth bay is bolted to the floor next to its adjacent bay, and the connections are made between it and the Switch Bay. The cable end guard assembly is discarded if all the stored cable has been used on that side of the Switch Bay. Otherwise, it is reattached to the new growth interface bay on the side away from the Switch Bay. Recommended growth is to the left of the Switch Bay until all the cables are used, then to the right of the Switch Bay.

### Interbay Cabling

A DACS IV-2000 can be one of several combinations of DS3, STS1/DS3, STS1/DS3/DS1, and DS1 Interface Bays. Cables transmitting N-rate signals connect the SWIO circuit packs in the Switch Module to MUX circuit packs in DS3 Interface Modules, to SMUX circuit packs in STS1 Interface-16 Modules, and to SWIF circuit packs in DS1 Interface Modules. Cables also connect unit controller (UC) circuit packs in DS3, STS1, and DS1 Interface Modules and DS3PM circuit packs in DS3 Interface Modules to the Switch Bay.

Logical, systematic rules are used in the naming of the interbay cables to aid technicians when installing, provisioning, and troubleshooting the frame. This section contains a summary of the cabling information. The summary is adequate for provisioning the frame.

## N-rate Cables

In a fully equipped frame, cables must carry 2048 N-rate signals between interface modules and the Switch Bay (512 service signals and 512 protection signals in each direction for a total of 2048). A total of 256 cables is used for this purpose. These cables are divided into 16 groups and designated by letters running from A through T, omitting I, O, Q, and S. Each of the 16 groups contains 16 cables. These cables are labelled J1-A, J2-A, ..., J16-A, for example. J1-A through J8-A serve SWIO-1, and J9-A through J16-A serve SWIO-2 (SWIO-1's mate circuit pack), and so on to J1-T through J16-T which serve SWIO-31 and SWIO-32. Table 3-2 contains the N-rate cable group that serves each SWIO circuit pack

Since 2048 N-rate signals are handled, each of the 256 cables must carry 8 N-rate signals. Each cable also contains two-wire pairs to carry a clock/ synchronizing signal so that each cable contains 20 wires. Any given cable serves four MUX, four SMUX, or four SWIF circuit packs, carrying two N-rate signals, either service or protection, to or from each circuit pack.

N-rate Cable groups A through H connect to interface modules on the left side and N-rate Cable groups J through T connect to interface modules on the right side of the Switch Bay as seen from the front of the frame. A DS3 Interface-32 Module requires two N-rate cable groups; a DS3 Interface-16 or STS1 Interface-16 Module requires one N-rate cable group; and two DS1 Interface Modules share an N-rate cable group. N-rate cable group A connects to the lowest module on the interface bay (Bay 4) closest to the switch matrix, and the other N-rate cable groups run alphabetically upward and outward from the switch matrix. N-rate cable group starting with J serve the interface bays on the right side of the frame in a similar fashion.

Table 3-2. SWIO N-Rate Cable Connections

| N-rate Cable Group | SWIO Circuit Packs | | N-rate Cable Group | SWIO Circuit Packs | |
|---|---|---|---|---|---|
| | Cables J1-An — J8-An | Cables J9-An — J16-An | | Cables J1-Bn — J8-Bn | Cables J9-Bn — J16-Bn |
| A | 1 | 2 | J | 17 | 18 |
| B | 3 | 4 | K | 19 | 20 |
| C | 5 | 6 | L | 21 | 22 |
| D | 7 | 8 | M | 23 | 24 |
| E | 9 | 10 | N | 25 | 26 |
| F | 11 | 12 | P | 27 | 28 |
| G | 13 | 14 | R | 29 | 30 |
| H | 15 | 16 | T | 31 | 32 |

## Control Cables

The 32 control cables that connect the unit controllers to the Switch Bay are labelled J1 through J32. J1 through J16 serve the interface bays to the left side of the Switch Bay, and J17 through J32 serve the interface bays on the right side. Numbering is similar to the letter assignments of N-rate cables in that numbering starts at the bottom of the interface by (Bays 4 and 6) nearest the Switch Bay and goes upward and outward. However, just as in the numbering of the 32 units, a number is assigned to each of the four available mode positions even if some positions are not occupied, For example, a DS3 Interface-32 Module in Bay 4 would have cables J2 and J3 assigned and cables J1 and J4 unassigned.

As many as sixteen DS3PM circuit packs can be used, one for each DS3 Interface-32 or Interface-16 Module. Numbering of the control cables to DS3PM circuit packs to the left of the Switch Bay starts at J9 and runs upward and outward through J16. DS3PM circuit pack control cable numbers to the right of the Switch Bay start at J25 and run upward and outward through J32. These DS3PM circuit pack control cable designations are the same as some in the set used for unit controller control cables. However, there is no numbering conflict in a given frame because unit controller control cable designations J9 through J16 are used for Bays 1, and 2; and J17 through J24 are used for Bays 8 and 9. For any given configuration of DS3 Interface Modules in the frame, a combination of Bays 1, 2, 8, and 9 is not present, therefore allowing the use of the associated UC control cables for the DS3PM circuit packs. Table 3-3 contains the control cable assignments for each interface module unit location.

Table 3-3. Control Cable Assignments

| Unit | Control Cable | Unit | Control Cable | Unit | Control Cable | Unit | Control Cable |
|---|---|---|---|---|---|---|---|
| 1 | J13 | 9 | J5 | 17 | J17 | 25 | J25 |
| 2 | J14 | 10 | J6 | 18 | J18 | 26 | J26 |
| 3 | J15 | 11 | J7 | 19 | J19 | 27 | J27 |
| 4 | J16 | 12 | J8 | 20 | J20 | 28 | J28 |
| 5 | J9 | 13 | J1 | 21 | J21 | 29 | J29 |
| 6 | J10 | 14 | J2 | 22 | J22 | 30 | J30 |
| 7 | J11 | 15 | J3 | 23 | J23 | 31 | J31 |
| 8 | J12 | 16 | J4 | 24 | J24 | 32 | J32 |

## Unit Numbering

To provide a standard numbering convention for the DACS IV-2000 system, the complete bay lineup for the system is considered. Figure 3-10 shows a DACS IV-2000 system nine-bay arrangement with each interface bay having four shelf positions (units). The numbering scheme assigns fixed unit numbers to the 32 possible shelf positions in a complete system. The type of module in a shelf position depends on the bay type. For example, an initial two-bay configuration consists of an STS1/DS3/DS1 Interface Bay, and a Switch Bay. This two-bay configuration has four units, numbered 13 through 16, starting at the bottom. For DS3 Interface Bays, shelf positions 1 and 4 are empty and are not labeled. For example, if an initial arrangement consists of a DS3 Interface Bay and a Switch Bay, the equipped shelves are units 14 and 15, while the unequipped shelves do not have unit labels.

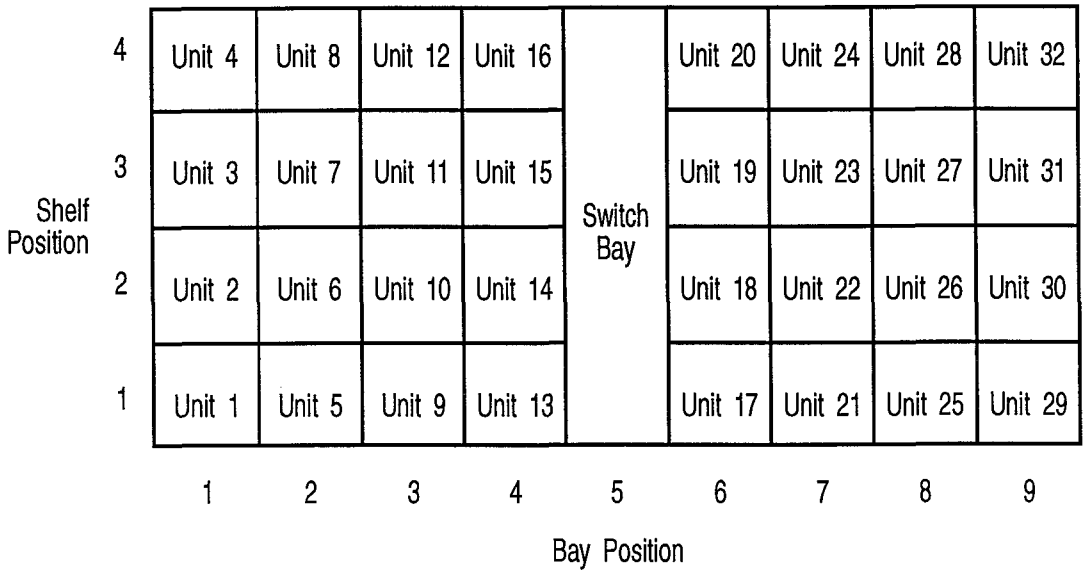



Figure 3-10. **Recommended Unit Numbering**

## Circuit Pack Numbering

The numbering convention used in a central office environment generally differs from the numbering convention used for the DACS IV-2000. The DACS IV-2000 numbering convention uses DS3 or STS-1 equivalents that correspond to a Multiplexer (MUX) circuit pack supporting one DS3, a SONET Multiplexer (SMUX) circuit pack supporting one STS-1, or a Switch Interface (SWIF) circuit pack supporting 28 DS1s. If the other end of a facility connected to the DACS IV-2000 connects to a DSX-3 or a DSX-1, it is difficult to reconcile the numbering conventions. The numbering convention uses the slot number in the interface module to designate a DS3 or a DS1. Table 3-4 shows the valid slot numbers in the DACS IV-2000 frame.

Table 3-4. **Valid Slot Number Conventions**

| Interface Module Type | Slot Number |
|---|---|
| STS1 Interface-16 | 1-15 |
| DS3 Interface-32 | 1-31 |
| DS3 Interface-16 | 1-15 |
| DS1 Interface | 1A,1B-8A,8B |
| DS1 Interface-Protection | 1A,1B-7A,7B |

Each slot in a DS3 or STS1 Interface Module (DS3 Interface-32, DS3 Interface-16, or STS1 Interface-16) corresponds to one MUX/SMUX circuit pack. Each MUX/SMUX circuit pack allows for addressing of 28 DS1/VT1.5 signals within a DS3/STS-1 signal, respectively. For example, a DS3 facility terminating in a DS3 Interface Module located in unit 16 on the MUX circuit pack in slot 14 is numbered 16-14. The associated DS1 signals are numbered 16-14-1 through 16-14-28.

To form a DS3 equivalent (identified by the slot number), two DS1IF circuit packs are required (each DS1IF is associated with 14 DS1 ports). Therefore, one of the DS1IF circuit packs is identified with an A appended to the slot number (addresses ports 1 through 14 of the equivalent DS3) and the other with a B appended to the slot number (addresses ports 15 through 28 of the equivalent DS3). For example, a DS1 facility terminating in a DS1 Interface Module located in unit 24 at slot 8B on port 20 of the DS1IF circuit pack is numbered 24-8-20.

In contrast to the above, a typical DSX numbering convention uses SRV (service) to designate a DS3 group (28 DS1s) and CRT (circuit) to designate individual DS1s within the group.

## Minimum Start-up Configurations

There are six initial bay configurations for the DACS IV-2000 system. Each one consists of a Switch Bay in combination with one of four interface bays. A particular startup bay configuration depends on the type of terminations required, such as for STS-1 signals. Empty interface bays are not provided in any configuration.

### DS3 Configuration

If only DS3 interfaces are required initially, the minimum configuration consists of a Switch Bay and either a DS3 Interface Bay (Figure 3-11) or an STS1/DS3 Interface Bay (Figure 3-12) equipped with four DS3 Interface-16 Modules. This configuration has an interface capacity of 62 DS3 signals (DS3 Interface Bay) or 60 DS3 signals (STS1/DS3 Interface Bay).

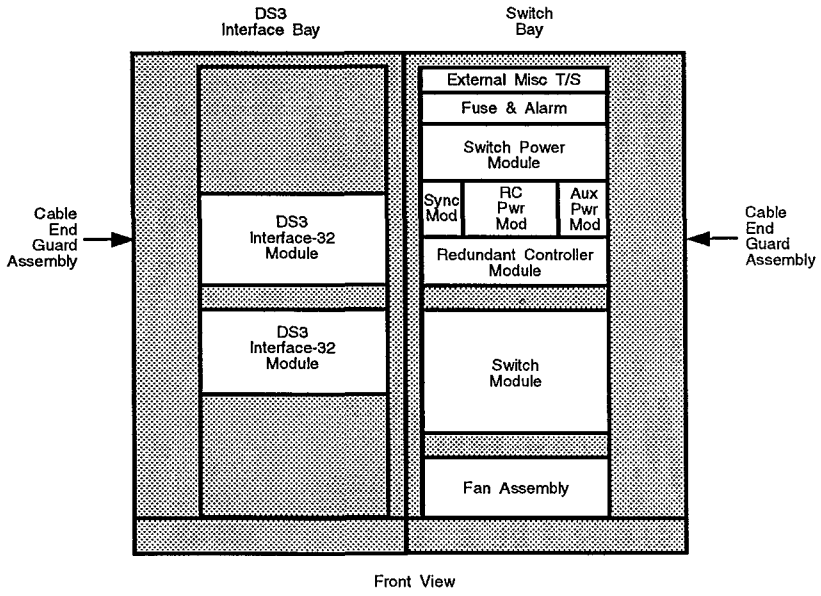



Figure 3-11. **Minimum Start-up Configuration for DS3 Interfaces (DS3 Interface Bay)**

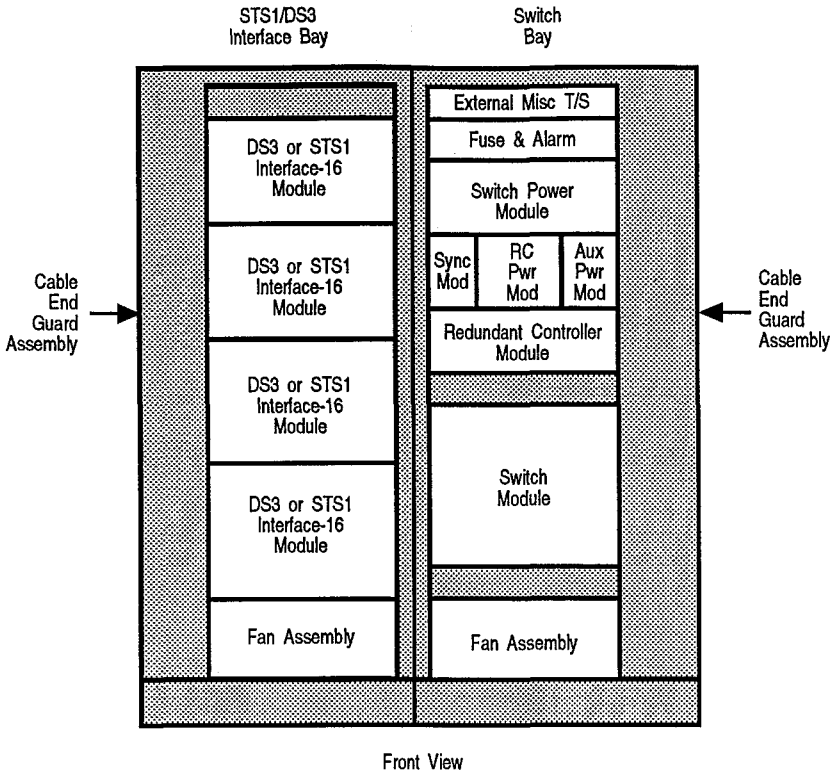



Figure 3-12. **Minimum Start-up Configuration for STS-1 or DS3 Interfaces Only (STS1/DS3 Interface Bay)**

## STS1 Configuration

If only STS-1 interfaces are required initially, the minimum configuration (Figure 3-12) consists of a Switch Bay and an STS1/DS3 Interface Bay equipped with four STS1 Interface-16 Modules. This configuration has an interface capacity of 60 STS-1 signals.

## STS1/DS3 Configuration

If a mix of STS-1 and DS3 interfaces is required, the bay configuration (Figure 3-12) consists of a Switch Bay and an STS1/DS3 Interface Bay equipped with STS1 and DS3 Interface-16 Modules totaling four. This configuration has an interface capacity of 60 STS-1 signals and/or DS3 signals.

## DS3/DS1 Configuration

If a mix of DS3 and DS1 interfaces is required, the configuration consists of a Switch Bay and an STS1/DS3/DS1 Interface Bay equipped with a DS3 Interface-16 Module (Figure 3-13). This configuration has an interface capacity of 46 DS3 signals and 420 DS1 signals.

## STS1/DS3/DS1 Configuration

If a mix of STS-1, DS3, and DS1 interfaces is required, the bay configuration consists of a Switch Bay and an STS1/DS3/DS1 Interface Bay equipped with an STS1 Interface-16 Module (Figure 3-13). This configuration has an interface capacity of 15 STS-1 signals, 31 DS3 signals, and 420 DS1 signals.

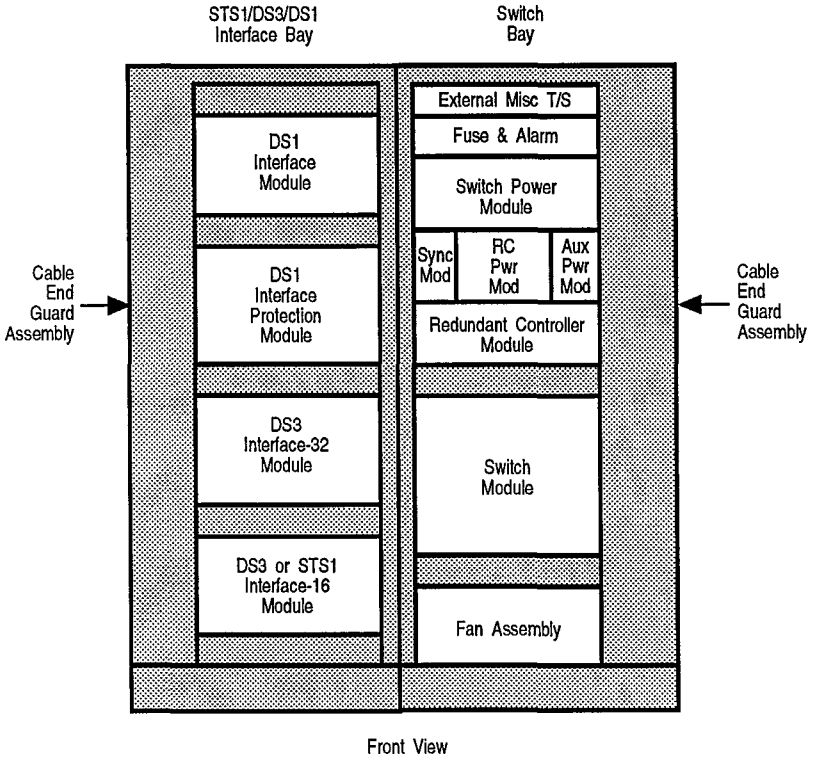



Figure 3-13. **Minimum Start-up Configuration for STS-1, DS3, and DS1 Interfaces**

## DS1 Configuration

If only DS1 interfaces are required initially, the bay configuration consists of an Switch Bay with a DS1 Interface Bay (Figure 3-14). This configuration has an interface capacity of 868 DS1 signals.

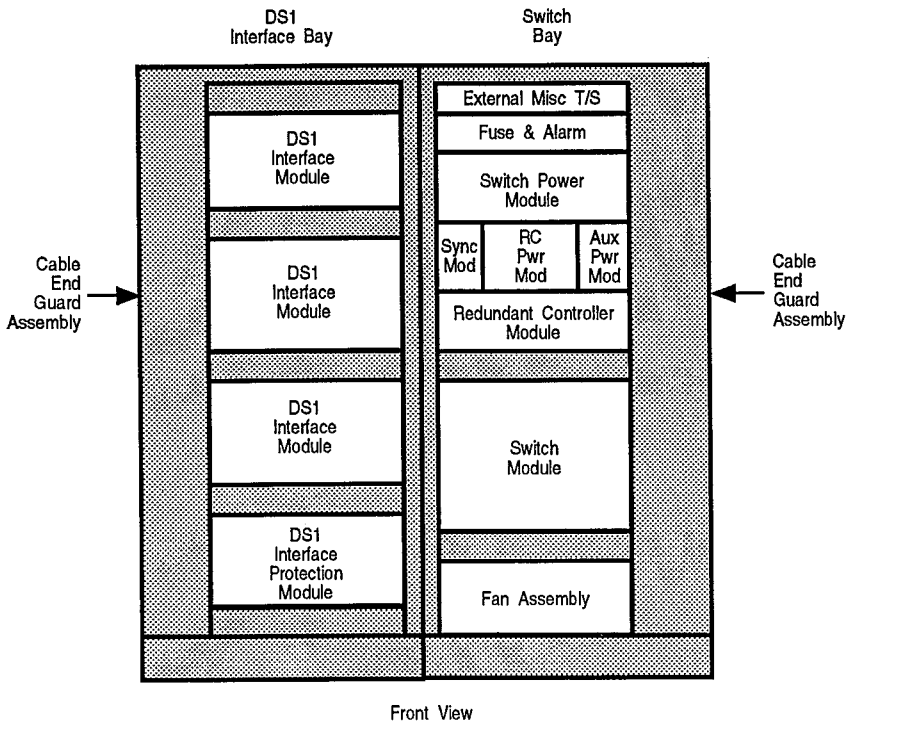



Figure 3-14. **Minimum Start-up Configuration for DS1 Interfaces Only**

## Modules

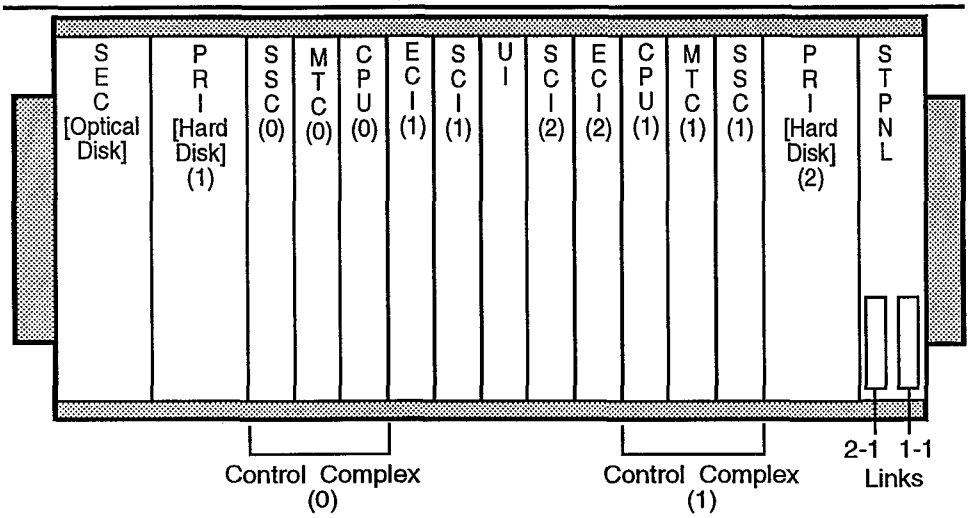
There are eleven DACS IV-2000 system modules, as follows:

- Redundant Controller (RC) Module
- Redundant Controller Power (RC PWR) Module
- Synchronizer (SYNC) Module
- Switch (SW) Module
- Switch Power (SW PWR) Module
- Auxiliary Power (AUX PWR) Module
- DS1 Interface (INTFC) Module
- DS1 Interface-Protection (INTFC-P) Module
- DS3 Interface-32 (INTFC-32) Module
- DS3 Interface-16 (INTFC-16) Module
- STS1 Interface-16 (INTFC-16) Module

Each of these modules is described in the sections that follow.

## Redundant Controller Module

The Redundant Controller Module manages the user interface (administrative links), performs user specified functions, and coordinates database management, maintenance, and fault recovery operations. Figure 3-15 shows the circuit pack locations in the Redundant Controller Module. Table 3-5 lists the Redundant Controller Module circuit packs, their functions, and quantity.




Note: Number in parentheses is circuit pack position in module.

Figure 3-15. **Redundant Controller Module**

Table 3-5. **Redundant Controller Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| CPU2 | Central Processing Unit 2 | 2 |
| ECI3 | Enhanced Communications Interface 3 | 2 |
| MTC3 | Maintenance Interface 3 | 2 |
| PRI5 | Primary Storage 5 | 2 |
| SCI3 | Switch Communications Interface 3 | 2 |
| SEC5 | Secondary Storage 5 | 1 |
| SSC5 | Secondary Storage Controller 5 | 2 |
| STPNL | Status Panel | 1 |
| UI2 | Unit Interface 2 | 1 |

Figure 3-16 shows a detailed block diagram of the Redundant Controller Module. Within the Redundant Controller Module are two control complexes. These control complexes provide protection of system control in the event the active control complex fails. A control complex consists of the CPU, SSC, and MTC circuit packs. The functions provided by the different circuit packs within the Redundant Controller Module are:

- Central Processing Unit (CPU) — controls and coordinates all system functions. The CPU contains the microprocessor circuitry. Two CPUs are provided with one active, controlling the system functions, and the other in the standby mode in the event the active CPU fails.
- Secondary Storage Controller (SSC) — controls the start-up and backup of the storage subsystem (disk and optical disk drives). The active SSC responds to signals from its associated CPU when disk accesses are necessary. The SSC directs the information exchange between the active CPU (through the control complex bus) and the nonvolatile backup memory devices, which are the 248-MByte hard disks (PRIs) and the 128-MByte optical disk drive (SEC).

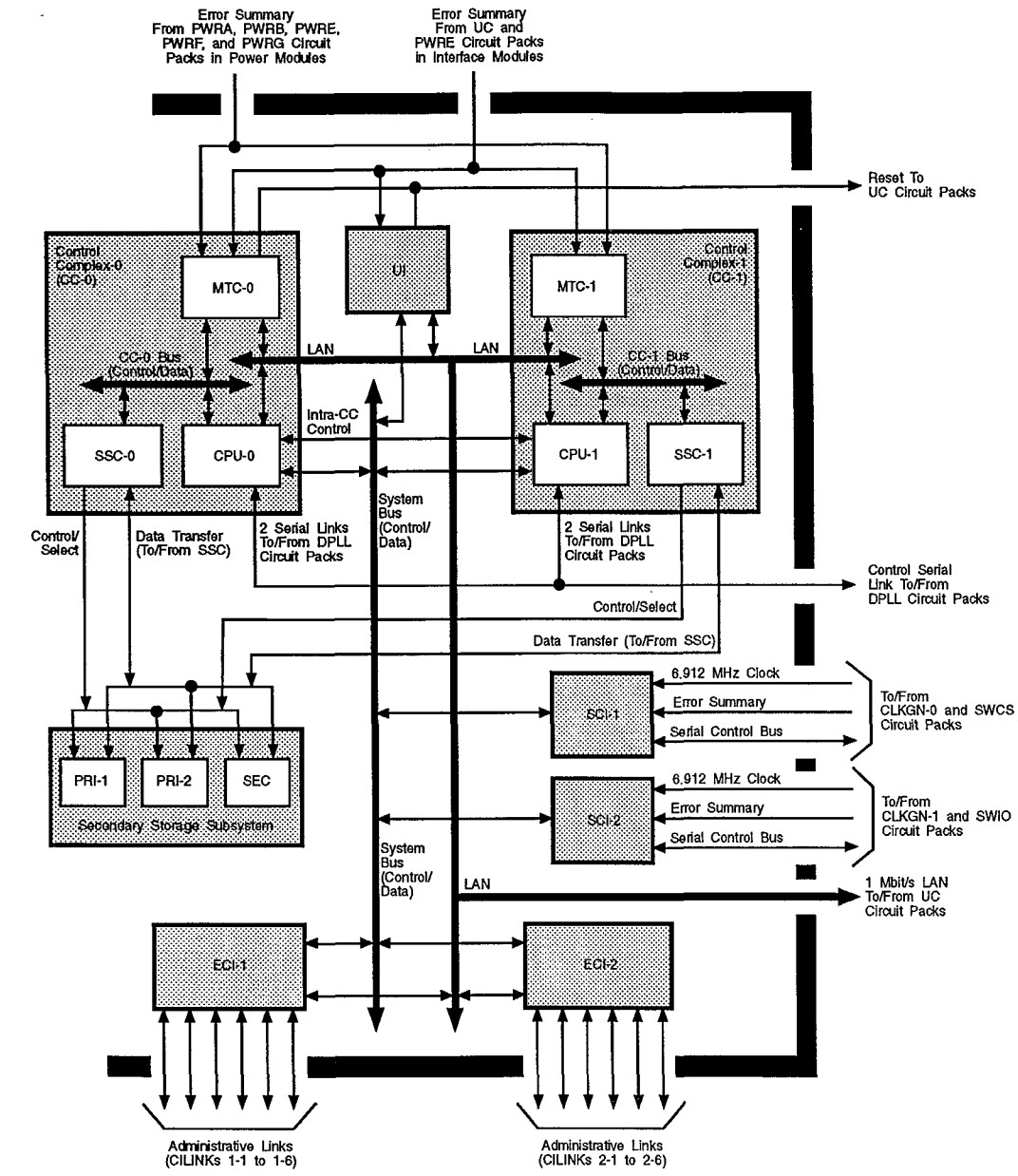


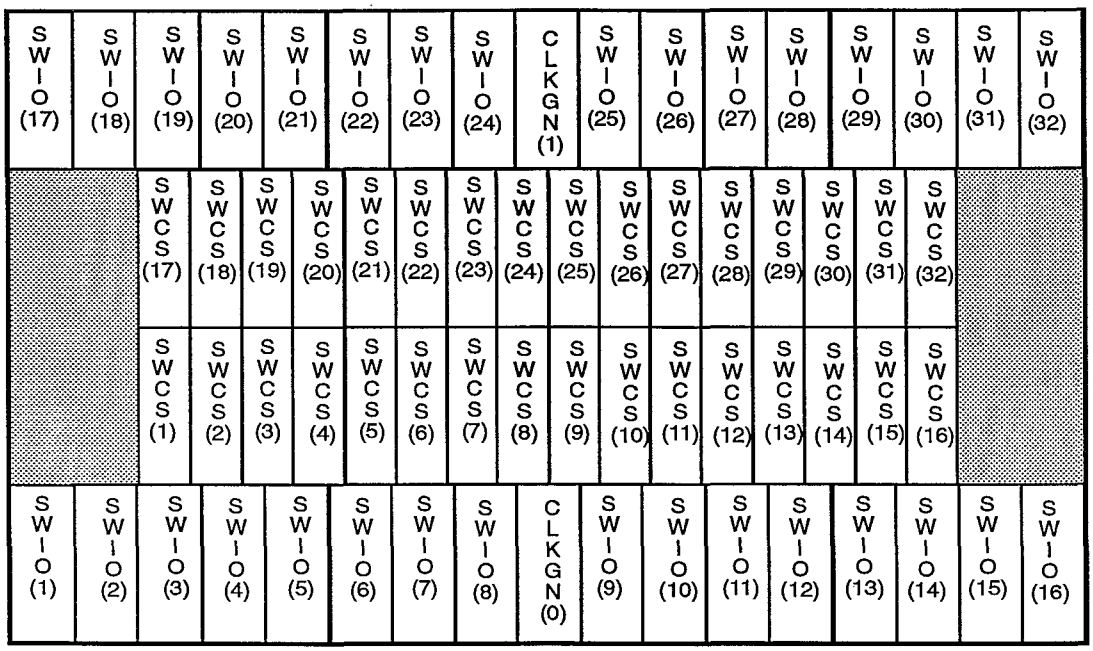

Figure 3-16. **RC Module Block Diagram**

- Maintenance Interface (MTC) — provides error detection for the Redundant Controller Module circuit packs and power module circuit packs. The active MTC, in conjunction with the Unit Interface (UI) circuit packs also provides error detection for the unit controller (UC) and power circuit packs in the interface modules. The MTC circuit packs contain the contact closures for office alarms, provide the hub of the local area network (LAN) communication with the UC circuit packs, and are used to reset UC circuit packs. Control of the MTC circuit pack is provided by its associated CPU circuit pack within the control complex. When the MC is in the OOS-MCOND state, and if the active MTC circuit pack is extracted, the alarm LEDs on the status panel turn off and remain off until a system reset is performed.
- Unit Interface (UI) — provides (in conjunction with the active MTC circuit pack) the LAN distribution and error summary functions for the UC and power circuit packs in the interface modules. The UI is the distribution point for communication over the 1-Mbit/s LAN. Information sent over the LAN provides for control of the UC circuit packs, which in turn control the functions of the interface modules. The active CPU provides control over the UI, by monitoring error summary information and controlling the LAN.
- Enhanced Communications Interface (ECI) — provides the interfaces for remote Operations Systems (OSs) and a local user interface terminal (UIT). Control and data transfer to and from the active CPU is provided through the system bus and the LAN.
- Switch Communications Interface (SCI) — provides the communication and maintenance interfaces between the active CPU and the Switch Module circuit packs (SCI-1 for the SWCS and CLKGN-0 circuit packs and SCI-2 for the SWIO and CLKGN-1 circuit packs) using a serial bus comprising information from the system bus (control, data, and status). The SCI receive a 6.912-MHz clock from its associated CLKGN to provide timing for the serial bus to the Switch Module.
- Primary hard disk drives (PRI) — are nonvolatile memory for the system and do not require continuous dc power to maintain the contents of their memories. The hard disks are the primary backup storage devices. The hard disks contain the system software, a current copy of the cross-connect map, and the functional status of the frame. These records are updated automatically by transfers through the SSC circuit pack.
- Secondary optical disk drive (SEC) — is nonvolatile memory for the system and does not require continuous dc power to maintain the contents of its memory. The main function of optical disk storage is to download new software into the system. Optical disk storage can also be used as secondary memory backup by periodically copying the hard disks. Automatic database backups can be scheduled to execute once in a 24-hour period on selected days or on every day of the week. You can also manually copy the contents of the hard disk to the optical disk or the contents of the internal RAM in the main controller to the optical disk when necessary.

## Switch Module

The Switch Module performs the DS1, STS-1, and VT1.5 cross-connections. Figure 3-17 shows the circuit pack locations in the Switch Module.Table 3-6 lists the Switch Module circuit packs, their functions, and quantity.

Front View




Note: Number in parentheses is circuit pack position in module.

Figure 3-17. **Switch Module**

Table 3-6. **Switch Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| SWIO1 | Switch Input/Output 1 | 2-32 (install in pairs) |
| SWCS1 | Switch Center Stage 1 | 32 |
| CLKGN3<br>CLKGN2 | Clock Generator 3<br>Clock Generator 2 | 2<br>2 (non-SONET only) |
| AWR-type | Filler Assembly | 30-0 (installed in pairs) |

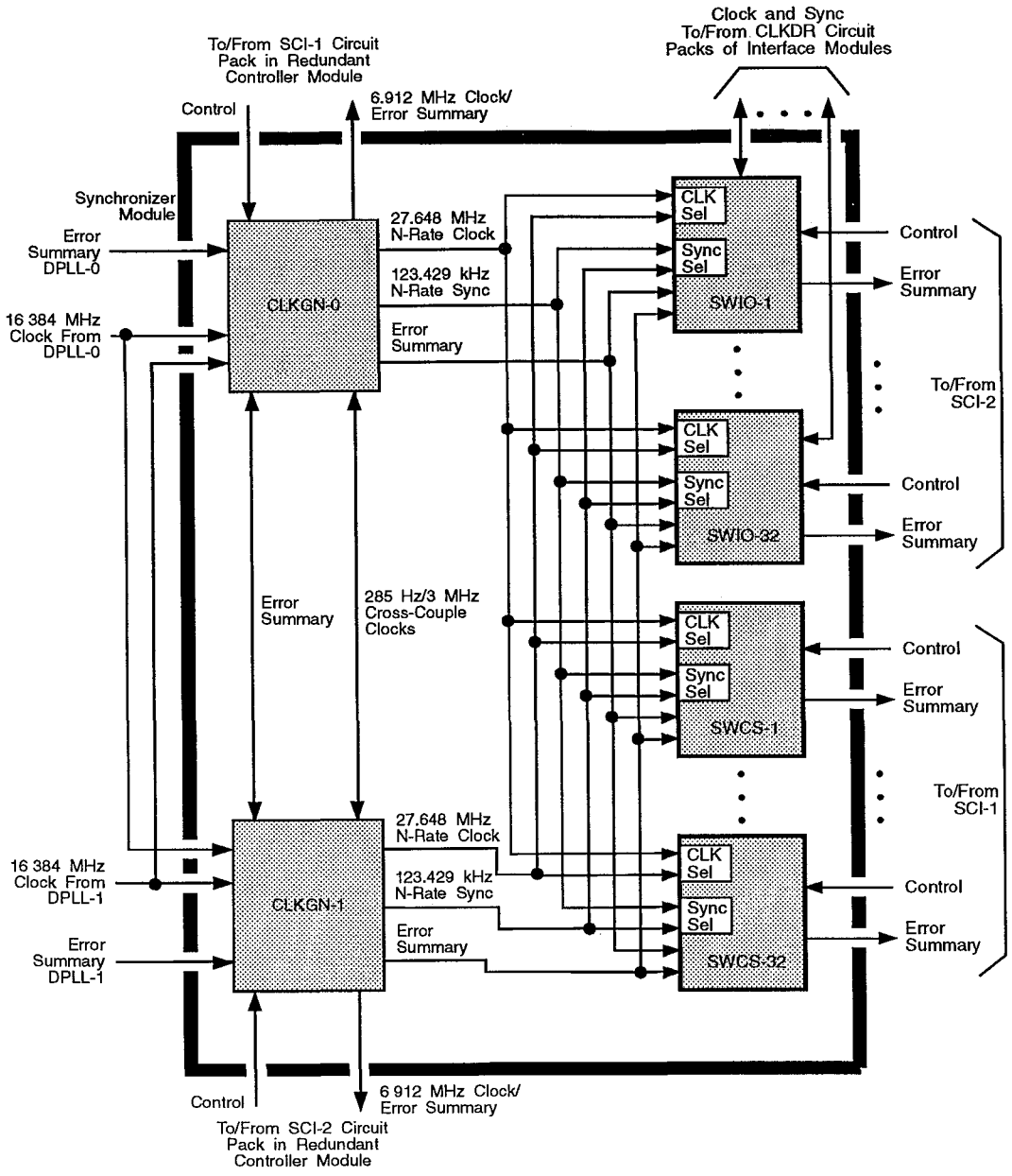
## Three-Stage Switch

Figure 3-18 shows a detailed block diagram of the Switch Module that makes up the non-blocking three-stage switch. Sheet 1 of Figure 3-18 shows the clocking/ synchronization and control functions, while sheet 2 of Figure 3-18 shows the switching (cross-connection) functions.

The functions provided by the circuit packs within the Switch Module are described below:

- Switch Input/Output (SWIO) — provides the input and output switch stages of the cross-connect network, the clock and sync signals from the CLKGN circuit packs to the CLKDR circuit packs in the interface modules, and error summary information to the SCI-2 circuit pack in the Main Controller. The SWIO circuit packs receive control (clock and cross-connect selection) from the SCI-2 circuit packs and timing information from both CLKGN circuit packs. The SWIO circuit packs provide the input and output stages of the 3-stage switch as follows:
  - — As the input stage, the SWIO circuit packs receive traffic-carrying signals (referred to as N-rate signals) from interface modules through N-rate cables (R1 Channel). SWIO circuit packs operate in pairs to protect against SWIO circuit pack failures. An odd-numbered circuit pack receives 16 service N-rate signals from one set of SWIF, SMUX, or MUX circuit packs, and 16 protection N-rate signals from another set of SWIF, SMUX, or MUX, circuit packs. An SWIO circuit pack normally processes and sends only the service signals it receives to the SWCS circuit packs (X1 Channel). However, if an SWIO circuit pack fails, the Main Controller (SCI circuit pack) directs its mate SWIO circuit pack to process both sets of signals and send them to the SWCS circuit packs. The 32 N-rate signals handled by the SWIO circuit pack in this protection operation contain 480 1.728 Mbits/sec tributaries (32 x 15) capable of directing each of these signals to a different destination. The SWIO circuit pack contains a 480 x 480 switch matrix.

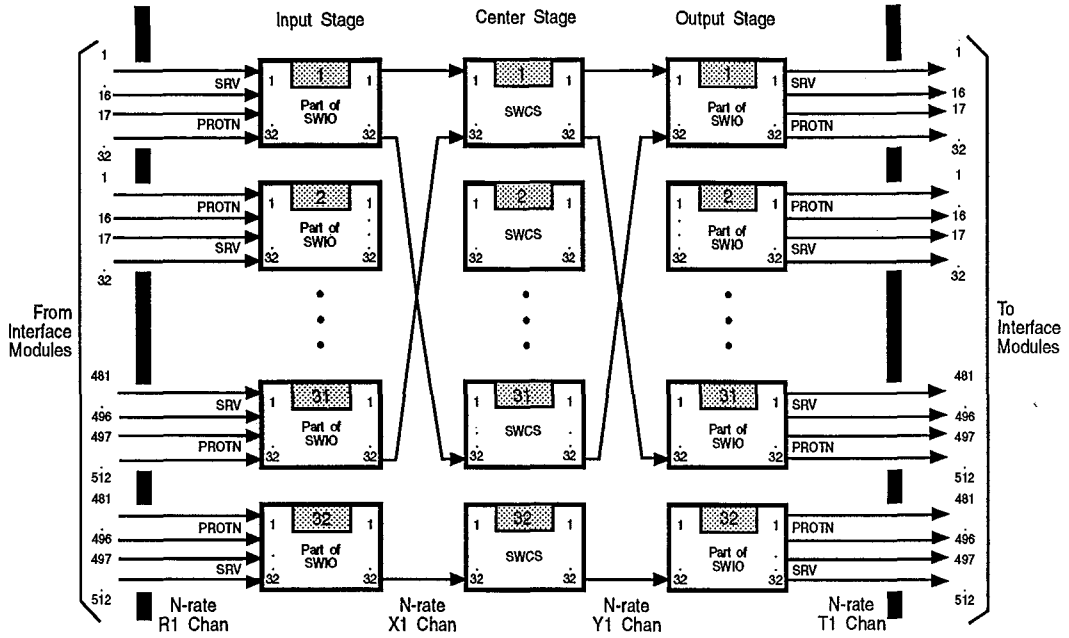
    Each SWIO circuit pack has 32 output ports, one connected to an input port on each of the 32 SWCS circuit packs. These connections form the X1 Channel to the switch center stage.
  - — As the output stage, the SWIO circuit packs receive cross-connected signals from the SWCS circuit packs (Y1 Channel). They then send them to the interface modules through the N-rate cables (T1 Channel). The switch in the output portion of an SWIO circuit pack has the same capacity as the one in the input portion.




**Notes:**
CLK Sel = Clock select
Sync Sel = N-rate synchronizer select

### Timing/Synchronization and Control

Figure 3-18. **Switch Module Block Diagram (Sheet 1 of 2)**




**Notes:**
SRV - Service
PROTN - Protection
Chan - Channel

**3-Stage Nonblocking Space Switch Matrix**

Figure 3-18. **Switch Module Block Diagram (Sheet 2 of 2)**

Both the incoming and outgoing signals handled by an SWIO circuit pack are switched to protection if either the input or output portion of the circuit pack fails. Service and protection signals are fed to pairs of SWIO circuit packs to provide 1 to 1 redundant protection (refer to the section titled "Switch Protection Group" in Chapter 2 for additional information on protection). There are 32 SWIO circuit packs in a fully loaded Switch Module. If fewer than 32 SWIO circuit packs are present, AWR-type filler assemblies are inserted into vacant slots.

- Switch Center Stage (SWCS) — provides the center stage for the cross-connect network. The SWCS receives timing and error summary information from both CLKGN circuit packs and N-rate signals from the input stage of the SWIO (X1 Channel). The SWCS circuit packs cross-connect the N-rate signals and provides N-rate signals to the output stage of the SWIO (Y1 Channel). The switch capacity of the SWCS circuit packs is the same as the input and output stages of the SWIO circuit packs (that is, 480 x 480). SWCS circuit packs do not function in pairs. SWCS circuit pack

number 32 serves as protection for the other 31 SWCS circuit packs providing protection on a 1 to 31 basis (refer to the section titled "Switch Protection Group" in Chapter 2 for additional information on protection). All SWCS circuit packs must be installed in the Switch Module.

- Clock Generator 3 (CLKGN3) — (for systems that have or will use SONET application) provides the N-rate clock and synchronization signals to the SWIO and SWCS circuit packs. The CLKGN3 circuit pack receives a stable 16.384 MHz clock signal from the Synchronizer Module used as a reference source to generate the N-rate clock (27.648 MHz) and the N-rate synchronizing (123.429 KHz) signals to the SWCS and SWIO circuit packs. In addition, the CLKGN3 circuit pack provides, on a programmable basis, a gapped 123.429 KHz synchronizing (gapped 432nd pulse) signal to the SWIO circuit packs that interface to STS1 Interface Modules of the DACS IV-2000 system. The clock and synchronizing signals also go through the SWIO circuit packs to the CLKDR circuit packs in the interface modules.

  CLKGN3 circuit packs are provisioned as Active and Standby (providing a 1 to 1 protection basis). They can be provisioned to listen to the synchronizer circuit on its own or its mate side. The active and standby CLKGN circuit packs are cross-coupled to minimize the phase skew between the clock sides.

  Each CLKGN3 circuit pack receives a status indicator from its associated DPLL circuit pack in the Synchronizer Module which becomes active when a fault is detected at the synchronizer on the associated CLKGN3 circuit pack side. If necessary, in the event of a failure to a synchronizer and/or CLKGN3 circuit pack, an autonomous switch takes place to activate the standby circuit packs, and alarm reports are generated by the Main Controller.

  If you do not have, or do not intend to upgrade to the SONET application, CLKGN2 circuit packs may be used. The CLKGN2 circuit pack provides the N-rate clock and synchronization signals to the SWIO and SWCS circuit packs. The CLKGN2 circuit pack generates the N-rate clock (27.648 MHz) and the N-rate synchronizing (123.429 KHz) signals to the SWCS and SWIO circuit packs by using a 16.384 MHz clock reference.

  The CLKGN circuit packs provide the SCI (SCI-1 provides control for CLKGN-0 and SCI-2 provides control for CLKGN-1) circuit packs in the Redundant Controller Module with a 6.912-MHz clock. The SCI circuit packs provide the CLKGN circuit packs with a data, address, and status interface to the Main Controller for alarm reporting and provisioning operations.

- AWR-type Filler Assembly—is installed in empty SWIO circuit pack slots to keep out dust and foreign objects and to maintain proper air flow from the fan assembly at the bottom of the Switch Bay.

The Switch Module backplane connects the SWCS and SWIO circuit packs to the printed power, ground, and control buses. The Switch Module is connected to the DS1, DS3, or STS1 Interface Modules by the backplane pin fields and cables associated with each SWIO circuit pack. These cables are referred to as N-rate cables and are designated A through T. As shown in Figure 3-19, Each N-rate cable is associated with an SWIO pair and 16 cables designated J1 through J16. Pin fields for the Redundant Controller Module interface are also provided on the Switch Module backplane. In addition, power and ground lugs are provided for connecting to the +5V and -5V fuse boards and ground lugs in the Switch Power Module. Unequipped SWIO positions are equipped with AWR-type filler assembly (faceplate).

Back View

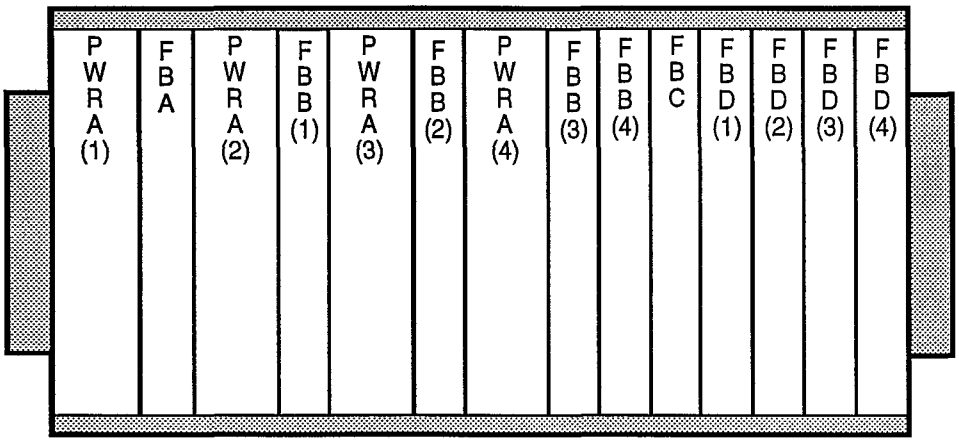
| N-Rate Cable T J1-T - J16-T (32) \| (31) | N-Rate Cable R J1-R - J16-R (30) \| (29) | N-Rate Cable P J1-P - J16-P (28) \| (27) | N-Rate Cable N J1-N - J16-N (26) \| (25) | CLKGN (1) | N-Rate Cable M J1-M - J16-M (24) \| (23) | N-Rate Cable L J1-L - J16-L (22) \| (21) | N-Rate Cable K J1-K - J16-K (20) \| (19) | N-Rate Cable J J1-J - J16-J (18) \| (17) |
|---|---|---|---|---|---|---|---|---|
| | (32) (31) (30) (29) (28) (27) (26) (25) | | | | (23) (22) (21) (20) (19) (18) (17) (16) | | | |
| | (16) (15) (14) (13) (12) (11) (10) (9) | | | | (8) (7) (6) (5) (4) (3) (2) (1) | | | |
| N-Rate Cable H J1-H - J16-H (16) \| (15) | N-Rate Cable G J1-G - J16-G (14) \| (13) | N-Rate Cable F J1-F - J16-F (12) \| (11) | N-Rate Cable E J1-E - J16-E (10) \| (9) | CLKGN (0) | N-Rate Cable D J1-D - J16-D (8) \| (7) | N-Rate Cable C J1-C - J16-C (6) \| (5) | N-Rate Cable B J1-B - J16-B (4) \| (3) | N-Rate Cable A J1-A - J16-A (2) \| (1) |

**Note:** Number in parentheses is circuit pack position number in module.

Figure 3-19. **Cable Designations for Switch Module**

## Switch Power Module

The Switch Power Module provides +5V power for the Switch and Synchronizer Modules and provides -5V fuse boards to distribute the -5V power from the Auxiliary Power Module to the Switch and Synchronizer Modules. Figure 3-20 shows the circuit pack locations in the Switch Power Module. Table 3-7 lists the Switch Power Module circuit packs, their functions, and quantity.




**Note:** Number in parentheses is circuit pack position number in module.

Figure 3-20. **Switch Power Module**

Table 3-7. **Switch Power Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PWRA or<br>PWRA2 | Power A (standard)<br>Power A2 (duplex) | 4<br>4 |
| FBA | Fuse Board A | 1 |
| FBB | Fuse Board B | 4 |
| FBC | Fuse Board C | 1 |
| FBD | Fuse Board D | 4 |

Figure 3-21 is a block diagram of the Switch Power Module. The functions provided by the different circuit packs within the Switch Power Module are summarized below:

- Power A (PWRA) — provides +5V power to the Switch Module and Synchronizer Module. The four PWRA power circuit packs provide the low-voltage power to common busses that are distributed to the DACS IV-2000 system. If a single PWRA power circuit pack fails, the remaining PWRA power circuit packs are sufficient to support low-voltage power to the common busses. Alarm and equipage information is supplied to the MTC circuit pack of the Redundant Controller Module from each PWRA circuit pack.

  Each PWRA circuit pack receives -48V power from one of the Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse and Alarm Panel located in the Switch Bay

- Fuse Board A (FBA) and Fuse Board B (FBB) — these five fuse boards (one FBA and four FBBs) are equipped with 77-type fuses and provide fuse protection for the +5V power supply to the Switch Module and Synchronizer Module.

- Fuse Board C (FBC) and Fuse Board D (FBD) — these five fuse boards (one FBC and four FBDs) are equipped with 78-type fuses and provide fuse protection for the -5V power supply to the Switch Module and Synchronizer Module.

For more information on fuses, refer to the section titled "Fuses" later in this chapter.

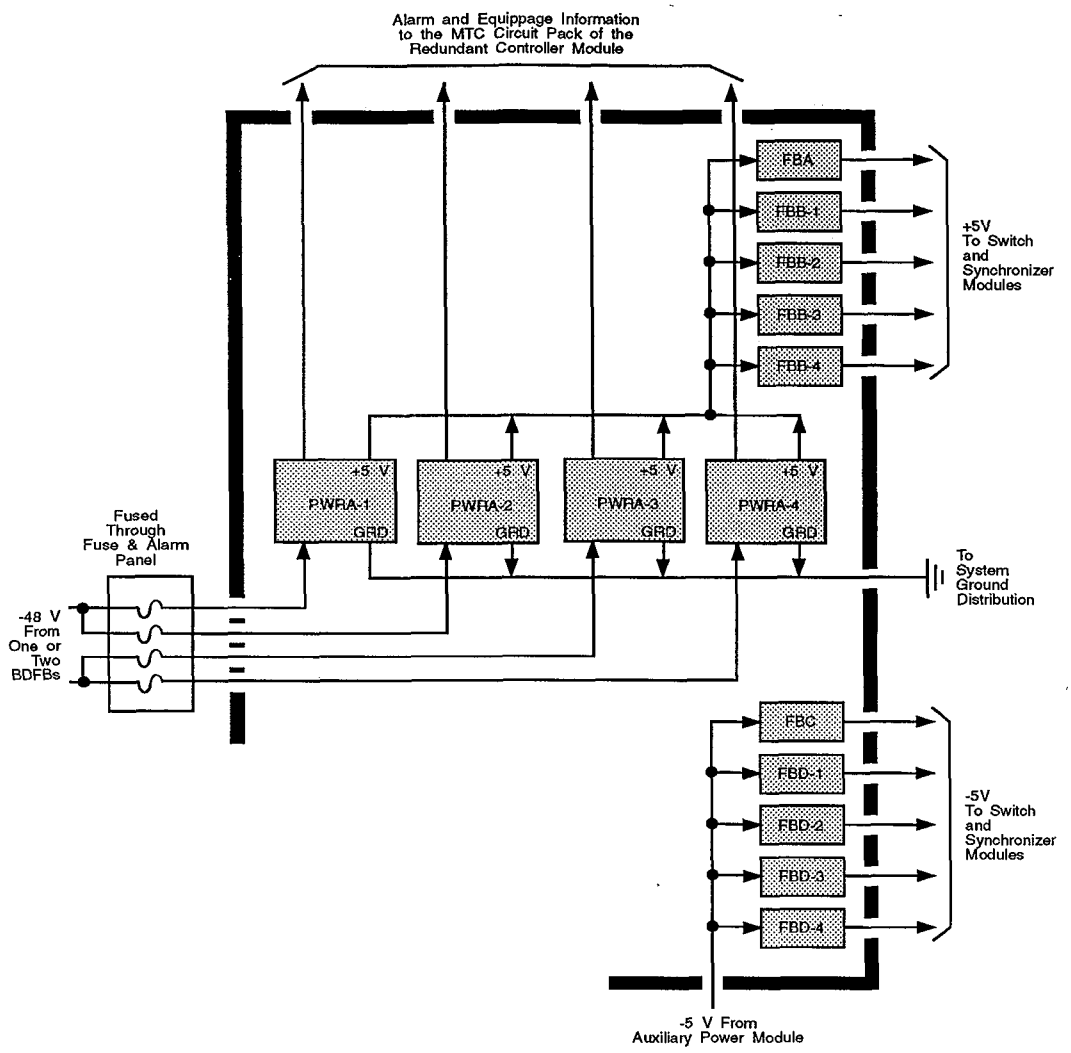
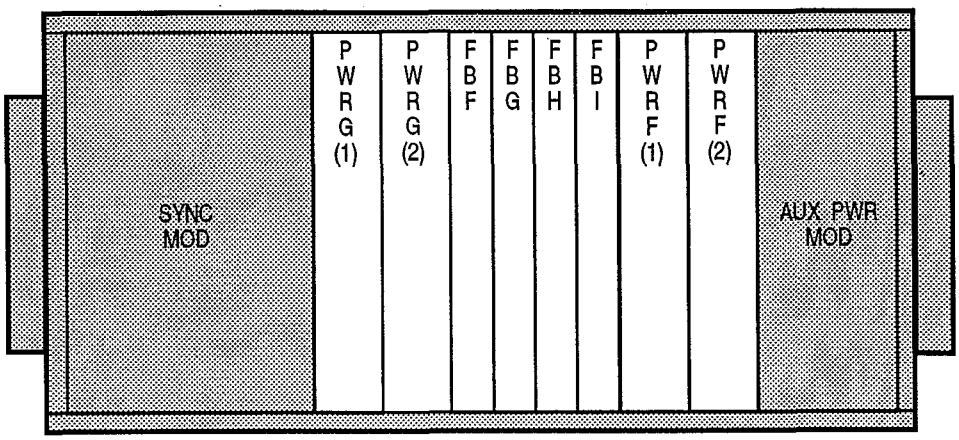



Figure 3-21. **Switch Power Module Block Diagram**

## Redundant Controller Power Module

The Redundant Controller Power Module provides power and fuse protection for the Redundant Controller Module. In addition, this module provides -48V power to the Synchronizer Module. Figure 3-22 shows the circuit pack locations in the Redundant Controller Power Module.Table 3-8 lists the Redundant Controller Power Module circuit packs, their functions, and quantity.




**Note:** Number in parentheses is circuit pack position number in module.

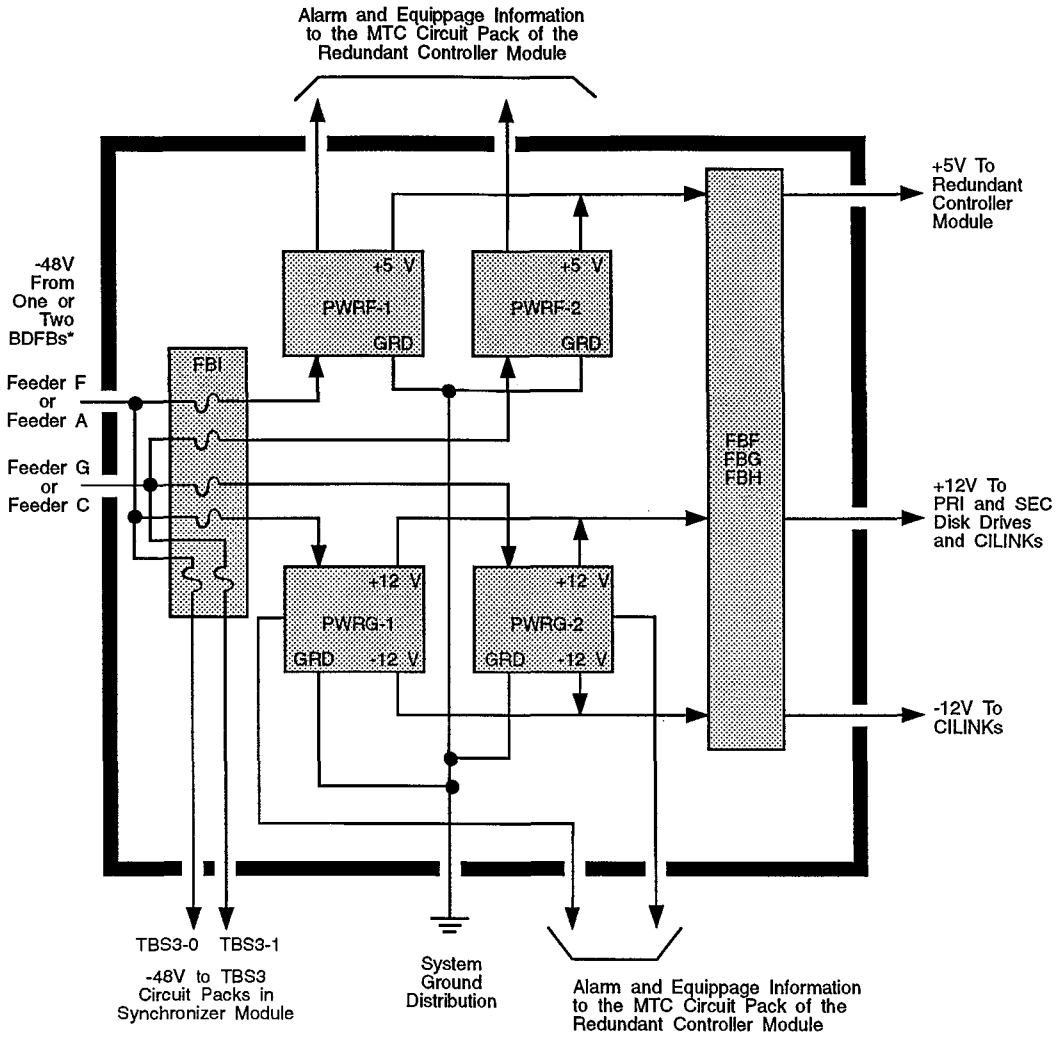
Figure 3-22. **Redundant Controller Power Module**

Table 3-8. **Redundant Controller Power Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PWRF | Power F | 2 |
| PWRG | Power G | 2 |
| FBF | Fuse Board F | 1 |
| FBG | Fuse Board G | 1 |
| FBH | Fuse Board H | 1 |
| FBI | Fuse Board I | 1 |

Figure 3-23 is a block diagram of the Redundant Controller Power Module. The functions provided by the different circuit packs within the Redundant Controller Module Power Module are summarized below:

- Power F (PWRF) — these two power circuit packs receive -48V power fused through FBI and provide +5V to the Redundant Controller Module. Each PWRF circuit pack provides redundant power for its mate circuit pack. Alarm and equipage information is supplied to the MTC circuit pack of the Redundant Controller Module from each PWRF circuit pack.
- Power G (PWRG) — these two power circuit packs receive -48V power fused through FBI and provide +12V to the PRI and SEC disk drives and +12V and -12V to the CILINKS. Each PWRG circuit pack provides redundant power for its mate circuit pack. Alarm and equipage information is supplied to the MTC circuit pack of the Redundant Controller Module from each PWRG circuit pack.
- Fuse Board F (FBF) — this fuse board provides:
  - 5A fuses for protection of the +5V supply to the CC-0 (CPU-0, MTC-0, SSC-0), ECI-1, circuit packs, and PRI-1 disk drive, and for protection of the +12V supply to the PRI-1 disk drive.
  - 1A fuses for protection of the +12V and -12V supply to the CILINKs (ECI-1 circuit packs).
- Fuse Board G (FBG) — this fuse board provides:
  - 5A fuses for protection of the +5V supply to the CC-1 (CPU-1, MTC-1, SSC-1), ECI-2, circuit packs, and PRI-2 disk drive, and for protection of the +12V supply to the PRI-2 disk drive.
  - 1A fuses for protection of the +12V and -12V supply to the CILINKs (ECI-2 circuit packs).
- Fuse Board H (FBH) — this fuse board provides:
  - 5A fuses for protection of the +5V supply to the SEC optical disk and UI, SCI-1, and SCI-2 circuit packs, and for protection of the +12V supply to the SEC optical disk drive.
  - 2A fuse for protection of the +5V supply to the status panel.
- Fuse Board I (FBI) — this fuse board provides 7.5A load fuses that provide protection for the -48V power supplied by one or both Battery Distribution Feeder Boards (BDFBs). Voltages from the FBI fuse board are distributed to the PWRF and PWRG circuit packs and to the TBS3 circuit packs in the Synchronizer Module.

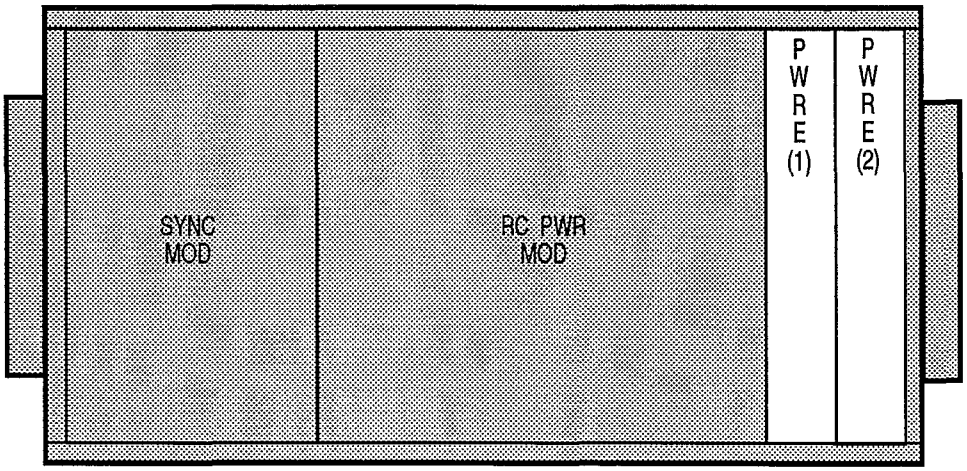



* When using one BDFB, feeders F and G supply power to the RC Power Module. When using two BDFBs, feeders A (fuse A1) and C (fuse C1) supply power to the RC Power Module. If fuse A1 fails, -48V power to PWRF-1, PWRG-1, and TBS3-0 (SYNC side 0) is lost. Likewise, if fuse C1 fails, -48V power to PWRF-2, PWRG-2, and TBS3-1 (SYNC side 1) is lost. If the fuse associated with the active SYNC side fails, an autonomous synchronizer switch occurs.

Figure 3-23. **RC Power Module Block Diagram**

## Auxiliary Power Module

The Auxiliary Power Module provides the -5V power for the Switch Module and Synchronizer Module. Figure 3-24 shows the circuit pack locations in the Auxiliary Power Module. Table 3-9 lists the Auxiliary Power Module circuit packs, their functions, and quantity.




**Note:** Number in parentheses is circuit pack position number in module.

Figure 3-24. **Auxiliary Power Module**

Table 3-9. **Auxiliary Power Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| PWRE3 | Power E3 | 2 |

Figure 3-25 shows a detailed block diagram of the Auxiliary Power Module. Power E (PWRE) supplies -5V power to the Switch Module through the -5V 78-type fuses located in the Switch Power Module. Each PWRE circuit pack provides redundant power for its mate circuit pack. Alarm and equipage information is supplied to the MTC circuit pack of the Redundant Controller Module from each PWRE circuit pack.

Each PWRE circuit pack receives -48V power from one of the Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse and Alarm Panel located in the Switch Bay.

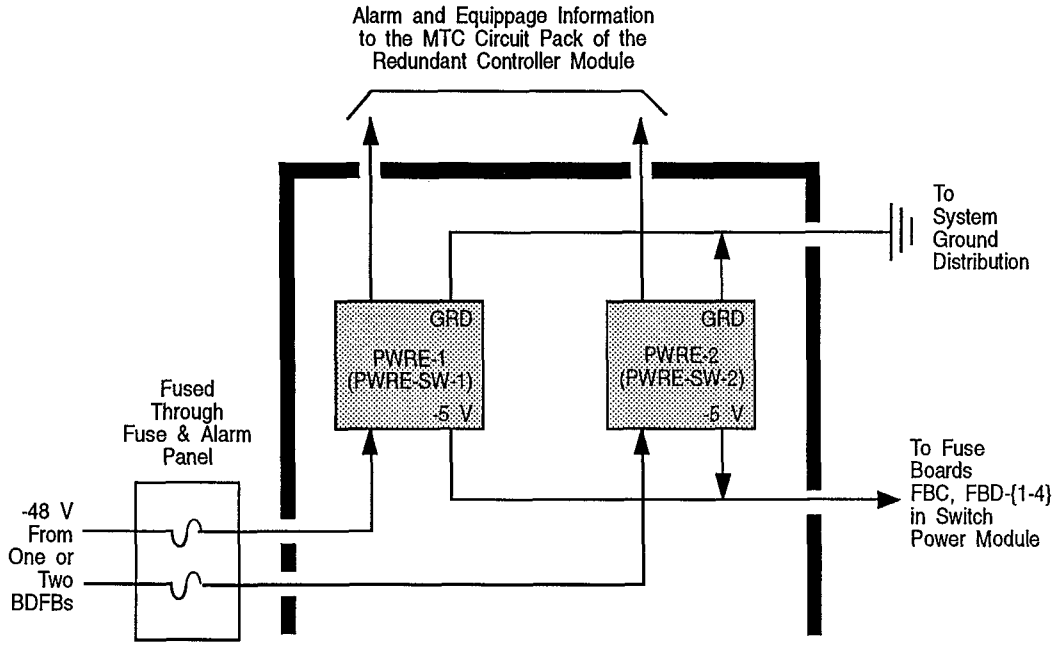
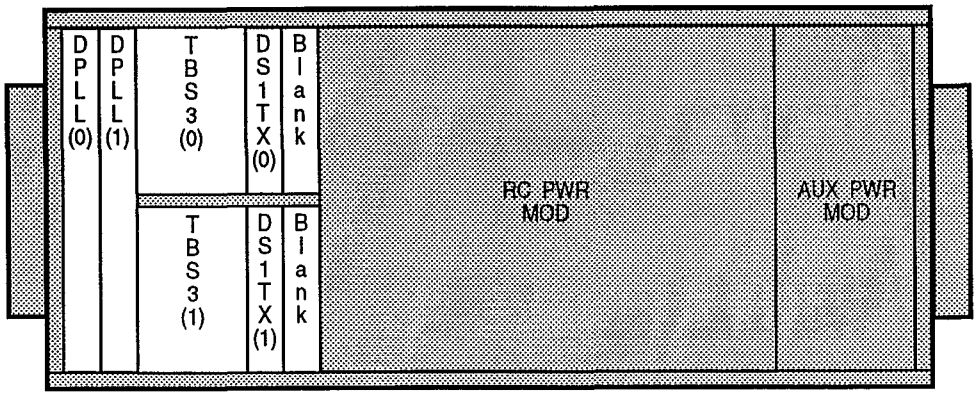



Figure 3-25. **Auxiliary Power Module Block Diagram**

## Synchronizer Module

The Synchronizer Module provides the timing signals to the CLKGN circuit packs in the Switch Module for distribution locally within the switch matrix and to the interface modules within the DACS IV-2000 frame. Figure 3-26 shows the circuit pack locations in the Synchronizer Module. Table 3-10 lists the Synchronizer Module circuit packs, their functions, and quantity.




**Note:** Number in parentheses is circuit pack position number in module.

Figure 3-26. **Synchronizer Module**

Table 3-10. **Synchronizer Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| DPLL1 or DPLL2* | Digital Phase Lock Loop 1 or 2 | 2 |
| DS1TX1 or DS1TX2* | DS1 Timing Extractor 1 or 2 | 2 |
| TBS31 or TBS32* | Stratum 3 Time Base Oscillator 1 or 2 | 2 |
| AWS-type | Blank Filler Assembly | 2 |

* Version 2 circuit packs contain red ALM and green ACT LEDs.

The synchronizer operates in phase-locked mode using one of the two DS1 input references from the Building Integrated Timing Supply (BITS) in the Central Office and has a Stratum 3 holdover capability in the event both of the input references fail. Figure 3-27 is a block diagram of the Synchronizer Module. The functions provided by the different circuit packs within the Synchronizer Module are summarized below:

- DS1 Timing Extractor (DS1TX) — extracts timing information from up to two incoming DS1 reference signals (1.544-MHz ± 12 ppm), designated SYNCPRI and SYNCSEC, and provides line error monitors and phase detector circuitry to enable the DPLL circuit packs to lock their frequency synthesizer circuitry to one of the two 1.544 Mb/s digital links. The line error monitors include a digital interface framer device for monitoring the signal

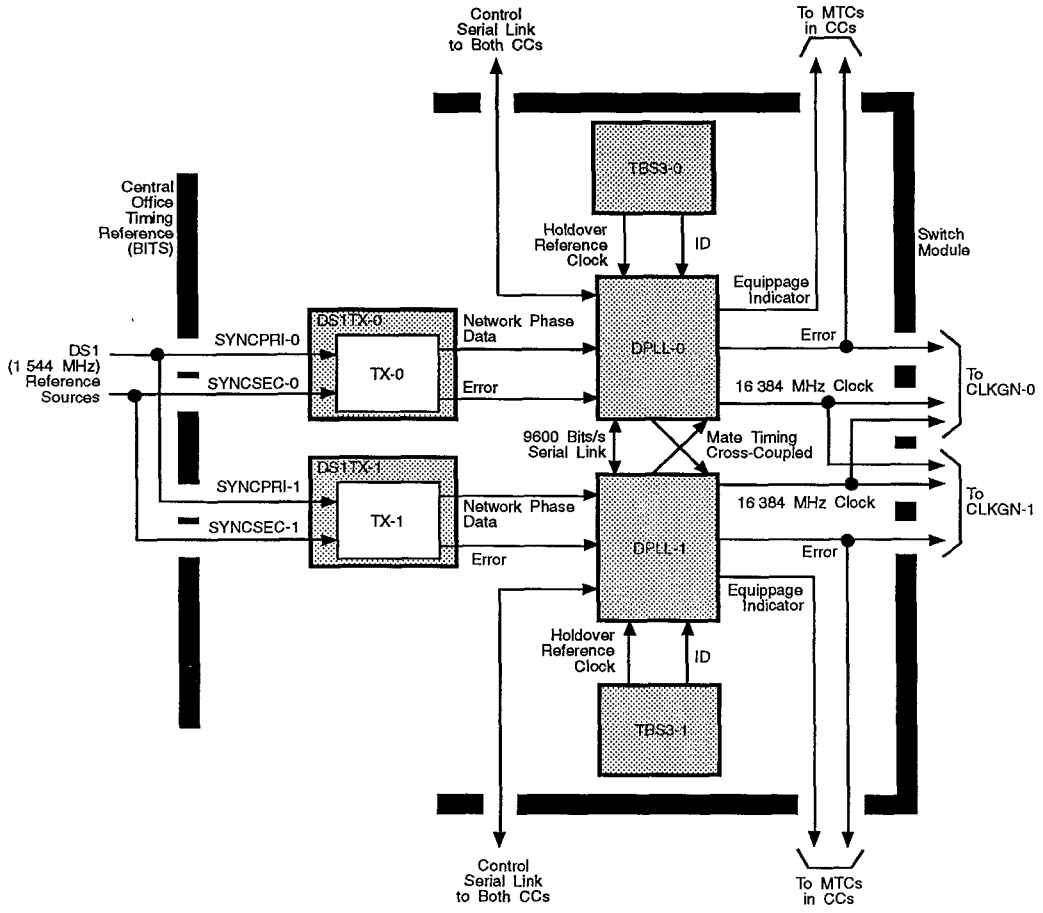



Figure 3-27. **Synchronizer Module Block Diagram**

failure activity (frame alignment, CRC-6, and loss of frame) on each of the two DS1 reference inputs. If an error occurs, the processor on the DPLL circuit pack is interrupted, indicating DS1 reference signal failure. The phase detector circuitry converts the bipolar DS1 signal to a dual-rail, 100% duty cycle, TTL compatible signal and extracts the 1.544-MHz clock. The DS1TX circuit packs can be provisioned to interface with line formats of AMI or B8ZS and framing formats of super frame (SF) or extended super frame (ESF) on a reference basis. Refer to the **ED-EQPT** command in the *DACS IV-2000 (256) Release 4.0 Commands and Messages* manual (AT&T 365-340-702).

- Stratum 3 Time Base Oscillator (TBS3) — contains a precision fixed frequency oscillator and associated circuitry to provide a stable 5 MHz reference frequency, and a low-level communications link to provide the stable reference frequency required by the DPLL circuit packs' frequency synthesizer circuitry to the DPLL circuit packs. When the DPLL circuit pack enters the holdover mode of operation or when the Synchronizer Module is operated in a stand-alone application, the TBS3 circuit packs determine the output clock stability. The TBS3 circuit pack is compatible with the Stratum-3 of the North American Synchronization Network.

  The TBS3 circuit packs and their associated DPLL circuit packs provide the output clock signals. If the TBS3 circuit pack enters an OOS state, its associated DPLL circuit pack enters the OOS-FEF state. After corrective maintenance is performed on the TBS3 circuit pack, both the TBS3 and DPLL circuit packs are put back into service at the same time.

- Digital Phase Lock Loop (DPLL) — receives network phase information that has been derived from reference inputs to the DS1TX circuit packs. The DPLL circuit packs process the phase information to provide the 16.384-MHz master clock (which is synchronized to the digital network) and send timing information to each CLKGN circuit pack in the Switch Module. Both DPLL circuit packs are cross-coupled and phase aligned to the same BITS reference input. The DPLL circuit packs are provided with serial communication links to the Redundant Controller Module (control complex circuitry) and its mate DPLL circuit pack. In addition, the DPLL circuit packs provide alarm and circuit pack installation information (for all equipment associated with the DPLL circuit pack's SYNC side) to the MTC circuit packs in the Redundant Controller Module and alarm information to the CLKGN circuit packs in the Switch Module. The error and circuit pack installation information is used for autonomous switching of circuit packs and/or timing references and alarm reports.

The DPLL circuit packs can operate in one of the following four modes:

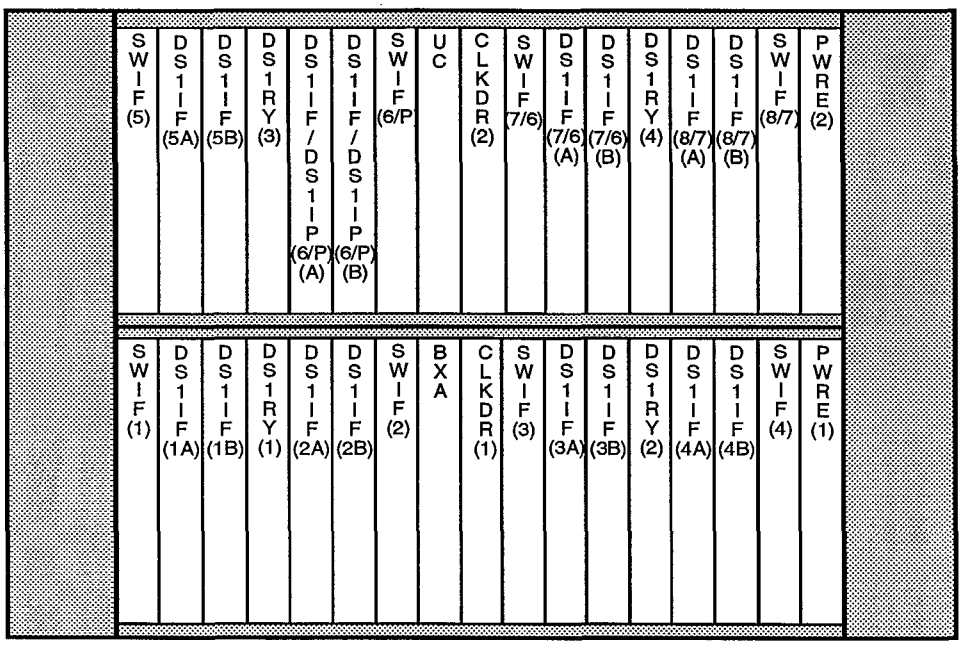
- Normal (steady state condition) — provides for maximum jitter filtering phase-locked to the incoming reference signal
- Fast — provides loop time constraints that allow fast lock to the reference input(s)
- Holdover — is entered when a failure occurs, and the output frequency is maintained at the last known good frequency setting
- Free-Run — fixes the output frequency at a rate that is related to the frequency of the clock reference oscillator.

The DPLL circuit packs and their associated TBS3 circuit packs provide the output clock signals. If the DPLL circuit pack enters an OOS state, its associated TBS3 circuit pack enters the OOS-FEF state. After corrective maintenance is performed on the DPLL circuit pack, both the DPLL and TBS3 circuit packs are put back into service at the same time.

Both DPLL, DS1TX, and TBS3 version 1 and version 2 Synchronizer circuit packs may be used on either Synchronizer side, but all circuit packs must be of the same version on the same side.

## DS1 Interface/Interface-Protection Modules

DS1 interface modules (Figure 3-28) provide the interface for incoming and outgoing DS1 facilities or network elements. These modules accept DS1 signals (in a format that is compatible with a DSX-1) and switch these signals to and from the Switch Module. There are two types of DS1 interface modules, DS1 Interface and DS1 Interface-Protection.




**Note:** Number in parentheses is circuit pack position number on module. For entries with slashes (/), the entry before the slash corresponds to the DS1 Interface Module and the entry after the slash corresponds to the DS1 Interface-Protection Module.

Figure 3-28. **DS1 Interface/Interface-Protection Module**

The DS1 Interface consists of eight working groups, all used for service. The DS1 Interface-Protection consists of eight working groups, seven used for service and one used to provide protection for all working groups within the associated Interface Bay. A DS1 Interface Module must always be connected to a DS1 Interface-Protection Module for protection purposes. The protection group in the DS1 Interface-Protection Module protects the seven working groups in that module along with the eight working groups in the other DS1 Interface Modules that are connected to it. Up to three DS1 Interface Modules can be connected to a DS1 Interface-Protection module for this purpose, giving a maximum protection ratio of 1 to 31.

Table 3-11 lists the circuit packs contained in a DS1 Interface Module; Table 3-12 lists the circuit packs contained in a DS1 Interface-Protection Module.

Table 3-11. DS1 Interface Module Circuit Packs

| Name | Function | Quantity |
|---|---|---|
| UC2 | Unit Controller 2 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| SWIF1 or SWIF2 | Switch Interface 1<br>Switch Interface 2<br>(SWIF2 circuit packs are required for the DS1 performance monitoring option.) | 1 to 8 |
| PMGR1 | Performance Monitor Test Signal Generator Receiver 1<br>(Optional; used for DS1 Performance Monitoring feature and replaces SWIF circuit packs.) | 0 to 8 |
| DS1RY1 | DS1 Relay 1 | 4 |
| DS1IF1 | DS1 Interface 1<br>(Installed in pairs.) | 2 to 16 |
| CLKDR1 | Clock Distributor 1 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped SWIF and DS1IF circuit pack slots of provisioned or non provisioned DS1 Interface Modules associated with a provisioned DS1 Interface-Protection Module.) | 21 to 1 |

Table 3-12. DS1 Interface-Protection Module Circuit Packs

| Name | Function | Quantity |
|---|---|---|
| UC2 | Unit Controller 2 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| SWIF1 or SWIF2 | Switch Interface 1<br>Switch Interface 2<br>(SWIF2 circuit packs are required for the DS1 performance monitoring option.) | 1 to 8 (1 provisioned as SWIF-P) |
| PMGR1 | Performance Monitor Test Signal Generator Receiver 1<br>(Optional: used for DS1 Performance Monitoring feature and replaces SWIF circuit packs.) | 0 to 7 |
| DS1RY1 | DS1 Relay 1 | 4 |
| DS1IF1 | DS1 Interface 1<br>(Installed in pairs.) | 2 to 14 |
| DS1IP1 | DS1 Interface (Protection) 1 | 2 |
| CLKDR1 | Clock Distributor 1 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped SWIF and DS1IF circuit pack slots in a provisioned DS1 Interface-Protection Module.) | 19 to 1 |

The functions of a DS1 Interface Module and the relationship existing in a DS1 protection group (all DS1 Interface Modules contained in a DS1 or STS1/DS3/DS1 Interface Bay), are described in the following sections.

## Timing/Synchronization, Control, and Power

Figure 3-29 is a block diagram of the timing/synchronization, control, and power distribution within a DS1 Interface or DS1 Interface-Protection Module. The functions provided by the different circuit packs are as follows:

Power E (PWRE) — supplies +5V power to the other circuit packs within the associated DS1 Interface Module. Each PWRE circuit pack can supply power for the entire DS1 Interface Module if required due to PWRE circuit pack failure. Error summary information is provided to the MTC circuit packs contained in the main controller. Alarm and power indication LEDs are controlled by the UC circuit pack.

Each PWRE circuit pack is supplied -48V power from one or both Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse and Alarm Panel located in the Switch Bay.

- Unit Controller (UC) — monitors the DS1 Interface Module hardware to detect and isolate faults and to monitor facilities. The UC circuit pack communicates (providing control) with other DS1 interface module circuit packs over 6.176-Mbit/s serial control links. Other inputs to the UC allow for error summary of all circuit packs within the DS1 Interface Module. Outputs from the UC control the LEDs associated with other DS1 Interface Module circuit packs. The UC communicates (system control) with the main controller over the 1-Mbit/s LAN. Software for the UC circuit pack is also downloaded from the main controller (the system disk) over the 1-Mbits/s LAN. The UC provides error summary information to and receives reset signals from the MTC circuit packs contained in the main controller. In addition, the UC provides protection switch control through the DS1IF, DS1IP, and DS1RY circuit packs.

- Clock Distributor (CLKDR) — together with its associated SWIO circuit pack provides N-rate synchronization for the SWIF circuit packs. The CLKDR circuit packs receive N-rate clock (27.648-MHz) and N-rate synchronizing (123.429 KHz) signals from SWIO circuit packs in the Switch Module (over the N-rate cable) and distributes these signals to the SWIF circuit packs. One CLKDR circuit pack provides service timing signals to the eight SWIF circuit packs, and the other CLKDR circuit pack provides protection timing signals to the same eight SWIF circuit packs. In addition, the CLKDR circuit packs reclocks the N-rate clock and synchronizing signals and sends them back to the SWIO circuit packs in the Switch Module (over the N-rate cable).

  A SWIO circuit pack pair (two adjacent SWIO circuit packs, the first odd-numbered and the second even-numbered) provide service for 16 equivalent DS3 signals. DS1 Interface Modules provide for eight DS3 equivalent signals, and DS1 Interface-Protection Modules provide for seven service and one protection DS3 equivalent signals. Therefore, one SWIO circuit pack pair services two DS1 Interface Modules or one DS1 Interface and one DS1 Interface-Protection Modules. Therefore, separate CLKDR circuit packs provide service and protection timing signals to the SWIF circuit packs. In this configuration, two CLKDR circuit packs (one from each DS1 Interface Module) are associated with each SWIO circuit pack, unlike the DS3 and STS1 Interface Modules where only one CLKDR circuit pack is associated with each SWIO circuit pack. CLKDR circuit packs within DS1 Interface Modules do not provide a typical 1to 1 protection arrangement in that two CLKDR circuit packs are used to provide service and protection signals where one CLKDR circuit pack in a DS3 or STS1 Interface Module provides the same capabilities. For DS1 Interface Modules, special care must be taken when performing maintenance on SWIO/CLKDR circuit pack combinations (one SWIO circuit pack and two CLKDR circuit packs).

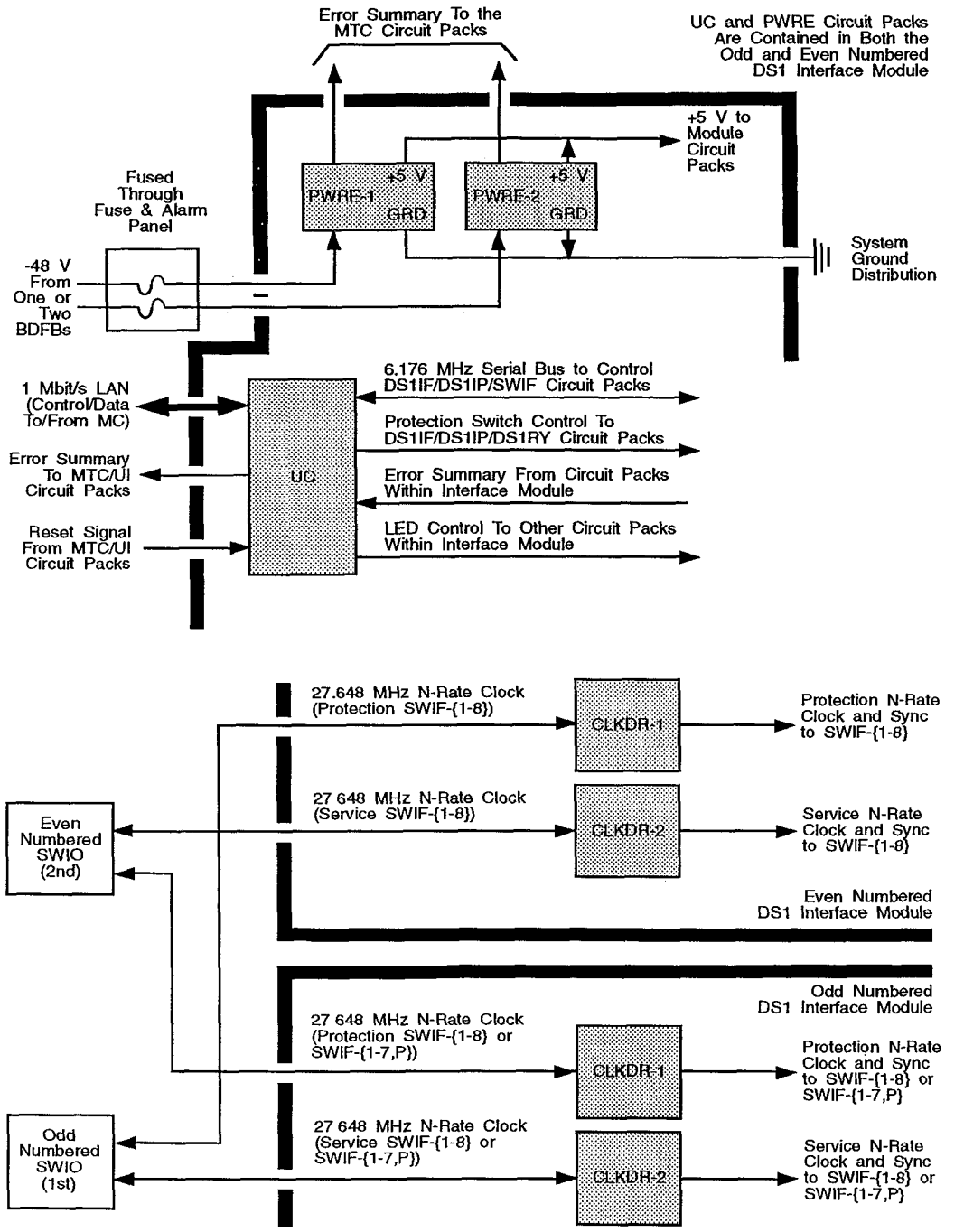



Figure 3-29. DS1 Interface Module Block Diagram (Control)

The bottom half of Figure 3-29 shows the timing signal distribution from the SWIO circuit pack pair to the CLKDR circuit packs of the two adjacent DS1 Interface Modules (the bottom one is odd-numbered and the top one is even-numbered). Under normal conditions (no failures or protection switches), the odd-numbered DS1 Interface Module's N-rate signals and CLKDR-2 is serviced by the odd-numbered SWIO circuit pack (1st). The even-numbered DS1 Interface Module's N-rate signals and CLKDR-2 is serviced by the even-numbered SWIO circuit pack (2nd). The SWIF circuit packs within a DS1 Interface Module normally receive timing from CLKDR-2. The odd-numbered SWIO circuit pack provides protection timing signals to the even-numbered DS1 Interface Module's CLKDR-1 circuit pack, and the even-numbered SWIO circuit pack provides protection timing signals to the odd-numbered DS1 Interface Module's CLKDR-1 circuit pack.

If, for example, the odd-numbered SWIO circuit pack is unable to provide service for any reason, all service in the odd-numbered DS1 Interface Module is switched to the even-numbered SWIO circuit pack. In this case, the even-numbered SWIO circuit pack is carrying the service (16 service DS1 groups or 15 service DS1 groups and 1 DS1 protection group) for both DS1 Interface Modules. At the same time, CLKDR-2 of the odd-numbered DS1 Interface Module no longer provides timing. Instead CLKDR-1 provides the timing. The opposite is true if the even-numbered SWIO circuit pack is unable to provide service.

Table 3-13 lists the CLKDR circuit packs that provide timing (service) to the DS1 Interface Modules, given the status of the associated SWIO circuit packs. If it becomes necessary to replace a CLKDR circuit pack in a DS1 Interface Module, the status of the associated SWIO circuit pack must be determined. If the associated SWIO circuit pack is carrying service (active), manual commands must be entered to switch service to its mate SWIO circuit pack.

Table 3-13. **DS1 Interface Module — SWIO/CLKDR Interworkings**

| SWIO Status | Traffic-Carrying CLKDR Circuit Packs | Standby CLKDR Circuit Packs |
|---|---|---|
| Odd SWIO Active<br>Even SWIO Active | Odd CLKDR-2<br>Even CLKDR-2 | Odd CLKDR-1<br>Even CLKDR-1 |
| Odd SWIO Active<br>Even SWIO Protected | Odd CLKDR-2<br>Even CLKDR-1 | Odd CLKDR-1<br>Even CLKDR-2 |
| Odd SWIO Protected<br>Even SWIO Active | Odd CLKDR-1<br>Even CLKDR-2 | Odd CLKDR-2<br>Even CLKDR-1 |

## Transmission

Figure 3-30 is a block diagram of the transmission paths within a DS1 Interface or DS1 Interface-Protection Module. The functions provided by the different circuit packs are as follows:

- DS1 Interface (DS1IF) — terminates fourteen two-way DS1 signals (1.544-Mbits/s). The format of the DS1 signals can be either alternate mark inversion (AMI) or bipolar with 8-zero substitution (B8ZS), selected on a per-port basis (refer to Chapter 5 in the *DACS IV-2000 (256) Release 4.0 Operations and Maintenance* manual [AT&T 365-340-701] for information on provisioning DS1 facilities). The following blocks are used to process DS1 signals in the receive direction:

  — Digital Signal Interface — receives fourteen DS1 bipolar signals and converts them to unipolar signals. In addition, the DS1 signals are routed to the Protection Relays circuitry. The functions performed are:

    1. Receive fourteen DS1 bipolar signals
    2. Extract clock
    3. Regenerate and retime data
    4. Detect and count bipolar violations (BPVs)
    5. Convert bipolar signals to unipolar signals; decode AMI or B8ZS format
    6. Shutdown clock if there is a loss of incoming signal with no internal loopback (LPBKI) set.

  In addition, provide for DS1 internal loopback (LPBKI, loopback from transmit to receive side) and DS1 line loopback (LPBKL, loopback from receive to transmit side).

  — Protection Relays — connects the DS1IF to the receive side of the DS1RY circuit packs. The DS1RY circuit pack bridges two DS1 interface groups to the DS1 protection bus that is routed to the DS1IP circuit packs. Refer to the next section titled "Protection Bus" for more information.

  — Line Codec and 46.32-MHz Reference Clock — receives fourteen DS1 unipolar signals from the Digital Signal Interface and modifies and outputs signals to the SWIF circuit pack. The functions performed are:

    1. Receive fourteen unipolar DS1 signals from the Digital Signal Interface circuitry
    2. Detect loss-of-clock (LOC)
    3. Autonomously insert AIS signal during an LOC condition
    4. Insert test data (1011000) toward the SWIF circuit pack

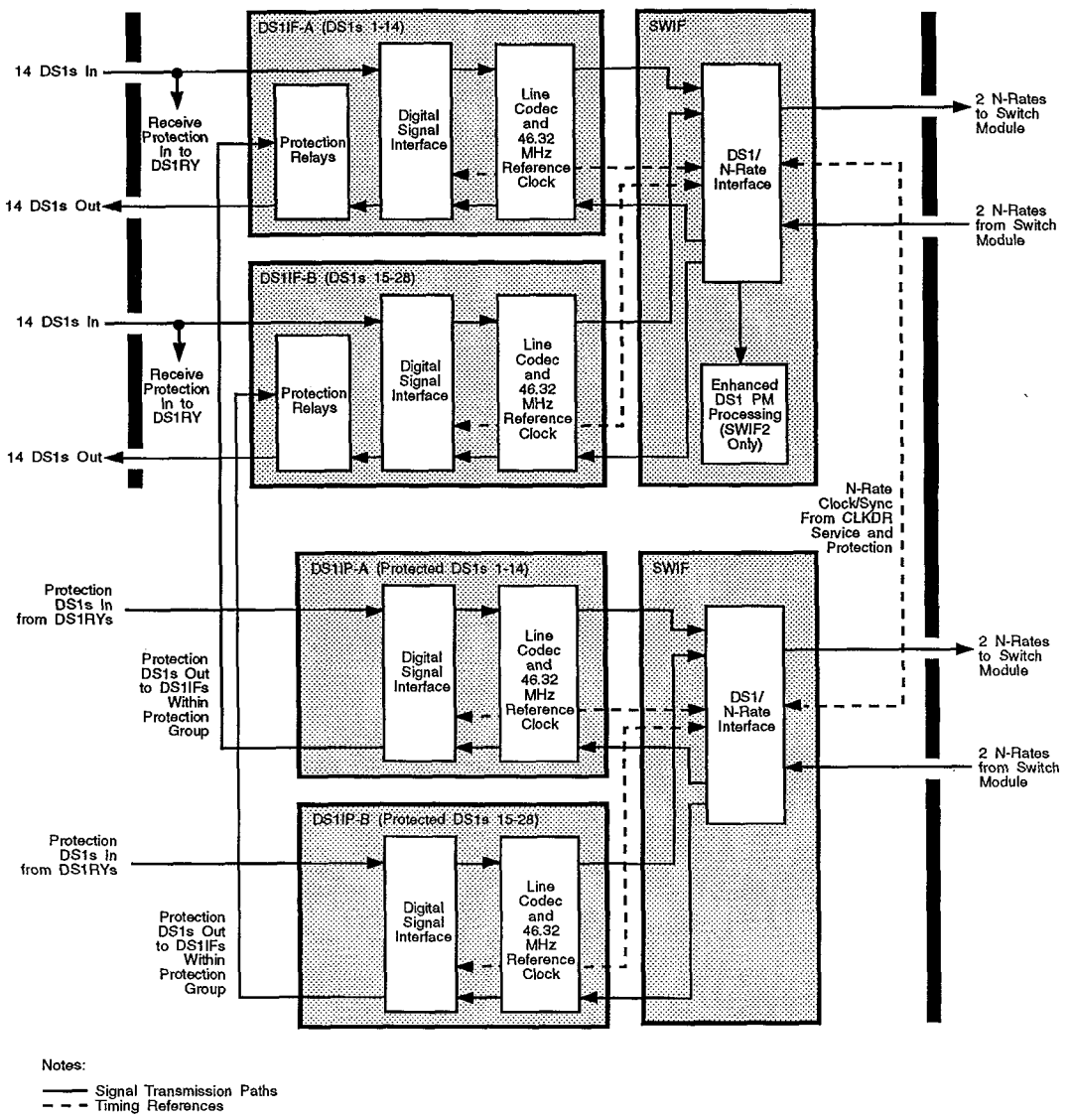



Figure 3-30. **DS1 Interface Module Block Diagram (Transmission Paths)**

5. Detect test data from the Digital Signal Interface circuitry.
6. Detect test data from the Digital Signal Interface circuitry.

The following blocks are used to process DS1 signals in the transmit direction:

— Line Codec and 46.32-MHz Reference Clock — receives fourteen DS1 unipolar signals from the SWIF circuit pack and synchronizes the data to the DS1 rate and output to the Digital Signal Interface circuitry. The functions performed are:

1. Receive fourteen unipolar DS1 signals from the SWIF circuit pack
2. Generate 1.544-MHz DS1 clock to synchronize data to the DS1 rate
3. Detect loss-of-clock (LOC)
4. Detect loss-of-data (AMI mode only)
5. Detect test data (1011000) from the SWIF circuit pack
6. Insert AIS signal, if provisioned to do so
7. Autonomously insert AIS signal during an LOC condition
8. Autonomously insert AIS signal during a loss-of-data condition in the AMI mode.

— Digital Signal Interface — receives fourteen DS1 bipolar signals and converts them to unipolar signals. In addition, the DS1 signals are routed to the Protection Relays circuitry. The functions performed are:

1. Receive fourteen unipolar DS1 signals from the Line Codec and 46.32-MHz Reference Clock circuitry
2. AMI or B8ZS coding (software controlled or through hardware switches)
3. Equalize output waveform to meet the DS1 template specification (software controlled or through hardware switches)
4. Convert unipolar signal to bipolar signal
5. Provide for DS1 internal loopback (LPBKI, loopback from transmit to receive side) and DS1 line loopback (LPBKL, loop back from receive to transmit side).

— Protection Relays—connects the DS1IF to the transmit side of the DS1RY circuit packs. The DS1RY circuit pack bridges two DS1 interface groups to the DS1 protection bus that is routed to the DS1IP circuit packs. The protection relay determines if the DS1 signals are output from the DS1IF or DS1IP circuit pack. Refer to the next section titled "Protection Bus" for more information.

- Switch Interface (SWIF) — sends and receives N-rate signals (27.648-Mbit/s) to and from the Switch Module. The following blocks are used to process DS1 signals in the receive direction:
  - DS1/N-Rate Interface — multiplexes the 28 DS1 signals into two service and two protection N-rate signals and sends the N-rate signals to the Switch Module. The functions performed are:
    1. Receive 28 DS1 signals from the two associated DS1IF/DS1IP circuit packs and multiplex into 28 N-rate channels on the two N-rate signals
    2. Generate and insert stuff channel parity over the DS1
    3. Generate and embed N-rate parity over the 16-bit N-rate data block
    4. Generate two N-rate balanced signals (upper and lower) and drive both service and protection interfaces
    5. Monitor service and protection N-rate clock
    6. Monitor N-rate sync for the 123-kHz sync information
    7. Monitor and generate DS1 AIS.
  - Enhanced DS1 PM Processing (SWIF2 circuit pack contained in an DS1 interface group only) — processes the information received from the DS1/N-Rate Interface circuitry to allow collection of enhanced DS1 performance monitoring data for dedicated full-time monitoring. No DS1 performance monitoring data is collected for protected DS1 signals.

  The following blocks are used to process DS1 signals in the transmit direction:

  - DS1/N-Rate Interface — demultiplexes the received cross-connected N-rate signals from the Switch Module into 28 DS1 signals. The lower DS1 signals (1-14) are output to the DS1IF/DS1IP circuit pack designated A, and the upper DS1 signals (15-28) are output to the DS1IF/DS1IP circuit pack designated B. The functions performed are:
    1. Receive service and protection balanced CMOS clock and sync from backplane
    2. Monitor service and protection N-rate clock
    3. Monitor service and protection N-rate sync for 123-kHz sync information
    4. Perform N-rate clock and sync protection switching under software control

5. Receive service and protection N-rate data sets (upper and lower) and perform protection switching under software control
6. Monitor service and protection N-rate data inputs for N-rate parity errors
7. Demultiplex N-rate channels to DS1 signals, monitor each DS1 stuff channel parity for errors to maintain cross-connect, and output the lower 14 DS1 signals (1-14) to the DS1IF/DS1IP circuit pack designated A and the upper 14 DS1 signals (15-28) to the DS1IF/DS1IP circuit pack designated B.

- DS1 Interface Protection (DS1IP) — provides protection for DS1IF circuit packs within an interface protection group (that is, all DS1 interface groups within the same interface bay). DS1IP circuit packs perform the same functions as DS1IF circuit packs (except for protection relay and hardware switch functions) when active. In a DS1 Interface Bay, protection for DS1 facilities is provided on a 1 to 31 basis. In a STS1/DS3/DS1 Interface Bay protection for DS1 facilities is provided on a 1 to 15 basis.
- Performance Monitor Generator/Receiver (PMGR) — allows bridged access DS1 performance monitoring. PMGR circuit packs replace SWIF circuit packs (except protection group SWIF). For more information on performance monitoring, refer to the section titled "Performance Monitoring" in Chapter 2 and "DS1 PM Hardware" later in this chapter.

### Protection Bus

Figure 3-31 is a block diagram of the protection bus within a DS1 protection group (that is, all DS1 Interface and DS1 Interface-Protection Modules within a interface bay). The functions provided by the different circuit packs are as follows:

- DS1 Interface (DS1IF) — contain protection relays, which when activated allow for the 14 DS1 signals to be processed by the associated DS1IP circuit pack. The 30 DS1IF circuit packs within a STS1/DS3/DS1 Interface Bay or the 62 DS1IF circuit packs within a DS1 Interface Bay are bridged together in pairs (for example DS1IF-1A/DS1IF-2A and DS1IF-1B/DS1IF-2B) and routed to DS1RY circuit packs (8 in STS1/DS3/DS1 Interface Bays and 16 in DS1 Interface Bays).

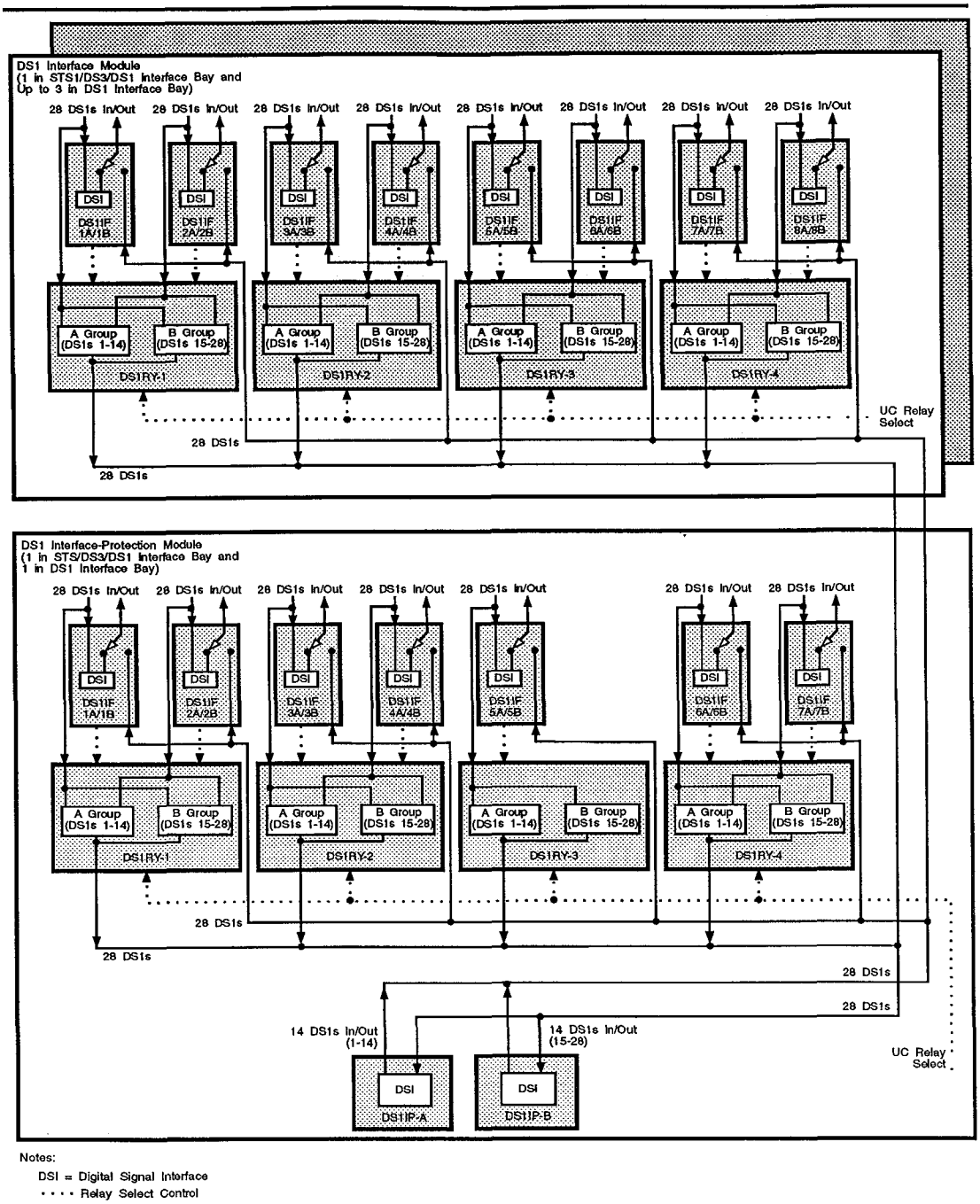



Figure 3-31. **DS1 Interface Module Block Diagram (Protection Bus)**

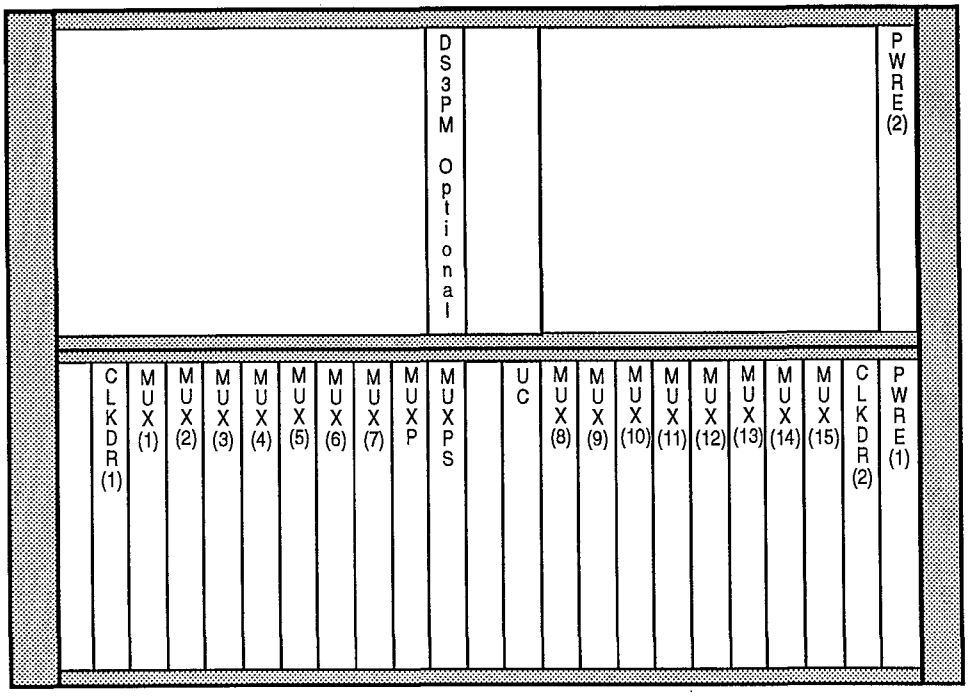
- DS1 Relay (DS1RY) — provides protection relays for two DS1 Interface Groups and routes the DS1 signals to the DS1IP circuit packs. Each DS1RY circuit pack serves two DS1 interface groups. Each of the 56 DS1 signals received by the two interface groups is also bridged to be received by the DS1RY circuit pack. If a DS1IF or a SWIF circuit pack fails, the UC/DS1IF directs the DS1RY circuit pack to send the 28 affected DS1 signals to the protection group and activates the associated protection relays within the DS1IF circuit packs within the failed DS1 interface group allowing the affected DS1 signals to be protected
- DS1 Interface Protection (DS1IP) — provides protection for DS1IP circuit packs within an interface protection group (that is, all DS1 interface groups within the same interface bay). The DS1RY circuit packs are directed to select the appropriate interface group by the UC and/or DS1IF circuit packs when protection for DS1 signals is needed. In a DS1 Interface Bay, protection for DS1/SWIF circuit packs is provided on a 1 to 31 basis. In a STS1/DS3/DS1 Interface Bay protection for DS1/SWIF circuit packs is provided on a 1 to 15 basis.
- Bus Extender A (BXA) — installed in empty DS1IF and SWIF circuit pack slots to provide proper termination of DS1 signals and to keep out dust and foreign matter.

## DS3 Interface-16/Interface-32 Modules

DS3 interface modules provide the interface for incoming and outgoing DS3 facilities or network elements. These modules accept DS3 signals (in a format compatible with a DSX-3) and switch these signals to and from the Switch Module.

The DS3 interface modules are:

- DS3 Interface-16 (INTFC-16) Module — supports 15 MUX circuit packs and one MUXP circuit pack (protection ratio of 1 to 15). Figure 3-32 shows a DS3 Interface-16 module, while Table 3-14 lists its circuit packs.
- DS3 Interface-32 (INTFC-32) Module — supports 31 MUX circuit packs and one MUXP circuit pack (protection ratio of 1 to 31). Figure 3-33 shows a DS3 Interface-32 module, while Table 3-15 lists its circuit packs.




**Notes:**

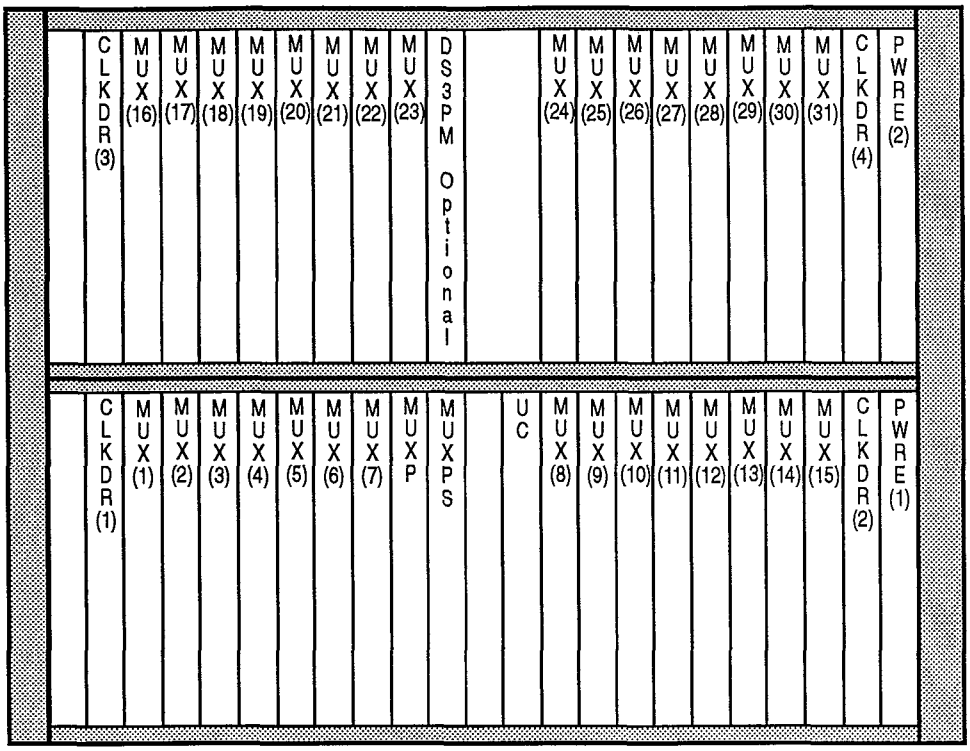
Number in parentheses is circuit pack position number on module.

To implement DS1 performance monitoring features, one to fourteen MUX circuit packs are replaced with PMGR circuit packs. For more information on DS1 performance monitoring configurations, refer to the section titled "DS1 PM Hardware" later in this chapter.

Figure 3-32. DS3 Interface-16 Module

Table 3-14. **DS3 Interface-16 Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC2 | Unit Controller 2 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| MUX1<br>MUX2 | Multiplexer 1<br>Multiplexer 2<br>(MUX2 circuit packs are required for enhanced DS3 performance monitoring and remote multiplexer communications features.) | 1 to 15 |
| PMGR1 | Performance Monitor Test Signal Generator Receiver 1<br>(Optional; used for DS1 Performance Monitoring feature and replaces MUX circuit packs.) | 0 to 14 |
| MUXP1 or MUXP2 | Multiplexer (Protection) 1<br>Multiplexer (Protection) 2 | 1 |
| MUXPS1 | Multiplexer Protection Switch 1 | 1 |
| DS3PM1 | DS3 Performance monitor 1<br>(Optional; used for DS3 Performance Monitoring reporting to GTP.) | 1 |
| CLKDR1 | Clock Distributor 1 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped MUX and DS3PM circuit pack slots. Provides proper termination for the interoffice DS3 signals.) | 15 to 0 |




**Notes:**

Number in parentheses is circuit pack position number on module.

To implement DS1 performance monitoring features, one to sixteen MUX circuit packs are replaced with PMGR circuit packs. For more information on DS1 performance monitoring configurations, refer to the section titled "DS1 PM Hardware" later in this chapter.

Figure 3-33. **DS3 Interface-32 Module**

Table 3-15. **DS3 Interface-32 Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC2 | Unit Controller 2 (Must be inserted into UC circuit pack slots or multiple alarms can occur.) | 1 |
| MUX1<br>MUX2 | Multiplexer 1<br>Multiplexer 2<br>(MUX2 circuit packs are required for enhanced DS3 performance monitoring and remote multiplexer communications features.) | 1 to 31 |
| PMGR1 | Performance Monitor Test Signal Generator Receiver 1<br>(Optional; used for DS1 Performance Monitoring feature and replaces MUX circuit packs.) | 0 to 16 |
| MUXP1 or<br>MUXP2 | Multiplexer (Protection) 1<br>Multiplexer (Protection) 2 | 1 |
| MUXPS1 | Multiplexer Protection Switch 1 | 1 |
| DS3PM1 | DS3 Performance Monitor 1<br>(Optional; used for DS3 Performance Monitoring reporting to GTP.) | 1 |
| CLKDR1 | Clock Distributor 1 | 4 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped MUX and DS3PM circuit pack slots. Provides proper termination for the interoffice DS3 signals.) | 31 to 0 |

The following sections describe the functions of a DS3 Interface Module and the relationship existing in a DS3 protection group (all MUX circuit packs contained in a DS3 Interface-16 or Interface-32 Module).

## Timing/Synchronization, Control, and Power

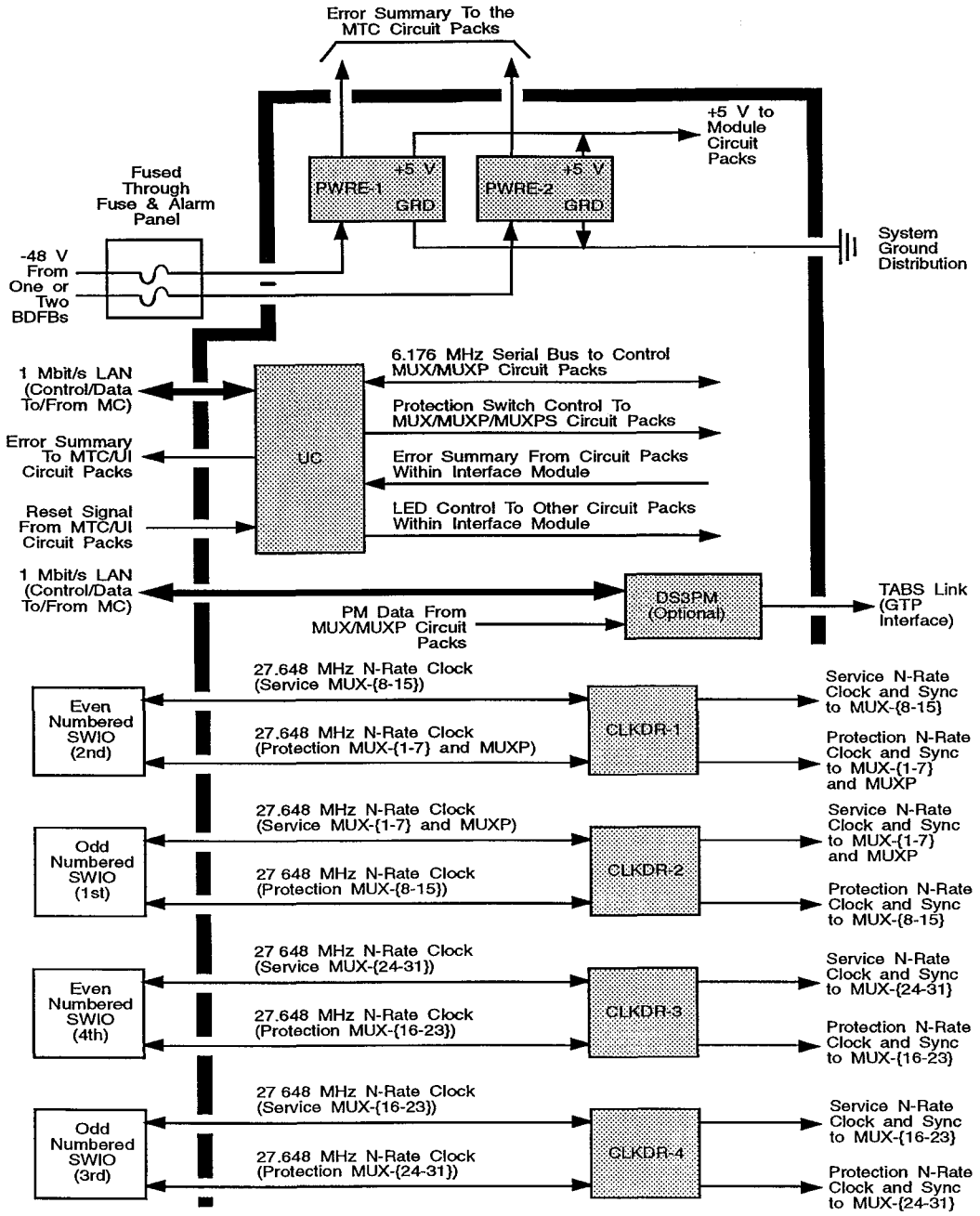
Figure 3-34 shows a detailed block diagram of the timing/synchronization, control, and power distribution within a DS3 Interface-16 or DS3 Interface-32 Module. The functions provided by the circuit packs are as follows:

- Power E (PWRE) — supplies +5V power to the other circuit packs within the associated DS3 Interface Module. Each PWRE circuit pack can supply power for the entire DS3 Interface Module, if required due to PWRE circuit pack failure. Error summary information is provided to the MTC circuit packs contained in the Main Controller. Alarm and power indication LEDs are controlled by the UC circuit pack.

  Each PWRE circuit pack is supplied -48V power from one of two Battery Distribution Feeder Boards (BDFB), which are fuse protected through the Fuse and Alarm Panel located in the Switch Bay.

- Unit Controller (UC) — monitors the DS3 Interface Module hardware to detect and isolate faults and to monitor facilities. The UC circuit pack communicates (providing control) with other DS3 Interface Module circuit packs over 6.176-Bit/s serial control links. Other inputs to the UC allow for error summary of all circuit packs within the DS3 Interface Module. Outputs from the UC control the LEDs associated with other DS3 Interface Module circuit packs. The UC communicates (system control) with the Main Controller over the 1-Mbit/s LAN. Software for the UC circuit pack is also downloaded from the Main Controller (the system disk or optical disk) over the 1-Mbit/s LAN. The UC provides error summary information to, and receives reset signals from, the MTC/UI circuit packs contained in the Main Controller. In addition, the UC provides protection switch control through the MUX, MUXP, and MUXPS circuit packs.

- Clock Distributor (CLKDR) — together with its associated SWIO circuit pack provides N-rate synchronization for the MUX circuit packs. The CLKDR circuit packs receive N-rate clock (27.648-MHz) and N-rate synchronizing (123.429 KHz) signals from SWIO circuit packs in the Switch Module (over the N-rate cable) and distributes these signals to the MUX circuit packs. Two CLKDR circuit packs are used to distribute service and protection timing signals for a DS3 Interface-16 Module and the lower shelf of a DS3 Interface-32 Module. An additional two CLKDR circuit packs are required in a DS3 Interface-32 Module to distribute service and protection timing signals to the upper shelf. Each CLKDR circuit pack distributes service signals to eight MUX/MUXP circuit packs and distributes protection signals to the eight other MUX/MUXP circuit packs within the same shelf. In addition, the CLKDR reclocks the N-rate clock and synchronizing signals and sends them back to the SWIO circuit packs in the Switch Module (over the N-rate cable).




**Note:** CLKDR-3 and CLKDR-4 are contained in DS3 Interface-32 Modules only.

Figure 3-34. **DS3 Interface Module Block Diagram (Control)**

A SWIO circuit pack pair (two adjacent SWIO circuit packs, the first odd-numbered and the second even-numbered) provides service for 16 DS3 signals. DS3 Interface-16 Modules provide 15 service signals and 1 protection DS3 signal and DS3 Interface-32 Modules provide for 31 service signals and 1 protection DS3 signal. Therefore, one SWIO circuit pack pair is needed for a DS3 Interface-16 Module, and two SWIO circuit pairs are needed for a DS3 Interface-32 Module. Therefore, each CLKDR circuit pack provides eight service and eight protection timing signals to MUX/MUXP circuit packs. In this configuration, one CLKDR circuit pack is associated with each SWIO circuit pack (providing for a typical 1to 1 protection arrangement), unlike the DS1 Interface Modules where two CLKDR circuit pack are associated with each SWIO circuit pack. For DS3 Interface Modules, special care must be taken when performing maintenance on SWIO/CLKDR circuit pack pairs.

The bottom portion of Figure 3-34 shows the timing signal distribution from the SWIO circuit pack pairs to the CLKDR circuit packs of a single DS3 Interface-16 or single DS3 Interface-32 Module. Under normal conditions (no failures or protection switches) for both DS3 Interface-16 and DS3 Interface-32 Modules, CLKDR-2 is served by the first odd-numbered SWIO circuit pack (1st) and CLKDR-1 is serviced by the first even-numbered SWIO circuit pack (2nd). In addition, for DS3 Interface-32 Modules, CLKDR-4 is served by the second odd-numbered SWIO circuit pack (3rd) and CLKDR-3 is serviced by the second even-numbered SWIO circuit pack (4th). MUX circuit packs 8-15 normally receive timing from CLKDR-1, and MUX circuit packs 1-7 and the MUXP circuit pack normally receive timing from CLKDR-2. In addition, for DS3 Interface-32 Modules, MUX circuit packs 24-31 normally receive timing from CLKDR-3, and MUX circuit packs 16-23 normally receive timing from CLKDR-4.

If, for example, the 1st SWIO circuit pack is unable to provide service for any reason, all service for MUX 1-7 and MUXP is switched to the 2nd SWIO circuit pack. In this case, the 2nd SWIO circuit pack is carrying the service (15 service MUXs and 1 MUXP) for an entire shelf. At the same time, CLKDR-2 no longer provides timing, but CLKDR-1 provides the timing for the entire bottom shelf of a DS3 Interface Module. The opposite is true if the 2nd SWIO circuit pack is unable to provide service. In a DS3 Interface-32 Module, CLKDR-3 and CLKDR-4 are unaffected by a failure of the 1st or 2nd SWIO circuit pack.

Table 3-16 lists the effects on service for various failures of CLKDR circuit packs in a DS3 Interface-32 Module, and Table 3-17 lists the effects on service for a DS3 Interface-16 Module based on the status of the associated SWIO circuit packs. If it becomes necessary to replace a CLKDR circuit pack in a DS3 Interface Module, the status of the associated SWIO circuit pack must be determined. If the associated SWIO circuit pack is carrying service (active), manual commands must be entered to switch service to its mate SWIO circuit pack.

Table 3-16. DS3 Interface-32 Module — SWIO/CLKDR Interworkings

| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted | CLKDR-3 Circuit Pack Fails or is Extracted | CLKDR-4 Circuit Pack Fails or is Extracted |
|---|---|---|---|---|
| 1st SWIO Active<br>2nd SWIO Active | Service hits on MUX-{8-15} | Service hits on MUX-{1-7} and MUXP | No effect | No effect |
| 1st SWIO Active<br>2nd SWIO Protected | No effect | Service outage on MUX-{1-15} and MUXP | No effect | No effect |
| 1st SWIO Protected<br>2nd SWIO Active | Service outage on MUX-{1-15} and MUXP | No effect | No effect | No effect |
| 3rd SWIO Active<br>4th SWIO Active | No effect | No effect | Service hits on MUX-{24-31} | Service hits on MUX-{16-23} |
| 3rd SWIO Active<br>4th SWIO Protected | No effect | No effect | No effect | Service outage on MUX-{16-31} |
| 3rd SWIO Protected<br>4th SWIO Active | No effect | No effect | Service outage on MUX-{16-31} | No effect |

Table 3-17. DS3 Interface-16 Module — SWIO/CLKDR Interworkings

| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted |
|---|---|---|
| 1st SWIO Active<br>2nd SWIO Active | Service hits on SMUX-{8-15} | Service hits on SMUX-{1-7} and SMUXP |
| 1st SWIO Active<br>2nd SWIO Protected | No effect | Service outage on SMUX-{1-15} and SMUXP |
| 1st SWIO Protected<br>2nd SWIO Active | Service outage on SMUX-{1-15} and SMUXP | No effect |

## Transmission

Figure 3-35 is a block diagram of the transmission path within a DS3 Interface-16 or DS1 Interface-32 Module. The functions provided by the circuit packs are as follows:

- Multiplexer (MUX) — terminates two-way DS3 (44.736-Mbit/s) facilities. The following blocks are used to process a DS3 signal in the receive direction:
  - — Splitter — receives a DS3 bipolar signal and splits the signal by diverting half the power to the DS3 Line Interface circuitry and half the power to the Protection Relay circuitry.
  - — Protection Relays — connects the MUX to the receive protection bus daisy-chain. The receive daisy-chain connects each MUX circuit pack to the MUXP circuit pack through the MUXPS circuit pack. Refer to the next section titled "Protection Bus" for more information.
  - — DS3 Line Interface — extracts clock and converts the 50% duty cycle bipolar DS3 signal, received from the Splitter circuitry, into a 100% duty cycle dual-rail signal. The extracted clock and converted signal is sent to the DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock circuitry.
  - — DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock — demultiplexes the DS3 signal, received from the DS3 Line Interface circuitry into seven DS2 signals and sends the DS2 signals to the DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock circuitry. In addition, the DS3 overhead data is sent to the Overhead/DS3PM Interface circuitry for processing.The functions performed are:
    1. Receive DS3 signal from the DS3 Line Interface circuitry
    2. Code B3ZS and M13 or C-bit parity format; dual-rail to single-rail signal conversion
    3. Detect LOS
    4. Extract DS3 overhead data and send to the Overhead/ DS3PM Interface circuitry.
  - — Overhead/DS3PM Interface — demultiplexes the DS3 overhead and distributes the information for processing. The FEBE, NEBE, AIS, and X-BIT information from the overhead link is demultiplexed and sent to the DS3PM circuit pack and CLINKs in the associated interface module.

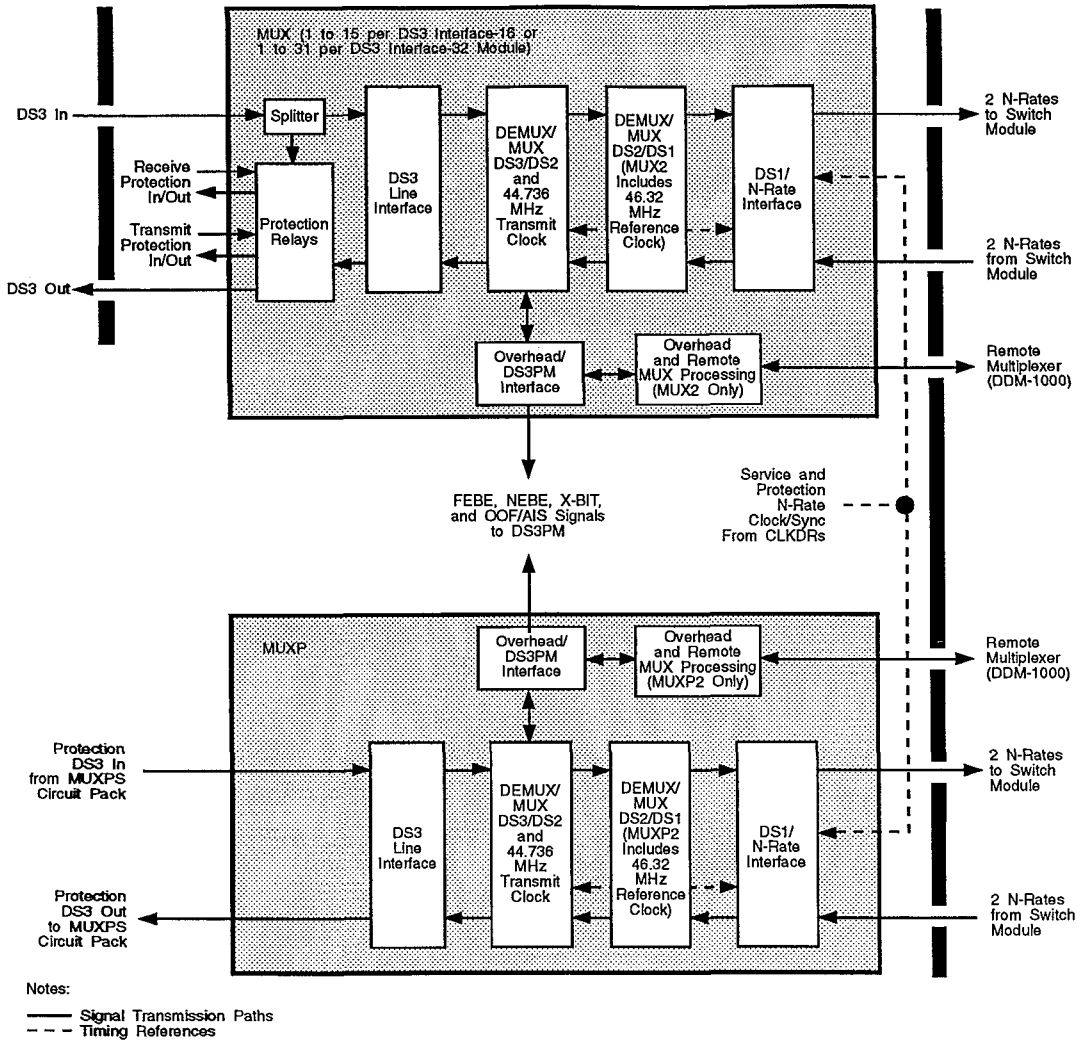



Figure 3-35. DS3 Interface Module Block Diagram (Transmission Paths)

— Overhead and Remote MUX Processing (MUX2 circuit pack only) — processes the information received from the Overhead/DS3PM Interface circuitry to allow collecting enhanced DS3 performance monitoring data and sending the information to a remote multiplexer (for example, the DDM-1000).

— DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock — demultiplexes the seven DS2 signals into 28 DS1 signals. In addition, clock circuitry is provided that is used to source a 1.544-MHz clock used by the DS1/N-Rate Interface circuitry.The functions performed are:

1. Receive seven DS2 signals from the DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock circuitry and demultiplex into 28 DS1 signals
2. Generate 1.544-MHz DS1 reference clock and send to the DS1/N-Rate Interface circuitry.

— DS1/N-Rate Interface — multiplexes the 28 DS1 signals into two service signals and two protection N-rate signals and sends the N-rate signals to the Switch Module. The functions performed are:

1. Receive 28 DS1 signals from the DEMUX/MUX DS2/DS1 and 44.32-MHz Reference Clock circuitry and multiplex into 28 N-rate channels on the two N-rate signals
2. Generate and insert stuff-channel parity over the DS1
3. Generate and embed N-rate parity over the 16-bit N-rate data block
4. Generate two N-rate balanced signals (upper and lower) and drive both service and protection interfaces
5. Monitor service and protection N-rate clock
6. Monitor N-rate sync for the 123-kHz sync information
7. Monitor and generate DS1 AIS.

The following blocks are used to process the two N-rate signals received from the Switch Module in the transmit direction:

— DS1/N-Rate Interface — demultiplexes the received cross-connected N-rate signals from the Switch Module into 28 DS1 signals. The functions performed are:

1. Receive service and protection balanced CMOS clock and sync from backplane
2. Monitor service and protection N-rate clock
3. Monitor service and protection N-rate sync for 123-kHz sync information
4. Perform N-rate clock and sync protection switching under software control
5. Receive service and protection N-rate data sets (upper and lower) and perform protection switching under software control

6. Monitor service and protection N-rate data inputs for N-rate parity errors
7. Demultiplex N-rate channels to DS1 signals, monitor each DS1 stuff channel parity for errors to maintain cross-connect, and output 28 DS1 signals to the DEMUX/MUX DS1/DS1 and 46.32-MHz Reference Clock circuitry
8. Insert DS1 AIS.

— DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock — multiplexes the 28 DS1 signals into seven DS2 signals. In addition, clock circuitry is provided that is used to source a 1.544-MHz clock used by the DS1/N-Rate Interface circuitry.The 28 DS1signals are received from the DS1/N-Rate Interface circuitry and multiplexed into seven DS2 signals

— Overhead and Remote MUX Processing (MUX2 circuit pack only) — processes the information received from the remote multiplexer (if provisioned to do so) and sends the information to the Overhead/ DS3PM Interface circuitry.

— Overhead/DS3PM Interface — multiplexes the DS3 overhead and sends the overhead to the DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock circuitry. The S-BIT data link received from the Overhead and Remote MUX Processing circuitry is multiplexed to the overhead link and sent to the DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock circuitry (MUX2 circuit pack only).

— DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock — multiplexes the seven DS2 signals, received from the DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock circuitry into one DS3 signal and sends the DS3 signal to the DS3 Line Interface circuitry. In addition, clock circuitry is used to generate the 44.736-MHz DS3 clock reference used to generate the DS3 signal for transmission. The functions performed are:

1. Receive seven DS2 signals from the DEMUX/MUX DS2/DS1 and 46.32-MHz Reference Clock circuitry
2. Receive overhead information from the Overhead/DS3PM Interface circuitry
3. Generate the 44.736-MHz DS3 transmit clock
4. Convert single-rail signal to dual-rail signal
5. Encode DS3 signal to M13 or C-bit parity format and B3ZS format
6. Clock duty cycle correction.

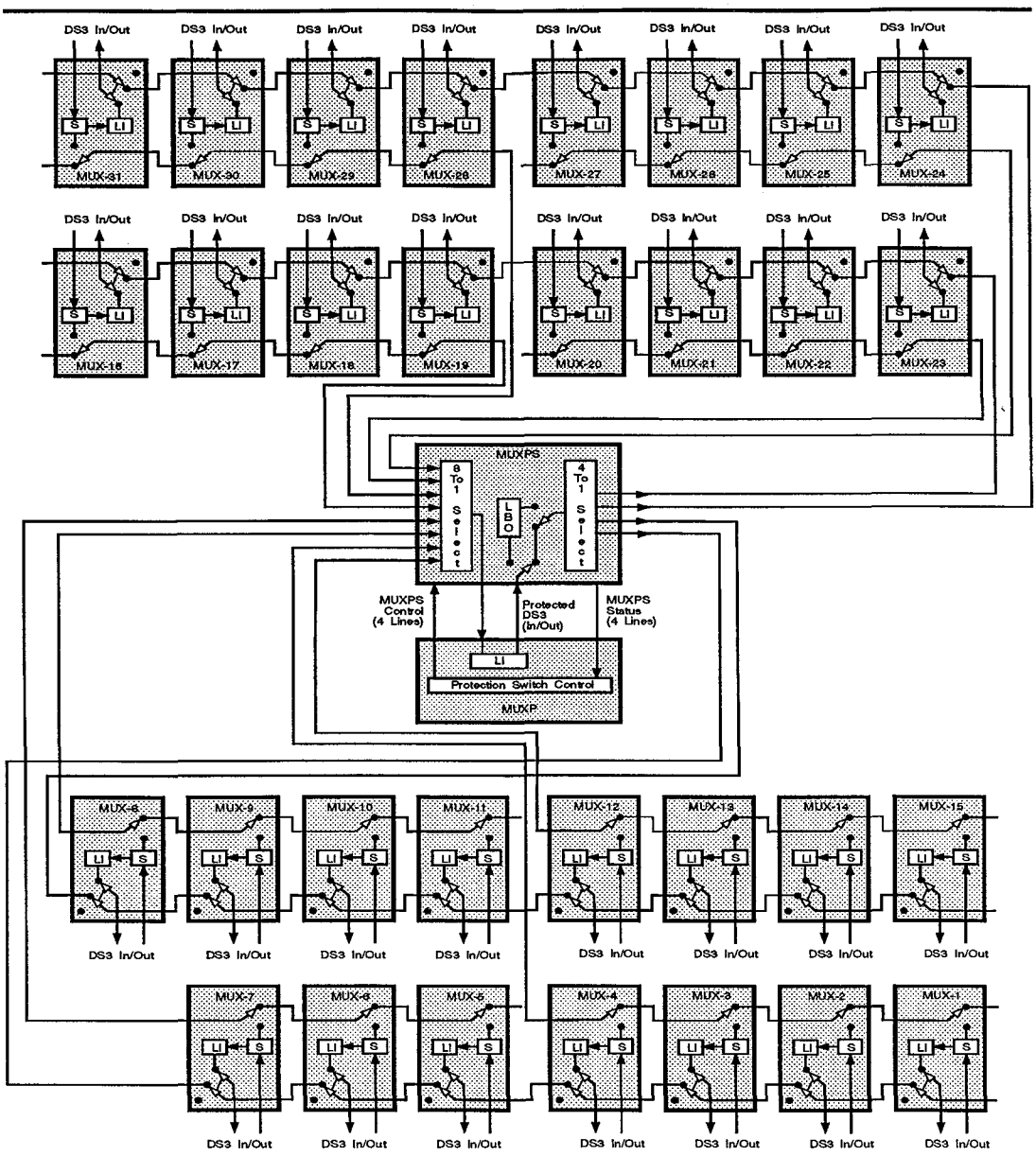
- — DS3 Line Interface — converts the dual-rail signal received from the DEMUX/MUX DS3/DS2 and 44.736-MHz Transmit Clock circuitry into a bipolar DS3 signal. This signal is output directly or through a jumper selectable line buildout (LBO) circuit to the Protection Relays circuitry.
- — Protection Relays — connects the MUX to the transmit protection bus daisy-chain. The transmit daisy-chain connects each MUX circuit pack to the MUXP circuit pack through the MUXPS circuit pack. In addition, the protection relay determines if the DS3 signal is output from the MUX or MUXP circuit pack. Refer to the next section titled "Protection Bus" for more information.

- Multiplexer Protection — provides protection for MUX circuit packs within an interface protection group (that is, all MUX circuit packs within the same interface module). MUXP circuit packs perform the same functions as MUX circuit packs (except for signal splitting and protection relay functions) when active. MUXP circuit packs are hard-wired with the LBO set to OUT (MUXPS has switchable LBO). In a DS3 Interface-32 Module, protection is provided for MUX circuit packs on a 1 to 31 basis. In a DS3 Interface-16 Module, protection is provided for MUX circuit packs on a 1 to 15 basis.
- DS3 Performance Monitor (optional) — collects performance monitoring data on both the incoming and outgoing DS3 signals, and transmits the information over a telemetry asynchronous block serial (TABS) link to an Operations System (OS). The data, obtained only if the DS3 signals are in the C-bit parity format, includes three types of errored seconds, the total of all errored seconds, and an out-of-frame (OOF) count. Each DS3PM circuit pack can handle up to 31 near-end and far-end paths (DS3 equivalent ports). For a full 496 DS3 system, eight DS3PM circuit packs are needed. Up to four DS3PM circuit packs can be connected to a single TABS link. Two TABS links are required for a full 496 DS3 system.
- Performance Monitor Generator/Receiver (optional) — allows bridged access DS1 performance monitoring. PMGR circuit packs replace MUX circuit packs. When inserted, PMGR circuit packs maintain the DS3 protection bus integrity. For more information on performance monitoring, refer to the section titled "Performance Monitoring" in Chapter 2 and "DS1 PM Hardware" later in this chapter.

## Protection Bus

Figure 3-36 is a block diagram of the protection bus within a DS3 protection group (that is, all MUX circuit packs within a DS3 Interface Module). The functions provided by the different circuit packs are as follows:

- Multiplexer (MUX) — contain protection relays, which when activated allow for a DS3 signal to be processed by the MUXP circuit pack. The 15 MUX within a DS3 Interface-16 module or the 32 MUX circuit packs within a DS3 Interface-32 Module are daisy-chained together and routed to the MUXPS circuit pack.
- Bus Extender A (BXA) — is installed in empty MUX circuit pack slots to provide protection bus integrity (that is, maintain the daisy-chain) and to keep out dust and foreign matter.
- Multiplexer Protection Switch(MUXPS) — terminates the receive and transmit protection daisy-chains of the MUX circuit packs and routes the DS3 signals to the MUXP circuit pack. In the receive direction, four groups of MUX circuit packs (DS3 Interface-16 Modules) or eight groups of MUX circuit packs (DS3 Interface-32 Modules) are daisy-chained together and routed to the MUXPS circuit pack. In the transmit direction, two groups of MUX circuit packs (DS3 Interface-16 Modules) or four groups of MUX circuit packs (DS3 Interface-32 Modules) are daisy-chained together and routed to the MUXPS circuit pack. Control from the UC/MUXP circuit packs selects the appropriate groups when necessary. If a MUX circuit pack fails, the UC directs the MUXP and MUXPS circuit packs to send the affected DS3 signal to the MUXP circuit pack and activates the associated protection relays within the failed MUX circuit pack, allowing the affected DS3 signal to be protected The MUXPS LBO setting is determined by the failed MUX circuit pack.
- Multiplexer Protection (MUXP) — provides protection for MUX circuit packs within an interface protection group (that is, all MUX circuit packs within the same interface module). The MUXP circuit pack selects the appropriate daisy-chain group when directed by the UC circuit pack to provide protection for a DS3 signal. Status lines from the MUXPS circuit pack provide state information of the MUXPS circuit pack to the MUXP. In a DS3 Interface-16 Module, the MUXP circuit pack provides protection for MUX circuit packs on a 1 to 15 basis, and in a DS3 Interface-32 Module, the MUXP circuit pack provides protection for MUX circuit packs on a 1 to 31 basis.




**Notes:**

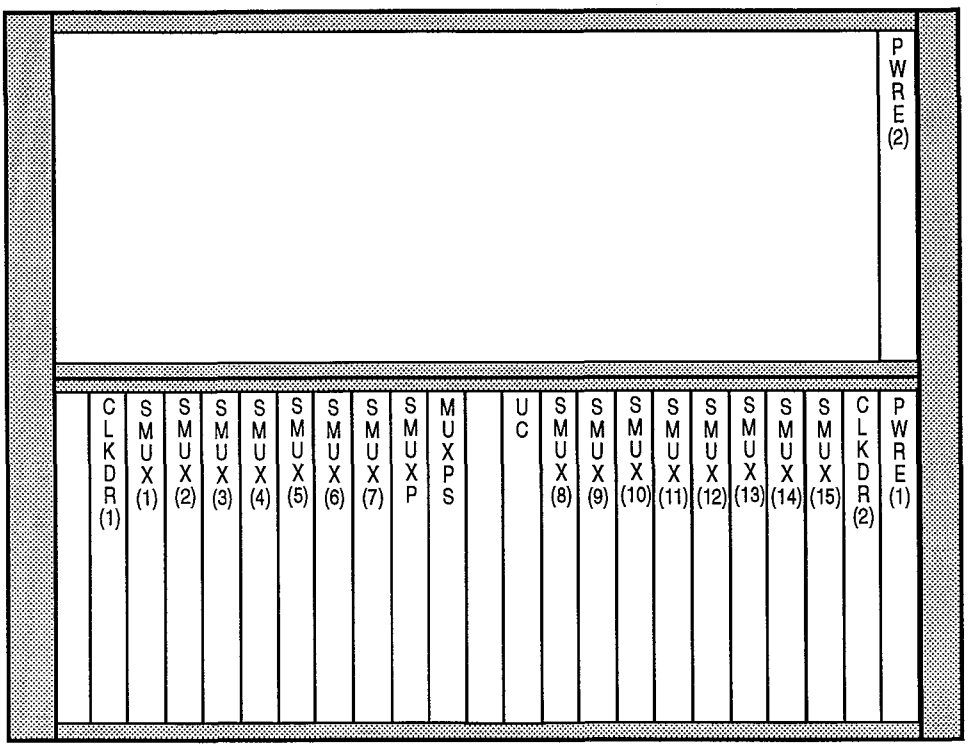
S = Signal Splitter
LI = DS3 Line Interface
LBO = Line Buildout

For DS3 Interface-16 Modules, only four of the receive select lines and two of the transmit select lines of the MUXPS circuit pack are needed. When BXA or PMGR1 circuit packs are inserted for MUX circuit packs, the daisy-chain connectors (receive and transmit paths) are maintained.

Figure 3-36. **DS3 Interface Module Block Diagram (Protection Bus)**

## STS1 Interface-16 Module

STS1 Interface-16 Modules provide the interface for incoming and outgoing EC-1 facilities or network elements. These modules accept STS-1 signals (in a format compliant with the SONET requirements) and switch these signals to and from the Switch Module. Figure 3-37 shows the circuit pack locations in the STS1 Interface-16 Module. Table 3-18 lists the STS1 Interface-16 Module circuit packs, their functions, and quantity.




**Note**: Numbers in parentheses is circuit pack position number on module.

Figure 3-37. **STS1 Interface-16 Module**

Table 3-18. **STS1 Interface-16 Module Circuit Packs**

| Name | Function | Quantity |
|---|---|---|
| UC2 | Unit Controller 2 (must be inserted into UC circuit pack slots or multiple alarms can occur) | 1 |
| SMUX1 | SONET Multiplexer 1 | 1 to 15 |
| SMUXP1 | SONET Multiplexer (Protection) 1 | 1 |
| MUXPS1 | Multiplexer Protection Switch 1 | 1 |
| CLKDR1 | Clock Distributor 1 | 2 |
| PWRE3 | Power E3 | 2 |
| BXA1 | Bus Extender A1<br>(Inserted into unequipped SMUX circuit pack slots.) | 14 to 0 |

The following sections describe the functions of an STS1 Interface-16 Module and the relationship existing in an STS1 protection group (all SMUX circuit packs contained in an STS1 Interface-16 Module).

## Timing/Synchronization, Control, and Power

Figure 3-38 shows a detailed block diagram of the timing/synchronization, control, and power distribution within an STS1 Interface-16 Module. The functions provided by the circuit packs are summarized below:

- Power E (PWRE) — supplies +5V power to the other circuit packs within the associated STS1 Interface-16 Module. Each PWRE circuit pack can supply power for the entire STS1 Interface-16 Module, if required due to PWRE circuit pack failure. Error summary information is provided to the MTC circuit packs contained in the Main Controller. Alarm and power indication LEDs are controlled by the UC circuit pack.

  Each PWRE circuit pack is supplied -48V power from one or both Battery Distribution Feeder Boards (BDFBs), which are fuse protected through the Fuse and Alarm Panel located in the Switch Bay.

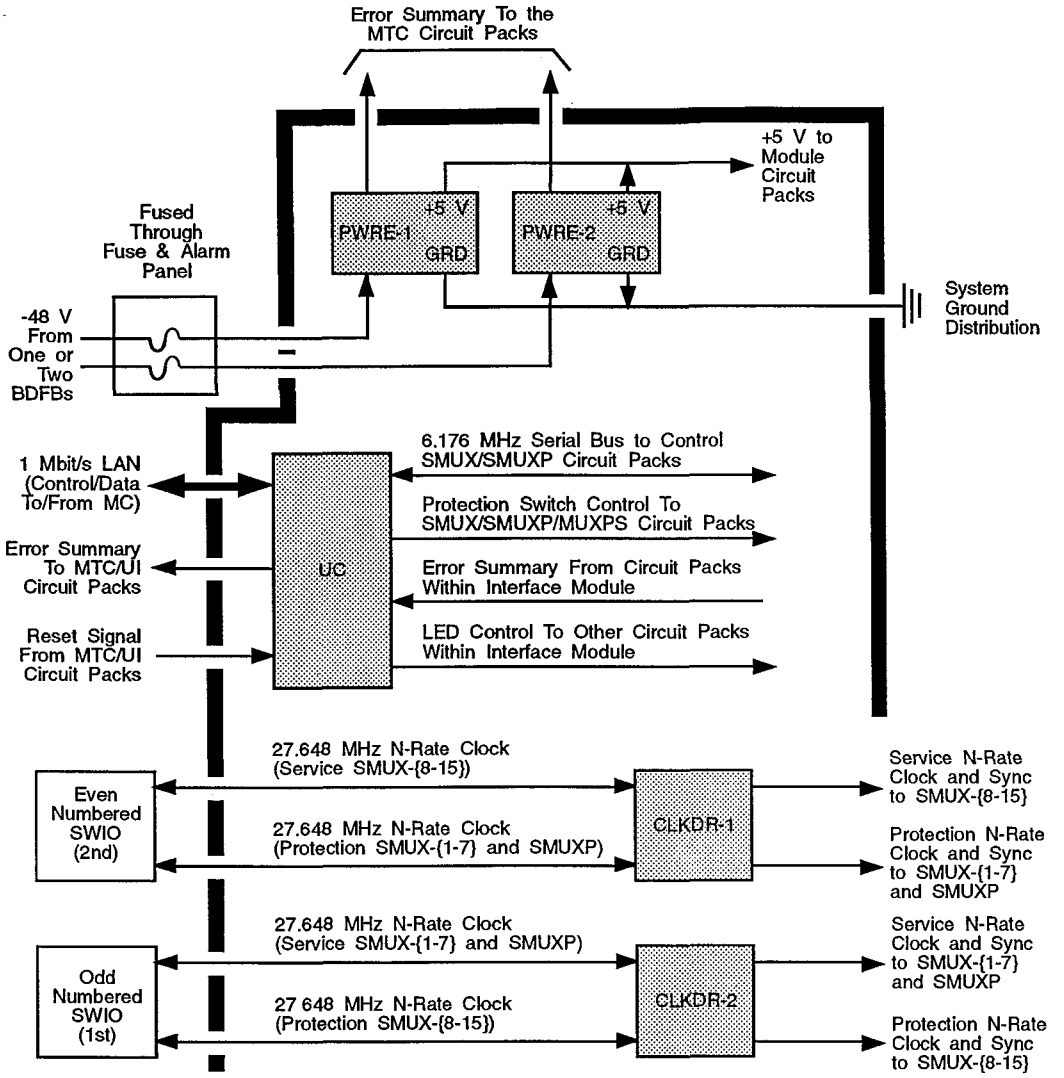



Figure 3-38. **STS1 Interface-16 Module Block Diagram (Control)**

- Unit Controller (UC) — monitors the STS1 Interface-16 Module hardware to detect and isolate faults and to monitor facilities. The UC circuit pack communicates (providing control) with other STS1 Interface-16 Module circuit packs over 6.176-Mbit/s serial control links. Other inputs to the UC allow for error summary of all circuit packs within the STS1 Interface-16 Module. Outputs from the UC control the LEDs associated with other STS1 Interface-16 Module circuit packs. The UC communicates (system control) with the Main Controller over the 1-Mbit/s LAN. Software for the UC circuit

pack is also downloaded from the Main Controller (the system disk or optical disk) over the 1-Mbit/s LAN. The UC provides error summary information to, and receives reset signals from, the MTC/UI circuit packs contained in the Main Controller. In addition, the UC provides protection switch control through the SMUX, SMUXP, and MUXPS circuit packs.

- Clock Distributor (CLKDR) — together with its associated SWIO circuit pack provides N-rate synchronization for the SMUX circuit packs. The CLKDR circuit packs receive N-rate clock (27.648-MHz) and N-rate synchronizing (123.429 KHz) signals from SWIO circuit packs in the Switch Module (over the N-rate cable) and distributes these signals to the SMUX circuit packs. Each CLKDR circuit pack distributes service signals to eight SMUX/SMUXP circuit packs and distributes protection signals to the other eight SMUX/SMUXP circuit packs within an STS1 Interface-16 Module. In addition, the CLKDR reclocks the N-rate clock and synchronizing signals and sends them back to the SWIO circuit packs in the Switch Module (over the N-rate cable).

  A SWIO circuit pack pair (two adjacent SWIO circuit packs, the first odd-numbered and the second even-numbered) provide service for 16 STS-1 signals. STS1 Interface-16 Modules provide 15 service and 1 protection STS-1 signals. Therefore, one SWIO circuit pack pair is needed for an STS1 Interface-16 Module. Therefore, each CLKDR circuit pack provides eight service and eight protection timing signals to the SMUX/SMUXP circuit packs. In this configuration one CLKDR circuit pack is associated with each SWIO circuit pack (providing for a typical 1:1 protection arrangement), unlike the DS1 Interface Modules where two CLKDR circuit pack are associated with each SWIO circuit pack. For STS1 Interface-16 Modules, special care must be taken when performing maintenance on SWIO/CLKDR circuit pack pairs.

  The bottom portion of Figure 3-38 shows the timing signal distribution from the SWIO circuit pack pair to the CLKDR circuit packs of a single STS1 Interface-16 Module. Under normal conditions (no failures or protection switches) for STS1 Interface-16 Modules, CLKDR-2 is served by the odd-numbered SWIO circuit pack (1st) and CLKDR-1 is serviced by the even-numbered SWIO circuit pack (2nd). SMUX circuit packs 8-15 normally receive timing from CLKDR-1 and SMUX circuit packs 1-7 and the SMUXP circuit pack normally receive timing from CLKDR-2.

  If, for example, the odd-numbered SWIO circuit pack is unable to provide service for any reason, all service for SMUX 1-7 and SMUXP is switched to the even-numbered SWIO circuit pack. In this case, the even-numbered SWIO circuit pack is carrying the service (15 service SMUXs and 1 SMUXP) for an entire STS1 Interface Module. At the same time, CLKDR-2 no longer provides timing, but CLKDR-1 provides the timing for the entire STS1 Interface Module. The opposite is true if the even-numbered SWIO circuit pack is unable to provide service.

Table 3-19 lists the effects on service for various failures of CLKDR circuit packs in an STS1 Interface-16 Module based on the status of the associated SWIO circuit packs. If it becomes necessary to replace a CLKDR circuit pack in an STS1 Interface-16 Module, the status of the associated SWIO circuit pack must be determined. If the associated SWIO circuit pack is carrying service (active), manual commands must be entered to switch service to its mate SWIO circuit pack.

Table 3-19. **STS1 Interface-16 Module — SWIO/CLKDR Interworkings**

| SWIO Status | CLKDR-1 Circuit Pack Fails or is Extracted | CLKDR-2 Circuit Pack Fails or is Extracted |
|---|---|---|
| Odd SWIO Active<br>Even SWIO Active | Service hits on SMUX-{8-15} | Service hits on SMUX-{1-7} and SMUXP |
| Odd SWIO Active<br>Even SWIO Protected | No effect | Service outage on SMUX-{1-15} and SMUXP |
| Odd SWIO Protected<br>Even SWIO Active | Service outage on SMUX-{1-15} and SMUXP | No effect |

## Transmission

Figure 3-39 is a block diagram of the transmission paths within an STS1 Interface-16 Module. The functions provided by the circuit packs are as follows:

- SONET Multiplexer (SMUX) — terminates two-way EC-1 (51.840-Mbit/s) facilities. The internal structure of the SMUX circuit packs is defined by the following functional blocks:
  - 51.840-MHz Clock — generates the 51.840-MHz clock used on the SMUX circuit pack. The 51.840-MHz clock is derived from the 27.648-MHz N-Rate clock received from the CLKDR circuit packs. To generate the 51.840-MHz clock, the Transmit N-Rate Interface circuitry divides the 27.648-MHz N-Rate clock to generate a 1.728-MHz reference clock, and receives a buffered version of the 51.840-MHz oscillator output and divides that down to 1.728-MHz. The two generated 1.728-MHz reference signals received by the 51.840-MHz Clock circuitry, are inputted to a phase detector and locked together by a phase lock loop. This locks the 51.840-MHz clock to the selected 27.648-MHz N-Rate clock (that is, the 51.840-MHz clock is totally dependent on the N-Rate clock frequency). Finally, the 51.840-MHz clock is buffered and distributed to the Receive

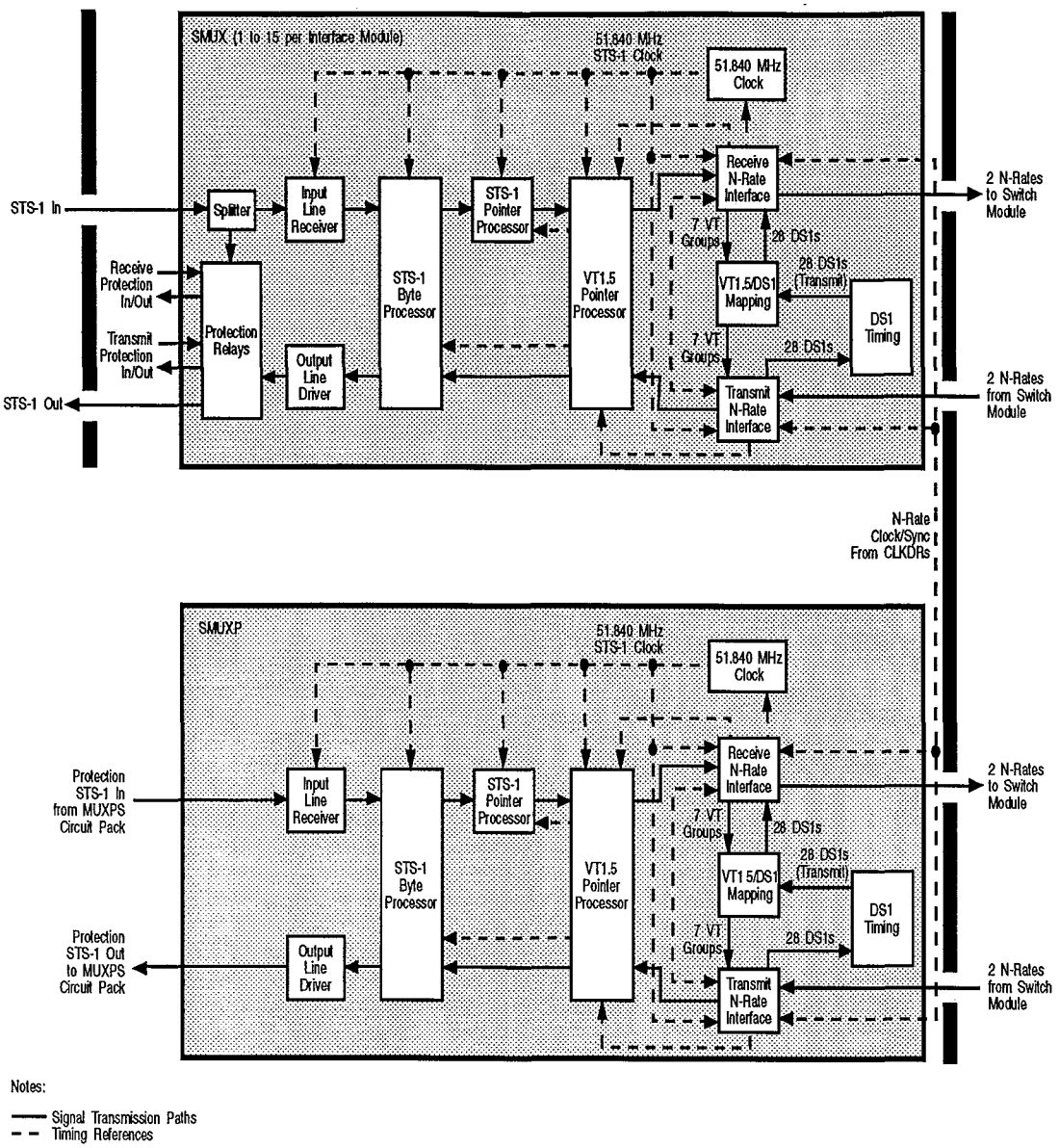



Figure 3-39. **STS1 Interface-16 Module Block Diagram (Transmission Paths)**

and Transmit N-Rate Interface, the VT1.5 Pointer Processor, the STS-1 Pointer Processor, and the STS-1 Byte Processor circuitry. In addition, a single ended 51.840-MHz clock is sent to the Input Line Receiver circuitry as a reference.

The following blocks are used to process an STS-1 signal received from an EC-1 facility in the receive direction:

- Splitter — receives an STS-1 bipolar signal and splits the signal by diverting half the power to the Input Line Receiver circuitry and half the power to the Protection Relay circuitry.
- Protection Relays — connects the SMUX to the receive protection bus daisy-chain. The receive daisy-chain connects each SMUX circuit pack to the SMUXP circuit pack through the MUXPS circuit pack. Refer to the next section titled "Protection Bus" for more information.
- Input Line Receiver — extracts clock and converts the 50% duty cycle bipolar signal into a 100% duty cycle dual-rail signal from the bipolar STS-1 signal received from the Splitter circuitry. The extracted clock and converted signal is sent to the STS-1 Byte Processor circuitry.
- STS-1 Byte Processor — terminates the transport overhead portion of the STS-1 signal. The functions performed are:

    1. B3ZS decoding, dual-rail to single rail signal conversion
    2. LOS detection
    3. STS-1 descrambling
    4. STS-1 A1A2 framing and OOF/LOF detection
    5. B2 parity monitoring
    6. Generate receive path AIS
    7. FERF monitoring
    8. Line AIS detection.

    In addition, when operating an STS-1 line loopback, the transmit output is looped back to the receive input.

- STS-1 Pointer Processor — removes the STS-1 SPE and rebuilds a basic STS-1 frame structure to be output to the VT1.5 Pointer Processor circuitry. The functions performed are:

    1. Receive balanced CMOS line data, sync, and clock from the STS-1 Byte Processor circuitry
    2. Monitor interdevice C1 parity over the incoming Line STS-1 data
    3. Detect and report loss of line clock and sync

4. Detect path AIS
5. Perform STS-1 SPE synchronization through pointer processing
6. Monitor pointer justifications
7. Report New Data Flag (NDF)
8. Build new STS-1 frame including insertion of A1A2 bytes based on the system frame sync received from the VT1.5 Pointer Processor circuitry
9. Generate new H1H2 pointer values based on the system frame sync received from the VT1.5 Pointer Processor circuitry
10. Insert STS-1 path AIS
11. Detect and report loss of system clock and sync.

— VT1.5 Pointer Processor — operates in one of two modes: STS-1 clear or VT1.5 mode.

In the STS-1 clear mode, the incoming STS-1 signal is passed through to the Receive N-Rate Interface unaltered. Path overhead monitoring can take place.

In the VT1.5 mode, the VT1.5 Pointer Processor circuitry performs VT pointer processing analogous to the STS-1 pointer processing done in the STS-1 Pointer Processor circuitry except on the 28 VT1.5 signals embedded in the received STS-1 payload. The functions performed in the VT1.5 mode are:

1. Receive balanced CMOS line data, sync, and clock from the STS-1 Pointer Processor circuitry
2. Monitor interdevice C1 parity over the incoming line STS-1 data
3. Detect and report loss of line clock and sync
4. Detect path AIS
5. Perform STS-1 pointer interpretation to find the STS-1 SPE
6. Terminate STS-1 path overhead
7. Monitor and count B3 parity errors
8. Detect STS-1 path FEBE
9. Generate VT1.5 path AIS on outgoing VT1.5 signals
10. Perform VT1.5 SPE synchronization through pointer processing
11. Monitor VT1.5 pointer justifications

12. Report STS-1 and VT1.5 NDF
13. Build new STS-1 frame including insertion of A1A2 bytes based on system frame sync received from the Receive N-Rate Interface circuitry
14. Generate new H1H2 pointer values based on the system frame sync received from the Receive N-Rate Interface circuitry
15. Insert STS-1 path AIS
16. Detect and report loss of system clock and two 8-kHz sync.

In addition, the VT1.5 Pointer Processor circuitry generates the 1-second Timebase Sync counter used for performance monitoring measurements.

— Receive N-Rate Interface — converts the received signal to two N-rate signals, which are sent to the Switch Module. The Receive N-Rate Interface supports three input signal format modes: STS-1 (cc-SPE), VT1.5(cc-SPE), and DS1. Both service and protection N-rate groups are supported. The Receive N-Rate Interface also performs N-rate clock and sync protection switching and sources switch and cross-connect maintenance information. The functions performed are:

1. Receive balanced CMOS data from the VT1.5 Pointer Processor circuitry
2. Monitor interdevice C1 parity over the incoming STS-1 data
3. Detect and report loss of system 51.840-MHz clock
4. Source two 8-kHz modulated sync clocks to the VT1.5 Pointer Processor circuitry
5. In the STS-1(cc-SPE) mode:
   - Generate CRC-6 over the STS-1 stream and embed in C1 byte to maintain cross-connect integrity through the Switch Module
   - Bit disinterleave serial STS-1 stream and map to 30 of the 32 N-rate channels.
6. In the VT1.5(cc-SPE) and DS1 mode:
   - Demultiplex the STS-1 signal into 28 VT1.5 channels
   - Generate seven 6.912 Mbit/s VT-group signals compatible with the VT1.5/DS1 Mapping circuitry from the 28 VT1.5 channels
   - Output VT-group signals along with VT-group clock and sync to the VT1.5/DS1 Mapping circuitry

- Generate parity over VT-group data.

7. In the VT1.5(cc-SPE) mode:
   - Map individual VT1.5(cc-SPE) signals to individual N-rate channels (this mapping uses up to 28 of the 32 total channels on the two N-rate signals)
   - Generate parity over the VT multiframe and embed in the V4 byte.
8. In the DS1 mode:
   - Receive 28 DS1 signals and map any number to individual N-rate channels (DS1 signals map up to 28 of the 32 total channels on the two N-rate signals)
   - Generate and insert stuff channel parity over the DS1
   - Generate X-bit value to be used for cross-connect maintenance.
9. Generate and embed N-rate parity over the 16 bit N-rate data block
10. Generate two N-rate balanced signals (upper and lower) and drive both service and protection interfaces
11. Monitor service and protection N-rate clock
12. Monitor N-rate sync for both 123-kHz sync and embedded 285 Hz gapped sync information
13. Monitor and generate DS1 AIS

— VT1.5/DS1 Mapping — receives VT-group data signals from the Receive N-Rate Interface circuitry, terminates the VT1.5 path overhead and maps DS1 signals from VT1.5 signals. The functions performed are:

1. Receive VT-group data signal from the Receive N-Rate Interface circuitry
2. Monitor VT-group parity over data
3. Monitor loss of VT-group clock and sync
4. Demultiplex VT-group signal into four VT1.5 signals
5. Perform pointer interpretation on VT1.5 signals to find SPE
6. Terminate VT path overhead
7. Monitor and count VT1.5 BIP-2 parity
8. Monitor for VT FEBE
9. Monitor VT path yellow

10. Detect VT path AIS
11. Extract DS1 from VT SPE
12. Insert DS1 AIS and AIS clock
13. Smooth DS1 data and clock through CMOS DS1 clock and data to the Receive N-Rate Interface circuitry.

The following blocks are used to process the two N-rate signals received from the Switch Module in the transmit direction:

— Transmit N-Rate Interface — converts the received cross-connected N-rate signals from the Switch Module to the STS-1 signal format. The Transmit N-Rate Interface supports three signal format modes: STS-1 (cc-SPE), VT1.5(cc-SPE), and DS1.N-rate data and timing protection switching is performed. The Transmit N-Rate Interface also performs switch and cross-connect maintenance functions and is used as the core timing source (in conjunction with the 51.840-MHz oscillator) for the SMUX circuit pack (that is, generates all internal timing and sync references from the 27.648-MHz service N-rate clock received from the CLKDR circuit packs). The functions performed are:

1. Receive service and protection balanced CMOS clock and sync from backplane
2. Monitor service and protection N-rate clock
3. Monitor service and protection N-rate sync for both 123-kHz sync and 285 Hz gapped sync information
4. Perform N-rate clock and sync protection switching under software control
5. Receive service and protection N-rate data sets (upper and lower) and perform protection switching under software control
6. Monitor service and protection N-rate data inputs for N-rate parity errors
7. In the STS-1(cc-SPE) mode:
   - Bit interleave the two serial N-rate data streams (except for parity bit position) and generate STS-1 signal
   - Generate CRC-6 over the STS-1 stream, compare to embedded value in C1 byte, and monitor for errors to maintain cross-connect integrity through the switch.

8. In the VT1.5(cc-SPE) mode:
   - Map individual N-rate channels to VT1.5(cc-SPE) signals (this mapping uses up to 28 of the 32 total channels on the two N-rate signals)
   - Extract and monitor V4 parity.
9. In the DS1 mode:
   - Demap N-rate channel to DS1 signal, monitor each DS1 stuff channel parity for errors to maintain cross-connect, and output up to 28 CMOS DS1 signals (data and clock) to the DS1 Timing circuitry
   - Monitor stuff channel parity
   - Monitor X-channel for cross-connect maintenance.
10. In the VT.15(cc-SPE) and DS1 modes:
    - Output VT-group clock and sync to the VT1.5/DS1 Mapping circuitry
    - Receive seven 6.912 Mbit/s VT-group signals from the VT1.5/DS1 mapping circuitry and demultiplex each VT-group into four VT1.5 signals
    - Monitor parity over VT-group data and report errors
    - Multiplex 28 VT1.5 channels into STS-1 SPE and build STS-1 frame with H1H2 pointers around the SPE.
11. Generate and insert interdevice C1 parity into STS-1 signal
12. Output balanced CMOS STS-1 data and two 8-kHz sync references to the VT1.5 Pointer Processor circuitry
13. Divide down 51.840-MHz STS-1 system clock from oscillator to 1.728-MHz and output to the Receive N-Rate Interface and 51.840-MHz Clock circuitry
14. Divide down selected service 27.648-MHz N-rate clock to 1.728-MHz reference and output to the Receive N-Rate Interface and 51.840-MHz Clock circuitry
15. Insert DS1 or VT1.5 AIS
16. Insert all zeros DS1.

— DS1 Timing — destuffs the N-rate channel rate to recover the DS1 data. The destuffing process leaves gaps in the DS1 data stream which are removed before converting to a VT1.5 signal. The DS1 Timing circuitry receives gapped data and clock signals from the Transmit N-Rate Interface circuitry, buffers the gapped data, and clocks it out on the smoothed clock to the VT1.5/DS1 Mapping circuitry. Each DS1 Timing half services and performs signal maintenance on 14 DS1 signals. The functions performed are:

1. Receive DS1 clock and data from the Transmit N-Rate Interface circuitry
2. Detect and report loss of DS1 clock on each DS1 input
3. Detect "stuck ats" on DS1 data inputs
4. Perform DS1 clock and data smoothing on each channel
5. Output smoothed DS1 clock and data to the VT1.5/DS1 Mapping circuitry
6. Receive and monitor DS1 test signal.

— VT1.5/DS1 Mapping — receives 28 DS1 data and clock signals from the DS1 Timing circuitry, maps DS1 signals to VT1.5 signals, and generates the VT path overhead. The functions performed are:

1. Receive DS1 clock and data from the DS1 Timing circuitry
2. Monitor and detect DS1 loss of clock
3. Monitor DS1 input
4. Autonomous insertion of DS1 AIS into VT1.5
5. Stuff DS1 and map into VT1.5 SPE
6. Insert VT path overhead
7. Generate BIP-2 parity
8. Insert VT FEBE
9. Insert VT path yellow
10. Generate VT pointers and build a VT1.5 signal based on VT-group sync from Transmit N-Rate Interface circuitry
11. Multiplex four VT1.5 signals into a VT-group serial stream
12. Generate VT-group parity and inset into VT-group serial stream
13. Output VT-group signal to the Transmit N-Rate Interface circuitry.

— VT1.5 Pointer Processor — operates in one of two modes: STS-1 clear or VT1.5 mode.

In the STS-1 clear mode, the incoming STS-1 signal is passed through to the STS-1 Byte Processor circuitry unaltered. Path overhead monitoring can take place.

In the VT1.5 mode, the VT1.5 Pointer Processor circuitry inserts STS-1 path overhead on the STS-1 data received from the Transmit N-Rate Interface circuitry. The functions performed in the VT1.5 mode are:

1. Receive balanced 51.840-Mbits/s data, and two modulated 8-kHz sync references from the Transmit N-Rate Interface circuitry
2. Monitor interdevice C1 parity over the incoming STS-1 data
3. Monitor loss of clock and sync
4. Insert STS-1 path overhead
5. Generate B3 parity
6. Insert STS-1 path FEBE
7. Insert STS-1 path yellow
8. Insert STS-1 path AIS source balanced CMOS 2-kHz sync and data to the Receive N-Rate Interface circuitry with embedded interdevice C1 parity.

In addition the VT1.5 Pointer Processor circuitry generates the one second Timebase Sync counter used for performance monitoring measurements.

— STS-1 Byte Processor — generates the transport overhead portion of the STS-1 signal. The functions performed are:

1. Receive balanced 51.840-Mbits/s data, clock, and sync from the VT1.5 Pointer Processor circuitry
2. Monitor interdevice C1 parity over the incoming STS-1 data
3. Insert A1A2 bytes
4. Insert C1 byte value = 00001111
5. Generate and insert B1 parity
6. Generate and insert B2 parity
7. Generate and insert line FERF
8. Generate path AIS
9. Source APS in K1K2 bytes
10. Pass remaining transport overhead or force to 00000000
11. Scramble STS-1 signal

12. Convert single rail signal to dual-rail signal
13. Encode STS-1 signal to B3ZS format
14. Clock duty-cycle correction.

In addition, when operating an STS-1 line loopback, the receive input is looped back to the transmit output.

— Output Line Driver — converts the dual-rail signal received from the STS-1 Byte Processor circuitry into a bipolar STS-1 signal. This signal is output directly or through a jumper-selectable line buildout (LBO) circuit to the Protection Relays circuitry.

— Protection Relays — connects the SMUX to the transmit protection bus daisy-chain. The transmit daisy-chain connects each SMUX circuit pack to the SMUXP circuit pack through the MUXPS circuit pack. In addition, the protection relay determines if the STS-1 signal is output from the SMUX or SMUXP circuit pack. Refer to the next section titled "Protection Bus" for more information.

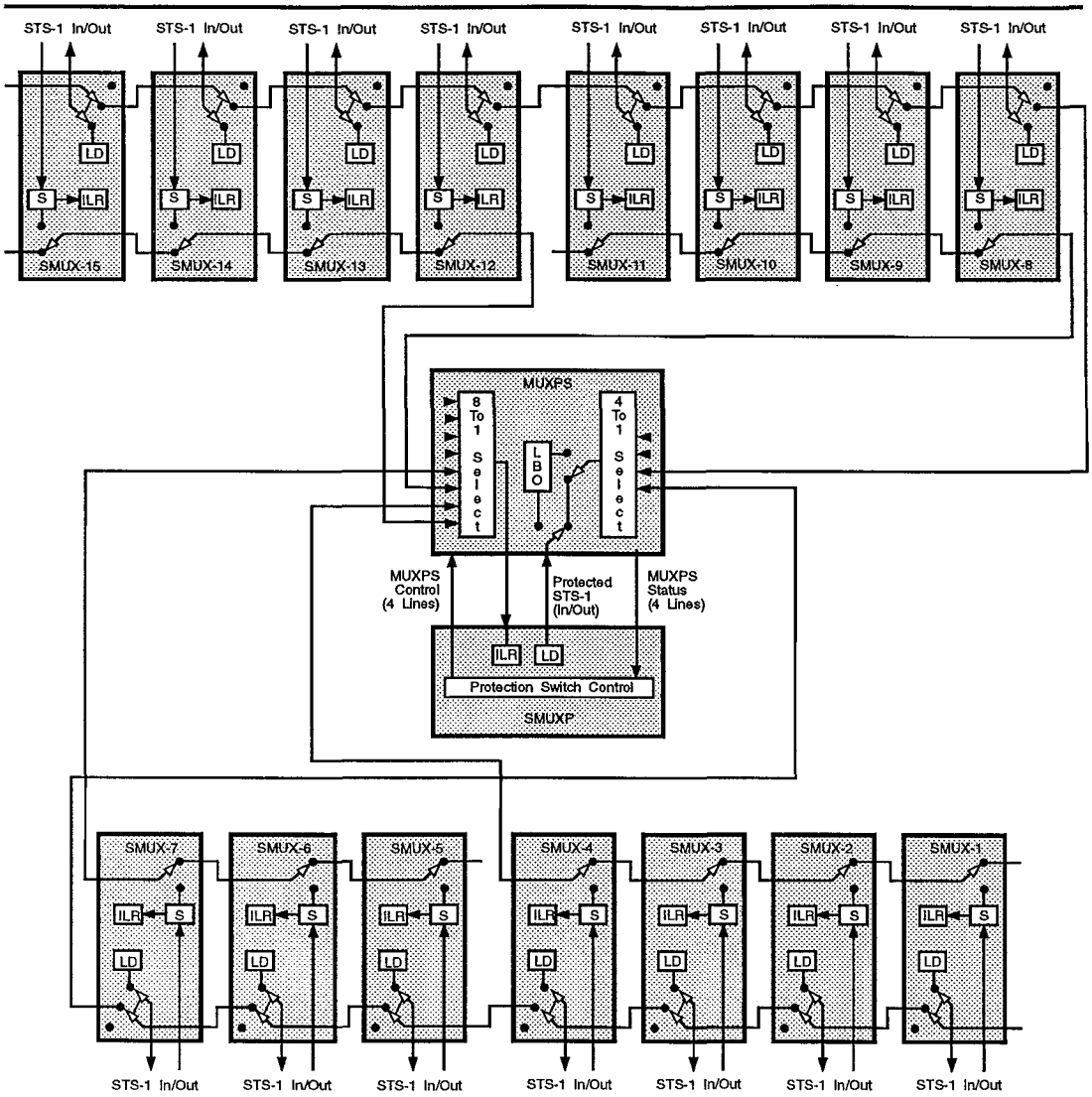
- SONET Multiplexer Protection (SMUXP) — provides protection for SMUX circuit packs within an interface protection group (that is, all SMUX circuit packs within the same interface module). When active, SMUXP circuit packs perform the same STS-1 transmission functions as SMUX circuit packs (except for signal splitting and protection relay functions). In an STS1 Interface-16 Module, protection is provided for STS-1 facilities on a 1 to 15 basis.

## Protection Bus

Figure 3-40 is a block diagram of the protection bus within an STS1 protection group (that is, all SMUX circuit packs within an STS1 Interface-16 Module). The functions provided by the different circuit packs are as follows:

- SONET Multiplexer (SMUX) — contains protection relays, which when activated allow for an STS-1 signal to be processed by the SMUXP circuit pack. The 15 SMUX circuit packs within an STS1 Interface-16 Module are daisy-chained together and routed to the MUXPS circuit pack.
- Bus Extender A (BXA) — is installed in empty SMUX circuit pack slot to provide protection bus integrity (that is, maintain the daisy-chain) and to keep out dust and foreign matter.

- Multiplexer Protection Switch (MUXPS) — terminates the receive and transmit protection daisy-chains of the SMUX circuit packs and routes the STS-1 signals to the SMUXP circuit pack. In the receive direction, four groups of SMUX circuit packs are daisy-chained together and routed to the MUXPS circuit pack. In the transmit direction, two groups of SMUX circuit packs are daisy-chained together and routed to the MUXPS circuit pack. Control from the UC/SMUXP circuit packs selects the appropriate groups when necessary. If an SMUX circuit pack fails, the UC directs the SMUXP and MUXPS circuit packs to send the affected STS-1 signal to the SMUXP circuit pack and activates the associated protection relays within the failed SMUX circuit pack, allowing the affected STS-1 signal to be protected. The MUXPS LBO setting is determined by the failed MUX circuit pack.
- SONET Multiplexer Protection (SMUXP) — provides protection for SMUX circuit packs within an interface protection group (that is, all SMUX circuit packs within the same interface module). The SMUXP circuit pack selects the appropriate daisy-chain group when directed by the UC circuit pack to provide protection for an STS-1 signal. Status lines from the MUXPS circuit pack provide state information of the MUXPS circuit pack to the SMUXP. In an STS1 Interface-16 Module, the SMUXP circuit pack provides protection for EC-1 facilities (STS-1 signals) on a 1 to 15 basis.




**Notes:**

ILR = Input Line Receiver
S = Signal Splitter
LD = Output Line Driver
LBO = Line Buildout

For STS-1 Interface Modules, only four of the receive select lines and two of the transmit select lines of the MUXPS circuit pack are needed. When BXA circuit packs are inserted for SMUX circuit packs, the daisy-chain connections (receive and transmit paths) are maintained.

Figure 3-40. **STS1 Interface-16 Module Block Diagram (Protection Bus)**

## Fan Assemblies

### ED-2C816-30,G1 and ED-2C906-30 Fans

Figure 3-41 shows fan assemblies ED-2C816-30,G1 and ED-2C906-30, which are used to cool vertically mounted assemblies only in the switch bay (not in the interface bays). Each fan assembly consists of three horizontally mounted fans along with a filter and control switches and indicators. You must keep the air intake (under the assembly) free of obstructions. You must also inspect the filter (and change if necessary) at recommended intervals. An autonomous message (`REPT FAN FILTER`), generated after the recommended filter replacement interval of 91 days has occurred, reminds you that the fan filter needs to be replaced. This message must be acknowledged with the **`ENT-FAN-FILTER`** command when the fan filter is changed. The input operating voltage range of the assembly is -40.5 to -60 Vdc at approximately 1.57 A.

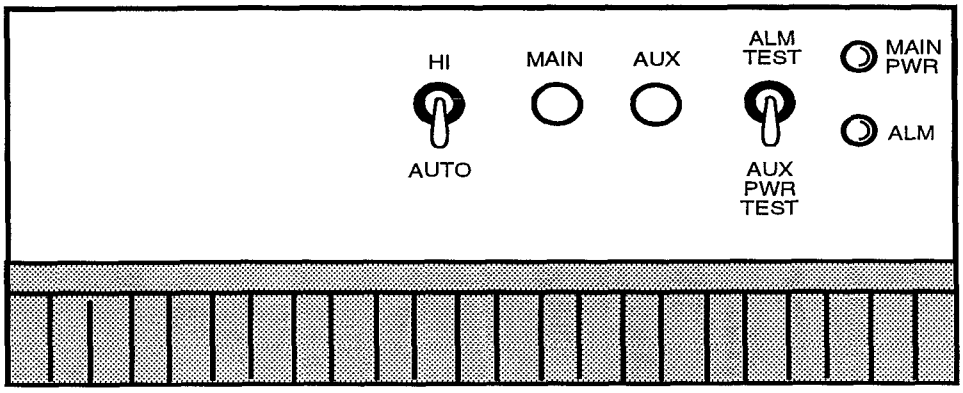



Figure 3-41. ED-2C816-30,G1 and ED-2C906-30 Fans

The front panel of the fan assembly contains the following switches and indicators:

- A two-position toggle switch labeled HI/AUTO. When the switch is in the AUTO position, a controller causes the fans to operate at reduced speed when the ambient air temperature is below 90° F. For a temperature of 90° F or higher, the fans automatically go to full speed operation. When the switch is in the HI position, the fans operate continuously at maximum speed.
- MAIN and AUX power circuit breakers

- A three-position spring-loaded toggle test switch labeled ALM TEST/AUX PWR TEST with the center position as off. When the switch is held to the ALM TEST position, input power is cut off to one fan causing the ALM LED indicator to light. The remaining two fans shift to high speed (if not already operating at high speed). When the switch is held to the AUX PWR TEST position the MAIN input power is overridden, forcing auxiliary power operation. This action causes the ALM indicator to light, the MAIN PWR indicator to go off, and all three fans to switch to high speed (if not already operating at high speed).
- A green LED labeled MAIN PWR to indicate that main power is available to the fan assembly.
- A red LED labeled ALM to indicate power or fan failure.

## ED-9C130-30,G1 and ED-9C130-30,G2 Fans

Figure 3-42 shows fan assemblies ED-9C130-30,G1 and ED-9C130-30,G2 which are used to cool vertically mounted assemblies in either the switch bay or STS1/DS3 Interface Bays. Each fan assembly consists of three horizontally mounted fans along with a filter and control switches and indicators. You must keep the air intake (under the assembly) free of obstructions. When the minor FILTER alarm LED on the fan assembly turns on, the fan filter must be replaced. After replacing the fan filter and pressing the RESET button, the FILTER alarm LED turns off. The input operating voltage range of the assembly is -40.5 to -60 Vdc at approximately 1.57 A.

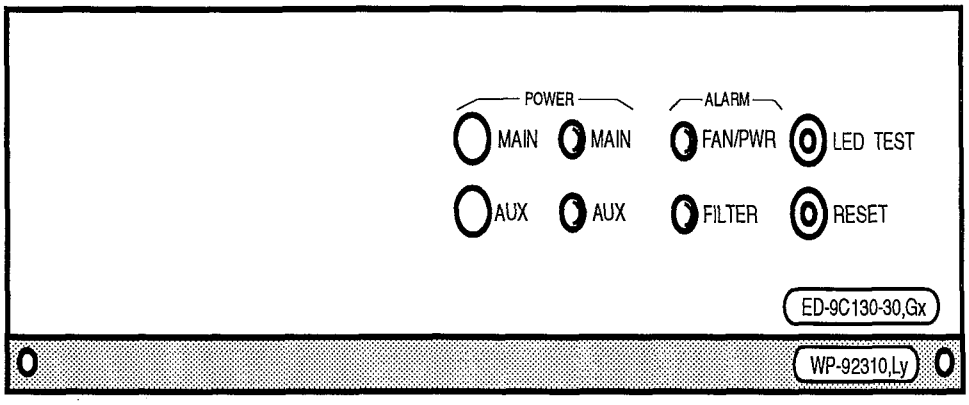



Figure 3-42. ED-9C130-30,G1 and ED-9C130-30,G2 Fans

The front panel of the fan assembly contains the following buttons and indicators:

- MAIN and AUX power circuit breakers
- Two green LEDs labeled MAIN and AUX; when lit, indicate main or auxiliary power is available to the fan assembly.
- A red LED labeled FAN/PWR; when lit, indicates a power or fan failure.
- A yellow LED labeled FILTER; when lit, indicates the fan filter needs replacing.
- A push button labeled LED TEST. Press this button to check the operation of the fan assembly LEDs.
- A push button labeled RESET. Press this button to clear an alarm and return the fan assembly to normal operation, after clearing an alarm associated with the fan assembly.

## BNC Connectors

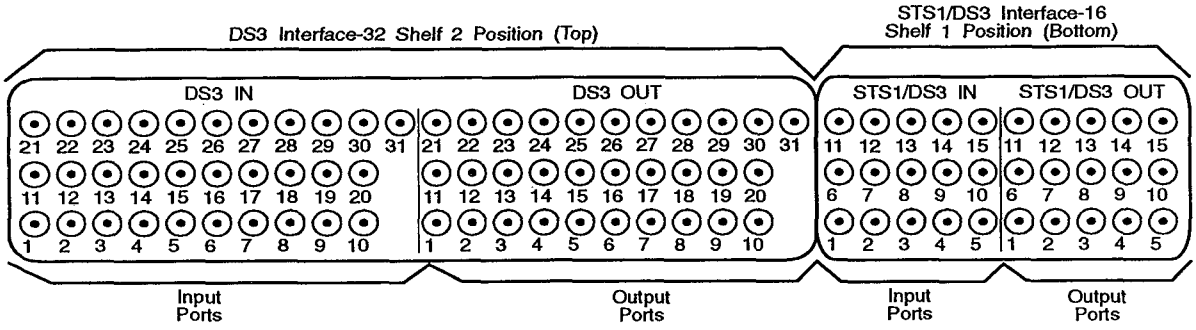
The DACS IV-2000 can be equipped with BNC connectors on STS1/DS3/DS1, STS1/DS3, and DS3 Interface Bays. These connectors provide the DACS IV-2000 with easy access to/from EC1 and DS3 facilities. BNC connectors, when provided are located at the top of the interface bay and are accessed from the rear of the bay lineup. BNC connectors are provided for each input and output port associated with MUX and SMUX circuit packs contained in STS1 and/or DS3 Interface Modules.

Figure 3-43 shows the different types of BNC connector panels for each of the STS1/DS3/DS1, STS1/DS3, and DS3 Interface Bays. The BNC connectors are panel-stamped to identify which connector is associated with the corresponding MUX/SMUX input/output port (that is, DS3 Interface-32 Module connectors are numbered 1 through 31 and STS1/DS3 Interface-16 Module connectors are numbered 1 through 15). In addition, Figure 3-43 associates the group of BNC connectors with its interface module shelf position.

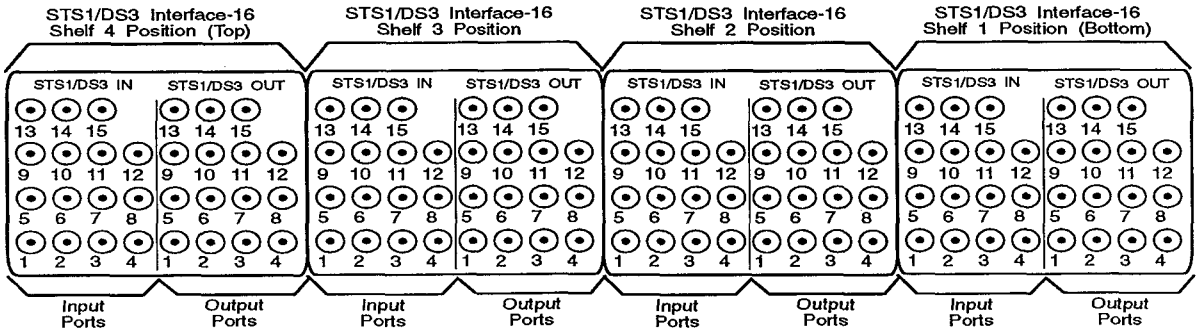
## EMC Enclosures

The DACS IV-2000 meets the electromagnetic compatibility (EMC) FCC criteria and the electrostatic discharge (ESD) requirements specified in Bellcore TR-NWT-001089. Enclosures must be ordered with any new frame and cannot be field retrofitted. For more detailed information on this option, see the paragraph entitled "EMC Enclosure Header Alarm Indicators" in Chapter 4.

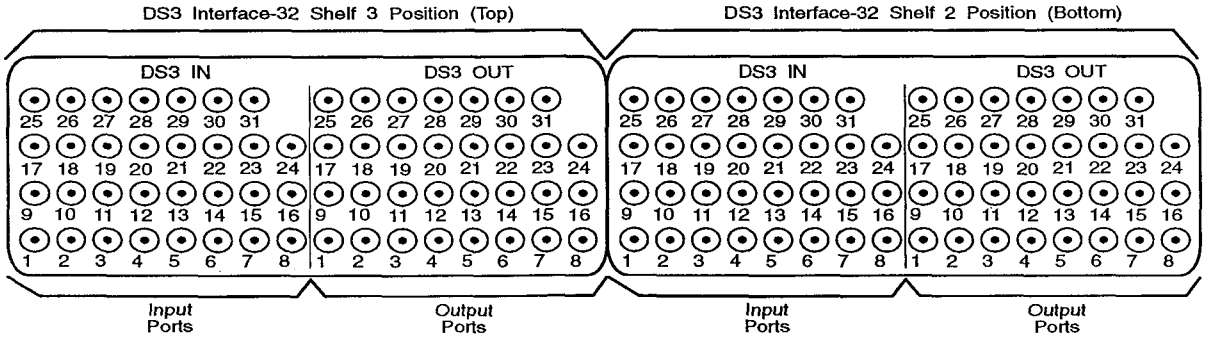
ESD grounding connections are provided on the front and rear of each bay and you are required to use wrist straps while handling the equipment.




A. STS1/DS3/DS1 Interface Bay




B. STS1/DS3 Interface Bay




C. DS3 Interface Bay

Figure 3-43. BNC Connector Panels

# Circuit Packs

Circuit packs have latches and faceplates, and are keyed to prevent their being inserted in the wrong slot. All circuit packs (except BXA, DPLL1, DS1TX1, and TBS31) have LED indicators to aid in fault isolation. Table 3-20 lists the circuit packs by function, code, module location, and number required.

Table 3-20. **Circuit Pack Equipment**

| Functional Name | Circuit Pack Code | Used In | Number Required |
|---|---|---|---|
| AWR-type filler assembly | 846103760 | SW Mod | As required* |
| AWS-type filler assembly | 846960664 | SYNC Mod | 2 |
| BXA1 (bus extender A 1) | AKM64 | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod<br>STS1 INTFC-16 Mod | As required† |
| CLKDR1 (clock distributor 1) | AKM56 | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>STS1 INTFC-16 Mod<br>DS3 INTFC-32 Mod | 2 per module<br><br><br><br>4 per module |
| CLKGN3 (clock generator 3)<br>CLKGN2 (clock generator 2) | AWR11<br>AWR7 | SW Mod | 2††<br>2 non-SONET |
| CPU2 (central processing unit 2) | AWP6 | RC Mod | 2 |
| DPLL1 (digital phase lock loop 1<br>or<br>DPLL2 (digital phase lock loop 2) | AWP9/<br>AWP9B<br><br>AWP15 | SYNC Mod | 2, required for SONET |
| DS1IF1 (DS1 interface 1) | AKM46/<br>AKM46B | DS1 INTFC Mod<br>DS1 INTFC-P Mod | 2-16 per module**<br>2-14 per module |
| DS1IP1 (DS1 interface [protection] 1) | AKM47 | DS1 INTFC-P Mod | 2 per module |
| DS1RY1 (DS1 relay 1) | AKM48 | DS1 INTFC Mod<br>DS1 INTFC-P Mod | 4 per module |

Table continued on next page. See footnotes at end of table.

Table 3-20. Circuit Pack Equipment (Continued)

| Functional Name | Circuit Pack Code | Used In | Number Required |
|---|---|---|---|
| DS1TX1 (DS1 timing extractor 1)<br>or<br>DS1TX2 (DS1 timing extractor 2) | AWS5<br><br>AWS9 | SYNC Mod | 2, required for SONET |
| DS3PM1 (DS3 performance monitor 1) [optional] | AKM62 | DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod | 1 |
| ECI3 (enhanced communications interface 3) | AWP8 | RC Mod | 2 |
| Fan assembly | ED-2C816-30,G1<br>ED-2C930-30 | SW Bay | 1 |
| Fan assembly | ED-9C130-30,G1<br>ED-9C130-30,G2 | STS1/DS3 Bay | 1 per bay |
| FBA (fuse board A) | ED-2C962-30,G1 | SW PWR Mod | 1 |
| FBB (fuse board B) | ED-2C960-30,G1 | SW PWR Mod | 4 |
| FBC (fuse board C) | ED-2C963-30,G1 | SW PWR Mod | 1 |
| FBD (fuse board D) | ED-2C961-30,G1 | SW PWR Mod | 4 |
| FBF (fuse board F) | ED-9C051-30,G2 | RC PWR Mod | 1 |
| FBG (fuse board G) | ED-9C052-30,G2 | RC PWR Mod | 1 |
| FBH (fuse board H) | ED-9C053-30,G3 | RC PWR Mod | 1 |
| FBI (fuse board I) | ED-9C055-30,G1 | RC PWR Mod | 1 |

Table continued on next page. See footnotes at end of table.

Table 3-20. **Circuit Pack Equipment (Continued)**

| Functional Name | Circuit Pack Code | Used In | Number Required |
|---|---|---|---|
| MTC3 (maintenance interface 3) | AWR10 | RC Mod | 2†† |
| MUX1 (multiplexer 1)<br>or<br>MUX2 (multiplexer 2) | AKM52B<br><br>AKM68B | DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod | 1-15 per module‡<br>1-31 per module‡ |
| MUXP1 (multiplexer protection 1)<br>or<br>MUXP2 (multiplexer protection 2) | AKM55<br><br><br><br>AKM70 | DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod | 1 per module‡<br>1 per module‡ |
| MUXPS1 (multiplexer protection switch 1) | AKM53 | DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod<br>STS1 INTFC-16 | 1 per module |
| PMGR1 (performance monitor test signal generator receiver 1) [optional] | AKM66 | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod | 1-8‡‡<br>1-7‡‡<br>1-14‡‡<br>1-16‡‡ |
| PRI5 (primary off-line storage 2) | ERB5 | RC Mod | 2 |
| PWRA (power A) standard<br>or<br>PWRA2 (power A2) duplex | 552A<br><br>566A | SW PWR Mod<br><br>SW PWR Mod | 4<br><br>4 |
| PWRE3 (power E3) | 556C | AUX PWR Mod<br>DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod<br>STS1 INTFC-16 Mod | 2 per module |
| PWRF (power F) | 427AB | RC PWR Mod | 2 |
| PWRG (power G) | 428AA | RC PWR Mod | 2 |
| SCI3 (switch communications interface 3) | AWR2C | RC Mod | 2 |
| SEC5 (secondary off-line storage 2) | ERB6 | RC Mod | 1 |

Table continued on next page. See footnotes at end of table.

Table 3-20. **Circuit Pack Equipment (Continued)**

| Functional Name | Circuit Pack Code | Used In | Number Required |
|---|---|---|---|
| SMUX1 (SONET multiplexer 1) | AKM84 | STS1 INTFC-16 Mod | 1-15 per module‡ |
| SMUXP1 (SONET multi-plexer protection 1) | AKM85 | STS1 INTFC-16 Mod | 1 per module‡ |
| SSC5 (secondary storage controller 5) | AWP14 | RC Mod | 2 |
| STPNL (status panel) | ED-9C049-30,G2 | RC Mod | 1 |
| SWCS1 (switch center stage 1) | AWS1B | SW Mod | 32 |
| SWIF1 (switch interface 1)<br>or<br>SWIF2 (switch interface 2) | AKM49<br>or<br>AKM50 | DS1 INTFC Mod<br>DS1 INTFC-P Mod | 1-8 per module |
| SWIO1 (switch input/ output 1) | AWR6 | SW Mod | 2-32** |
| TBS31 (stratum 3 time base oscillator 1)<br>or<br>TBS32 (stratum 3 time base oscillator 2) | AWS3<br><br>AWS8 | SYNC Mod | 2, required for SONET |
| UC1 (unit controller 1)<br>or<br>UC2 (unit controller 2) | AKM59<br><br>AKM59B | DS1 INTFC Mod<br>DS1 INTFC-P Mod<br>DS3 INTFC-16 Mod<br>DS3 INTFC-32 Mod | 1 per module |
| UC2 (unit controller 2) | AKM59B | STS1 INTFC-16 Mod | 1 per module |
| UI2 (unit interface 2) | AWR12 | RC Mod | 1 |

**Notes:**

* The AWR-type filler assemblies are installed in the Switch Module in place of AWR6 (SWIO1) circuit packs when the Switch Module is not equipped with the full complement of 32 AWR6 circuit packs.

† The AKM64 circuit packs are used in these modules when they are not filled to capacity with either AKM46B, AKM50, AKM68B, or AKM84 circuit packs.

‡ One protection and at least one service circuit pack must be installed.

** Must be installed in pairs.

†† Two identical MTC3 circuit packs (slots labeled MTC); two identical CLKGN3 circuit packs.

‡‡ PMGR is a optional circuit pack that can be used to replace only SWIF or MUX circuit packs. (It can not be used as a replacement for an SMUX circuit pack.)

# Power

The DACS IV-2000 frame is configured to accept two power supply arrangements, standard or duplex. The standard configuration consists of one Battery Distribution Feeder Board (BDFB) powered from a single Lineage® 2000 (or equivalent) battery plant. The duplex configuration consists of two BDFBs powered from one or two Lineage 2000 (or equivalent) battery plants.

## Standard Power Configuration

In the standard configuration (Figure 3-44), the DACS IV-2000 operates with a Lineage 2000 (or equivalent) battery plant (-48 Vdc nominal) in a central office environment supplying power to a single BDFB. Seven power buses are connected to the fuse and alarm panel from five feeders (A, B, C, D, and E) at the BDFB. Feeders A, B, C, and D have quad feeder connections to the fuse and alarm panel. The fuse and alarm panel is provided with the initial frame arrangement, and it is not necessary to provide any extra power feeders as the system is expanded. Feeders F and G are connected directly to the RC Power Module.

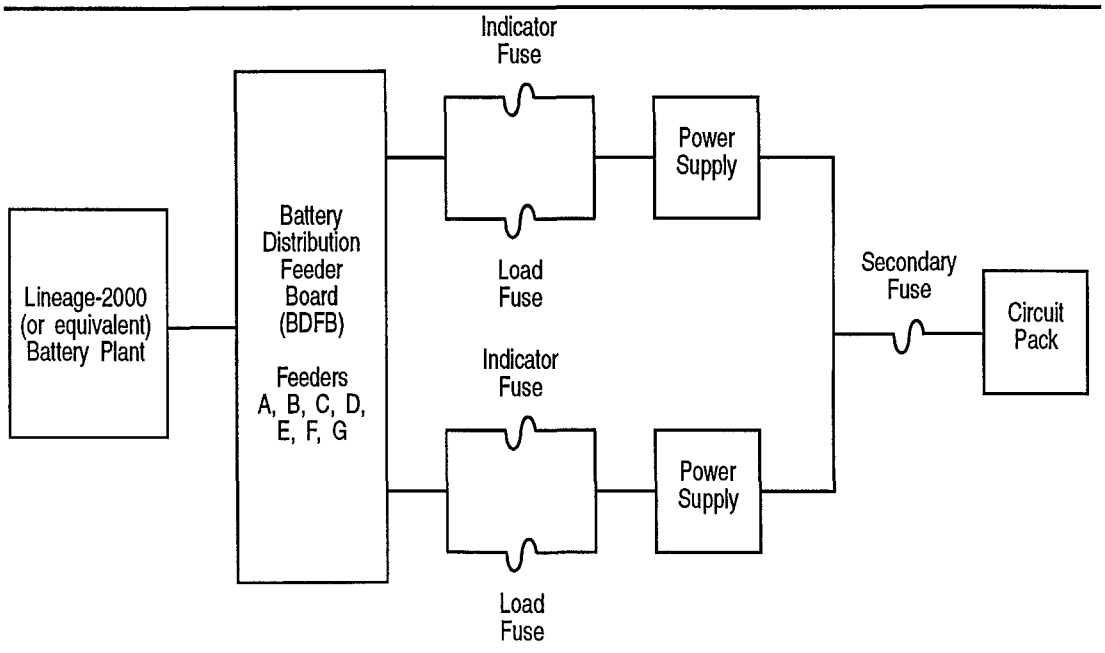



Figure 3-44. **Standard Power Fuse Interconnection**

## Duplex Power Configuration

In the duplex power configuration (Figure 3-45), the DACS IV-2000 operates with one or two Lineage 2000 (or equivalent) battery plants (-48 Vdc nominal) in a central office environment, which supply power to two BDFBs. BDFB-A supplies power buses A and B and BDFB-B supplies power buses C and D to the Switch Bay. All feeders have four connections to the fuse and alarm panel. Feeders A and B supply power to buses A, B, and E; feeders C and D supply power to fuse buses C, D and F.

The two BDFBs enable duplication of the power supply to allow the system to operate in the event one battery plant fails (except where there is only one battery plant).

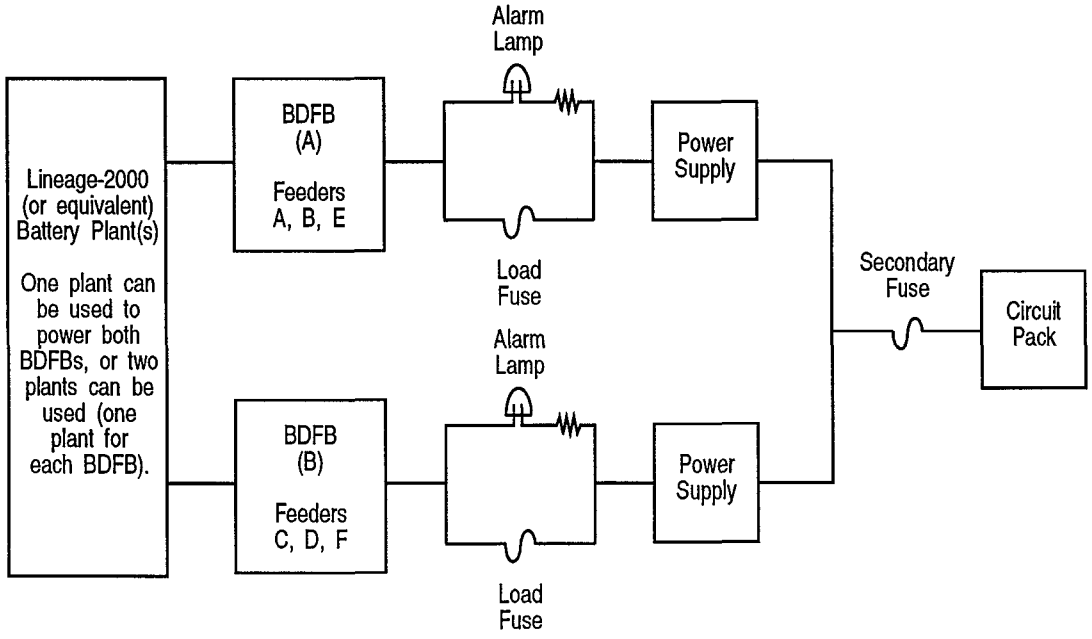



Figure 3-45. Duplex Power Fuse Interconnection

## Power Circuit Packs

There are four types of power circuit packs in the DACS IV-2000. These are PWRA, PWRE, PWRF, and PWRG. These power circuit packs convert the -48V service from the BDFB(s) into levels usable by the system.

The Redundant Controller Module has four dedicated power circuit packs (two PWRFs and two PWRGs contained in the Redundant Controller Power Module), which provide power to the printed backplane power buses. The Redundant Controller Module circuit packs are connected to, and receive power, from these backplane power buses. Fuses for Redundant Controller Module circuit packs are provided by fuse boards located in the Redundant Controller Power Module.

Fuse boards, along with the PWRA power circuit packs for the Switch Module, are located in the Switch Power Module. The Auxiliary Power Module contains two PWRE circuit packs that provide power for the Switch Module through fuses in the Switch Power Module. These power circuit packs are interconnected by a dedicated printed backplane. The power circuit pack outputs are placed on power buses connected to the Switch Module by local cables.

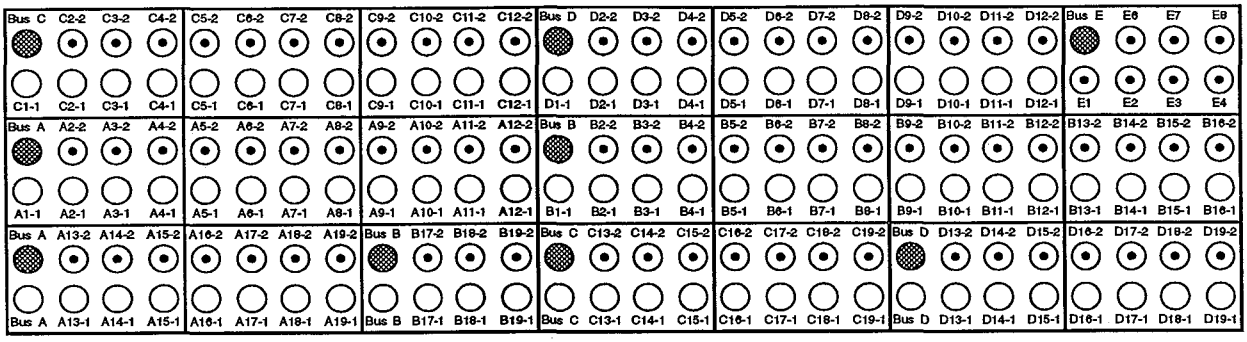
Each DS1, DS3, or STS1 Interface Module contains two PWRE circuit packs. These circuit packs provide power to the module backplane power buses. The circuit packs in the module are individually fused internally and draw power from the power buses. Figure 3-44 (standard power feeds) and 3-45 (duplex power feeds) shows how the power is fused to the individual circuit packs.

## Fuses

Figures 3-46 (standard power feed) and 3-47 (duplex power feed) show the main fuse panel. Tables 3-21and 4 relate DACS IV-2000 system fuses for the power circuit packs in the Switch Bay and interface modules to their physical location on the fuse and alarm panel at the top of the Switch Bay.

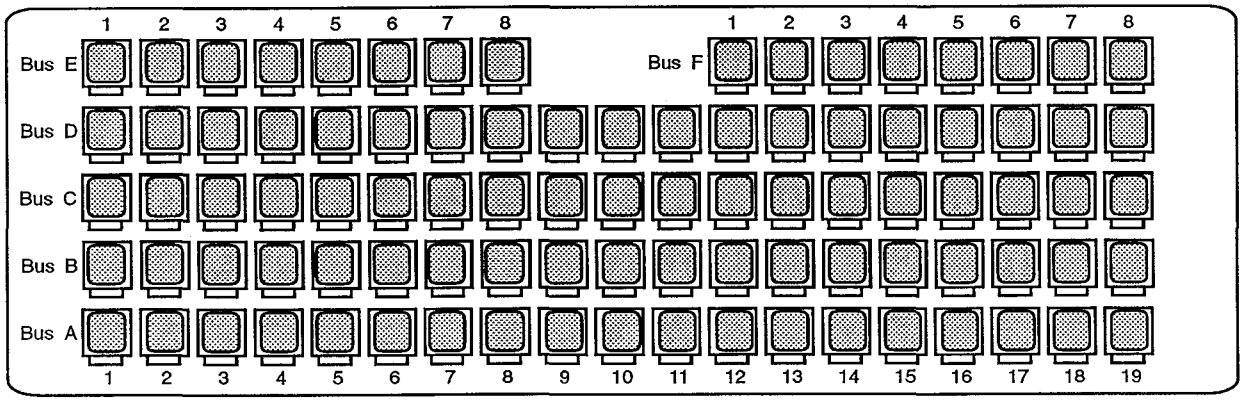
Figure 3-48 shows the secondary fuse arrangement on the DACS-IV 2000. Table 4-2 relates the secondary fuses contained in the Switch Power Module to their associated circuit pack.

Figure 3-49 shows the location of the fuses in the Redundant Controller Power Module fuse boards FBF, FBG, FBH, and FBI. The associated equipment is panel stamped by each fuse.




**Note:** Fuses for power buses A, B, C, and D come in pairs, the load fuse labeled "-1" and the indicator fuse labeled "-2". Fuses for power bus E are not paired (one load and one indicator), they are all indicator fuses.

Figure 3-46. **ED-2C940-30 Fuse and Alarm Panel**




**Note:** Fuses A1, A2, B2, C1, C2, and D2 are rated at 12A, fuse D1 is rated at 2A, and all other fuses are rated at 10A. All fuses have a red alarm lamp to indicate failure. Fuse B1 is not connected.

Figure 3-47. **ED-9C114-30 Fuse and Alarm Panel**

Table 3-21. **Fuse Chart Interface Bays (Bay 1-4 and 6-9)**

| Shelf | PWR Circuit Pack | Bay 1 | Bay 2 | Bay 3 | Bay 4 | Bay 6 | Bay 7 | Bay 8 | Bay 9 |
|---|---|---|---|---|---|---|---|---|---|
| **Standard Power (ED-2C940-30 Fuse Panel)** | | | | | | | | | |
| 4 | PWRE-2 | C17 | D14 | D4 | D10 | C12 | D6 | B15 | C19 |
| | PWRE-1 | A17 | C15 | B4 | C10 | B12 | B6 | C8 | A19 |
| 3 | PWRE-2 | D16 | D13 | C4 | B10 | D12 | C6 | B8 | D18 |
| | PWRE-1 | A16 | A14 | A4 | A10 | A12 | A6 | A8 | C18 |
| 2 | PWRE-2 | B18 | C14 | D3 | C9 | D11 | D5 | C7 | D19 |
| | PWRE-1 | A15 | B17 | C3 | B9 | B11 | C5 | B7 | A18 |
| 1 | PWRE-2 | D15 | C13 | B3 | D9 | C11 | B5 | D7 | D17 |
| | PWRE-1 | C16 | A13 | A3 | A9 | A11 | A5 | A7 | B19 |
| Fan | Main | — | A16 | B18 | A17 | C19 | D17 | D19 | — |
| | Auxiliary | — | D16 | D15 | C17 | C19 | D17 | D19 | — |

**Note:** All load fuses are 10A and all indicator fuses are 0.5A.

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Duplex Power (ED-9C114-30 Fuse Panel)** | | | | | | | | | |
| 4 | PWRE-2 | F4 | D14 | D4 | D10 | D12 | D6 | D8 | F8 |
| | PWRE-1 | E4 | B14 | B4 | B10 | B12 | B6 | B8 | E8 |
| 3 | PWRE-2 | F3 | C14 | C4 | C10 | C12 | C6 | C8 | F7 |
| | PWRE-1 | E3 | A14 | A4 | A10 | A12 | A6 | A8 | E7 |
| 2 | PWRE-2 | D15 | D13 | D3 | D9 | D11 | D5 | D7 | D18 |
| | PWRE-1 | B15 | B13 | B3 | B9 | B11 | B5 | B7 | B18 |
| 1 | PWRE-2 | F2 | C13 | C3 | C9 | C11 | C5 | C7 | F6 |
| | PWRE-1 | E2 | A13 | A3 | A9 | A11 | A5 | A7 | E6 |
| Fan | Main | E1 | A15 | A16 | B16 | B19 | A19 | A18 | E5 |
| | Auxiliary | F1 | C15 | C16 | D16 | D19 | C19 | C18 | F5 |

**Note:** All fuses are 10A with a red alarm lamp to indicate failure.

Table 4. Fuse Chart Switch Bay (Bay 5)

| Auxiliary Power PWRE | | Switch Power PWRA | | | | Fan Assembly | |
|---|---|---|---|---|---|---|---|
| 1 | 2 | 1 | 2 | 3 | 4 | Main | Auxiliary |
| **Standard Power (ED-2C940-30 Fuse Panel)** | | | | | | | |
| B14 | D8 | A2 | B2 | C2 | D2 | E6 | B13-2 |

**Note:** Fuses A2-1, B2-1, C2-1, and D2-1 are 12A and fuses B14-1 and D8-1 are 10A. Fuses A2-2, B2-2, B14-2, C2-2, D2-2, and D8-2 (indicator fuses) are 0.5A. The fan assembly fuses E6 and B13-2 are indicator fuses rated at 5A.

| Duplex Power (ED-9C114-30 Fuse Panel) | | | | | | | |
|---|---|---|---|---|---|---|---|
| B14 | D8 | A2 | B2 | C2 | D2 | A17 | C17 |
| PWRF-1, PWRG-1, TBS3-0 (SYNC-0) | | | PWRF-2, PWRG-2, TBS3-1 (SYNC-1) | | | Header Designation Assembly | |
| A1 | | | C1 | | | D1 | |

**Note:** Fuses A1, A2, B2, C1, C2, and D2 are rated at 12A, fuse D1 is rated at 2A, and all other fuse are rated at 10A. All fuses contain a red alarm lamp to indicate failure.

Table 4-1.

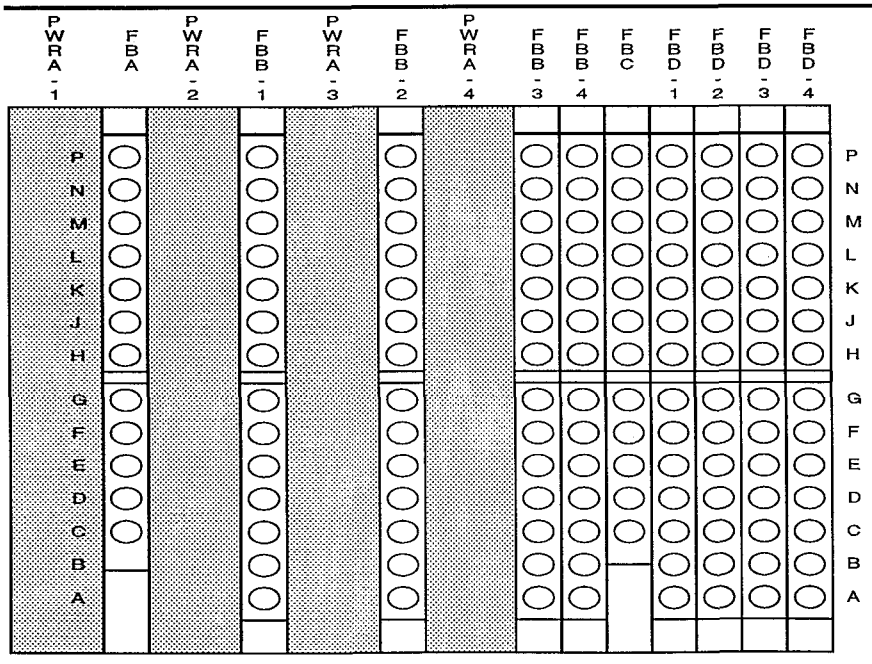
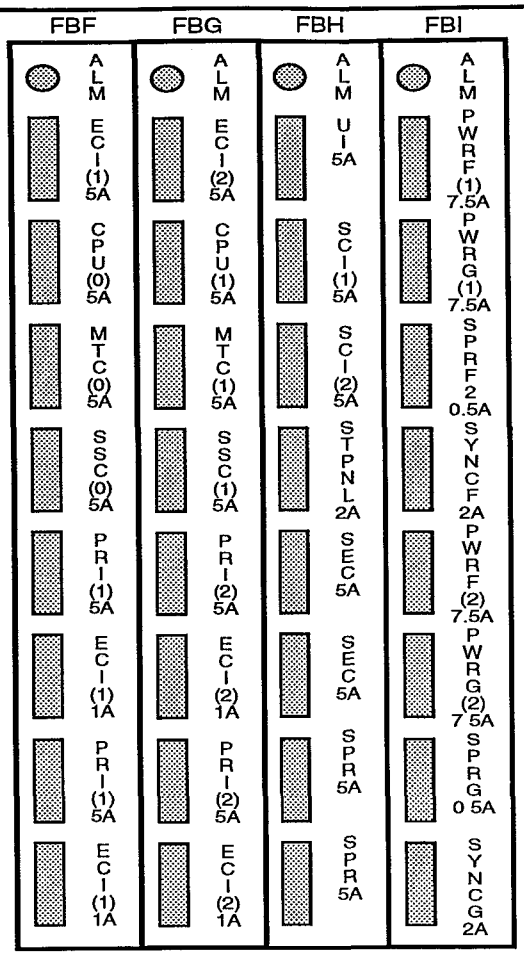



Figure 3-48. Secondary Fuses (FBA, FBB, FBC, and FBD)

Table 4-2. Secondary Fuse Chart for System

| Location | Type 77D (10A) Fuse for +5V Supply | | | | |
|---|---|---|---|---|---|
| | FBA | FBB-1 | FBB-2 | FBB-3 | FBB-4 |
| P | SWIO-11 | SWCS-9 | SWCS-23 | SWIO-21 | SYNC-1* |
| N | SWIO-10 | SWCS-8 | SWCS-22 | SWIO-20 | SYNC-0* |
| M | SWIO-9 | SWCS-7 | SWCS-21 | SWIO-19 | SWIO-32 |
| L | CLKGN-0 | SWCS-6 | SWCS-20 | SWIO-18 | SWIO-31 |
| K | SWIO-8 | SWCS-5 | SWCS-19 | SWIO-17 | SWIO-30 |
| J | SWIO-7 | SWCS-4 | SWCS-18 | SWCS-32 | SWIO-29 |
| H | SWIO-6 | SWCS-3 | SWCS-17 | SWCS-31 | SWIO-28 |
| G | SWIO-5 | SWCS-2 | SWCS-16 | SWCS-30 | SWIO-27 |
| F | SWIO-4 | SWCS-1 | SWCS-15 | SWCS-29 | SWIO-26 |
| E | SWIO-3 | SWIO-16 | SWCS-14 | SWCS-28 | SWIO-25 |
| D | SWIO-2 | SWIO-15 | SWCS-13 | SWCS-27 | SWIO-24 |
| C | SWIO-1 | SWIO-14 | SWCS-12 | SWCS-26 | SWIO-24 |
| B | - | SWIO-13 | SWCS-11 | SWCS-25 | SWIO-23 |
| A | - | SWIO-12 | SWCS-10 | SWCS-24 | SWIO-22 |
| Location | Type 78J (7.5A) Fuse for -5V Supply | | | | |
| | FBC | FBD-1 | FBD-2 | FBD-3 | FBD-4 |
| P | SWIO-11 | SWCS-9 | SWCS-23 | SWIO-21 | SYNC-1* |
| N | SWIO-10 | SWCS-8 | SWCS-22 | SWIO-20 | SYNC-0* |
| M | SWIO-9 | SWCS-7 | SWCS-21 | SWIO-19 | SWIO-32 |
| L | CLKGN-0 | SWCS-6 | SWCS-20 | SWIO-18 | SWIO-31 |
| K | SWIO-8 | SWCS-5 | SWCS-19 | SWIO-17 | SWIO-30 |
| J | SWIO-7 | SWCS-4 | SWCS-18 | SWCS-32 | SWIO-29 |
| H | SWIO-6 | SWCS-3 | SWCS-17 | SWCS-31 | SWIO-28 |
| G | SWIO-5 | SWCS-2 | SWCS-16 | SWCS-30 | SWIO-27 |
| F | SWIO-4 | SWCS-1 | SWCS-15 | SWCS-29 | SWIO-26 |
| E | SWIO-3 | SWIO-16 | SWCS-14 | SWCS-28 | SWIO-25 |
| D | SWIO-2 | SWIO-15 | SWCS-13 | SWCS-27 | SWIO-24 |
| C | SWIO-1 | SWIO-14 | SWCS-12 | SWCS-26 | SWIO-24 |
| B | - | SWIO-13 | SWCS-11 | SWCS-25 | SWIO-23 |
| A | - | SWIO-12 | SWCS-10 | SWCS-24 | SWIO-22 |

* SYNC fuses provide fuse protection for all three circuit packs (DPLL, TBS3, and DS1TX) associated with a synchronizer side.




**Notes:**

- Numbers in parentheses are circuit pack position numbers in the Redundant Controller Module. Fuse ratings are listed below the circuit pack identifier.
- The 7.5A fuses are the load fuses to the PWRF and PWRG power circuit packs.
- The 5A (2A for the Status Panel) fuses are the secondary fuses (or the +5V supply) to the circuit packs contained in the Redundant Controller Module.
- The 1A fuses associated with the ECI circuit packs are for +12V and -12V supplied to the CILINKS. When these fuses blow, communication with the CILINKS can be interrupted.
- The 5A fuse for the optical disk drive (SEC) is for the +5V and +12V supply.
- The 5A fuses for the hard disk drives (PRI) are for the +5V and +12V supply.
- The 2A fuses for SYNCF (TBS3-0) and SYNCG (TBS3-1) are for the -48V supply to the TBS3 circuit packs.
- The labels SPR, SPRF, and SPRG denote spare fuses that are not connected to any circuit pack.

Figure 3-49. **Redundant Controller Power Module Fuses (FBF, FBG, FBH, and FBI)**

# DS1 Performance Monitoring Hardware

The DACS IV-2000 can support different hardware configurations to allow for the following three options of DS1 performance monitoring:

- Full-Time Monitoring
- Scanned Monitoring
- Camp-On Monitoring.

Due to interface module configuration constraints, the number of PMGR circuit packs per interface module is limited.

- UC4 circuit pack memory (scan performance monitoring has a higher demand on memory than full-time/camp-on performance monitoring)
- Only one PMGR circuit pack can be provisioned to perform scan performance monitoring per SWIO circuit pack pair.

Table 4-3 lists the maximum number of PMGR circuit packs in each interface module type for given performance monitoring mode combinations.

Table 4-3. **Maximum PMGR Circuit Packs per Interface Module**

| Interface Module Type | Performance Monitoring Mode | |
|---|---|---|
| | Scan | Full-Time/Camp-On |
| DS3 Interface-32 | 0 | 16 |
| | 1 | 8 |
| | 2 | 2 |
| DS3 Interface-16 | 0 | 15 |
| | 1 | 8 |
| DS1 Interface | 0 | 8 |
| | 1/0* | 7 |
| DS1 Interface-Protection | 0 | 7 |
| | 1/0† | 6 |

* Zero if there is a SCAN performance monitoring PMGR circuit pack in the DS1 Interface or Interface-Protection Module associated with the same SWIO circuit pack pair.

† Zero if there is a SCAN performance monitoring PMGR circuit pack in the DS1 Interface Module associated with the same SWIO circuit pack pair.

The following sections describe the hardware configurations necessary to accommodate the different options of DS1 performance monitoring (including PMGR circuit pack usage). For more information on the DS1 performance monitoring feature, refer to the section titled "DS1 Performance Monitoring" in Chapter 2.

## Full-Time Monitoring

Full-time monitoring is provided where continuous performance monitoring is required (for example, end customer DS1 services); it can be implemented in one of the two following options:

- Dedicated Full-Time — uses the SWIF2 circuit pack and monitors a group of 28 DS1 signals associated with the SWIF2 circuit pack's two DS1IF circuit packs. This option is generally employed when all or a large fraction of the incoming DS1 facilities require full-time monitoring. Figure 3-50 shows this type of configuration.

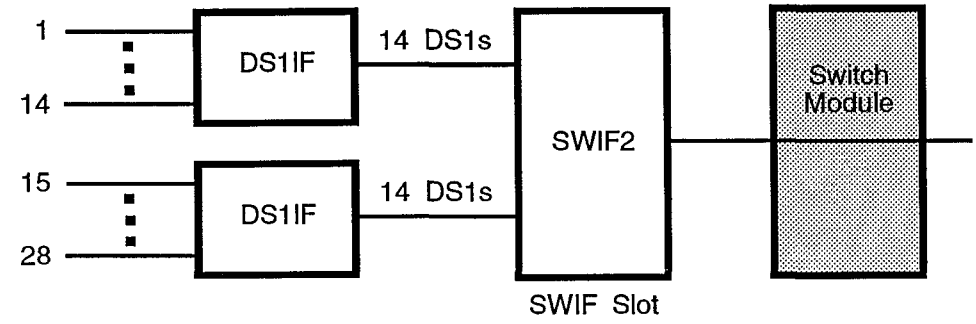



Figure 3-50. **Dedicated Full-Time DS1 PM**

To implement the dedicated full-time mode for DS1 facilities, SWIF2 circuit packs are required for the DS1 interface groups that are going to be monitored. Any number of SWIF circuit pack slots (except protection SWIF slots) can be equipped with a SWIF2 circuit pack with no loss of switching capacity and constraints on number of PMGR circuit packs used for other modes of DS1 performance monitoring. Performance-monitoring data is not collected when a DS1 interface group is being protected by the DS1 protection group. Procedures for changing SWIF1 circuit packs are in Chapter 14 of the *DACS IV-2000 (256) Release 4.0 Operations and Maintenance* manual (AT&T 365-340-701).

- Camp-on Full-Time — uses the PMGR circuit pack and monitors any DS1 signal not already monitored in the dedicated full-time option. This option is generally employed when you desire to perform selected full-time monitoring of DS1 signals on DS1 facilities and/or full-time monitoring of DS1 tributaries within DS3 or EC-1s. Figure 3-51 shows this type of configuration.

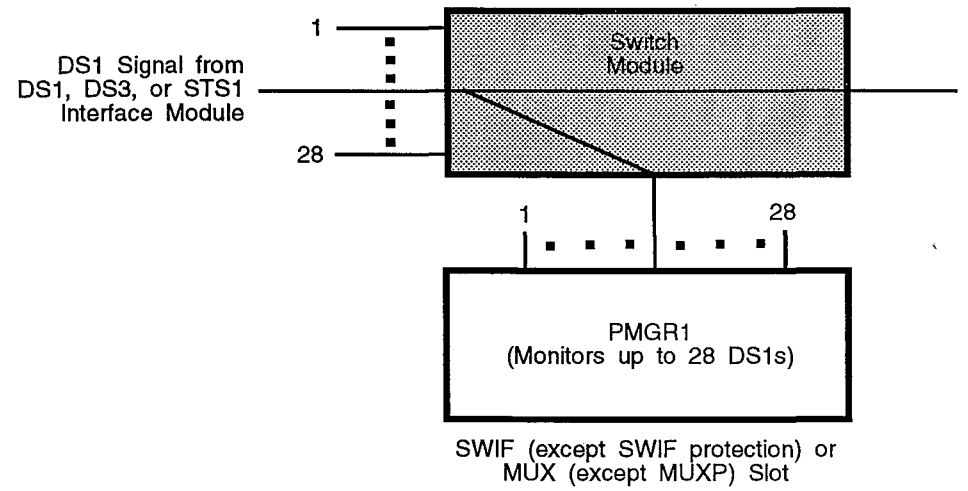



Figure 3-51. **Camp-On Full-Time DS1 PM**

To implement the camp-on full-time mode for DS1 facilities or DS1 tributaries within a DS3, PMGR1 circuit packs are required to be inserted into SWIF or MUX (except protection SWIF or MUXP) circuit pack slots. When using SWIF circuit pack slots, the associated DS1IF circuit pack slots must contain either DS1IF or BXA circuit packs. Switching capacity is decreased by 28 DS1 signals for each PMGR1 circuit pack used. In addition, depending on your configuration of camp-on and scan monitoring, the number of PMGR1 circuit packs used for the camp-on mode can be limited. The following constraints (summarized in Table 4-3) apply:

— No scan monitoring used:

- DS1 Interface Modules — up to 8 PMGR1 circuit packs
- DS1 Interface-P Modules — up to 7 PMGR1 circuit packs
- DS3 Interface-16 Modules — up to 15 PMGR1 circuit packs
- DS3 Interface-32 Modules — up to 16 PMGR1 circuit packs

— Scan monitoring used:

- Pair of DS1 Interface Modules associated with the SWIO circuit pack pair scan monitored by a PMGR circuit pack — up to 15/14 PMGR1 circuit packs for camp-on mode
- DS3 Interface-16 Module using PMGR circuit for scan monitoring SWIO circuit pack pair — up to 8 PMGR1 circuit packs for camp-on mode
- DS3 Interface-32 Module using one PMGR circuit for scan monitoring SWIO circuit pack pair (either MUX-{1-15} or MUX-{16-31}) — up to 8 PMGR1 circuit packs for camp-on mode
- DS3 Interface-32 Module using two PMGR circuit for scan monitoring both SWIO circuit pack pairs (MUX-{1-15} and MUX-{16-31}) — up to 2 PMGR1 circuit packs for camp-on mode.

## Scanned Monitoring

Scanned monitoring is provided when the performance health of the DS1 signal is desired but when full-time monitoring is not required. This mode is the most cost-effective mode provided by the DACS IV-2000, as one PMGR circuit pack can monitor up to 420 DS1 signals (each of the 28 ports associated with a PMGR circuit packs can scan up to 15 DS1 signals). Figure 3-52 shows this type of configuration.

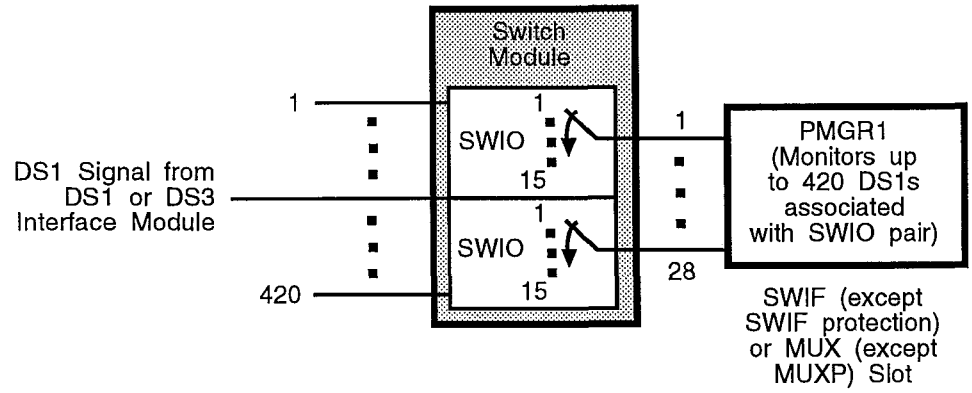



Figure 3-52. Scanned DS1 PM

To implement the scanned mode for DS1 facilities or DS1 tributaries within DS3 facilities, PMGR1 circuit packs are required to be inserted into SWIF (except protection SWIF) or MUX (except MUXP) circuit pack slots. When using SWIF circuit pack slots, the associated DS1IF circuit pack slots must contain either DS1IF or BXA circuit packs. Switching capacity is decreased by 28 DS1 signals for each PMGR1 circuit pack used. Only one PMGR1 circuit pack can be used for scanned monitoring per SWIO circuit pack pair. That is, one PMGR1 circuit pack can be used for each pair of DS1 Interface Modules (upper pair or lower pair within an DS1 or STS1/DS3/DS1 Interface Bay), one PMGR1 circuit pack per DS3 Interface-16 Modules, and up to two PMGR1 circuit packs per DS3 Interface-32 Modules (one for MUX-{1-15} and one for MUX-{16-31}). In addition, the constraint on the number of PMGR1 circuit packs used for scanned monitoring depends on the number of PMGR1 circuit packs used for bridged access or camp-on monitoring. Scanned monitoring can not be done for DS1s within Vt1.5s of EC-1 facilities. Refer to the previous section titled "Full-Time Monitoring" or Table 4-3 for additional restrictions.

The procedure for provisioning PMGR circuit packs is in the section titled "Provisioning PMGR1 Circuit Packs for DS1 PM" in Chapter 5 of the *DACS IV-2000 (256) Release 4.0 Operations and Maintenance* manual (AT&T 365-340-701).

# User Interfaces

# 4

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# User Interfaces

# 4

The DACS IV-2000 provides user interfaces that allow you to issue commands to control system operations. This same user interface provides a mechanism that delivers messages regarding changes in system status.

## Commands and Messages

The DACS IV-2000 supports a message set (previously called Message Set 2)[1] that is compatible with Transaction Language (TL)1, Issue 4. This message set provides alarm, provisioning, administration, and maintenance (including test access and performance monitoring) commands and messages. This message set also provides support for communication with Bellcore Operations Systems/ Intelligent Network Elements (OPS/INE) and Network Monitoring and Analysis (NMA) OSs.

The format of the DACS IV-2000 commands and messages follows the CCITT MML Standards and Recommendations from Bellcore. The dialog procedure used to enter commands follows the methodology given in Bellcore TR-TSY-000824.

1. Message Set 1 is not supported for Release 3.0 and later.

Messages can be issued either in response to a command (manual response) or to report a change in the state of the system due to autonomous actions (autonomous messages). Manual responses fall into two categories:

- Normal responses — indicating completion of a command, including data associated with the completion of the command.
- Error responses — indicating that the command was not successfully completed, including the reason for denial.

Messages have two formats, as follows:

- Human-machine — provides information over the administrative links that technical personnel can interpret.
- Machine-machine — provides additional parsable information that can be used by operations systems to further clarify and supplement information provided by the human-machine messages.

## Dialog Mode

Associated with each user (User ID) in the DACS IV-2000 is a parameter called dialog mode. The value of this parameter determines whether a particular session with the system is handled as human-machine or machine-machine. The dialog modes of operation are:

- MENU/prompt mode — provides the human-machine operation. Users enter this mode by typing a question mark at the command prompt (<). The menu/prompt mode provides three menu levels (called Activity Menus) that allow users to select an activity from the first (and possibly second) menu level and a command (verb-modifier) from the second (or possibly third) menu level. Figure 4-1 shows the basic menu/prompt mode structure. Details of the human-machine interactions and Activity Menus are given in Appendix B of the *DACS IV-2000 (256) Release 4.0 Commands and Messages* manual (AT&T 365-340-702).
- COMMAND-line mode - provides the machine-machine operation. This mode can also be used by experienced users who have knowledge of the command structure. When using this mode, commands are selected and parameters entered within a single line [a backslash (\) followed by a carriage-return (<cr>) is considered a single line of input].

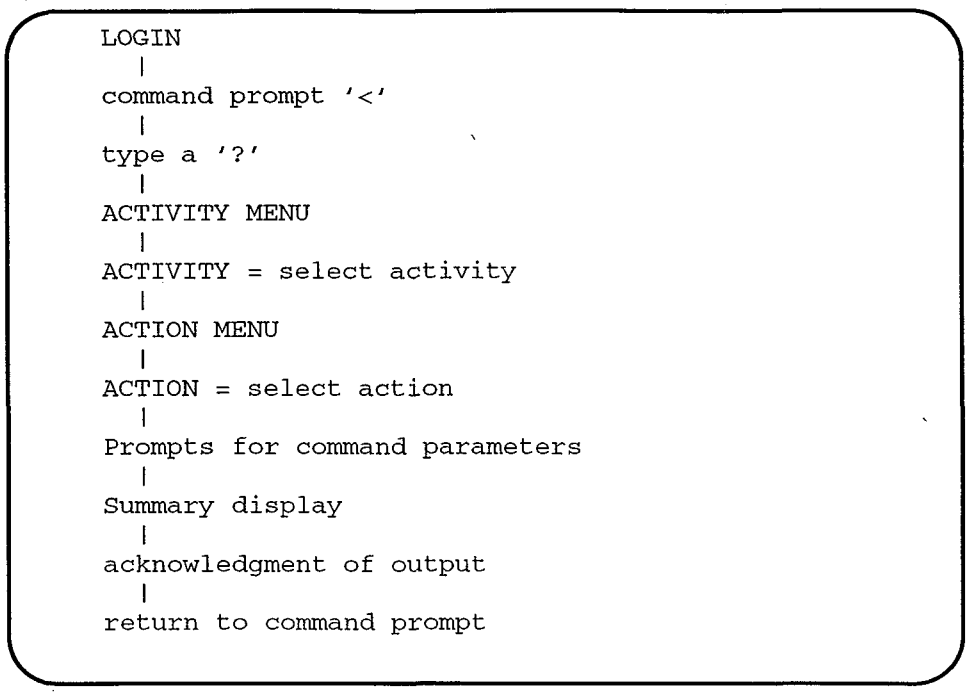



Figure 4-1. **Menu/Prompt Mode Structure**

## Message Screening

There are two message-screening parameters that users can set. One governs the amount of information that is sent over a link when no one is logged into the DACS IV-2000. The other governs the amount of information that is sent to a user who is logged into the DACS IV-2000. Each link and each user can be provisioned for a message screening value. These values need not be the same.

Virtual circuits associated with a link all share the same message screening value. The value of the message screening that is set for a user overrides the value set for the link when a user logs into the DACS IV-2000 (the link takes on the value set for the User ID). When a user logs into the DACS IV-2000 over a virtual circuit and the other virtual circuits of that link have no one logged in over them, the value of message screening for the user who logged on to the virtual circuit is used, and the other virtual circuits continue to use the value of message screening defined for the link.

The **ENT-SECU-USER** or **ED-SECU-USER** commands are used to set the user message screening values, and the **ED-PRMTR-LINK** command is used to set or change the link message screening value.

The message screening values and their definitions are as follows:

- INPUT — specifies that the User ID (UID) or link receives responses to its own input commands.
- AUTO — specifies that the UID or link receives responses to its own input commands and autonomous messages except `REPT DBCHG` messages due to manual command input.
- ALL — specifies that the UID or link receives responses to its own input messages, autonomous messages except `REPT DBCHG` messages due to manual command input, and responses to input commands from other UIDs.
- DBAUTO — specifies that the UID or link receives responses to its own input messages and autonomous messages, including `REPT DBCHG` messages due to manual command input.
- DBALL — specifies that the UID or link receives responses to its own input messages, autonomous messages including `REPT DBCHG` messages due to manual command input, and responses to input commands from users (UIDs) links.

### Command Verification

Each UID is assigned a user type, either Human or Machine. This user type is checked when a user enters a command. If the command is potentially service-affecting or may prevent access to the DACS IV-2000 for an extended period of time and the user type is Human, the DACS IV-2000 displays a warning message and requests that the user verify the command. This warning message is displayed in both the Menu and Command dialog modes. The warning message is not displayed if the user type is Machine. The warning message is placed in the Review of Parameter Responses menu after the parameter responses and before the `EXECUTE COMMAND? [YES/NO/MODIFY]` prompt.

## System Addressing

Within the input commands, there are two levels of addressing. The first level consists of the target identifier (TID) parameter, and the second level is the entity identifier (EID) parameter.

## TID Addressing

The TID uniquely identifies the target DACS IV-2000. This parameter is set by the input command **ED-NE**. It can optionally be specified in any input command, and is always printed on all output messages. The 11-character CLLI® code is the recommended value for the TID. If the CLLI code for a DACS IV-2000 is not unique, the CLLI code can be augmented with additional characters for a total of 18 characters. If communications are point-to-point between the user and the DACS IV-2000, the TID is not necessary.

## EID Addressing

The EID identifies either equipment, facility, or link locations. For the most part, the equipment domain is used with command names ending with the **EQPT** modifier. The facility domain is used with command names ending with the **T1**, **T3**, **EC1**, or **VT1** modifier. The CILINK domain is used with command names ending in the **LINK** modifier. However, some command entries allow mixing of these domains.

An equipment domain address is a combination of a physical description and a logical address. The first component of the address is the physical description (SSC, SCI, etc.). If necessary, a hierarchic logical address is appended to the physical description (for example, **UC-16** identifies the unit controller in unit 16). Addressing within the facility domain also follows a hierarchic scheme, which is shown in Table 4-1.

The DS1 Ports are all DS1 signals that enter the system, either as a DS1, a DS1 within a DS3, or as a DS1 within a VT1.5. The DS1 Interface Ports are the subset of DS1 Ports that enter the system as DS1 facilities. VT1.5 Ports are tributaries of the STS1 Ports. The DS3 Interface Ports are DS3 facilities that enter the system. The STS1 Interface Ports are EC1 facilities that enter the system. DS1, DS3, VT1.5, and STS1 Ports can also be addressed by module name (for example, **DS1GRP**, **VT1GRP**, or **UNIT**).

Table 4-1. **EID Facility Addressing**

| Facility | Address {unit number}-{slog number}-{port number} |
|---|---|
| DS1 Port | {1-32}-{1-31}-{1-28} |
| DS1 Interface Module DS1 Port | {1-32}-{1-8}-{1-28} |
| DS1 Interface-P Module DS1 Port | {1-32}-{1-7}-{1-28} |
| DS3 Interface-32 Module DS1 Port | {1-32}-{1-31}-{1-28} |
| DS3 Interface-16 Module DS1 Port | {1-32}-{1-15}-{1-28} |
| STS1 Interface-16 Module DS1 Port | {1-32}-{1-15}-{1-28} |
| DS3 Interface-32 Module DS3 Port | {1-32}-{1-31} |
| DS3 Interface-16 Module DS3 Port | {1-32}-{1-15} |
| STS1 Interface-16 Module VT1.5 Port | {1-32}-{1-15}-{1-28} |
| STS1 Interface-16 Module EC-1 Port | {1-32}-{1-15} |

DS1 Port addressing has the form:

{unit number}-{slot number}-{port number}

where:

- Unit Number — is the number of the unit that supports the port.
- Slot Number (physical slot location occupied by a MUX, SMUX, or SWIF circuit pack) — is the DS3 or STS-1 equivalent within the interface module. The DS3 equivalent corresponds to either a MUX circuit pack that supports one DS3, or to a SWIF circuit pack that supports 28 DS1s. The STS-1 equivalent corresponds to the SMUX circuit pack that supports one STS-1 signal. The range of numbers associated with these elements is related to the DACS IV-2000 architecture.
- Port Number (for DS1 Ports and VT1.5 Ports) — is the DS1 within the DS3 equivalent or the VT1.5 within the STS-1 equivalent.

DS3 Ports have the same form except the port number is omitted.

Addressing within the link domain consists of a single format:

```
CILINK-{1,2}-{1-6}
```

which indicates a physical link on the ECI circuit pack and is generically known as a communications interface link (CILINK).

# Security Interface

For security purposes, access to the DACS IV-200 is restricted to authorized users through the security interlace. The security interface consists of user login IDs and associated passwords, and user privilege codes. Input command priorities are established through the use of user priority levels.

## User ID Passwords

To allow access to the DACS IV-2000, the system administrator creates valid UIDs (logins) and their associated passwords. These UID/password pairs allow users to access the DACS IV-2000 to perform administrative, operational, provisioning, and maintenance functions.

Valid UIDs consist of one to ten characters. Allowable characters are letters (A-Z, a-z), decimal digits (0-9), and *special legal characters* (- . # % +). Valid passwords consist of six to eight characters. At least two of the characters must be non-alphabetic characters with at least one character being a *special legal character.* Password characters are letters (A-Z, a-z), decimal digits (0-9), and *special legal characters* (# % +). The first character of the password must be a letter.

The DACS IV-2000 allows the current set of UIDs and their associated passwords even if they do not adhere to the above rules. However, new passwords must conform to the above rules.

## User Privilege Codes

Restricting access to information stored in a DACS IV-2000 database to those who need access is an effective security strategy to preserve the integrity of the database. This strategy grants the smallest set of privileges necessary to perform tasks.

To assist in this restrictive access, UIDs are assigned User Privilege Codes. User Privilege Codes are made up of User Community Functional Categories (UCFC) and User Community Authorization Levels (UCAL) pairs. These components of security management are described in Appendix E of the *DACS IV-2000 Release 4.0 Commands and Messages* manual (AT&T 365-340-702).

## User/Superuser Priority Levels

The five levels of user login input commands priority (UCPL) are ranked: 5(highest), 4, 3, 2, and 1(lowest). There are no restrictions for assignment of priority levels to user logins; however, it is suggested that the operation system support user logins provisioned for the highest priority level.

Only a superuser (UCFC/UCAL = S5) can change all parameters for all users. A user with a UCFC/UCAL of S1 can change only the following parameters: his own password, Message Screening, Dialogue Mode, and User Type. For a superuser, the Old Password field is checked against the current password only if it is given. If the superuser specifies the old password in the `CHG-LGN` command, that password must be validated. The last superuser cannot reduce the UCFC/UCAL below S5.

Characteristics of a superuser (UCFC/UCAL = S5) are as follows:

- The only user that can edit a user's UCFC/UCAL pair
- Must enter own password when changing own login; however, this is not necessary when changing other users' logins
- Has permission to create and delete a user login
- Can log out other users from a working session
- Is able to retrieve parameters associated with all user logins
- Can execute `RTRV-SECU-AUD` and `DLT-SECU-AUD` commands.

Passwords can be changed more than once in a login session. All changes to passwords take effect immediately. To change passwords you must use the password that you changed to, not the password that you logged in with. When you change your own login parameters, the old password must be supplied. If the old password is used, even when optional, it is checked.

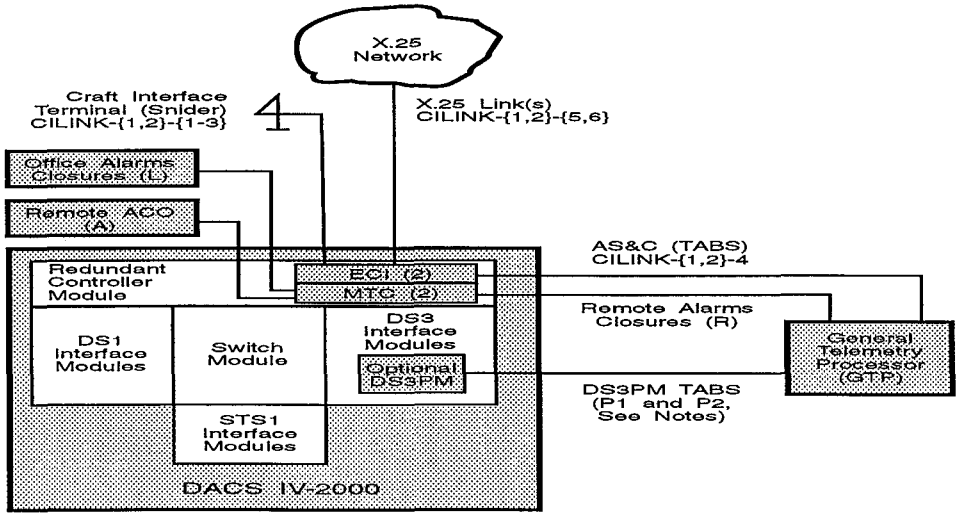
Non-superusers are able to retrieve privilege parameters associated with their own logins only.

# Links

The DACS IV-2000 provides twelve administrative links (CILINKs) to interface with operations systems (OSs) using a X.25 network (CILINK-{1,2}-{5,6}) and user interface terminals using Snider protocol (CILINK-{1,2}-{1-3}). The administrative links are used to access all the features and functions of the system, both locally and remotely. They also provide alarm closures and a remote reset function to local and remote offices. In addition, a separate optional OS interface can be used to provide path performance monitoring information for DS3s that are provisioned with the C-bit parity format.

TABS/TBOS links (CILINK-{1,2}-4) are provided for communications with a General Telemetry Processor (GTP). The system designates one ECI circuit pack as the master and the other ECI circuit pack as the slave (on a system reset, ECI-1 is designated the master). For example, when using a GTP on a TABS/TBOS link, the GTP must be connected to ECI-1 (CILINK-1-4) in the initial installation. ECI-1 becomes the slave only when it fails and is restored (**RST-EQPT** command) without resetting the frame. When ECI-1 fails, ECI-2 becomes the master and the GTP connection must be moved to ECI-2 (CILINK-2-4) if your office procedures do not require a system reset when ECI-1 fails; otherwise, the GTP connection remains on CILINK-1-4 and a system reset is performed after replacing ECI-1.

Figure 4-2 and Table 4-2 summarize the interfaces provided by the DACS IV-2000.




**Notes:**

1. One or two P links.
2. Up to eight DS3PMs per link.
3. Up to 16 DS3PMs per DACS IV-2000 system.

Figure 4-2. System Interfaces

Table 4-2. Link Characteristics

| Interface (Figure 4-2) | Physical | Baud | Electrical | Functional |
|---|---|---|---|---|
| CILINK 1-1 and 2-1 | EIA-232-D | 300, 1200, 2400, 4800, and 9600<br>Default: 9600* | EIA-232-D | Async. Snider |
| CILINK 1-2 and 2-2 | EIA-449 | 300, 1200, 2400, 4800, and 9600<br>Default: 2400* | EIA-423 | Async. Snider |
| CILINK 1-3 and 2-3 | EIA-449 | 300, 1200, 2400, 4800, and 9600<br>Default: 9600* | EIA-423 | Async. Snider |
| CILINK 1-4† and 2-4† | EIA-449 | **TABS/TBOS**: 2400<br>System value: 2400<br>**Snider**: 300, 1200, 2400, 4800, and 9600<br>Default: 9600* | EIA-485 | TABS/TBOS point-to-point AS&C or Async. Snider |
| CILINK 1-5, 1-6, 2-5, and 2-6 | EIA-449 | Based on external timing.<br>System value: 9600 | EIA-423 | Sync. X.25 or Async. Terminal Interface with external PAD |
| P1 and P2 (optional) | Connector | 2400 | RS-485 | TABS Async. multipoint DS3PM |
| L | Wirewrap | - | Closures | Local alarms (Visual and Audible) |

See footnotes at end of table.

Table continued on next page.

| Interface (Figure 4-2) | Physical | Baud | Electrical | Functional |
|---|---|---|---|---|
| R | Wirewrap | - | Closures | Remote alarms (GTP) |
| A | Wirewrap- | - | Closures | Remote ACO |

**Notes:**

* For maintenance reasons, it is recommended that default values be used when provisioning CILINKs.

† CILINKs 1-4 and 2-4 have the same characteristics as CILINKs 1-2, 1-3, 2-2, and 2-3 when CILINK 1-4 or 2-4 is provisioned as a Snider link.

1. All EIA-423 links are interoperable with EIA-232-D via the use of the suggested adaptors. For Snider links DACS IV-2000-to-terminal communication, it is suggested the ED-2C646,G1 adapter be used. For Snider links DACS IV-2000-to-OS via modem communication, it is suggested the ED-2C646,G2 adapter be used.
2. Links 1-2 and 2-2 are electrically compatible with the EIA-232-D (see note 1) standard up to 4800 baud. Links 1-3 and 2-3 are electrically compatible with the EIA-232-D standard up to 9600 baud. Although these links may operate with the EIA-232-D above these data rates, the four percent rise time specification of EIA-232-D is violated.
3. To supply internal timing for the X.25 links, the ED-2C646,G7 adapter must be used and the baud rate is fixed at 9600. All baud rates can be used with an external timing source.

Twelve administrative links on two ECI circuit packs support the operations, administration, maintenance, and provisioning functions. They are:

- CILINKs 1-1 through 1-3 and 2-1 through 2-3 - are asynchronous links (convertible to EIA-232 with an optional passive adapter). CILINKs 1-1 and 2-1 supports the local user interface, and CILINKs 1-2, 1-3, 2-2, and 2-3 support remote terminals and OSs, such as 2A Switching Control Center System (2ASCCS) or 2BSCCS, using the SCCS AI (asynchronous interface, also called Snider) protocol. These Snider interfaces operate at 300, 1200, 2400, 4800, or 9600 baud.
- CILINKs 1-4 and 2-4 - can be provisioned as asynchronous TABS or TBOS links operating at 2400 baud or Snider links operating at 300 to 9600 baud.
- CILINKs 1-5, 1-6, 2-5, and 2-6 - can be provisioned to use either the synchronous X.25 protocol or asynchronous link with the addition of an external Packet Assembler and Disassembler (PAD) device. Each X.25 link supports CCITT MML on as many as four virtual circuits. The synchronous interfaces operate at up to 9600 baud as determined by the external devices.

All CILINKs support the message set (TL1, Issue 4) for communication with Bellcore, Operations Systems/Intelligent Network Elements (OPS/INE) and Network Monitoring and Analysis (NMA).

The optional DS3PM multipoint asynchronous interface (P1 and P2) operates at 2400 baud. A general telemetry processor (GTP) remote processor can be connected to these links and interfaced to a modem over an E2A or compatible data link to the telemetry OS. These links provide DS3 path performance data to telemetry-based OSs.

Figure 4-3 shows the location of the CILINK TTY connectors on the back of the Redundant Controller Module.

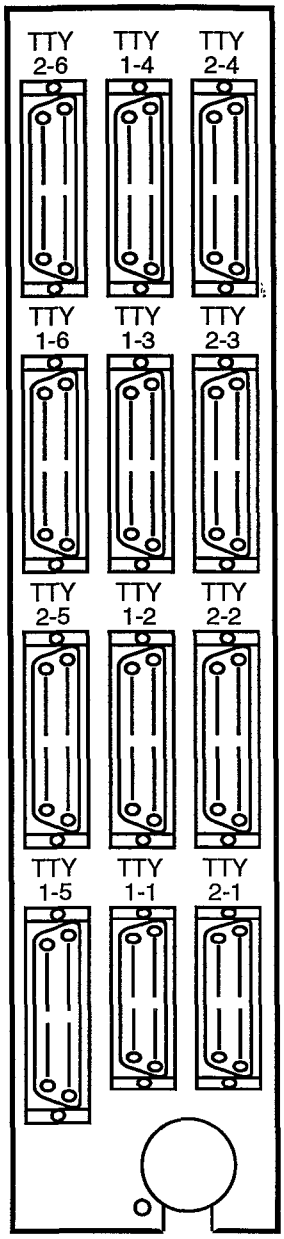



Figure 4-3. **CILINK Connectors at the Back of the Redundant Controller Module**

# Indicators and Switches

The following sections describe the indicators and switches found on the Status Panel and circuit packs.

## Indicators

All circuit packs (except version 1Synchronizer and BXA circuit packs) have a red LED indicator for trouble isolation. The LEDs flash on and off at 1-second intervals on circuit packs that have input DS1, DS3, or STS-1 signal failures and on the Synchronizer Module circuit packs that have a timing reference failure. The LEDs stay on for internal circuit pack failures. The normal LED condition is off. In addition to the LED alarm indication, `REPT ALM` messages are generated for all system circuit pack and facility failures.

Power circuit packs have green LEDs that indicate normal operation. They also have red LEDs for trouble isolation as described above.

The CPU circuit packs have green LEDs to indicate the on-line CPU and version 2 Synchronizer circuit packs have green LEDs to indicate the active side.

The disk drives (PRI and SEC) have both green and red LEDs. The green LED indicates that the disk drive is In Service, and the red LED indicates that the disk drive has been manually removed from service or has failed.

The MUXPS and DS1RY circuit packs have green LEDs to indicate protection is active.

The status panel (Figure 4-4) has eight equipment indicators:

- CRITICAL — is red and signals a critical alarm condition.
- MAJOR — is red and signals a major alarm condition.
- MINOR — is yellow and signals a minor alarm condition.
- ABNORMAL — reserved for future use.
- ACO (Alarm CutOff) — is green and shows that the audible alarms have been silenced (ACO switch activated).
- POWER ON — green LED that indicates that power is present at the status panel
- FAILURE — is a red processor major alarm and signals a failure in the RC module.
- FAR END — reserved for future use.

When the main controller (MC) is in the OOS-MCOND state and if the MTC circuit pack of the active control complex (CC) is extracted, the alarm LEDs on the Status Panel turn off and remain off until a system reset is performed.

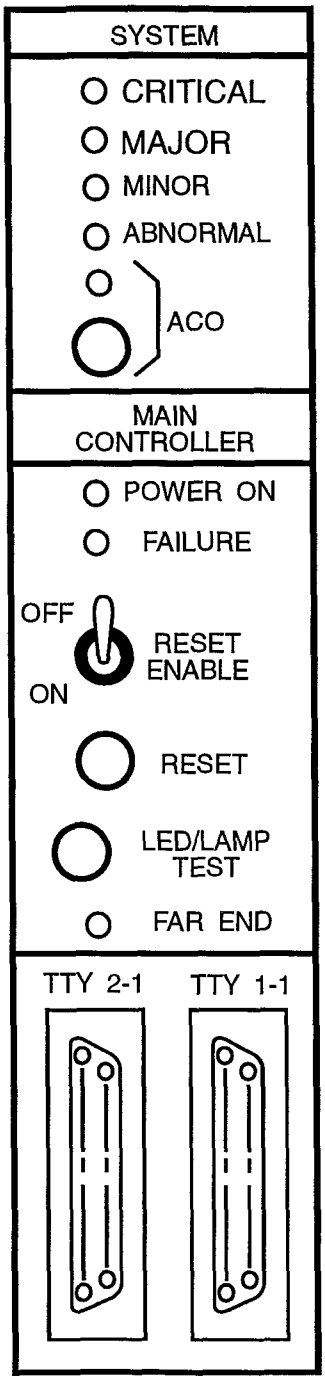



Figure 4-4. **Status Panel**

## Equipment Control Switches

The Status Panel (Figure 4-4) in the Redundant Controller Module has four momentary contact switches used for equipment control. They are:

- ACO (alarm cutoff) — silences the audible alarms when pressed.
- LED/LAMP TEST — tests the operation of the LEDs/lamps in the DACS IV-2000 frame. This function is performed on a per-shelf basis in sequential order. Pressing this switch is equivalent to entering the **EX-EQPT** command. If the system is busy executing another command, there is a delay before the LEDs light. When this switch is pressed, the LEDs on the Redundant Controller Module, Status Panel (except FAR END LED), Switch Power Modules, Switch Module, and provisioned interface modules are lit on a module-by-module basis.
- RESET — resets the DACS IV-2000. The RESET switch starts the reset function when operated simultaneously with the RESET ENABLE switch. This combination allows the main controller to be booted manually. Requiring simultaneous operation of the RESET and RESET ENABLE switches helps prevent the reset function from being initiated accidentally.
- RESET ENABLE — See RESET above.

The Status Panel also has two TTY connectors (TTY 1-1 and TTY 2-1) that allow the user interface terminal (UIT) to be used from the front of the frame.

The Redundant Controller Module has twelve administrative link connectors, TTY 1-1 through TTY 1-6 and TTY 2-1 through TTY 2-6 located on the back. In addition, two connectors, Q2 1-1 and Q2 2-1 located on the back, are reserved for future use.

**⚠ CAUTION:**
*Never connect terminals to the same TTY jack on the Status Panel and the TTY jack on the RC Module at the back of the Switch Bay (for example, never connect terminals to both jacks for TTY1-1 at the same time).*

## EMC Enclosure Header Alarm Indicators

With the EMC option for the DACS IV-2000, the front of the Switch Bay is covered with EMC doors to help eliminate electromagnetic interference. Because of this, the visual alarm indicators are only visible when viewed straight on. In addition to the EMC doors, a Header Designation Assembly (HDA) (Figure 4-5) is provided to house the additional alarm indicators:

Switch Bay HDA contains:

- a green Power On indicator lamp
- a red Critical alarm indicator lamp
- a red Major alarm indicator lamp
- a yellow Minor alarm indicator lamp
- a red MC Failure alarm indicator lamp
- a header assembly Lamp Test button.

When lit, the green Power On indicator lamp indicates power is available; when off, it indicates the power has failed.

When lit, the alarm indicator lamps indicate an alarm of the associated severity is present.

When lit, the MC Failure indicator lamp indicates the Main Controller has failed.

The header assembly Lamp Test button is used to test the header assembly indicator lamps.

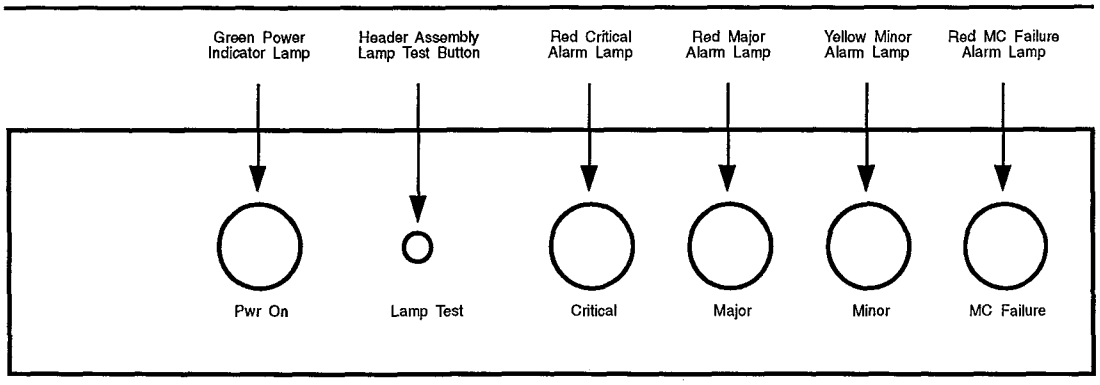



Figure 4-5. **Header Designation Assembly**

# Alarm and Timing Terminal Strip Panel

The DACS IV-2000 provides a terminal strip panel that allows access to the central office alarm system and BITS timing references. Figure 4-6 shows the BITS reference terminals (TS0 and TS1 located on the left side of the Terminal Strip Panel above the Fuse Panel), and Figure 4-7 shows the office and telemetry alarm terminals (TS2 located on the right side of the Terminal Strip Panel). Table 4-3 identifies the connections available through the terminal strips, and is provided as reference information. The connections from this terminal strip to the central office alarm system are made at installation or when the DACS IV-2000 frame is relocated. This access provides for:

- Central office audible and visual alarms for the DACS IV-2000
- Remote monitoring and resetting of the DACS IV-2000
- Central office BITS timing references

The terminal strip is located at the top of the switch bay above the fuse and alarm panel. In order to access the terminal strip, the cover plate must be removed. Under normal operations and in procedures contained in this manual, the terminals do not need to be accessed.

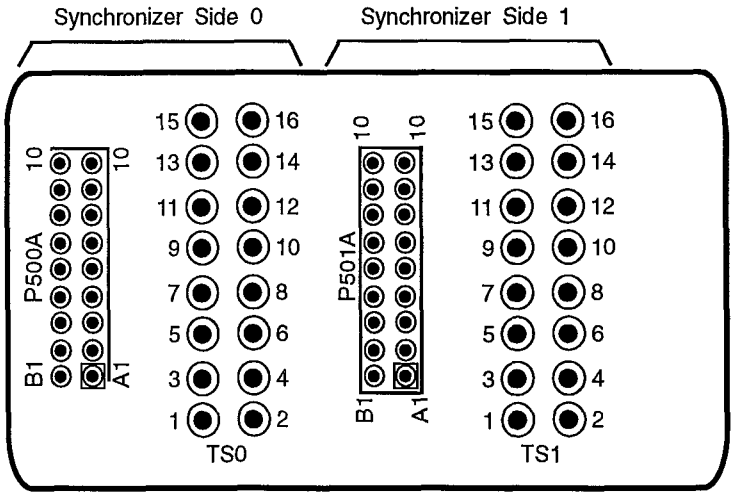



Figure 4-6. **BITS Timing Terminals**

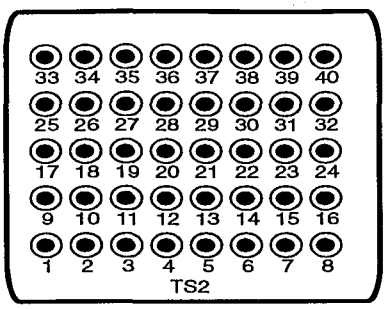



Figure 4-7. Office and Telemetry Alarm Terminals

Table 4-3. Terminal Strip Point Connections

| Terminal | System Signal | Central Office Connection |
|---|---|---|
| **Terminal Strip TS0 (BITS Timing Reference to Synchronizer Side 0)** | | |
| 13 | SYNCPRI-0 (Tip) | BITS Reference |
| 14 | SYNCPRI-0 (Ring) | BITS Reference |
| 15 | SYNCSEC-0 (Tip) | BITS Reference |
| 16 | SYNCSEC-0 (Ring) | BITS Reference |
| **Terminal Strip TS1 (BITS Timing Reference to Synchronizer Side 1)** | | |
| 13 | SYNCPRI-1 (Tip) | BITS Reference |
| 14 | SYNCPRI01 (Ring) | BITS Reference |
| 15 | SYNCSEC-1 (Tip) | BITS Reference |
| 16 | SYNCSEC-1 (Ring) | BITS Reference |
| **Terminal Strip TS2 (Office and Telemetry Alarms)** | | |
| 1 | Minor Audible Alarm Return | Local Office Alarm |
| 2 | Minor Audible Alarm | Local Office Alarm |
| 3 | Major Audible Alarm Return | Local Office Alarm |
| 4 | Major Audible Alarm | Local Office Alarm |
| 5 | Major Visual Alarm Return | Local Office Alarm |
| 6 | Major Visual Alarm | Local Office Alarm |
| 7 | Minor Visual Alarm Return | Local Office Alarm |
| 8 | Minor Visual alarm | Local Office Alarm |

Table continued on next page.

Table 4-3. **Terminal Strip Point Connections (Continued)**

| Terminal | System Signal | Central Office Connection |
|---|---|---|
| 9 | Remote ID Return | Remote Alarm |
| 10 | Remote ID | Remote Alarm |
| 11 | Remote Minor Alarm Return | Remote Alarm |
| 12 | Remote Minor Alarm | Remote Alarm |
| 13 | Remote Major Alarm Return | Remote Alarm |
| 14 | Remote Major Alarm | Remote Alarm |
| 15 | Remote Reset B | Remote Alarm |
| 16 | Remote Reset A | Remote Alarm |
| 17 | Critical Audible Alarm Return | Local Office Alarm |
| 18 | Critical Audible Alarm | Local Office Alarm |
| 19 | Critical Visual Alarm Return | Local Office Alarm |
| 20 | Critical Visual Alarm | Local Office Alarm |
| 22 | Remote Critical Alarm Return | Remote Alarm |
| 23 | Remote Critical Alarm | Remote Alarm |
| 24 | Processor Major Visual Alarm Return | Local Office Alarm |
| 25 | Processor Major Visual Alarm | Local Office Alarm |
| 26 | Remote Processor Major Alarm Return | Remote Alarm |
| 27 | Remote Processor Major Alarm | Remote Alarm |
| 28 | Remote LED Test Switch Return | Not Connected |
| 29 | Remote LED Test Switch | Not Connected |
| 30 | Remote ACO Switch Return | Not Connected |
| 31 | Remote ACO Switch | Not Connected |

**Notes:**

1. All terminal locations not listed are not used.
2. Cables for connections to remote reset, remote alarm, local office alarm, and the BITS timing references in the central office are not supplied with the DACS IV-2000 frame.

# Technical Specifications

# A

## Contents

# Contents

# Technical Specifications

# A

This appendix describes the technical specifications that must be considered when engineering the DACS IV-2000 (256) Release 4.0 into a network. It provides technical specifications for the following areas:

- Interface
- Commands and messages
- System performance
- Power
- Physical
- Environmental
- Availability and reliability.

## Interface Specifications

This section describes the transmission interface and the alarm and control interface specifications for the DACS IV-2000.

## Transmission Interface

The transmission interface characteristics of the DACS IV-2000 include the port capacity, signal characteristics, signal impairments, and cable characteristics. Each of these areas is described, and the particular specifications and requirements associated with each area are listed.

### Port Capacity

Port capacity defines the number of DS1, DS3, and/or STS1 ports that can be terminated on the DACS IV-2000 and is a function of the number and types of interface bays. The maximum configurations include:

- 6944 DS1 ports for a 9-bay arrangement consisting of all DS1 ports (248 equivalent DS3s)
- 248 DS3 ports for a 5-bay arrangement consisting of all DS3 ports
- 240 STS1 ports for a 5-bay arrangement consisting of all STS1 ports.

Bay arrangements include:

- 9-bay arrangement: one Switch Bay and eight DS1 Interface Bays
- 5-bay arrangement: one Switch Bay and four DS3 Interface-32 Bays
- 5-bay arrangement: one Switch Bay and four STS1 Interface-16 Bays.

The port capacities of the DACS IV-2000 are summarized in Table A-1.

Table A-1. **Port Capacity**

| Item | Value |
|---|---|
| Maximum System Capacity | Up to 248 equivalent DS3 or 240 STS1 input and output interface ports |
| Maximum DS1 Port Capacity | Up to 6944 input and output DS1 interface ports |
| Maximum DS3 Port Capacity | Up to 248 input and output DS3 interface ports |
| Maximum STS1 Port Capacity | Up to 240 input and output STS1 interface ports |

## Signal Characteristics

The transmission interfaces to the DACS IV-2000 are DSX-3, DSX-1, and STSX-1 compatible facilities or network elements.

### DS3 Signal

The DACS IV-2000 accepts incoming DS3 signals at the specified line rate of 44.736 Mbits/s with the specified B3ZS line code. Acceptable signal formats are asynchronous M13 or C-bit parity. (See Table A-2.)

Table A-2. DS3 Signal Characteristics

| Item | Value |
|---|---|
| Frame Format | Asynchronous M13/C-bit parity |
| DS3 Line Rate | 44.736 Mbits/s ±20 ppm |
| Line Code | B3ZS |
| Test Load Impedance | 75Ω ±5% resistive, unbalanced |

### DS1 Signal

The DACS IV-2000 accepts incoming DS1 signals at the specified line rate of 1.544 Mbits/s with the specified AMI or B8ZS line code. (See Table A-3.) The DACS IV-2000 is fully transparent to the DS1 bit stream; that is, all overhead and payload bytes are passed through unchanged.

Table A-3. DS1 Signal Characteristics

| Item | Value |
|---|---|
| DS1 Line Rate | 1.544 Mbits/s ±130 ppm |
| Line Code | AMI or B8ZS |
| Test Load Impedance | 100Ω ±5% resistive, balanced |

### STS-1 Signal

The DACS IV-2000 accepts incoming STS-1 signals at the specified line rate of 51.84 Mbits/s with the specified B3ZS line code. (See Table A-4.)

Table A-4. **STS-1 Signal Characteristics**

| Item | Value |
|---|---|
| STS-1 Signal Format | Conforms to TR-NWT-000253 |
| STS-1 Line Rate | 51.84 Mbits/s ±4.6 ppm |
| Line Code | B3ZS |
| Duty Cycle (measured at output cable terminals) | Nominal 50%, RZ pulse with 1.03V (±10%) peak output amplitude |
| Frame Synchronous Scrambling | Conforms to TR-NWT-000253 |
| Wideband Power Level | -2.7 dBm to 4.7 dBm (measured at 450 ft) |

## Signal Impairments

The requirements related to signal impairments in electronic digital signal cross-connect equipment are specified in Bellcore TA-TSY-000241. The requirements applicable to the DACS IV-2000 are summarized in the following paragraphs.

### DS3 Signal

The jitter accommodation (tolerance) requirement for a DS3 signal input is specified in terms of the amount of sinusoidal jitter (peak-to-peak) that must be accommodated versus the frequency of that jitter. The DACS IV-2000 meets the jitter accommodation requirements for a DS3 signal given in Bellcore TR-NWT-000499. The DACS IV-2000 does not generate more than 0.01 unit interval (UI; timeslots) of rms jitter with a high-pass measurement filter with 12-kHz cutoff frequency. Jitter generation at the DS3 outputs of the DACS IV-2000 is negligible.

The peak signal-to-rms noise (S/N) power ratio for an *all ones* pattern measured over the bandwidth of the digital signal in the DACS IV-2000 is greater than 46 dB on any digital output line signal.

The return loss at a half bit rate (normal cross-connection) measured at the input of a cross-connection in the DACS IV-2000 is greater than 18 dB. The cross-connection must be properly terminated when making this measurement.

The DACS IV-2000 provides better than 46-dB (measured at 22.368 MHz) isolation between any two DS3 output ports.

The DS1-to-DS3 nominal transmission delay (normal cross-connection) through the DACS IV-2000 is 21 µs for AMI-coded DS1 inputs and 25.5 µs for B8ZS-coded DS1 inputs. The DS3-to-DS3 nominal transmission delay (normal cross-connection) through the DACS IV-2000 is 19 µs.

The DACS IV-2000 provides an operational bit error rate (BER) of less than $10^{-10}$ per cross-connect path across the system regardless of the number of other cross-connections established. The DS3 signal impairment specifications are listed in Table A-5.

Table A-5. **DS3 Signal Impairment Specifications**

| Item | Value |
|---|---|
| Jitter Accommodation | Conform to TR-TSY-000009 (Figure 7) and TR-NWT-000499 (Figure 7-2) |
| Jitter Generation (rms) | < 0.01 UI |
| S/N Power Ratio | > 46 dB for all ones signal pattern |
| Return Loss at 22.368 MHz (normal cross-connection) | >18 dB |
| Crosstalk | > 46-dB isolation between any two DS3 output ports |
| Transmission Signal Delay DS1 to DS3 (normal cross-connection) | 21.0 µs (AMI), 25.5 µs (B8ZS) |
| Transmission Signal Delay DS3 to DS3 | 19 µs |
| Bit Error Rate (BER/cross-connect path) | $< 1 \times 10^{-10}$ |

## DS1 Signal

The jitter accommodation (tolerance) requirement for a DS1 signal input is specified in terms of the amount of sinusoidal jitter (peak-to-peak) that must be accommodated versus the frequency of that jitter. The DACS IV-2000 meets the jitter accommodation requirements for a DS1 signal given in Figure 7 of Bellcore TR-TSY-000009, and Figure 7-2 of Bellcore TR-NWT-000499. The DACS IV-2000 does not generate more than 0.3 UI of rms jitter or more than 1 UI of peak-to-peak jitter over a 10-Hz to 40-kHz jitter spectrum in the absence of input jitter.

The peak signal-to-rms noise (S/N) power ratio for an *all ones* pattern measured over the bandwidth of the digital signal in the DACS IV-2000 is greater than 46 dB on any digital output line signal.

The return loss at a half bit rate (normal cross-connection) measured at the input of a cross-connection in the DACS IV-2000 is greater than 18 dB. The cross-connection must be properly terminated when making this measurement. The DACS IV-2000 provides better than 46-dB (measured at 772 kHz) isolation between any two DS1 output ports.

The DS1-to-DS1 nominal transmission delay (normal cross-connection) through the DACS IV-2000 is 23.5 μs for AMI-coded DS1 inputs/outputs and 33 μs for B8ZS-coded DS1 inputs/outputs. The nominal DS1 line loopback transmission delay is 3 μs.

The DS1 signal impairment specifications are summarized in Table A-6.

Table A-6. **DS1 Signal Impairment Specifications**

| Item | Value |
|---|---|
| Jitter Accommodation | Conform to TR-TSY-000009 (Figure 7) and TR-NWT-000499 (Figure 7-2) |
| Jitter Generation (rms) | < 0.3 UI |
| Jitter Generation (peak-to-peak) | < 1.0 UI |
| S/N Power Ratio | > 46 dB for all ones signal pattern |
| Return Loss at 772 kHz (normal cross-connection) | >18 dB |
| Crosstalk | > 46-dB isolation between any two DS1 output ports |
| Transmission Signal Delay DS1 to DS1 (normal cross-connection) | 23.5 μs (AMI), 33 μs (B8ZS) |
| Transmission Signal Delay DS1 Line Loopback | 3.0 μs |
| Bit Error Rate (BER/cross-connect path) | $< 1 \times 10^{-10}$ |

## STS-1 Signal

The jitter accommodation (tolerance) requirement for an STS-1 signal input is specified in terms of the amount of sinusoidal jitter (peak-to-peak) that must be accommodated versus the frequency of that jitter. The DACS IV-2000 meets the jitter accommodation requirements for an STS-1 signal given in Bellcore TA-NWT-000253. The DACS IV-2000 does not generate more than 0.01 UI of rms jitter with a high-pass measurement filter with 12-kHz cutoff frequency.

The STS-1 signal impairment specifications are summarized in Table A-7.

Table A-7. **STS-1 Signal Impairment Specifications**

| Item | Value |
|---|---|
| Jitter Accommodation | Conform to TA-NWT-000253 |
| Jitter Transfer (terminating DS1 signals on STS1 interfaces) | Conform to TA-NWT-000253 |
| Jitter Amplitude (terminating DS1 signals on STS1 interfaces) | < 5 UI peak-to-peak |
| Jitter Generation (rms) | < 0.01 UI |

## Cable Characteristics

There are various options available in the types and length of cables and the types of connectors used for interconnection of the DACS IV-2000 either to a DSX-1, DSX-3, STSX-1, or directly to another network element (NE).

### DS3 Interface Cable and Connectors

The DACS IV-2000 supports both overhead and underfloor type cable distribution. The DS3 interface cable and connector characteristics are summarized in Table A-8.

Table A-8. DS3 Cable and Connector Characteristics

| Item | Value |
|---|---|
| Maximum Distance to DSX-3 (KS-19224 type cable) | 150 ft |
| Maximum Distance to DSX-3 (734-type cable*) | 450 ft |
| Maximum Distance to DSX-3 (735-type cable) | 250 ft |
| Maximum Distance to DS3 NE (KS-19224 type cable) | 300 ft |
| Maximum Distance to DS3 NE (734-type cable*) | 900 ft |
| Maximum Distance to DS3 NE (735-type cable) | 500 ft |
| DS3 Connector Type (982-type) at the DACS IV-2000 | 2 x 4 |
| DS3 Connector Type (at DS3 NE) | connectorized |

* Identical characteristics to previous 728B-type cable.

## DS1 Interface Cable and Connectors

The DACS IV-2000 supports both overhead and underfloor type cable distribution. The DS1 interface cable and connector characteristics are summarized in Table A-9.

Table A-9. DS1 Cable and Connector Characteristics

| Item | Value |
|---|---|
| Maximum Distance to DSX-1 (600-type cable) | 655 ft |
| Maximum Distance to DSX-1 (1249-type cable*) | 450 ft |
| Maximum Distance to DS1 NE (600-type cable) | 1310 ft |
| Maximum Distance to DS1 NE (1249-type cable*) | 900 ft |
| DS1 Connector Type (963T) or Wirewrap at the DACS IV-2000 | 2 x 14 (in)<br>1 x 28 (out) |
| DS1 Connector Type (at DSX-1) | wirewrap |

* 1249 is preferred for overhead installation; required for underfloor installation.

### STS1 Interface Cable and Connectors

The DACS IV-2000 supports both overhead and underfloor type cable distribution. The STS1 interface cable and connector characteristics are summarized in Table A-10.

Table A-10. STS1 Cable and Connector Characteristics

| Item | Value |
|---|---|
| Maximum Distance to STSX-1 (735-type cable or equivalent) | 450 ft |
| Maximum Distance to STS1 NE (734-type cable or equivalent) | 900 ft |
| STS1 Connector Type (982-type) at the DACS IV-2000 | 2 x 4 |
| STS1 Connector Type (at STSX-1) | connectorized |

## Alarm and Control Interfaces

The alarm and control interfaces for the DACS IV-2000 consist of office and telemetry alarms, technician, telemetry, and operations systems (OSs). Each of these interfaces is discussed, and the particular specifications and characteristics associated with each interface are given.

### Office and Remote Alarms

The DACS IV-2000 has seven office alarm outputs: Critical Audible; Critical Visual; Major Audible; Major Visual; Minor Audible; Minor Visual; and Main Controller Failure. Contact closures for visual alarms remain latched until the failure is cleared.

The DACS IV-2000 provides a set of relay closures for critical, major, and minor alarms, which can be picked up by a remote telemetry system in the local office and sent to the appropriate OS.

All alarm contacts are rated as follows: maximum current (1.0A), maximum voltage (48V), and maximum volt-amperage (25 VA).

The activation of the alarms is delayed to avoid calling technicians to respond to transient errors of short duration. The alarm delay is programmable over a range of 1 to 30 seconds. The alarm delay operates on all audible and visual office alarm outputs, including major and minor visual indicators, autonomous messages, and OS (telemetry) alarm points. The OS status points associated with the delayed alarm points is similarly delayed.

The minimum alarm duration is 20 seconds for all office audible and visual alarm outputs, major and minor visual indicators, and OS (telemetry) alarm points. The minimum duration is not programmable. All alarm points are stretched to a total of at least 20 seconds beyond the programmed delay interval, even if the condition causing the alarm does not persist for the 20-second interval.

The office and telemetry alarm types and requirements for the DACS IV-2000 are summarized in Table A-11.

Table A-11. **Office and Telemetry Alarms and Requirements**

| Item | Value |
|---|---|
| Office Audible Alarms | Critical, Major, Minor |
| Office Visual Alarms | Critical, Major, Minor, MC Fail |
| Remote Telemetry Alarms | Critical, Major, Minor, MC Fail Remote Indicator |
| Alarm Contact Closure Rating | 1.0A, 48V, 25 VA (max) |
| Alarm Holdoff Delay (non-SONET facilities and equipment) | 1 to 30 sec (default 10 sec) |
| Alarm Clear Delay (non-SONET facilities and equipment) | 1 to 20 sec (default 10 sec) |
| Soak Time — Alarm Onsets (SONET facilities) | 1 to 30 sec (default 2 sec) |
| Soak Time — Alarm Clears (SONET facilities) | 1 to 20 sec (default 10 sec) |
| GTP Poll Time | 10 to 60 sec (default 20 sec) |

## Link and OS Interfaces

Table A-12 summarizes the characteristics of the links connecting technician and OSs to the DACS IV-2000.

Table A-12. Link Characteristics

| Interface | Physical | Baud | Electrical | Functional |
|---|---|---|---|---|
| CILINK 1-1 and 2-1 | EIA-232-D | 300, 1200, 2400, 4800, and 9600<br>Default: 9600* | EIA-232-D | Async. Snider |
| CILINK 1-2 and 2-2 | EIA-449 | 300, 1200, 2400, 4800, and 9600<br>Default: 2400* | EIA-423 | Async. Snider |
| CILINK 1-3 and 2-3 | EIA-449 | 300, 1200, 2400, 4800, and 9600<br>Default: 9600* | EIA-423 | Async. Snider |
| CILINK 1-4† and 2-4† | EIA-449 | **TABS/TBOS**: 2400<br>System value: 2400<br>**Snider**: 300, 1200, 2400, 4800, and 9600<br>Default: 9600* | EIA-485 | TABS, TBOS, or async. Snider point-to-point AS&C |
| CILINK 1-5, 1-6, 2-5, and 2-6 | EIA-449 | Based on external timing.<br>System value: 9600 | EIA-423 | Sync. X.25 or Async. Terminal Interface with external PAD |

**Notes:**

* For maintenance reasons, it is recommended that default values be used when provisioning CILINKs.

† CILINKs 1-4 and 2-4 have the same characteristics as CILINKs 1-2, 1-3, 2-2, and 2-3 when CILINK 1-4 or 2-4 is provisioned as a Snider link.

1. All EIA-423 links are interoperable with EIA-232-D via the use of the suggested adaptors. For Snider links DACS IV-2000-to-terminal communication, it is suggested the ED-2C646,G1 adapter be used. For Snider links DACS IV-2000-to-OS via modem communication, it is suggested the ED-2C646,G2 adapter be used.
2. Links 1-2 and 2-2 are electrically compatible with the EIA-232-D (see note 1) standard up to 4800 baud. Links 1-3 and 2-3 are electrically compatible with the EIA-232-D standard up to 9600 baud. Although these links may operate with the EIA-232-D above these data rates, the four percent rise time specification of EIA-232-D is violated.
3. To supply internal timing for the X.25 links, the ED-2C646,G7 adapter must be used and the baud rate is fixed at 9600. All baud rates can be used with an external timing source.

## Protocols

The message interface protocol for Links 1-1, 1-2, 1-3, 2-1, 2-2, and 2-3 is Snider, which is defined in Bellcore FR-NWT-000064, and FSD 35-08-0100, *SPCS (Stored Program Control Systems) OS Interface, SCCS (Switching Control Center System), Asynchronous Interface.*

The message interface protocol for Links 1-4 and 2-4 (TABS/TBOS) is specified in Compatibility Bulletin 149, *Maintenance Standards for Digital Transmission Systems* (Issue 4).

The message interface protocol for Links 1-4 and 2-4 (when provisioned for Snider) is Snider, which is defined in Bellcore FR-NWT-000064, and FSD 35-08-0100, *SPCS (Stored Program Control Systems) OS Interface, SCCS (Switching Control Center System), Asynchronous Interface.*

The synchronous Links 1-5, 1-6, 2-5, and 2-6 operate up to 9600 baud. The message interface protocol for the four links is X.25 as verified with Bellcore TR-NWT-001213, or asynchronous terminal interface with the use of an external PAD.

The network layer for the synchronous links is X.25. The DACS IV-2000 meets the CCITT X.25 1984 specification and has been verified with Bellcore TR-NWT-001213.

## Snider Link Specifications

The specifications for links 1-1, 1-2, 1-3, 2-1, 2-2, and 2-3 are summarized in Table A-13.

Table A-13. **Links 1-1, 1-2, 1-3, 2-1, 2-2, and 2-3 Specifications**

| Item | Value |
|---|---|
| Communications Interface Terminal Ports | Four EIA-449/EIA-423 asynchronous (1-2, 1-3, 2-2, and 2-3)<br>Two EIA-232-D per EIA IEB No.12 (1-1 and 2-1) |
| Baud | 300, 1200, 2400, 4800, or 9600 |
| Communications Interface Terminal Type | AT&T 4425 or compatible terminal |
| Communications Interface Terminal Interaction | Command and Menu modes |
| Communications Interface Interconnections | Connectorized |

## TABS/TBOS Link Specifications

The DACS IV-2000 has a TABS/TBOS port as an electrical interface to a telemetry-based operations system. The electrical interface specifications are given in Compatibility Bulletin 149, *Maintenance Standards for Digital Transmission Systems* (Issue 4). The interface can be connected to the monitoring equipment on a point-to-point basis. The interface operates at 2400 baud.

All alarm and status indications available over the user interface link are also available over the TABS/TBOS telemetry link. (Note that the mapping between user and telemetry interfaces is not on a one-to-one basis.) The only control functions available over the telemetry links are protection switches and locks, and CLKGN circuit pack switches.

The specifications for links 1-4 and 2-4 are summarized in Table A-14.

Table A-14. **Links 1-4 and 2-4 Specifications**

| Item | Value |
|---|---|
| Telemetry Interface Port | TABS/TBOS or Snider asynchronous point-to-point |
| Baud | 2400 (TABS/TBOS)<br>300, 1200, 2400, 4800, or 9600 (Snider) |
| Telemetry Interface Protocol | TABS/TBOS or Snider |

## X.25 Link Specifications

The DACS IV-2000 has two synchronous EIA-449/EIA-423 ports for electrical interfaces to message-based OSs. The electrical interface specifications are given in EIA Standard 449 (November 1977). The synchronous links have the balanced voltage signals of EIA-423. The functions that can be performed over the synchronous links depend on the OS. The links can be converted to an asynchronous terminal interface with the use of an external PAD.

The specifications for links 1-5, 1-6, 2-5, and 2-6 are summarized in Table A-15.

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Table A-15. **Links 1-5, 1-6, 2-5, and 2-6 Specifications**

| Item | Value |
|---|---|
| Physical/Electrical Interface Ports | EIA-449/EIA-423 synchronous or asynchronous |
| Baud | 9600 |
| Message Protocol | X.25 level 2 and 3 |
| Switched Virtual Circuits | Four per link |
| Cable Length | Up to 50 ft |

# Command and Message Specifications

The DACS IV-2000 message interface is compatible with two operations systems from Bellcore: the Operations Systems/Intelligent Network Elements (OPS/INE) and Network Monitoring and Analysis (NMA). This message set includes alarm, provisioning, administration, and maintenance (including test access and performance monitoring) commands and messages. This message set, known as Transaction Language 1, Issue 4, is based on the Bellcore special reports, technical advisories, and technical references listed in Table A-16.

Table A-16. **Command and Message Specifications**

| Document Number | Specification |
|---|---|
| SR-STS-001578 | *OPS/INE Generic Interface Support* (Issue 2, December 1992) |
| SR-STS-001665 | *Network Monitoring and Analysis Generic Network Element Interface Support* (Issue 2, December 1992) |
| TA-NWT-000199 | *Specification of Memory Administration Messages at the OS/NE Interface* (Issue 7, January 1993) |
| TA-NWT-000200 | *Specification of System Maintenance Messages at the OS/NE Interface* (Issue 5, December 1990) |
| TR-NWT-000811 | *OTGR: Operations Application Messages - TL1 Message Index* (Issue 2, May 1992) |
| TR-NWT-000818 | *OTGR Section 6.1: Network Maintenance: Access and Testing - Generic Test Architecture* (Issue 1, November 1992) |
| TR-NWT-000833 | *OTGR: Operations Application Messages Network Maintenance: Generic Requirements for Network Element and Transport Surveillance Messages, Section 12.3* (Issue 5, Revision 2, April 1993) |
| TR-NWT-000835 | *OTGR: Operations Application Messages - Network Element (NE) Security Parameter Administration Messages, Section 12.5* (Issue 3, Revision 1, May 1991) |

# System Performance Specifications

The system capabilities and performance specifications for the DACS IV-2000 include switch types and capacity, cross-connection capabilities, boot time, fault tolerance and protection, and maintenance. Each of these areas is discussed, and the particular specifications and requirements associated with each area are given.

## Switch Type and Capacity

All cross-connect related functions in the DACS IV-2000 are accomplished via a nonblocking, 3-stage space division switch. Nonblocking here implies the ability to access any/all of the free paths through the switch so that a connection from an input port to an output port can always be completed.

The switch type and capacity for the DACS IV-2000 are shown in Table A-17.

Table A-17. **Switch Capacity**

| Item | Value |
|---|---|
| Switch Type | Nonblocking, 3-stage space division switch |
| Switch Capacity | 7168 input and output switch ports (256 equivalent DS3s) |

## Cross-Connect Capability

The DACS IV-2000 supports four types of cross-connections:

- One-way
- Two-way
- Bridge
- Roll.

The execution time for a command depends on the type of command, speed and status of the administrative links, activities in the DACS IV-2000, and the status of the equipment in the system needed to make the connection.

The cross-connection capabilities of the DACS IV-2000 are described below and summarized in Table A-18.

The cross-connect command to the DACS IV-2000 can be one-way or two-way. The cross-connect setup time specification includes the time from which the system receives the command to the time the connection is made; it does not include the output message. The time to set up a one-way or two-way cross-connection is less than 1 second for DS1 and VT1.5 and less than 3 seconds for STS-1 clear-channel.

The DACS IV-2000 can bridge any existing connection by cross-connecting the input port to a second output port without affecting service (that is, the existing cross-connect path is not affected). The time to set up a bridge is less than 1 second for DS1 and VT1.5 and less than 3 seconds for STS-1 clear-channel.

A tail-end switch occurs when an existing cross-connect path is disconnected and a new cross-connection made at the tail-end of a facility. The in-service rolling operation requires that a tail-end switch be made in less than 2 ms (less than 3 ms for STS-1 clear-channel). In executing the tail-end switch (command), the DACS IV-2000 does not cause more than a 2-ms interruption in the transmission signal (error-free transmission is established within 2 ms), 3 ms for STS-1 clear-channel.

A one-way signal split of an existing cross-connect path between an input port and an output port is accomplished by rerouting the input port signal to a test output port and cross-connecting the signal from the test input port to the output port. The DACS IV-2000 does not cause more than a 2-ms interruption in the signal appearing at the output port (error-free transmission is established within 2 ms), 3 ms for STS-1 clear-channel.

The original cross-connect path is established automatically when the split function is disabled. In establishing the original cross-connection, the system does not cause more than a 2-ms interruption in the signal appearing at the output port (error-free transmission is established within 2 ms).

Table A-18. **Cross-Connect Capabilities**

| Cross-Connect Procedures | Value |
|---|---|
| One-way Cross-Connect Setup Time | < 1 sec (DS1, VT1.5)<br>< 3 sec (STS-1 clear-channel) |
| Two-way Cross-Connect Setup Time | < 1 sec (DS1, VT1.5)<br>< 3 sec (STS-1 clear-channel) |
| Bridge Setup Time | < 1 sec (DS1, VT1.5)<br>< 3 sec (STS-1 clear-channel) |
| Rolling (Signal Interruption Time) | < 2 ms<br>< 3 ms (STS-1 clear-channel) |
| One-way Signal Split (Signal Interruption Time) | < 2 ms<br>< 3 ms (STS-1 clear-channel) |

## Boot Time

The system boot time is the elapsed time from the moment a system reset request is made to the moment the system is ready for an input command. The boot time encompasses the downloading of all the system programs and the latest cross-connect maps from the hard disk to the appropriate controllers. If the information on the hard disk has been corrupted, additional time is required to restore the information to the hard disk from a backup optical disk before the DACS IV-2000 can be booted. The memory update procedures conform to Bellcore TA-NWT-000199.

The boot time specifications for the DACS IV-2000 are summarized in Table A-19.

Table A-19. **Boot Time Specifications**

| Procedure | Value |
|---|---|
| Cold Boot Time (from hard disk) | < 15 min |
| Cold Boot Time (from backup optical disk) | < 15 min |
| Restart Time (MC, ECI) | < 5 min |
| Memory Administration Procedures | Conform to TA-NWT-000199 |

## Fault Tolerance and Protection

The DACS IV-2000 can isolate a fault to the facility or equipment, and can isolate the fault to the equipment circuit pack level.

The DACS IV-2000 provides two provisionable input facility signal monitor alarm threshold BERs. The high category shows failures at $10^{-3}$, and the low category shows failures at $10^{-6}$. If the facility connects to a MUX2 circuit pack (DS3) or a SWIF2 circuit pack (DS1), you can choose from the following bit error rate thresholds: $10^{-3}$, $10^{-4}$, $10^{-5}$, $10^{-6}$,$10^{-7}$, $10^{-8}$, or $10^{-9}$ errors per second.

If the facility connects to an SMUX circuit pack (STS-1), you can choose from the following section and line bit error rate thresholds: $10^{-3}$, $10^{-4}$, $10^{-5}$, $10^{-6}$,$10^{-7}$, $10^{-8}$, or $10^{-9}$. At the local office, the incoming signal failures are indicated at the threshold you've specified (major, minor, or no alarm).

Any single hard equipment failure (a nontransient failure that can cause interruption in the transmission path) in the DACS IV-2000 is protected, and the protection switching capability restores error-free transmission within 60 ms from the moment such a failure occurs. Following a correct protection switch around a failed circuit pack and after the failed circuit pack is replaced by a new circuit pack, the health of this new circuit pack is checked and service is restored to this new circuit pack from the protection circuit pack automatically. The automatic restoration time is the elapsed time between the replacement of a circuit pack and the restoration of service to this new circuit pack. The automatic restoration time is less than 10 seconds. The automatic restoration does not cause more than a 60-ms interruption in the transmission path.

The DACS IV-2000 supplies DS1 idle (unframed all ones), STS-1 idle, or VT1.5 idle signals automatically to the output ports (toward facilities/DSX-3) to drive facilities that are not cross-connected through the DACS IV-2000. When an existing cross-connect path is disconnected, a DS1, STS-1, or VT1.5 idle signal is substituted at the output port in approximately 3 ms.

**NOTE:**
When STS-1 and VT1.5 signals are idle, the DACS IV-2000 outputs STS and VT path AIS, respectively.

The fault tolerance and protection specifications for the DACS IV-2000 are summarized in Table A-20.

Table A-20. **Fault Tolerance and Protection Specifications**

| Item | Value |
|---|---|
| Cross-Connect Path Monitoring | Continuous |
| Input Signal Alarm, BER Threshold (DS1 and DS3 interfaces) | > $10^{-3}$ through $10^{-6}$ (selectable) |
| Input Signal Alarm, BER Threshold (DS1 and DS3 interfaces) [optional] | $10^{-3}$ through $10^{-9}$ |
| Input Signal Alarm, Section BER Threshold (STS1 interfaces) | $10^{-3}$ through $10^{-9}$ |
| Input Signal Alarm, Line BER Threshold (STS1 interfaces) | $10^{-3}$ through $10^{-9}$ |
| Input Signal Failure Alarm | Major, Minor, or No Alarm (selectable) |
| Input Signal Failure Visual Indication | ALM (flashes at 1-sec intervals) |
| DS1 AIS Substitution Time (DS1 and DS3 interfaces) | < 3 ms |
| DS1 AIS Substitution Time (STS1 interfaces) | < 50 ms |
| STS-1 Path AIS Substitution Time | < 125 µs |
| VT1.5 Path AIS Substitution Time | < 500 µs |
| Protection Switching Time | < 60 ms |
| Automatic Restoration Time | < 10 sec |

## Frame Indicators and Controls

Eight visual equipment indicators are provided on the DACS IV-2000 status panel:

- CRITICAL signals a critical alarm condition; red
- MAJOR signals a major alarm condition; red
- MINOR signals a minor alarm condition; yellow
- ABNORMAL is reserved for future use
- ACO (alarm cutoff) signals that the audible alarms have been turned off (ACO switch activated); green
- POWER ON — green LED that indicates that power is present at the status panel
- FAILURE (Main Controller Failure) is a processor major alarm that signals a failure in the Redundant Controller Module; red
- FAR END is reserved for future use.

All circuit packs, except version one synchronizer circuit packs, contain a red LED to aid in problem identification. (In addition, some circuit packs contain a green LED to indicate that they are in service.) The LED is mounted so that it is visible while the circuit pack is in the equipment. The LED is controlled by a main/unit controller so that it can be illuminated even if the circuit pack it is mounted in is defective. In addition to the red LEDs, alarm messages are generated for all circuit-pack failures.

For the DS1, DS3, and STS1 interface circuit packs, as well as the DS1TX2 circuit pack, the LED indicators flash continuously at 1-second intervals on circuit packs that have input signal failures, and remain on for failures in the circuit packs themselves. (Circuit-pack failure indicators have a minimum duration of 2 seconds, to distinguish them from incoming signal failures.) The power circuit packs activate their respective LEDs when a fault exists. Because the power circuit pack failure LED is powered from the primary power supply, it lights even when there is a loss of logic level power.

Four controls (momentary-action push-button or toggle switches) are located on the DACS IV-2000 status panel:

- LED/LAMP TEST tests all LEDs in the DACS IV-2000 (except FAR END LED)
- RESET, when operated simultaneously with the RESET ENABLE switch, initiates the system reset function
- RESET ENABLE inhibits the reset function from being activated accidentally
- ACO silences the office audible alarms.

The alarm selection criteria in the DACS IV-2000 conform to Bellcore TR-TSY-000191.

The alarm indications for maintenance support are summarized in Table A-21.

Table A-21. **Visual Indicators**

| Item | Value or Specification |
|---|---|
| System Visual Indicators | CRITICAL, MAJOR, MINOR, ACO (alarm cutoff), FAILURE |
| Circuit Pack Failure Visual Indicator | ALM (2-second minimum duration); red LED lit (1-second flash for signal failure) |
| Protection Bus Active Visual Indicator | Green LED lit on MUXPS or DS1RY1 |
| Primary Disk Active Visual Indicator (when disk is spinning) | Green LED lit |
| Power Feed Status Visual Indicator | Green LED lit |
| System Controls | LED/LAMP TEST, RESET, RESET ENABLE, and ACO |
| Power Bus Failure Indicator (standard power)<br>Primary Fuse Indicator (duplex power | BUS ALM<br><br>Red LED lit on Fuse and Alarm Panel |
| Power Circuit Pack Failure Visual Indicator | ALM; red LED lit |
| Power Feed Status Visual Indicator | ON |
| Alarm Selection Criteria | Conform to TR-TSY-000191 |
| CPU (Control Complex) Active Visual Indicator | Green LED lit |
| Version Two Synchronizer Active Visual Indicator | Green LED lit |

# Power Specifications

The DACS IV-2000 frame is configured to accept two power supply arrangements, standard (existing frames upgraded to Release 4.0) or duplex (new frame orders). The standard configuration consists of one Battery Distribution Feeder Board (BDFB) powered from a single Lineage 2000 (or equivalent) battery plant. The duplex configuration allows the DACS to be powered from one or two Lineage 2000® (or equivalent) battery plants.

## Standard Power Configuration

In the standard configuration, the DACS IV-2000 operates with a lineage 2000 (or equivalent) battery plant (-48 Vdc nominal) in a central office environment.

Seven power feeders and seven returns are terminated at the Switch Bay and provide power for the entire DACS IV-2000. The feeders are designated by the loads they serve: A, B, C, D, E, F, and G. Each load is fused separately.

- Feeders A, B, C, D, and E (connected through the Fuse and Alarm Panel) supply power to the facility interface bays, the SW PWR Module, and the fan assemblies.
- Feeders F and G (connected directly to the RC PWR Module) supply power to the RC PWR Module.

## Duplex Power Configuration

The duplex power feature provides compatibility with the "red and blue" central office power distribution being deployed in the AT&T Network, and with other power distribution arrangements. The duplex power feature uses one or two -48V diverse power plants. (A diverse power plant is one that does not share common components, such as rectifiers, batteries, BDFBs, and cable racks.)

Four power feeders (A, B, C, and D) and four returns are terminated at the Switch Bay and provide power for the entire DACS IV-2000. Power feeders A and B supply power buses A, B, and E and power feeders C and D supply power buses C, D, and F. All power feeders are connected to the Fuse and Alarm Panel.

When the DACS IV-2000 is powered using two battery plants, the following requirements apply:

- Power feeders to the DACS IV-2000 must be placed in two groups to allow connection to two separate BDFDs.
- Two BDFBs are required.
- Feeders A and B are fed from BDFB-A; feeders C and D are fed from BDFB-B.

Loss of one battery plant or loss of one group of feeders does not cause any loss of service (except where there is only one battery plant supplying power).

The power supply requirements are summarized in Table A-22.

Table A-22. **Power Supply Requirements**

| Item | Value |
|---|---|
| Primary Supply Voltage | -48 Vdc nominal (-42.5 to -60.0 Vdc) |
| Secondary Supply Voltage | -48 Vdc nominal (-42.5 to -60.0 Vdc) |
| Transient Voltage Limit | -60.0 Vdc |
| Battery Noise (voice frequency) | < 56 dBrnc0 |
| Battery Noise (radiation frequency) | 100 mV rms in any 3-kHz band over 10 kHz to 20 MHz |
| Power Bus Interconnection | Connectorized |
| Number of Power Feeders | 7 (standard), 4 (duplex) |
| Fuse Rating at BDFB (feeders A,B,C,D, E, F, and G) | Depends on bay configuration (see floor plan data sheets) |
| Maximum Current Drain over A, B, C, D, E, F, and G Feeders (under failure condition) | Depends on bay configuration (see floor plan data sheets) |
| Maximum Current Drain over E Feeder | < 2.0A |

## Power Dissipation

Enough redundancy is provided in the DACS IV-2000 so a single failure of a bus or power circuit pack does not affect service. Each power circuit pack is fed through either a 7.5A, 10A, or 12A fuse located in the fuse and alarm panel. A power feed status visual indicator and a power circuit pack failure visual indicator are located on each power circuit pack.

The power dissipation of the DACS IV-2000 bays conforms to Bellcore TR-NWT-000063.

Power specification requirements are summarized in Table A-23.

Table A-23. **Bay Power Dissipation**

| Item | Value |
|---|---|
| Power Circuit Pack Fuse Rating<br>PWRA<br>PWRE<br>PWRF<br>PWRG | <br>12A<br>10A<br>7.5A<br>7.5A |
| Switch Bay Power Dissipation (fully equipped) | 1253W |
| DS1 Interface Bay Power Dissipation (fully equipped) | 620W |
| DS3 Interface Bay Power Dissipation (fully equipped) | 597W |
| STS1/DS3/DS1 Interface Bay Power Dissipation (fully equipped) | 770W |
| STS1/DS3 Interface Bay Power Dissipation (fully equipped) | 1105W |

# Physical Specifications

The floor load from the DACS IV-2000 frames (excluding cable distribution system) averaged across the associated floor area does not exceed 115 lb/ft$^2$. Other physical characteristics of the DACS IV-2000 are provided in Table A-24.

Table A-24. **Physical Characteristics**

| Item | Value |
|---|---|
| DACS IV-2000 | Up to nine standard 26 in (W) x 84 in (H) x 12 in (D) bays* |
| Framework Type | Network Bay |
| Weight (Switch Bay) | 512 lbs |
| Weight (DS3 Interface Bay) | 230 lbs |
| Weight (DS1 Interface Bay) | 440 lbs |
| Weight (STS1/DS3/DS1 Interface Bay) | 450 lbs |
| Weight (STS1/DS3 Interface Bay) | 450 lbs |
| Floor Load (excluding cable distribution) | Conform to TR-NWT-000063 |
| Maintenance Aisle, Front (minimum width) | 30 in |
| Wiring Aisle, Rear (minimum width) | 24 in |

* All interface bays are 12 inches deep; the Switch Bay is 13 inches deep.

# Environmental Specifications

The environmental considerations for the DACS IV-2000 include the thermal characteristics, handling and transportation requirements, earthquake, acoustical noise, EMC, and ESD specifications. These environmental specifications conform to Bellcore TR-NWT-000063, and TR-NWT-001089.

Each of these areas is discussed below and the particular specifications and requirements associated with each area are given.

## Ambient Characteristics

The DACS IV-2000 remains operational within the following room ambient temperature and humidity limits.

Room ambient refers to conditions at a location 5 feet above the floor and 15 inches in front of the equipment. The short term refers to a period of not more than 72 consecutive hours and a total of not more than 15 days in one year. Relative humidities must be less than 80 percent for ambient temperatures above 95°F. At the short-term emergency condition of 120°F, the relative humidity must be below 20 percent.

The DACS IV-2000 remains operational when installed in COs (central offices) located from 200 feet below sea level to 13,000 feet above sea level.

The DACS IV-2000 environmental characteristics are summarized in Table A-25.

Table A-25. **Environmental Characteristics**

| Item | Value or Specification |
|---|---|
| Normal Operating Temperature Range | +40° to +100°F (4.4° to 37.8°C) |
| Minimum Short-Term Temperature | 35°F (1.6°C) |
| Maximum Short-Term Temperature | 120°F (48.8°C) |
| Maximum Rate of Temperature Change | 15°F (8.4°C) per hour |
| Operating Relative Humidity | 20 to 55% |
| Minimum Short-Term Relative Humidity | 20% |
| Maximum Short-Term Relative Humidity | 80% < 0.024 lb of water/lb of dry air |
| Operational Altitude | From 200 ft below to 13,000 ft above sea level |
| Equipment Cooling | Natural convection:<br>DS1, DS3, and STS1/DS3/DS1 Interface Bays<br>Forced convection (fans):<br>Switch and STS1/DS3 Interface Bays |
| Fire Resistance and Dust | Conform to TR-NWT-000063 |
| Standard Heat Dissipation | Conform to TR-NWT-000063 |

## Handling and Transportation

The DACS IV-2000 meets the shock, vibration, temperature, and relative humidity criteria specified in TR-NWT-000063, *Network Equipment-Building System (NEBS) Generic Equipment Requirements* (Issue 5, September 1993) for handling and transportation. (See Table A-26.)

Table A-26. **Handling and Transportation Specifications**

| Item | Value or Specification |
|---|---|
| Vibration and Shock Design Criteria | Conform to TR-NWT-000063 |
| Temperature (Transportation/Storage) | Conform to TR-NWT-000063 |
| Relative Humidity (Transportation/ Storage) | Conform to TR-NWT-000063 |
| Storage/Shipment Altitude | Up to 40,000 ft |

## Earthquake, Acoustical Noise, EMC, and ESD

The design techniques for the DACS IV-2000 minimize emissions for an open frame design. The objective is to conform to the emission and immunity electromagnetic compatibility (EMC) limits as outlined in Part 15, Subpart J, of the FCC rules for Class A Computing Devices; see TR-NWT-000063 and TR-NWT-001089.

The DACS IV-2000 is designed to meet the electrostatic discharge (ESD) requirements specified in TR-NWT-001089.

ESD grounding connections are provided on the front and rear of each bay, and the use of wrist straps is required. EMC enclosures are required for the DACS IV-2000 to be fully compliant with EMC limits and ESD requirements.

The earthquake, acoustical noise, EMC, and ESD specifications are shown in Table A-27

Table A-27. Earthquake, Acoustical Noise, EMC, and ESD Specifications

| Item | Value or Specification |
|---|---|
| Earthquake and Office Vibration | Conform to TR-NWT-000063 |
| Acoustical Noise Limits under Normal Operating Temperatures | < 65 dBA<br>Conform to TR-NWT-000063 |
| Electromagnetic Compatibility (EMC) with EMC Enclosures | Conform to TR-NWT-001089 Part 15, Subpart J, *Class A Computing Devices* |
| Electrostatic Discharge (ESD) with EMC Enclosures | Conform to TR-NWT-001089 |

## Availability and Reliability Specifications

Availability and reliability can be defined in terms of the following three components, which are described in this section and summarized in Table A-28.

- Mean time between failures
- Mean time between maintenance activities for the equipment
- Quality and reliability of the software.

### Mean Time Between Failures

Mean Time Between Failures (MTBF) indicates the frequency of service-affecting failures within the DACS IV-2000. MTBF is greater than 9000 years per DS3, greater than 17,000 years per DS1, and greater than 9000 years (est.) per EC-1 facility. The outage time is less than 0.012 minute per year per DS3, less than 0.006 minute per year per DS1, and less than 0.012 minute per year (est.) per EC-1 facility as specified in Bellcore TA-NWT-000233 and TA-NWT-001339).

### Mean Time Between Maintenance Activities

Reliability is specified in terms of Mean Time Between Maintenance Activities (MTBMA), which indicates the frequency of failures within the DACS IV-2000. This is a measurement of how often a maintenance activity occurs and includes

both service-affecting and non-service-affecting failures. The MTBMA is greater than 3000 hours for a fully equipped DACS IV-2000 standard bay. The MTBMA specified in Table A-28 is for fully equipped standard bays and depends on bay type.

The MTBMA, MTBF, and outage times are based on 2 hours Mean Time To Repair (MTTR) as specified in Bellcore TA-NWT-000233 and TA-NWT-001339.

The availability and reliability specifications for the DACS IV-2000 are summarized in Table A-28.

Table A-28. **Availability and Reliability Specifications**

| Item | Value or Specification |
|---|---|
| MTBF (per DS3) | > 9000 years (est.) |
| MTBF (per DS1) | > 17,000 years (est.) |
| MTBF (per EC-1) | > 9000 years (est.) |
| Outage Time (per DS3) | 0.012 min/year; better than TA-NWT-000233 and TA-NWT-001339 |
| Outage Time (per DS1) | 0.006 min/year; better than TA-NWT-000233 and TA-NWT-001339 |
| Outage Time (per EC-1) | < 0.012 min/year; better than TA-NWT-000233 and TA-NWT-001339 |
| MTBMA Switch Bay (fully equipped) | 4299 hours |
| MTBMA DS3 Interface Bay (fully equipped) | 4144 hours |
| MTBMA STS1/DS3/DS1 Interface Bay (fully equipped) | 3835 hours |
| MTBMA DS1 Interface Bay (fully equipped) | 5323 hours |
| MTBMA STS1/DS3 Interface Bay (fully equipped) | 4144 hours |
| MTTR | 2 hours |
| Reliability Prediction Procedure | Conform to TR-TSY-000332, Issue 4 |

## Software Quality and Reliability

The software quality criteria conform to Bellcore TR-TSY-000179.

The software reliability criteria conform to Bellcore TA-TSY-000282.

The reliability prediction procedures conform to Bellcore TR-NWT-000332.

# Alarm, Scan, and Control Points

# B

## Contents

# Contents

# Alarm, Scan, and Control Points

# B

This appendix is provided to describe the interface between the DACS IV-2000 and telemetry operations systems (OSs). The AS&C points are used with administrative link (CILINKs 1-4 and 2-4). CILINKs 1-4 and 2-4 support the TABS (telemetry asynchronous block serial) and TBOS (telemetry byte oriented serial) protocols as defined in AT&T Compatibility Bulletin No. 149 entitled *Maintenance Standards for Digital Transmission Standards, Issue 3.* Both protocols use a polling format between the telemetry system and the DACS IV-2000 with the telemetry system initiating all communications by sending a request message to the DACS IV-2000 during each poll cycle. The system responds by sending the surveillance (or scan) point to the telemetry remote. The TABS protocol supports both point-to-point and multipoint architectures while TBOS only supports the point-to-point architecture. CILINKs 1-4 and 2-4 are used as a dedicated links. When using a General Telemetry Processor (GTP), the GTP must be connected to link 4 of the master ECI circuit pack at all times. If both ECI circuit packs are available, ECI-1 is the master ECI on system reset.

## Types of AS&C Points

Point is a term which is used to describe a single element of binary information. Physically, an AS&C point can be a single bit position in a serial telemetry message or it can be a discrete relay contact closure. Functionally, three distinct classes of AS&C points exist as follows:

- Alarm Points — provide the telemetry remote with information concerning alarm conditions existing within the DACS IV-2000. This information is available as both dedicated binary bit positions in the telemetry messages (sent by the DACS IV-2000 to the telemetry remote) and also as a set of discrete relay closures.

- Scan Points — provide the telemetry remote with status information concerning the DACS IV-2000. This information is available as dedicated binary bit positions in the telemetry messages (sent by the DACS IV-2000 to the telemetry remote).
- Control Points — provide the telemetry remote with operational control of certain aspects of the DACS IV-2000. This information is available as dedicated binary bit positions in the telemetry messages (received by the DACS IV-2000 from the telemetry remote).

## Alarm Points via Relay Closures

Alarm points are provided, through relay closures, to telemetry remote equipment accepting discrete inputs (for example, the General Telemetry Processor [GTP]). The relay closures provide the same alarm information to the OS as is available locally through the office alarms. The DACS IV-2000 software supports relay closures for critical, major, and minor alarms. The conditions for activating each type of alarm point are:

- Critical Alarm (CR) — is set on the occurrence of a severe, service-affecting condition which requires immediate corrective action regardless of time-of-day or day-of-the-week.
- Major Alarm (MJ) — is set whenever there are one or more service-affecting failures or whenever failures which can mask service-affecting failures (for example, main controller failures).
- Minor Alarm (MN) — is set whenever there are one or more non-service-affecting failures exist, or when certain manually initiated functions (for example, manual protection switches are in effect).

## Scan and Control Displays

The serial telemetry data is broken down into logical groups of 64 points each, called *displays*. This grouping, in general, conforms to the manner in which the data is shown on a terminal, with one display presenting a single terminal screen full of data. There are two types of displays:

- Scan — transmitted by the DACS IV-2000, consists of combinations of alarm and scan points. Scan point indications for momentary conditions (for example, an intermittent failure) are stretched to a minimum duration of 20 seconds to ensure that the conditions are sensed by the telemetry system. The 64th scan point in a display is reserved to indicate to the telemetry remote that serial link errors have occurred.
- Control — received by the DACS IV-2000, consists of control points from a remote site. Through the use of control points, certain aspects of system operation can be controlled by a remote site.

The DACS IV-2000 has the flexibility to support three levels of display sets:

- Summary — providing system level alarms and status identifying:
  - — Type of equipment or facility failure
  - — Presence of a protection switch or of a inhibition of protection switching (that is, lock-out) in a specific type of module

  This set does not indicate the specific facilities, equipment, or modules affected. The primary application for the summary set is as a backup source of alarm data when a message Operations System [OS] (for example, SCCS) is used as the primary source of alarm data.
- Detailed — providing expanded information which identifies the particular module(s) experiencing a problem and usually containing information to isolate a failure to the circuit pack level. This set also allows remote control of manual protection switching and the inhibition or the locking of protection switching. Selecting the detailed set automatically includes the transmission of the summary set.
- Extended Facility — providing additional circuit pack and interface port information, particularly on the DS1 facility level, on the VT1.5 facility level, on out-of-frame (OOF) conditions on DS2s within DS3 facilities, on DS3 input format mismatches, and on EC-1 facility conditions. For STS1 (modules 1-32), DS3 (modules 9-32), and DS1 (modules 33-64) Interface Modules there are control points included in the extended facility set. In addition, for DS3 (modules 9-32) and DS1 (modules 33-64) Interface Modules and Switch Input/Output (modules 3 and 4) Modules, the extended facility set includes detailed set information (scan and control points). Selecting the extended facility set automatically includes the transmission of the summary and detailed sets. Due to the large number of displays in the detailed alarm sets, only the summary set is supported by the TBOS protocol. The choice of alarm sets is made by you when the telemetry link (CILINK-1-4 and CILINK-2-4) is provisioned. The display sets are described in the following sections.

## Summary Display Set

The summary display set provides the OS with data on the severity of the failure and the type of module that indicates the failure. Failures are identified as either non-service affecting (NSA) or service affecting (SA) as specified in Bell Communications Research TA-NWT-000474, Issue 1, or without an indication of the specific facilities affected or the circuit packs responsible for the failure. The main controller failure (MC:FAIL or OOS) point indicates failure(s) in the control complexes (CCs) circuit packs are preventing the execution of system control functions. The point CC:FAIL or OOS indicates a failure with CC-0 and/or CC-1. Failure of one of the ECI circuit packs is indicated by ECI:FAIL or OOS. Failures of the primary (PRI) and secondary (SEC) backup memories or the secondary storage controller (SSC) are indicated with separate alarm points and are therefore not included in the MC FAIL alarm point. The `SYNC Reference:FAIL NSA` point indicates the presence of a NSA failure of one or both synchronizer timing references.

Scan points indicate if any protection groups are switched to protection or have protection locked (either manually or as a result of an autolock). The type of module is specified, but not the specific protection group affected. If the equipment is in an abnormal state as a result of a manual control (for example, locking or forcing of protection switching), this is indicated by setting a scan point for *manual function initiated.* Failure of any frame audit that results in an autonomous message over the Snider and X.25 links also sets the Frame Audit Failure scan point for one polling cycle.

No control points are associated with the summary set. Table B-1 lists the summary set scan points.

Table B-1. **Summary Display Set Scan Points**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 0 | 1 | A | MC Fail or OOS |
| | 2 | A | PRI Fail or OOS |
| | 3 | A | SEC Fail |
| | 4 | A | Switch Power Fail SA |
| | 5 | A | Switch Power Fail NSA |
| | 6 | A | Clock Hardware Fail SA |
| | 7 | A | Clock Hardware Fail NSA |
| | 8 | A | SWCS Fail SA |
| | 9 | A | SWCS Fail NSA |
| | 10 | A | SWIO Fail SA |
| | 11 | A | SWIO Fail NSA |
| | 12 | A | DS1 Interface Module UC Fail or OOS |
| | 13 | A | DS1 Interface Module Power Fail |
| | 14 | A | CC Fail or OOS |
| | 15 | A | DS1 Interface Module CLKDR Fail SA |
| | 16 | A | DS1 Interface Module CLKDR Fail NSA |
| | 17 | A | DS1IF/SWIF/DS1RY Fail SA |
| | 18 | A | DS1IF/SWIF/PMGR1 Fail NSA |
| | 19 | A | Incoming DS3/STS-1 Fail |
| | 20 | A | Multiple Incoming DS3/STS-1 Fail |
| | 21 | A | DS3/STS1 Interface Module UC Fail or OOS |
| | 22 | A | DS3/STS1 Interface Module Power Fail |
| | 23 | A | ECI Fail or OOS |
| | 24 | A | DS3/STS1 Interface Module CLKDR Fail SA |
| | 25 | A | DS3/STS1 Interface Module CLKDR Fail NSA |
| | 26 | A | MUX/SMUX Fail SA |

* A = Alarm
S = Scan

† There is one display per system.

Table continued on next page.

Table B-1. **Summary Display Set Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| | 27 | A | MUX/PMGR1/SMUX Fail NSA |
| | 28 | A | Fan Fail |
| | 29 | A | Switch Module Manual Function Initiated |
| | 30 | A | DS1 Interface Module Manual Function Initiated |
| | 31 | A | DS3/STS1 Interface Module Manual Function Initiated |
| | 32 | A | Time of Day Clock Fail |
| | 33 | S | SWCS Protection Switch Active |
| | 34 | S | SWCS Protection Switch Locked |
| | 35 | S | SWCS Protection Switch Auto-Locked |
| | 36 | S | SWIO Protection Switch Active |
| | 37 | S | SWIO Protection Switch Locked |
| 0 | 38 | S | SWIO Protection Switch Auto-Locked |
| | 39 | A | SYNC Reference Fail NSA |
| | 40 | S | DS1IF Protection Switch Active |
| | 41 | S | DS1IF Protection Switch Locked |
| | 42 | S | DS1IF Protection Switch Auto-Locked |
| | 43 | S | Incoming DS1 Fail |
| | 44 | S | Multiple Incoming DS1s Fail |
| | 45 | - | Unassigned |
| | 46 | S | MUX/SMUX Protection Switch Active |
| | 47 | S | MUX/SMUX Protection Switch Locked |
| | 48 | S | MUX/SMUX Protection Switch Auto-Locked |
| | 49 | - | Unassigned |
| | 50 | S | CILINK 1-4 OOS or Lock-Out |
| | 51 | S | Transfer to SEC Fail |

* A = Alarm
S = Scan

† There is one display per system.

Table continued on next page.

Table B-1. Summary Display Set Scan Points (Continued)

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 0 | 52 | A | Frame Audit Fail |
| | 53 | S | CILINK 1-1 OOS or Lock-Out |
| | 54 | S | CILINK 1-2 OOS or Lock-Out |
| | 55 | S | CILINK 1-3 OOS or Lock-Out |
| | 56 | S | CILINK 1-5 OOS or Lock-Out |
| | 57 | S | CILINK 1-6 OOS or Lock-Out |
| | 58 | S | CILINK 2-1 OOS or Lock-Out |
| | 59 | S | CILINK 2-2 OOS or Lock-Out |
| | 60 | S | CILINK 2-3 OOS or Lock-Out |
| | 61 | S | CILINK 2-4 OOS or Lock-Out |
| | 62 | S | CILINK 2-5 OOS or Lock-Out |
| | 63 | S | CILINK 2-6 OOS or Lock-Out |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There is one display per system.

## Detailed Display Set

Most applications that use the telemetry AS&C points as the primary source of maintenance data need more detail than is provided by the summary set. The following paragraphs describe the functions provided by the detailed AS&C points and include tables with the specific scan and control points needed for each product.

Most equipment failures are identified by the specific affected circuit pack. The failures are specified as either NSA or SA as specified in Bell Communications Research TA-NWT-000474, Issue 1. An NSA alarm indicates the failure of a circuit pack that does not affect service, such as a controller, or a failure that resulted in a successful protection switch to restore service. In the latter case, a scan point is provided to indicate the state of the protection switch. SA alarms indicate failures that result in service being lost.

The DACS IV-2000 can distinguish between equipment failures and incoming facility failures. Incoming DS3 failures are assigned individual alarm points, while incoming DS1 failures are indicated by a multiple scan point that specifies the affected module but not the individual DS1.

Terminating DS3 facilities have four alarm points[1] per DS3. The first alarm point indicates a loss-of-signal (LOS) or high bit error rate (BER) condition. The BER can be determined through either bipolar violations (BPVs), which is the default, or by monitoring DS3 parity errors. The alarm point is set when the BER exceeds the threshold of $10^{-3}$ (default) through $10^{-9}$ as provisioned. The second alarm point indicates an out-of-frame (OOF) condition. Under LOS or when the BER is high enough to cause an OOF, both alarm points are set. The other two alarm points indicate detection of incoming DS3 alarm indication signal (AIS) and detection of incoming DS3 idle signal.

The DS1 facilities associated with the DS1 Interface Module have two scan points indicating that one or more of the incoming DS1 signals to the module have either an LOS condition or a BER that exceeds the threshold of $10^{-3}$ (default) through $10^{-9}$ as determined by monitoring BPVs.

Control points allow manual protection switching of individual circuit packs and permit inhibiting (lockout) protection switching. Three controls are provided:

- Make protection switch — transfers service to the protection circuit pack if it is available and good and locks it in that state. This control has no effect if service on the indicated circuit pack is already on protection, if protection is unavailable, or if protection is inhibited (locked).
- Lock protection — inhibits service from being transferred to the protection circuit pack. In this state, no automatic switch to protection occurs if the service circuit pack is diagnosed as bad.
- Unlock protection — allows manual or automatic protection switching on the indicated circuit pack. If a manual protection switch has been made on a *good* circuit pack, the unlock control allows the DACS IV-2000 to release the switch. No control point is provided to force a circuit pack into the unprotected state if it is in the protected state and diagnosed as bad.

For each control, a corresponding scan point is provided to allow verification that the action specified by the control was completed.

Tables B-2 through B-11 define the scan and control points required for each module or assembly of the DACS IV-2000. Scan points are divided by type into alarm and scan points, and alarm points are further designated as either NSA or SA.

## RC, SYNC, and SW Modules

Tables B-2 and B-3 list the detailed Redundant Controller, Synchronizer, and Switch Module scan and control points, respectively.

1. An additional alarm point is provided in the extended display set for DS3 format mismatches. Refer to the section titled "Extended Facility Display Sets" (page B-24) for more information on the extended display sets.

Table B-2. **Detailed Display Set (RC/SYNC/SW Modules) — Scan Points**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1 | A | MC Fail |
| | 2 | A | PRI-1 Fail |
| | 3 | A | SEC Fail NSA |
| | 4 | A | Switch Power Fail SA |
| | 5 | A | Switch Power Fail NSA |
| | 6 | A | MC Power Fail NSA |
| | 7 | A | CLKGN Fail SA |
| | 8-9 | A | CLKGN-{0,1} Fail NSA |
| | 10 | A | Frame Audit Fail |
| | 11 | A | Fan Fail |
| | 12-43 | A | SWIO-{1-32} Fail NSA |
| | 44 | A | Switch Module Manual Function Initiated |
| | 45 | A | Time of Day Clock 1 Fail |
| | 46 | A | CC-1 Fail or OOS |
| | 47 | A | Time of Day Clock 2 Fail |
| | 48 | A | CC-0 Fail or OOS |
| | 49 | S | SYNCPRI Active Timing Reference |
| | 50-51 | S | CLKGN-{0,1} Active |
| | 52 | S | SYNCSEC Active Timing Reference |
| | 53 | S | Transfer to SEC Fail |
| | 54 | S | CILINK 1-1 OOS-MTCE |
| | 55 | S | CILINK 1-2 OOS-MTCE |
| | 56 | S | CILINK 1-3 OOS-MTCE |
| | 57 | S | CILINK 1-5 OOS-MTCE |
| | 58 | S | CILINK 1-6 OOS-MTCE |
| | 59 | S | CILINK 1-4 OOS-MTCE |

* A = Alarm
S = Scan

† There are six displays for the RC/SYNC/SW Modules.

Table continued on next page.

Table B-2. **Detailed Display Set (RC/SYNC/SW Modules) — Scan Points (Continued)**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 60-61 | A | ECI-{1,2} Fail or OOS |
| | 62-63 | S | SYNC-{0,1} Active |
| | 64 | - | Reserved |
| 2 | 1-32 | A | SWIO-{1-32} Fail SA |
| | 33 | A | SWCS-32Fail SA |
| | 34-39 | S | CILINK 1-{1-6} OOS-FLT, Protocol, or Lock-Out |
| | 40-45 | S | CILINK 2-{1-6} OOS-MTCE |
| | 46-51 | S | CILINK 2-{1-6} OOS-FLT, Protocol, or Lock-Out |
| | 52 | A | TBS3 Fail SA |
| | 53-54 | A | TBS3-{0,1} Fail NSA |
| | 55 | A | DPLL Fail SA |
| | 56-57 | A | DPLL-{0,1} Fail NSA |
| | 58-59 | - | Unassigned |
| | 60-62 | S | Reserved |
| | 63 | A | PRI-2 Fail or OOS |
| | 64 | - | Reserved |
| 3 | 1-32 | S | SWIO-{1-32} Protection Switch Active |
| | 33-36 | - | Unassigned |
| | 37 | A | DS1TX-0 Fail NSA |
| | 38 | A | DS1TX-1 Fail NSA |
| | 39-40 | - | Unassigned |
| | 41 | A | SYNCPRI-0 (DS1TX-0 Primary Reference Fail NSA |
| | 42 | A | SYNCSEC-0 (DS1TX-0 Secondary Reference Fail NSA |

* A = Alarm
S = Scan

† There are six displays for the RC/SYNC/SW Modules.

Table continued on next page.

Table B-2. Detailed Display Set (RC/SYNC/SW Modules) — Scan Points (Continued)

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 3 | 43 | A | SYNCPRI-1 (DS1TX-1 Primary Reference Fail NSA |
| | 44 | A | SYNCSEC-1 (DS1TX-1 Secondary Reference Fail NSA |
| | 45-46 | - | Unassigned |
| | 47 | A | SYNC Mode Fail NSA |
| | 48-63 | - | Unassigned |
| | 64 | - | Reserved |
| 4 | 1-16 | S | SWIO Pair {1-16} Protection Switch Auto-Locked |
| | 17-48 | S | SWIO-{1-32} Protection Switch Locked |
| | 49 | A | MC OOS-MCOND |
| | 50-51 | A | CC-{0,1} OOS-MTCE |
| | 52 | A | PRI-1 OOS-MTCE |
| | 53 | - | Unassigned |
| | 54 | A | PRI-2 OOS-MTCE |
| | 55-56 | - | Unassigned |
| | 57 | A | Transfer to SEC Fail Minor NSA |
| | 58-63 | - | Unassigned |
| | 64 | - | Reserved |
| 5 | 1-31 | A | SWCS-{1-31} Fail SA |
| | 32-63 | A | SWCS-{1-32} Fail NSA |
| | 64 | - | Reserved |
| 6 | 1 | S | SWCS Protection Auto-Locked |
| | 2-32 | S | SWCS-{1-31} Protection Switch Active |
| | 33-63 | S | SWCS-{1-31} Protection Switch Locked |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are six displays for the RC/SYNC/SW Modules.

Table B-3. **Detailed Display Set (RC/SYNC/SW Modules) — Control Points**

| Display † | Point No. | Description |
|---|---|---|
| 1 | 1-2 | CLKGN-{0,1} Make CLKGN Active |
| | 3-4 | SYNC-{0,1} Make SYNC Active |
| | 5 | SYNCPRI Make Timing Reference |
| | 6 | SYNCSEC Make Timing Reference |
| | 7-64 | Unassigned |
| 2 | 1-32 | SWIO-{1-32} Make Protection Switch |
| | 33-64 | Unassigned |
| 3 | 1 | SWIO-1 Lock Protection |
| | 2 | SWIO-1 Unlock Protection |
| | 3 | SWIO-2 Lock Protection |
| | 4 | SWIO-2 Unlock Protection |
| | 5 | SWIO-3 Lock Protection |
| | 6 | SWIO-3 Unlock Protection |
| | 7 | SWIO-4 Lock Protection |
| | 8 | SWIO-4 Unlock Protection |
| | 9 | SWIO-5 Lock Protection |
| | 10 | SWIO-5 Unlock Protection |
| | 11 | SWIO-6 Lock Protection |
| | 12 | SWIO-6 Unlock Protection |
| | 13 | SWIO-7 Lock Protection |
| | 14 | SWIO-7 Unlock Protection |
| | 15 | SWIO-8 Lock Protection |
| | 16 | SWIO-8 Unlock Protection |
| | 17 | SWIO-9 Lock Protection |
| | 18 | SWIO-9 Unlock Protection |
| | 19 | SWIO-10 Lock Protection |
| | 20 | SWIO-10 Unlock Protection |

† There are five displays for the RC/SYNC/SW Modules.

Table continued on next page.

Table B-3. Detailed Display Set (RC/SYNC/SW Modules) — Control Points (Continued)

| Display † | Point No. | Description |
|---|---|---|
| | 21 | SWIO-11 Lock Protection |
| | 22 | SWIO-11 Unlock Protection |
| | 23 | SWIO-12 Lock Protection |
| | 24 | SWIO-12 Unlock Protection |
| | 25 | SWIO-13 Lock Protection |
| | 26 | SWIO-13 Unlock Protection |
| | 27 | SWIO-14 Lock Protection |
| | 28 | SWIO-14 Unlock Protection |
| | 29 | SWIO-15 Lock Protection |
| | 30 | SWIO-15 Unlock Protection |
| | 31 | SWIO-16 Lock Protection |
| | 32 | SWIO-16 Unlock Protection |
| | 33 | SWIO-17 Lock Protection |
| 3 | 34 | SWIO-17 Unlock Protection |
| | 35 | SWIO-18 Lock Protection |
| | 36 | SWIO-18 Unlock Protection |
| | 37 | SWIO-19 Lock Protection |
| | 38 | SWIO-19 Unlock Protection |
| | 39 | SWIO-20 Lock Protection |
| | 40 | SWIO-20 Unlock Protection |
| | 41 | SWIO-21 Lock Protection |
| | 42 | SWIO-21 Unlock Protection |
| | 43 | SWIO-22 Lock Protection |
| | 44 | SWIO-22 Unlock Protection |
| | 45 | SWIO-23 Lock Protection |
| | 46 | SWIO-23 Unlock Protection |
| | 47 | SWIO-24 Lock Protection |

† There are five displays for the RC/SYNC/SW Modules.

Table continued on next page.

Table B-3. Detailed Display Set (RC/SYNC/SW Modules) — Control Points (Continued)

| Display † | Point No. | Description |
|---|---|---|
| 3 | 48 | SWIO-24 Unlock Protection |
| | 49 | SWIO-25 Lock Protection |
| | 50 | SWIO-25 Unlock Protection |
| | 51 | SWIO-26 Lock Protection |
| | 52 | SWIO-26 Unlock Protection |
| | 53 | SWIO-27 Lock Protection |
| | 54 | SWIO-27 Unlock Protection |
| | 55 | SWIO-28 Lock Protection |
| | 56 | SWIO-28 Unlock Protection |
| | 57 | SWIO-29 Lock Protection |
| | 58 | SWIO-29 Unlock Protection |
| | 59 | SWIO-30 Lock Protection |
| | 60 | SWIO-30 Unlock Protection |
| | 61 | SWIO-31 Lock Protection |
| | 62 | SWIO-31 Unlock Protection |
| | 63 | SWIO-32 Lock Protection |
| | 64 | SWIO-32 Unlock Protection |
| 4 | 1-31 | SWCS-{1-32} Switch to Protection |
| | 32-64 | Unassigned |
| 5 | 1 | SWCS-1 Lock Protection |
| | 2 | SWCS-1 Unlock Protection |
| | 3 | SWCS-2 Lock Protection |
| | 4 | SWCS-2 Unlock Protection |
| | 5 | SWCS-3 Lock Protection |
| | 6 | SWCS-3 Unlock Protection |
| | 7 | SWCS-4 Lock Protection |
| | 8 | SWCS-4 Unlock Protection |

† There are five displays for the RC/SYNC/SW Modules.

Table continued on next page.

Table B-3. Detailed Display Set (RC/SYNC/SW Modules) — Control Points (Continued)

| Display † | Point No. | Description |
|---|---|---|
| | 9 | SWCS-5 Lock Protection |
| | 10 | SWCS-5 Unlock Protection |
| | 11 | SWCS-6 Lock Protection |
| | 12 | SWCS-6 Unlock Protection |
| | 13 | SWCS-7 Lock Protection |
| | 14 | SWCS-7 Unlock Protection |
| | 15 | SWCS-8 Lock Protection |
| | 16 | SWCS-8 Unlock Protection |
| | 17 | SWCS-9 Lock Protection |
| | 18 | SWCS-9 Unlock Protection |
| | 19 | SWCS-10 Lock Protection |
| | 20 | SWCS-10 Unlock Protection |
| | 21 | SWCS-11 Lock Protection |
| 5 | 22 | SWCS-11 Unlock Protection |
| | 23 | SWCS-12 Lock Protection |
| | 24 | SWCS-12 Unlock Protection |
| | 25 | SWCS-13 Lock Protection |
| | 26 | SWCS-13 Unlock Protection |
| | 27 | SWCS-14 Lock Protection |
| | 28 | SWCS-14 Unlock Protection |
| | 29 | SWCS-15 Lock Protection |
| | 30 | SWCS-15 Unlock Protection |
| | 31 | SWCS-16 Lock Protection |
| | 32 | SWCS-16 Unlock Protection |
| | 33 | SWCS-17 Lock Protection |
| | 34 | SWCS-17 Unlock Protection |
| | 35 | SWCS-18 Lock Protection |

† There are five displays for the RC/SYNC/SW Modules.

Table continued on next page.

Table B-3. **Detailed Display Set (RC/SYNC/SW Modules) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| 5 | 36 | SWCS-18 Unlock Protection |
| | 37 | SWCS-19 Lock Protection |
| | 38 | SWCS-19 Unlock Protection |
| | 39 | SWCS-20 Lock Protection |
| | 40 | SWCS-20 Unlock Protection |
| | 41 | SWCS-21 Lock Protection |
| | 42 | SWCS-21 Unlock Protection |
| | 43 | SWCS-22 Lock Protection |
| | 44 | SWCS-22 Unlock Protection |
| | 45 | SWCS-23 Lock Protection |
| | 46 | SWCS-23 Unlock Protection |
| | 47 | SWCS-24 Lock Protection |
| | 48 | SWCS-24 Unlock Protection |
| | 49 | SWCS-25 Lock Protection |
| | 50 | SWCS-25 Unlock Protection |
| | 51 | SWCS-26 Lock Protection |
| | 52 | SWCS-26 Unlock Protection |
| | 53 | SWCS-27 Lock Protection |
| | 54 | SWCS-27 Unlock Protection |
| | 55 | SWCS-28 Lock Protection |
| | 56 | SWCS-28 Unlock Protection |
| | 57 | SWCS-29 Lock Protection |
| | 58 | SWCS-29 Unlock Protection |
| | 59 | SWCS-30 Lock Protection |

† There are five displays for the RC/SYNC/SW Modules.

Table continued on next page.

Table B-3. Detailed Display Set (RC/SYNC/SW Modules) — Control Points (Continued)

| Display † | Point No. | Description |
|---|---|---|
| 5 | 60 | SWCS-30 Unlock Protection |
| | 61 | SWCS-1 Lock Protection |
| | 62 | SWCS-31 Unlock Protection |
| | 63 | SWCS-32 Lock Protection |
| | 64 | SWCS-32 Unlock Protection |

† There are five displays for the RC/SYNC/SW Modules.

## DS1 Interface Modules

Tables B-4 and B-5 list the detailed scan and control points, respectively, for each DS1 Interface and DS1 Interface-Protection Module. The same points are used for both the DS1 Interface and DS1 Interface-Protection Modules. Detailed display sets for modules 33-64 are part of the extended displays sets.

Table B-4. Detailed Display Set (DS1 INTFC Module) — Scan Points

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1 | A | Power Circuit Pack(s) Fail |
| | 2 | - | Unassigned |
| | 3 | A | UC Fail or OOS |
| | 4 | A | CLKDR Fail SA |
| | 5-6 | A | CLKDR-{1,2} Fail NSA |
| | 7-22 | A | DS1IF-{1-16} Fail SA |
| | 23-38 | A | DS1IF-{1-16} Fail NSA |
| | 39-46 | A | SWIF-{1-8} Fail SA |
| | 47-54 | A | SWIF/PMGR-{1-8} Fail NSA |
| | 55-58 | A | DS1RY-{1-4} Fail SA |
| | 59 | A | SW Module Manual Function Initiated |

* A = Alarm
S = Scan

† There are two displays per DS1 Interface Module

Table continued on next page.

Table B-4. Detailed Display Set (DS1 INTFC Module) — Scan Points (Continued)

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 60-63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1 | S | DS1 Incoming Fail |
| | 2 | S | Multiple DS1s Incoming Fail |
| | 3 | - | Unassigned |
| | 4-19 | S | DS1IF-{1-16} Protection Switch Active |
| | 20-35 | S | DS1IF-{1-16} Protection Switch Locked |
| | 36 | S | DS1IF Protection Switch Auto-Locked |
| | 37-63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are two displays per DS1 Interface Module

Table B-5. Detailed Display Set (DS1 INTFC Module) — Control Points

| Display † | Point No. | Description |
|---|---|---|
| 1 | 1 | Unassigned |
| | 2 | DS1IF-{1A,1B} Switch to Protection |
| | 3 | Unassigned |
| | 4 | DS1IF-{2A,2B} Switch to Protection |
| | 5 | Unassigned |
| | 6 | DS1IF-{3A,3B} Switch to Protection |
| | 7 | Unassigned |
| | 8 | DS1IF-{4A,4B} Switch to Protection |
| | 9 | Unassigned |
| | 10 | DS1IF-{5A,5B} Switch to Protection |
| | 11 | Unassigned |
| | 12 | DS1IF-{6A,6B} Switch to Protection |

† There is one display per DS1 Interface Module

Table continued on next page.

Table B-5. Detailed Display Set (DS1 INTFC Module) — Control Points (Continued)

| Display † | Point No. | Description |
|---|---|---|
| | 13 | Unassigned |
| | 14 | DS1IF-{7A,7B} Switch to Protection |
| | 15 | Unassigned |
| | 16 | DS1IF-{8A,8B} Switch to Protection |
| | 17-19 | Unassigned |
| | 20 | DS1IF-{1A,1B} Lock Protection |
| | 21 | DS1IF-{1A,1B} Unlock Protection |
| | 22-23 | Unassigned |
| | 24 | DS1IF-{2A,2B} Lock Protection |
| | 25 | DS1IF-{2A,2B} Unlock Protection |
| | 26-27 | Unassigned |
| | 28 | DS1IF-{3A,3B} Lock Protection |
| 1 | 29 | DS1IF-{3A,3B} Unlock Protection |
| | 30-31 | Unassigned |
| | 32 | DS1IF-{4A,4B} Lock Protection |
| | 33 | DS1IF-{4A,4B} Unlock Protection |
| | 34-35 | Unassigned |
| | 36 | DS1IF-{5A,5B} Lock Protection |
| | 37 | DS1IF-{5A,5B} Unlock Protection |
| | 38-39 | Unassigned |
| | 40 | DS1IF-{6A,6B} Lock Protection |
| | 41 | DS1IF-{6A,6B} Unlock Protection |
| | 42-43 | Unassigned |
| | 44 | DS1IF-{7A,7B} Lock Protection |
| | 45 | DS1IF-{7A,7B} Unlock Protection |

† There is one display per DS1 Interface Module

Table continued on next page.

Table B-5. **Detailed Display Set (DS1 INTFC Module) — Control Points (Continued)**

| Display † | Point No. | Description |
|---|---|---|
| 1 | 46-47 | Unassigned |
| | 48 | DS1IF-{8A,8B} Lock Protection |
| | 49 | DS1IF-{8A,8B} Unlock Protection |
| | 50-64 | Unassigned |

† There is one display per DS1 Interface Module

## DS3 Interface Modules

The same points are assigned to the DS3 Interface-16 or DS3 Interface-32 Modules, except that the points referring to MUX number 17-32 or CLKDR number 3-4 are not needed for the DS3 Interface-16 Modules. MUX-16 (DS3 Interface-16 Modules) and MUX-32 (DS3 Interface-32 Modules) refers to the MUXP circuit packs. These points are always set to 0 in the DS3 Interface-16 Module displays. Tables B-6 and B-7 list the required scan and control points, respectively. In addition to equipment failures, alarm points are required to indicate incoming DS3 facility alarms. These points specify whether the DS3 is OOF or if there is a LOS or BER exceeding the selected threshold (either $10^{-3}$ or $10^{-6}$). Detailed display sets for modules 9-32 are part of the extended displays sets.

Table B-6. **Detailed Display Set (DS3 INTFC Module) — Scan Point**

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1 | A | Power Circuit Pack(s) Fail |
| | 2 | - | Unassigned |
| | 3 | A | UC Fail SA |
| | 4-7 | A | CLKDR-{1-4} Fail SA |
| | 8-11 | A | CLKDR-{1-4} Fail NSA |
| | 12 | A | MUXPS Fail SA |
| | 13 | A | DS3PM Fail NSA |
| | 14 | A | DS3 Interface Manual Function Initiated |

* A = Alarm
S = Scan

† There are five displays per DS3 Interface Module

Table continued on next page.

Table B-6. Detailed Display Set (DS3 INTFC Module) — Scan Point (Continued)

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 15-18 | - | Unassigned |
| | 19-49 | S | MUX-{1-31} Protection Switch Active |
| | 50-63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1 | S | MUX Protection Switch Auto-Locked |
| | 2-32 | S | MUX-{1-31} Protection Switch Locked |
| | 33-63 | A | DS3 Signal-{1-31} ID Error |
| | 64 | - | Reserved |
| 3 | 1-31 | A | MUX-{1-31} Fail SA |
| | 32-62 | A | MUX/PMGR-{1-32} Fail NSA |
| | 63 | A | MUX-32 (MUXP) Fail NSA |
| | 64 | - | Reserved |
| 4 | 1-31 | A | Incoming DS3 Signal-{1-31} LOS/BER |
| | 32-62 | A | Incoming DS3 Signal-{1-31} OOF |
| | 63 | A | MUX-32 (MUXP) Fail SA |
| | 64 | - | Reserved |
| 5 | 1-31 | A | Incoming DS3 Signal-{1-31} AIS Detected |
| | 32-62 | A | Incoming DS3 Signal-{1-31} Idle Detected |
| | 63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm
S = Scan

† There are five displays per DS3 Interface Module

Table B-7. **Detailed Display Set (DS3 INTFC Module) — Control Points**

| Display † | Point No. | Description |
|---|---|---|
| 1 | 1 | Unassigned |
| | 2-32 | MUX-{1-31} Switch to Protection |
| | 33-64 | Unassigned |
| 2 | 1 | MUX-1 Lock Protection |
| | 2 | MUX-1 Unlock Protection |
| | 3 | MUX-2 Lock Protection |
| | 4 | MUX-2 Unlock Protection |
| | 5 | MUX-3 Lock Protection |
| | 6 | MUX-3 Unlock Protection |
| | 7 | MUX-4 Lock Protection |
| | 8 | MUX-4 Unlock Protection |
| | 9 | MUX-5 Lock Protection |
| | 10 | MUX-5 Unlock Protection |
| | 11 | MUX-6 Lock Protection |
| | 12 | MUX-6 Unlock Protection |
| | 13 | MUX-7 Lock Protection |
| | 14 | MUX-7 Unlock Protection |
| | 15 | MUX-8 Lock Protection |
| | 16 | MUX-8 UnLock Protection |
| | 17 | MUX-9 Lock Protection |
| | 18 | MUX-9 Unlock Protection |
| | 19 | MUX-10 Lock Protection |
| | 20 | MUX-10 Unlock Protection |
| | 21 | MUX-11 Lock Protection |
| | 22 | MUX-11 Unlock Protection |
| | 23 | MUX-12 Lock Protection |
| | 24 | MUX-12 Unlock Protection |

† There are two displays per DS3 Interface Module

Table continued on next page.

Table B-7. Detailed Display Set (DS3 INTFC Module) — Control Points (Continued)

| Display † | Point No. | Description |
|---|---|---|
| | 25 | MUX-13 Lock Protection |
| | 26 | MUX-13 Unlock Protection |
| | 27 | MUX-14 Lock Protection |
| | 28 | MUX-14 Unlock Protection |
| | 29 | MUX-15 Lock Protection |
| | 30 | MUX-15 Unlock Protection |
| | 31 | MUX-16 Lock Protection |
| | 32 | MUX-16 Unlock Protection |
| | 33 | MUX-17 Lock Protection |
| | 34 | MUX-17 Unlock Protection |
| | 35 | MUX-18 Lock Protection |
| | 36 | MUX-18 Unlock Protection |
| | 37 | MUX-19 Lock Protection |
| 2 | 38 | MUX-19 Unlock Protection |
| | 39 | MUX-20 Lock Protection |
| | 40 | MUX-20 Unlock Protection |
| | 41 | MUX-21 Lock Protection |
| | 42 | MUX-21 Unlock Protection |
| | 43 | MUX-22 Lock Protection |
| | 44 | MUX-22 Unlock Protection |
| | 45 | MUX-23 Lock Protection |
| | 46 | MUX-23 Unlock Protection |
| | 47 | MUX-24 Lock Protection |
| | 48 | MUX-24 Unlock Protection |
| | 49 | MUX-25 Lock Protection |
| | 50 | MUX-25 Unlock Protection |
| | 51 | MUX-26 Lock Protection |

† There are two displays per DS3 Interface Module

Table continued on next page.

Table B-7. Detailed Display Set (DS3 INTFC Module) — Control Points (Continued)

| Display † | Point No. | Description |
|---|---|---|
| 2 | 52 | MUX-26 Unlock Protection |
| | 53 | MUX-27 Lock Protection |
| | 54 | MUX-27 Unlock Protection |
| | 55 | MUX-28 Lock Protection |
| | 56 | MUX-28 Unlock Protection |
| | 57 | MUX-29 Lock Protection |
| | 58 | MUX-29 Unlock Protection |
| | 59 | MUX-30 Lock Protection |
| | 60 | MUX-30 Unlock Protection |
| | 61 | MUX-31 Lock Protection |
| | 62 | MUX-31 Unlock Protection |
| | 63-64 | Unassigned |

† There are two displays per DS3 Interface Module

# Extended Display Sets

## Extended Facility Display Sets

The detailed scan points described previously are not always sufficient to identify the specific facility affected by a failure. In particular, incoming DS1 failures are specified by a single scan point for a DS1 Interface Module that can interface with up to 224 DS1 signals. The extended set provides the telemetry remote with increased information concerning incoming DS1 failures, and incoming DS3 OOF and format mismatches.

The extended facility scan and control points listed in Tables B-8, B-9, B-10, and B-11 overcome the limitations of the detailed AS&C set previously described. Even with the addition of the scan points, failures relating to outgoing DS1 and DS3 facilities are not identified to the specific affected facility.

### DS1 Facilities

A single scan point is provided for each incoming DS1 signal. This point indicates whenever the specified DS1 signal exceeds the BPV error threshold of $10^{-3}$ through $10^{-9}$ or is in an LOS condition. Table B-8 lists these scan points. These scan points require four additional displays for each DS1 Interface Module.

Table B-8. Extended Display Set (DS1 INTFC Module) — Scan Points

| Display † | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1-56 | S | Incoming DS1 Signal-{1-56} Fail |
| | 57-63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1-56 | S | Incoming DS1 Signal-{57-112} Fail |
| | 57-63 | - | Unassigned |
| | 64 | - | Reserved |
| 3 | 1-56 | S | Incoming DS1 Signal-{113-168} Fail |
| | 57-63 | - | Unassigned |
| | 64 | - | Reserved |
| 4 | 1-56 | S | Incoming DS1 Signal-{169-224} Fail |
| | 57-63 | - | Unassigned |
| | 64 | - | Reserved |

* S = Scan

† There are four displays per DS1 Interface Module.

## DS3 Facilities

For each service MUX circuit pack in a DS3 Interface Module, one alarm point is provided to indicate signal format mismatches (M13 or CBIT) and seven alarm points are provided to indicate DS2 signals within the incoming DS3 facility that are OOF. Table B-9 lists these points. These scan points require four additional displays for each DS3 Interface Module.

Table B-9. **Extended Display Set (DS3 INTFC Module) — Scan Points**

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1-7 | A | DS3 1, DS2-{1-7} OOF |
| | 8-14 | A | DS3 2, DS2-{1-7} OOF |
| | 15-21 | A | DS3 3, DS2-{1-7} OOF |
| | 22-28 | A | DS3 4, DS2-{1-7} OOF |
| | 29-35 | A | DS3 5, DS2-{1-7} OOF |
| | 36-42 | A | DS3 6, DS2-{1-7} OOF |
| | 43-49 | A | DS3 7, DS2-{1-7} OOF |
| | 50-56 | A | DS3 8, DS2-{1-7} OOF |
| | 57-63 | A | DS3 9, DS2-{1-7} OOF |
| | 64 | - | Reserved |
| 2 | 1-7 | A | DS3 10, DS2-{1-7} OOF |
| | 8-14 | A | DS3 11, DS2-{1-7} OOF |
| | 15-21 | A | DS3 12, DS2-{1-7} OOF |
| | 22-28 | A | DS3 13, DS2-{1-7} OOF |
| | 29-35 | A | DS3 14, DS2-{1-7} OOF |
| | 36-42 | A | DS3 15, DS2-{1-7} OOF |
| | 43-49 | A | DS3 16, DS2-{1-7} OOF |
| | 50-56 | A | DS3 17, DS2-{1-7} OOF |
| | 57-63 | A | DS3 18, DS2-{1-7} OOF |
| | 64 | - | Reserved |
| 3 | 1-7 | A | DS3 19, DS2-{1-7} OOF |
| | 8-14 | A | DS3 20, DS2-{1-7} OOF |
| | 15-21 | A | DS3 21, DS2-{1-7} OOF |
| | 22-28 | A | DS3 22, DS2-{1-7} OOF |
| | 29-35 | A | DS3 23, DS2-{1-7} OOF |
| | 36-42 | A | DS3 24, DS2-{1-7} OOF |

* A = Alarm

† There are four displays per DS3 Interface Module.

Table continued on next page.

Table B-9. Extended Display Set (DS3 INTFC Module) — Scan Points (Continued)

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 3 | 43-49 | A | DS3 25, DS2-{1-7} OOF |
| | 50-56 | A | DS3 26, DS2-{1-7} OOF |
| | 57-63 | A | DS3 27, DS2-{1-7} OOF |
| | 64 | - | Reserved |
| 4 | 1-7 | A | DS3 28, DS2-{1-7} OOF |
| | 8-14 | A | DS3 29, DS2-{1-7} OOF |
| | 15-21 | A | DS3 30, DS2-{1-7} OOF |
| | 22-28 | A | DS3 31, DS2-{1-7} OOF |
| | 29-59 | A | DS3 Signal-{1-31} Format Mismatch |
| | 60-63 | - | Unassigned |
| | 64 | - | Reserved |

* A = Alarm

† There are four displays per DS3 Interface Module.

## STS1 Interface Module AS&C Points

All AS&C points for STS1 Interface Modules are provided as extended alarm sets. Alarm, scan, and control points are provided for equipment associated with STS1 Interface Modules. In addition, for each incoming STS-1 facility to a SMUX circuit pack, eight alarm points (120 alarm points for each SMUX circuit pack) are provided to indicate:

- Loss of signal or high bit error rate (LOS/T-BERL)
- Loss of frame (LOF)
- Loss of pointer (LOP)
- Line alarm indication signal (AISL)
- Path alarm indication signal (AISP)
- Path yellow (YEL)
- Far-end remote failure (FERF)
- Signal label match failure (SLMF)

For a VT1.5 tributary signal within an EC-1 facility, the following points are provided:

- Fifteen alarm points to identify one or more VT LOP condition(s)
- Fifteen status points to identify one or more VT path yellow condition(s) has been detected on an upstream tributary failure

Tables B-10 and B-11 lists the extended set scan and control points, respectively.

Table B-10. **Extended Display Set (STS1 INTFC Module) — Scan Points**

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 1 | 1 | A | Power Circuit Pack Fail |
| | 2 | - | Unassigned |
| | 3 | A | UC Fail SA |
| | 4-5 | A | CLKDR-{1,2} Fail SA |
| | 6-7 | A | CLKDR-{1,2} Fail NSA |
| | 8 | A | MUXPS Fail SA |
| | 9 | A | STS1 Interface Manual Function Initiated |
| | 10-14 | - | Unassigned |
| | 15-29 | S | SMUX-{1-15} Protection Switch Active |
| | 30 | S | SMUX Protection Switch Auto-Locked |
| | 31-45 | S | SMUX-{1-15} Protection Switch Locked |
| | 46-63 | - | Unassigned |
| | 64 | - | Reserved |
| 2 | 1-15 | A | SMUX-{1-15} Fail SA |
| | 16 | A | SMUXP (SMUX-16) Fail SA |
| | 17-31 | A | SMUX-{1-15} Fail NSA |
| | 32 | A | SMUXP (SMUX-16) Fail NSA |
| | 33-47 | A | Incoming STS-1 Signal-{1-15} LOF/T-BERL |
| | 48-62 | A | Incoming STS-1 Signal-{1-15} LOF |
| | 63 | - | Unassigned |

* A = Alarm
S = Scan

† There are five displays per STS1 Interface-16 Module.

Table continued on next page.

Table B-10. Extended Display Set (STS1 INTFC Module) — Scan Points (Continued)

| Display† | Point No. | Type * | Description |
|---|---|---|---|
| 3 | 64 | - | Reserved |
| | 1-15 | A | Incoming STS-1 Signal-{1-15} LOP |
| | 16-30 | A | Incoming STS-1 Signal-{1-15} AISL |
| | 31-45 | S | Incoming STS-1 Signal-{1-15} AISP |
| | 46-60 | S | Incoming STS-1 Signal-{1-15} YEL |
| | 61-63 | - | Unassigned |
| | 64 | - | Reserved |
| 4 | 1-15 | S | Incoming STS-1 Signal-{1-15} FERF |
| | 16-30 | A | Incoming STS-1 Signal-{1-15} SLMF |
| | 31-63 | - | Unassigned |
| | 64 | - | Reserved |
| 5 | 1-15 | A | STS1-{1-15}, VT1.5-{1-28} VT LOP |
| | 16-30 | S | STS1-{1-15}, VT1.5-{1-28} VT AISP |
| | 31-45 | S | STS1-{1-15}, VT1.5-{1-28} VT YEL |
| | 46-63 | - | Unassigned |
| | 64 | - | Reserved |

A = Alarm
S = Scan

† There are five displays per STS1 Interface-16 Module.

Table B-11. Extended Display Set (STS1 INTFC Module) — Control Points

| Display† | Point No. | Description |
|---|---|---|
| 1 | 1 | Unassigned |
| | 2-16 | SMUX-{1-15} Make Protection Switch |
| | 17 | SMUX-1 Lock Protection |
| | 18 | SMUX-1 Unlock Protection |
| | 19 | SMUX-2 Lock Protection |
| | 20 | SMUX-2 Unlock Protection |

† There is one display per STS1 Interface-16 Module.

Table continued on next page.

Table B-11. Extended Display Set (STS1 INTFC Module) — Control Points (Continued)

| Display† | Point No. | Description |
|---|---|---|
| 1 | 21 | SMUX-3 Lock Protection |
| | 22 | SMUX-3 Unlock Protection |
| | 23 | SMUX-4 Lock Protection |
| | 24 | SMUX-4 Unlock Protection |
| | 25 | SMUX-5 Lock Protection |
| | 26 | SMUX-5 Unlock Protection |
| | 27 | SMUX-6 Lock Protection |
| | 28 | SMUX-6 Unlock Protection |
| | 29 | SMUX-7 Lock Protection |
| | 30 | SMUX-7 Unlock Protection |
| | 31 | SMUX-8 Lock Protection |
| | 32 | SMUX-8 Unlock Protection |
| | 33 | SMUX-9 Lock Protection |
| | 34 | SMUX-9 Unlock Protection |
| | 35 | SMUX-10 Lock Protection |
| | 36 | SMUX-10 Unlock Protection |
| | 37 | SMUX-11 Lock Protection |
| | 38 | SMUX-11 Unlock Protection |
| | 39 | SMUX-12 Lock Protection |
| | 40 | SMUX-12 Unlock Protection |
| | 41 | SMUX-13 Lock Protection |
| | 42 | SMUX-13 Unlock Protection |
| | 43 | SMUX-14 Lock Protection |
| | 44 | SMUX-14 Unlock Protection |
| | 45 | SMUX-15 Lock Protection |
| | 46 | SMUX-15 Unlock Protection |
| | 47-63 | Unassigned |
| | 64 | Reserved |

† There is one display per STS1 Interface-16 Module.

# Display Requirements

The number of displays required depends on the choice of AS&C set and on the configuration of the system. The following paragraphs discuss the total number of displays required for each of the three AS&C sets previously described.

## Summary AS&C Points

The summary set consists of a single scan display.

## Detailed and Extended AS&C Points

Tables B-12 (scan points) and B-13 (control points) list the number of displays required for each module and, for each module type, how many modules can be equipped in a single system. Although the maximum number of DS3 or STS1 Interface Modules is 16 and the maximum number of DS1 Interface Modules is 32, the switch is limited to a capacity of 256/248 DS3/STS-1 equivalents and, therefore, the number of DS1 Interface Modules must be reduced by 4 for each DS3 Interface-32 Module and by 2 for each DS3 Interface-16 or STS1 Interface-16 Module in the system.

The maximum number of displays (detailed and extended) is 198 (6 for the Redundant Controller, Synchronizer, Switch, and Switch Power Modules and 192 for the 32 DS1 Interface Modules) for a DACS IV-2000 configuration consisting of a fully equipped switch, 32 DS1 Interface Modules, and no DS3 or STS1 Interface Modules. In normal practice, only changed displays are transmitted, and this greatly reduces the number of displays sent in any given polling interval. Displays for modules that are not equipped are not sent in response to a *Scan All* or *Scan Changed Displays*, but are indicated by a gap in the response.

The DACS IV-2000 can be equipped in a variety of configurations with different combinations of DS1, DS3, and STS1 interfaces. The configuration with the most displays has 32 DS1 Interface Modules and no DS3 or STS1 Interface Modules and requires 70 detailed displays (6 for the Redundant Controller, Switch, Synchronizer, and Switch Power Modules and 64 for the 32 DS1 Interface Modules).

Table B-12. Number of Scan Point Displays

| Module Type | Maximum Modules | Number of Displays per Module | |
|---|---|---|---|
| | | Detailed | Extended |
| RC, SYNC, and SW Modules | 1 | 6 | 0 |
| DS1 Interface Module (1-32) | 32 | 2 | 4 |
| DS3 Interface Module (1-8) | 8 | 5 | 4 |
| DS3 Interface Module (9-16) | 8 | 0 | 9 |
| STS1 Interface Module (1-16) | 16 | 0 | 5 |

Table B-13. Number of Control Point Displays

| Module Type | Maximum Modules | Number of Displays per Module | |
|---|---|---|---|
| | | Detailed | Extended |
| RC, SYNC, and SW Modules | 1 | 5 | 2 |
| DS1 Interface Module (1-32) | 32 | 1 | 0 |
| DS3 Interface Module (1-8) | 8 | 2 | 0 |
| DS3 Interface Module (9-16) | 8 | 0 | 2 |
| STS1 Interface Module (1-16) | 16 | 0 | 1 |

## Display Numbering

Table B-14 lists the AS&C display numbering assignments.

Table B-14. Scan Point Display Numbering

| Scan Display | Control Display | Module |
|---|---|---|
| 0 | - | Summary (entire system) |
| 1-6 | 1-5 | Redundant Controller Module, Synchronizer Module, Switch Module, and Switch Power Module |
| 7-11 | 7-8 | DS3 Interface 1 |
| 12-16 | 12-13 | DS3 Interface 2 |
| 17-21 | 17-18 | DS3 Interface 3 |
| 22-26 | 22-23 | DS3 Interface 4 |
| 27-31 | 27-28 | DS3 Interface 5 |
| 32-36 | 32-33 | DS3 Interface 6 |
| 37-41 | 37-38 | DS3 Interface 7 |
| 42-46 | 42-43 | DS3 Interface 8 |
| 47-48 | 48 | DS1 Interface 1 |
| 49-50 | 50 | DS1 Interface 2 |
| 51-52 | 52 | DS1 Interface 3 |
| 53-54 | 54 | DS1 Interface 4 |
| 55-56 | 56 | DS1 Interface 5 |
| 57-58 | 58 | DS1 Interface 6 |
| 59-60 | 60 | DS1 Interface 7 |
| 61-62 | 62 | DS1 Interface 8 |
| 63-64 | 64 | DS1 Interface 9 |
| 65-66 | 66 | DS1 Interface 10 |
| 67-68 | 68 | DS1 Interface 11 |
| 69-70 | 70 | DS1 Interface 12 |
| 71-72 | 72 | DS1 Interface 13 |
| 73-74 | 74 | DS1 Interface 14 |
| 75-76 | 76 | DS1 Interface 15 |
| 77-78 | 78 | DS1 Interface 16 |

Table continued on next page.

Table B-14. Scan Point Display Numbering (Continued)

| Scan Display | Control Display | Module |
|---|---|---|
| 79-80 | 80 | DS1 Interface 17 |
| 81-82 | 82 | DS1 Interface 18 |
| 83-84 | 84 | DS1 Interface 19 |
| 85-86 | 86 | DS1 Interface 20 |
| 87-88 | 88 | DS1 Interface 21 |
| 89-90 | 90 | DS1 Interface 22 |
| 91-92 | 92 | DS1 Interface 23 |
| 93-94 | 94 | DS1 Interface 24 |
| 95-96 | 96 | DS1 Interface 25 |
| 97-98 | 98 | DS1 Interface 26 |
| 99-100 | 100 | DS1 Interface 27 |
| 101-102 | 102 | DS1 Interface 28 |
| 103-104 | 104 | DS1 Interface 29 |
| 105-106 | 106 | DS1 Interface 30 |
| 107-108 | 108 | DS1 Interface 31 |
| 109-110 | 110 | DS1 Interface 32 |
| 111-119 | - | Unused |
| 120-123 | - | DS3 Interface 1 Extended Facilities |
| 124-127 | - | DS3 Interface 2 Extended Facilities |
| 128-131 | - | DS3 Interface 3 Extended Facilities |
| 132-135 | - | DS3 Interface 4 Extended Facilities |
| 136-139 | - | DS3 Interface 5 Extended Facilities |
| 140-143 | - | DS3 Interface 6 Extended Facilities |
| 144-147 | - | DS3 Interface 7 Extended Facilities |
| 148-151 | - | DS3 Interface 8 Extended Facilities |
| 152-155 | - | DS1 Interface 1 Extended Facilities |
| 156-159 | - | DS1 Interface 2 Extended Facilities |
| 160-163 | - | DS1 Interface 3 Extended Facilities |
| 164-167 | - | DS1 Interface 4 Extended Facilities |

Table continued on next page.

Table B-14. Scan Point Display Numbering (Continued)

| Scan Display | Control Display | Module |
|---|---|---|
| 168-171 | - | DS1 Interface 5 Extended Facilities |
| 172-175 | - | DS1 Interface 6 Extended Facilities |
| 176-179 | - | DS1 Interface 7 Extended Facilities |
| 180-183 | - | DS1 Interface 8 Extended Facilities |
| 184-187 | - | DS1 Interface 9 Extended Facilities |
| 188-191 | - | DS1 Interface 10 Extended Facilities |
| 192-195 | - | DS1 Interface 11 Extended Facilities |
| 196-199 | - | DS1 Interface 12 Extended Facilities |
| 200-203 | - | DS1 Interface 13 Extended Facilities |
| 204-207 | - | DS1 Interface 14 Extended Facilities |
| 208-211 | - | DS1 Interface 15 Extended Facilities |
| 212-215 | - | DS1 Interface 16 Extended Facilities |
| 216-219 | - | DS1 Interface 17 Extended Facilities |
| 220-223 | - | DS1 Interface 18 Extended Facilities |
| 224-227 | - | DS1 Interface 19 Extended Facilities |
| 228-231 | - | DS1 Interface 20 Extended Facilities |
| 232-235 | - | DS1 Interface 21 Extended Facilities |
| 236-239 | - | DS1 Interface 22 Extended Facilities |
| 240-243 | - | DS1 Interface 23 Extended Facilities |
| 244-247 | - | DS1 Interface 24 Extended Facilities |
| 248-251 | - | DS1 Interface 25 Extended Facilities |
| 252-255 | - | DS1 Interface 26 Extended Facilities |
| 256-259 | - | DS1 Interface 27 Extended Facilities |
| 260-263 | - | DS1 Interface 28 Extended Facilities |
| 264-267 | - | DS1 Interface 29 Extended Facilities |
| 268-271 | - | DS1 Interface 30 Extended Facilities |
| 272-275 | - | DS1 Interface 31 Extended Facilities |
| 276-279 | - | DS1 Interface 32 Extended Facilities |
| 280-284 | 280-281 | DS3 Interface 9 |

Table continued on next page.

Table B-14. Scan Point Display Numbering (Continued)

| Scan Display | Control Display | Module |
|---|---|---|
| 285-289 | 285-286 | DS3 Interface 10 |
| 290-294 | 290-291 | DS3 Interface 11 |
| 295-299 | 295-296 | DS3 Interface 12 |
| 300-304 | 300-301 | DS3 Interface 13 |
| 305-309 | 305-306 | DS3 Interface 14 |
| 310-314 | 310-311 | DS3 Interface 15 |
| 315-319 | 315-316 | DS3 Interface 16 |
| 320-323 | - | DS3 Interface 9 Extended Facilities |
| 324-327 | - | DS3 Interface 10 Extended Facilities |
| 328-331 | - | DS3 Interface 11 Extended Facilities |
| 332-335 | - | DS3 Interface 12 Extended Facilities |
| 336-339 | - | DS3 Interface 13 Extended Facilities |
| 340-343 | - | DS3 Interface 14 Extended Facilities |
| 344-347 | - | DS3 Interface 15 Extended Facilities |
| 348-351 | - | DS3 Interface 16 Extended Facilities |
| 352-355 | 355 | STS1 Interface 1 |
| 356-359 | 359 | STS1 Interface 2 |
| 360-363 | 363 | STS1 Interface 3 |
| 364-367 | 367 | STS1 Interface 4 |
| 368-371 | 371 | STS1 Interface 5 |
| 372-375 | 375 | STS1 Interface 6 |
| 376-379 | 379 | STS1 Interface 7 |
| 380-383 | 383 | STS1 Interface 8 |
| 384-387 | 387 | STS1 Interface 9 |
| 388-391 | 391 | STS1 Interface 10 |
| 392-395 | 395 | STS1 Interface 11 |
| 396-399 | 399 | STS1 Interface 12 |
| 400-403 | 403 | STS1 Interface 13 |
| 404-407 | 407 | STS1 Interface 14 |

Table continued on next page.

Table B-14. **Scan Point Display Numbering (Continued)**

| Scan Display | Control Display | Module |
|---|---|---|
| 408-411 | 411 | STS1 Interface 15 |
| 412-415 | 415 | STS1 Interface 16 |
| 416 | - | STS1 Interface 1 Extended Facilities |
| 417 | - | STS1 Interface 2 Extended Facilities |
| 418 | - | STS1 Interface 3 Extended Facilities |
| 49 | - | STS1 Interface 4 Extended Facilities |
| 420 | - | STS1 Interface 5 Extended Facilities |
| 421 | - | STS1 Interface 6 Extended Facilities |
| 422 | - | STS1 Interface 7 Extended Facilities |
| 423 | - | STS1 Interface 8 Extended Facilities |
| 424 | - | STS1 Interface 9 Extended Facilities |
| 425 | - | STS1 Interface 10 Extended Facilities |
| 426 | - | STS1 Interface 11 Extended Facilities |
| 427 | - | STS1 Interface 12 Extended Facilities |
| 428 | - | STS1 Interface 13 Extended Facilities |
| 429 | - | STS1 Interface 14 Extended Facilities |
| 430 | - | STS1 Interface 15 Extended Facilities |
| 431 | - | STS1 Interface 16 Extended Facilities |

# Glossary

## A

**ABS (Absent)**
The circuit pack and a blank circuit pack is not in the associated slot.

**ACO (Alarm Cutoff)**
A button on the Status Panel used to silence audible alarms. Audible alarms can also be silenced using the `OPR-ACO-ALL` command.

**ACT (Active)**
The circuit pack or module is in service and not protected. If it is a traffic-carrying circuit pack or module, it is carrying traffic.

**Alarm**
An indication that a failure has occurred within a piece of equipment and/or a transmission facility.

**Alarm Delay**
Specifies the alarm delay (in seconds) for software-detected alarm conditions. Initial value is 10 seconds.

**Alarm Indication Signal (AIS)**
A signal transmitted downstream if the incoming signal is defective.

**All-Ones Signal**
Signal that is defined to contain all ones, AIS is an example of an all-ones signal.

**Alphanumeric Characters**
Letters and digits.

**Alternate Mark Inversion (AMI)**
A DS1 line code in which alternate one bits are positive and negative, but zero substitution is not used.

**ASCII Characters**
Letters, digits, and symbols used in the American Standard Code for Information Interchange.

**AS&C (Alarm, Scan, and Control) Points**
Interface between the DACS IV-2000 and telemetry operations systems (OSs).

**Attribute (ATTR)**
Alarm indication level: critical, major, minor, or no alarm.

**Autolock**
When the system autolocks an circuit pack, it switches to protection and forbids return to the working circuit pack even if the trouble clears. This is usually caused by multiple protection switches on that circuit pack in a short time period.

**Autolock Numbers of Switches**
This parameter is the number of times that the system restores a circuit pack to service (after intermittent failures) in a given autolock switching interval before the circuit pack is autolocked.

**Autolock Release Time**
The number of hours between times when the system automatically releases autolock.

**Autonomous**
Done by the system without direction by you.

**Auto-provisioning**
Put into the provisioned state automatically by the system.

**AVAIL (Available)**
Circuit pack or interface module is not provisioned and not assigned in the database. The circuit pack or interface module is not monitored by the system.

# B

**B3ZS**
Bipolar with 3-zero substitution; a DS3 or STS-1 line code.

**B8ZS**
Bipolar with 8-zero substitution; a DS1 line code.

**Battery Distribution Feeder Board (BDFB)**
Lineage 2000 (or equivalent) battery plant (-48 Vdc nominal) used to supply power to the DACS IV-2000. New Release 4.0 frame orders use two BDFBs (red and blue power feeds), while existing frames software upgraded to Release 4.0 use one BDFB.

**Baud Rate**
Transmission rate (bits per second) on a link.

**BER Metric**
Specifies the metric for calculating bit error rate at a DS3 interface port. Options are bipolar variations (BPV) or parity (PTY). Initial value is BPV.

**Bipolar Variation**
A variation of the alternating +1, -1 pattern in a 3-level code.

**Bit Error Rate (BER) Threshold**
Point at which an alarm is issued for bit errors.

**BLK (Blank)**
Circuit pack slot contains a bus extender (blank) circuit pack.

**Blue Code**
Same as alarm indication signal (AIS).

**Boot**
To transfer contents of backup memory into the system's working memory.

**Broadcast**
To take a signal from a single input port and connect it to multiple output ports.

**Byte**
Usually refers to a group of eight consecutive binary digits, but sometimes used for bit groups of other sizes.

# C

**Call Redirect**
Autonomous action taken when the ECI circuit pack an X.25 network is connected to fails. A call redirect takes up to 2 minutes to complete and switches the X.25 network to the working ECI circuit pack.

**C-bit Parity**
Parity checks on blocks of data are used to detect bits in error. C-bit parity is a DS3 format specified by ANSI T1.107 that supports near-end and far-end path performance monitoring, contains far-end alarm/control, and three end-to-end overhead communications channels.

**CILINK (Communication Interface Link)**
Access port that allows users or operations systems (OSs) to communicate with the DACS IV-2000.

**Clear (CL)**
The state where an alarm condition no longer exists.

**Clear-channel**
A channel in which all bandwidth is used, with no overhead bits.

**Command Mode**
One of two modes used to communicate with the DACS IV-2000. This mode involves entering commands directly into the system without any prompts.

**Condition**
The type of alarm failure, such as internal and loss of signal.

**Control Cable ID**
Specifies the controller cable identification associated with an interface module or a DS3 performance monitor (DS3PM) circuit pack (J cable).

**Control Complex (CC)**
A set of circuit packs (CPU/MTC/SSC) that provide all control functions for the DACS IV-2000. For the redundant controller, two control complexes are provided for increased reliability of the main controller.

**Critical (CR)**
Indicates a severe, service-affecting condition.

**Cross-Connect**
Hardware used to interconnect line-terminating equipment, multiplexers, and other equipment, allowing access to these facilities and having the ability to change these facilities as required.

**Crosstalk**
An unwanted signal induced into one transmission line from another transmission line.

**Current Value**
In the dialog mode, it indicates that the current value of a parameter is used by the system unless you direct otherwise.

# D

**Database**
A record of cross-connections, status of circuit packs and facilities, and other data.

**Default**
A value the system automatically uses for a parameter if the you do not specify a value.

**Delimiter**
A punctuation mark (colon or comma) used to separate two parameters in an input message.

**Demultiplexer**
An electronic device used with a multiplexed signal for recovering signals combined within it and restoring the distinct individual channels of these signals.

**Diagnose**
To test a circuit pack.

**Display Number**
Specifies a TABS display number.

**Double Ampersand (&&)**
Specifies multiple addressed ranges of equipment, links, or ports. For example, 1&&-6 means equipment/link/port locations 1 through 6.

**Driven**
A condition in which an interface with a connection is being monitored.

**DS1GRP**
A group of 28 DS1 ports in either an SWIF, a MUX, or an SMUX [VT1.5(DS1) signals] circuit pack.

**DS1 Port**
Terminates a DS1 signal on either a DS1IF (one of 14 ports), as part of a DS3 signal on a MUX, or as part of an STS-1(VT1.5) signal on an SMUX circuit pack.

**DS1 Signal**
A logical signal with a data rate of 1.544 Mbits/s (ANSI T1.107). A DS1 signal is produced by combining 192 payload bits and one framing bit; for example, 24 DS0 signals (eight bits per DS0) can be combined with one framing bit, thereby transmitting 193 bits per frame.

**DS2 Signal**
A logical signal with a data rate of 6.312 Mbits/s (ANSI T1.107). A DS2 signal is produced by combining seven DS1 signals.

**DS3 Equivalent**
The second item in the address of a port. It refers either to a MUX circuit pack or to an SWIF circuit pack, which handles 28 DS1 signals.

**DS3 Format**
Specifies the line format of a DS3 interface port. The initial value is M13, the common multiplexer format.

**DS3 Idle Signal**
A signal that can be optionally applied to any DACS IV-2000 output port that is not cross-connected to any input port. This signal lets *downstream* network elements know that the facility is operating normally even though the DACS IV-2000 is not sending a normal DS3 signal.

**DS3 Interface Port**
Specifies a DS3 port on a MUX circuit pack. If the value UNIT is given, it indicates all the DS3 interface ports in that DS3 Interface Module.

**DS3 Signal**
A logical or electrical B3ZS signal with a data rate of 44.736 Mbits/s (ANSI T1.107). For the DACS IV-2000, a traffic-carrying DS3 signal is made up of 28 DS1 signals and control bits used for synchronization and other purposes. The DS3 signal consists of a succession of masterframes approximately 106 μs long. Each masterframe contains seven subframes, each of which consists of eight data blocks. A data block contains one control bit and 84 data bits, with three data bits coming from each of the 28 DS1 signals that make up the DS3 signal.

**DSX-1, 2, 3**
Digital cross-connect used to interconnect equipment, provide patch capability, and provide test access at the DS1, DS2, or DS3 level.

**Duplex Entity**
A pair of circuit packs in which one is active and the other is in hot standby (clock generators).

# E

**Electrical Carrier 1 (EC-1)**
The industry standard nomenclature for an electrical STS-1 signal.

**Echo**
Display an input at a terminal (a user ID is echoed, but a password is not).

**Electromagnetic Compatibility (EMC)**
A measure of equipment tolerance to external electromagnetic fields.

**Electromagnetic Interference (EMI)**
Interference generated in a circuit by electromagnetic radiation energy coupling.

**Electrostatic Discharge (ESD)**
Static electrical energy potentially harmful to circuit packs and humans.

**Enter**
To provision a circuit pack or interface module by a command, not automatically by the system.

**Entity**
A specific piece of hardware (such as a circuit pack, memory device, or communication link) that has been assigned a name recognized by the system.

**Entity Identifier**
The name used by the system to refer to a circuit pack, memory device, or communication link.

**EQPT (Equipped)**
The circuit pack or interface module is in the system database and physically in the frame, but is not yet provisioned.

**Equalizer**
A circuit adjustment used to maintain signal strength between desired limits.

## F

**Facility**
A one-way or two-way circuit connected to the DACS IV-2000 that carries a transmission signal (such as a DS1 or STS-1 signal).

**Fault**
The circuit pack has a hard (not temporary) fault and can not be able to provide its normal function.

**Forced**
A traffic-carrying circuit pack (either service or protection) has been deliberately locked into a service-providing state by a manual command despite being bad.

**Frame**
The smallest repetitive block of digital data being transmitted (for example, 193 bits in a DS1 signal), which contains twenty-four 8-bit bytes and a synchronizing frame bit. Also refers to an assembly of equipment units, such as a DACS IV-2000 frame.

## G

**Grooming**
Rearrangement of DS1/VT1.5 signals in DS3/STS-1 signals.

## H

**Hardware ID**
Specifies the hardware identification (type and version) of a circuit pack.

**Header**
The first line of a message.

**Header Date**
Specifies the current date as YYMMDD, where YY is the last two digits of the year, MM is the month, and DD is the day of the month.

**Header Time**
Specifies the current time of day as HHMMSS, where HH is the hour (00 to 23), MM is the minutes, and SS is the seconds.

**Hierarchy**
An orderly ranking or sequence of elements, such as that of menus presented at a terminal.

**Hit**
A momentary disruption of service.

**Hot Standby**
A circuit pack ready for fast, automatic placement into operation to replace an active circuit pack.

# I

**Idle**
An output port is idle if it is not cross-connected to an input port.

**Idle Code**
A signal I that is transmitted downstream automatically from an idle output port; it can also be transmitted downstream by a manual command from a cross-connected output port. The DS1 idle code (the same as DS1 alarm indication signal) consists of all ones.

**In-Service (IS)**
A state in which the circuit pack is performing normal service functions, in either active or standby mode.

**Input Status**
The input signal status of a DS1, DS3, VT1.5, or STS1 interface port, which can be:

- DRVN (driven) — where a signal is expected at the port, and the port is being monitored for failures
- NDRVN (not driven) — where no valid signal is expected at the port, and the port is not being monitored for failures
- INIT (initialized) — or unset meaning that the port is considered not driven until a valid signal is detected, at which time it becomes driven
- QRSS (quasi-random signal source) — a DS1 port is provisioned as the QRSS for the system.

Initial values are INIT for a DS1 interface port, DRVN for a DS3, VT1.5, and STS-1 interface port, and DRVN for DS1 ports of an DS3 interface port.

# J

**Jitter**
Short-term variations in properties of a digital signal.

# L

**Line**
A transmission medium, together with the associated equipment, required to provide the means of transporting information between two consecutive network elements; one network element originates the line signal and the other terminates the line signal.

**Line Buildout**
An attenuating (signal-reducing) element used to keep DS3 or STS-1 output signal strength within desired limits. The line buildout setting for MUX or SMUX circuit packs includes:

- IN — the line buildout is in use, reducing the output signal strength
- OUT — the line buildout is not in use
- INIT — initialized (unset)

**Linecode Type**
Specifies the code type for a DS1 port terminating in a DS1 circuit pack, B8ZS or AMI.

**Line Layer**
The third layer of the standard SONET signal, used for reliable transport of the path layer payload and its overhead across the physical medium. The added overhead is accessed at points where STS signals are formed or terminated. Both lower layers (the photonic and section layers) exist to provide transport for this layer.

**Link ID**
The location and type of a user interface link.

**Literal Character**
A letter, digit, or symbol that is entered in a command. The first hyphen in UNIT-{1-64} is a literal character; the braces and the second hyphen are not literal characters.

**Location**
An identifier for a specific circuit pack, interface module, interface port, or communications link.

**Loopback (LPBK)**
A circuit arrangement that causes a received signal to be returned to its source.

**Loopback State**
Specifies the state of DS1, VT1.5, and STS-1 port loopback

- LPBKL (line loopback) — loops the signal from an input port to the corresponding output port in the same circuit pack by a connection in the circuit pack
- LPBKT (terminal loopback) — loops the signal from an input port to the corresponding output port in the same circuit pack by a cross-connection in the switch module
- LPBKI (internal loopback) — loops the signal from an output port to the corresponding input port of the same circuit pack.

# M

**M13**
A standard format used for DS3 signals, produced by a DS1-to-DS3 multiplexer.

**Maintenance Condition (MCOND)**
A circuit pack state in which some normal service functions are suspended, either because of a problem or to perform special functions (copy memory) that cannot be performed while normal service is being provided.

**Mapped**
Cross-connected.

**Memory Class**
One of two types of memory in the DACS IV-2000: PROG (software release) or DBASE (database).

**Memory Data**
Specifies the data (eight hexadecimal digits) associated with a memory type.

**Memory Location**
Specifies the equipment, DS1 interface port, DS3 MUX port, or STS-1 SMUX port location associated with a memory type.

**Memory Type**
Specifies the memory device, which may be:

- WKG — working (system) random access memory
- PRI — primary backup (disk)
- SEC — secondary backup (optical disk), INIT.

**Menu/Prompt Mode**
One of two modes used to communicate with the DACS IV-2000. When operating in this mode, the system lets you choose commands from menus and then prompts you for information to complete the command.

**Major (MJ)**
Indicates a service-affecting failure, main or unit controller failure, or power supply failure.

**Minor (MN)**
Indicates a non-service-affecting equipment or facility failure.

**Multiplexer**
An electronic device that allows two or more signals to pass over one communications circuit.

**Multipoint Address**
Specifies the Layer 2 (multipoint) address used on a TABS link.

# N

**N-Rate Cable**
A cable that carries an N-rate signal (27.648 Mbits/s), which includes 14 DS1 signals, half of an STS-1(cc-SPE) signal, or 14 STS-1(VT1.5) signals and timing information.

**Network Element**
A DACS IV-2000 frame is a network element.

**Notification Code**
The notification code for alarm and status conditions, which include:

- MJ — major alarm
- MN — minor alarm
- NA — indicates no alarm (status only)
- CL — cleared alarm.

**NOVAL (no value)**
In dialog mode, it indicates that no value is used for this parameter unless you enter one.

# O

**Out Of Service (OOS)**
*The circuit pack is not providing its normal service function (removed from service or protected)* either because of a system problem or because it has been removed from service manually.

**Outage**
A disruption of service that lasts for more than one second.

**Output Mode**
Specifies what is being transmitted from a DS1, VT1.5, or STS-1 output port. The modes are:

- NORM — normal cross-connected data
- TERM (terminated) — IDLE code
- AIS — alarm indication signal
- QRSS (quasi-random signal source) — an externally generated DS1 test signal, assumed to be quasi-random.

Initial value is NORM.

# P

**Parity Check**
A check that tests whether the number of ones (or zeros) in an array of binary bits is odd or even; checks to determine that the received signal is the same as the transmitted signal.

**Path**
A logical connection between the point at which a standard frame format for the signal at the given rate is assembled, and the point at which the standard frame format for the signal is disassembled.

**Path Layer**
The highest of the four layers of a standard SONET signal, used to transport services between path terminating network elements. Examples of such services include DS1s, DS3s (synchronous and asynchronous), and video signals.

**Path Overhead (POH)**
Informational bytes assigned to and transported with the payload until the payload is demultiplexed.

**Payload Pointer**
The pointer that shows the location of the beginning of the Synchronous Payload Envelope (SPE).

**Photonic Layer**
The lowest of the four layers in a standard SONET signal, used to convert STS signals and OC (optical carrier) signals.

**Poll Timing**
Specifies how often (in seconds) the system expects a poll request from a telemetry remote on a TABS link.

**Port**
The place of access on an interface circuit pack that connects the DACS IV-2000 to a DS1, DS3, or STS-1 signal.

**Primary Line**
The second line in an output message.

**Program**
The software that directs the operation of the main controller and other frame elements.

**Protocol**
Detailed format and procedures used for transmitting digital data.

**Protocol Type**
Indicates the protocol supported on a interface link.

**Provision**
To set parameters to establish the environment required for correct interaction of hardware, software, and peripherals.

**Provisioned (PROV)**
The circuit pack is ready to perform its intended function. A provisioned circuit pack can be active (ACT), in-service (IS), standby (STBY), provisioned out-of-service (POS), or out-of-service (OOS).

**Pulse Code Modulation (PCM)**
The process by which analog signals are sampled, quantized, and coded into a digital bit stream.

# Q

**Quasi-random Signal Source (QRSS)**
Equipment that generates a specific, reproducible but complicated digital test signal that resembles a normal traffic-carrying DS1 signal.

# R

**Redlined**
A circuit that is given special protection against unintentional disconnection.

**Released**
If an input port, it is not under test access; if an output port, it is not cross-connected to an input port under test access.

**Return to Zero**
A code form having two information states termed zero and one and having a third state or an at-rest condition to which the signal returns during each period.

**Rollover**
Operation used when the transmission facility between the system and an upstream system is to be replaced.

# S

**Section**
The portion of a transmission facility, including terminating points, between:

- a terminal network element and a line-terminating network element, or
- two line-terminating network elements.

A terminating point is the point, after single regeneration, at which performance monitoring is done.

**Section Layer**
The second of the four levels in a standard SONET signal, used to transport an STS frame across a physical medium. This layer uses the photonic layer to form the physical transport.

**Side Switch**
The autonomous action taken when the active control complex (CC) fails. A side switch takes up to 5 minutes to complete and switches the standby CC to the active state.

**Single Ampersand (&)**
Specifies multiple addressed equipment, links, or ports. For example, 1&-5 means equipment/link/port locations 1 and 5.

**Snider**
Protocol (message format) used on administrative links.

**Software ID**
Number that provides the software version information for the system. The software ID contains:

- a 1-digit number that indicates the software release
- a 2-digit number that indicates the issue
- a 3-digit number that indicates the point release

**Split**
Test access state in which an incoming signal is cross-connected to the receiver of a test set rather than to a previously connected output port, and a signal from the transmitter of the test set is cross-connected to the previously connected output port.

**Standby (STBY)**
The circuit pack is in service but is not providing service functions. It is ready to be used to replace a similar circuit pack either by protection or by duplex switching.

**State**
The state of a circuit pack indicates whether it is defective or normal (ready for normal use).

**STSX-1**
Digital cross-connect used to interconnect equipment, provide patch capability, and provide test access at the STS-1 level.

**STS1 Interface Port**
Specifies an STS1 port on an SMUX circuit pack.

**STS Envelope Capacity**
Bandwidth within, and aligned to, the STS frame that carries the STS SPE.

**STS Path Overhead**
Nine evenly distributed path overhead bytes per 125 µs starting at the first byte of the STS SPE. STS path overhead provides for communications between the point of assembly of an STS SPE and its point of disassembly.

**STS Payload Capacity**
The maximum bandwidth within the STS SPE that is available for payload.

**STS-1 Signal**
The basic building block signal in the SONET standard (ANSI T1.105 and Bellcore TR-NWT-000253, *SONET Transport Systems: Common Generic Criteria for Operations Communications Routing and LAN Support* (Issue 7, September 1992). An STS-1 signal has a data rate of 51.84 Mbits/s. An STS-1 signal frame consists of 90 columns and 9 rows of 8-bit bytes, for a total of 810 bytes (6480 bits) for a frame length of 125 µs. The first three columns of an STS-1 signal are the *transport overhead*, which contains overhead bytes of *section* (nine bytes) and *line* (eighteen bytes) layers. The remaining 87 columns of 9 rows of bytes (783 bytes) make up the *STS-1 envelope capacity.*

**STS Synchronous Payload Envelope (STS SPE)**
A 125-µs frame structure composed of STS path overhead and bandwidth for payload.

**STS Transport Overhead**
The overhead (informational bytes that contain the line and section overhead) added to the STS SPE for transmission.

**Synchronous**
The essential characteristic of time scales or signals such that their corresponding significant instances occur at precisely the same average rate.

**Synchronous Network**
The synchronization of transmission systems with synchronous payloads to a master (network) clock that can be traced to a reference clock.

**Synchronous Payload**
Payloads that can be derived from a network transmission signal by removing integral numbers of bits from every frame; that is, no variable bit stuffing rate adjustments are required to fit the payload in the transmission signal.

**Subrate**
In the Digital Data System, a data bit rate that is either 2.4, 4.8, or 9.6 kbits/s.

# T

**T1**
Transmission carrier system at the rate of 1.544 Mbits/s (same as DS1 signal).

**T2**
Transmission carrier system at the rate of 6.312 Mbits/s (same as DS2 signal).

**T3**
Transmission carrier system at the rate of 44.736 Mbits/s (same os DS3 signal).

**Terminated**
Output mode in which idle code is transmitted downstream.

**Test Access**
Allows the DACS IV-2000 the ability to apply and monitor test signals in accordance with Bellcore TA-TSY-000203.

**Test Mode**
Specifies the test access mode.

**Test Signal Identification (TSID)**
Unique name given to a DS1 test signal.

**Tributary**
One of the 28 DS1 (1.544 Mbits/s) channels in a DS3 (44.736 Mbits/s) signal or one of 28 VT1.5 (1.728 Mbits/s) channels in an STS-1 (51.84 Mbits/s) signal.

# U

**User Community Authorization Level (UCAL)**
One of five levels that specify the user authorization level: 5 identifies a super user (system administrator); 1 identifies an ordinary user.

**Unit**
An interface module; the term is sometimes used instead of entity or subassembly.

**Unit Type**
Specifies the type of interface module:

- 32DS3 — for DS3 Interface-32 Module
- 16DS3 — for DS3 Interface-16 Module
- 16STS1 — for STS1 Interface-16 Module
- DS1 — for DS1 Interface Module
- DS1P — for DS1 Interface-Protection Module.

# V

**Virtual Tributary (VT)**
A structure designed for transporting and switching some STS1 payloads.

**Volatile Memory**
Type of memory that is lost if electrical power to it is interrupted.

**VT1.5 Port**
Terminates a VT1.5 signal that is part of an STS-1 signal on an SMUX circuit pack.

**VT1.5 Tributary**
A SONET logical signal with a data rate of 1.728 Mbits/s. In the 9-row structure of the STS-1 SPE, a VT1.5 occupies three columns. VT-structured STS-1 SPEs are divided into seven VT groups. Each VT group occupies twelve columns of the 9-row structure and, for VT1.5s, contains four VTs per group.

**VT Envelope Capacity**
Bandwidth within, and aligned to, the VT Superframe that is available for the VT SPE.

**VT Group**
A 9-row by 12-column structure (108 bytes) that carries one or more VTs of the same size. Seven VT groups (756 bytes) are byte-interleaved within the VT-organized SPE.

**VT Path Overhead**
One path overhead byte per 500-µs located at the first byte of the VT SPE. VT path overhead provides for communication between the point of assembly of the VT SPE and the point of its disassembly.

**VT Payload Capacity**
The maximum bandwidth within the VT SPE that is available for payload.

**VT Superframe**
The VT is organized into a 500-µs superframe structure overlaid on, and aligned to, a 125-µs STS1 SPE. Contained within this structure is the VT payload pointer and the VT SPE.

**VT Synchronous Payload Envelope (VT SPE)**
A 500-µs frame structure carried by the VT, composed of VT path overhead and bandwidth for payload. The envelope is contained within the VT envelope capacity and can have any alignment with respect to it.

# W

***Wideband Digital Cross-Connect System (WDCS)***
A digital cross-connect system that interfaces any one or combinations of the following signals: SONET, DS3, DS1 and has the basic functionality of cross-connecting at the floating SONET Virtual Tributary 1.5 (VT1.5) or the DS1 level. A SONET WDCS is a DCS that cross-connects at the VT1.5 level and provides SONET signal multiplexing and termination. A DSC 3/1 is a DCS that cross-connects at the D1 level and provides DS3 multiplexing and termination.

**Wideband Loopback**
The connection of a VT1.5 [VT1.5(cc-SPE) or VT1.5(DS1)] tributary from an incoming STS-1 facility to the outgoing direction of the same facility. This type of loopback differs from a line loopback in that the signal being looped-back is not at the line rate, and it is necessary to modify the VT pointer bits to perform the loopback. The DACS IV-2000 implements the wideband loopback as a terminal loopback (the loopback point is in the cross-connect network).

# Acronyms

## Symbols

| | |
|---|---|
| ° C | Degrees Celsius |
| ° F | Degrees Fahrenheit |

## A

| | |
|---|---|
| A | Ampere |
| ABS | Absent |
| AC | Alternating Current |
| ACO | Alarm Cutoff |
| ACPWR | AC Power<br>AC Power Failure |
| ACT | Activate<br>Active |
| ADM | Add-Drop Multiplexer |
| AIS | Alarm Indication Signal |
| AISFRAMED | Alarm Indication Signal Framed |
| AISL | Alarm Indication Signal, Line |
| AISP | Alarm Indication Signal, Path |
| AISS | Alarm Indication Signal Seconds |
| AISUNFRAMED | Alarm Indication Signal, Unframed |
| ALLDS2OOF | All DS2 Out-of-Frame |
| ALLDS2SOOF | All DS2s within DS3 Signal Out-of-Frame |
| ALLREFFAIL | All Timing References Failed |
| ALM | Alarm |
| ALW | Allow |
| AMI | Alternate Mark Inversion |
| ANSI | American National Standards Institute |
| AS&C | Alarm, Scan, and Control |
| ATTR | Attribute |
| AUTO | Automatic |
| AUX PWR | Auxiliary Power |

## B

| | |
|---|---|
| B3ZS | Bipolar with 3-Zero Substitution |
| B8ZS | Bipolar with 8-Zero Substitution |
| BDFB | Battery Distribution Feeder Board |
| BEC | Block Error Count |
| BER | Bit Error Rate |
| BERL | Line Bit Error Rate |
| BESP | Bursty Errored Seconds, Path |
| BIP | Bit Interleaved Parity |
| BKUPMEMS | Backup Memory Secondary Failure |
| BLK | Blank |
| BNC | Bayonet Navy Connector |
| BPV | Bipolar Violation |
| BXA | Bus Extender A |

## C

| | |
|---|---|
| CANC | Cancel |
| CB | Compatibility Bulletin |
| CC | Control Complex |
| cc | Clear Channel |
| CCITT | International Telegraph and Telephone Consultative Committee |
| CILINK | Communications Interface Link |
| CLKDR | Clock Distributor |
| CLKGN | Clock Generator |
| CLLI | Common Language Location Identification |
| CMOS | Complementary Metal Oxide Semiconductor |
| COM | Common |
| COMPL | Complete |
| CONTBUS | Control Bus Failure |
| CP-BITS | Copy of Parity Bits |
| CPU | Central Processing Unit |
| CPY | Copy |
| CR | Critical |
| CRC | Cyclic Redundancy Code |
| CRS | Cross-Connect |
| CRT | Circuit |
| CSS | Controlled Slipped Seconds |
| CVL | Code Violations, Line |
| CVP | Code Violations, Path |

## D

| | |
|---|---|
| DACS | Digital Access and Cross-Connect System |
| dBA | Decibels at sound-level meter A-weighting scale setting |
| DBCHG | Database Change |
| DISC | Disconnect |
| DM | Degraded Minute |

| | |
|---|---|
| DPLL | Digital Phase Lock Loop |
| DS0 | Digital Signal, Level 0 |
| DS1 | Digital Signal, Level 1 |
| DS1IF | DS1 Interface |
| DS1IP | DS1 Interface Protection |
| DS1RY | DS1 Relay |
| DS1TX | DS1 Timing Extractor |
| DS2 | Digital Signal, Level 2 |
| DS3 | Digital Signal, Level 3 |
| DS3FRMTMISMATCH | DS3 Format Mismatch |
| DS3PM | DS3 Performance Monitoring |
| DSAB | Digital Systems Access Bay |
| DSX | Digital Signal Cross-Connect |
| DSX-1 | Digital Signal Cross-Connect, Level 1 |
| DSX-3 | Digital Signal Cross-Connect, Level 3 |
| DTAU | Digital Test Access Unit |
| DTLCH | Data Latch Error |

## E

| | |
|---|---|
| EC-1 | Electrical Carrier, Level 1 |
| ECI | Enhanced Communications Interface |
| EID | Entity Identifier |
| EMC | Electromagnetic Compatibility |
| ENT | Enter |
| EOR | End-of-Range Error |
| ERRANAL | Error Analysis |
| ESA | Errored Seconds Type A |
| ESB | Errored Seconds Type B |
| ESD | Electrostatic Discharge |
| ESL | Errored Seconds, Line |
| ESP | Errored Seconds, Path |
| EVT | Event |
| EXJIT | Excessive Jitter |
| EXPHR | Excessive Phase Error |
| EXTERR | Error Detected External to System |
| EXZ | Excessive Zeros |

## F

| | |
|---|---|
| FAD | Facility Access Digroup |
| FBA | Fuse Board A |
| FBB | Fuse Board B |
| FBC | Fuse Board C |
| FBD | Fuse Board D |
| FBE | Framing Bit Error |
| FBF | Fuse Board F |
| FBG | Fuse Board G |
| FBH | Fuse Board H |
| FBI | Fuse Board I |
| FCC | Federal Communications Commission |
| FEAC | Facility and Equipment Alarm Conditions<br>Far-End Alarm and Control |
| FEBE | Far-End Bit Error |
| FEF | Family of Equipment Failure |
| FEPS | Facility and Equipment Planning System |
| FERF | 'Far-End Receive Failure<br>Far-End Receive Failure<br>Far-End Remote Failure |
| FLT | Fault |
| FMA-BITS | F and M Bits Adjusted |
| FMN-BITS | F and M Bits Nonadjusted |
| FRD | Security Violation has Occurred |
| FRQOF | Frequency Offset Error |
| FSNLN | Frequency Synthesizer Loss of Energy |
| FSTO | Phase Lock Loop Fast Start Timeout |

## G

| | |
|---|---|
| GRP | Group |
| GTP | General Telemetry Processor |

## H

| | |
|---|---|
| HDA | Header Designation Assembly |
| HI | High |

## I

| | |
|---|---|
| ICTLR | Interrupt Controller Error |
| ID | Denticulation |
| IHRER | Interrupt Holding Register Error |
| IMPROPBLK | Improper Blank |
| IMPROPRMVL | Improper Removal |

| | |
|---|---|
| INC | Incoming<br>Incoming Signal |
| INH | Inhibit |
| INHSWPR | Inhibit Switch to Protection |
| INHSWWKG | Inhibit Switch to Working |
| INT | Internal |
| INTFC | Interface |

## L

| | |
|---|---|
| LBO | Line Buildout |
| LCV | Line Code Violations |
| LED | Light Emitting Diode |
| LERDF | Line Error Detector Failure |
| LOC | Loss-of-Clock |
| LOCL | Local |
| LOF | Loss-of-Frame |
| LOOPE | Loop E |
| LOOPF | Loop F |
| LOP | Loss-of-Pointer |
| LOS | Loss-of-Signal |
| LOSS | Loss-of-Signal Seconds |
| LPBK | Loopback |
| LPBKI | Loopback, Internal |
| LPBKL | Loopback, Line |
| LPBKT | Loopback, Terminal |
| LSSIG | Loss-of-Signal |

## M

| | |
|---|---|
| MAN | Manual |
| Mbit/s | Mega Bits per Second |
| MC | Main Controller |
| MCOND | Maintenance Condition |
| MEM | Memory |
| MHz | Mega Hertz |
| MINC | Multiple Incoming<br>Multiple Incoming Signals |
| MJ | Major |
| MN | Minor |
| MONE | Monitor E |
| MONEF | Monitor E F |
| MONF | Monitor F |
| ms | Millisecond |
| MTBF | Mean Time Between Failures |
| MTBMA | Mean Time Between Maintenance Activities |
| MTC | Maintenance Controller<br>Maintenance Interface |
| MTCE | Maintenance |
| MTTR | Mean Time To Repair |
| MUX | Multiplexer |
| MUXP | Multiplexer Protection |
| MUXPS | Multiplexer Protection Switch |

## N

| | |
|---|---|
| NA | No Alarm<br>Not Available |
| NDF | New Data Flag |
| NE | Network Element |
| NEBE | Near-End Bit Error |
| NMA | Network Monitoring Analysis |
| NSA | Non-Service Affecting |
| NTE | Network Terminating Equipment |

## O

| | |
|---|---|
| OC-12 | Optical Carrier, Level 12 |
| OC-3 | Optical Carrier, Level 3 |
| OC-48 | Optical Carrier, Level 48 |
| OCS | Operations Communications System |
| OOF | Out-of-Frame |
| OOFAIS | Out-of-Frame Alarm Indication Signal |
| OOFS | Out-of-Frame Seconds |
| OOS | Out-of-Service |
| OPS/INE | Operations System/Intelligent Network Element |
| OS | Operations System |

## P

| | |
|---|---|
| PAD | Packet Assembler and Disassembler |
| PFLCH | Phase/Frequency Latch Error |
| PHSTP | Phase Step Error |
| PLL | Phase Lock Loop |
| PMGR | Performance Monitoring Generator/Receiver |
| PMREP | Performance Monitoring Report |
| POH | Path Overhead |

| | |
|---|---|
| PRI | Primary Storage |
| PRTL | Partial |
| PSET#1 | Parameter Set 1 |
| PSET#2 | Parameter Set 2 |
| PSHLN | Phase Shifter Output Loss-of-Energy |
| PTE | Path Terminating Equipment |
| PTY | Parity |
| PWR | Power |
| PWRA | Power A |
| PWRE | Power E<br>Power Supply E |
| PWRF | Power F |
| PWRG | Power G |

## Q

| | |
|---|---|
| QRSS | Quasi-Random Signal Source |

## R

| | |
|---|---|
| RAM | Random Access Memory |
| RAMER | RAM Error |
| RC | Redundant Controller |
| RC PWR | Redundant Controller Power |
| REPT | Report |
| RL | Retry Later |
| RLS | Release |
| RMS | Remote Management System |
| ROLL | Rollover |
| ROM | Read-Only Memory |
| ROMER | ROM Error |
| RTRV | Retrieve |
| RTV | Real-Time Violation |

## S

| | |
|---|---|
| SA | Service Affecting |
| SARTS | Switched Access Remote Testing System |
| SBIT | DS3 Stuff Bit Protocol |
| SBITFAIL | S Bits Failure |
| SCCS | Switching Control Center System |
| SCHED | Schedule |
| SCI | Switch Control Interface |
| SCSI | Small Computer System Interface |
| SEC | Secondary Storage |
| SEFS | Severely Errored Frame Seconds |
| SESL | Severely Errored Seconds, Line |
| SESP | Severely Errored Seconds, Path |
| SF | Super Frame |
| SLMF | Signal Label Match Failure |
| SLS | Slipped Seconds (see CSS) |
| SMUX | SONET Multiplexer<br>Synchronous Multiplexer |
| SMUXP | SONET Multiplexer Protection |
| SONET | Synchronous Optical Network |
| SPE | Synchronous Payload Envelope |
| SPLTA | Split A |
| SPLTB | Split B |
| SPLTE | Split E |
| SPLTEF | Split E F |
| SPLTF | Split F |
| SRV | Service |
| SSC | Secondary Storage Controller |
| SSS | Secondary Storage Subsystem |
| STPNL | Status Panel |
| STS-1 | Synchronous Transport Signal, Level 1 |
| SW | Switch |
| SW PWR | Switch Power |
| SWCS | Switch Center Stage |
| SWIF | Switch Interface |
| SWIO | Switch Input/Output |
| SYNC | Synchronizer |
| Sync | Synchronous |
| SYNCCLK | Synchronizer Clock Failure |
| SYNCFRNG | Synchronizer Transitioned to Free-Running Mode |
| SYNCFST | Synchronizer Transitioned to Fast-Start Mode |
| SYNCHLDOVR | Synchronizer Transitioned to Hold-over Mode |
| SYNCN | Synchronizer |
| SYNCPRI | Primary Timing Reference |
| SYNCSEC | Secondary Timing Reference |
| SYPLN | Sync Pulse Generator Loss-of-Energy |

## T

| | |
|---|---|
| T+BER | Bit Error Rate Threshold Exceeded |
| TA | Technical Advisory |

| | |
|---|---|
| TABS | Telemetry Asynchronous Block Serial |
| TACC | Test Access |
| TAP | Test Access Port |
| TB | Time Base (TBS3) |
| TBCOLD | Time Base Oven Cold |
| T-BER | Bit Error Rate Threshold |
| T-BERL | Line Bit Error Rate Threshold |
| TBIOER | Time Base Communication Error |
| TBLEN | Time Base Strobe Loss-of-Energy |
| TBNDF | Time Base Strobe Energy Detector Failure |
| TBOS | Telemetry Byte Oriented Serial |
| TBS3 | Time Base Stratum 3 |
| TCA | Threshold Crossing Alert |
| TH | Threshold |
| TID | Target Identifier |
| TIRKS | Trunks Integrated Record Keeping System |
| TL1 | Transaction Language 1 |
| TNM | Total Network Management |
| TODC | Time-of-Day Clock |
| TOPROTN | To Protection |
| TOWKG | To Working |
| TPA | Errored Seconds, Type A |
| TPB | Errored Seconds, Type B |
| TPC | Errored Seconds, Type C |
| TR9 | TR-TSY-000009 Remote Multiplexer |
| TRBER | High Bit Error Rate |
| TRMNBER | Minor Bit Error Rate |
| TS0 | Terminal Strip 0 |
| TS1 | Terminal Strip 1 |
| TS2 | Terminal Strip 2 |
| TSTF | Tests Failed |
| TTY | Terminal Typewriter |
| TX | Timing Extractor (DS1TX) |

## U

| | |
|---|---|
| UART | Universal Asynchronous Receiver/ Transmitter |
| UAS | Unavailable Seconds |
| UC | Unit Controller |
| UCAL | User Community Authorization Levels |
| UCFC | User Community Functional Category |
| UCPL | User Community Priority Level |
| UI | Unit Interface |
| UID | User Identification |
| UIT | User Interface Terminal |
| UNF | Unframed |
| UPC | User Privilege Code |
| URTER | UART Error |

## V

| | |
|---|---|
| VA | Volt Ampere |
| Vdc | Volts direct current |
| VT | Virtual Tributary |
| VT1.5 | Virtual Tributary, Level 1.5 |

## X

| | |
|---|---|
| X1LEN | Synchronizer 1 ms Cross-Couple Loss-of-Energy |
| X3LEN | Synchronizer 30 ms Cross-Couple Loss-of-Energy |
| XCOOL | Synchronizer Cross-Couple Out-of-Lock Error |
| XCRTV | Synchronizer Cross-Couple Real-Time Violation Error |
| XCSUM | Synchronizer Cross-Couple Summary Error |
| XFLRG | Synchronizer Cross-Couple Fast Lock Range Error |
| XFQOF | Synchronizer Cross-Couple Frequency Offset Error |
| XLKDN | Synchronizer Cross-Couple Communication Link Error |

## Y

| | |
|---|---|
| YEL | Yellow Signal |

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