Lucent Technologies
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DACS II
Release 8.0

Technical Specification

365-099-144TS
Issue 1
September 1998

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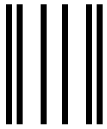

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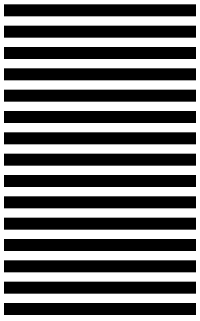

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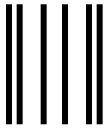

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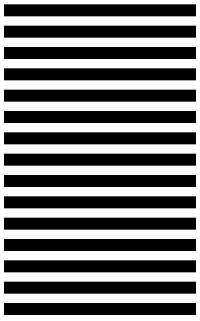

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Contents

Contents

Contents

Contents

Figures

6 Facility Alarms and Performance Monitoring

Tables

Tables

Tables

Tables

15 System Reliability

General Description

1

Contents

General Description

1

Overview

DACS II is a software-controlled Digital Cross-Connect System (DCS) which terminates DS1s, DS1s and E1s (2Mbit/s) within a DS3, and 2Mbit/s or 2048 kbit/s primary block facilities. DACS II provides cross-connect and test access for DS0, Nx64Kbit/s, clear DS1, clear 2Mbit/s, and Digital Data System (DDS) subrate signals. DACS II also supports Digital Signal Processing (DSP) functions for DS0 and DDS subrate signals. It also performs facility and equipment maintenance and provides interfaces for remote operations support. A fully equipped DACS II Capacity Expansion Frame (CEF) supports 7 bays and 16 units and provides a maximum capacity of 2,560 DS1 terminations, 2,048 2048 kbit/s primary block terminations, or 96 DS3 facilities (equivalent to 2,688 DS1 terminations). In addition, it supports the DSP functions with the capacity of 4,096 DS0 (64 kb/s) channels per Digital Signal Processing Unit (DSPU).

DACS II system timing is provided by a duplicated Synchronizer (SYNC) which obtains a reference signal from either a high-stability internal clock or from one of several external reference signals. DACS II internal operations and maintenance activities are controlled by a multiprocessor system interconnected by a Local Area Network (LAN). The system also provides nonvolatile storage for the executable code and the system data base.

This document contains technical specifications for DACS II features, performance information, external interfaces, environmental considerations, and system reliability. This information supplements the information contained in the DACS II documentation listed on the next page.

DACS II DOCUMENTATION

365-353-085	DACS II, Release 7.0, 24 Channel - Product Description
365-353-086	DACS II, Release 7.0, 30 Channel - Product Description
365-353-121	DACS II, Release 8.0 (PDS) - Operation and Maintenance Manual
365-353-122	DACS II, Release 8.0 (PDS) - Command and Message Manual
365-353-123	DACS II, Release 8.0 (PDS) - Quick Reference Guide
365-353-131	DACS II, Release 8.0 (MML) - Operation and Maintenance Manual
365-353-132	DACS II, Release 8.0 (MML) - Command and Message Manual
365-353-133	DACS II, Releases 8.0 (MML) - Quick Reference Guide
365-353-141	DACS II, Release 8.0 (PDS) 2.048 Mbit/s Interface - Operation and Maintenance Manual
365-353-142	DACS II, Release 8.0 (PDS) 2.048 Mbit/s Interface - Command and Message Manual
365-353-143	DACS II, Release 8.0 (PDS) 2.048 Mbit/s Interface - Quick Reference Guide
365-353-151	DACS II, Release 8.0 (MML) 2.048 Mbit/s Interface - Operation and Maintenance Manual
365-353-152	DACS II, Release 8.0 (MML) 2.048 Mbit/s Interface - Command and Message Manual
365-353-153	DACS II, Release 8.0 (MML) 2.048 Mbit/s Interface - Quick Reference Guide
CIR 365-099-136TD	DACS II Technical Description, Release 7.0 Features
SD 96683-01	Application Schematic for DACS II Enclosed Single Bay Frame (ESBF)
SD 96699-01	Application Schematic for DACS II Enclosed Capacity Expansion Frame (ECEF)

Synchronization and Timing

2

Contents

Contents

Synchronization and Timing

2

Overview

The Synchronizer is the main timing element for DACS II. It generates timing signals that are synchronized to the network timing references. The Synchronizer consists of fully duplicated circuit packs, each containing a set of up to four Timing Link Interfaces (TLIs), a Digital Phase Locked Loop (DPLL), a Time Base (TB), and a Synchronizer Power Unit (SPU).

The TLIs provide the external timing interface for the Synchronizer and can be optionally equipped as timing extractors (to derive timing) or timing distributors. The options may be equipped in a mixed configuration that both extracts and distributes timing signals.

The DPLL provides timing signals for DACS II. The two DPLLs in the duplicated Synchronizer exchange timing and status information for phase alignment and facilitate hitless protection switching operations.

The TBs contain oscillators used by the DPLLs to synthesize the DACS II system timing signals at the frequency of the incoming timing reference. In the event that all external timing references fail, the stability of the TBs determines the holdover stability of the Synchronizer.

Synchronizer Operation

The Synchronizer can be optionally equipped to operate at either the Stratum 3 or Stratum 2 level in the North American Synchronization Hierarchy in accordance with the following standard documents:

- "Digital Synchronization Network Plan", Bellcore Technical Advisory TA-NPL-000436, Issue 1, November 1986.
- "Synchronization Interface Standards for Digital Networks", ANSI T1.101-1987.
- "Digital Synchronization Network Plan", Technical Reference PUB 60110, December, 1983.

The Synchronizer can also be equipped to operate at either the CEPT Toll or CEPT Local level in the hierarchy defined by the ITU-TSS. Any option can be configured to operate in a slave or master synchronization mode. In the master synchronization mode, DACS II can serve as a timing source for an isolated timing network without external timing links.

The Synchronizer supports three operational modes:

- Fast lock
- Normal
- Holdover.

The fast lock mode is used to quickly lock internal oscillators to an external reference frequency. The normal mode is active during typical operation, and the holdover mode is utilized when all external timing references are impaired. In the holdover mode, the Synchronizer maintains the output frequency at the last known good value of the external reference and is subject to the stability of the TB option specified.

Time Base Options

There are four time base stability options. Each option is provided by a different code of TB circuit pack.

Time Base Stratum 3 (TG60)

The Stratum 3 time base option provides an overall frequency stability of better than $\pm 1 \times 10^{-7}$/day over DACS II's operating temperature range and input voltage range.

Time Base CEPT Local (TG61)

The CEPT Local time base option provides an overall frequency stability of better than $\pm 1 \times 10^{-8}$/day over DACS II's operating temperature range and input voltage range.

Time Base CEPT Toll (TG62)

The CEPT Toll time base option provides an overall frequency stability of better than $\pm 2 \times 10^{-9}$/day over DACS II's operating temperature range and input voltage range.

Time Base Stratum 2 (TG63)

The Stratum 2 time base option provides an overall frequency stability of better than $\pm 1 \times 10^{-10}$/day over any 15˚C temperature interval in DACS II's operating temperature range and input voltage range.

Timing Input Options

There are six options for timing reference inputs. Each option is provided by a different code of TLI circuit pack.

Timing Extractor Bipolar 1544 kbit/s (TG64)

This circuit pack is compatible with the signal specifications for DSX-1 interconnection detailed in the following two standard documents:

- "Digital Hierarchy - Electrical Interfaces", ANSI T1.102-1987.
- "Interconnection Specifications for Digital Cross-Connects", Compatibility Bulletin 119.

Signal Characteristics

Number of Inputs: 2 per circuit pack
Frequency: 1544 kbit/s
Line Format: Bipolar, B8ZS
Framing Format: D4, ESF, T1DM
Level: 1.0 V peak to peak minimum
Acceptable Jitter: Bellcore TR-TSY-00009, Issue 1

Cable Characteristics

Type: twisted pair, balanced
Impedance: 100Ω resistive (2% tolerance).

Timing Extractor 2048 kbit/s Primary Block, 120Ω (TG65)

This circuit pack is compatible with ITU-T signal specifications for 2048 kbit/s Primary Block signals terminated at 120 ohms detailed in "Physical/Electrical

Characteristics of Hierarchical Digital Interfaces", ITU-T Blue Book, Recommendation G.703 Section 6, 1988.

Signal Characteristics

Number of Inputs: 2 per circuit pack
Frequency: 2048 kbit/s
Line Format: AMI, HDB3
Framing Format: CCS, ERSM, PCS0, PCS1
Level: 1.0 V peak to peak minimum
Acceptable Jitter: ITU-T, G.823 Table 2, 1989

Cable Characteristics

Type: twisted pair, balanced
Impedance: 120Ω resistive (2% tolerance).

Timing Extractor Composite Clock (TG66)

This circuit pack is compatible with the Composite Clock signal specifications described in Bellcore Document TA-TSY-000378 "Timing Signal Generator (TSG) Requirements and Objectives", April 1986, Section 5.1 part 11.

Signal Characteristics

Number of Inputs: 2 per circuit pack
Frequency: 64 kb/s
Format: DDS Composite Clock
Level: 3.8V to 6.6V peak to peak
Acceptable Jitter: less than 5 microseconds rms.

Cable Characteristics

Type: twisted pair, balanced
Impedance: 135Ω resistive (2% tolerance).

Timing Extractor Unipolar Clock (TG67)

This circuit pack terminates sinusoidal or square wave balanced clock signals.

Signal Characteristics

Number of Inputs: 2 per circuit pack
Frequency: 512 KHz, 1.0 MHz, 1.544 MHz, 2.048 MHz, 5.0 MHz
Format: Sinusoidal or square wave
Level: 0.3V to 3.0V peak to peak
Acceptable Jitter: less than 5 microseconds rms.

Cable Characteristics

Type: twisted pair, balanced
Impedance: 100Ω resistive (2% tolerance).

Timing Extractor BSRF Clock (TG68)

This circuit pack terminates a 2.048 MHz BSRF analog carrier signal or a 2048 kbit/s 2.048 MHz timing signal.

Signal Characteristics

Number of Inputs: 2 per circuit pack
Frequency: 2.048 MHz
Format: sine wave or square wave
Level: -20 dBm ± 6 dBm minimum
Acceptable Jitter: less than 5 microseconds rms.

Cable Characteristics

Type: coaxial cable, single ended
Impedance: 75Ω resistive (2% tolerance).

Timing Extractor 2048 kbit/s Primary Block, 75Ω (TG75)

This circuit pack is compatible with ITU-T signal specifications for 2048 kbit/s Primary Block signals terminated at 75 ohms detailed in "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", ITU-T Blue Book Fascicle III.4, Recommendation G.703, 1988.

Signal Characteristics

Number of Inputs: 2 per circuit pack
Frequency: 2048 kbit/s
Line Format: AMI, HDB3
Framing Format: CCS, ERSM, PCS0, PCS1
Level: 1.0 V peak to peak minimum
Acceptable Jitter: ITU-T, G.823 Table 2, 1989

Cable Characteristics

Type: coaxial cable, single ended
Impedance: 75Ω resistive (2% tolerance).

ITU-T Timing Extractor Composite Clock (TG97)

The TG97 circuit pack is compatible with the signal specifications for ITU-T Composite Clock, in accordance with ITU-T Fascicle III.4, Recommendation G.703, Section 1.2.2, Table 2.

Signal Characteristics

Number of Inputs: 2 per circuit pack
Frequency: 64 kb/s
Format: ITU-T Composite Clock
Level: 1.26V to 2.2V peak to peak
Acceptable Jitter: less than 5 microseconds rms.

Cable Characteristics

Type: twisted pair, balanced
Impedance: 110Ω resistive (2% tolerance), with return loss greater than 18 dB at 128 kHz.

Timing Output Options

This section describes the timing output options. Each option is provided by a different code of TLI circuit pack.

Timing Distributor 64 kb/s Composite Clock (TG70)

This circuit pack distributes four timing references that are compatible with the signal specifications for the DDS Composite Clock, in accordance with Lucent Technologies requirements.

Signal Characteristics

Number of Outputs: 4 per circuit pack
Frequency: 64 kb/s
Format: DDS Composite Clock
Level: 4.8 V peak to peak (nominal).

Cable Characteristics

Type: twisted pair
Impedance: 135Ω resistive (2% tolerance).

Note: The timing provided by a circuit pack may give different readings when measured by different test sets, if one test set provides errored blocks and another provides error-free transmission.

Timing Distributor 2.048 MHz Sine Wave Clock (TG71)

This circuit pack distributes four 2.048 MHz sine wave timing references in accordance with ITU-T specifications for 2.048 MHz synchronization interfaces detailed in "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", ITU-T Blue Book Fascicle III.4, Recommendation G.703, 1988.

Signal Characteristics

Number of Outputs: 4 per circuit pack
Frequency: 2.048 MHz
Format: Sine wave
Level: 2.2V peak to peak into 75Ω (nominal)
3.0V peak to peak into 120Ω (nominal).

Cable Characteristics

Type: coaxial or twisted pair
Impedance: Coaxial 75Ω resistive; twisted pair 120Ω resistive (2% tolerance in either case).

Pull-in Range

For any signal used to derive timing, the Synchronizer has a frequency lock range of ±9 ppm.

Jitter Tolerance

Input Jitter Tolerance

An external timing reference is considered impaired and is removed from service if the input jitter exceeds 5 microseconds rms.

DACS II meets the requirements for susceptibility to jitter on the incoming 1544 kbit/s signal in accordance with the Bellcore Technical Reference TR-TSY-000009, Issue 1, May 1986, "Asynchronous Digital Multiplexers Requirements and Objectives," and AT&T PUB 43802. Operation with larger jitter amplitudes may result in bit errors, reframes, and slips.

DACS II DS3 interfaces meet the requirements for transmitted jitter and received jitter accommodation in accordance with the Bellcore Technical Reference TR-TSY-000009, Issue 1, May 1986, "Asynchronous Digital Multiplexers Requirements and Objectives"; Section 4.6 and Figure 7.

DACS II is designed to operate error free when the 2048 kbit/s primary input signal contains jitter or wander within the bounds as specified in ITU-T Recommendation G.823; paragraph 3.1.1, Table 2/G.823.

Jitter Transfer

The DACS II Synchronizer meets the following three ITU-T requirements for jitter transfer from the timing reference signal to any output signals:

- "Timing Requirements at the Outputs of Slave Clocks Suitable for Plesiochronous Operation of International Digital Links", ITU-T Blue Book Fascicle III.5, Recommendation G.812, 1988.
- "The Control of Jitter and Wander within Digital Networks which are based on the 2048 (&1544) Kbit/s Hierarchy ", ITU-T Blue Book, Recommendations G.823 and G.824, 1988.

Output Jitter

DACS II has maximum jitter at the output port, with no jitter on the input signal, not exceeding 0.05 Unit Interval peak to peak, measured over a bandwidth of 20 - 100 KHz. The test methods specified by ITU-T Recommendation G.823 Section 4, were used. (One UI = 488.28 ns for a 2048 Kbit/s signal.)

Timing Reference Maintenance

Performance and failure monitoring capabilities depend on the type of timing references provided to the Synchronizer. All types of timing references are monitored for timing errors. Timing references containing framing are also monitored for framing errors. All in-service timing references, regardless of type, are simultaneously monitored unless otherwise noted.

DACS II provides the following performance/failure monitoring on timing references:

- Loss of Signal/Carrier Failure Alarm
- Out of Frame (on framed references only)
- Bit Error Rate (on framed references only)
- Excessive Jitter
- Phase Step (on active reference only)
- Frequency Offset (on active reference only).

The performance/failure monitoring algorithms are described below.

Loss of Signal/Carrier Failure Alarm (LOS/CFA)

The DACS II Synchronizer monitors all timing references for an LOS/CFA failure. The LOS/CFA failure is triggered differently for unframed and framed timing references. For unframed timing references, this failure corresponds to a loss of signal condition. The failure is triggered by the absence of input clock pulses for 8 milliseconds or more. For framed timing references (1544 kbit/s and 2048 kbit/s Primary Rate signals), this failure corresponds to a Carrier Failure Alarm. The Synchronizer asserts the CFA alarm based on the detection of out-of-frame events. The failure is triggered by either a continuous loss of framing for at least one second, or hit-integration of an intermittent but persistent framing failure. Note that reception of 1544 kbit/s Alarm Indication Signal (AIS) triggers the CFA failure.

Once the LOS/CFA alarm is asserted on a reference, the Synchronizer maintains the alarm and marks the reference unavailable for use until it receives no out-of-frames for 16 continuous seconds. This hysteresis prevents the Synchronizer from returning prematurely to an intermittently failing reference.

Out of Frame (OOF)

The DACS II Synchronizer continuously monitors framed timing references for OOF events. Before any phase sample is input into the phase-locked loop, the microprocessor determines if either a framing error or OOF event occurred since

the last phase sample. If so, the phase sample is discarded to isolate the DACS II Synchronizer's output timing from bad input data.

As described previously, OOF event information is integrated off-line to determine whether a Carrier Failure Alarm is present on the reference. Isolated OOF events by themselves will not cause a reference switch by the DACS II Synchronizer. However, there is a correlation between OOF events on a reference and its Bit Error Rate, described below, which is used in the reference selection algorithm.

Bit Error Rate (BER)

The DACS II Synchronizer continuously monitors framed timing references for framing error events. Framing error information is digitally filtered to compute a Bit Error Rate for each framed timing reference. The DACS II Synchronizer determines whether the BER has exceeded a major threshold, internally set at a 10^{-3} rate, a minor threshold, internally set at a 10^{-6} rate, or neither the major nor minor threshold. This information is used by the DACS II Synchronizer to fine tune its selection of the best performing available timing reference as its input source.

Excessive Jitter

The DACS II Synchronizer monitors all timing references for excessive jitter. The Synchronizer continuously runs a variance calculation on the phase samples from each timing reference and sets the excessive jitter alarm if the jitter on a reference exceeds 5 microseconds rms. Once the excessive jitter alarm is asserted, the Synchronizer will maintain the alarm and mark the reference unavailable for use until the measured jitter remains below the threshold for 16 continuous seconds. This hysteresis prevents the Synchronizer from returning prematurely to an intermittently failing reference.

Phase Step

The DACS II Synchronizer monitors the active timing reference for phase steps. The Synchronizer checks every phase sample for a step in phase beyond an internally programmed threshold. If the phase sample is determined to be a phase step, it is discarded to isolate the loop's output timing from bad input data. Phase step information is also input into the jitter monitoring algorithm to determine whether excessive jitter is present on the reference.

Frequency Offset

The DACS II Synchronizer monitors the active timing reference for frequency offset and in conjunction with the DACS II Main Controller, autonomously

removes a timing reference from service, raising a frame alarm, if the offset exceeds 9 parts per million from nominal.

Timing Reference Selection

In the slave synchronization configuration, the Synchronizer employs a reference switching algorithm that always chooses the best performing available timing reference. If no references meet its minimum acceptable standards, the Synchronizer remains in holdover during the outage plus hysteresis period.

Only one reference (out of a maximum of eight) is selected to derive timing. Reference selection is in accordance with a user provisioned reference priority in conjunction with the timing reference service state (in/out of service) and error status.

Of all the available timing references, the Synchronizer selects the highest priority reference for which no error conditions that affect timing have been detected. The error conditions that make a reference unacceptable are LOS/CFA, Excessive Jitter, and Frequency Offset. Among any references without these failures, the Synchronizer then fine tunes its determination of the healthiest references by preferring those with no BER threshold crossing over those with a 10^{-6} threshold crossing. References with either of those BERs are preferred over those with a 10^{-3} BER. If multiple non-failed links have equivalent BER performance levels, then the user-provisioned source priority is used to select the active reference.

It is possible to manually override the automatic reference selection mechanism by modifying the reference priority and/or the reference service state.

All reference selection and switching are hitless and do not cause perturbation of any internal or external timing signals.

Timing Generation Maintenance

In addition to providing performance/failure monitoring for the timing references, the DACS II Synchronizer monitors the timing generation and phase-locked loop operation by detecting the following alarms:

- Synchronizer End of Control Range (EOR) - This alarm is raised when the Synchronizer exceeds 3/4 of its frequency control range in order to lock the DPLL to the active timing reference.
- Synchronizer Phase Alignment Error - This alarm is raised when a phase offset of greater than 125 microseconds exists between the DPLL and the active timing reference.

- Frequency Accuracy Error - This alarm applies only to the master synchronization mode in which DACS II serves as a timing source for an isolated timing network without external timing links. This alarm is set when the Synchronizer output clocks reach the frequency accuracy limits of the operational stratum.

Error Recovery and Protection Switching

Each Synchronizer (DPLL, TB, SPU) comprises a single failure group. A failure of any one of the circuit packs within the active Synchronizer (the Synchronizer that is currently supplying timing information to the facility terminating units in the DACS II frame) will result in switching to the duplicate Synchronizer and removal of the failed Synchronizer from service. In the event that the duplicate Synchronizer is already out of service and the active Synchronizer fails, a switch will not be executed.

Each timing reference input is an independent failure group. Timing reference inputs are also independent of Synchronizer (DPLL, TB, SPU) failure groups. Error recovery for the timing references is performed entirely by each Synchronizer through the use of internal error monitors in combination with a user programmable priority scheme. In the event that all timing references fail, the Synchronizer will enter the holdover mode. If the duplicate Synchronizer has a good timing reference available, then a switch to the duplicate Synchronizer will be executed.

Transmission Characteristics

3

Contents

Contents

Transmission Characteristics

3

Overview

The DACS II interfaces with digital transmission facilities at the 1544 kbit/s, 2048 kbit/s primary block, and DS3 (44.736 Mbit/s) levels.

1544 kbit/s Interface

Interface Characteristics

The DACS II 1544 kbit/s interface has a nominal termination impedance of 100Ω. The 1544 kbit/s signal meets the requirements specified in ITU-T Recommendation G.703 and ANSI T1.102-1987 entitled "Digital Hierarchy - Electrical Interfaces" for signals interfacing at the DSX-1 cross-connect frame. The signal characteristics and cable characteristics are:

Signal Characteristics

Number of Inputs: 2 per circuit pack
Frequency: 1544 kbit/s
Line Format: Bipolar, B8ZS
Framing Format: D4, ESF, T1DM
Receive Level: 1.0 V minimum
Acceptable Jitter: Bellcore TR-TSY-00009, Issue 1

Cable Characteristics

Type: twisted pair, balanced
Impedance: 100Ω resistive (2% tolerance).

Two cable types are recommended for the 1544 kbit/s facilities:

- Lucent Technologies 1249C

  This cable type provides 20 twisted pairs and meets the requirements with up to 450 feet between the DACS II frame and the DSX-1.

- Lucent Technologies 609C (ABAM)

  This cable type provides 25 twisted pairs in a fire-retardant, shielded cable and meets the requirements with up to 655 feet between the DACS II frame and the DSX-1.

Transmit and receive signals of the 1544 kbit/s interface are carried in separate cables. Five programmable equalizer settings are provided to maintain the pulse shape and amplitude within the template specified in Lucent Technologies Compatibility Bulletin CB 119 over the full range of cabling distance.

DACS II Enclosed frames meet European Norms (EN) 55 022 by having an adapter panel for each module, with individual cable connectors, of type BT43 or IEC169-13 1.6/5.6. These panels are required for connection with 75Ω coaxial cables. The maximum allowable cable diameter is 5.2mm (0.20''). The minimum center-to-center distance between connectors is 22.2mm (0.875'').

1544 kbit/s Framing Mode

DACS II supports the following 1544 kbit/s framing modes:

- D4 Superframe (SF): in accordance with AT&T PUB 43801, "Digital Channel Bank Requirements and Objectives."
- Extended Superframe (ESF): in accordance with Bellcore Technical Reference TR-TSY-000194, Extended Superframe Format, Issue 1, December 1987 and Lucent Technologies Compatibility Bulletin 142 (CB 142), "Extended Framing Format Interface Specification."
- DDS T1 Data Multiplexer (T1DM): in accordance with Bellcore Technical Advisory TA-TSY-000278, "Digital Data System (DDS) T1 Data Multiplexer (T1DM) Requirements," Issue 1, October 1985 and Bell System Technical Journal (BSTJ) Vol. 54 No. 5 May/June 1975, pages 893 - 918, "Digital Data System Digital Multiplexers."
- SLC® 96 Carrier Framing Format: in accordance with Bellcore Technical Reference TR-TSY-000008, "Digital Interface Between The SLC® 96 Digital Loop Carrier System And A Local Digital Switch," Issue 2, August 1987.
- Transparent: 1544 kbit/s signal with and without framing pattern.

1544 kbit/s Reframe Time

DACS II meets the 50 ms maximum average reframe time requirement for 1544 kbit/s facilities specified in Bellcore TR-TSY-000170. The reframe time is dependent upon framing formats, as follows:

- D4 SF: 9 milliseconds
- ESF: 12 milliseconds
- T1DM: 2 milliseconds
- SLC 96 Carrier: 9 milliseconds.

1544 kbit/s False Framing Immunity and Rejection

For false framing immunity at the 1544 kbit/s level, DACS II equipment utilizes the 193rd bit Fs+Ft framing pattern, and the in-frame condition is declared only when one unique pattern is identified.

The possibility of false framing pattern propagation is suppressed in DACS II equipment by overwriting signaling bit positions.

1544 kbit/s Facility Out-of-Frame (OOF) Detection Limits

The 1544 kbit/s facility OOF detection limits are mode dependent and are listed below:

- D4 SF and T1DM framing modes: 2 out of 4 framing bits in error
- ESF framing mode: 2 out of 4 framing bits in error or, if the facility is already out-of-frame, 32 out of 33 CRC-6 check bit errors.

1544 kbit/s Line Coding

DACS II supports the following 1544 kbit/s line codes:

- Alternate Mark Inversion (AMI) Bipolar with Zero Code Suppression (ZCS)
- Alternate Mark Inversion (AMI) Bipolar with no Zero Code Suppression (NZCS)
- Bipolar with 8 Zero Substitution (B8ZS)
- Zero Byte Time Slot Interchange (ZBTSI).

1544 kbit/s Channel Sequencing Formats

DACS II provides 1544 kbit/s transmission interfaces having the following channel numbering formats in accordance with AT&T PUB 43801:

- D1D
- D2
- D4.

1544 kbit/s Signaling Characteristics

DACS II supports the following per channel signaling modes for 1544 kbit/s facilities:

- Robbed bit: The signaling bits are transmitted in the least significant bit of the data channel every sixth frame. The signaling frames and bits are identified by a superframe sequence (12 frames for the D4 mode; 24 frames for the ESF mode) in the 193rd bit.
- Digital Multiplexed Interface-Bit Oriented Signaling (DMI-BOS): It provides a signaling channel (in channel 24) without robbing bits from the data channel. The signaling bits are identified by a superframe sequence in channel 24.
- Transparent: No signaling bits are associated with the channel.

Signaling Formats

DACS II supports the following DS0 signaling formats:

- 2-state signaling
- 4-state signaling
- 16-state signaling
- Transparent Signaling.

The application of the signaling formats is framing mode dependent, as follows:

- The 2-state and 4-state signaling and transparency are applicable for either the D4 SF or ESF framing mode.
- The 16-state signaling is only applicable for the ESF framing mode signals.

Signaling Fixing

For DS0 channels provisioned with the robbed bit signaling mode, DACS II performs the following signaling fixing features:

- For 4-state signaling, if both A and B signaling bits are not equal (that is, 01 or 10), on a cross-connection with signaling, DACS II forces the least significant bit of the outgoing channel to 1 in a signaling frame when the incoming channel was in a signaling frame.
- For 16-state signaling, the least significant bit of a signaling frame is forced to 1 if A,B,C, and D signaling bits are not equal (that is, 0001,0010,.....,1110), if the incoming channel was in a signaling frame.

This algorithm prevents generation of false framing patterns when a circuit traverses multiple DACSs.

Signaling Freeze

DACS II enters the signaling freeze state when one of the following conditions occurs:

- An out of frame (OOF)
- A single framing bit error, or
- In the D4 with DMI-BOS mode when 2 frames contain remote frame alarm (RFA) - yellow alarm.

The signaling freeze is done by maintaining the signaling state that existed before the detection of the failure condition. The signaling freeze state is released when the above conditions are removed and two superframes have passed or when a Carrier Failure Alarm (CFA) is entered.

Signal Distortion

DACS II does not insert any envelope distortion in the line signal. The only noise contribution is associated with robbed bit signaling and the lack of superframe alignment.

1544 kbit/s Programmable Signaling Insertion Modes

DACS II supports the following per channel signaling output insertion modes for 1544 kbit/s facilities:

- Pass-through (transparent)
- Robbed bit signaling.
- Alternate Message Store (AMS): A predefined (per-channel programmable) 8-bit word is inserted when the circuit is not provisioned or, in the event of a facility or equipment failure, when the circuit is provisioned.
- 1544 kbit/s level alarm code outputs (yellow alarm, AIS).

64 kbit/s Channel Capability

The DACS II supports DS0 or 64 kb/s channel capability for the following modes:

- B8ZS provides a 64 kb/s clear data channel. If signaling is required, it can be either robbed bit or DMI-BOS.
- No Zero Code Suppression (NZCS) prevents the normal overwriting of the second least significant bit (bit 7) of an all-zero word. This requires the source of the 64 kbit/s or 1544 kbit/s signal to ensure that 1544 kbit/s pulse density requirements are met. This option is normally used when DACS II provides cross-connection of 1544 kbit/s (24 channel) services such as digitally encoded video signals for teleconferencing. If signaling is required, it can be either robbed bit or DMI-BOS.
- Zero Byte Time Slot Interchange (ZBTSI) provides ZCS by using the ESF data link to pass address information when the ones density constraint (no more than 15 consecutive zeros) is violated.

These options are selected on a per-1544 kbit/s basis as part of the DACS II equipment provisioning commands.

Clear-1544 kbit/s Capability

The DACS II supports clear-1544 kbit/s cross-connect and test-access capabilities. The non-channelized 1544 kbit/s signal can be framed or unframed, selectable on a per-1544 kbit/s signal basis using DACS II facility provisioning commands. Performance monitoring is enabled for a framed clear 1544 kbit/s signal, only limited PM is done for unframed clear 1544 kbit/s signal.

2048 kbit/s Interface

Interface Characteristics

The DACS II 2048 kbit/s primary block interface has a nominal termination impedance of 100/120Ω or 75Ω. The 2048 kbit/s primary block signal meets the pulse shape and amplitude requirements specified in ITU-T Blue Book, Recommendation G.703, Interface at 2048 kb/s.

For the 2048 kbit/s interface, DACS II provides the same connector/adaptor panels as those for 1544 kbit/s interface, to which customer cables can be attached. The same cable types for the 1544 kbit/s facilities are recommended for the 2048 kbit/s primary block facilities. Transmit and receive signals should be carried in separate cables.

The signal characteristics are:

Number of Inputs: 2 per circuit pack
Frequency: 2048 kbit/s
Line Format: HDB3
Framing Format: ITU-T Recommendation G.704
Level: 2.37 V for 75Ω resistive and 3 V for 120Ω resistive
Acceptable Jitter: ITU-T, G.823 Table 2, 1989

The cable characteristics for 120Ω are:

Type: twisted pair, balanced
Impedance: 120Ω resistive (2% tolerance).

The cable characteristics for 75Ω are:

Type: coaxial cable, single ended
Impedance: 75Ω resistive (2% tolerance).

2048 kbit/s Primary Block Framing Mode

DACS II supports the basic frame structure at 2048 kbit/s in accordance with the following:

- "Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels", ITU-T Recommendation G.704, 1991.
- "Frame Alignment and CRC Procedures Relating to Basic Frame Structures Defined in Recommendation G.704", ITU-T Recommendation G.706, 1991.

2048 kbit/s Primary Block Reframe Time

DACS II conforms to the ITU-T Recommendation G.706 Frame Alignment Recovery Strategy.

2048 kbit/s Primary Block False Framing

For 2048 kbit/s primary block facilities, the TS0 frame is used to maintain in-frame conditions.

2048 kbit/s Primary Block Facility Out-of-Frame (OOF) Detection Limits

The 2048 kbit/s primary block OOF detection limits are three consecutive errored 7-bit framing patterns (that is, 7 bits of TS0 frame word) or three consecutive bit 2 errors of the Non Frame Word (NFW).

2048 kbit/s Line Coding

DACS II supports the High Density Bipolar of order 3 (HDB3) 2048 kbit/s primary block line code.

2048 kbit/s Primary Block Channel Sequencing Formats

DACS II also meets the telephone channel numbering and time slot channel numbering as specified in ITU-T standards for cross-connecting time slots between 2048 kbit/s primary blocks.

2048 kbit/s Signaling Characteristics

DACS II supports two multiframe and signaling formats for 2048 kbit/s primary block facilities:

- Nonsignaling Associated (NSA) format

  With this format, DACS II does not process signaling; that is, it is transparent to signaling, but can carry signaling formats such as Common Channel Signaling (CCS), in-band signaling, or data channel with no signaling.

- Channel Associated Signaling (CAS)

  With this format, Time Slot 16 (TS16) of the 2048 kbit/s primary block facility is used to carry channel associated signaling information as specified in ITU-T Recommendation G.704.

Signaling Formats

DACS II supports the following DS0 signaling formats:

- 2-state signaling
- 4-state signaling
- 16-state signaling
- Transparent Signaling.

When either 2-state or 4-state signaling is applied, the unused signaling bits can be set at fixed values.

Signaling Freeze

DACS II enters the signaling freeze state when one of the following conditions occurs:

- An out of frame (OOF)
- A single framing bit error.

The signaling freeze is done by maintaining the signaling state that existed before the detection of the failure condition. The signaling freeze state is released when the above conditions are removed and two superframes have passed or when a Carrier Failure Alarm (CFA) is entered.

Signal Distortion

DACS II does not insert any envelope distortion in the line signal.

2048 kbit/s Programmable Signaling Insertion Modes

DACS II supports the following per channel signaling output insertion modes for 2048 kbit/s primary block facilities:

- AMS: A predefined (per-channel programmable) 8-bit word is inserted when the circuit is not provisioned or, in the event of a facility or equipment failure, when the circuit is provisioned.
- 2048 kbit/s primary block facility alarm code outputs [Remote Alarm Indication (RAI)].

Clear 2048 kbit/s Capability

The DACS II also supports cross connection and test access of clear 2048 kbit/s signals. The non-channelized 2048 kbit/s signal can be framed or unframed, selectable on a per-facility basis. Performance monitoring is enabled for a framed clear 2048 kbit/s signal, only limited PM is done for unframed clear 2048 kbit/s signals.

DS3 Interface

The DACS II frame can have up to 16 DS3 units depending on the individual frame configuration, each DS3U terminates 6 asynchronous DS3 signals. These DS3 signals are demultiplexed into 28 DS1s and eventually formatted further into 4032 DS0 channels to be cross-connected through the ECCN. In the outgoing transmission direction 28 DS1 signals are multiplexed into a DS3 signal in two steps. First, four DS1 signals are multiplexed into a DS2 signal in an M12 stage. Seven DS2 signals are then multiplexed to one DS3 in an M23 stage.

With the Hybrid DS3 unit, the DACS II frame may terminate DS3 signals embedded with a mixture of 1544 Kbit/s and 2048 Kbit/s signals. The DS3 signal is demultiplexed into 7 DS2s. Each DS2 consists of either four 1544 Kbit/s or three 2048 Kbit/s signals, which are further formatted into 4032 DS0 channels to

be cross-connected through the ECCN. In the outgoing transmission direction, the DS0 channels can be multiplexed into 1544 Kbit/s or 2048 Kbit/s signals, which are multiplexed into DS2s. And then, seven DS2s are multiplexed into a DS3 signal to be transmitted.

Interface Characteristics

The DACS II DS3 interface has a nominal termination impedance of 75Ω. The DS3 signal meets the pulse shape and amplitude requirements specified in the ANSI T1.102-1987 standard for electrical interfaces in the digital hierarchy and is DSX-3 compatible.

The recommended cable type for DS3 facilities is Lucent Technologies 734A coaxial cable or equivalent which meets the requirements with up to 450 feet between the DACS II frame and the DSX-3.

Transmit and receive signals of the DS3 interface are carried in separate cables. In the transmit direction, a programmable Line Build Out (LBO) setting, per DS3, is provided to maintain the pulse shape and amplitude within the template specified in T1.102-1987 over the full range of cabling distance.

DS3 Framing Modes

DACS II supports the following DS3 framing modes (except that the Hybrid DS3 does not support C-Bit Parity):

- M13: as per Bellcore Technical Reference TR-TSY-000009, "Asynchronous Digital Multiplexers Requirements and Objectives", Issue 1, May 1986.
- C-Bit Parity: as defined in "DS3 C-Bit Parity Format Path and Idle Signal Identification Features - Lucent Technologies NOG Requirements for DS3 NTE, DACS III, and the DS3 Performance Monitor", V.T. Tatulis, August 31, 1987.

DS3 Reframe Time

DACS II meets the DS3 facility reframe time requirements specified in Bellcore TR-TSY-000009.

DS3 False Framing Immunity and Rejection

For DS3 circuits, the framing and multiframe alignment bits (F-bits and M-bits, respectively) are used to maintain in-frame conditions.

DS3 Facility Out-of-Frame (OOF) Detection Limits

The DS3 facility OOF detection limits are 3 out of 16 consecutive F-bits in error, or 2 mismatches in the M-bits of 4 consecutive frames.

DS3 Line Coding

DACS II supports the Bipolar with 3 Zero Substitution (B3ZS) DS3 line code

Internal Transmission Characteristics

Loss and Delay Distortion

The DACS II equipment does not introduce any delay distortion in the transmission path. There is programmable gain and loss associated with the DMB function (see DMB details in Section 4).

Blocking

DACS II is a fully nonblocking cross-connect system. That is, it allows absolute connectivity through the system.

Transmission Delay

Table 3-1 specifies the absolute delay introduced by DACS II for a 64 kbit/s channel passing through a DACS II system. DACS II meets Bellcore TR-TSY-000170 requirements with all maximum delay points less than 0.7 ms, except for the case where special processing such as ZBTSI or DSP is required.

Table 3-1. Absolute Transmission Delay Through DACS II

CONDITION	DELAY (microseconds)			
	DS1+ECCN Processing	DS1+ZBTSI+ECCN Processing	DS1+DSPC+ECCN Processing	DS3+DS1+ECCN Processing
Minimum	40	560	293	41
Maximum	544	1064	797	545
Nominal	293	813	546	294

The 1544 kbit/s and Expanded Cross-Connect Network (ECCN) processing delay include:

- 1544 kbit/s line phase uncertainty relative to the internally (DACS II) defined reference.
- Transport and processing delay through the 1544 kbit/s termination ports and the cross-connect network.
- Channel rearrangement delay.

The values used for the Digital Signal Processing Circuit (DSPC) assumes that the signal only passes through the DSPC once.

DS0 Errors

The DACS II introduces no errors on signals cross-connected through it and provides virtually error-free; that is, less than one error in 10^{10} bits, transmission of DS0 signals across the system. The only exception is circuits using robbed bit signaling in which, due to the nature of the robbed bit signaling, the least significant bit is overwritten with signaling information every sixth frame.

Digital Signal Processing

4

Contents

Digital Signal Processing

4

Overview

Each DACS II Digital Signal Processing Unit (DSPU) provides signal processing functions for a maximum of 4,096 DS0 (64 kbit/s) channels. The DSPU interfaces to the ECCN and Main Controller (MC). In this configuration, specific channels that require digital signal processing are terminated by the FTU/IFTU or DS3U and then cross-connected by the ECCN to the DSPU. Conversely, the processed channels from the DSPU are sent to the ECCN for cross-connection to the appropriate outgoing facilities.

The total number of DS0 channels that can be processed on a DACS II frame depends on how many DSPUs are equipped on the frame. Each DSPU has capacity for eight duplicated (total of 16 circuit pack equipment locations) general purpose Digital Signal Processing Circuits (DSPCs). Each DSPC can process a maximum of 512 DS0 channels, resulting in 4,096 DS0 channels per DSPU.

The DSPU is partitioned into three basic functions:

- Signal processing
- Control interface
- Power.

The signal processing section has capacity to support a maximum of eight duplicated DSPCs. The control section contains two simplex (nonduplicated) circuit packs: the Central Processor Unit (CPU) and the Digital Signal Processing Interface (DSPI). The CPU pack (TM657 or TM657B) serves as the DSPU controller, and the DSPI pack supports communication between the CPU and the DSPCs. The power section consists of three power converters and a fuse board. There is a separate power converter for each duplicate group of

eight DSPCs (0DSPC 1-8, and 1DSPC 1-8) and a single power converter for the CPU and DSPI.

Digital Multipoint Bridge (DMB) TM665

The Digital Multipoint Bridge (DMB) circuit pack has the capacity to process a maximum of 512 PCM DS0 channels and is used when establishing symmetrical (voice) and multipoint (data) conferences. Level adjustment, noise guard, and return loss enhancement (Echo Suppression) digital signal processing functions are provided on a per-DS0-channel basis. Since each DMB processes a maximum of 512 channels, the DMB function is expandable in increments of 512 channels, and the maximum capacity for each DSPU is 4,096 channels.

Receive Level Adjust

Each channel data signal is level adjusted as specified in control memory within the range of +8.8 to -9.0 dB in 0.2 dB increments.

Conferencer

Conferencing is available for voice, voiceband data, and broadcast modes. Only voice mode symmetrical and multipoint data conferences are performed in the DMB. Broadcast functions are performed in the ECCN.

Transmit Coarse Level Adjustment

Transmit channel data received from the Conferencer is level adjusted. The level adjustment is "coarse" and is done in 6-dB increments within the range of +6 to -6 dB.

Transmit Fine Level Adjustment

The coarse level adjusted signal is fine level adjusted over a range of +2.8 to -3.0 dB, in 0.2-dB increments. The combination of coarse level adjustment and fine level adjustment provides a composite adjustment range of -9.0 dB to +8.8 dB in 0.2-dB increments.

Return Loss Magnitude Compare Function

The Return Loss Magnitude Compare function determines whether the receive side conferencer signal is of greater absolute magnitude than the transmit side. This activity is performed on a per-channel basis.

Return Loss and Noise Guard

The Return Loss characteristics are as follows:

- Maximum attack time (change from -18.0 to 0.0 dB) is 5.75 ms; loss is removed all at once.
- Maximum holdover time (change from 0.0 to -18.0 dB) is 69.5 ms; loss is inserted at a rate of one 6-dB step per 2-ms interval during the last 6 ms of the holdover time.
- Sensitivity is -42 dBm0. Signal levels below this threshold are ignored. Receive and transmit signal levels having a minimum difference of 1 dBm0 can be resolved.

The Noise Guard characteristics are as follows:

- Maximum attack time (change from -18.0 to 0.0 dB) is 2.75 ms; loss is removed all at once.
- Maximum holdover time (change from 0.0 to -18.0 dB) is 10.625 ms; loss is inserted at a rate of one 6-dB step per 125 microseconds during the last 375 microseconds of the holdover time.
- Sensitivity is -42 dBm0. Signal levels below this threshold are attenuated, and signal levels above this threshold are passed without attenuation.

Both the Return Loss and Noise Guard functions have flat response in the voice band for either the loss or no-loss modes. Each channel in the DMB can be provisioned with separate maximum attenuation values for the Noise Guard and Return Loss functions. A value of zero specified for Noise Guard or Return Loss will disable that function for the respective channel.

DMB Configurations

The DMB configurations and capabilities are summarized in Table 4-1.

Table 4-1. DACS II Digital Multipoint Bridge Capacity

NUMBER OF DMBs EQUIPPED	DS0 CHANNEL CAPACITY	MAX. NUMBER OF 3-LEG CONFERENCES
1	512	170
2	1,024	340
3	1,536	510
4	2,048	680
5	2,560	850
6	3,072	1,020
7	3,584	1,190
8	4,096	1,360

2048 kbit/s C-Bit Processor (TM747)

The C-Bit Processor (CPR) TM747 can concurrently monitor state changes and source repetitive data sequences in the "C" signaling bits of all channels in up to 128 2048 kbit/s primary circuits. Monitoring and sourcing of C-Bits are provisioned on a per-channel basis. With monitoring enabled on a channel, C-Bit state changes are reported to the administrative links; when monitoring is disabled, state changes for the channel are not reported. With modification enabled on a channel, C-Bit output data is generated by the CPR (according to a provisioned data sequence). When modification is disabled on a channel, C-Bit data may be cross-connected through the DACS II.

Monitoring

Reports are generated for monitored channels whose C-bits transition to Idle (all zeros), C-Bit Pattern (framed bit sequence), or Network Alarm (error) states. A C-Bit pattern sequence is a repetitive 14-bit data sequence with an alternating, logic "1" and "0", 15th framing bit. Separate Network Alarm timers, with a common timeout threshold, are maintained for each monitored channel. When a channel has been in an errored state for longer than the timeout threshold, a Network Alarm is reported for that channel. Errored state is defined as a channel whose 2048 kbit/s primary is correctly receiving a multiframe alignment signal, has monitoring enabled, and has either of the following conditions in its C-Bit:

- Neither Idle nor Framed Pattern states, or
- Both Idle and Framed Pattern states.

The Network Alarm threshold can be provisioned on a CPR basis to one of the ranges shown in Table 4-2.

Table 4-2. DACS II CPR Network Alarm Ranges

OPTION	MINIMUM	MAXIMUM
1	600 ms	750 ms
2	1.5 sec	1.65 sec
3	2.4 sec	2.55 sec
4	4.65 sec	4.8 sec

The CPR stops monitoring C-Bits on channels in any 2048 kbit/s primary that has lost multiframe signaling alignment and resumes again after multiframe alignment has been reestablished. Multiframe alignment detection and loss algorithms comply with ITU-T Recommendation G.732, 1988.

Modification

The CPR can generate any repetitive 14-bit data sequence, with 15th framing bit (alternating logic "0" and "1"), for up to 30 channels in each of up to 128 2048 kbit/s primaries. The 14-bit data sequence can be provisioned independently for each channel.

C-Bit Processing Capacity

CPRs must be equipped as duplex pairs, with each pair processing up to 128 2048 kbit/s primaries and up to 30 channels per primary. Table 4-3 shows how C-Bit processing capacity can be increased by equipping additional CPR pairs.

Table 4-3. DACS II C-Bit Processing Capacity

NUMBER OF DUPLEX CPR PAIRS	MAX. NO. OF 2048 kbit/s PRIMARIES WITH C-BIT PROCESSING*	MAX. NO. OF CHANNELS WITH C-BIT PROCESSING*
1	128	3,840
2	256	7,680
3	384	11,520
4	512	15,360
5	640	19,200
6	768	23,040
7	896	26,880
8	1024	30,720

* Processing includes monitoring and/or sourcing C-Bits.

C-Bit Message Filter

This filter would require that a new C-bit state would be stable for a given number of seconds prior to reporting that state. The filter mechanism is a timer which can be set in one second increments from zero to ten seconds. If a change of state is to be reported, the timer is started. When the timer expires, the new state will be reported. If the state changes again before the timer expires, the timer will be restarted. If the timer is set to zero, filtering will be done by the hardware timer.

Each channel (time slot) has a separate timer but the timeout value for a single NPC applies to all the channels served by that NPC. When the NPC is provisioned, the timeout value will be set to the default value of 10 seconds. The timeout value can be changed to a value from zero to 10 in one second increments.

The state change timer is in addition to the alarm state timer on the CPR circuit. The timer value specified represents the total time for alarm state changes. Therefore, the timing done in the hardware, 600 ms - 4.8 seconds, must be considered as part of the specified timer. For network alarm states, the software will time for the difference between the hardware timer and the specified timer. If the specified value is less than that provisioned on the hardware, alarm state changes will still be timed on the hardware for the provisioned amount of time and will not be reported any sooner.

Remote Power Supply Failure Indication (RPSFI)

The RPSFI feature uses the C-bit modification capability to inform outgoing channels cross-connected to the channels of an incoming facility that declared a remote power supply failure situation.

Certain MUX equipment when it looses power will change bit 6 of the NFW from "1" to "0" until it looses the signal. When the DACS II detects that TS0 bit 6 of NFW changes from "1" to "0", it will interpret this transition as a RPSFI condition. When the RPSFI condition is detected on a facility, an alarm will be generated and the system will inhibit notification of facility alarms (including AIS, LOF, and LOS) and stop incrementing the performance monitoring counters on that facility. The consequent action of these facility alarms is not affected. In addition, the system will look at all NPCs with downstream channels cross connected to channels of the incoming RPSFI facility. For those NPCs that have C-bit indication enabled (TS16 cross connected to a CPR circuit pack), the DACS II will activate C-bit modification with bit 12 set to "0". IF C-bit modification is already activated on a particular downstream timeslot when the RPSFI condition is declared, the setting bit 12 to a "0" for RPSFI takes precedence over the current value being signalled. If C-bit modification is not activated on the downstream timeslot when the RPSFI condition is declared, it will be activated by the system with bit 12 set to "0" and default values for all other C-bits. If while in

the RPSFI condition, the operator requests that C-bit be activated, the operator C-bit moification value specified will be sent except bit 12 will stay "0". If the operator requests C-bit modification be de-activated while the RPSFI condition is being signalled, bit 12 will be set to "0" and the default values will be sent for all the other C-bits.

Subrate Multiplexer Circuit Pack (TM739)

The SRM circuit pack provides standard digital data subrate multiplexing of 2.4, 4.8, and 9.6 kb/s DS0A formatted signals and dataport error correction. It also provides three types of subrate multiplexers for DS0B channels which serve five, ten, or twenty subrate channels. Each SRM has the capacity to process a maximum of 512 DS0A or DS0B channels. Various rate multiplexers can be supported simultaneously within an SRM. Five-channel multiplexers use six timeslots (one DS0B and five DS0A); 10-channel multiplexers use eleven timeslots (one DS0B and ten DS0A), and 20-channel multiplexers use twenty-one timeslots (one DS0B and twenty DS0A).

Any subrate channel interfacing the SRM pack can have dataport subrate error correction performed on it as an independent function or in combination with multiplexer processing. Similarly, 56 kb/s DS0A channels can interface the pack and have parity channel error correction performed as an independent function. This function can also be performed on the DS0B channel associated with any multiplexer.

Multipoint Junction Unit Circuit Pack (TM740)

The MJU circuit pack provides standard digital data multipoint bridging of subrate and 56 kb/s DS0A formatted signals, and dataport error correction. Each MJU pack has the capacity to support a maximum of 512 DS0A channels for the MJU function. Each MJU function has one control channel and four branch channels. Therefore, each MJU pack supports a maximum of 102 multipoint circuits. Multipoint circuits requiring more than four branches are formed by cascading MJU branch channels to the control channels of additional MJUs. The MJUs operate at 2.4, 4.8, 9.6, or 56 kb/s and perform the signal processing necessary for the secondary channel capability.

As with the SRM pack, channels interfacing the MJU pack can have subrate or parity channel dataport error correction performed on them as an independent function or as part of the MJU processing.

Office Alarms

5

Contents

Office Alarms

5

Overview

The DACS II equipment provides relay contact closures for interfacing with the central office alarm grid. The DACS II status panel is equipped with alarm indicators and an alarm cutoff (ACO) switch. The ACO switch is provided to silence local audible alarms. The ACO function can also be activated/deactivated from a local or remote terminal by entering the ACO command.

The classification (levels) and types of alarms are described in the sections below.

Alarm Classification

DACS II provides four classifications (levels) of alarms. These have the following general definitions:

- Minor Alarm (Deferred Maintenance Alarm; that is, DMA, in 2048 kbit/s application)

  Any non-service-affecting failure, the failure of at least one but not all synchronization ports, or minor facility alarm

- Major Alarm (Prompt Maintenance Alarm Major; that is, PMA Major, in 2048 kbit/s application)

  Any failure affecting five or fewer 1544 kbit/s/2048 kbit/s Primary Block facilities, the failure of all synchronization ports, a non-service-affecting failure of duplex/protected equipment, a power failure, a Main Controller

(MC) failure, or a Unit Controller (UC) failure

- Critical Alarm (PMA Critical in 2048 kbit/s application)

  Any failure affecting more than five 1544 kbit/s/2048 kbit/s Primary Block facilities, more than five major alarms (combination of equipment and facility alarms) in facility terminating NPCs, failures on both sides of the cross-connect network, or failures of both service and protection entities.

In addition, DACS II provides the Maintenance Information (MI) for the 2048 kbit/s application. The MI is a condition resulting when only informational messages need to be sent over the DACS II administrative links and DACS II alarms are not indicated.

Alarm Types

DACS II provides contact closures for the following:

- Local Visual alarms: critical, major, processor major, and minor
- Local Audible alarms: critical, major, and minor
- Remote Alarms: critical, major, processor major, and minor.

The remote frame identification code (remote ID) is activated when any remote alarm is invoked. A "remote only" alarm mode can be set by software commands and results in the generation of only remote alarms (local visual and audible alarms are suppressed) until the "remote only" mode is released by entry of another software command.

Alarm Interface Parameters

All central office alarm relay contact closures are rated as follows:

- Maximum instantaneous and steady state current: 1.0 ampere
- Maximum voltage: 60 V
- Maximum volt-ampere rating: 25 VA
- Transient noise suppression devices (diodes, networks, or other devices) must be used to protect terminations from inductive load transients.

A remote reset capability for DACS II is provided with the following relay contact closure ratings:

- Maximum current: 0.5 ampere
- Maximum voltage: 100 V.

For CEF/SBF/non-CEF DACS II frames, all alarm and remote reset connections should be twisted pair wire wrapped to the DACS II miscellaneous terminal strip. DACS II ECEF/ESBF frames use a connectorized twisted pair for the remote reset leads, and two 15-pin connectors for local and remote alarms.

Alarm Severity (International only)

The alarm severity feature allows the users to change the severity level of most alarms to Maintenance Information (MI), Deferred Maintenance Action Minor (DMA-Minor), Prompt Maintenance Action Major (PMA-Major), or Prompt Maintenance Action Critical (PMA-Critical). The alarm severity of output messages, alarm indicating LED, alarm relay outputs and alarm query outputs will reflect the new assignment for a given alarm. If the feature is OFF, the system will have alarm severities which match their default values. If the feature is ON the user will have the ability to change the alarm severity levels and the alarm severity of an alarm will be what was last assigned. If the feature is subsequently turned OFF, the changes will not be in effect until it is turned on again. While the feature is off, the alarm severity default values will be in effect.

Hardware alarms drive alarm relays and alarm indicating LED directly. The alarm severity feature will not be able to change the severity of these alarms.

Shelf alarms that refer to alarms caused by suspected DACS II equipment failures will be individually changeable to any of the four levels of severity. Facility alarms that are associated with a single 2 Mbit/s facility will be changeable to any of the four severity levels for a PA, PB, or PC type of NPC.

For the performance monitoring alarms that are associated with a 2 Mbit/s facility, the alarm severity feature will not change the current method of assigning threshold values and setting the alarm severity. However, it will add the capability to assign a PMA-Critical severity to each of the thresholds.

Intervention Level Setting (International only)

The intervention level setting feature allows users to change the intervention level setting of most alarms. The intervention level setting will filter the alarm severity of an alarm and convert it into an intervention level of Immediate Maintenance Action (IMA), Defferred Maintenance Action (DMA), or No Intervention (NI). IMA will operate the PMA Critical alarm relay and LED. DMA will operate the PMA Major alarm relay and LED. NI will not operate any alarm relay or LED.

There are 6 intervention level settings from 1 to 6. Intervention level setting of 1 demands the highest level of intervention (Immediate Maintenance Action) and intervention level setting 6 demands the lowest level of intervention (No

Intervention). See Table 5-1 for the relationship between alarm severity and intervention level action for the six defined intervention level settings. When the feature is ON, it controls the alarm level indicated in output messages, alarm indicating LEDs, and alarm relay outputs. When the feature is OFF, the control of output messages, alarm indicating LEDs and alarm relay outputs return to the alarm severity defined by the default values or by the Alarm Severity Feature.

Table 5-1. Intervention Level Table

Intervention Level Settings	Alarm Severity as defined by Default Values or Alarm Severity			
	PMA Critical	**PMA Major**	**DMA Minor**	**MI**
1	IMA	IMA	IMA	DMA
2	IMA	IMA	DMA	DMA
3	IMA	DMA	DMA	NI
4	DMA	DMA	NI	NI
5	DMA	NI	NI	NI
6	NI	NI	NI	NI

PMA Critical - Prompt Maintenance Alarm Critical severity
PMA Major - Prompt Maintenance Alarm Major severity
DMA Minor - Defered Maintenance Alarm Minor severity
MI - Maintenance Information Alarm severity
IMA - Immediate Maintenance Action
DMA - Deferred Maintenance Action
NI - No Intervention

The default intervention level 2 will be set for all resources when the frame is grown. The intervention levels can be changed for the following resources:

- An Individual 2 Mbit/s facility set by NPC number

  This will affect the shelf alarms (LTF, DSPC), facility alarms and performance monitoring alarms associated with that NPC.

- Each Timing Link Interface

  This will affect timing link interface shelf alarms (TLI, CRO, TREF). The SSP timing references (TREF) are affected if the TLI is grown as an extractor. There are 2 SSPs per TLI extractor. CRO is affected if the TLI is grown as a Clock Reference Oscillator. Only TLI 3 can be grown as a CRO.

- Both Synchronizers

  This will affect the synchronizer shelf alarm (SYNC).

- Both Cross Connects

  This will affect any Cross Connect related shelf alarms (CCN, CCNI, TSI, and CCB).

This feature allows for assigning six Intervention Level Settings from level 1 through 6 for each of these resources. All other resources will have the intervention level setting of 2 which is not changeable.

Facility Alarms and Performance Monitoring

6

Contents

Contents

Facility Alarms and Performance Monitoring

6

Overview

DACS II collects and reports 1544 kbit/s, DS3 and 2048 kbit/s facility alarms and performance data and supports programmable thresholds. Pre-Release 6.0 1544 kbit/s PM is based on Bellcore TR-170. 1544 kbit/s PM supported Release 6.0 and later, using new circuit packs (TG191 or EMXR/EMIU), can be based on Bellcore TR-170, or Bellcore TR-820 and ANSI T1.403. Pre-Release 6.0 2048 kbit/s PM is based on ITU-T Recommendation G.821. The TG192 circuit pack is capable of supporting existing 2048 kbit/s PM, or ITU-T Recommendations G.821 and G.826 - Blue Book Series.

DACS II reports whenever any of these facility degradations exceeds the user programmable maintenance and service limits. It provides a 24-hour alarm summary report and autonomous daily audits.

1544 kbit/s Facility Alarms and Performance Monitoring

1544 kbit/s Facility Alarms

DACS II continuously monitors both 1544 kbit/s facilities directly terminated and embedded in DS3s, and detects and reports the occurrence and retirement of Carrier Group Alarms (CGAs). The CGA is the combination of a Carrier Failure Alarm (CFA) plus suitable Trunk Conditioning (TC).

- Red CGA Alarm

  The RED CGA alarm indicates that DACS II cannot frame on the 1544 kbit/s signal coming from the facility. A RED CGA may supersede either an Alarm Indication Signal (AIS) or a YELLOW CGA. The occurrence of a RED CGA inhibits further processing of all other performance parameters (that is, BER, Errored Seconds, SLIPS, etc.). When the RED CGA condition clears, the BER algorithms are reset and the performance monitoring is resumed. A RED CGA is also known as a Loss of Signal (LOS) in newer 1544 kbit/s PM standards.

- Yellow CGA Alarm

  The YELLOW CGA alarm indicates that the far end facility cannot frame on the 1544 kbit/s signal transmitted by DACS II. For 1544 kbit/s facilities with the D4 SF mode, the yellow alarm signal is sent by forcing bit 2 to zero in all channels over the digital line. For 1544 kbit/s facilities with the ESF mode, the yellow alarm signal is sent in the 4 kb/s data channel. For 1544 kbit/s facilities with the T1DM mode, the yellow alarm signal is sent in the bit 6 position of the 24th timeslot. A YELLOW CGA may supersede an existing RED CGA, but it does not inhibit further alarm or performance monitoring processing.

  The DACS II yellow alarm transmission (set bit 2 to "0" for all 24 channels in a frame) can be disabled when the TO-end facility is connected to a 24-channel wide Test Group (TG) which is in split mode. The TO-end facility NPC which is provisioned with TA, TE, or DA type and with D4 or Ericsson Cellular Framing format mode will then not send yellow alarm upstream while the facility NPC recognizes a carrier group alarm (CGA). DACS II will enable the yellow alarm transmission when the test access group is changed from split mode to monitor mode or when the active test access group is released.

- Alarm Indication Signal (AIS) CGA Alarm

  The AIS is a signal associated with a maintenance alarm detected on a failed span that is transmitted in the direction of the failure. It indicates to entities downstream that a service failure has been identified. The occurrence of an AIS CGA inhibits further processing of all other performance parameters. An AIS CGA may supersede a YELLOW CGA. Once the AIS CGA condition clears, the BER algorithms are reset and the performance monitoring is resumed.

- Loss of Multiframe Alarm (LMA)

  The LMA is valid only in DMI-BOS signaling modes and indicates that DACS II cannot frame on the word 24 multiframe pattern of the 1544 kbit/s signal.

- Remote Multiframe Alarm (RMA)

  The RMA is valid only in DMI-BOS signaling modes and indicates that the far end facility cannot frame on the word 24 multiframe pattern of the 1544 kbit/s signal transmitted by the DACS II.

Table 6-1 summarizes the declaration, retirement, and action performed by DACS II for the 1544 kbit/s facility alarms.

Table 6-1. DACS II 1544 kbit/s Carrier Group Alarms

ALARM	MODE	DETECTION		RETIREMENT	
		Algorithm	Action	Algorithm	Action
RED (voice)	D4, ESF, SLC® 96 Carrier	OOF active for 2 to 3 seconds or hit integration 5/1	Transmit YELLOW upstream and Trunk Conditioning downstream	OOF inactive for 10 to 15 seconds or hit integration 1/5	Remove YELLOW and Trunk Conditioning
RED (data)	ESF, T1DM	OOF active for 420 ms or hit integration 5/1	Same as above	OOF inactive for 84 ms	Same as above
LMA (voice)	D4 (DMI), ESF (DMI)	LMA active for 2 to 3 seconds or hit integration 5/1	Transmit RMA	LMA inactive for 10 to 15 seconds or hit integration 1/5	Remove RMA
LMA (data)	ESF (DMI)	LMA active for 420 ms or hit integration 5/1	Same as above	LMA inactive for 84 ms	Same as above
YELLOW (voice)	D4, ESF	RFA active for 420 ms or hit integration 5/1 (facility is in-frame)	Transmit Trunk Conditioning downstream	RFA Inactive for 84 ms	Remove Trunk Conditioning
YELLOW (data)	ESF, T1DM	RFA active for 168 ms (facility is in-frame)	Same as above	RFA inactive for 84 ms	Same as above
RMA (voice)	D4 (DMI), ESF (DMI)	RMA active for 420 ms or hit integration 5/1 (facility is in-frame)	Transmit Trunk Conditioning downstream	RMA inactive for 84 ms	Remove Trunk Conditioning
RMA (data)	ESF (DMI)	RMA active for 168 ms (facility is in-frame)	Same as above	RMA inactive for 84 ms	Same as above

Table 6-1. Continued

ALARM	MODE	DETECTION		RETIREMENT	
		Algorithm	Action	Algorithm	Action
AIS (voice)	D4, ESF, SLC 96 Carrier	OOF active to declare RED and AIS active for 1 second or hit integration 6/1	Transmit YELLOW upstream and Trunk Conditioning downstream	OOF inactive and AIS inactive for 168 ms, if OOF active and AIS inactive hold AIS and restart RED algorithm	Remove YELLOW and Trunk Conditioning
AIS (data)	ESF, T1DM	OOF active to declare RED and AIS active for 252 ms or hit integration 3/1	Same as above	OOF inactive and AIS inactive for 84 msec, if OOF active and AIS inactive hold AIS and restart RED algorithm	Same as above

Pre-Release 6.0 1544 kbit/s Facility Performance Monitoring Parameters

DACS II continuously monitors the incoming 1544 kbit/s signals for framing losses, slips, and bit errors. User programmable thresholds are provided to assist the determination of whether maintenance or out-of-service limits have been exceeded for a particular 1544 kbit/s facility. Minor alarms are declared at thresholds corresponding to degradations that would initiate maintenance activities. Major alarms are declared at thresholds where the service is unacceptable to customers.

The following facility performance parameters are collected by DACS II for 1544 kbit/s facilities:

- Change of Frame Alignment (COFA) - indicates the DACS II 1544 kbit/s signal receiver has gone out of frame and come back in frame at a different framing bit position. Major and minor threshold exceptions are declared when the respective programmable COFA thresholds are reached.
- Slips (SLIP) - indicates elastic store overflow or underflow events identifying synchronization problems between system and network timing. Major and minor threshold exceptions are declared when the respective programmable slip count thresholds are reached.

- Bit Error Rate (BER) - Indicates an error rate on the incoming 1544 kbit/s signal. Major and minor threshold exceptions are declared when the respective programmable BER thresholds are reached. A bit error count is not available, but the current error rate (in the form of a factor of 10) is available. The BER algorithms use the following error conditions as input:
  - — Cyclic Redundancy Checksum Errors (CRC-6) in ESF mode
  - — Framing errors and Bipolar Violation (BPV) counts in the D4 SF mode
  - — Word 24 framing errors in the T1DM mode.
- Errored Seconds (ES) - An ES is a 1±0.05 second interval during which one or more errors (or problems) are detected. A threshold exception is declared when the programmed threshold is reached. The ES is measured in the ESF mode using CRC-6 errors, and in the T1DM mode using Word 24 framing errors. The ES counts are not applicable to the D4 SF mode.
- Severely Errored Seconds (SES) - An SES is a 1±0.05 second interval with a BER of 10^{-3} or worse. A threshold exception is declared when the programmable threshold is reached. The SES counts, like the ES counts, are only for the ESF and T1DM modes of operation.
- Cyclic Redundancy Checksum Errors (CRC-6) - The CRC-6 is only applicable to the ESF mode and is a 16-bit resettable error count. No user programmable alarm threshold value is supported for the CRC-6 counts.
- Bipolar Violations (BPV) - The BPV counts are only applicable to the D4 SF mode of directly terminated 1544 kbit/s facilities. It is defined as one or more BPVs in 3 ms. No user programmable alarm threshold value is supported for the BPV counts.
- Framing Errors (FrEr) - The FrEr is only applicable to the T1DM mode which is a 16-bit resettable error count. No user programmable alarm threshold value is supported for the FrEr counts.
- Out of Frame (OOF) - The OOF counts are supported in all framing modes except the transparent mode; that is, no framing. It is a 16-bit resettable error count; no user programmable alarm threshold value is available for the OOF counts.

Table 6-2 lists the DACS II 1544 kbit/s facility performance monitoring parameters.

Table 6-2. DACS II 1544 kbit/s Facility Performance Monitoring Parameters

Parameter	Mode	Alarming Condition	Alarm Threshold Value Range	Default Alarm Threshold Value
COFA Major	D4 SF, ESF, SLC® Carrier, T1DM	Major threshold reached	001 to 511	511
COFA Minor	D4 SF, ESF, SLC Carrier, T1DM	Minor threshold reached	001 to 255	17
SLIP Major	D4 SF, ESF, SLC Carrier, T1DM	Major threshold reached	001 to 255	255
SLIP Minor	D4 SF, ESF, SLC Carrier, T1DM	Minor threshold reached	001 to 255	4
BER Major	D4 SF, ESF, SLC Carrier, T1DM	Major threshold reached	10^{-3}--10^{-5} for D4 SF; 10^{-4}--10^{-6} for SLC Carrier modes; 10^{-3}--10^{-6} for ESF, T1DM modes	10^{-3} for D4 SF, ESF and T1DM modes; 10^{-4} for SLC Carrier modes
BER Minor	D4 SF, ESF, SLC Carrier, T1DM	Minor threshold reached	10^{-4}--10^{-6} for D4 SF, SLC Carrier modes; 10^{-4}--10^{-7} for ESF, T1DM modes	10^{-6} for D4 SF, SLC Carrier modes; 10^{-7} for ESF, T1DM modes
ES	ESF, T1DM	Threshold reached	00001 to 65535	864

Table 6-2. Continued

Parameter	Mode	Alarming Condition	Alarm Threshold Value Range	Default Alarm Threshold Value
SES	ESF, T1DM	Threshold reached	001 to 255	255
CRC-6	ESF	N/A	N/A	N/A
BPV	D4 SF	N/A	N/A	N/A
FrEr	T1DM	N/A	N/A	N/A
OOF	D4 SF, ESF, SLC Carrier, T1DM	N/A	N/A	N/A

ANSI/Bellcore-Compliant 1544 kbit/s Performance Monitoring

DACS II Release 8.0 can be provisioned to support the above 1544 kbit/s PM, or to support line and path PM parameters according to Bellcore TR-820 and ANSI T1.403.

A 1544 kbit/s line is defined by the network endpoints at which the 1544 kbit/s line coding (AMI, B8ZS) is generated and terminated. A DACS II line termination function exists at each direct 1544 kbit/s interface in an FTU/IFTU. A 1544 kbit/s path is defined by the network endpoints at which the 1544 kbit/s frame structure (D4, ESF, T1DM) is generated and terminated. A 1544 kbit/s path may traverse multiple 1544 kbit/s lines. A DACS II path termination function exists at each 1544 kbit/s interface that is not configured as a Clear-1544 kbit/s cross-connection in an FTU/IFTU or a DS3U.

The following line performance parameters have been defined by Bellcore for 1544 kbit/s PM:

- Line Coding Violations (CV) - This parameter is a count of CVs based on the 1544 kbit/s line format. For AMI line coding, this is a count of bipolar violations (BPV). For B8ZS line coding, it is a count of BPVs that are not part of the zero substitution pattern. For B8ZS-coded lines, unexpected bit sequences such as 8 or more consecutive zeros are also a BPV. DACS II must monitor and accumulate the count of line CVs without converting it into a BER estimate for reporting purposes.

- Line Errored Seconds (ES) - This parameter is a count of seconds during which at least one line CV has occurred.
- Line Severely Errored Seconds (SES) - This parameter is a count of seconds during which at least 1544 line CVs have occurred. The number is based on ITU-T guidelines and corresponds to approximately a 10e-3 BER.

Before defining the 1544 kbit/s path performance parameters, it is necessary to discuss a new path impairment event, the Severely Errored Framing (SEF) event, which has been defined by Bellcore and the ANSI T1M1 committee. It is used in the definition of various 1544 kbit/s path performance parameters.

For 1544 kbit/s, an SEF event is the occurrence of 2 or more framing bit errors within a 3-ms period, where contiguous 3-ms periods are examined. This definition applies to both D4 and ESF framing modes. However, in order to provide compatibility with older 1544 kbit/s equipment, Bellcore allows the occurrence of an OOF or a COFA event to be substituted for an SEF event. In these cases, the existing *m* or more out of *n* consecutive framing bit errors criteria is used.

The following *path* performance parameters have been defined by ANSI for ESF 1544 kbit/s PM:

- Path Coding Violations (CV) - For ESF framing, this is a count of detected CRC-6 CVs. For D4 framing, since there is no embedded CRC mechanism, this is a count of detected framing bit errors. DACS II must monitor and accumulate the count of path CVs without converting it into a BER estimate for reporting purposes.
- Path Errored Seconds (ES) - This parameter is a count of seconds during which at least one of the following has occurred: a path CV, a controlled slip, or an SEF event. Note that for D4 framing, this definition condenses into a second containing one or more framing bit errors or a controlled slip.
- Path Severely Errored Seconds (SES) - For ESF framing, this parameter is a count of seconds during which at least one of the following has occurred: 320 or more CRC-6 CVs or an SEF event. For D4 framing, this parameter is a count of seconds during which the following has occurred: 8 or more framing bit errors or an SEF event.
- Path Severely Errored Framing Seconds (SEFS) - This parameter is a count of seconds during which at least one SEF event has occurred.
- Path Controlled Slip Seconds (CSSP) - This parameter is a count of seconds during which a controlled slip has occurred.
- Path Unavailable Seconds (UASP) - This parameter is a count of seconds from the *onset* of the condition that causes an Unavailable Signal Status to be declared to the *onset* of the condition that causes it to be cleared. Only UASP is collected during a failure.

The following *line* PM parameters are collected by DACS II Release 8.0: Far-end ES, near-end CV, ES and SES.

The following *path* PM parameters are collected by DACS II Release 8.0 for both far-end and near-end: CV, ES, SES, SEFS, CSSP and UASP.

The following register intervals are kept for each PM parameter: current 15-minute interval, previous 15-minute interval, current day, previous day, 95 additional recent 15-minute intervals, and 6 additional recent days. The register size for 15-minute CV counts is 2,097,151 (21-bit), and for daily CV counts is 134,217,727 (27-bit). The maximum register size for 15-minute intervals is 900 (seconds/15 minutes), and for daily intervals is 86400 (seconds/day).

The default threshold values for all PM parameters are shown Table 6-3.

Table 6-3. Line and Path Parameter Default Threshold Values

Performance Parameter	Number/Day	Number/15 Minutes
Line CVs (BPVs)*	133,400	13,340
Path CVs (CRCs)*	132,960	13,296
Path CVs (FEs in D4)*	691	72
CSSP	4	1
SEFS	17	2
Line/Path ES	648	65
Line/Path SES	100	10
UASP	10	10

* These default threshold values correspond to an approximate BER of 10e-5 for 15-minute registers and 10e-6 for daily registers using a uniform distribution model.

Alarms and Performance Monitoring for SLC® 96 Carrier Facility

The DACS II SLC 96 Carrier interface feature, not applicable to 1544 kbit/s facilities embedded in the DS3, supports two types of alarm information which can either be received from or sent to a SLC 96 Carrier Remote Terminal (RT) or equivalent terminals:

- Data link alarm information

  The data link alarm information is supported by both the Mode I and Mode III interfaces, and it contains four kinds of alarm messages:

— Major Alarm (MJ) message - indicates the existence of a major alarm condition defined as the loss of transmission or service to customers on one or more 1544 kbit/s facilities. An MJ condition detected at DACS II is reported as a RED CGA. An MJ message along with a shelf alarm message (defined below) received from the RT is reported as a YELLOW CGA by DACS II. Note that an MJ message without being accompanied by a shelf alarm message is not a facility alarm.

— Minor Alarm (MN) message - indicates the existence of a minor alarm condition, defined as a system state caused by a non-service-affecting fault.

— Shelf Alarm message - indicates the 1544 kbit/s that loses its operational integrity, such as framing error, loss of signal, or excessive BPVs. The receipt of a shelf alarm message is not reported as a facility alarm; however, two performance parameters, Shelf Alarm Near End (SANE) and Shelf Alarm Far End (SAFE), are kept by DACS II for each SLC 96 Carrier facility as health indicators. The SANE counter is incremented by one each time DACS II sends a shelf alarm message for the 1544 kbit/s facility; the SAFE counter is incremented by one each time a shelf alarm message for the facility is received. The threshold range is 00001 to 65535 with the value 00000 as the default for both parameters. When the threshold is exceeded, an information report is generated.

— Power/Miscellaneous (PWR/MISC) alarm message - indicates that a power failure or a prearranged alarm condition (flood alarm, fire alarm, or noxious gas alarm) exists at the RT location. The PWR/MISC alarm is not a facility alarm and, when received from the RT, will cause DACS II to raise either a major or a minor alarm (user programmable).

- Yellow alarm signal

  The yellow alarm signal is only used by the SLC 96 Carrier Mode III system. When DACS II detects the signal, it will declare a YELLOW CGA alarm.

Alarms and Performance Monitoring for SLC Series 5 Carrier System Facility

DACS II SLC Series 5 Carrier System Feature Package C (FPC) interface feature, not applicable to 1544 kbit/s facilities embedded in the DS3, supports three types of alarm information which can either be received from or sent to an FPC RT:

- Data link alarm information

  The SLC Series 5 Carrier System FPC data link alarm information contains five kinds of alarm messages:

  - Major alarm message - same as the SLC 96 Carrier interface.
  - Minor alarm message - same as the SLC 96 Carrier interface.
  - Shelf alarm message - same as the SLC 96 Carrier interface, except that no shelf alarm parameters are monitored.
  - Power minor alarm message - indicates loss of AC power or rectifier failure at the RT (not a facility alarm).
  - Miscellaneous alarm - indicates that a prearranged alarm condition has occurred at the RT (not a facility alarm).

- Alarm Indication Signal (AIS)

  Same as the AIS CGA defined in Section 6.1.1.

- Yellow alarm signal

  Same as the ESF mode YELLOW CGA defined in Section 6.1.1.

Alarms and Performance Monitoring for Clear 1544 kbit/s Facility

A Clear 1544 kbit/s facility is a 1544 kbit/s signal provisioned with no framing format. DACS II Release 8.0 supports unframed and framed Clear 1544 kbit/s, the latter is achieved by using an off-line framer which allows for 1544 kbit/s PM.

Only the RED CGA facility alarm is available for the unframed Clear-1544 kbit/s facilities. The RED CGA is declared when the Loss of Signal (LOS) (for directly terminated 1544 kbit/s) or Loss of Receive Clock (LRLC) (for embedded 1544 kbit/s) is detected. When a RED CGA is declared for a Clear 1544 kbit/s facility, the AIS is transmitted downstream.

Although Bellcore does not require path PM for Clear-1544 kbit/s signals, DACS II Release 8.0 provides both line and path PM for framed Clear 1544 kbit/s, as defined for ANSI/Bellcore-Compliant 1544 kbit/s PM.

For Unframed Clear 1544 kbit/s in DACS II, only line PM is done. DACS II monitors the SLIP, BER, and BPV parameters for directly terminated unframed Clear 1544 kbit/s facilities, and it only monitors the SLIP parameter for embedded 1544 kbit/s facilities.

DS3 Facility Alarms and Performance Monitoring

For both the M13 and C-bit Parity DS3 framing formats, DACS II detects and retires the following DS3 facility alarms and status conditions:

- Loss of Signal (LOS)

  An LOS alarm is declared when ten consecutive 1-second intervals contain an LOS event. An LOS event occurs when 175±75 successive zeros are encountered on the DS3 line. An LOS alarm is retired when ten consecutive one second intervals contain no LOS events.

- High Bit Error Rate (HBER)

  An HBER alarm is declared when ten consecutive 1-second intervals contain an HBER event. An HBER event is declared when the number of bit errors that occur in a one second interval reaches or exceeds a programmable threshold (10^{-3} or 10^{-6}). Either bipolar violations or parity errors can be selected for the bit error rate calculation. An HBER alarm is retired when ten consecutive 1-second intervals contain no HBER events measured at a threshold by a factor of 10 below the programmed threshold.

- Out-of-Frame (OOF)

  An OOF alarm is declared when ten consecutive 1-second intervals contain an OOF event. The OOF alarm is retired when ten consecutive 1-second intervals do not contain an OOF event.

- Alarm Indication Signal (AIS)

  A DS3-AIS condition is declared when an AIS signal is detected for ten consecutive 1-second intervals. An AIS condition is retired when an AIS event is absent for ten consecutive 1-second intervals. Note that the DS3-AIS indication is reported as information rather than an alarm.

DACS II also accumulates and provides the following Near-End and Far-End path performance monitoring parameters, via a TABS link, for DS3 facilities using the C-bit Parity framing format:

- Data Missing Indicator
- Number of Detected Errors
- Out-of-Frame Seconds
- Type A Errored Seconds
- Type B Errored Seconds

- Type C Errored Seconds.

2048 kbit/s Primary Block Facility Alarms and Performance Monitoring

DACS II continuously monitors the 2048 kbit/s primary block facilities for both Primary Block Alarms (PBAs) and facility performance parameters. Prior to Release 6.0 DACS II provides 2048 kbit/s alarm and PM for PB/BC primary type according to ITU-T Rec. G.821. In Release 6.0 and later, DACS II also provides new 2048 kbit/s PA type facility PM according to the following ITU-T recommendations:

- ITU-T Recommendation, "Frame alignment and Cyclic Redundancy Check (CRC) procedures relating to basic frame structures defined in Recommendation G.704," Rec. G.706, April 1991.
- ITU-T Recommendation, "Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s," Blue Book Vol. III, Fascicle III.4, Rec. G.732, November 1988.
- ITU-T Recommendation, "Error performance of an international digital connection forming part of an integrated service digital network," Blue Book Vol. III, Fascicle III.5, Rec. G.821, November 1988.
- Draft ITU-T Recommendation, "Error performance parameters and objectives for international constant bit rate digital paths at or above the primary rate," Draft Rec. G.826, June 10, 1992.
- ITU-T Recommendation, "Synchronous Digital Hierarchy (SDH) management," Rec. G.784, December 1990.
- ITU-T Recommendation, "Maintenance philosophy for telecommunications network," Blue Book Vol. IV, Fascicle IV.1, Rec. M.20, November 1988.
- ITU-T Recommendation, "Performance limits for bring into service and maintenance of digital paths, sections, and line sections," Blue Book Vol. IV, Fascicle IV.1, Rec. M.550, November 1988.
- ITU-T Recommendation, "Equipment to perform in-service monitoring on 2048 kbit/s signals," Blue Book Vol. IV, Fascicle IV.1, Rec. O.162, November 1988.

The facility monitoring is a continuous process that allows DACS II to

- Detect errors or failures
- Identify the failed direction and/or location (facility or equipment)
- Accumulate and calculate performance parameters.

In this section the pre-Release 6.0 2048 kbit/s PM will be referred to as "PB/PC-type 2048 kbit/s PM", and the Release 6.0 and later enhanced 2048 kbit/s PM will be referred to as "PA-type 2048 kbit/s PM".

Pre-Release 6.0 2048 kbit/s Primary Block Alarms and Performance Monitoring

PB/PC-Type 2048 kbit/s Primary Block Alarms

PB/PC type 2048 kbit/s primary block facilities terminating on DACS II are monitored for two types of Primary Block Alarms (PBAs): the 2048 kbit/s alarms and the Time Slot 16 (TS16) alarms.

- 2048 kbit/s alarms:
  - — AIS - The AIS alarm is declared when the Alarm Indication Signal is received in all 32 time slots.
  - — Primary Block Failure (PBF) - The PBF alarm is declared when the Loss of Frame Alignment (LOFA) or the Loss of Signal (LOS) condition is detected. The LOFA is defined in Section 6.3.2, and the LOS is defined as the receipt of 11 to 50 consecutive zeros.
  - — Excessive Error Rate (EER) - The EER alarm is declared when four consecutive 1-second intervals each have 19 or more FAS+* errors.
  - — Bit Error Rate (BER) - The BER alarm is declared when three consecutive 2-second intervals are "flagged". A 2-second interval is flagged if two or more CRC errors are detected within that interval.
  - — Remote AIS (RAIS) - The RAIS alarm is declared when the RAIS indication is detected in TS0 Bit 4 of the NFW.
  - — Remote Alarm Indication (RAI) - The RAI alarm is declared when the remote alarm indication is received in TS0 Bit 3 of the NFW.
  - — Remote Bit Error Rate (RBER) - The RBER alarm is declared when the RBER indication is detected in Time Slot 0 (TS0) Bit 4 of the Non Frame Word (NFW).
- TS16 alarms:
  - — A16 - The A16 alarm is declared when AIS is received in TS16 of a facility using CAS.

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* FAS+ is defined as the 8-bit total consisting of the Frame Alignment Signal (FAS) (0011011 pattern in the even frame of Time Slot 0) and bit 2 (set to 1) contained in the odd framing word of TS0.

— Loss of Multiframe Alignment (LMA) - The LMA alarm is declared when LMA or loss of incoming signal is detected on TS16 of a facility using CAS.

— R16 - The R16 alarm is declared when the remote alarm indication is received in bit 6 of frame 0 of TS16.

Table 6-4 summarizes the PBA report priority, coexistence, and consequent action.

Table 6-4. PB/PC-Type Primary Block Alarm Types

Alarm Type	Priority	Coexistence	Consequent Action				
			Maintenance Classification	Remote Alarm Indication Transmitted in TS0 Bits	Remote Alarm Indication Transmitted in TS16, Bit 6 Frame 0	AIS Applied to All Received Timeslots	AIS Applied to Received Signaling Channels in TS16
AIS	(Highest Level)	None	MI	Y(RAI,RAIS)		Y	Y
PBF		None	PMA	Y(RAI)		Y	Y
EER		None	PMA	Y(RAI)		Y	Y
BER		A16, LMA, RAIS, RAI, RBER	DMA	Y(RBER)			
RAIS		BER, RAI, A16, LMA	MI				Y*
RAI		BER, RAIS, RBER, A16, LMA	MI				Y*
RBER		BER, RAI, A16, LMA, R16	MI**				
A16		BER, RAIS, RAI, RBER	MI		Y(R16)		Y
LMA		BER, RAIS, RAI, RBER	PMA		Y(R16)		Y
R16	(Lowest Level)	BER, RBER	MI				Y*

* Dependent on the 2048 kbit/s NPC type provisioned

** Can be disabled

PB/PC-Type 2048 kbit/s Performance Monitoring

DACS II supports the following performance monitoring parameters for PB/PC type 2048 kbit/s primary blocks provisioned with the CRC-4 error detection:

- CRC check block errors (CRC)

  A CRC occurs when computed CRC-4 bits do not equal received CRC-4 bits. The CRC is not counted during AIS, LOFA, or LOS.

- Degraded Minutes (DM) - DM is a minute with BER worse than $1x10^{-6}$ and is calculated on an hourly basis.
- Severely Errored Seconds (SERS) - SERS is an available second with one or more Loss of Frame Alignments (LOFA), LOS, or one or more SLIPs, or more than 805 CRC errors.
- Errored Seconds (ERS) - ERS is an available second with one or more LOFA, LOS, or one or more SLIPs, or one or more CRC errors.
- Unavailable Seconds (US) - If SERS appear for more than 10 consecutive seconds, these 10 seconds are USs. Each additional second will also be counted as US. If the BER is less than $1x10^{-3}$ for 10 consecutive seconds, these 10 seconds are not USs.
- Slip event (SLIP) - The occurrence of one or more underflows or overflows of the slip buffer in a 1-second period when no loss of frame alignments occurred.
- Loss of frame alignment (LOFA) - LOFA is declared when one or more of the following conditions occur:
  - — Three consecutive Frame Alignment Signals (FASs) have been received with an error.
  - — TS0 Bit 2 of the NFW has been received with an error on three consecutive occasions.
  - — Nine hundred and fifteen or more CRC errors have been found in a 1-second interval.

  A continuous LOFA is counted as one LOFA and the LOFA counter is updated once a second. LOFAs are not counted during AIS or LOS.
- Framing error (FRER) - An FRER is one or more errors in four consecutive FAS or NFW bit 2 signals; that is, in four consecutive FAS+. FRERs are not counted during AIS, PBF, or EER.
- Multiframe alignment error (MER) - MER is the occurrence of one or more errors in the 0000 signaling multiframe alignment signal of TS16. MER is monitored only when the facility is provisioned with CAS. MERs are not counted during AIS, PBF, A16, or LMA.

If a 2048 kb/s digital line is not provisioned with CRC-4 capability, Framing Errors are used to derive performance information. All of the parameters are defined as in the "provisioned with CRC" case, except for the following:

- DM - The DM is the same as the definition in "provisioned with CRC", except that DMs are those with one or more errors in the FAS.
- SERS - The SERS is an available second with one or more LOFA, LOS or SLIPs, or 19 errors in FAS+.
- ERS - The ERS is an available second with one or more LOFA, LOS or SLIPs, or an error in the FAS+.

Table 6-5 displays the performance monitoring parameters for 2048 kbit/s primary block facilities. For those parameters with user programmable thresholds, DACS II also provides user programmable alarm levels.

Table 6-5. DACS II PB/PC-Type 2048 kbit/s Facility Performance Monitoring Parameters

Parameter	Threshold Range	Default Value	Alarm
DM, 1 hour	1-60	60	MI, DMA, PMC or PMA
DM, 24 hours	1-1440	1440	MI, DMA, PMC or PMA
SERS, 15 mins	1-900	900	MI, DMA, PMC or PMA
SERS, 24 hours	1-65535	65535	MI, DMA, PMC or PMA
ERS, 15 mins	1-900	900	MI, DMA, PMC or PMA
ERS, 24 hours	1-65535	65535	MI, DMA, PMC or PMA
US, 15 mins	1-900	900	MI, DMA, PMC or PMA
US, 24 hours	1-65535	65535	MI, DMA, PMC or PMA
SLIP, 15 mins	1-900	900	MI, DMA, PMC or PMA
SLIP, 24 hours	1-65535	65535	MI, DMA, PMC or PMA
CRC	N/A	N/A	NONE
FRER	N/A	N/A	NONE
LOFA	N/A	N/A	NONE
MER	N/A	N/A	NONE

Enhanced 2048 kbit/s Alarms and Performance Monitoring

DACS~II continuously monitors the 2048 kbit/s primary block transmission line for both Primary Block Alarms (PBAs) and transmission line performance parameters.

2048 kbit/s transmission lines terminating on DACS~II are monitored for three types of 2048 kbit/s transmission line alarms: signal alarms, Time Slot 0 (TS0) detected alarms and Time Slot 16 (TS16) detected alarms.

Signal Alarms

- Loss of Signal (LOS)
  The LOS condition is declared when more than 32 consecutive zeros are detected.
- Alarm Indication Signal (AIS) Alarm
  AIS is detected when 2 consecutive 512 bit blocks with fewer than 3 zeroes are detected.
- Loss of Frame (LOF)
  The LOF condition is declared when three consecutive Frame Alignment Signals (FASs) have been received with an error or when TS0 bit 2 of the Non Frame Word (NFW) have been received with an error on 3 consecutive occasions. In addition, DACS~II will declare a LOF when 915 or more CRC-4 block errors are detected in a one second interval.
- Excessive Error Rate (EER)
  The EER alarm is declared when 8192 or more coding violations are detected in a four second interval, which is equivalent to a Bit Error Rate (BER) of $1X10^{-3}$. The EER alarm is also declared when four consecutive 1-second intervals each have 19 or more FAS+* errors.
- Bit Error Rate (BER)
  The BER alarm is declared when 1228 or more coding violations are detected in a 1 minute interval, which is equivalent to a BER of $1X10^{-5}$. The BER is also declared when 3 consecutive 2-second intervals each contain 2 or more CRC block errors (for transmission line interface provisioned with CRC-4), or 2 or more FAS+ block errors (for transmission line interface provisioned without CRC-4).
- Loss of CRC-4 Multiframe Alignment (LCMA)
  The LCMA alarm is declared when basic frame alignment is valid but CRC-4 multiframing is lost on the transmission line interface which is provisioned with CRC mode. If the automatic CRC mode is provisioned, then no LCMA alarm is declared even though CRC-4 multiframing is lost or is not present. However, the CRC-4 multiframe pattern is generated in the transmit direction. Automatic CRC mode is primarily intended for situations where circuits are gradually upgraded (a few at a time) to CRC-4 multiframing use, but alarms need to be avoided on circuits that have not yet been upgraded.
- Far End LCMA (FLCMA)
  The FLCMA alarm is declared when more than 990 CRC-4 block errors are reported from the far end equipment (via E-Bits) in each second for five consecutive seconds.

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* FAS+ is defined as the 8-bit total consisting of the Frame Alignment Signal (FAS) (0011011 pattern in the even frame of Time Slot 0) and bit 2 (set to 1) contained in the odd framing word of TS0.

TS0 Detected Alarms

- Remote Alarm Indication (RAI)
  The RAI alarm is declared when the remote alarm indication is received in TS0 Bit 3 of the NFW.
- Remote AIS (RAIS)
  The RAIS alarm is declared when the RAIS indication is detected in TS0 Bit 4 of the NFW on the transmission line interface which is provisioned with RAIS alarming capability enabled.
- Remote Bit Error Rate (RBER)
  The RBER alarm is declared when the RBER indication is detected in TS0 Bit 4 of the NFW on the transmission line interface which is provisioned with RBER alarming capability enabled.
- Synchronization Failure Indication (SFI)
  The SFI alarm is declared when SFI indication is detected in TSO Bit 5 of the NFW. Detection of this alarm is software programmable on a per 2048 kbit/s transmission line interface basis.
- Pseudo Frame Word Out-of-Frame (PFWOOF)
  For timeslot zero to non-timeslot zero cross-connections using the Pseudo Frame Word (PFW) mode, the PFWOOF alarm will be declared if the PFW cannot be recognized.

TS16 Detected Alarms

- A16
  The A16 alarm is declared when "ALL-Ones" is received in TS16 of a transmission line interface using CAS.
- Loss of Multiframe Alignment (LMA)
  The LMA alarm is declared when LMA or loss of incoming signal is detected on TS16 of a transmission line interface using CAS.
- R16
  The R16 alarm is declared when the remote alarm indication is received in bit 6 of TS16 of Frame 0.

Alarm Maintenance Classification and Consequent Action

The alarm levels that can be raised include the following:

- PMA - Prompt Maintenance Action Major Alarm
- PMC - Prompt Maintenance Action Critical Alarm
- DMA - Deferred Maintenance Alarm
- MI - Maintenance Information.

Table 6-6 specifies the alarm types and levels to be declared for each detected 2048 kbit/s failures or TS0 failure indications. The "k" column represents the alarm type keyword to be output in the DACS II alarm message.

Note that the TH type NPC does not support FLCMA alarm.

Table 6-6. 2048 kbit/s Alarm Types and Levels

Failure	Alarm Type (k)	Alarm Level
LOS	R	PMA
LOF	F	PMA
EER	X	PMA
AIS	A	PMA or PMC or DMA or MI or Disabled (Default MI)
SFI	S	MI
BER	B	DMA
LCMA	C	MI
RAI	Y	MI
RAIS	I	MI
RBER	E	MI
PFWOOF	P	MI
FLCMA	G	MI

Table 6-7 specifies the alarm types and alarm levels for each detected TS16 failures or failure indications.

Table 6-7. TS16 Alarm Types and Levels

Failure	Alarm Type (k)	Alarm Levels
LMA	L	PMA
RMA	M	MI
A16	V	MI

Table 6-8 summarizes the consequent actions for detected alarms.

NOTE:
The FLCMA and SFI alarms are not available for TH type NPCs.

Table 6-8. Consequent Actions for Detected Alarms

Detected Alarm	Consequent Action			
	Remote Alarm Indication Transmitted in TS0 Bits	**Remote Alarm Indication Transmitted in TS16, Bit 6, Frame 0**	**AIS Applied to All Received Timeslots**	**AIS Applied to Received Signaling Channels in TS16**
LOS/LOF	RAI	—	yes	yes
AIS	RAI,RAIS*	—	yes	yes
EER	RAI	—	yes	yes
BER	RBER*	—	—	—
RAI	—	—	—	yes*
RAIS	—	—	—	yes*
A16	—	R16	—	yes
LMA	—	R16	—	yes
R16	—	—	—	yes*
FLCMA	—	—	—	—
LCMA	Set E bits	—	yes†	yes†
SFI‡	—	—	—	—

* Dependent on the 2048 kbit/s transmission line NPC type provisioned.

† No consequent action if Automatic CRC-4 is enabled.

‡ Extracted line clock to synchronizer is squelched.

Figure 6-1 shows the alarm reporting priority and coexistence scheme in a tree type format. An offspring alarm on the tree has a lower priority than its root alarm and is not reported if there is an existing root alarm. Two alarms can coexist if they are not in each other's root path.

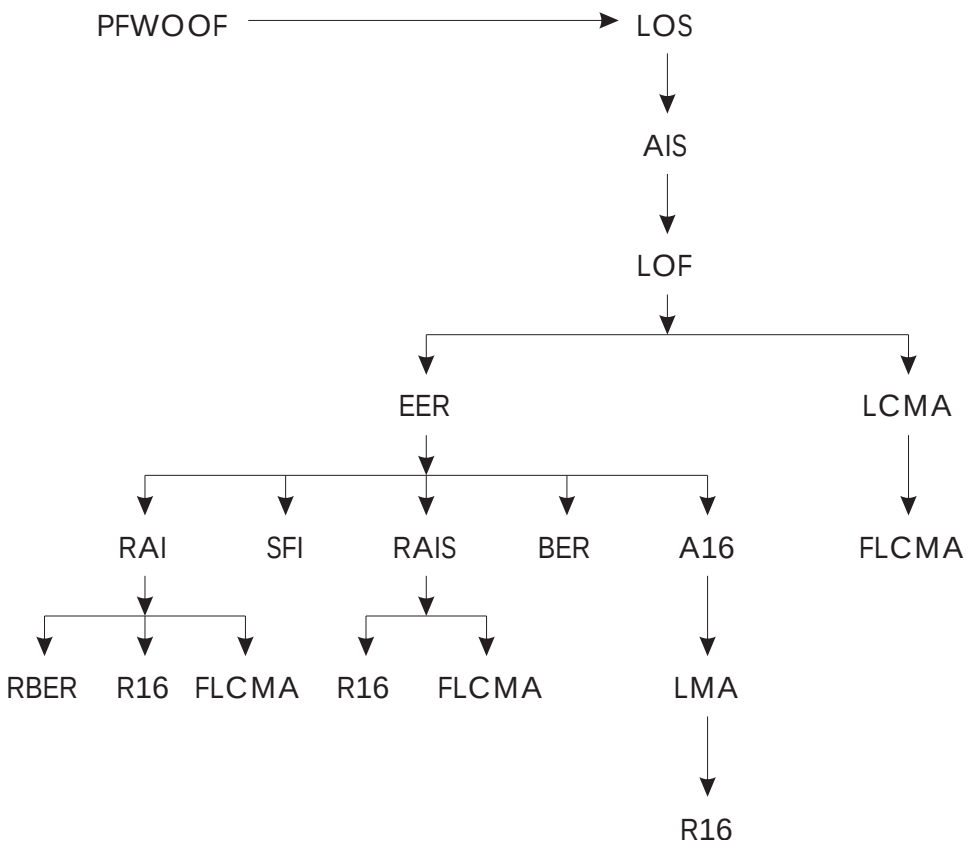

Figure 6-1. DACS~II Facility Alarm Priority and Coexistence

PA/TH-Type 2048 kbit/s Performance Monitoring

DACS II Release 8.0 collects the following PM parameters for the 2048 kbit/s signals supported by the new PA-type primaries, framed (channelized and clear) 2048 kbit/s and unframed clear 2048 kbit/s:

- Code Violation (CV) - The CV count is incremented every time a CV is detected.
- Controlled Slip Seconds (CSS) - The CSS count is incremented for every 1-second interval with one or more controlled slip(s).

- Framing Error (FRER) - The FRER count is incremented every time a framing error is detected.
- CRC - The CRC count is incremented every time a CRC block error is detected. For NPCs with automatic CRC-4 mode, the CRC count shall not be accumulated when an LCMA is declared.
- Out of Frame Seconds (OFS) - The OFS count is incremented for every 1-second interval with one or more LOS defect.
- Errored Seconds (ES) - The ES count is incremented for every 1-second interval with one or more of these conditions: CV, slip, LOS, LOF, framing error, CRC-4 block error, or AIS event.
- Severely Error Seconds (SES) - The SES count is incremented for every 1-second interval with one or more of these defects: CV, slip, LOS, LOF, AIS event, distributed errored FAS+ or CRC blocks.
- Unavailable Time Count (UATC) - A period of Unavailable Time (UAT) begins when the bit error ration in each second is worse than 0.001 for a period of 10 consecutive seconds. These 10 seconds are considered to be UAT. The UATC is incremented every time a UAT period is entered.
- Unavailable Seconds (UAS) - The UAS is incremented for every 1-second interval in a UAT period.
- Multiframe Alignment Error (MER) - The MER count is incremented when one or more error is detected in the "0000" signaling multiframe alignment signal of TS16.
- Far End Block Error (FEBE) - The FEBE count is incremented every time an E bit is received with a binary value of "0".
- Far End Errored Seconds (FES) - The FES count is incremented for every 1-second interval with one or more FEBEs.
- Far End Severely Errored Seconds (FSES) - The FSES count is incremented for every 1-second interval with 002 to 915 or more FEBEs.
- Far End Unavailable Seconds (FUAS) - The FUAS is calculated using FSES. If 10 consecutive FSESs are detected, the FE is declared Unavailable (UA), and the 10 FSESs are not counted as FSES. Instead, these 10 seconds and any additional seconds are counted as FUAS, until the Unavailable status is cleared. The UA status is cleared at the beginning of a 10-second interval in which no FSES occurs.

Note: The FEBE, FES, FSES, and FUAS are not available for the TH type NPCs.

Table 6-9 summarizes the various parameter accumulation for the new TH-type and PA-type framed/unframed 2048 kbit/s signals, and the older PB/PC 2048 kbit/s signals. All parameters are collected for 15-minute, previous 15-minute, 24-hour, and previous 24-hour intervals.

Table 6-9. Parameter Accumulation During Failures or UAT

Termination Type	Parameters	Failures							
		LCMA	UAT	TS16	EER	LOF	AIS	LOS	FUAT
Unframed 2 Mbit/s	CV	NA	M	NA	M	NA	NA	I	N/A
	CSS	NA	M	NA	M	NA	NA	I	N/A
Framed 2 Mbit/s	CV	M	M	M	M	I	I	I	M
	FRER	M	M	M	I	I	I	I	M
	CRC	I	M	M	M	I	I	I	M
	CSS	M	M	M	M	I	I	I	M
	OFS	M	M	M	M	M	I	I	M
	ES	M	I	M	M	M	M	M	M
	SES	M	I	M	M	M	M	M	M
	UAS	M	M	M	M	M	M	M	M
	MER (MERS)	M	M	I	M	I	I	I	M
	UATC	M	M	M	M	M	M	M	M
	FEBE	I	M	M	M	I	I	I	M
	FES	I	M	M	M	I	I	I	I
	FSES	I	M	M	M	I	I	I	I
	FUAS	I	M	M	M	I	I	I	M
	TS0M	M	I	M	I	I	I	I	M
PB/PC 2 Mbit/s	DM	NA	I	M	M	I	I	I	N/A
	SERS	NA	I	M	M	M	M	M	N/A
	ERS	NA	I	M	M	M	M	M	N/A
	US	NA	M	M	M	M	M	M	N/A
	Slips (CSS)	NA	M	M	M	I	I	I	N/A
	LOFA (OFS)	NA	M	M	M	M	I	I	N/A
	CRC	NA	M	M	M	I	I	I	N/A
	FRER	NA	M	M	I	I	I	I	N/A
	MER (MERS)	NA	M	I	M	I	I	I	N/A

I - Inhibited M - Monitored NA - Not Applicable

TS16 is defined as A16 or LMA.

UAT is Unavailable Time (defined as the time when the Primary is unavailable).
FUAT is Far-End Unavailable Time.

Table 6-10 specifies the minimum register sizes, threshold ranges and default values.

Table 6-10. Parameter Register Threshold Range and Default Values

Interval	Parameter	Min. Size/Threshold Range	Default
15-Minute	CV	1 - 1843200	18432
	FRER	1 - 3600000	18432
	CRC	1 - 823500	18432
	UATC	1 - 45	3
	CSS	1 - 900	1
	OFS	1 - 900	4
	ES	1 - 900	300
	SES	1 - 900	30
	UAS	1 - 900	30
	MER	1 - 900	255
	FEBE	1 - 823500	18432
	FES	1 - 900	300
	FSES	1 - 900	30
	FUAS	1 - 900	30
24-hour	CV	1 - 176947200	176947
	FRER	1 - 345600000	176947
	CRC	1 - 79056000	176947
	UATC	1 - 4320	9
	CSS	1 - 86400	4
	OFS	1 - 86400	4
	ES	1 - 86400	4320
	SES	1 - 86400	90
	UAS	1 - 86400	90
	MER	1 - 86400	4095
	FEBE	1 - 79056000	176947
	FES	1 - 86400	4320
	FSES	1 - 86400	90
	FUAS	1 - 86400	90

Equipment and Facility Protection

7

Contents

Equipment and Facility Protection

7

Hardware Protection

The DACS II architecture provides complete redundancy to equipment which carries or affects service for more than two 1544 kbit/s/2048 kbit/s Primary Block facilities. This redundancy results in different types of equipment protection.

Duplicated Equipment and Protection Switching Performance

The duplicated equipment redundancy consists of two independent but fully duplicated sides (Side 0 and Side 1) for signal and clock distribution paths. This duplicated, redundant architecture provides protection for Format Converters (in FTU/IFTU), a Formatter (in DS3U), Digital Signal Processing Circuits (DSPCs), and the ECCN.

The protection switching of duplicated equipment; that is, side switching, can be initiated autonomously or manually. The autonomous side switching is performed when an entity on the active side fails, provided that the inactive side is in service. The manually initiated side switching is performed when a valid side switching command is entered while the inactive side is in service.

Table 7-1 specifies DACS II Release 8.0 autonomous side switching performance data including the failure detection time. The manually initiated side switching is hitless.

Table 7-1. DACS II Release 8.0 Circuit Pack Switching Performance

Circuit Pack Failed	Nominal Switching Time (in ms)
CCNI	0.0
CCI	0.0
BT	0.0
CCB	4.2
TSI	7.9
ETSI	3.7
Sync TB	0.7
Sync DPLL	54.3
FC	50.8
FMT	15.3
DMB	40.0
SRM	40.0
MJU	40.0

DS3 Unit Equipment Protection and Switching Performance

DACS II provides a 1:1 protection for the Facility Line Interface (FLI) circuit packs within the DS3U. DACS II also provides a 6:1 protection for the Multiplexer (MXR), Enhanced MXR (EMXR) and Enhanced Multiple Interface Unit (EMIU) in the DS3U as well as the Hybrid Multiplexer (HMXR) circuit packs in the Hybrid DS3U. These two protection mechanisms operate independently from sides 0 and 1. The EMXR and EMIU are new circuit packs in Release 6.0. The EMXR is a superset of the MXR, and is used with the EMIU to provide enhanced 1544 kbit/s performance monitoring in compliance with ANSI T1.403 standards for the 1544 kbit/s embedded in a DS3. The MXR/EMIU pairing is not allowed.

The HMXR and HFMT are new circuit packs in Release 8.0. The HFMT is required if the HMXR is used. The HMXR supports Hybrid DS3 functionality allowing the DS2s within a DS3 to be provisioned with four 1544 Kbit/s circuits or three 2048 Kbit/s circuits. The HMXR/EMIU pairing is not allowed.

The MXR/EMXR/EMIU/HMXR protection switching is performed when a service MXR/EMXR/EMIU/HMXR fails or a valid manual switching command is entered, provided that the protection MXR/EMXR/EMIU/HMXR is in service and is not protecting another MXR/EMXR/EMIU/HMXR. An MXR cannot be used to protect an EMXR nor HMXR. An EMXR cannot be used to protect an HMXR.

The FLI protection switching can be initiated by a service FLI failure or a valid switching command, provided that the protection FLI is in service.

Table 7-2 specifies DACS II DS3U MXR/EMXR/EMIU/HMXR and FLI protection switching performance data. The time specified for the autonomous protection includes the failure detection time.

Table 7-2. DACS II Release 8.0 DS3U Entity Protection Switching Performance

Circuit Pack	Switching Method	Nominal Switching Time (in ms)
EMXR/EMIU	Autonomous	45.35
	Manual Command	5.65
FLI	Autonomous	14.15
	Manual Command	7.60

SLC® Carrier Interface Protection and Switching Performance

DACS II Release 6.0 supports two types of SLC Carrier 1544 kbit/s interfaces:

- Bellcore TR-TSY-000008 compatible SLC Carrier Interface
- SLC Series 5 Carrier System Feature Package C (FPC) Interface.

For both interfaces, an optional 1544 kbit/s protection switching feature is provided between DACS II and the SLC Carrier RT. The protection switching can be activated autonomously in response to a facility or equipment failure detected on either end (that is, at the DACS II or RT end). It can also be activated by manual request (craft) initiated from either end. The protection switching activity is controlled by the software and requires data link message exchanges on one of the 1544 kbit/s between DACS II and the RT.

Dependent on the data link used by the SLC Carrier System, the protection switching performance is different.

TR08 Compatible SLC Carrier Interface

A DACS II TR08 compatible SLC Carrier RT interface consists of up to four primary digroups referred to as the A, B, C, and D digroups and provides an optional spare digroup, P, that is automatically switched to when one of the regularly used digroups fails. The TR08 SLC Carrier Mode I interface has a one-for-four protection arrangement, while the Mode III interface provides one-for-two protection (for the A and C digroups). The protection digroup is always

powered up and carries a live signal that under normal operating conditions is the same as the signal on digroup A including the Fs' framing and data link bits. The protection line switch can be initiated from either the DACS II or the RT.

Table 7-3 specifies the TR08 SLC Carrier interface protection switching performance. The performance data for Digroups B, C, and D are grouped due to the fact that the same protection switching protocols and procedures are used for these digroups.

Table 7-3. DACS II TR08 SLC® Carrier Interface Protection Switching Performance

Initiated From	Method	Type	Digroup	Nominal Switching Time (in ms)
DACS II	Manual	Switch	DGA	12.2
		Unswitch	DGA	14.0
		Switch	DGB/C/D	7.0
		Unswitch	DGB/C/D	7.2
	Failure	Switch	DGA	511.5
		Unswitch	DGA	31.5
		Switch	DGB/C/D	704
		Unswitch	DGB/C/D	707.5
RT	Manual	Switch	DGA	0.0
		Unswitch	DGA	0.0
		Switch	DGB/C/D	7.1
		Unswitch	DGB/C/D	549
	Failure	Switch	DGA	9268
		Unswitch	DGA	5581
		Switch	DGB/C/D	980
		Unswitch	DGB/C/D	1378

SLC Series 5 Carrier System FPC Interface

Table 7-4 specifies the SLC Series 5 Carrier System FPC protection switching performance.

Table 7-4. DACS II SLC Series 5 Carrier System Interface Protection Switching Performance

Initiated From	Method	Type	Digroup	Nominal Switching Time (in ms)
DACS II	Manual	Switch	DGA	185
		Unswitch	DGA	0.0
		Switch	DGB/C/D	202
		Unswitch	DGB/C/D	0.0
	Failure	Switch	DGA	1866
		Unswitch	DGA	1
		Switch	DGB/C/D	1162
		Unswitch	DGB/C/D	2
RT	Manual	Switch	DGA	207
		Unswitch	DGA	0.0
		Switch	DGB/C/D	191
		Unswitch	DGB/C/D	3
	Failure	Switch	DGA	1750
		Unswitch	DGA	0.0
		Switch	DGB/C/D	1000
		Unswitch	DGB/C/D	0.0

Software Protection and Data Transfer Performance

DACS II Release 8.0 provides protection for the executable software code and data base by using hardware parity bits and software checksums. In addition, all data is duplicated on the system's nonvolatile Memory Cards. The socket location of the primary nonvolatile backup Memory Card (PMEM) is accessible by removing the CPU2 circuit pack from the frame. The socket for the secondary backup Memory Card (SMEM) is located on the faceplate of the CPU2 ciruit pack. In the event of loss of data in the operating memories (RAM), the system is rebooted from the Memory Cards.

Table 7-5 shows DACS II Release 8.0 data transfer and system reset performance. The timing specified is for a fully provisioned and cross-connected 16-unit CEF equipped with 8 IFTUs, 4 DSPUs, and 4 DS3Us. The execution time is measured from the time the termination character is entered or the frame reset button is pushed, to the time the first character of the completion message is output.

Table 7-5. DACS II Release 8.0 Data Transfer and System Reset Performance

Operation	Nominal Execution Time (min)
Disk to Tape data base transfer	30.55
Tape to Disk data base transfer	18.08
Restore MC (Cold Boot)	7.45
System Reset (Cold Boot)	23.29
Boot Frame (Warm Boot)	3.39

System reset, also known as cold boot, is defined as a manual reset of the DACS II, which results in all controllers being reset, downloading of the data bases and software executables from the Memory Card, and a rewrite of the hardware with the data base information. Boot frame, also known as warm boot, does not require code downloading.

Cross-Connect Capability and Performance

8

Contents

Cross-Connect Capability and Performance

8

Overview

DACS II Release 8.0 provides its cross-connect capability by employing the duplicated ECCN. A fully equipped 7-bay DACS II frame, which supports 16 units, has an ECCN with a 65,536×65,536 switch matrix. The ECCN is fully duplicated for reliability and is fully nonblocking for any equipment configuration or cross-connect type. The ECCN and the digital signal terminating and processing circuitry maintain byte integrity for all DS0 signals cross-connected. That is, each DS0 signal experiences the same number of frame delays.

Supported Cross-Connect Types

DACS II performs several types of DS0 (64 Kbit/s), N×64 kbit/s, Clear-1544 kbit/s, and Clear-2048 kbit/s cross-connections. The circuit types include:

- 2-way, 2-point cross-connections
- 1-way, 2-point cross-connections
- Multipoint broadcasts with selectable return path
- Multipoint, 1-way broadcast.

In addition, a DACS II frame equipped with the DMB circuit pack supports the following two DS0 multipoint bridging cross-connect types:

- Symmetrical multipoint bridging
- Data polling multipoint bridging.

Note that DMB and virtual circuits are not applicable to Clear-1544 kbit/s and Clear-2048 kbit/s cross-connections.

Finally, a DACS II frame equipped with the SRM and MJU circuit packs provides cross-connections and multipoint junctions of the standard DDS data rates (2.4, 4.8, 9.6, 56 kb/s).

For additional details and allowed options, please refer to the documentation listed in the beginning of this document.

Cross-Connect Execution Time

The time required to complete a cross-connection depends on many factors, including:

- The type of cross-connection specified
- Other activities occurring in the DACS II
- The bit rate of the administrative links
- The service status of the equipment
- The existence of previous, conflicting cross-connections.

Tables 8-1 through 8-5 specify DACS II Release 8.0 cross-connect and disconnect performance with the following assumptions:

- All required equipment is in-service.
- There are no conflicting cross-connections.
- DACS II is not currently executing any other command.
- There are no other input messages in queue.
- DACS II MML language is used.

The cross-connect execution times specified do not include input/output times for the cross-connect command on the administrative link. They are defined as from the time at which the DACS II CI/ECI/HECI controller detects a carriage return to the time at which the CI/ECI/HECI controller begins to send out the first output character. The completion of the cross-connection/disconnection occurs earlier.

Table 8-1. Two-point DS0 Cross-Connect/Disconnect Execution Time

Number of DS0s	Cross-Connect Type	Nominal Execution Time (in ms)
Single DS0	2-way, 2-point Cross-Connect	422
	2-way, 2-point Disconnect	1281
	1-way, 2-point Cross-Connect	415
	1-way, 2-point Disconnect	1297
	Terminate and Leave Active	309
	Terminate and Leave Released	294
24 DS0s	2-way, 2-point Cross-Connect	863
	2-way, 2-point Disconnect	1698
	1-way, 2-point Cross-Connect	710
	1-way, 2-point Disconnect	1641
	Terminate and Leave Active	695
	Terminate and Leave Released	505

Table 8-2. DMB Cross-Connect/Disconnect Execution Time

DMB Leg Type	Cross-Connect Type	Nominal Execution Time (in ms)
Symmetrical Leg	Cross-Connect	560
	Disconnect	360
Data Polling Backbone Leg	Cross-Connect	545
	Disconnect	1346
Data Polling Tributary Leg	Cross-Connect	562
	Disconnect	1370

Note that the DMB does not support DS0 ranges and the numbers specified are the times used to establish a DS0 leg. The time required to establish a whole conference is dependent on the number of legs needed.

Table 8-3. Clear-1544 kbit/s Cross-Connect/Disconnect Execution Time

Cross-Connect Type	Nominal Execution Time (in ms)
2-way, 2-point Cross-Connect	689
2-way, 2-point Disconnect	756
1-way, 2-point Cross-Connect	559
1-way, 2-point Disconnect	558
Broadcast, Cross-Connect	1003
Broadcast, Disconnect	1904

Table 8-4. Clear-2048 kbit/s Cross-Connect/Disconnect Execution Time

Cross-Connect Type	Nominal Execution Time (in ms)
2-way, 2-point Cross-Connect	1387
2-way, 2-point Disconnect	1397
1-way, 2-point Cross-Connect	941
1-way, 2-point Disconnect	923
Broadcast, Cross-Connect	1816
Broadcast, Disconnect	2513

Table 8-5. Subrate Cross-Connect/Disconnect Execution Time

Subrate Circuit Type	Cross-Connect Type	Nominal Execution Time (in ms)
-	Channel Establish	395
2-point	Cross-Connect	358
2-point	Disconnect	368
Multipoint	Cross-Connect	878
Multipoint	Disconnect	1809

Test Access

9

Contents

Test Access

9

Overview

DACS II provides test access for subrate, DS0, Nx64 kbit/s, Clear-1544 kbit/s and Clear-2048 kbit/s circuits passing through the system. The access of subrate and 2-point DS0 circuits is provided via the Test Access Digroups (TADs) called NPCs for Test Ports (NPCTPs). For 2-point and broadcast Nx64 kbit/s circuits, test access is supported by TADs called NPCs for Test Groups (NPCTGs). Test access of clear 1544 kbit/s and 2048 kbit/s is provided via Facility Access Digroups (FADs).

An NPCTP has 12 DS0 Test Ports (TPs), each consisting of a pair of DS0 channels. DACS II Release 8.0 supports up to eight NPCTPs for a total of 96 TPs. Each DACS II frame supports up to 400 NPCTGs, which can be used to provision up to 400 Test Groups (TGs) for Nx64 kbit/s test access. Each TG can be provisioned for a particular bandwidth N, where N can be from 1 up to 24 (or 31 for CEPT TGs). NPCTPs, NPCTGs, TPs and TGs are predesignated. FADs are non-channelized digroups/facilities used for clear-1544 kbit/s and clear-2048 kbit/s test access. FADs are not predesignated and can be set up on a need basis; the number of FADs on a DACS II is limited by the number of available non-channelized 1544 kbit/s or 2048 kbit/s signals on a frame.

Test Access Types

DACS II provides the following test access modes:

- Monitor
- Split
- Hub
- Terminated
- Looped TAD or loopback of FAD.

For details and allowed options, see the Lucent Technologies DACS II Command and Message Manuals.

Test Access Execution Time

The time required to complete a test access depends on many factors. These factors include:

- The type of circuit being accessed
- Other activity occurring in the DACS II
- The bit rate of the administrative links
- The service status of the equipment
- The existence of previous, conflicting test connections.

The test access execution times shown in Tables Y through AC apply to access of existing 2-way, 2-point DS0 cross connections; 2-way, 2-point non-channelized cross connections; 2-way, 2-point subrate cross connections; and, 2-way multipoint subrate connections between two 1544 kbit/s signals with the following assumptions:

- All required equipment is in-service.
- There are no conflicting test connections.
- DACS II is not currently executing any other command.
- There are no other input messages in queue.
- DACS II MML message is used.

The time numbers do not include input/output times for the Test Access command on the administrative link. They are defined as from the receipt of the input command termination character by the CI/ECI/HECI to the the outputs of the first character in the command completion message. Completion of the test access connection occurs earlier.

Table 9-1. DACS II DS0 Test Access Execution Time

Access Type	Action	Nominal Execution Time (ms)
MONITOR	Activate	320
	Release	302
SPLIT	Activate	286
	Release	346
TERMINATE AND LEAVE ACTIVE	Activate	240
	Release	250
TERMINATE AND LEAVE RELEASE	Activate	237
	Release	252

Table 9-2. Nx64 kbit/s Test Access Execution Time

Access Type (N = 1)	Action	Nominal Execution Time (ms)
MONITOR	Activate	528
	Release	683
SPLIT	Activate	680
	Release	859
Access Type (N = 24)	**Action**	**Nominal Execution Time (ms)**
MONITOR	Activate	1662
	Release	1834
SPLIT	Activate	2374
	Release	3275
Access Type (N = 30)	**Action**	**Nominal Execution Time (ms)**
MONITOR	Activate	2005
	Release	2221
SPLIT	Activate	2962
	Release	4068

Table 9-3. DACS II Clear-1544 kbit/s Test Access Execution Time

Access Type	Direction/End	Action	Nominal Execution Time (ms)
MONITOR	One End	Activate	1381
		Release	1433
	Both Ends	Activate	1536
		Release	1626
SPLIT	One Direction	Activate	1880
		Release	1687
	One End	Activate	1909
		Release	1701
	Both Directions	Activate	2417
		Release	2100
	Both Ends	Activate	2498
		Release	2165
LOOP	One End	Activate	2038
		Release	1914
LOOP FAD	One FAD	Activate	1468

Table 9-4. DACS II Clear-2048 kbit/s Test Access Execution Time

Access Type	Direction/End	Action	Nominal Execution Time (ms)
MONITOR	One End	Activate	1675
		Release	1596
	Both Ends	Activate	2031
		Release	1909
SPLIT	One Direction	Activate	2285
		Release	1947
	One End	Activate	2265
		Release	1986
	Both Directions	Activate	3249
		Release	2601
	Both Ends	Activate	3430
		Release	2587
LOOP	One End	Activate	2443
		Release	2331
LOOP FAD	One FAD	Activate	1696

Table 9-5. DACS II Subrate Test Access Execution Time

Access Type	Access Point	Action	Nominal Execution Time (in ms)
MONITOR	SRM/MJU	Activate	403
		Release	426
SPLIT	SRM/MJU	Activate	426
		Release	500
Note: All access points are DS0B.			

Service Reconfiguration

10

Contents

Service Reconfiguration

10

Overview

DACS II Release 8.0 offers these functions for service reconfiguration: Alternate Map, Alternate Cross-Connect (ACON), DS0 Roll, 1544 kbit/s, and 2048 kbit/s Roll. The DS0 Roll feature also works for DS0A and DS0B circuits carrying subrate circuits.

Alternate Map Outage Time

The Alternate map outage time is measured from the time the existing cross-connection is disconnected to the time the new cross-connection is established. Table 10-1 lists the alternate map outage time.

Table 10-1. DACS II Release 6.0 Alternate Map Outage Time

Alternate Map Size (Two-way DS0s)	Outage Time (in ms)
24	786
72	1898
120	3617

ACON Outage Time

Table 10-2 lists the Alternate Cross-Connect (ACON) function service outage time.

Table 10-2. DACS II Release 8.0 ACON Outage Time

Circuit Type	Outage Time (in ms)
Two-way, two-point	11
Broadcast Leg	162
Virtual Leg	0.0
DMB Leg	0.0

Subrate Roll Outage Time

DACS II Release 8.0 supports switching of a subrate DS0-B channel to an alternate DS0-B channel with less than 60 ms of outage time. The actual measured outage time for a DS0-B is 0.5 ms.

DS0 Roll Outage Time

In DACS II Release 8.0, receive points of an NxDS0 circuit can be switched to alternate receive points with less than 1 ms of outage time. The actual outage time measured for N from 1 to 12 (bandwidth from 56Kbit/s to 768Kbit/s) is 0.0 ms.

1544 kbit/s Roll Outage Time

In DACS II Release 8.0, a 1544 kbit/s circuit receive point can be switched to an alternate receive point with measured outage time of 4.6 ms, or maximum outage time of 25 ms.

Administrative Interfaces

11

Contents

Administrative Interfaces

11

Administrative Link Options

The following DACS II circuit packs are available to provide user options regarding the physical and electrical interfaces of the administrative links:

- Enhanced Communications Interface (TM736C-ECI).
- High-speed ECI (TM762-HECI)

The Enhanced Communications Interface (TM736C-ECI) circuit pack provides two synchronous X.25 links and four asynchronous administrative links, two of which are Snider links and two of which may be programmed independently as either Snider or TABS links. The physical and electrical interface of the asynchronous Snider and synchronous links conforms to EIA Standard RS-449/423 using fixed waveshaping with a nominal risetime of 10 microseconds. The maximum usable cable length shall not exceed 2000 feet at a transmission rate of 1200 b/s, or 400 feet for transmission rates of 9.6 kb/s. The maximum baud rate supported by the ECI pack is 9.6k b/s, for the synchronous and asynchronous links. The electrical interface of the TABS links conforms to inverted EIA Standard RS-485.

The High-speed ECI (TM762-HECI) circuit pack is capable of providing two synchronous X.25 links and four asynchronous links, with the same combinations as those for the ECI pack. The HECI synchronous links are EIA RS-423 compliant for transmission rates 19.2k baud and up to 56k baud, with nominal risetime of 4.4 microseconds, and maximum cable length of 400 feet. HECI RS-423 asynchronous links have maximum transmission rate of 9.6k baud, with nominal risetime of 4.4 microseconds, and maximum cable length of 400 feet. The TM762 circuit pack is compatible with the ECI circuit pack for cable length of 400 feet or less.

Asynchronous Administrative Links

Physical and Electrical

DACS II provides two types of asynchronous administrative links: Snider links designed with a physical interface according to EIA Standard RS-449 and an electrical interface according to EIA Standard RS-423, and TABS links designed with a physical interface according to EIA Standard RS-449 and an electrical interface according to inverted EIA Standard RS-485.

For the RS-449/423 interfaces, optional passive adapters are available to work with equipment operating according to the following specifications:

- RS-232C DTE
- RS-232C DCE
- RS-423 (twisted pair) - data only connections to DACS II
- CIU - for SLC Series 5 Carrier System feature package C (FPC) remote provisioning.

In the case of RS-423 data only connections to DACS II, this configuration provides only two pairs of signal connections to the DACS II SEND DATA and RECEIVE DATA leads.

Terminal Requirements

Any terminal having the following features is acceptable for communicating with the DACS II equipment, either locally or remotely via suitable modems:

- EIA RS-449 or RS-232C interface with full duplex operation
- ASCII characters (10 bits) with even parity (7 data bits, 1 start bit, 1 stop bit, and 1 parity bit)
- 300, 1200, 2400, 4800, and 9600 baud asynchronous operation.
- Responds with ASCII "ACK" when it receives an ASCII "ENQ" character. DACS II asynchronous Snider links implement the ENQ/ACK communication protocol, provisionable on a per-link basis, with 'enabled' as the default selection.

  If the connecting terminal does not respond to DACS II "ENQ" characters, communication between DACS II and the terminal is still possible. However, all DACS II command responses, other than echoes and immediate responses to commands, will be delayed by 2 seconds after an initial delay of 24 seconds. This 2-second delay on the asynchronous links is caused by ENQ/ACK protocol requirements. The delay may cause the output buffer in the DACS II to fill, slowing down responses on

other DACS II administrative links as well.

- A terminal has the option to employ the XON/XOFF flow control protocol on DACS II asynchronous Snider links, to temporarily suspend DACS II output messages. This option is provisionable on a per-link basis for Snider links, and the default selection is 'disabled'.

  The connection terminal may send DACS II an XOFF ASCII character "DC3" (hexadecimal value 0x13 or CTRL-S), and DACS II will suspend its output for up to 60 seconds. The terminal may send an XON ASCII character "DC1" (hexadecimal value 0x11 or CTRL-Q), prior to the 60-second time limit to resume transmission. If an XON is not received after 60 seconds, DACS II will resume transmission automatically. Additional XOFF characters may be sent by the terminal to continue output control. XON/XOFF may only be used while a link is in output mode.

Modem Requirements

The recommended method for administering DACS II frames remotely is via dedicated private line data circuits. For operation over 1200 b/s (asynchronous analog circuits), the recommended modem is a Lucent Technologies 202T type or equivalent with the following features:

- Asynchronous, binary, serial, full-duplex operation
- EIA RS-449 or RS-232C interface
- 4-wire private line operation
- 1200 b/s data rate without line conditioning
- Clear-to-send delay of 8 ± 0.3 ms
- Carrier detection:

  Operate = 6.9 ± 0.4 ms

  Release = 5.0 ± 0.5 ms

- Soft carrier turn-off: 8 ± 0.4 ms
- Received data is clamped when received line signal is off.

Synchronous Administrative Links

Packet Assembler/Disassembler Requirements

Any packet assembler/disassembler (PAD) having the following features is acceptable for communicating with the DACS II:

- EIA RS-449 or RS-232C interface
- 300, 1200, 2400, 4800, 9600 b/s operation, or 56 kb/s, 65 kb/s with the HECI pack.

Direct connection to a PAD is supported with a passive modem eliminator.

Packet Network Interface Requirements

The recommended method for administering DACS II frames remotely is via dedicated private line circuits. The modem must have the following features:

- Synchronous, binary, serial, full-duplex operation
- EIA RS-449 or RS-232C interface
- 4-wire private line operation
- Received data is clamped when received line signal is off.

Access Security and Screening

DACS II Release 8.0 provides the following link/user access security and screening feature for applications where it is necessary to administer the system over a public network:

- Input Command Restriction

  DACS II input commands are categorized into seven functional groups. Different privileges of entering commands of a particular group are assignable to each link, VC, or user. A command is denied if it is entered from a link/VC/user without the correct privilege.

  By setting the appropriate input privileges, access to the administrative links or VCs can be restricted. With the restriction, the link can be accessed only if valid user identification and password are entered.

- Output Message Screening

  DACS II provides an output screening feature so that a message of a specific function group will only be generated to the links/VCs/users with the correct screening privilege. This feature can also be used to avoid the receipt of unwanted outputs.

Security Warning Notice

DACS II provides a feature package to output a security warning notice once a user is logged in, along with the log-in completion message.

Manual Interface

DACS II provides the following indicators and controls for local maintenance.

Status Panel:

- LEDs indicating the alarm state of the system
- Alarm Cutoff (ACO) switch to silence local audible alarms, with LED display
- System reset switch and reset enable switch
- A local appearance of administrative link No. 1 for temporarily connecting a maintenance terminal
- Lamp test switch.

Power and Fusing:

- LEDs on power units
- Indicator fuses
- Power alarm lamps.

Message Logging (MML only)

Messages are reported over the administrative links. If an administrative link goes down, messages could be lost. With the Message Logging feature, messages will be logged at the DACS II so that they can be retrieved by the network management system at a later time.

When the feature is turned ON, all autonomous messages and output messages of all commands which affect the system database will be logged. Each message will be stored with a sequence message log number in a "circular" buffer which is large enough to hold 2000 messages. The message log number will be set to 1 whenever the feature is turned ON or the DACS II frame is initialized (warm boot or cold boot) or the user issues an input command to clear the message log. To retrieve these logged messages, the user will use an administrative input command.

The network management system can identify the last valid message that was received from the DACS II prior to the link outage. When the link comes back up, the network management system can then query for the messages that were collected and stored in the DACS II frame since the link went down. The message retrieval can be aborted with no effect on the buffer contents.

This feature requires that requested logged messages be output in blocks with "start" and "end" indicators. All messages sent in between the "start" and "end" indicators are logged messages only. The priority output messages can still be sent with higher priority over a block of messages, but must not interrupt the sending of the block. This block is treated as a complete unit.

Power and Battery

12

Contents

Power and Battery

12

Overview

DACS II is designed to operate from a nominal -48 V dc central office battery plant. Power is delivered by four feeders (A, B, C, D) which are separately fused. Side-0 entities (for example, side-0 Synchronizer Power Unit (0SPU)), are fed by A or B distributions, while Side-1 entities are fed by C or D distributions. Thus, if one of the four frame feeders should fail, transmission is maintained.

Power for low voltage circuits is obtained from power converter units in the DACS II frame. Low voltage fusing and distribution are provided as part of the factory supplied wiring.

Primary Power Supply Limits

DACS II Release 8.0 primary power supply limits are shown in Table 12-1.

Table 12-1. DACS II Release 8.0 Primary Power Supply Limits

CONDITION	LIMITS
Normal Input Operating Voltage	Wide range power -36 - -72 VDC
Generated Ripple	100 mV peak-to-peak at full load from DC to 20 MHz
Generated Noise	Meet FCC Subpart J of Part 15 Class A and CE mark (ESBF/ECEF only) Requirement for Radiated and Conducted Emissions

Common Equipment and Unit Power Consumption

Table 12-2 specifies the power consumptions of DACS II Expanded Frame Controller (EFC), ECCN, IFTU, DS3U, and DSPU shelves.

Table 12-2. DACS II Release 8.0 Unit Power Consumptions

UNIT TYPE	TOTAL POWER (WATTS)
Expanded Frame Controller (EFC)	150
Expanded Cross-Connect Network (ECCN)	24 x (1 + # of units) = 408 max
FTU w/ Series 6, 7 TG80Bs	180
IFTU and DS3U	180
DSPU	180

The numbers are average numbers for fully equipped units. To determine the total power dissipation of a DACS II frame simply add the power consumption of the frame controller, CCN or ECCN, and all units. For example, a fully loaded CEF frame has 16 units, its total power consumption is:

EFC: 150 Watts
ECCN: 24(1+16)= 408 Watts
Units: 180x16 = 2880 Watts

Total: 3438 Watts

Power Failure Indicators

In the event of a failure in one of the low voltage power converters, a red light emitting diode (LED) is illuminated on the failed unit and an alarm message is transmitted over the administrative links. In addition, summary alarm indications are sent to the office audible and visual alarm systems and to remote systems. DACS II also uses indicator fuses and power alarm lamps to indicate failures.

Power-on Indicator

A green LED is provided on the faceplate of the DS3U power units as a power-on indicator.

Power Protection

DACS II Release 8.0 provides an orderable option for dual power feeders, the redundancy provides added protection against transmission failure. In this arrangement dual feeders are wired OR together via diodes, A1 with A2, B1 with B2, C1 with C2, and D1 with D2.

Physical Specifications

13

Contents

Physical Specifications

13

Frame Types

DACS II Release 8.0 frames are available in either Network Bay Frame (NBF) or enclosed frame constructions. Release 8.0 software also supports existing Electronic Switching System (ESS) bays for certain configurations.

The dimensions of a NBF bay are:

HEIGHT: 2133mm (7' 0'').

DEPTH: 330mm (1' 1'') (368mm or 1' 2.5'' for retrofit CEF frame).

WIDTH: 660mm (2' 2'').

MINIMUM FRONT AISLE: 711mm (2' 6'')

MINIMUM REAR AISLE: 584mm (1' 11'') (546mm or 1'9.5'' for retrofit CEF frame).

The dimensions for an enclosed bay are:

HEIGHT: 2200mm (86.6''), extendable to 2600mm (102.3'').

DEPTH: 600mm (23.6''), including front and rear doors, hinges and handles.

WIDTH: 600mm (23.6'').

OPEN DOOR: 150mm (5.9'') fully opened; 343mm (13.5'') at 90-degree angle.

MINIMUM FRONT AISLE: 711mm (2' 6'')

MINIMUM REAR AISLE: 711mm (2’ 6’’)

The enclosed bays are Electromagnetic Compatibility (EMC) Compliant, and meet CE mark standards.

Frame Configurations

DACS II Release 8.0 supports these frame configurations:

- Single Bay Frame (SBF): one NBF bay, up to 2 units.
- Capacity Expansion Frame (CEF): 2 to 7 bays of NBF type, up to 16 units.
- Non-CEF: 2 or 3 bays of NBF type, up to 6 units, (not orderable, software support only).
- Non-CEF: 2 or 3 bays of ESS type, up to 6 units, (not orderable, software support only).
- Enclosed SBF (ESBF): one enclosed bay, up to 2 units.
- Enclosed CEF (ECEF): 2 to 7 enclosed bays, up to 16 units.

For each unit of CEF, ESBF and ECEF frames, DACS II Release 8.0 will support any of these unit types in any position: Integrated Facility Terminating Unit (IFTU), DS3 Unit (DS3U), Hybrid DS3 Unit, and Digital Signal Processing Unit (DSPU). SBF, non-CEF and retrofitted frames have some restrictions on the unit types in certain positions.

Shipping Dimensions

Three standard DACS II shipping dimensions are specified: two bays (one Switch Bay and one Flexible Interface Bay), one bay (one Flexible Interface Bay) and one enclosed bay. The two-bay package is shipped vertically, the one-bay packages are shipped horizontally on their sides. Table 13-1 summarizes the dimensions.

Table 13-1. DACS II Release 8.0 Shipping Dimensions

CAPACITY	HEIGHT	WIDTH	DEPTH
Two Bays (Not enclosed)	2362mm (93’’)	1625mm (64’’)	1117mm (44’’)
One Bay (Not enclosed)	863mm (34’’)	2286mm (90’’)	736mm (29’’)
One Bay (Enclosed)	850mm (33.5’’)	2500mm (98.5’’)	850mm (33.5’’)

Installed Weight and Shipping Weight

Table 13-2 specifies the maximum installed weight and shipping weight, for one and two fully equipped DACS II bay(s):

Table 13-2. DACS II Release 8.0 Frame Weight

EQUIPAGE	INSTALLED WEIGHT*	SHIPPING WEIGHT
Two-Bay (Not enclosed)	800 lbs.	1100 lbs.
One-Bay (Not enclosed)	400 lbs.	500 lbs.
One-Bay (Enclosed)	750 lbs.	1100 lbs.
* Installed weight is less external cables.		

Environmental Specifications

14

Contents

Environmental Specifications

14

Temperature and Humidity

DACS II Release 8.0 Enclosed frames are compliant with the ETS 300 019-2-3, part 3 and 3E standards, and the Bellcore NEBS requirements, GR-63-CORE, Issue 1, for transportation/storage extremes in temperature and humidity.

DACS II operates under the ambient temperature and humidity conditions shown in Table 14-1 (GR-63-CORE, Issue 1). These ambient conditions are measured at a location 5 feet above the office floor and 15 inches in front of the equipment. Limits are shown for both normal and long-term conditions. Short-term is defined as no longer than 72 consecutive hours and no more than 15 total days in one year. The maximum rate of temperature change is 15˚F per hour.

Table 14-1. DACS II Operating Temperature and Humidity Limits

OPERATING TEMPERATURE AND HUMIDITY LIMITS		
CONDITION	**NORMAL LIMITS**	**SHORT-TERM LIMITS**
Ambient Temperature	40˚F to 104˚F	23˚F to 122˚F
Ambient Humidity	5% to 85%	5% to 90% but not to exceed 0.024 kg of water/kg of dry air.

Handling, Transportation, and Office Vibration

During transportation, DACS II will withstand shock, vibration, and temperature

and humidity conditions as specified by the Bellcore TR-NWT-000063 NEBS requirements documents.

DACS II Enclosed frames suffer no damage and degradation to performance when subjected to the transportation vibration test and drop-distance test specified in Section 5.4.4 Test 4 of TR-NWT-000063.

Electrostatic Discharge (ESD)

DACS II Release 8.0 Enclosed frames suffer no equipment damage and no network service-affecting failures exceeding one errored second of transmission, when subjected to 4 kv or 15 kv Electrostatic Discharge (ESD) with the direct air discharge test setup specified by IEC Standard, "Electromagnetics Compatibility for Industrial Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements," 801-2, Second edition, 1991-04.

Electromagnetic Interference (EMI)

The DACS II Release 8.0 ECEF and ESBF meet these EMI standards: EN 55022 - ETSI Class A, Bellcore TR-NWT-001089, and FCC Class A.

DACS II Release 8.0 CEF meets the EMI specifications described in the remaining subsections.

Radiated Emission

The compliances of DACS II CEF to the Bellcore TR-EOP-000063 and NEBS PUB 51001 requirements for the emission of electromagnetic radiation are detailed below:

- Electric Fields
  - — Frequency range from 10 KHz to 30 MHz:

    Within this range, the radiated emission performance of DACS II CEF is compliant with the Bellcore criteria specified in TR-EOP-000063, Issue 3, except for the emissions at 24.59 MHz.
  - — Frequency range from 30 MHz to 220 MHz:

    Within this range, the radiated emission performance of DACS II CEF was measured to be above the FCC Class A emission objectives by at most 23.4 dB at 164.4 MHz.
  - — Frequency range from 200 MHz to 1000 MHz:

Within this range, the radiated electric field emission performance of DACS II CEF was above the FCC Class A emission objectives by at most 16.1 dB at 459.2 MHz.

— Frequency range form 1 GHz to 10 GHz:

Within this range, the radiated emission performance of DACS II CEF is fully compliant with Bellcore emission criteria specified in TR-EOP-000063, Issue 3.

- Magnetic Fields

  The DACS II CEF radiated emission measurements for "Magnetic Fields" 60 Hz to 30 MHz are fully compliant with Bellcore TR-EOP-000063, Issue 3, criteria with a minimum of a 3.9 dB margin.

Conducted Emission

DACS II CEF conducted emission performance from 10 KHz to 100 MHz is fully compliant with Bellcore TR-EOP-000063, Issue 3, criteria for the following leads:

- T1 signal leads DS3 shield cables
- Remote reset lead
- Remote alarm leads
- Local alarm leads
- Timing extraction leads
- Timing distribution leads.

Except for the Feeder C lead, DACS II CEF conducted emission performance on the DC power leads is also compliant with the Bellcore criteria.

Radiated Susceptibility

The compliances of DACS II CEF to the Bellcore TR-EOP-000063 NEBS objectives for the radiated susceptibility are detailed below:

- Electrical Susceptibility

  — Frequency range from 10 KHz to 180 MHz:

  DACS II CEF is fully compliant with Bellcore TR-EOP-000063 performance criteria when subjected to a radiated electric field with a 10 V/m intensity.

  — Frequency range from 180 MHz to 1000 MHz:

DACS II CEF is fully compliant with Bellcore TR-EOP-000063 performance criteria when subjected to a radiated electric field with a 5 V/m intensity.

— Frequency range from 1 GHz to 10 GHz:

DACS II CEF is fully compliant with Bellcore TR-EOP-000063 performance criteria when subjected to a radiated electric field with a 10 V/m intensity.

- Magnetic Susceptibility

DACS II CEF is fully compliant with Bellcore TR-EOP-000063 performance criteria when subjected to a magnetic field with intensity H = *50 - 20 log f*, from 60 Hz through 30 KHz on the front and rear surfaces of the frame.

Conducted Susceptibility

When DACS II CEF power leads are subjected to common mode noise from 10 KHz to 350 KHz, power feeders B and D meet Bellcore TR-EOP-000063 performance objectives; however, power feeders A and C do not. When subjected to common mode noise from 350 KHz to 100 MHz, all four power feeders meet the Bellcore performance objectives.

DACS II CEF T1 signal leads are not affected by the common mode noise for the frequency range from 10 KHz to 100 MHz and are compliant with the Conducted Immunity Objectives given in Bellcore TR-EOP-000063, Issue 3.

Fire Resistance and Flammability

All components of DACS II Release 8.0 CEF/ECEF/ESBF have an oxygen index of 28% or greater as determined by the American Society for Testing and Materials (ASTM) Standard D2863-77, *Standard Method for Measuring the Minimum Oxygen Concentration to Support Candle-like Combustion of Plastics (Oxygen Index)*, and a 94 V-1 or better rating as determined by Underwriters Laboratories (UL) Standard 94, *Test for Flammability of Plastic Materials for Parts in Devices and Appliances*, in the paragraph titled: "Vertical Burning Test for Classifying Material 94 V-0, 94 V-1, or 94 V-2.

Underwriters Laboratories Listing

DACS II Release 8.0 CEF meets the Underwriters Laboratories (UL) safety standards listed under section 1459, second edition, which states the safety standards for telephone equipment in a dedicated equipment room.

UL 1459 & 1950 and IEC950/EN60950 certifications have been approved for DACS II Release 8.0 ECEF/ESBF.

System Reliability

15

Contents

System Reliability

15

Overview

Table 15-1 provides a summary of the hardware downtime estimates calculated for the DACS II Release 8.0 frames. These downtime estimates are calculated for a DACS II equipped with 16 fully loaded units (maximum configuration). The configuration consists of eight IFTUs, six DS3Us, and two DSPUs.

A 2-hour Mean Time To Repair (MTTR) interval is assumed which includes the dispatch time, diagnostic time, repair time, and time to restore the system back to its original state. The unavailability per 1544 kbit/s/2048 kbit/s port is the amount of time that a given customer of the 1544 kbit/s/2048 kbit/s port is unable to transmit or receive signals through DACS II. It is calculated by summing the downtime contribution for each failure mode that affects a given 1544 kbit/s/2048 kbit/s port. The protection switching capability of the SLC Carrier interface was included in the calculation for the unavailable time of a SLC Carrier 1544 kbit/s port. The unavailability per DS3 port is the amount of time that a given customer of the DS3 port is unable to transmit or receive signals through DACS II.

Table 15-1. DACS II Release 8.0 System Reliability Estimates

PARAMETER	DACS II RELEASE 8.0 ESTIMATE (minutes/year)
Unavailability Per 1544 kbit/s/2048 kbit/s Port	
DDC/DPC PORT (Non-SLC® Carrier)	1.72
SLC 96 Carrier MODE I	0.039
SLC 96 Carrier MODE III	0.039
SLC Series 5 Carrier System FPC	0.039
Unavailability Per DS3 Port	0.053
Total System Outage	0.022

The steady-state failure rate predictions for all circuit packs used in DACS II Release 8.0 are given in Table 15-2. The basis for steady-state failure rate predictions for each circuit pack is Bellcore TR-NTW-000332, "Reliability Prediction Procedures for Electronic Equipment (RPP)," Issue 4, September 1992. The circuit pack estimates are based on Method I (Parts Count Method) with a 40°C operating temperature and a 50% electrical stress.

Table 15-2. DACS II Release 8.0 Circuit Pack Failure Rates

Code	Name and Function	FIT Rate (failures/10^9 hrs)
BBR1	Bus Terminator (BT)	100
BBS1	Clock & Control Interface (CCI)	4,100
BBS2	Expanded Time Slot Interchanger (ETSI)	2,700
KCR1	Multiplexer (MXR)	4,500
KCR4	Facility Line Interface (FLI)	4,100
KCR5	Enhanced Multiplexer (EMXR)	4,500
KCR6	Enhanced MIU (EMIU)	4,300
KCR8	Hybrid Multiplexer (HMXR)	9400
KER1	Formatter (FMT)	3,700
KER2	Unit Controller (UC)	4,400
KER5	Hybrid Formatter (HFMT)	5,300
KER6	New Unit Controller (UC)	3,200
SM565	Main Controller Power	1,000
SM566	DSP Controller Power	800
SM624	Main Controller Power Unit - 60V	1,000
TG58B	Synchronizer Power Unit (SPU)	1,000
TG60B	Stratum 3 (TBS3)	4,400
TG61B	Time Based 2048 kbit/s Local (TBCL)	4,400
TG62B	Time Based 2048 kbit/s Toll (TBCT)	4,400
TG63B	Stratum 2 (TBS2)	4,400
TG64B	Timing Extractor, Bipolar 1544 kbit/s (TXB1)	1,000
TG65B	Timing Extractor, 2Mbit/s 120 ohm (TXB2)	1,000
TG66B	Timing Extractor, Composite Clock (64 kb/s)	1,100
TG67B	Timing Extractor, Unipolar Clock (TXUC)	600
TG68B	Timing Extractor, BSRF Clock (TXRF)	600
TG70B	Timing Distribution, Composite Clock (TDCL)	800
TG71B	Timing Distribution, Sine 2 MHz (TDS2)	600
TG75B	Timing Extractor, 2Mbit/s 75 ohm (TXBT)	1,000
TG79	Format Converter (FC)	400
TG80B	Dual Digroup Circuit (DDC)	700
TG81	Facility Terminating (FTMI)	800
TG97B	Timing Extractor, ITU-T Composite Clock (64Kb/s)	1,100
TG182	Dual Primary Circuit - 120 ohm (DPC)	1,400
TG183	SLC® 96 Carrier DDC (S96D)	700
TG184	SLC Series 5 Carrier System (SS5D)	700
TG185	Dual Primary Circuit - 75 ohm (DPC)	1,400
TG186	Zero Byte TSI Dual Digroup Circuit (ZDDC)	700
TG191	Enhanced DDC - ANSI T1 PM (EDDC)	1,300
TG192	Enhanced DPC - ITU-T PM (EDPC)	2,300
TM590	Digital Phase Locked Loop (DPLL)	2,800
TM657B	Enhanced Central Processor Unit (CPU)	4,100

Table 15-2. (Continued)

Code	Name and Function	FIT Rate (failures/10^9 hrs)
TM658C	Communications Interface (CI)	3,500
TM659C	Secondary Storage Controller (SSC)	3,100
TM665	Digital Multipoint Bridge (DMB)	2,300
TM736C	Enhanced Communications Interface (ECI)	4,200
TM739	Subrate Multiplexer (SRM)	2,600
TM740	Multipoint-junction Unit (MJU)	2,700
TM747	C-Bit Processor (CPR)	2,500
TM778	CPU 2 Central Processor Unit	3,000
UM28	Unit Bus Extender (UBX)	1,000
UM29	Digital Signal Processing Interface (DSPI)	2,300
UM56	Expanded Maintenance Circuit (EMTC)	3,300
UM71	Expanded Bus Extender (EBX) for CEF	5,300
UM72	Expanded Bus Extender (BX2) for non-CEF	3,300
UM75B	Expanded Maintenance Circuit (EMTC-60V)	2,700
411AA	Power Unit (PU)	2900
484GA	Power Unit (PU)	2800
563A	Power Unit (PU)	2000
ED-2C863	DSPU Fuse Board	100
ED-2C980	DS3U Fuse Board	100
ED-9C011	IFTU Fuse Board	100
ED-9C012	IFTU Fuse Board	100
ED-9C015	Disk Drive Assembly (Before Release 7.0 only)	14,100
ED-9C016	Tape Drive Assembly (Before Release 7.0 only)	12,200
ED-9C017	Status Panel Assembly	12,200

Glossary

A

AAC
ACCULINK Access Controller

ABT
Abort

ACO
Alarm Cutoff

Active
For duplicated entities, the entity is providing service rather than operating in hot standby.

AI
Alarm Interface

AIS
Alarm Indication Signal (Also known as all 1s signal)

Alarm Delay
The alarm delay (in seconds) for software-detected alarm conditions. Initial value is 20 seconds.

Alarm Indication Signal (AIS)
A signal transmitted downstream to indicate that network transmission line failures were detected upstream.

All Ones Signal
Another name for DS1 Alarm Indication Signal (AIS).

ALM
Alarm

Alphanumeric Characters
Letters and digits.

Alternate Mark Inversion (AMI)
A DS1 line code in which alternate one bits are positive and negative, but zero substitution is not used.

AMI
Alternate Mark Inversion

ANSI
American National Standards Institute

AS&C
Alarm Surveillance and Control

ASCII Characters
Letters, digits, and symbols used in the American Standard Code for Information Interchange.

ATP
All Tests Passed

AUD
Audit

Autonomous
Done automatically by the system without any manual intervention from the user.

B

B8ZS
Bipolar Eight Zero Substitution

Baud Rate
Transmission data rate (bits per second) on an administrative link.

BBL
Backbone Leg

BCON
Broadcast Cross-Connect

BDIS
Broadcast Disconnect

BER
Bit Error Rate

Bipolar Violation
A violation of the alternating +1, -1 pattern in a 3-level code.

Blue Code
Same as AIS

BMTR
Back-up Memory Transfer

Boot
To transfer contents of a Memory Card into the system's working memory and system hardware. The contents of a Memory Card can include both system software and database.

BOS
Bit Oriented Signaling

BPV
Bipolar Violation

BRD
Broadcast Leg

Broadcast
Form a bridge connection.

Byte
A group of eight binary digits.

C

CAS
Channel Associated Signaling

CATP
Conditional All Tests Passed

CCIS
Common Channel Interoffice Signaling

CCITT
International Telephone and Telegraph Consultative Committee

CCN
Cross-Connect Network alarm condition no longer exists.

CEF
Capacity Expansion Frame

CEPT
Conference Europeene des Postes et Telecommunications

CFA
Carrier Failure Alarm

CGA
Carrier Group Alarm

CHG
Change

Clear
An alarm condition no longer exists.

CMAP
Channel Map

COFA
Change-Of-Frame-Alignment

CP
Circuit Pack

CPU
Central Processing Unit

CRC
Cyclic Redundancy Checking

Cross-Connection
An interconnection between two specified NPC channels.

Crosstalk
A signal induced into one transmission line from another transmission line.

D

DACS
Digital Access and Cross-Connect System

Database
A record of the system configuration and status. It contains cross-connections, status of entities and transmission lines, performance monitoring threshold values and collected data.

DC
Direct Current

DCC
Disconnect Code

Default
A value the system automatically uses for a parameter if you do not specify a value.

Delimiter
A colon, comma, or space used to separate two parameters in a command or message.

Diagnose
Test an entity.

DIF
DACS Interface Module

DL
Data Link

DMA
Deferred Maintenance Alarm

DMAP
Digroup Map

DMI
Digital Multiplex Interface

DND
DACS II Network Director

DOTS
Digital Office Timing Supply

DS0
Digital Signal Level 0 (64-kb/s)

DS1
Digital Signal Level 1 (1.544-Mb/s)

DS1 Data Rate
The DS1 Data Rate is calculated as follows:
DS1 = (24 Channels x 8 bit/sample + 1 frame bit) x 8000 samples/sec
DS1 = 193 x 8000 = 1.544 Mb/s

DSP
Digital Signal Processor

DSU
Data Service Unit

DSX
Digital Signal Cross-Connect

DTAC
Digital Test Access Connector

Duplicated Entity
A pair of entities in which one is active and the other is in hot standby (for example, the Synchronizer Cross-Connect (SXC) circuit packs).

E

E1 Data Rate
The E1 Data Rate is calculated as follows:
E1 = (32 Channels x 8 bit/sample) x 8000 samples/sec
E1 = 256 x 8000 = 2.048 Mb/s

NOTE:
With this data rate, 30 channels carry traffic and two channels are reserved; one channel contains framing information and the other channel contains signaling information.

E2A
Type of Alarm Telemetry

Echo
Display of keystrokes entered from a terminal (passwords are not echoed).

EDDC
Enhanced Dual Digroup Circuit

EDPC
Enhanced Dual Primary Circuit

EER
Excessive Error Rate

EIA
Electronic Industries Association

EMC
Electromagnetic Compatibility

Entity
A specific piece of hardware (such as the Main Controller (MC) or Network Processing Circuit (NPC)) that has been assigned a name and is recognized by the system.

Entity Identifier
The name used by the system to refer to an entity.

Equalizer
A circuit adjustment used to maintain signal strength between desired limits.

Equipped
The entity is entered in the system database via a user provisioning command.

ERS
Errored Seconds

ESD
Electrostatic Discharge

ESF
Extended Superframe

ESR
Error Source Register

ETSI
European Telecommunication Standardization Institute

F

FAS
Frame Alignment Signal

FDL
Facility Data Link

FELP
Far End Loopback

FMAC
Facility Maintenance and Administration Center

FRADT
Frame Audit

FW
Framing Word

H

HDB3
High Density Bipolar 3 Zero Substitution

Header
The first line of a message.

Header Date
Specifies the current date as YYMMDD, where YY is the last two digits of the year, MM is the month, and DD is the day of the month.

Header Time
Specifies the current time of day as HHMMSS, where HH is the hour (00 to 23), MM is the minutes, and SS is the seconds.

Hierarchy
An orderly ranking or sequence of elements, such as that of menus presented at a terminal.

Hit
A disruption of service that lasts for less than 1 second. See Outage.

I

IDLD
Idled

Idle Channel
A channel on an NPC that has not been cross-connected.

In Service
The entity is performing normal service functions, either active or standby.

In-Sevice (IS)
The entity is performing normal service functions, either active or standby.

ISX
Integral Shelf Cross-Connect

ITU-TSS
International Telecommunication Union-Telecommunication Standardization Sector

J

Jitter
Short term variations in the phase of a digital signal.

K

kb/s
Kilobit Per Second

kHz
Kilohertz

L

LAN
Local Area Network

LCMA
Loss of CRC-4 Multiframe Alignment

LED
Light-Emitting Diode

LFA
Loss of Frame Alignment

LILB
Line Interface Loopback

LLB
Line Loopback

LMA
Loss of Multiframe Alignment

LOF
Loss of Frame

Loopback
A circuit arrangement that causes a received signal to be returned to its source.

LOS
Loss of Signal

LSIU
Low Speed Interface Unit

M

Maintenance Condition (MCOND)
MCOND is a condition in which the Main Controller (MC) is isolated from system hardware in order for the user to perform memory transfer operations. Placing the MC in MCOND is non-service affecting. When the MC is in the MCOND service state, the system software and database are not transferred to the Memory Cards. The Maintenance Condition enables the user to transfer database and/or system software among the Memory Cards and the MC's Random Access Memory (RAM) in a controlled manner via user commands. The MCOND service state is also used to perform system software upgrades.

Mapped
Cross-connected.

Mb/s
Megabit Per Second

MBER
Minor Bit Error Rate

MC
Main Controller

MCOND
Maintenance Condition

MCP
Main Controller Peripheral

MG
Message Generator

MI
Maintenance Information

MML
HuMan-Machine Language

N

NBF
Network Bay Frame

Network Element
A DACS II ISX system is a network element.

NFW
Not Framing Word

NOBBL
No Backbone Leg

Notification Code
The notification code for alarm and status conditions, which include: MJ - major alarm; MN - minor alarm.

NPC
Network Processing Circuit

NPCTG
Network Processing Circuit Test Group

NPCTP
Network Processing Circuit Test Port

NPM
Network Processing Module

NPSM
Network Processing Sub-Module

NSA
Nonsignaling Associated

O

OA&M
Operation, Administration and Maintenance

OOF
Out-Of-Frame

OS
Operations System

Out Of Service (OOS)
The entity is not providing its normal service function (removed from service) either because of a system problem or because it has been removed from service manually.

Outage
A disruption of service that lasts for more than one second. See Hit.

P

Parity Check
To determine whether a block of digital data has been corrupted in transmission, you can use an even-parity format in which an extra bit is added to the block at the transmitter if necessary so that the block always contain an even number of one bits. A parity-checking circuit at the receiving end can determine whether an error has occurred in transmission. An odd-parity format can also be used for the same purpose.

PBA
Primary Block Alarm

PBF
Primary Block Failure

PBX
Private Branch Exchange

PCM
Pulse Code Modulation

PCMCIA
Personal Computer Memory Card International Association

PDS
Program Documentation Standards (Language)

PFWOOF
Pseudo Frame Word Out-Of-Frame

PLL
Phase-Locked Loop

PMA
Prompt Maintenance Alarm

PMEM
Primary Memory Card Slot

PNI
Packet Network Interface

Protocol
Detailed format and procedures used for transmitting digital data.

Provisioned
The entity has been configured by the user and entered into the system database and is ready to be restored to service.

PSF
Platform Service Function

PU
Power Unit

Pulse Code Modulation (PCM)
The process by which analog signals are sampled, quantized, and coded into a digital bit stream.

PVC
Permanent Virtual Circuit

R

R16
Remote Alarm Indication in TS16

RAI
Remote Alarm Indication

RAIS
Remote Alarm Indication Signal

RAM
Random Access Memory

RBER
Remote Bit Error Rate

RDC
Red Circuit

Released
If an input port, it is not under test access; if an output port, it is not cross-connected to an input port under test access.

RMS-D
Remote Measurement System - Digital

RMS-I
Remote Measurement System - International

RTS
Remote Test System

S

SAP
Status and Alarm Panel

SARTS
Switched Access Remote Test System

SCCSAI
Switching Control Center System Asynchronous Interface

SERS
Severely Errored Seconds

SFI
Synchroniztion Failure Indication

SMEM
Secondary Memory Card Slot

SNIDER
Protocol (message format) used on asynchronous administrative links.

Software ID
The software version information for the system.

Standby
Entity is one of a duplicated pair, but not providing service. It is ready to be used to replace a similar entity either by protection or by duplex switching.

State
The state of an entity indicates whether it is defective or normal, whether it is ready for normal use, etc.

SVC
Switched Virtual Circuit

SXC
Synchronizer Cross-Connect

Synchronizer Cross Connect
A dual function circuit pack that performs both synchronization and cross-connect functions.

System Executables
The software that directs the operation of the Main Controller (MC) and other system entities.

T

T1DM
T1 Data Multiplexer

TC
Trunk Conditioning

TDM
Time Division Multiplexed

Test Access
A mode of operation that provides full access to the circuit under test but does not interfere with any other cross-connections that have been established.

TG
Test Group

TLA
Terminate and Leave Activate

TLI
Timing Link Interface

TLR
Terminate and Leave Release

TP
Test Port

TPR
Test Port Release

TREF
Timing Reference

TSI
Time Slot Interchange

U

UAC
Unassigned Channel Code

V

VC
Virtual Circuit

Z

ZCS
Zero Code Suppression

Index

A

B

C

D

E

F

G

H

I

J

L

M

O

P

R

S

T

U