

## J-99347 VF AMPLITUDE AND DELAY EQUALIZING EQUIPMENT

### DESCRIPTION

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#### 1. GENERAL

**1.01** This section describes the J-99347 VF amplitude and delay equalizing equipment. Associated plug-in apparatus consisting of 950A-type and 950B-type equalizers which may be required to complement this arrangement are described in the sections entitled 950A-Type Equalizer—Description (314-820-107), and 950B-Type Equalizer—Description (314-820-108).

**1.02** The J-99347 VF amplitude and delay equalizing equipment was designed to replace the J-99292C amplitude and delay equalizing unit and the associated 384- and 385-type delay equalizers. The J-99347 VF amplitude and delay equalizing equipment consists of a J-99347AA VF amplitude and delay equalizing unit, hereafter referred to as the "J-board equalizer"; the J-99347B-L1 VF amplitude and delay equalizing equipment bay, hereafter call the "J-board bay"; and the J-99347C-L1

VF amplitude and delay equalizing equipment shelf, hereafter referred to as the "J-board shelf."

**1.03** The J-board equalizer and associated equipment, including the plug-in 950-type equalizers, can provide a greater latitude for conditioning voiceband data transmission facilities than the equipment it replaces. The J-board equalizer (see Fig. 1) supplies gain needed to make up for equalizer loss. When the J-board equalizer is complemented with plug-in 950-type equalizers (see Fig. 2), then adjustable amplitude and/or delay equalization is provided to accomplish conditioning of the facility. Since only two codes of the 950-type equalizer are necessary to condition any facility, the central office inventory of spare equalizers will be minimized.

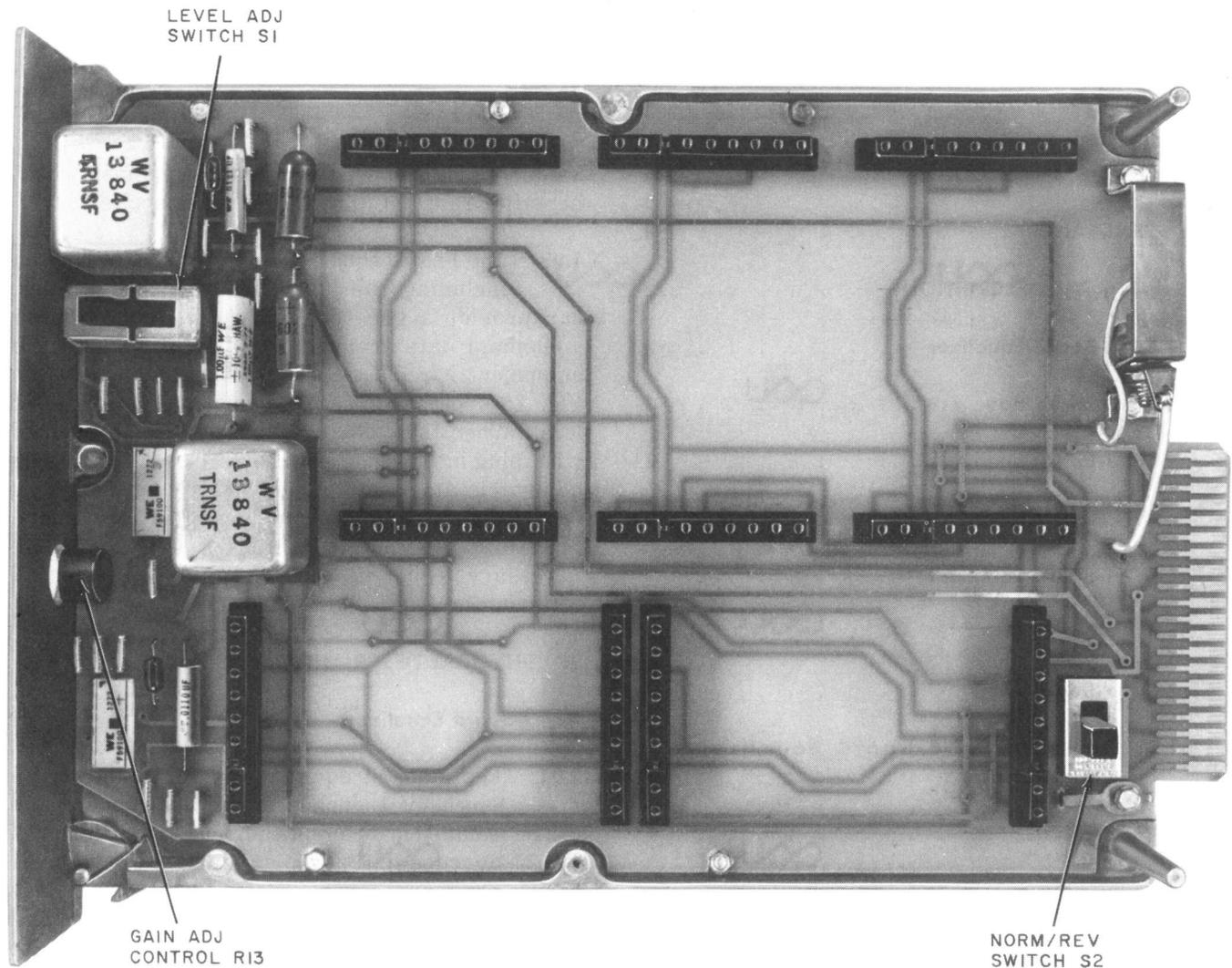
#### 2. PHYSICAL DESCRIPTION

##### A. J-Board Equalizer

**2.01** The J-board equalizer is contained on an 8-inch by 12-inch printed wiring board and can be mounted in different equipment arrangements. The J-board equalizer provides mounting and connectors for up to five 950-type equalizers. Each set of connectors for a 950-type equalizer is provided with normal-through contacts, so dummy plugs are unnecessary. The connectors are keyed so the 950-type equalizers can be added only when positioned correctly.

##### B. J-Board Bay

**2.02** The J-board bay (Fig. 3) is approximately 11.5 feet high and 26.5 inches wide. Each J-board bay contains 15 J-99347A-L1 shelves, and each shelf provides 12 positions for J-board equalizers and associated apparatus. The J-board bay can provide 180 J-board equalizer positions, which can be connected into the data transmission facilities as required. A fuse and alarm panel mounted at the top of the bay provides fuse-protected battery voltage to each of the 15 shelves and a central office minor alarm circuit to alert maintenance personnel. A visual alarm is provided by a fuse



**Fig. 1—J-99347AA VF Amplitude and Delay Equalizer Circuit (J-Board Equalizer)**

alarm lamp, which is also energized by the shelf voltage malfunction.

### C. J-Board Shelf

**2.03** The J-board shelf (Fig. 4) provides 12 positions for J-board equalizers and associated apparatus. The J-board shelf functions identically to a bay shelf with the following exceptions.

(a) The J-board shelf is provided with a fuse and alarm panel which distributes individual fused battery voltage to each J-board position.

(b) The J-board shelf is provided with a jack panel which facilitates monitoring signals into or out of the J-board equalizer at each position.

(c) The data transmission facility or equipment is conveniently terminated on terminal strips mounted on the fuse and alarm panel.

(d) The approximate dimensions of the J-board shelf are 23 inches wide, 12.5 inches high, and 11.5 inches deep. It can be mounted in any 23-inch wide bay having 1-inch mounting holes.

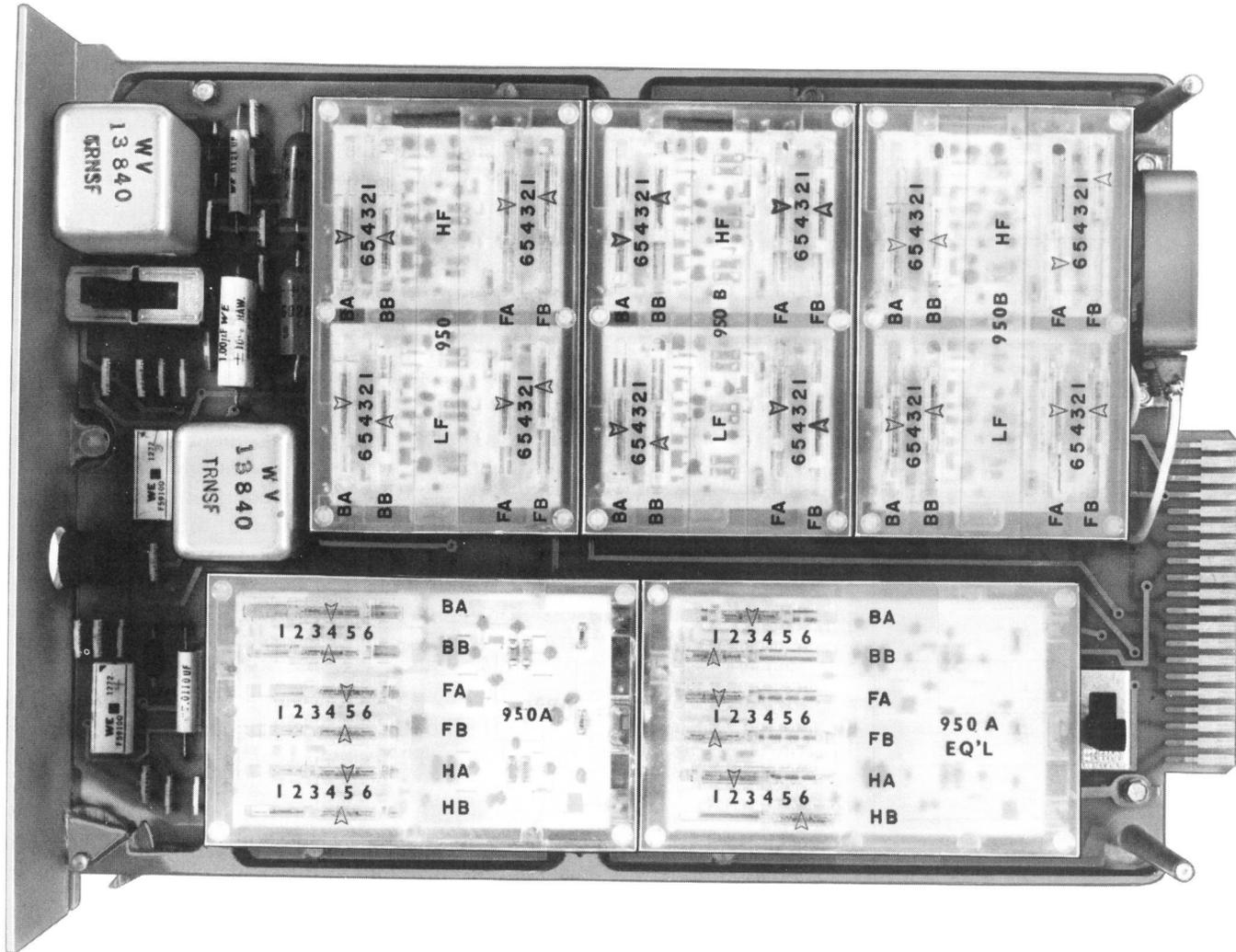


Fig. 2—J-99347AA (or J-Board Equalizer) With Five 950-Type Equalizers

### 3. FUNCTIONAL DESCRIPTION

#### A. J-Board Equalizer

**3.01** A circuit sketch of the J-board equalizer is shown in Fig. 5. Both the input and output circuits are transformer-coupled for isolation and to provide a balanced impedance of 600 ohms. The integrated circuits are protected from external surge voltages by diodes across the transformer secondary windings. Gain is provided by integrated circuit operational amplifiers which are connected in feedback loops. Compensation is provided internally in the amplifier chips.

**3.02** The J-board equalizer circuit is designed to be used as a zero gain device. It can be

inserted into the facility where the transmission level point (TLP) is known to be +7, -2, or -16, or approximates one of these TLPs. A 3-position switch (S1) mounted on the J-board is marked to indicate these specific TLP designations. The switch contacts connect appropriate components into the amplifier circuit to provide optimum performance at these levels.

**3.03** An adjustment to the overall gain of the J-board equalizer circuitry from -4 to +3 dB is provided by the setting of the GAIN ADJ (R13) control. This control is screwdriver-adjustable through a hole in the front plate. The +3 dB gain is available at the maximum clockwise rotation of the control. The range of the GAIN ADJ control is independent of the position of switch S1. This

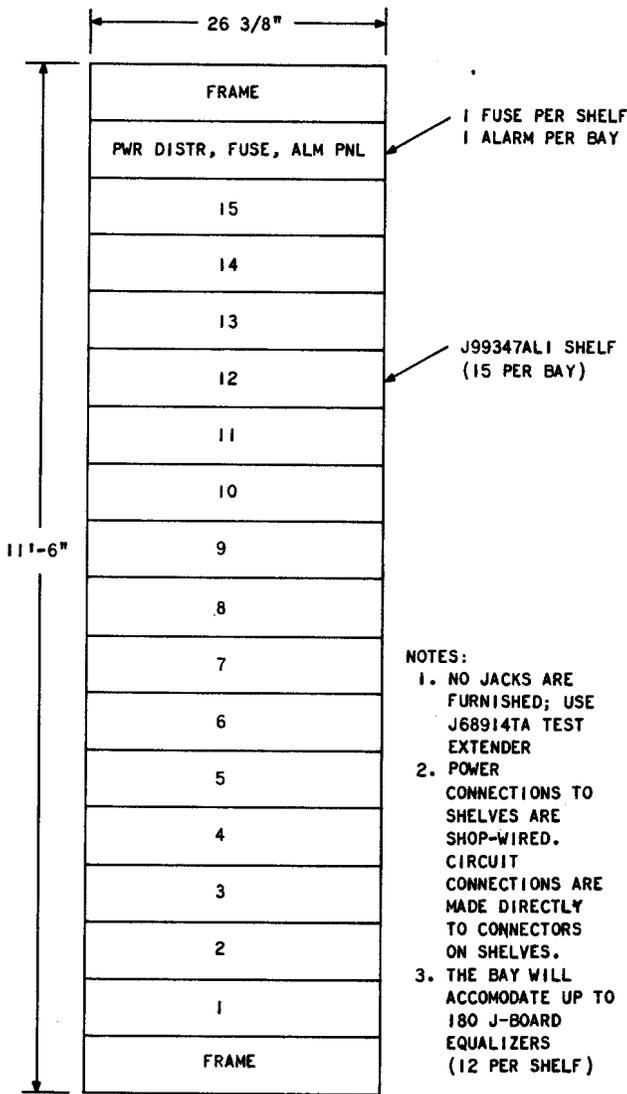


Fig. 3—J-99347B-L1 Shop-Wired Bay For Up to 180 J-99347AA Equalizer Units

gain adjustment is made using the 1000-Hz test signal after the appropriate 950-type equalizers are added to the circuit and adjusted.

**3.04** A 2-position (NORM/REV) phase turnover switch (S2) is part of the output circuit. The NORM position is used when either *zero* or an *even* number of 950A-type equalizers are used on the J-board equalizer. The REV position is used when any *odd* number of 950A-type equalizers are connected into the circuit. 950B-type equalizers do not cause phase turnovers.

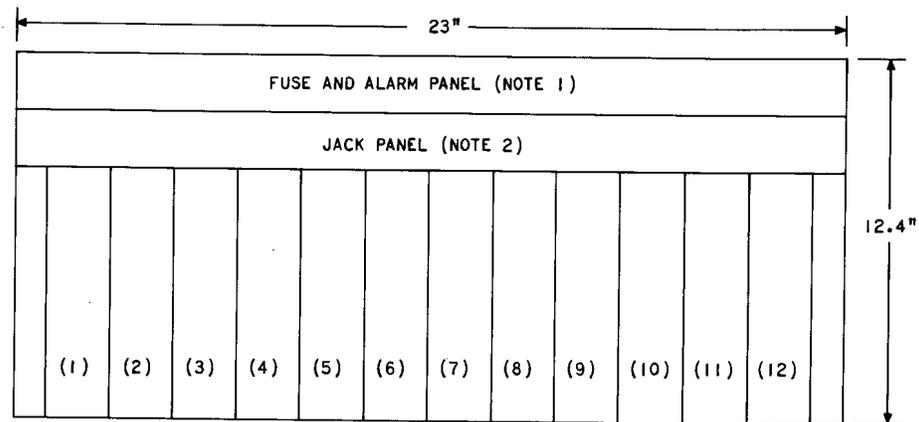
**3.05** Power for the J-board equalizer is supplied through a circuit fed by -48V central office battery voltage. The integrated circuits on the J-board equalizer and in the 950-type equalizers, when used, require equal positive and negative voltages with respect to their circuit ground. A regulating diode (CR3) reduces the applied input voltage to approximately 25 volts dc. Two matched resistors (R8 and R9) divide this voltage into two equal potentials. A connection between R8 and R9 is used to establish a circuit ground to which all equalizer voltage and signal levels are referenced. Each resistor is bypassed by an electrolytic capacitor, C2 and C3, to reduce the ac impedance of the power supply. This arrangement of splitting the input battery voltage provides the required +12 Vdc and -12 Vdc and a common circuit ground required for the operation of both the J-board equalizer and associated 950-type equalizers, when used. Diode CR2 protects all J-board equalizer circuitry from a surge voltage which might come from the battery.

**3.06** A power supply connection at terminal 7 of the J-board equalizer bypasses the regulating diode CR3. This connection is provided so that a nominal 24-volt battery voltage can be used if the J-board equalizer is operated in the logic position of a 4A echo suppressor shelf. The 24-volt input is split as previously described into the required +12 Vdc and -12 Vdc operating voltages.

**3.07** The nominal current drain of a J-board equalizer without 950-type equalizers connected to the circuit and operating in standby condition is approximately 0.012 ampere. The current required for amplification of the ac signal to deliver +11 dBm to the 600-ohm load and with switch S1 set to +7 position is approximately 0.028 ampere.

**3.08** When the facility requires the inclusion of 950-type equalizers, the current drain of 0.008 ampere for *each* 950A, and/or 0.018 ampere for *each* 950B must be added to the current drain for one J-board equalizer.

**3.09** On the J-board equalizer, sets of two connectors for each of the five 950-type equalizer positions are sequentially numbered from 1 to 5. It is important to use the lowest numbered vacant positions first for adding 950A-type equalizers to the circuit. This procedure minimizes overall circuit noise. Unused 950-type equalizer positions are left vacant (no dummy plugs) because



## NOTES:

1. PROVIDES ONE FUSE FOR EACH POSITION, ONE ALARM CIRCUIT FOR THE SHELF, AND THREE CIRCUIT TERMINAL BLOCKS.
2. PROVIDES BOTH IN AND OUT JACKS FOR EACH SHELF EQUALIZER POSITION.
3. THE J99347AA EQUALIZER (J-BOARD EQUALIZER) UNITS ARE NOT FURNISHED WITH THE SHELF AND MUST BE ORDERED SEPARATELY. THE SHELF WILL ACCOMMODATE 12 J-BOARD EQUALIZERS.

**Fig. 4—J-99347C-L1 VF Amplitude and Delay Equalizing Equipment Shelf (J-Board Shelf) Layout and Dimensions**

normal-through contacts in each of the position connectors provide circuit continuity.

#### B. J-Board Bay

**3.10** Each J-board bay is manufactured with shop-wired voltage and ground connections to each shelf. Every bay shelf is shop-wired to distribute the applied battery voltage, battery ground, and frame ground connections to all position connectors. All data transmission facility or equipment connections are terminated directly on the appropriate shelf-position connectors. A jack field panel is not provided with the J-board bay, which requires all tests and adjustments necessary for installing a J-board equalizer be performed using a J-68914TA test extender. The J-board equalizers are not supplied with the J-board bay and must be ordered separately.

#### C. J-Board Shelf

**3.11** A simplified sketch illustrating some typical factory-wired connections and signal paths into and out of a J-board shelf is shown in Fig. 6. Similar to the J-board bay, a fuse failure to a J-board equalizer position will energize a minor alarm in the office alarm circuit and illuminate

the fuse alarm lamp which is common to all 12 fuses on the fuse and alarm panel. The jacks on the jack panel provide a means to test the connected facility or equipment in either direction or conveniently isolate and test the J-board equalizer in position.

#### D. Summary of J-Board Equalizer Characteristics

**3.12** The J-board equalizer, either mounted in a J-board bay, in a J-board shelf, or in the logic circuit position of a 4A echo suppressor, provides equalization to meet the conditioning requirements for voiceband data facilities or alternate voice/data circuits. Four typical applications are shown in simplified form in Fig. 7. These application figures basically show how the J-board equalizer and associated equipment can be used with either 4-wire full-duplex or 2-wire half-duplex facilities to provide either pre-equalization (nearest the data transmitter) or post-equalization (nearest the data receiver) as required. Note that two J-board equalizers are required for 4-wire full-duplex (one for each direction) while only one J-board equalizer is used in half-duplex operation, for pre-equalization or post-equalization as required.

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**3.13** The following limitations are imposed on the J-board equalizer regardless of the facility being used.

- (a) Each J-board can be provided with from zero to five 950-type equalizers. When the 950-type equalizer codes are mixed (ie, using both 950A and 950B equalizers), the lowest-numbered position on the J-board must be used first for a 950A amplitude equalizer to minimize circuit noise. Unused positions for 950-type equalizers must be left vacant on each J-board equalizer to maintain circuit continuity (ie, no dummy plugs required).
- (b) The level switch S1 on each J-board equalizer unit must be set to +7, -2, or -16 position to match the nearest circuit transmission level.
- (c) The NORM/REV switch S2 on each J-board equalizer must be set to NORM position when *zero* or an *even* number of 950A-type equalizers complement the J-board equalizer circuitry. Switch S2 must be set to REV position only when an *odd* number (1, 3, or 5) of 950A-type equalizers are used on the J-board equalizer. The number of 950B-type equalizers used on any J-board equalizer does not influence the setting of switch S2.
- (d) The front panel GAIN ADJ control at each installed J-board equalizer position must be adjusted to provide 0 dB gain *after* the required 950-type equalizers have been added to the J-board equalizer circuitry and have been appropriately set by the prescription tables or from the computer program.
- (e) The jack connections shown in Fig. 6 are included as part of the J-board shelf. Similar jack connections will be available on the J-board bay at each equalizer position when using the J98614TA test extender.
- (f) The installer is required to segregate cables when different transmission levels are used on the connecting circuits.
- (g) Facility or equipment connections will be terminated at the J-board equalizer position connector on the J-board bay or terminated on the appropriate terminal strip provided with the J-board shelf on the fuse and alarm panel. Tables

A, B, and C identify the terminal strip designations applicable to the factory-wired J-board shelf.

**3.14** One condition must be met when the J-board equalizer is used for pre-equalization of a facility (nearest the transmitter). The gain at any frequency between 300 Hz and 3200 Hz shall not be greater than +5 dB more than the 1000-Hz calibration signal gain. This maximum gain is only acceptable if the system signal and crosstalk requirements are also met.

**3.15** When the J-board equalizer is used to provide post-equalization (nearest the receiver), the requirements of 3.14 do not apply. Post-equalization functions are provided to restore line signal fidelity by using amplification or attenuation as necessary before the signal is delivered to customer equipment.

**3.16** One feature not shown by the diagrams in Fig. 7 is that if necessary equalization cannot be provided with one J-board equalizer, even with a full complement of 950-type plug-in equalizers, a second and third J-board equalizer with 950-type apparatus can be connected in series until the required conditioning is met. However, the need for more than one J-board equalizer unit is expected to be very infrequent.

**3.17** When a J-board equalizer is used in either a J-board bay position or in a 4A echo suppressor logic position, external test equipment consisting of a J68914TA test extender and a 21A transmission measuring set (TMS) is required to obtain the proper setting of the J-board GAIN ADJ control. The test extender provides the necessary jack connector access to measure the facility parameters and to inject oscillator signals at the required levels. The 21A TMS provides the calibrated signal detector and the oscillator circuits.

**CAUTION:** *Special testing instructions are required with the use of the J68914TA test extender. Basically, the instructions require:*

**(1) All J68914TA test extender key switches be in NORM position before, during, and after testing a J-board equalizer to obtain reliable test information.**

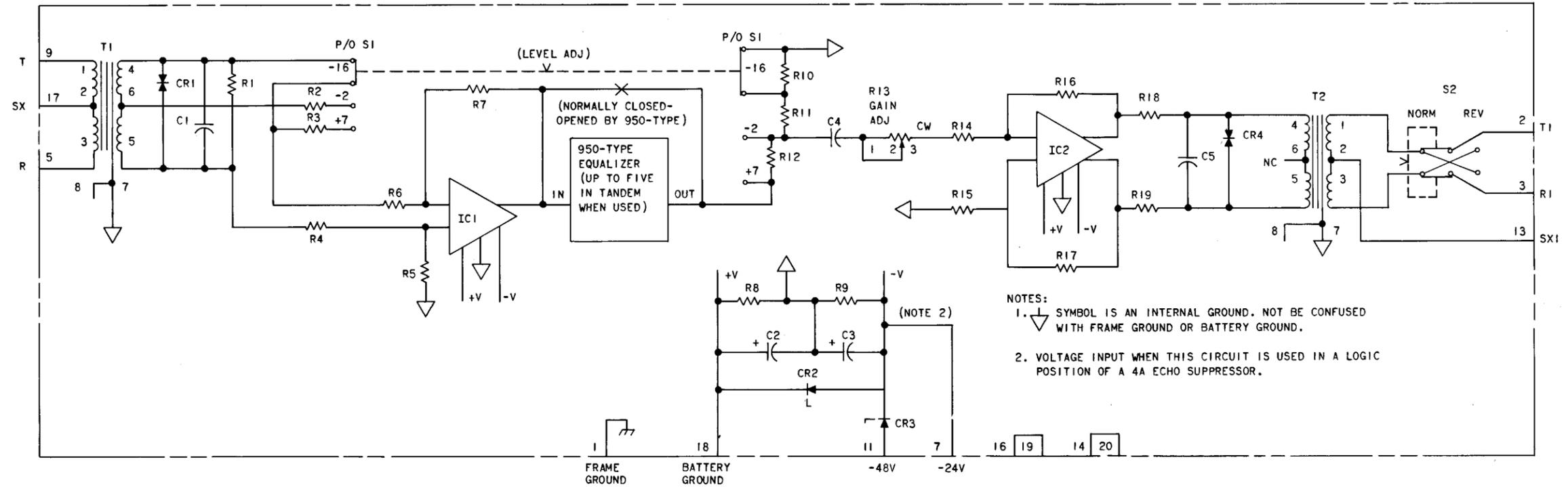


Fig. 5—J-99347AA VF Amplitude and Delay Equalizer Circuit (J-Board Equalizer)

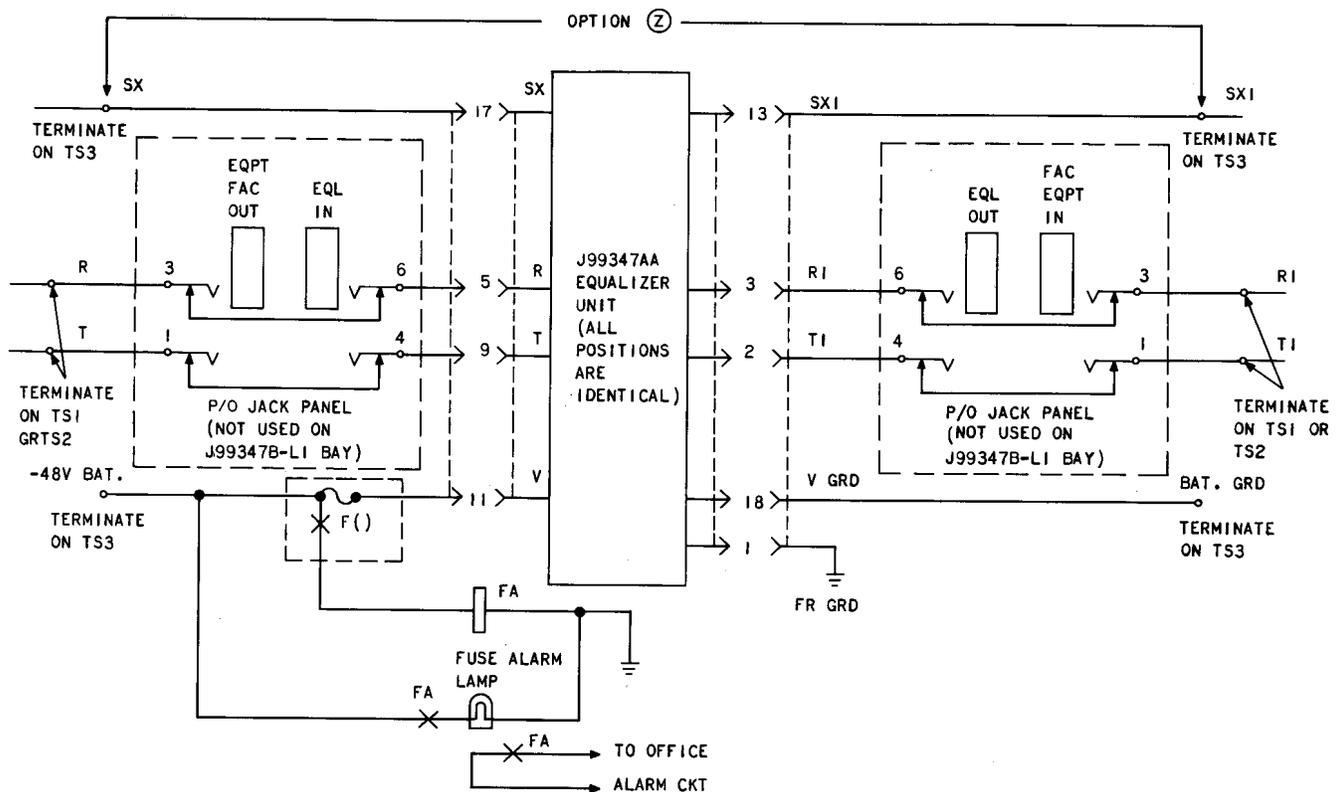


Fig. 6—Typical J-99347C-L1 J-Board Shelf Position Circuit



*Momentary operation of the TD CHECK key switch on the J68914TA test extender, when connected between a bay position and a J-board equalizer under test, can result in damage to the J-board equalizer under test and/or the J68914TA test extender circuits.*

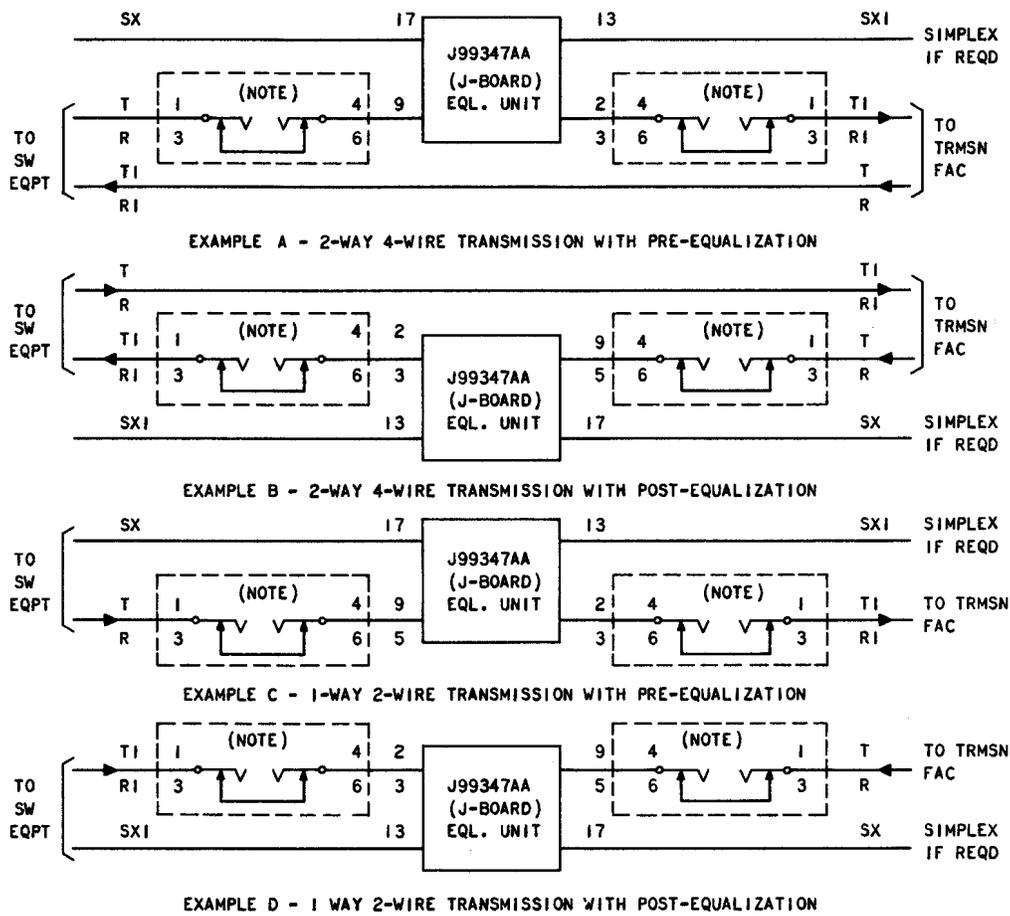
*(2) Valid test results are only accomplished using the specified jack connections and in the sequence as listed in the testing instructions.*

**3.18** The special testing instructions are provided in the section entitled J-99347 VF Amplitude and Delay Equalizing Equipment—Installation Tests and Adjustments (314-820-206).

#### 4. REFERENCES

**4.01** The following publication and document numbers are provided as a guide to supporting and supplementary information for equipment referred to in text.

SECTION	TITLE
314-820-107	950A-Type Equalizer—Description
314-820-108	950B-Type Equalizer—Description
314-820-206	J99347 VF Amplitude and Delay Equalizing Equipment—Installation and Adjustment



NOTE:  
 JACKS ARE AVAILABLE FOR USE WITH THE J-BOARD SHELF. FOR J-BOARD BAY ARRANGEMENT, JACKS ARE AVAILABLE WHEN USING A J68914TA TEST EXTENDER. THE SIGNAL FLOW IS SHOWN BY ARROWS.

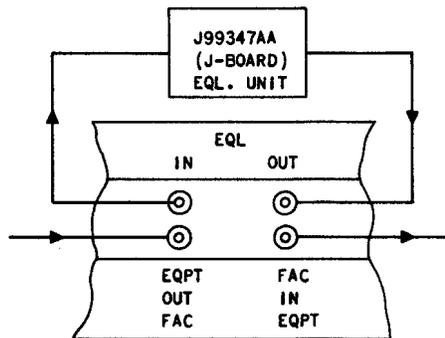


Fig. 7—Typical Transmission Circuits for Equalizing VF Data Circuits

SECTION	TITLE	SECTION	TITLE
314-820-506	J99347 VF Amplitude and Delay Equalizing Equipment—Maintenance Testing	856-200-100	ADE 950 Equalizer Program
332-414-105	4A Echo Suppressor—J68914TA Test Extender—Description	SD-6G069-01	4A Echo Suppressor Test Extender
801-401-153	Equipment Specifications for the J99347 Equalizer Equipments	SD-99559-01	Common Systems—VF Amplitude and Delay Equalizer Circuit

**TABLE A**  
**J99347C-L1 SHELF**  
**SIGNAL INPUT AND OUTPUT TERMINATIONS**

CKT POS	SIGNAL INPUT		SIGNAL OUTPUT	
	T (PIN 9)	R (PIN 5)	T1 (PIN 2)	R1 (PIN 3)
1	TS1-11	TS1-21	TS1-31	TS1-41
2	-12	-22	-32	-42
3	-13	-23	-33	-43
4	-14	-24	-34	-44
5	-15	-25	-35	-45
6	TS1-16	TS1-26	TS1-36	TS1-46
7	TS2-11	TS2-21	TS2-31	TS2-41
8	-12	-22	-32	-42
9	-13	-23	-33	-43
10	-14	-24	-34	-44
11	-15	-25	-35	-45
12	TS2-16	TS2-26	TS2-36	TS2-46

**TABLE B**  
**J99347C-L1 SHELF**  
**SIMPLEX SIGNAL INPUT AND OUTPUT TERMINATIONS**

CKT POS	SIGNAL INPUT	SIGNAL INPUT
	SX (PIN 17)	SX1 (PIN 13)
1	TS3-12	TS3-22
2	-32	-42
3	-13	-23
4	-33	-43
5	-14	-24
6	-34	-44
7	-15	-25
8	-35	-45
9	-16	-26
10	-36	-46
11	-17	-27
12	TS3-37	TS3-47

TABLE C  
J99347C-L1 SHELF  
INPUT BATTERY VOLTAGE DISTRIBUTION

CKT POS	BAT. VOLTAGE WIRE COLOR	FUSE DESIG	BAT. GRD WIRE COLOR
1	Y-G	F1	Y
2	O-W	F2	O
3	Y-G	F3	Y
4	O-W	F4	O
5	Y-G	F5	Y
6	O-W	F6	O
7	Y-G	F7	Y
8	O-W	F8	O
9	Y-G	F9	Y
10	O-W	F10	O
11	Y-G	F11	Y
12	O-W	F12	O