# GENERAL DESCRIPTION
# CARRIER SUPPLY CIRCUIT
# B1 DATA CARRIER TERMINAL

## 1. GENERAL

**1.01** The carrier supply circuit per SD-73018-01 is part of the B1 data carrier terminal and is designed to supply eight sine-wave carrier frequencies and two square-wave clock frequencies to a maximum of six B1 data carrier terminal units within a terminal frame.

**1.02** As shown in Fig. 1 the carrier supply consists of two 23-inch trays incorporating the following equipment: two −48 to +12 volt power supply converters, two filters, 621A and 621B, and a total of 18 circuit packages consisting of six different types.

**1.03** This circuit performs an analog-to-digital-to-analog set of frequency conversions which provide a means of generating the eight carrier frequencies and the two clock frequencies from a base reference oscillator. This reference frequency is crystal controlled and at time of manufacture is within a tolerance of ±0.006 per cent.

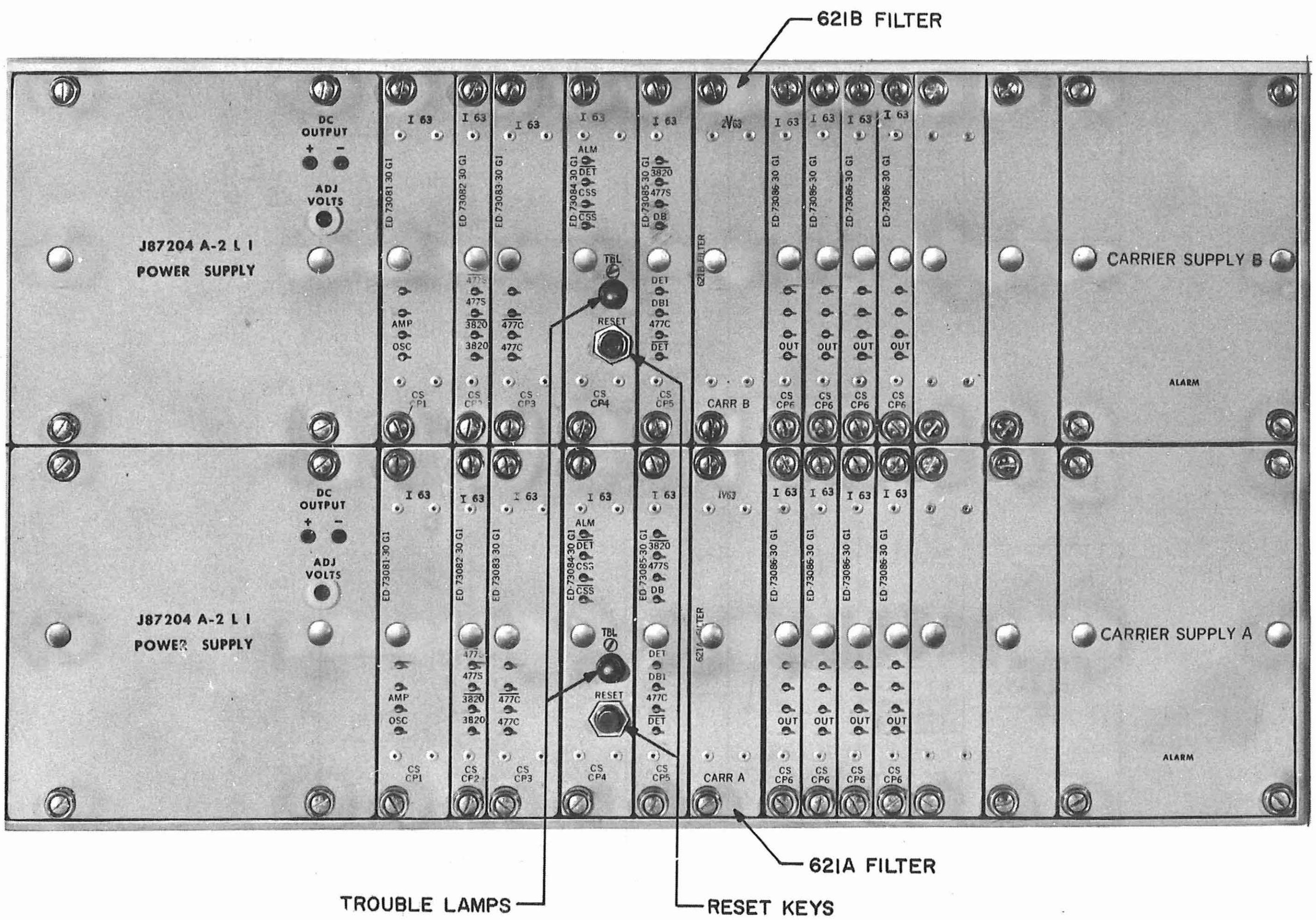



Fig. 1 – Carrier Supply Circuit — B1 Data Carrier Terminal

**1.04** The eight sine-wave carrier frequencies are supplied to the data channel circuits for the purpose of modulation and demodulation of the data signals as explained in Section 314-020-150, B1 Data Carrier Terminal Modulation Plan.

**1.05** The two square-wave clock frequencies are provided to the supervisory signaling circuits for the purpose of reference timing as explained in Section 314-018-150, B1 Data Carrier Terminal Supervisory Signaling Circuits.

## 2. GENERAL METHOD OF OPERATION

**2.01** As indicated by Fig. 2, the carrier supply circuit is composed of two frequencies generators designated A and B, alarm and load transfer circuits A and B, two different filters, 621A and 621B, and two sets of output amplifiers, A and B.

**2.02** The generation and conversion of frequencies involved within the frequencies generator and the outputs provided are shown in block diagram form in Fig. 3. A free running crystal-controlled transistor oscillator generates a 3820-cps sine-wave signal which is used as the base reference frequency. This signal is applied to a squaring circuit, the output of which is a 3820-cps square wave. The 3820-cps square wave is divided down by eight via the eight-to-one (8:1) countdown circuit. The output of the countdown circuit is thus a 477.5-cps square wave which is in turn applied to a pulse shaping

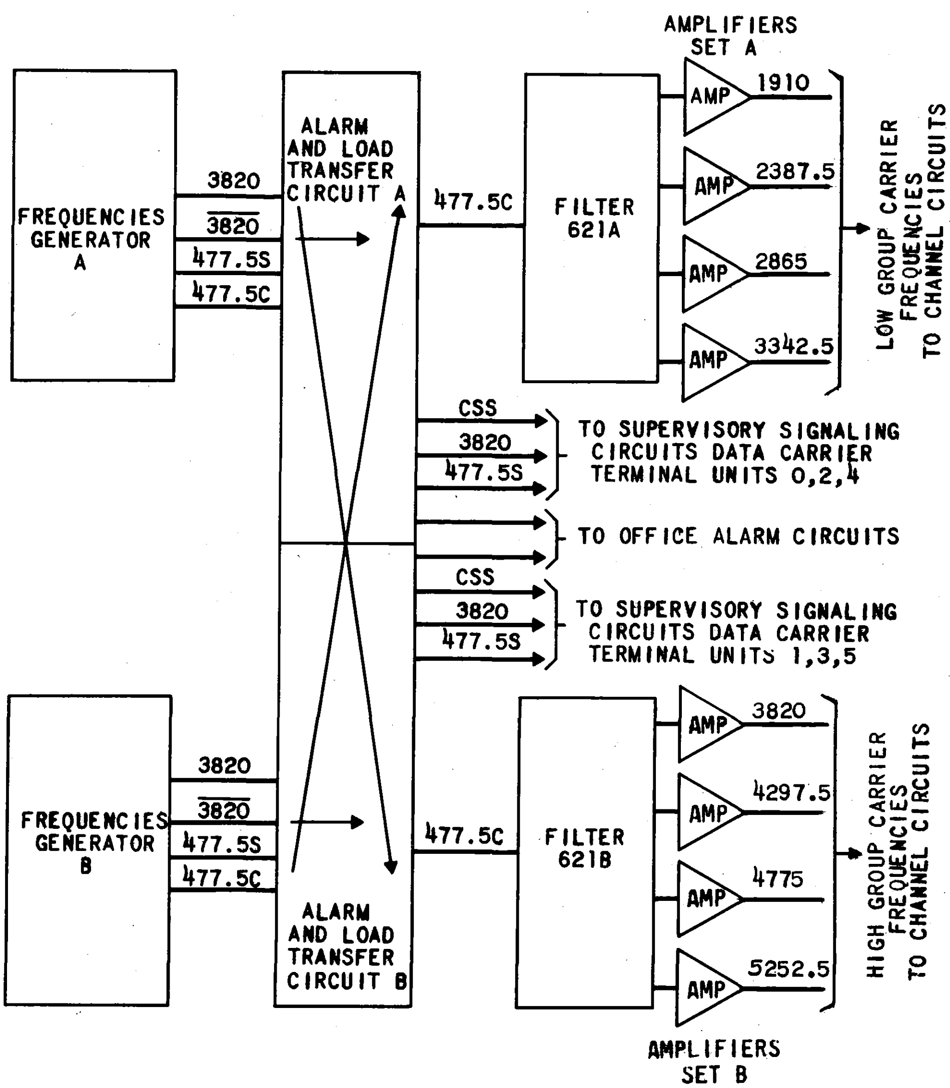



**Fig. 2 – Carrier Supply Block Diagram**

circuit. The pulse shaping circuit converts this square wave to a 477.5-cps train of narrow negative-going pulses which serve as a base carrier supply signal. As shown in Fig. 2, the circuitry for deriving the base carrier supply frequency output, the 477.5-cps pulse train, and other associated clock signals is duplicated within the carrier supply and designated frequencies generator A and B.

**2.03** The 477.5 cps pulse trains from frequency generators A and B are applied, via the alarm and transfer circuits, to the filters 621A and 621B as shown in Fig. 2. The filter 621A is composed of four narrow-band filters in parallel. Each of these is a slot filter possessing a pass band at one and only one of the fourth through the seventh harmonics of the 477.5-cps pulse train. Thus the outputs of the 621A filter are the low group carrier frequencies 1910,2387.5, 2865, and 3342.5 cps.

**2.04** In a similar fashion the 621B filter is composed of four slot filters in parallel, each of which possesses a pass band at one and only one of the eighth through the eleventh harmonics of the 477.5-cps pulse train. Thus the outputs of the 621B filter are the high group carrier frequencies 3820, 4297.5, 4775, and 5252.5 cps.

**2.05** Amplifier sets A and B, consisting of four feedback amplifiers per set, introduce voltage and power gain to each of the four frequencies comprising the low and high group carrier frequencies, respectively. These eight carrier frequencies are then distributed to the proper channel circuits within each data carrier terminal unit in the frame.

**2.06** The two clock frequencies provided to the supervisory signaling circuit, within any given data carrier terminal unit, are the 3820- and 477.5-cps square waves. These clock frequencies are distributed to the supervisory signaling circuit within a terminal frame via the alarm and transfer circuits. In the normal, non-alarm, mode of operation the clock frequencies from frequencies generator A are distributed to the supervisory signaling circuits within data carrier terminal units 0, 2, and 4 while those from frequencies generator B are distributed to terminal units 1, 3, and 5.

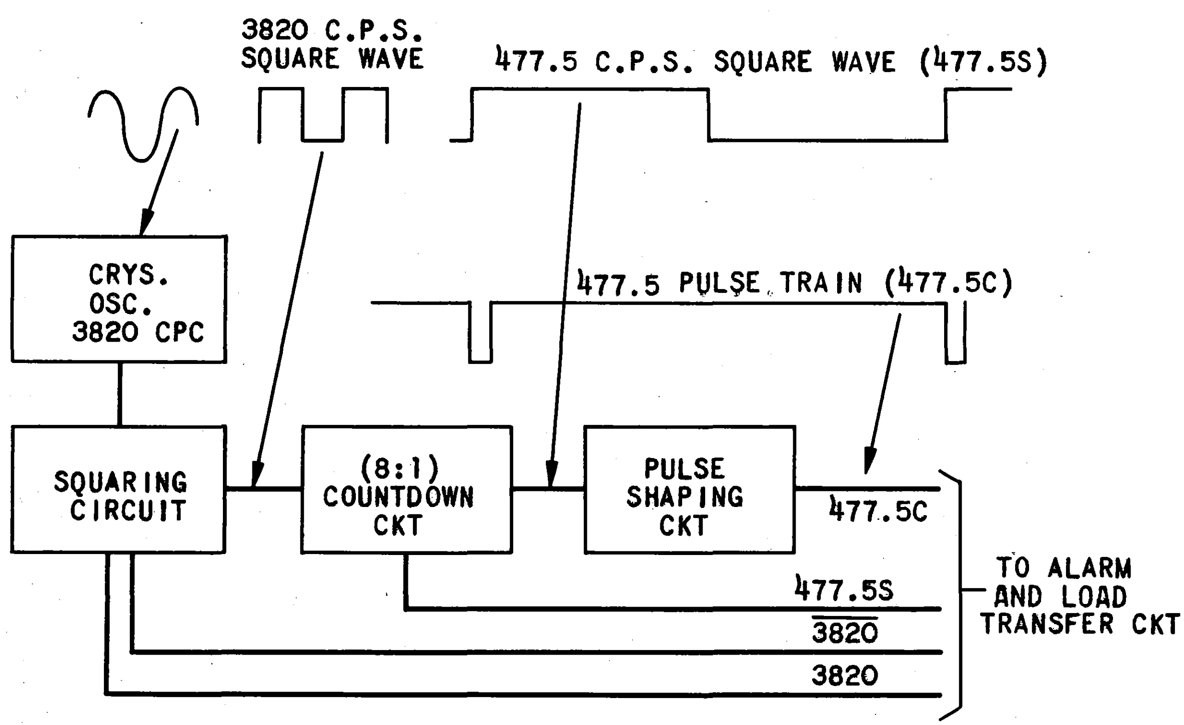



**Fig. 3 – Frequencies Generator Block Diagram**

**2.07** The alarm and load transfer circuits provide a means of operating the carrier supply without degradation upon a failure within one of the two frequencies generators. This is accomplished by switching the loads (3820- and 477.5-cps square-wave clock frequencies and the 477.5-cps pulse train) from the frequencies generator which indicates a trouble condition to the generator which is operating properly. Reserve power is available at each frequencies generator so that upon failure of one, the entire load within a terminal frame will operate without degradation upon being switched to the other. During the switching interval a signal is provided to all the supervisory signaling circuits within the bay so that a minimum of errors are created within the supervisory signaling information. The load switching within the carrier supply is so arranged that a minimum of errors are created in the data channels via the temporary loss of four carrier frequencies. The carrier supply will yield proper signals to the office audible and visual alarm circuits upon failure of one or both of the frequencies generators. An office ***minor*** alarm is created upon failure of one of the two frequencies generators, and an office ***major*** alarm upon failure of both generators.

## 3. CIRCUIT DETAILS — FREQUENCIES GENERATOR

**3.01** The functional schematic representation of the frequencies generator is shown in Fig. 4. The following paragraphs of this part will explain each of the functional schematics (the oscillator, squaring circuit, 8:1 countdown circuit, and the pulse shaping circuit) which comprise the frequencies generator.

### Crystal Oscillator (See Fig. 5)

**3.02** The crystal-controlled transistor oscillator generates the base reference frequency of 3820.0 cps with a maximum expected offset of ±0.2 cps (±0.006 per cent) when operated in the central office environment. No factory or field adjustment is provided on the oscillator.

**3.03** The oscillator circuit, shown as a simplified schematic in Fig. 5, employs an amplifier (transistor Q1) to provide sufficient loop gain for oscillation, a low-pass filter (L1 and C3-C7) for proper loop phase, and crystal Y1 for frequency control. Diode limiting, RV1-RV3, is used at the collector of Q1 to maintain the output voltage of the oscillator reasonably constant for wide ranges of environmental conditions and circuit component values. The crystal Y1 operates positive reactance, and C8 adjusts the impedance of the crystal-capacitor combination for series resonance. Transformers T1 and T2 provide impedance transformations and dc isolation. The −22.5 volt regulated power supply for the oscillator is obtained from −48 volt office battery via the zener diode CR1 with filtering provided by capacitor C10.

### Squaring Circuit (See Fig. 6)

**3.04** The squaring circuit converts the 3820-cps sine wave output of the crystal oscillator to a square wave with a rise and fall time of approximately 0.3 $\mu$sec. This circuit consists of an amplifier, monopulser, and a transistor-resistor gate TRL as indicated by the functional blocks in Fig. 6.

**3.05** The amplifier (AMP) is so biased that with the sine-wave input from the oscillator it will act as a switch and be driven from cutoff to saturation. Thus, its output is essentially a clipped sine wave between 0 and +6 volts with relatively long rise and fall times.

**3.06** The monopulser (MP) accepts the clipped sine wave output of the amplifier and through the use of positive feedback generates an output pulse of a prescribed width and with a rise time of approximately 0.3 microseconds, for each positive going transition which appears at its input. Thus, we have created a 3820-cps square wave at its output which is the emitter of transistor Q3. This square wave is inverted, and designated $\overline{3820}$, by the TRL transistor gate Q4. The fall time of the square wave at the collector of Q4 is approximately 0.3 $\mu$sec.

### The 8:1 Countdown Circuit (See Fig. 7)

**3.07** The purpose of this circuit is to divide down the frequency of the $\overline{3820}$-cps square wave by a factor of eight yielding a 477.5-cps square wave. This is accomplished by using three low-frequency binary cells (LBC) connected in tandem as shown by the functional blocks in Fig. 7.

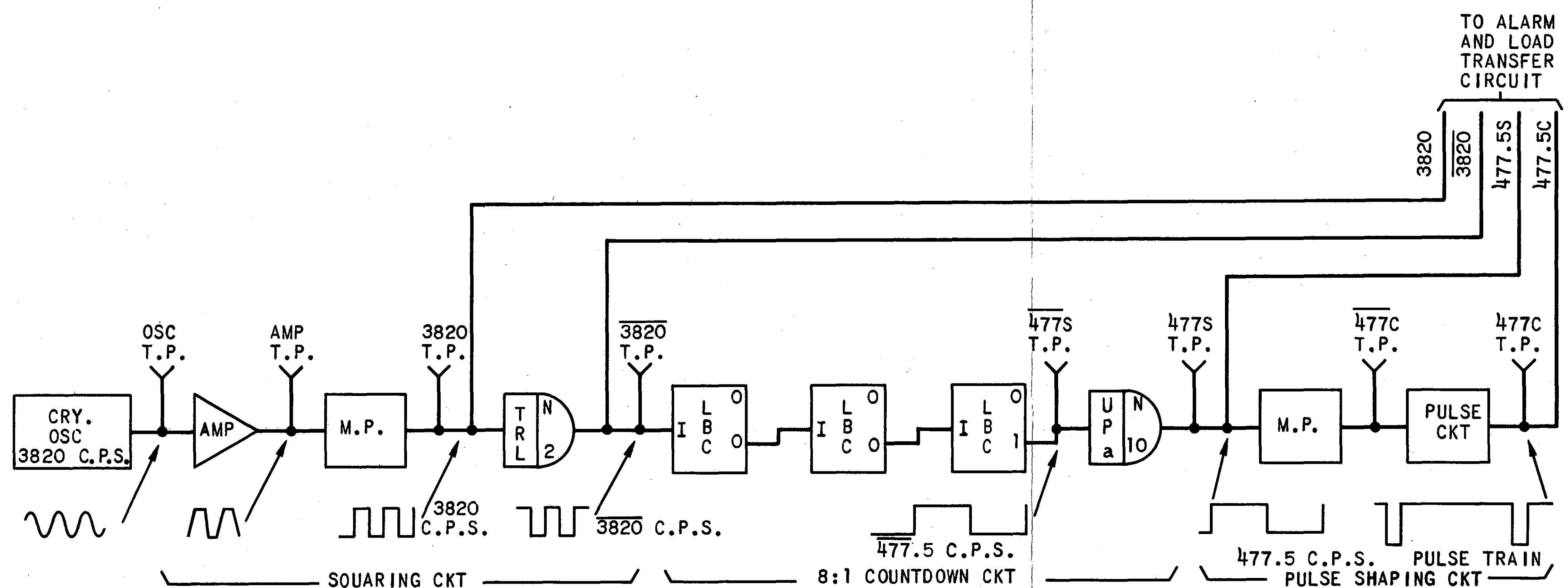



Fig. 4 – Frequencies Generator Functional Schematic

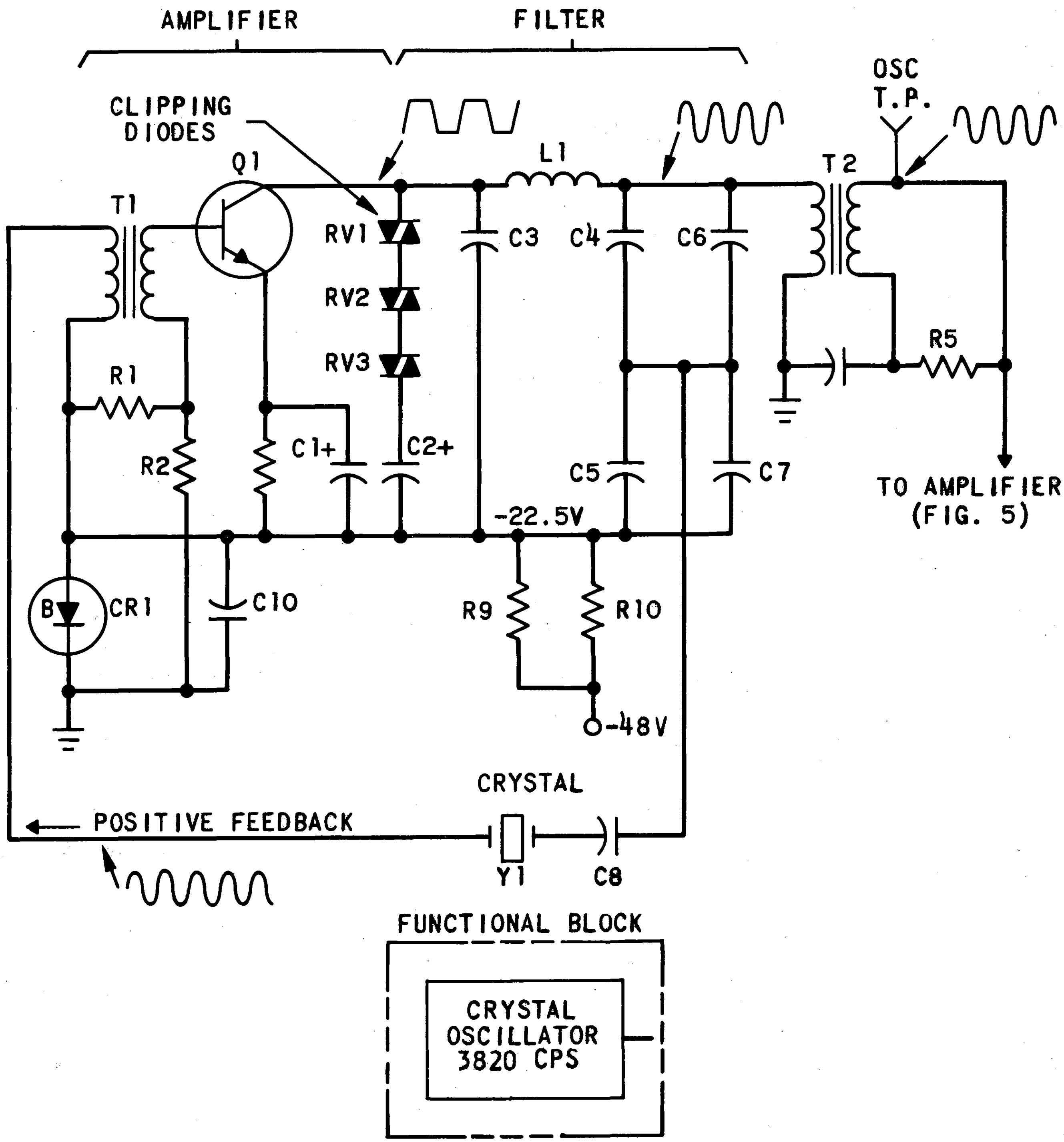



Fig. 5 – Crystal Oscillator Simplified Schematic

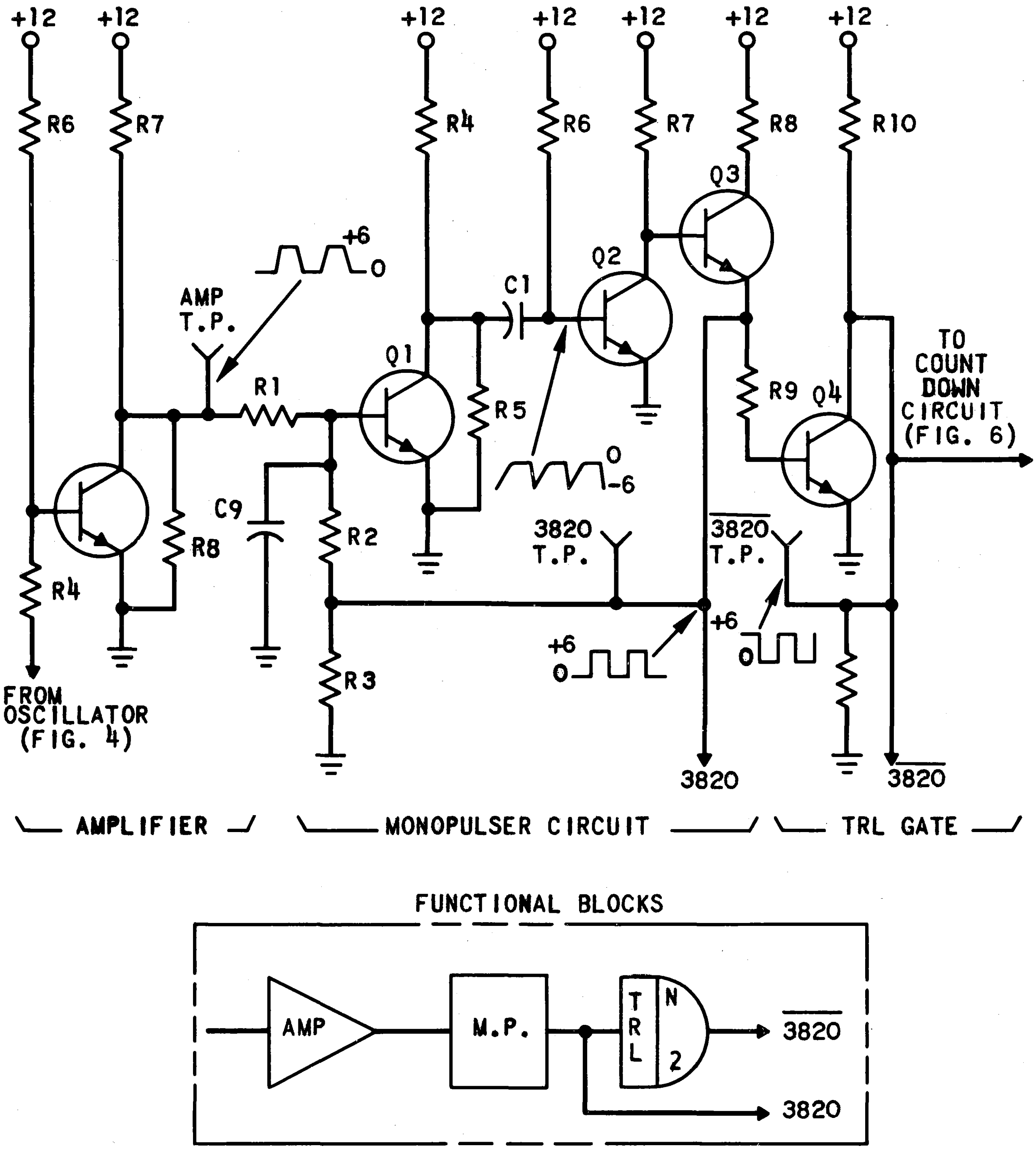



Fig. 6 – Squaring Circuit Functional Block Diagram

**3.08** The LBC is a flip-flop with the addition of a pulse steering network. This steering network consists of a capacitor C- and a diode CR- which provides the temporary memory required to steer the negative-going transition of the input to the base of the on transistor of the flip-flop. The negative transition will turn the on transistor off, and by the use of positive feedback the off transistor is turned on. Thus, the LBC changes state for each negative-going transition which corresponds to division by two in frequency of the input square wave.

**3.09** The $\overline{3820}$-cps square wave output of the squaring circuit is applied to the first LBC. Its output, being a $\overline{1910}$-cps square wave, is applied to a second LBC which yields a 955-cps square wave output. The $\overline{955}$-cps square wave is applied to the third LBC yielding a 477.5-cps square wave. The counted down 477.5-cps square wave is inverted and power amplified by a transistor gate (UPa) transistors Q11 and Q12 yielding a 477.5-cps square wave output at the emitter of Q12.

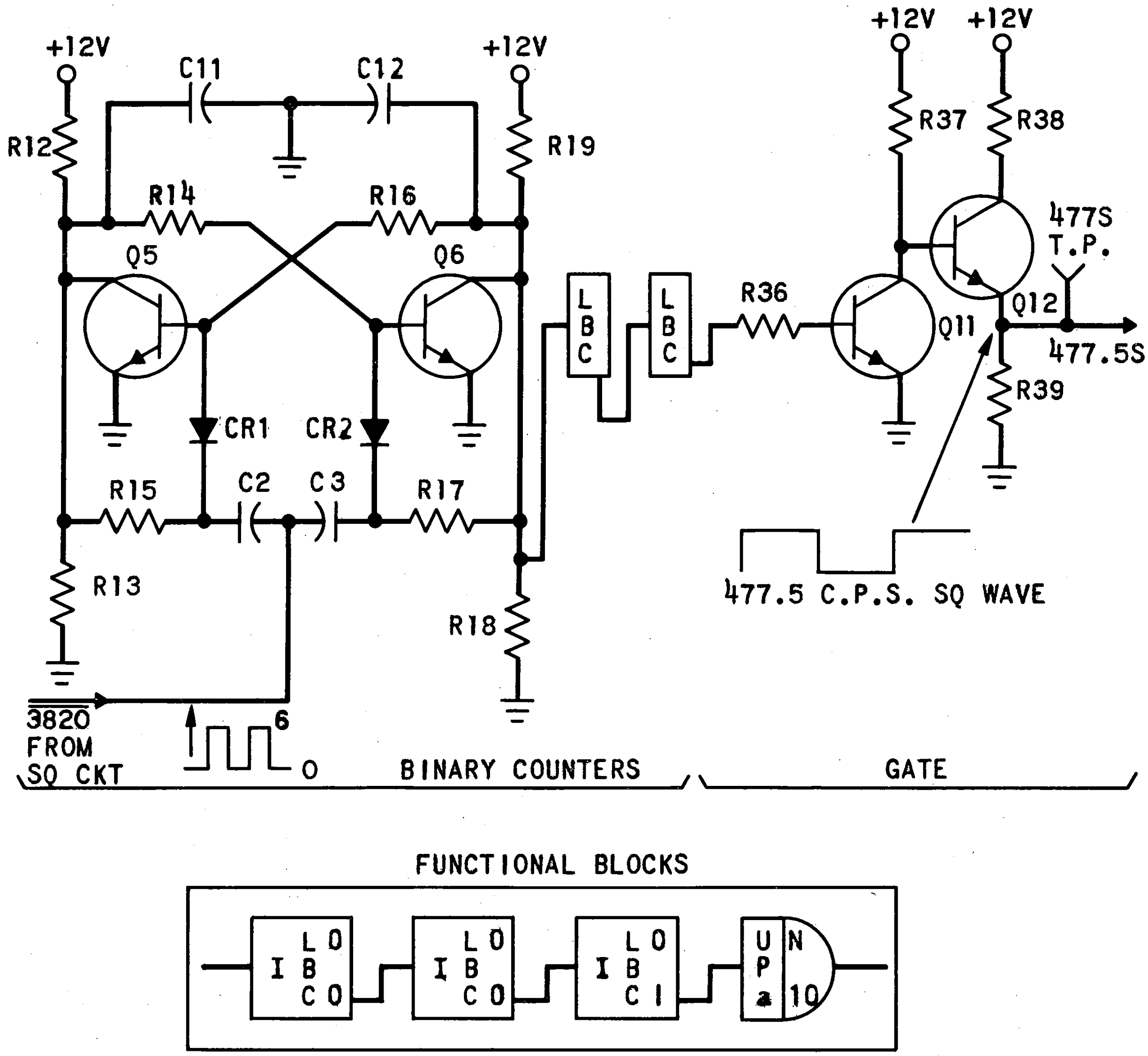



**Fig. 7 – 8:1 Countdown Circuit Functional Block Diagram**

**Pulse Shaping Circuit (See Fig. 8)**

**3.10** This circuit accepts the output of the countdown circuit and generates a train of 95-μsec pulses at a repetition rate of 477.5-cps. This is accomplished by the use of a 95-μsec monopulser (transistor Q1 and Q2) and a pulse circuit amplifier consisting of transistors Q3, Q4, and Q5.

**3.11** In the quiescent condition the output of the monopulser is 0 volt. Transistor Q4 is turned on and transistors Q3 and Q5 are off. The output of the pulse circuit is at approximately +0.7 volt through a low impedance to ground (ie, diode CR3 forward biased). When the input to the pulse circuit (ie, the output of the monopulser) goes to +6 volts for 95 microseconds, transistor Q4 turns off and transistors Q3 and Q5 turn on. When transistor Q5 is turned on diode CR3 is back-biased and the output of the pulse circuit goes to approximately −6 volts for 95 μsec. The output impedance is low and consists of the collector-emitter saturated junction of Q5.

**Frequencies Generator Outputs (See Fig. 9)**

**3.12** The four outputs of the frequencies generator are as follows: 3820-cps square wave, $\overline{3820}$-cps square wave inverted, 477.5-cps square wave, and the 477.5-cps train of 95-μsec pulses. These outputs along with the internal signals of the frequencies generator are shown in time sequence in the operation sequence diagram Fig. 9. The test points on the equipment for the 477.5C and 477.5S signals have been abbreviated to 477C and 477S because of limited space available for character stampings.

**3.13** The 3820- and 477.5-cps square-wave frequencies are the clock frequencies provided to the supervisory signaling circuit. The 477.5-cps train of 95-μsec pulses is used as the source for the harmonics needed for derivation of the carrier frequencies for use in the data channel modulators and demodulators.

## 4. CIRCUIT DETAILS — 621A AND 621B FILTERS (See Fig. 10)

**4.01** The 621-type filter consists of four different and independent sections. The purpose of each section is to provide a narrow passband which will transmit a preselected harmonic of the 477.5-cps pulse train, while presenting adequate insertion loss to all other harmonics. The 621A filter contains four such sections which pass the low group carrier frequencies, ie, the fourth through the seventh harmonics of 477.5-cps. The 621B filter contains four sections which pass the high group carrier frequencies, ie, the eighth through the eleventh harmonics of the 477.5-cps pulse train. A typical filter frequency versus insertion loss characteristic is shown.

**4.02** Each section of the 621-type filters is designed to work between a 25-ohm unbalanced input impedance and a 150-ohm unbalanced output impedance. The low input impedance driving source is provided by the output of the 477.5-cps pulse circuit described in 3.10. The termination impedance for any given section of the filter is determined by resistor R1 and the input impedance of the output feedback amplifier. The purpose of resistors R2 and R3 is described in 5.03.

## 5. CIRCUIT DETAILS — OUTPUT AMPLIFIER (See Fig. 11)

**5.01** The eight carrier frequencies are distributed to the channel circuits from the carrier supply via the eight output amplifiers which comprise amplifier set A and set B. Amplifier set A consists of four identical amplifiers used to distribute the low group carrier frequencies 1910, 2387.5, 2865, and 3342.5 cps which are the outputs of the 621A filter. In a similar manner, amplifier set B distributes the high group carrier frequencies 3820, 4297.5, 4775, and 5252.5 cps which are the outputs of the 621B filter.

**5.02** The output amplifier is a two transistor feedback amplifier utilizing shunt feedback at the input (base of Q1) and output (emitter of Q2). Shunt feedback is provided at the output to reduce the output impedance below 40 ohms, thereby minimizing the crosstalk between channels which use a given carrier frequency. Shunt feedback is provided at the input so that the input impedance is relatively small and stabilized. The total output impedance as seen by the 621-type filter section thereby consists of resistor R1 (within the filter) plus the input impedance to the amplifier.

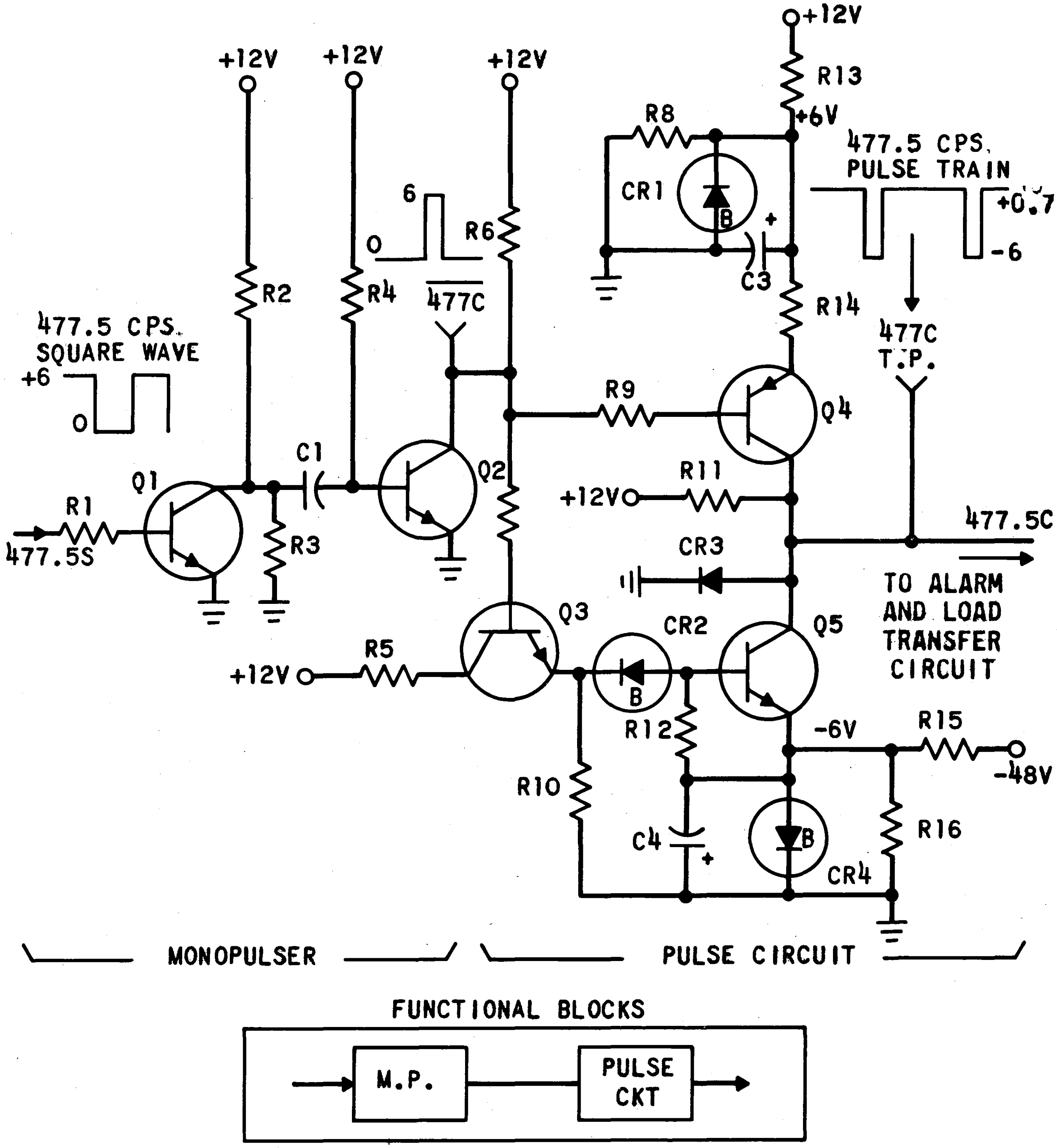



Fig. 8 – Pulse Shaping Circuit

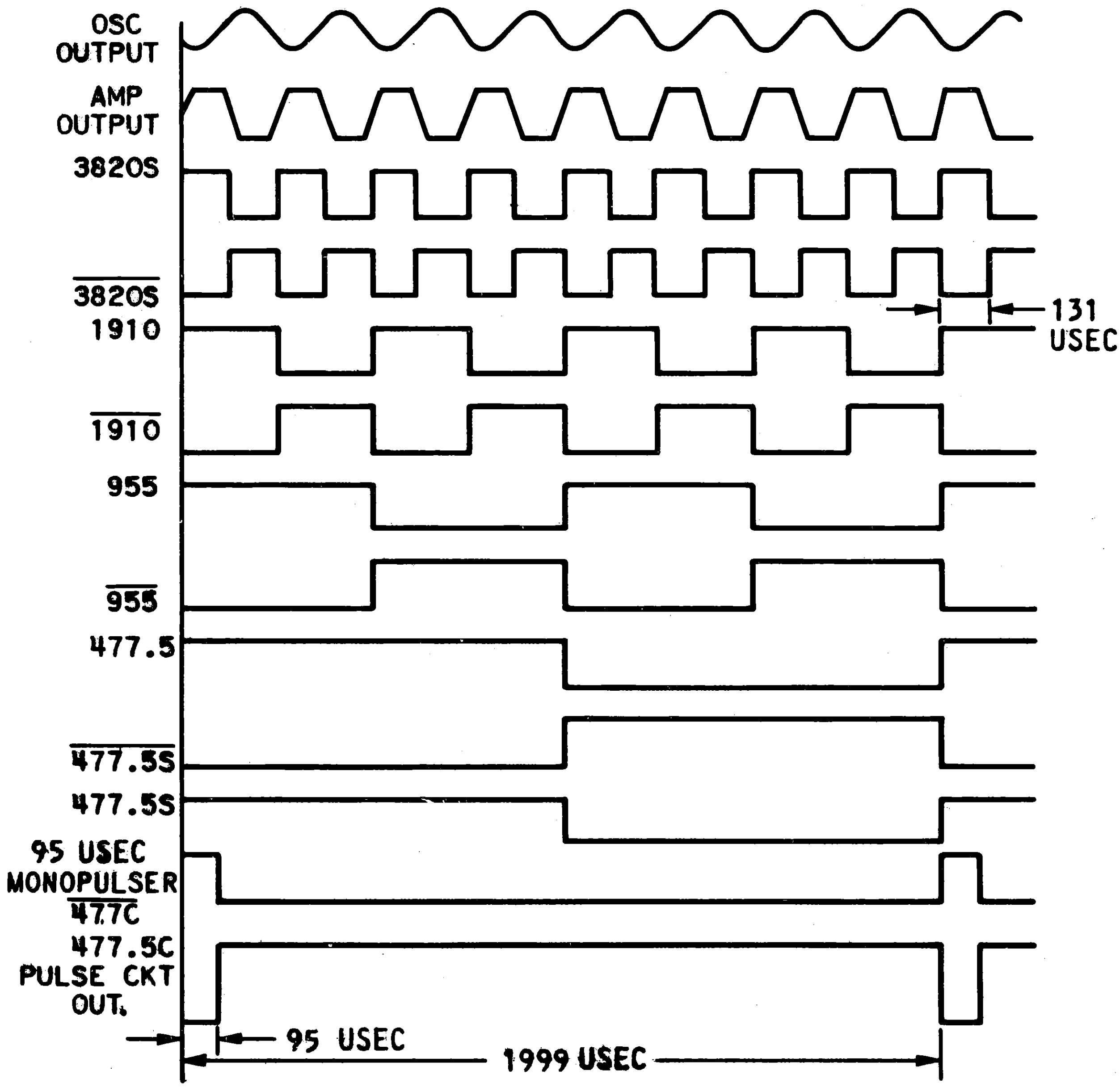
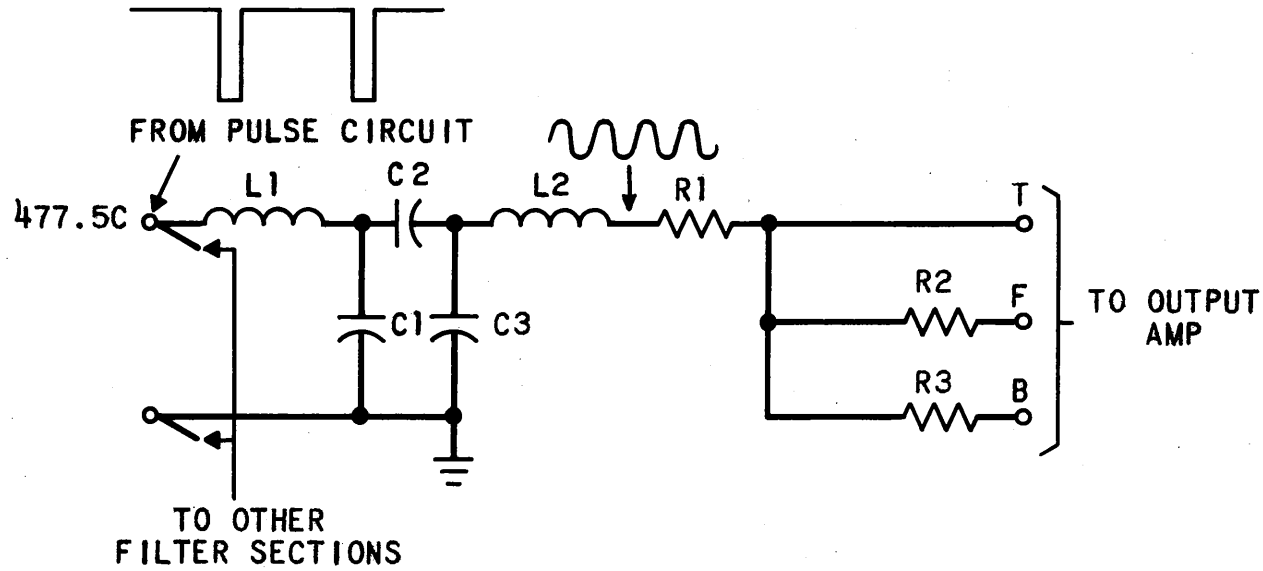
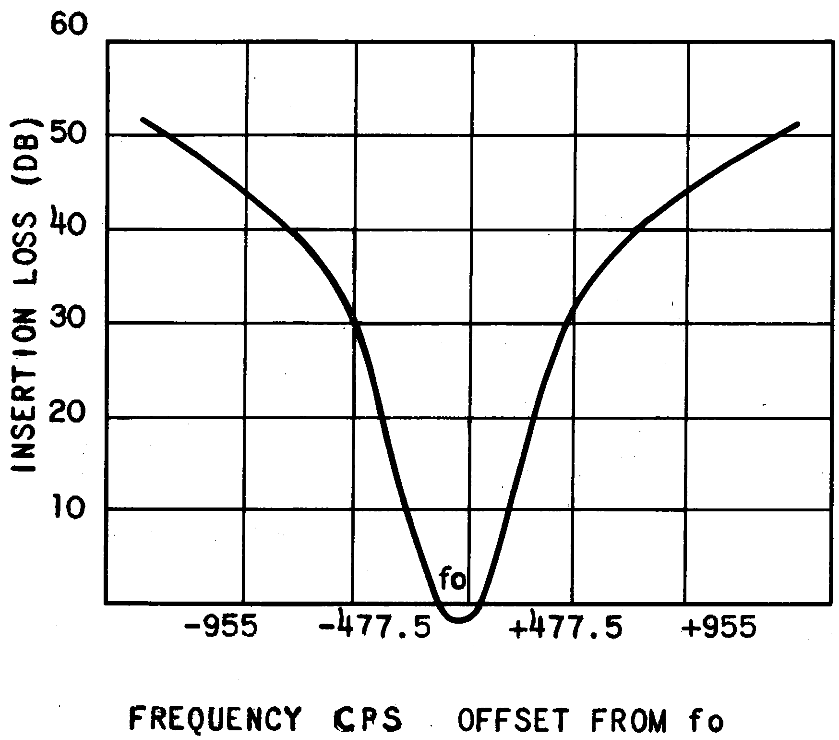



Fig. 9 – Operation Sequence Diagram




| FILTER | SECTION | fo(C.P.S.) |
|---|---|---|
| 621A | 1 | 1910 |
| 621A | 2 | 2387.5 |
| 621A | 3 | 2865 |
| 621A | 4 | 3342.5 |
| 621B | 1 | 5252.5 |
| 621B | 2 | 4775 |
| 621B | 3 | 4297.5 |
| 621B | 4 | 3820.0 |

**Fig. 10 – Circuit Details — 621-Type Filter**

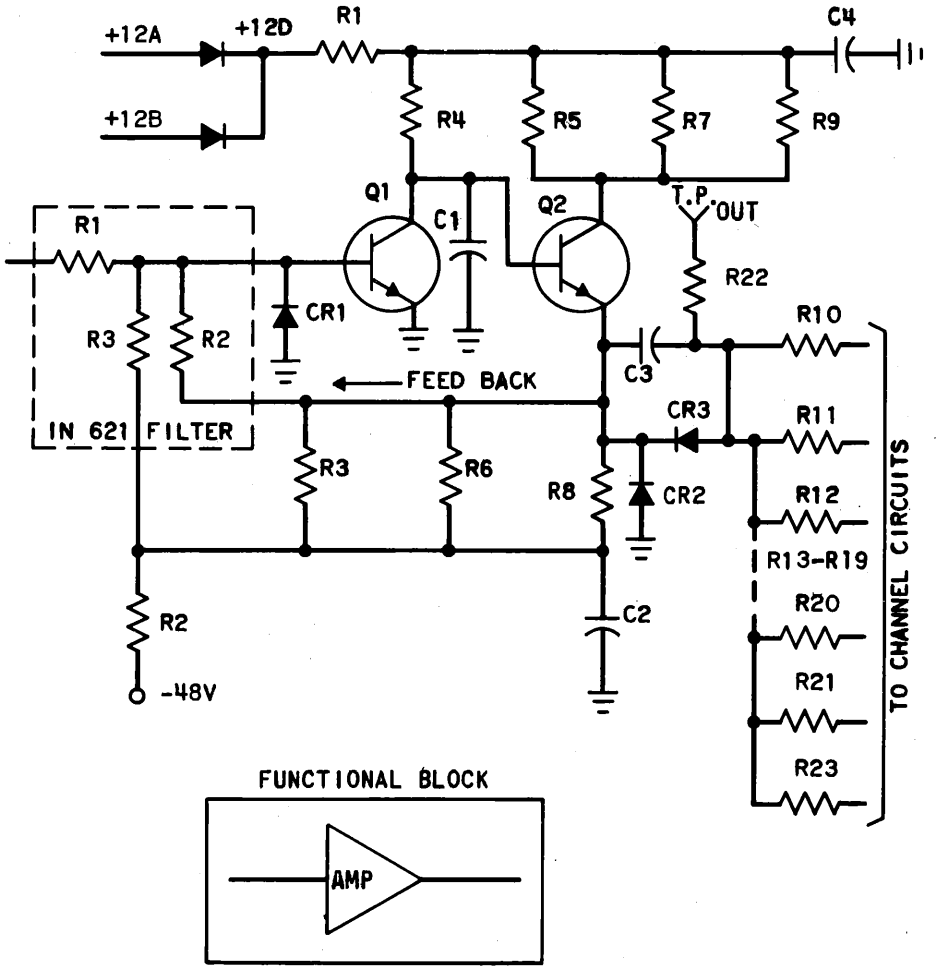



**Fig. 11 – Circuit Details — Output Amplifier**

**5.03** The two transistors Q1 and Q2 of this amplifier are biased class A and dc stabilized by the feedback path from the emitter of Q2 to the base of Q1 via resistor R2 which is within the filter section. Resistor R3 within the filter section in conjunction with R2 fixes the bias condition at the base of transistor Q1.

**5.04** Due to the spectral distribution of the harmonic frequencies of the 477.5-cps pulse train and the variations in the insertion loss (or gain) of the filter sections it was necessary to introduce different amounts of forward gain within each of the eight output amplifiers. This is accomplished by incorporating the resistors R1, R2, and R3, which differ in value for each section of the filter, into the 621-type filters. With this equipment arrangement all of the eight output amplifiers are identical and interchangeable circuit packages.

**5.05** The loop gain, in the baseband, for the output amplifier with two normal Beta transistors is approximately 30 db. The forward voltage gain, between the harmonic of the 477.5-cps pulse train and the output of the amplifier at Q2 is essentially determined by the negative ratio of the feedback resistor R2 to the source impedance as seen looking back into the filter from the base of Q1.

**5.06** Capacitor C1, at the base of Q2 establishes a corner cutoff frequency beyond which the loop gain falls off at 6 db per octive. This provides gain-phase margin against "singing".

**5.07** The distribution circuit for this amplifier is composed of capacitor C3 and resistors R10 through R23. Capacitor C3 provides dc isolation of the output. The resistors R10 through

R23 are a portion of the carrier supply source impedance for the modulator and demodulators of the channel circuits. This means of distribution provides isolation between channels and prevents the disabling of an entire amplifier output by an accidental short on any of the distribution leads.

## 6. ALARM AND LOAD TRANSFER CIRCUITS

### Alarm Functions and Features

**6.01** The carrier supply incorporates two identical frequencies generators. Failure in one brings in a minor alarm and causes the transfer of its supply loads to the second frequencies generator, thus providing continued unimpaired operation of the B1 data carrier terminal units. Concurrent failures in both frequencies generators bring in a major alarm and disrupts service on all the B1 terminals in the bay. An alarm signal to the supervisory signaling circuits causes each of the channels involved to appear busy after a time out interval of approximately 3 seconds. The channels are made busy both at the terminal where the carrier supply failure occurred and at the far end terminal.

**6.02** A failure within either of the frequencies generators is detected for one or more of the following conditions:

- Absence of one or more of the pulse transitions of the 3820- and/or 477.5-cps square-wave clock frequencies to the supervisory signaling circuits.
- Absence of the 477.5-cps pulse train supplied to the 621-type filters.
- A doubling of the counted-down 477.5-cps frequency (ie, if a failure yields 955 cps at the output of the 8:1 countdown circuit).
- Loss of +12 volts and/or loss of −48 volts.

**6.03** The occurrence of a minor alarm due to a failure in one of the frequencies generators causes the following operations:

- A temporary inhibit signal CSS is applied to the supervisory circuits to freeze the ***E*** and ***M*** lead information in the existing state until the transfer of loads to the properly operating frequencies generator is completed.
- The loads for the two supervisory signaling circuits clock frequencies and the pulse train are transferred to the properly working generator.
- The output amplifiers normally associated with the generator in trouble are transferred to an auxiliary −48 volt supply.
- A red trouble lamp TBL is lit steadily or intermittently in accordance with the nature of the trouble.
- Activation of appropriate visual and audible minor office alarms.
- A white guard lamp (CSA or CSB) at the side of the equipment bay-frame will light to indicate which of the generator supplies has failed.

**6.04** Concurrent failures in both of the frequencies generators results in the following major alarm mode of operation:

- A permanent inhibit signal CSS is applied to the supervisory signaling circuits. This causes the channels to be made busy after an approximate 3-second time out.
- Separate red trouble lamps TBL will light steadily or intermittently in accordance with the nature of the trouble within each generator.
- Activation of appropriate visual and audible major office alarms.
- Both white guard lamps (CSA and CSB) at the side of the bay-frame will light indicating that both generators have failed.

**6.05** A red reset key is associated with each of the frequencies generators for manually restoring the loads to normal upon clearing the trouble condition within the faulty generator. Alarm cutoff keys for the office minor and major alarms, ACMN and ACMJ respectively, are provided at the side of the terminal bay-frame.

**6.06** The eight output amplifiers will remain in service at all times provided one of the two −48 to +12 volt power supplies is operative.

This is accomplished by feeding the +12 volts to the amplifiers as indicated in Fig. 11. The power supplies designated +12A and +12B are fed through diodes CR1 and CR2 respectively to a common node designated +12D. A similar diode arrangement is used in the alarm circuits logic to provide +12 volt power.

**Alarm Circuits — Details (See Fig. 12 through Fig. 17)**

**6.07** The alarm and transfer circuits for the carrier supply are composed of two identical sets of logic circuits, and associated transfer relays. One set of logic is associated with frequencies generator A and designated alarm circuit A. A second set associated with generator B is designated alarm circuit B. The transfer relays are designated as ALMA and ALMB.

**6.08** As indicated by functional blocks in Fig. 12 the alarm circuit logic is composed of four detectors, two monopulsers, eight TRL logic gates, a circuit trouble lamp, a control relay circuit, a reset key, and a transfer relay.

**6.09** Detectors 1 and 3 monitor the $\overline{3820}$- and 477.5-cps square wave clock frequencies respectively. Detector 2 monitors the 477.5-cps pulse train. These detectors work in essentially the same manner to detect missing transitions within one or more of the outputs of the frequencies generator. A simplified schematic of a typical detector is shown in Fig. 13. The input to the detector changing from the 0-volt state to the +6 volt state will turn on transistor Q1, thereby discharging capacitor C2. When the input returns to the 0-volt state Q1 will turn off and its collector node starts to rise toward +12 volts with a time constant determined by R2 and C2. This time constant is so adjusted that the voltage at the collector of Q1 will only rise to +4 volts before being reset to 0 volt by the next positive going transition at the input. If the input transitions fail to occur then the collector node of Q1 will rise toward +12 volts breaking down diode CR2 at +6 volts, and thereby supply current through diodes CR2 and CR3 to operate a transistor gate. This initiates the alarm sequence by firing monopulser SMP on Fig. 12.

**6.10** Detector 4, gates 3 and 4, and the monopulser MP are used to detect the doubling in frequency of the 477.5-cps output of the 8:1 countdown circuit. The operation of this circuit is shown functionally in Fig. 14. In normal operation transistor gate 4 is turned on by either the positive portion of the input square wave or the positive portion of the output signal at gate 3. The output pulse width from the monopulser (MP) is so adjusted that if the input frequency doubles then gate 4 will not be turned on at all times: hence, we will get a train of positive pulses at DB, while DB1, the output of detector 4, will rise from the normal state of 0 volt to the +6-volt alarm state. DB or DB1 will initiate the alarm by firing the monopulser SMP shown in Fig. 12.

**6.11** As indicated there exists multiple paths through which the carrier supply alarms may be initiated. Thus, except for a few critical components the alarm can be initiated even though a component failure may exist within the alarm circuits.

**6.12** When the alarm sequence is initiated by a signal output from one or more of the detectors it causes gate 1, in Fig. 12, acting as an OR gate to all inputs, to be turned on thereby turning off gate 2. Gate 2 turning off will thereby fire the monopulser SMP. The output of this monopulser $\overline{CSS}$ is inverted and amplified by gate 8 and is the temporary inhibit signal CSS transmitted to the supervisory signaling circuits within the bay. The CSS output is fed back to turn on gate 5, and holds gate 5 turned on, thereby operating the circuit trouble lamp and turning gate 7 off. When gate 7 turns off this will turn off Q11 and cause the ALM relay to release (see Fig. 15). Relay ALM releasing will release the slave relay ALM- by opening its holding path through a front contact of ALM. Upon release of relay ALM the path between the collector of Q5 through resistor R19 to the base of Q11 is opened by a front contact. The purpose of this arrangement is to prevent relay ALM from reoperating if the alarming sequence was initiated by an intermittent trouble which may clear itself.

**6.13** The circuit trouble lamp indicated on Fig. 12 is used for maintenance purposes. If this lamp is lit then there exists a permanent trouble condition within the frequencies generator. The lamp flashing indicates that there exists an intermittent trouble within the generator.

**6.14** The reset key on Fig. 12 and 15 is used to manually reset to normal the proper distribution of loads from the frequencies generators. No attempt to reset should be made if the red trouble lamp is lit or flashing. Upon clearance of trouble condition the red trouble lamp will be extinguished and transistor gate 1 will be turned off while gate 6 will be turned on. Gate 6 being turned on will cause the collector of transistor Q2, Fig. 15, to be at 0 volt. Thus, pushing the reset key will turn on transistor Q11 through the path established from its base through R29 and the front contact of the reset key. When Q11 turns on relay ALM will operate which in turn will operate its slave relay ALM- and thereby cause the load transfers. Pushing of the reset key will also fire monopulser SMP by applying a positive voltage, the output of gate 1, through its front contact as shown in Fig. 12. The purpose of firing the monopulser SMP upon resetting is to transmit the temporary inhibit signal CSS to the supervisory signaling circuit. Since the output of this monopulser is fed back to gate 5 and held there for 110 milliseconds, the duration of the SMP monopulser, the reset key must remain depressed for a minimum of 110 milliseconds so that the ALM relay will remain operated.

**6.15** The transfer of loads from one frequencies generator to the other is accomplished via the non-continuity transfer contacts of the slave relays ALMA and ALMB as shown on Fig. 16. As indicated by this figure, series resistance is inserted at the carrier supply on the ***3820,477.5,*** and ***CSS*** leads to the supervisory signaling circuits. Thus, a trouble short to ground on any one of these leads, beyond the carrier supply distribution circuit, will create a failure in only one of the six possible data carrier terminal units within the terminal frame. The operation of the proper office alarm circuits and the switching of −48 volt supply to the output amplifiers is also realized by a contact network of the slave ALMA and ALMB relays.

**6.16** Fig. 17 is a simplified functional schematic, for alarm circuit A, indicating the circuits by which the CSS inhibit signal is distributed to the supervisory signaling circuits. A duplicate of this circuit is also used for alarm circuit B. In the normal non-alarm mode of operation the output of gate No. 8 (approximately +6 volts) is transmitted to the supervisory signaling circuits through the front contacts of relays ALM and ALMB in parallel. The diode CR is back biased due to the ground on its anode. Upon failure in frequencies generator A the SMP monopulser is fired, thereby turning on gate No. 8 in both alarm circuits A and B for approximately 110 milliseconds. The CSS signals will then go to the 0-volt state for the 110 millisecond duration of the monopulser thereby informing the supervisory signaling circuit of the switching within the carrier supply. The purpose of diode CR and resistor R to +12 volts from the lead designated TSCC is to supply a positive voltage, of approximately +6 volts, to the ***CSS*** leads under the condition that the circuit package on which gate No. 8 is located may be removed from the carrier supply for maintenance purposes. Removal of this circuit package from its connector will lift the ground on the anode of diode CR thereby applying a positive voltage to lead ***CSS,*** provided that frequencies generator B is operating normally. Upon concurrent failures in frequencies generators A and B both ALM relays and slaves ALMA and ALMB will be released. The ***CSS*** leads will be "floated" due to the open contacts in their transmission paths, thereby indicating a permanent inhibit signal to the supervisory signaling circuits in the terminal frame.

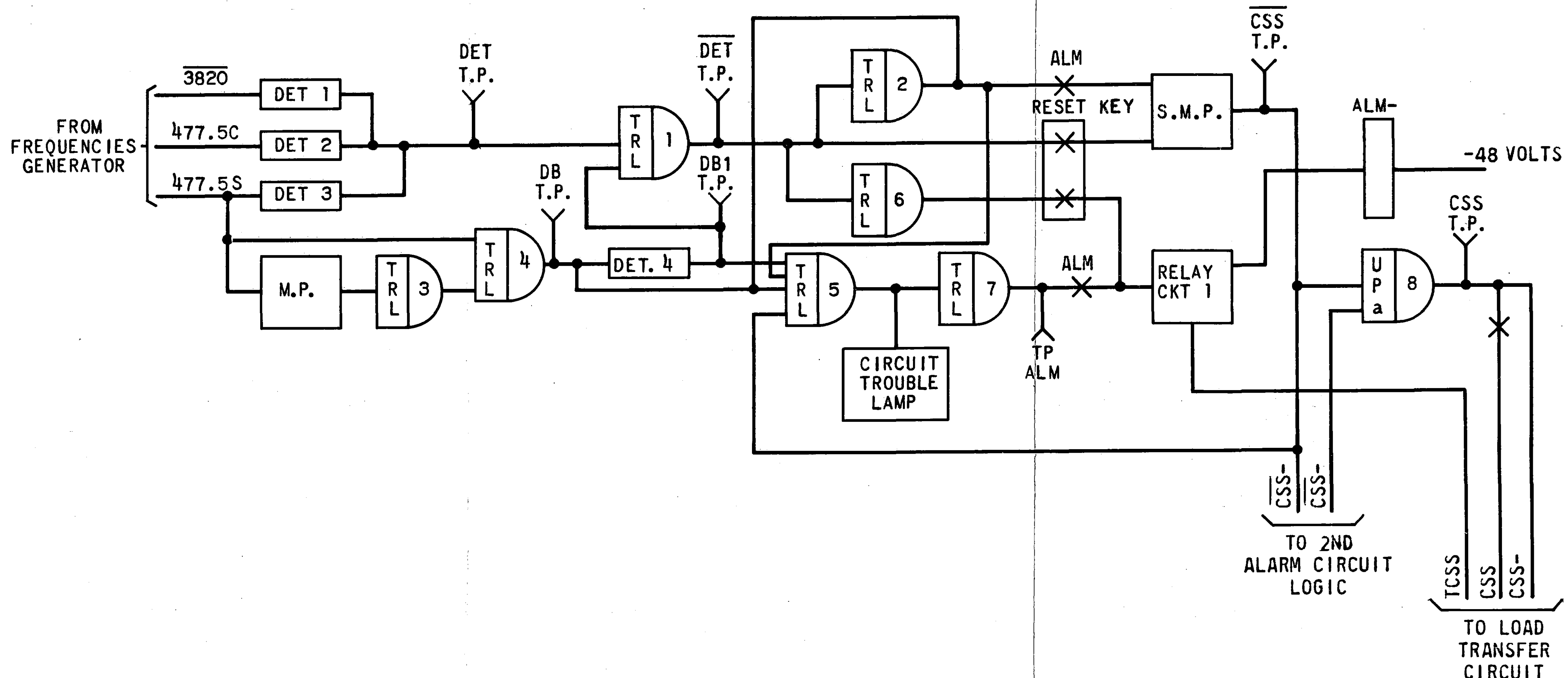



**Fig. 12 — Alarm Circuit Functional Diagram**

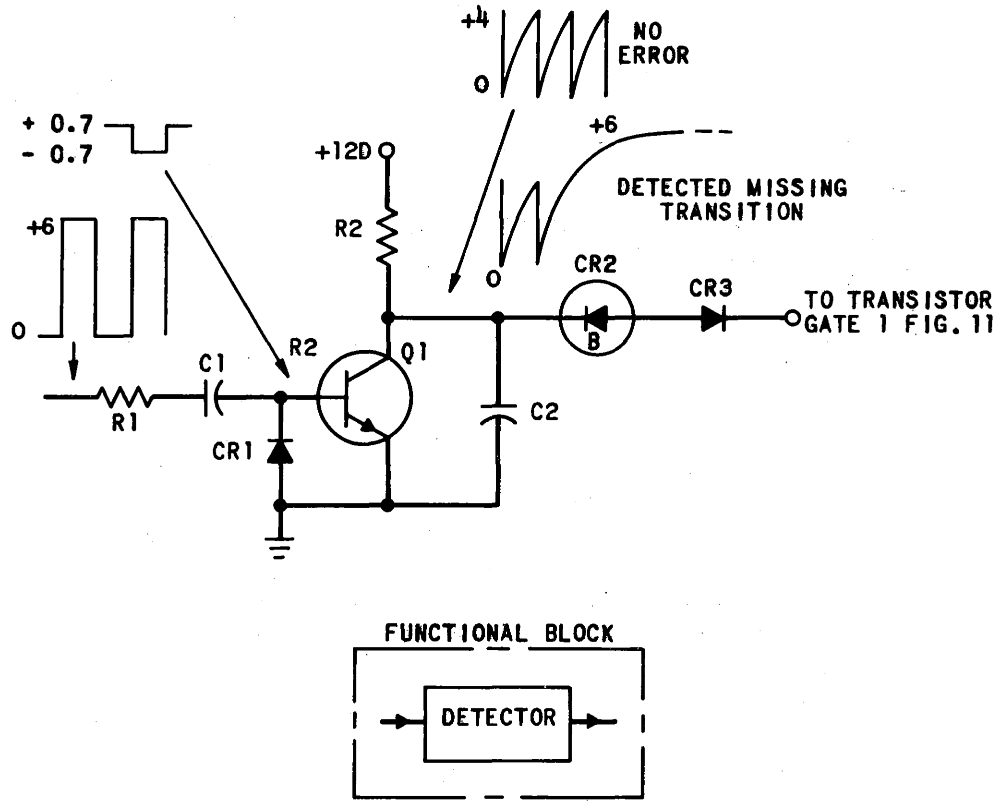



**Fig. 13 – Detector — Simplified Schematic**

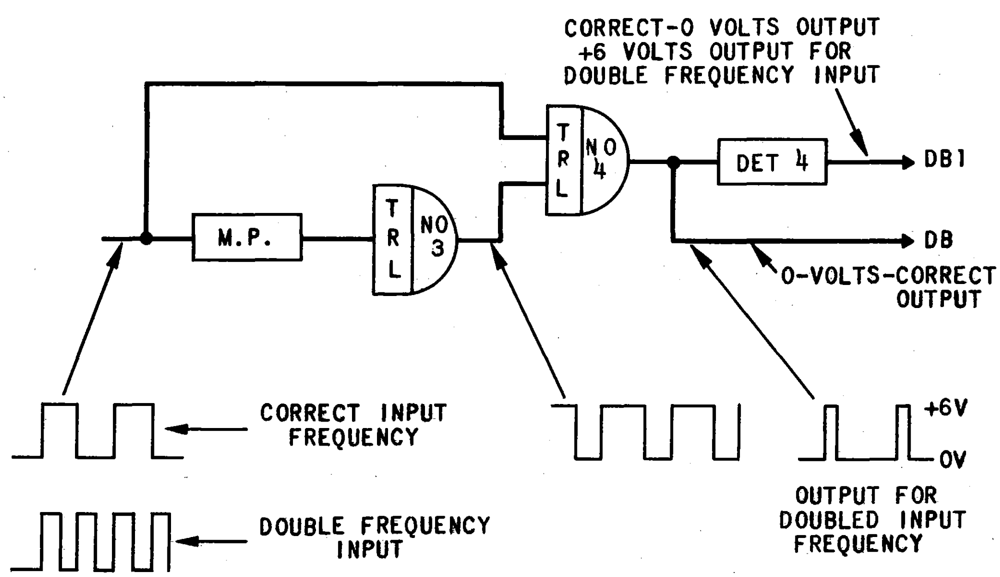



**Fig. 14 – Frequency Double Detector**

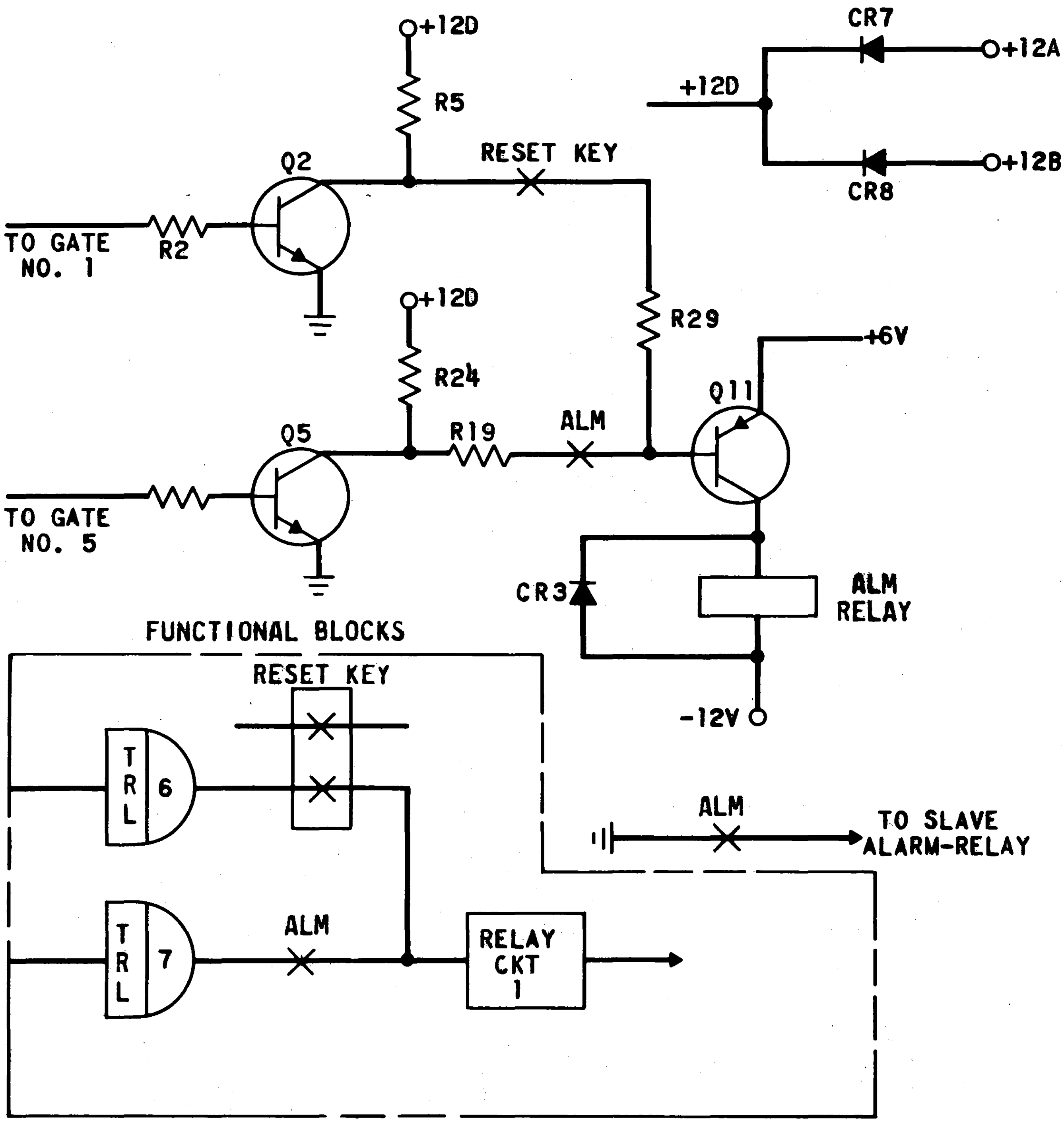



Fig. 15 – Relay Circuit 1 Control

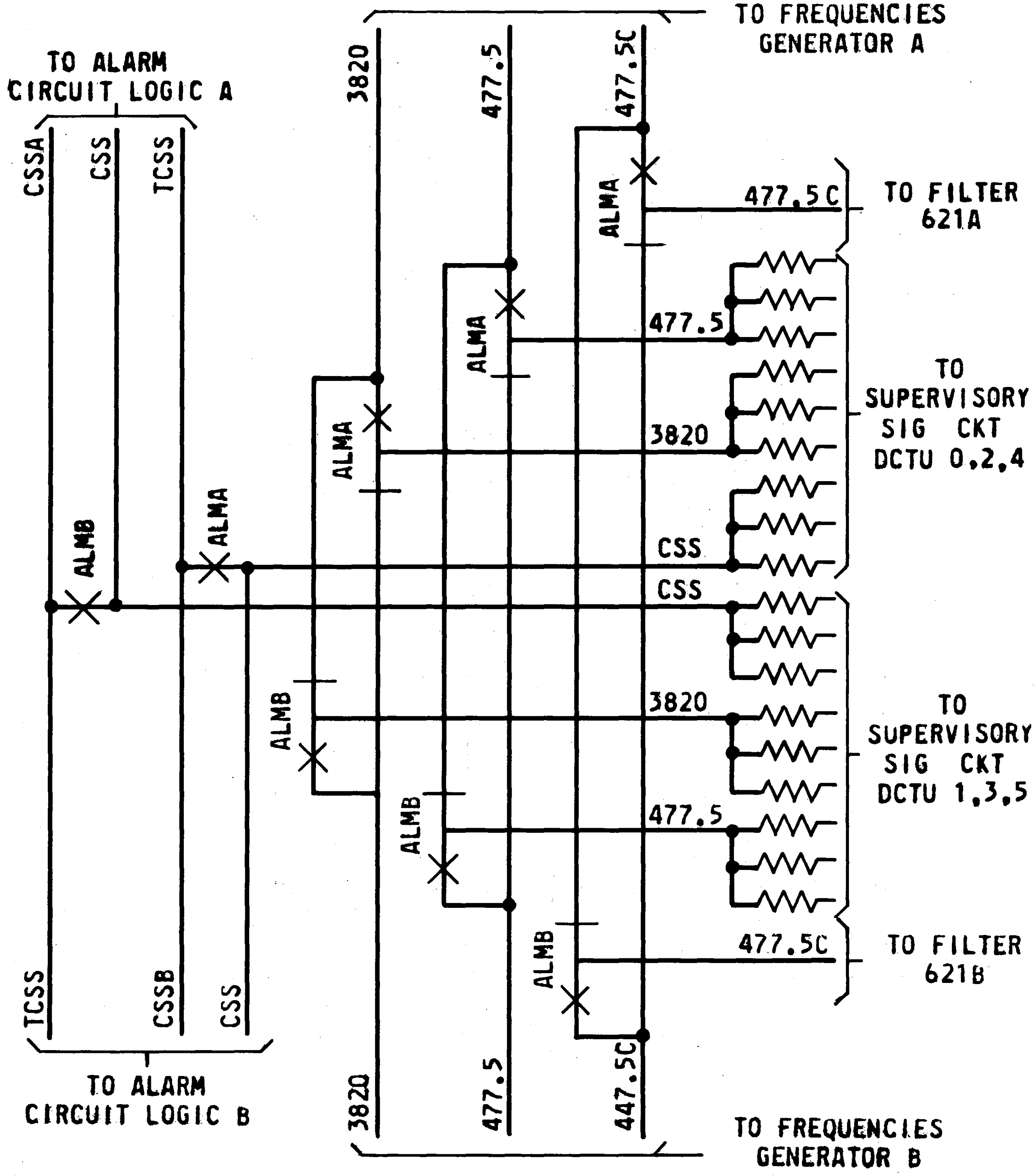



Fig. 16 — Load Transfer Circuit

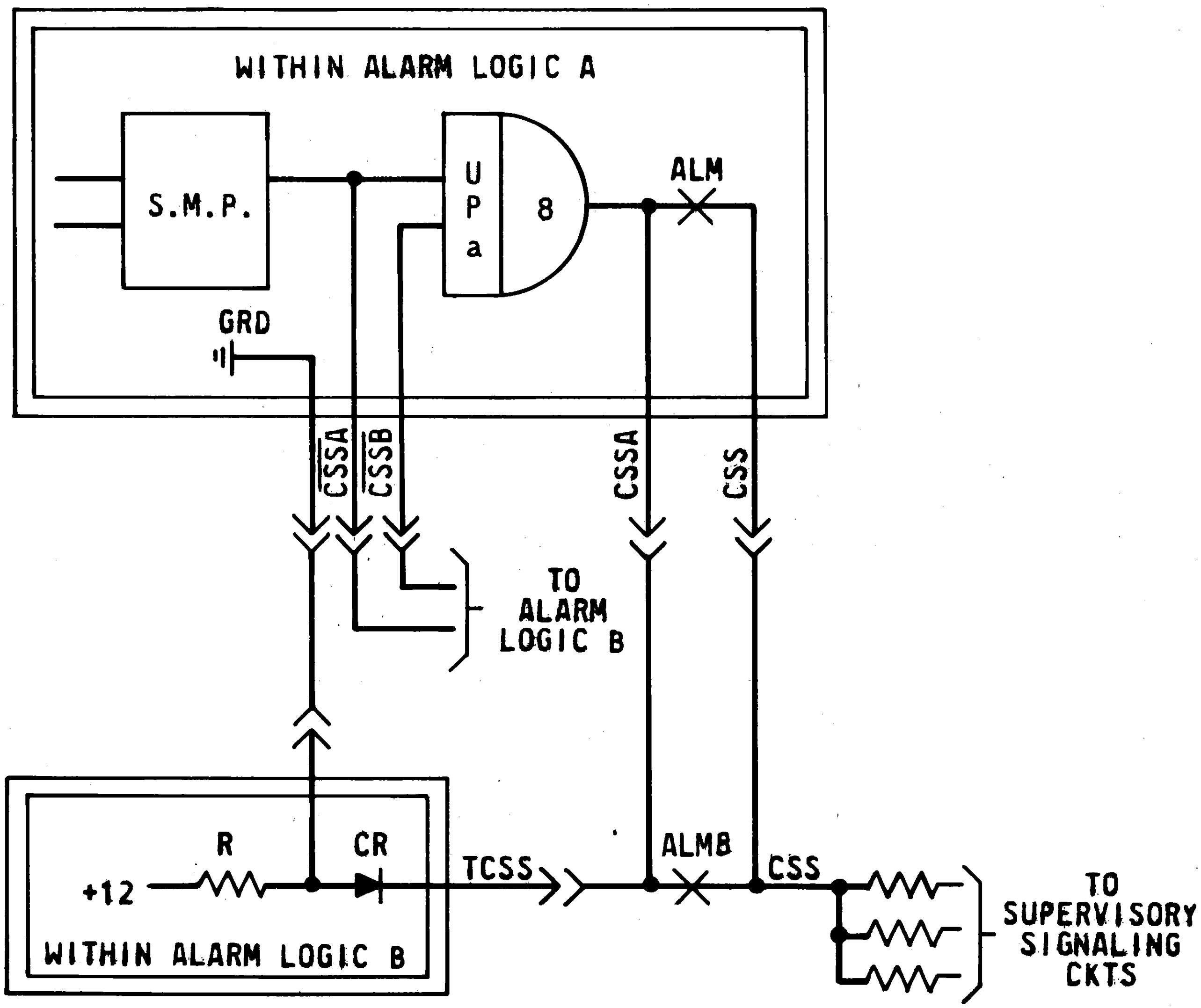



Fig. 17 — CSS Distribution