Critical Release Notice

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The content of this customer NTP supports the SN06 (DMS) software release.

Bookmarks used in this NTP highlight the changes between the NA015 baseline and the current release. The bookmarks provided are color-coded to identify release-specific content changes. NTP volumes that do not contain bookmarks indicate that the NA015 baseline remains unchanged and is valid for the current release.

Bookmark Color Legend

Black: Applies to content for the NA015 baseline that is valid through the current release.

Red: Applies to new or modified content for NA017 that is valid through the current release.

Blue: Applies to new or modified content for NA018 (SN05 DMS) that is valid through the current release.

Green: Applies to new or modified content for SN06 (DMS) that is valid through the current release.

Attention!
Adobe Acrobat Reader 5.0 is required to view bookmarks in color.

Publication History

September 2003

For the SN06 (DMS) release, 11.01, the following changes were added:

Volume 1

- No changes

Volume 2

- No changes

Volume 3

- No changes

Volume 4

- No changes

Volume 5

- Updates were made to NT9X76AA according to CR Q00177945.

297-8991-805

DMS-100 Family

Hardware Description Manual

Volume 1 of 5

2001Q1 Standard 09.01 March 2001

NORTEL NETWORKS

How the world shares ideas.

DMS-100 Family

Hardware Description Manual

Volume 1 of 5

Publication number: 297-8991-805
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About this document

When to use this document

This document describes DMS-100 circuit cards, frames, and shelves. These hardware descriptions help operating company personnel isolate faults and provision offices. This manual is used for operating company personnel in maintenance and provisioning.

How to check the version and issue of this document

The version and issue of the document are indicated by numbers, for example, 01.01.

The first two digits indicate the version. The version number increases each time the document is updated to support a new software release. For example, the first release of a document is 01.01. In the *next* software release cycle, the first release of the same document is 02.01.

The second two digits indicate the issue. The issue number increases each time the document is revised but rereleased in the *same* software release cycle. For example, the second release of a document in the same software release cycle is 01.02.

To determine which version of this document applies to the software in your office and how documentation for your product is organized, check the release information in the *DMS-10 and DMS-100 Family Product Documentation Directory,* 297-8991-001.

This document is written for all DMS-100 Family offices. More than one version of this document may exist. To determine whether you have the latest version of this document and how documentation for your product is organized, check the release information in the *DMS-10 and DMS-100 Family Product Documentation Directory,* 297-8991-001.

General specifications

As a result of the DMS-100 customer documentation restructure program, General Specifications (GSs) are integrated in this manual. This integration started in BCS36.

Information that was in General Specification documents is now in hardware description documents. Hardware descriptions now have product engineering codes (PEC). These codes have the prefix NT instead of GS. For example, a GS0X42 now is an NT0X42AA. When a product is updated, the suffix of the product changes. For example, NT0X42AA changes to NT0X42AB.

Note: The PECs do not always relate to a hardware description designated GS. A specified product does not always have a GC.

Hardware descriptions do not normally have descriptions like the descriptions of GS because of the nature of the HDM. Refer to The organization of this document.

Document organization

This document contains descriptions of circuit card, frame and shelf descriptions. Each description has a separate section. The sections are arranged in alphanumeric order according to the PEC. Cards, frames and shelves can appear in the same section in PEC order.

The PEC includes the version suffix for each component (examples: AA, AB, CA). This document provides a separate description for each version of the component.

Customers can order the components described in this document as provisionable items or as spare or replacement items. The size of the office, office traffic capacity requirements or office feature requirements provide a basis for the quantities necessary.

This document does not include descriptions of components that are internal to, or subunits of, equipment ordered under a certain PEC.

Standard headings

The PEC appears at the top of the page for each description. The name of the component follows the PEC. Each PEC description has numbered pages. The PEC appears as a header at the top of each page.

If the component is a frame or shelf, the following standard headings are in the text:

- Description
  - — includes physical and functional descriptions
- Components
  - — identifies each component with PEC and describes the function of the components
- Design
  - — a diagram of the component illustrates the arrangement of subcomponents

If the component is a card, some or all of the following headings appear. These headings appear if the headings apply to the card:

- Product description
- Functional description
  - — includes a description and diagram of functional blocks on the card
- Signaling
  - — can include pin-out diagrams and timing diagrams
- Technical data
  - — includes power requirements

Where to find information

The circuit card descriptions in this manual contain references to shelves and card slots where the cards can be located. Normally, card locations are not specified.

The task-oriented Nortel publications (NTP) contain installation, verification and maintenance procedures for circuit cards . These NTPs can associate with specified products or can apply to base DMS-100 maintenance. Refer to the *DMS-10 and DMS-100 Family Product Documentation Directory*, 297-8991-001, to identify NTPs.

CAUTION
Potential loss of service
Do not use this reference manual as a guide to procedures for installation or maintenance of DMS-100 Family equipment. Consult the *DMS-10 and DMS-100 Family Product Documentation Directory*, 297-8991-001, to identify the correct document for the job.

Common technical data

All circuit cards in the DMS-100 Family of switches operate under the range of environmental conditions in this section. Northern Telecom Technical Specification contains this information.

Ambient temperature and humidity

Operations are separated into normal conditions and short-term conditions.

Normal conditions can range in temperature from 5°C to 38°C (40°F to 100°F). This condition applies if the monthly average for the upper range does not exceed 30°C (86°F). The system meets all performance and reliability parameters in this temperature range. At an ambient temperature that cannot exceed 21°C (70°F), a relative humidity of 80% is acceptable. At an ambient temperature of 49°C (120°F), the maximum relative humidity is 30%.

The rate of temperature change must not exceed 6.7°C (12°F) per hour.

Short term conditions are 72 continuous hours and 15 days maximum for each year.

Temperature and humidity are measured at 1.254 m (5 ft) above floor level and mid-aisle. Temperature and humidity are measured at 380 mm (15 in.) in front of the equipment. Take the lower temperature and humidity reading.

What precautionary messages mean

The types of precautionary messages used in Nortel Networks documents include attention boxes and danger, warning, and caution messages.

An attention box identifies information that is necessary for the proper performance of a procedure or task or the correct interpretation of information or data. Danger, warning, and caution messages indicate possible risks.

Examples of the precautionary messages follow.

ATTENTION
Information needed to perform a task

ATTENTION
If the unused DS-3 ports are not deprovisioned before a DS-1/VT Mapper is installed, the DS-1 traffic will not be carried through the DS-1/VT Mapper, even though the DS-1/VT Mapper is properly provisioned.

DANGER
Possibility of personal injury

DANGER
Risk of electrocution
Do not open the front panel of the inverter unless fuses F1, F2, and F3 have been removed. The inverter contains high-voltage lines. Until the fuses are removed, the high-voltage lines are active, and you risk being electrocuted.

WARNING
Possibility of equipment damage

WARNING
Damage to the backplane connector pins
Align the card before seating it, to avoid bending the backplane connector pins. Use light thumb pressure to align the card with the connectors. Next, use the levers on the card to seat the card into the connectors.

CAUTION
Possibility of service interruption or degradation

CAUTION
Possible loss of service
Before continuing, confirm that you are removing the card from the inactive unit of the peripheral module. Subscriber service will be lost if you remove a card from the active unit.

1 NT0Xnnaa

NT0X02AB through NT0X91KA

NT0X02AB

Product Description

The NT0X02AB has three other names. The selection of name depends on the application:

- Miscellaneous equipment frame (MIS)-when a DMS-100 Family office uses the NT0X02AB.
- Remote service equipment frame (RSE)-when a DMS-100 remote line module (RLM) office uses the NT0X20B
- Remote miscellaneous equipment frame (RME)-when a DMS-100 remote line concentrating module (RCLM) or a DMS-100 remote switching center (RSC) office uses the NT0X02AB.

The MIS/RSE/RME is a general purpose equipment frame. This frame accommodates different DMS, common systems and other hardware a DMS office or remote site requires.

Provisionable multi-fuse frame supervisory panels (FSP) and grounding hardware provide full flexibility in the use of the frame.

Parts

The NT0X02AB consists of different equipment shelves and a *collection* of some of the following components:

- NT0X88AB-Miscellaneous equipment FSP
- NT0X88AD-RSE FSP
- NT0X88AE-10-A, filtered miscellaneous equipment FSP
- NT0X88AF-20-A, filtered miscellaneous equipment FSP
- NT3X25BA-Terminal block assembly
- NT3X25BB-Terminal block assembly
- NT5X98AA-Auxiliary fuse panel for TOPS, ESAC

Miscellaneous equipment frame supervisory panel

NT0X02AB FSP is the default FSP. Use the NT0X02AB unless a need for one of the other provisionable FSPs is present.

Remote service equipment frame supervisory panel

Provide one NT0X88AD RSE FSP for each NT0X02AB frame when an RLM office uses the NT0X02AB.

10-A, filtered miscellaneous equipment FSP

Provide one NT0X88AE 10-A, filtered FSP for each NT0X02AB frame. Perform this action when any of the different circuits require 10-A, filtered, -48V circuit breakers. An example of a different circuit is a remote office test line unit.

20-A, filtered miscellaneous equipment FSP

Provide one NT0X88AF 20-A, filtered FSP for each NT0X02AB frame. Perform this action under the condition that follows. When up to 24 (48-V filtered) alarm battery supply fuses and two 10-A circuit breakers (filtered) are required to power one of the following:

- two Bell Labs fire report systems
- 15 centralized automatic message accounting (CAMA) units
- one resistor-transistor logic (RTL) unit and up to six CAMA units

The FSP cannot exceed 10 A on any feed.

Terminal block assembly

Provide NT3X25BA terminal block assemblies, as required, to locally cross-connect MIS-frame-mounted equipment, like a bank of modems.

Terminal block assembly

Provide NT3X25BB terminal block assemblies, as required for DMS-250, in place of the distribution frame for cabling and cross-connecting.

Auxiliary fuse panel for TOPS, ESAC

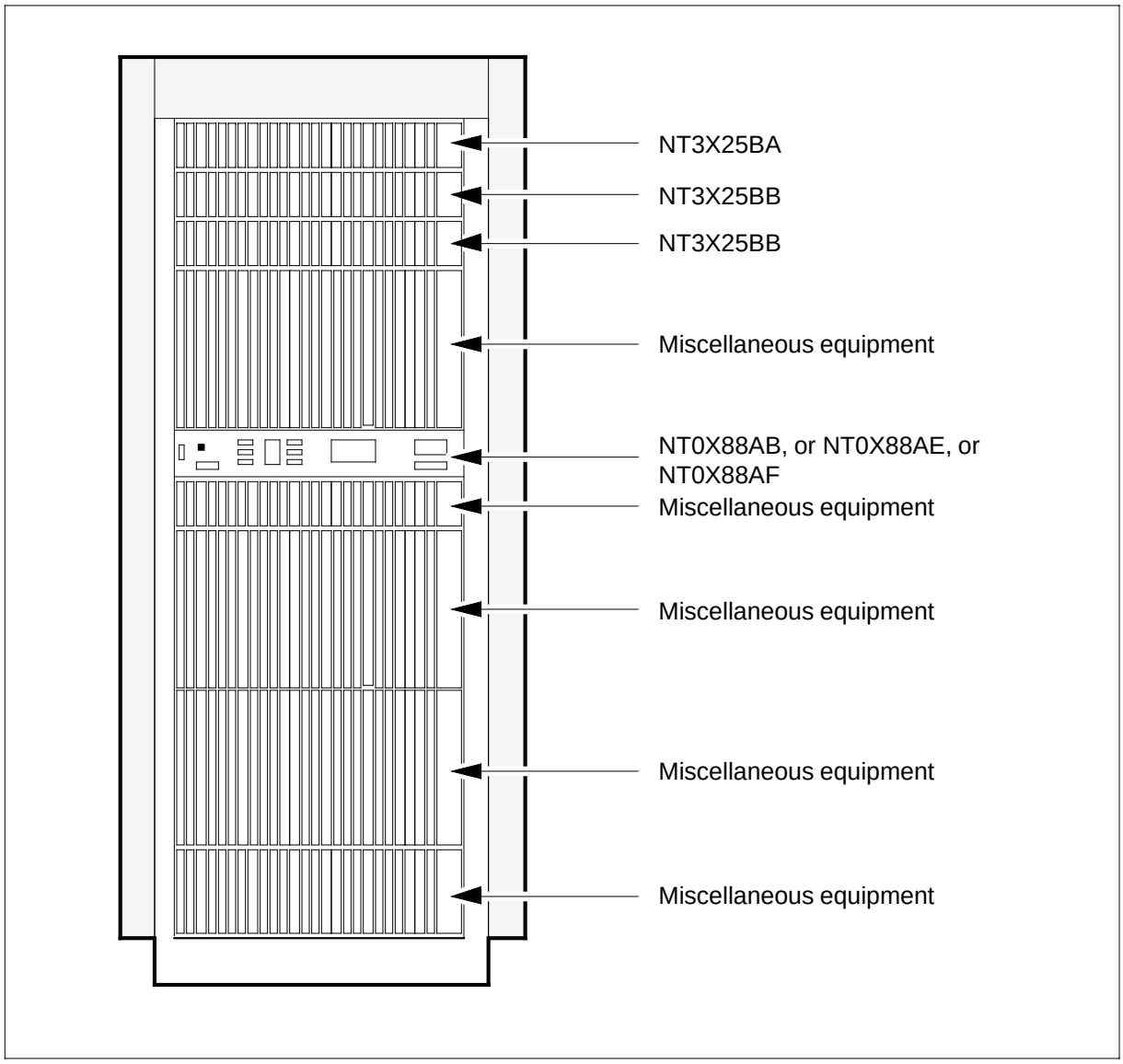
Use one NT5X98AA auxiliary fuse panel when a TOPS position requires fusing. You can power a maximum of 30 TOPS positions.

Design

The design of the NT0X02AB appear in the following figures.

NT0X02AB (continued)

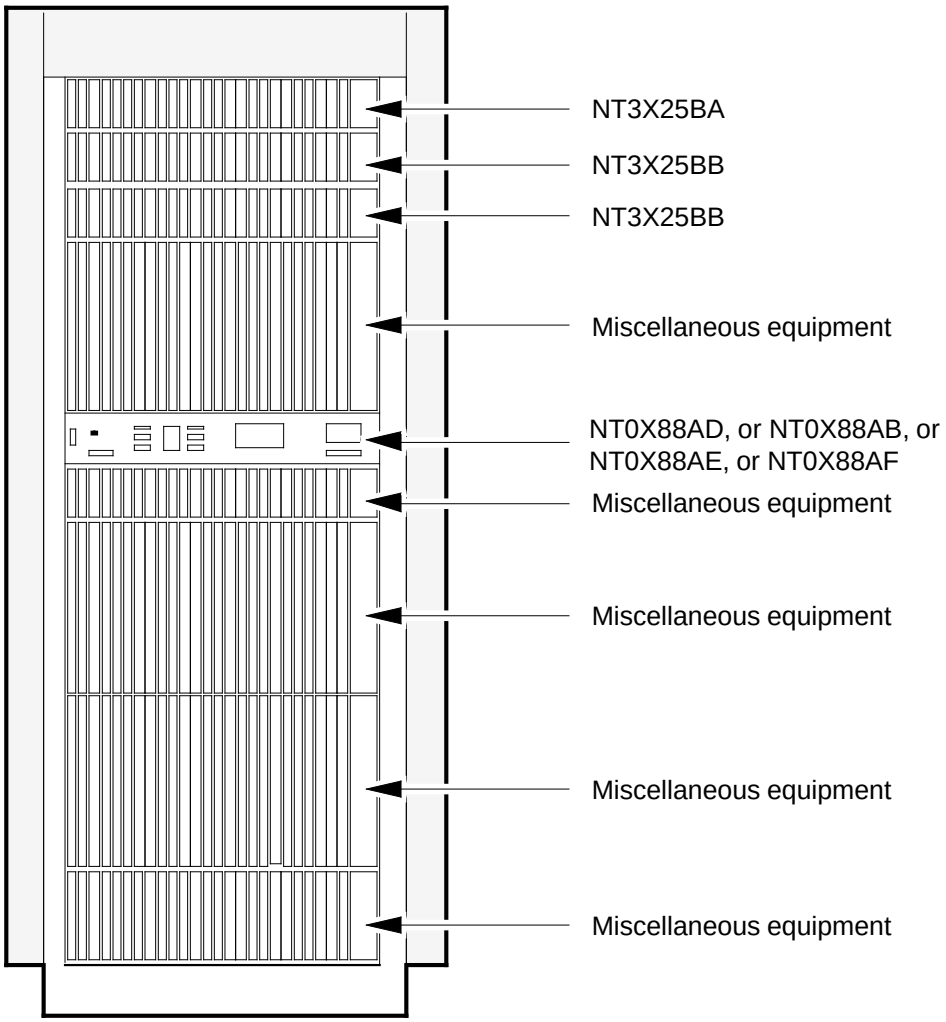
NT0X02AB miscellaneous equipment frame components



Note: This diagram is not to scale.

NT0X02AB (end)

NT0X02AB remote service equipment frame or remote miscellaneous equipment frame components



Note: This diagram is not to scale.

NT0X10

Product description

The miscellaneous scan detector card determines the state of a variety of equipment in the DMS-100 Family of digital switching systems. Different states include alarm conditions, like blown fuses and open doors. Control signals from the maintenance trunk module (MTM) or office alarm unit (OAU) activate scan detector circuits. The scan detector circuits require two trunk appearances.

The NT0X10 card contains 14 scan detector circuits for each card and provides a self-test mode. This self-test mode verifies the scan detection circuits under software control. You can configure this card as a loop detector, ground detector, or battery detector.

Location

The miscellaneous scan detector occupies one card position in the MTM or OAU. Normally, all scan detector external input leads are cabled to the office distributing frame to facilitate job engineering.

Functional description

You can configure each scan detector circuit card as a loop, group, or battery detector with manual settings of miniature switches S1-A and S1-B. The Technical Data section labelled Configuration specifications presents the selection of input options instead of switch settings.

Communication from the MTM to the miscellaneous scan detector card occurs through the receive data (RDAT) bus in the MTM. Communication from the card to the MTM occurs through the transmit data (XDAT) bus in the MTM.

Note: The NT2X58 describes relationships between the trunk logic circuits (TLC), the RDAT bus, the XDAT bus, the enable signals and the other components of the MTM.

Each scan detector card has two TLCs (TLC-0 and TLC-1) that interface the MTM buses to the scan detector. Each TLC interfaces with seven scan detector circuits. The number of scan detector cards in the MTM depends on the job engineering requirements.

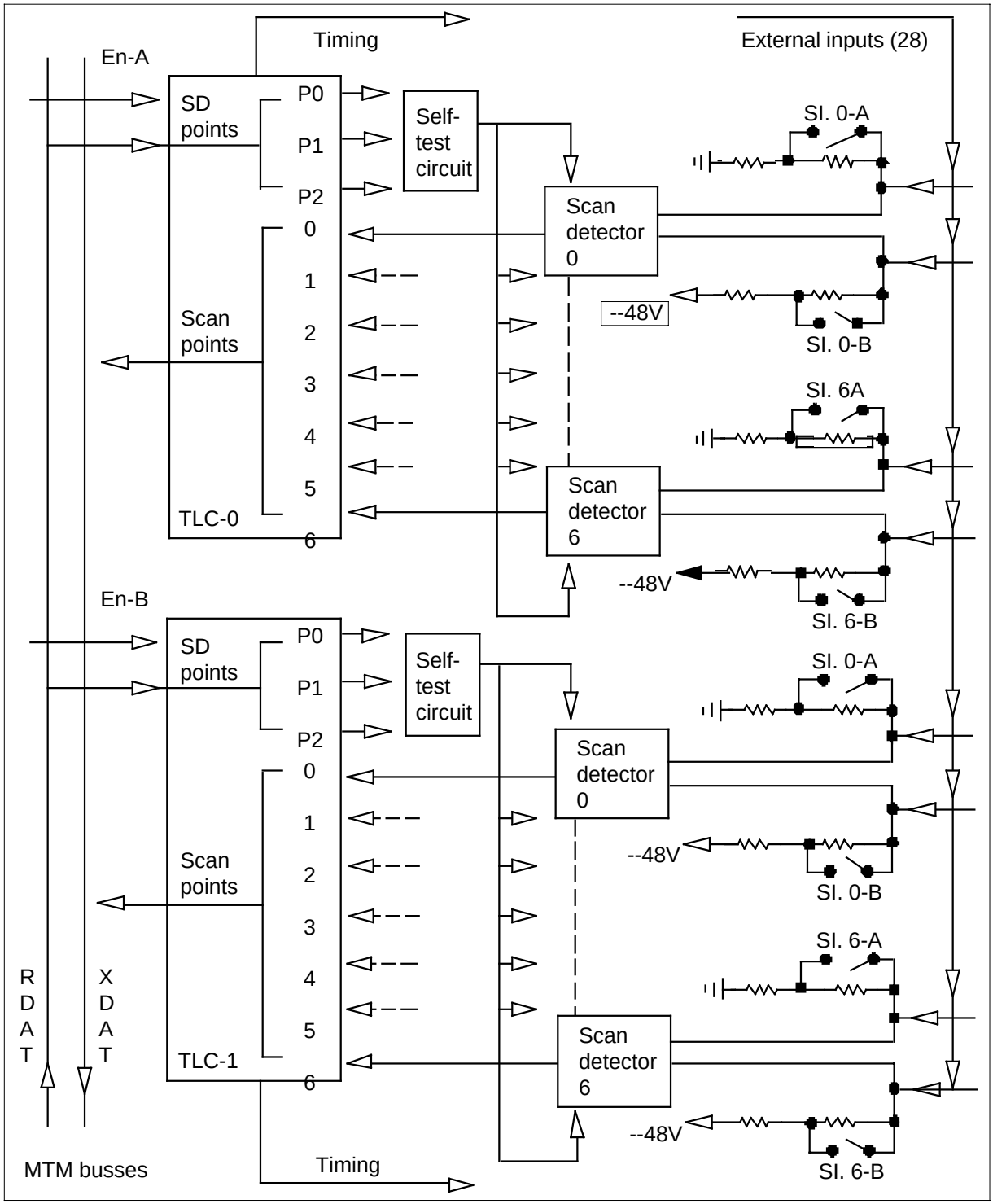
Each self-test circuit controls the test mode of seven scan detector circuits. The self-test circuits force the scan detector to the self-test mode. This event occurs after the scan detects or receives control signals the MTM or OAU send through the RDAT bus TLC signal distribution (SD) points.

Functional blocks

A diagram of the functionality of the miscellaneous scan detector card appears in the following figure.

NT0X10 (continued)

NT0X10 functional blocks



Technical data

This section describes the technical specifications for the miscellaneous scan detector card. The specifications include power requirements, configuration specifications, environmental conditions and equipment dimensions.

Power requirements

The power requirements for the miscellaneous scan detector card appear in the following table.

Power requirements

Voltages required	+5 V	+12 V	-15 V	-48 V
Current required	90 mA	32 mA	28 mA	2 mA

Configuration specifications

When the scan detector circuit is configured as a loop detector, the appropriate switch position is both closed. When the scan detector circuit is configured as a ground or battery detector, the appropriate switch position is both open.

Other configuration specifications appear in the following table.

Configuration	Options
Loop detector	Maximum nonoperate loop resistance is 11500 ohms. Minimum operate loop resistance is 6980 ohms.
Ground detector	Maximum nonoperate ground resistance is 11500 ohms. Minimum operate ground resistance is 6980 ohms.
Battery detector	Maximum nonoperate condition is -52V with a source resistance of 12400 ohms. Minimum operate loop condition -52V with source resistance of 6980 ohms.

NT0X10 (end)

Environmental conditions

The miscellaneous scan detector card performs under limited environmental constraints. These constraints appear in the following table.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	10°C to 30°C (50°F to 86°F)	5°C to 49°C (41°F to 120.2°F)
Humidity	20% to 55%	20% to 80%

Equipment dimensions

The miscellaneous scan detector card dimensions are 317.5 mm (12.5 in.) in height and 254 mm (10 in.) in depth.

NT0X28AF

Product Description

The NT0X28AF frame supervisory panel (FSP) contains power control and alarm circuits. These circuits provide interfaces between the power distribution center (PDC) and the equipment frames of the DMS-100 Family digital switching system. The FSP also provides a focal point to allow operating company personnel to monitor the switching system.

The NT0X28AF provides alarms to indicate problems in the central control complex (CCC) frame. An example of a problem is a fan or power converter unit that does not work. The FSP provides controls, like those for manual override of an alarm. The FSP provides test facilities, like the four service jacks that provide access to two telephone lines (TEL-A, TEL-B) and two data lines (DATA-A, DATA-B).

The power control and alarm circuits are on circuit packs (CP) NT0X36AB power control and alarm (PCA).

Parts

NT0X28AF contains the following parts:

Power control

The NT0X28AF FSP contains two identical NT0X36AB PCA CPs, designated PCA-1 and PCA-2. Each PCA contains two power control circuits and one alarm circuit.

The four -48V feeds from the PDC frame connect to PCA-1 and PCA-2 through fuses F01 through F04.

Power control -1 in PCA-1 is standard for of all four power control circuits. The power control consists of an electronically-controlled switch A1. Switch A1 closes the -48V feed from F01 to shelf 65 of the frame. This frame contains the FSP. This action occurs when the power-up inputs ON/OFF and RESET are applied in the correct sequence. The ON/OFF and RESET inputs connect to the ON/OFF switch and RESET buttons. The ON/OFF switch and reset buttons are on the faceplate of the power converters in shelf 65.

When OFF, the ON/OFF switch in the converter maintains a closed circuit to the battery return (BR). This action holds A1 inactive. When ON, the circuit to the BR opens and the first stage of A1 activates. The circuit 0does not close the -48 V to shelf 65 at this time. Refer to the simplified block diagram figure.

When you press the RESET button on the converter, a momentary circuit to the BR closes and A1 activates in a timed sequence. In this sequence, the main

NT0X28AF (continued)

-48V feed to shelf 65 is closed first, and the drive to the power converter follows.

After the converter is operating, the converter output latches the RESET circuit closed to the BR. When the converter fails, the RESET circuit opens and A1 opens the -48V feed to shelf 65.

The -48V power feeds act in the same method. The F03 to shelf 32 is power control-2, PCA-1. The F02 to shelf 51 is power control-1, PCA-2. The F04 to shelf 18 is power control-2, PCA-2.

Alarm circuits

A separate -48V dedicated feed from the PDC frame powers all alarm circuits in the FSP. These separate -48V feeds from the central office battery A feed in the PDC. These feeds are distributed to the alarm circuits for frames in the DMS-100 Family. These feeds are the alarm battery supply (ABS).

The system distributes the ABS to the PCA circuits and to other alarm circuits through four fuses, F05 through F08. All eight fuses, F01 through F08, have fuse guard contacts that close when a fuse activates. Any closed guard contact applies an input to the alarm detector circuit A2. When input is not present, A2 operates alarm relay K, that holds the contact open. When an input is present at A2, K is released and the aisle alarm and frame fail contacts close. This alarm circuitry monitors all battery and ABS feeds.

Alarm contacts on both PCAs act in parallel. An alarm on a circuit operates the frame fail lamp and closes the aisle alarm circuit.

Fused test jack access to the ABS is available at the front and back of each FSP.

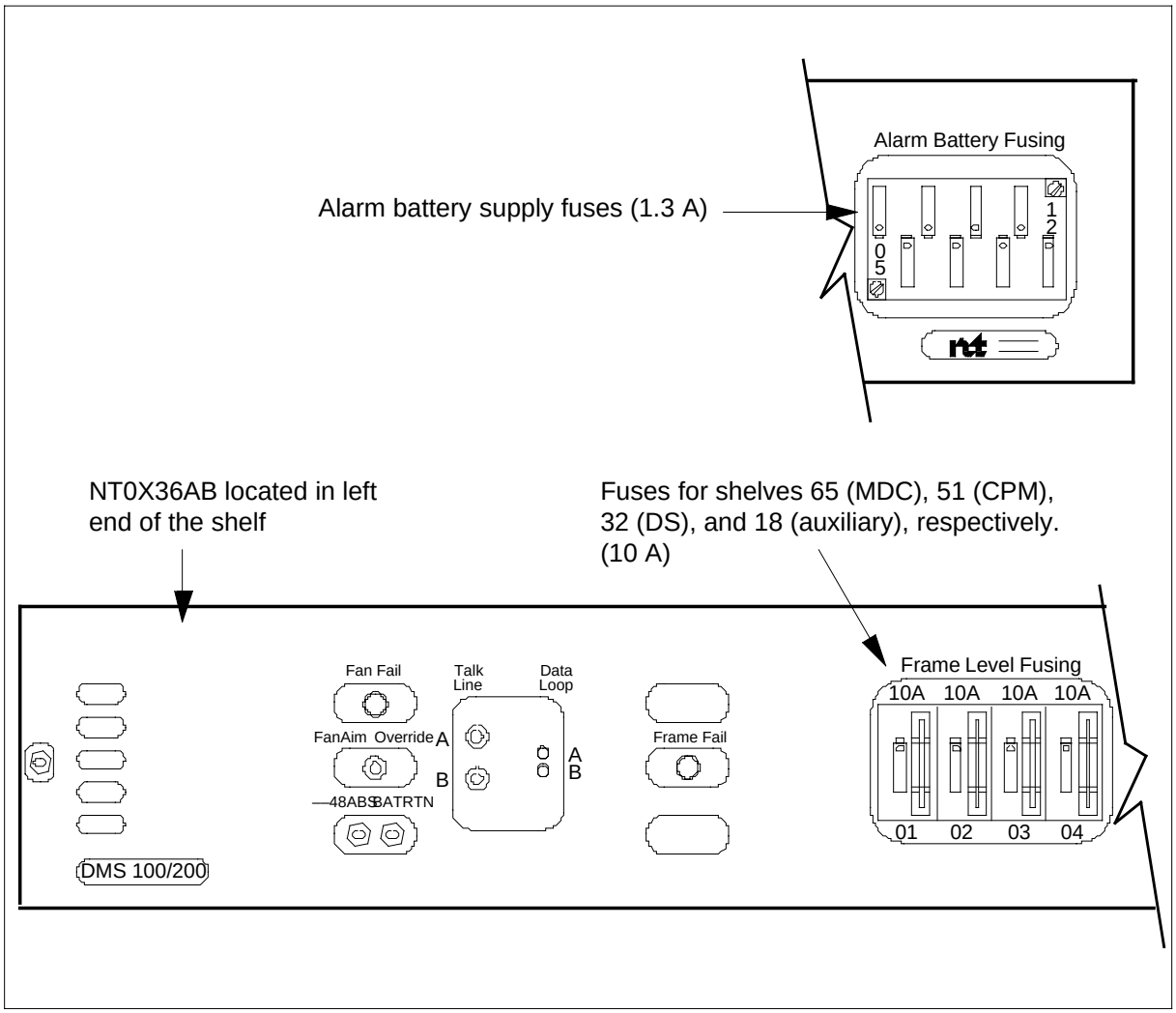
Fan switches in the cooling unit (NT3X90) monitor frame cooling. A fan that has faults causes application of the -48V ABS from F08 through the fan switch return to the alarm circuit A3. This event closes the fan fail lamp circuit to BR and F06, and causes the lamp to light. The fan fail condition provides an alarm input to A2 through the fan alarm override switch S1. This event results in an aisle alarm and a frame fail lamp indication. When you want the fan fail lamp indication only, the user switches to S1 to the fan alarm override position. This action cancels the aisle alarm and frame fail, but leaves the fan fail indication on. This action releases the alarm circuit A2 to monitor other alarm inputs. The fan fail lamp remains lit until the fan alarm input stops and switch S1 restores to the normal (no override) position.

The alarm battery fuse panel has space for a maximum of eight fuses (F05 to F12). The FSP requires only four ABS fuses (F05 to F08). Dummy fuses occupy positions 09 to 12.

Design

The following figure provides a front view of the NT0X28AF FSP shelf.

NT0X28AF front view

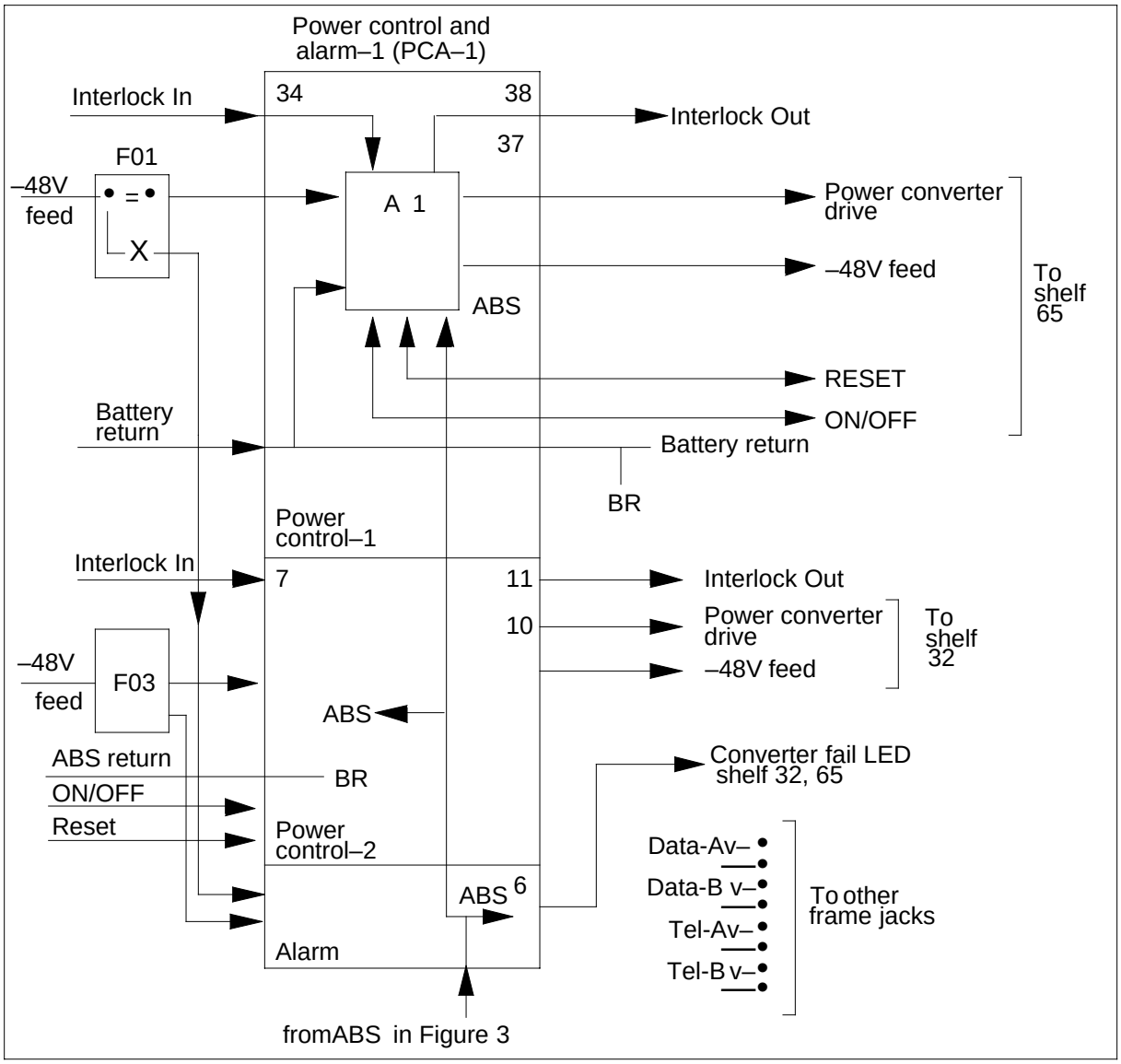


Note: This diagram is not to scale.

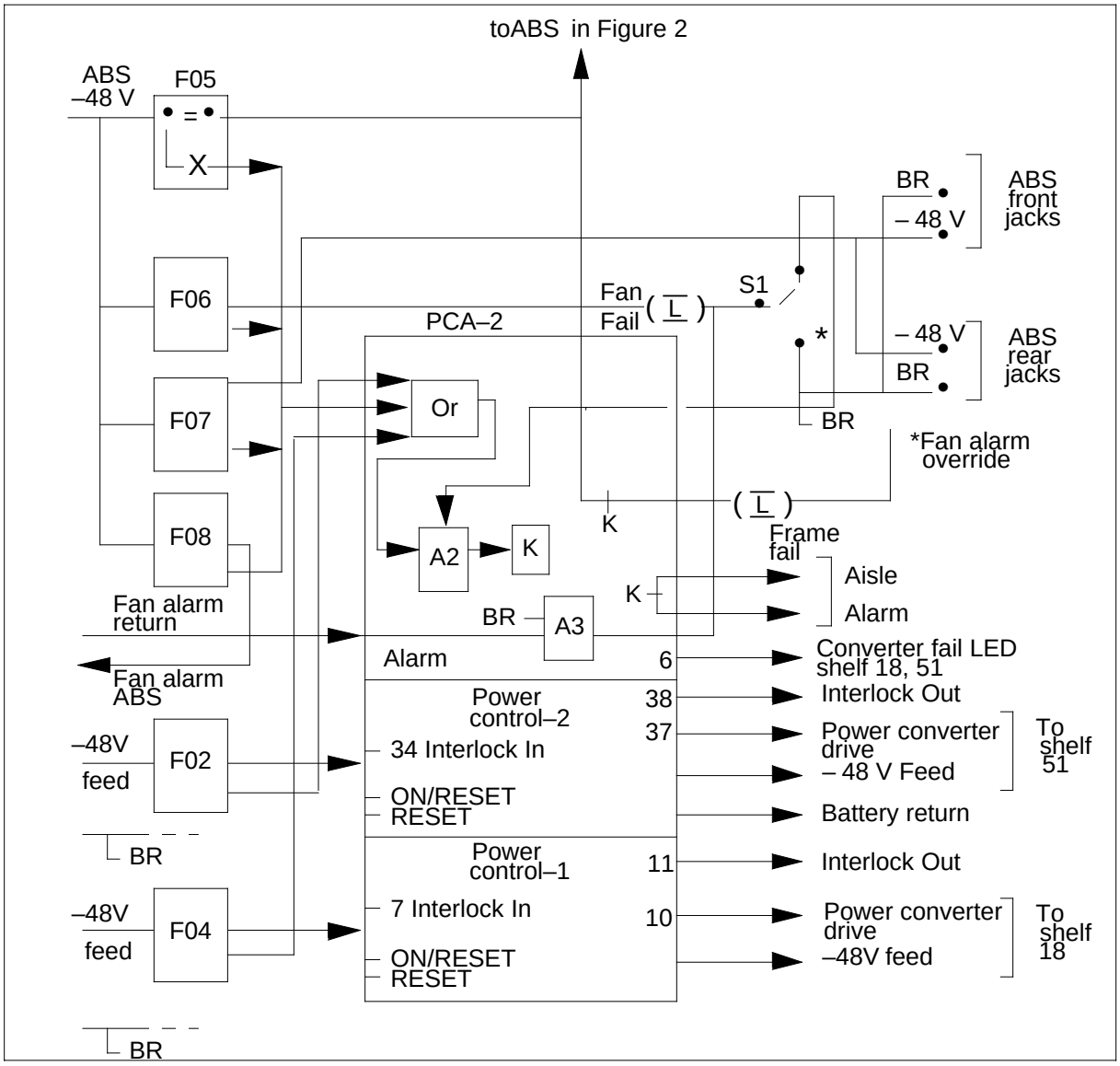
The following figures provide simplified block diagrams that indicate the signal flow into and from the FSP.

NT0X28AF (continued)

NT0X28AF Simplified block diagram



NT0X28AF simiplified block diagram



NT0X28AL

Product Description

The NT0X28AL frame supervisory panel (FSP) contains power control and alarm circuits. These items provide interfaces between the power distribution center (PDC) and the input/output equipment (IOE) frame of the DMS-100 Family digital switching system. The FSP provides a focal point for operating company personnel to monitor the switching system.

The NT0X28AL provides alarms to indicate problems in the IOE frame. The FSP provides controls, like manual overrides of an alarm. The FSP provides controls for test facilities, like the four service jacks that provide access to two telephone lines (TEL-A, TEL-B) and two data lines (DATA-A, DATA-B).

The power control and alarm circuits are on Circuit packs (CP) NT0X36AB, power control and alarm (PCA).

The NT0X28AL FSP is like the NT0X28AJ FSP. The difference is in the number of power feeds. The AL version uses three power feeds and the AJ uses two.

Parts

The NT0X28AL FSP contains two general categories of parts: NT0X36AB PCA CPs, and alarm circuits.

Power control

The NT0X28AL FSP contains two identical NT0X36AB PCA CPs, designated PCA-1 and PCA-2. Each PCA contains two power control circuits and one alarm circuit.

The three -48V feeds from the PDC frame connect to PCA-1 and PCA-2 through fuses F01 through F03. Fuse F04 is not fitted.

Power control -1 in PCA-1 is standard for all three power control circuits. The power control consists of an electronically-controlled switch A1. Switch A1 closes the -48V feed from F01 to shelf 32 of the frame. This frame contains the FSP. This action occurs when the power-up inputs ON/OFF and RESET are applied in the proper sequence. The ON/OFF and RESET inputs connect to the ON/OFF switch and RESET buttons. The ON/OFF and RESET buttons are on the faceplate of the power converters in shelf 32.

When OFF, the ON/OFF switch in the converter maintains a closed circuit to the battery return (BR). This action holds A1 inactive. When ON, the circuit to the BR opens and A1 activates but does not close the -48V to shelf 32 at this time.

When you press the RESET button on the converter, a momentary circuit to the BR closes and A1 activates in a timed sequence. In this sequence, the main -48V feed to shelf 32 is closed first, and the drive to the power converter follows.

After the converter is operative, the converter output latches the RESET circuit is latched closed to the BR. When the converter fails, the RESET circuit opens and A1 opens the -48V feed to shelf 32.

The other -48V power feeds act in the same manner: F03 to shelf 04 and F02 and to shelf 18.

Alarm circuits

All alarm circuits in the FSP are powered through a separate -48V dedicated feed from the PDC frame. These separate -48V feeds from the central office battery A feed in the PDC. These feeds are distributed to the alarm circuits for frames in the DMS-100 Family. These feeds are the alarm battery supply (ABS).

The ABS is distributed to the PCA circuits and to other alarm circuits through four fuses, F05 through F08. All seven fuses, F01-F03 and F05-F08 have fuse guard contacts that close when a fuse activates. Any closed guard contact applies an input to the alarm detector circuit A2. When input is not present, A2 operates alarm relay K, that holds the contact open. When an input is present at A2, K releases and the aisle alarm and frame fail contacts close. This alarm circuitry monitors all battery and ABS feeds.

Alarm contacts on both PCAs act in parallel. Fused test jack access to the ABS is available at the front and rear of each FSP.

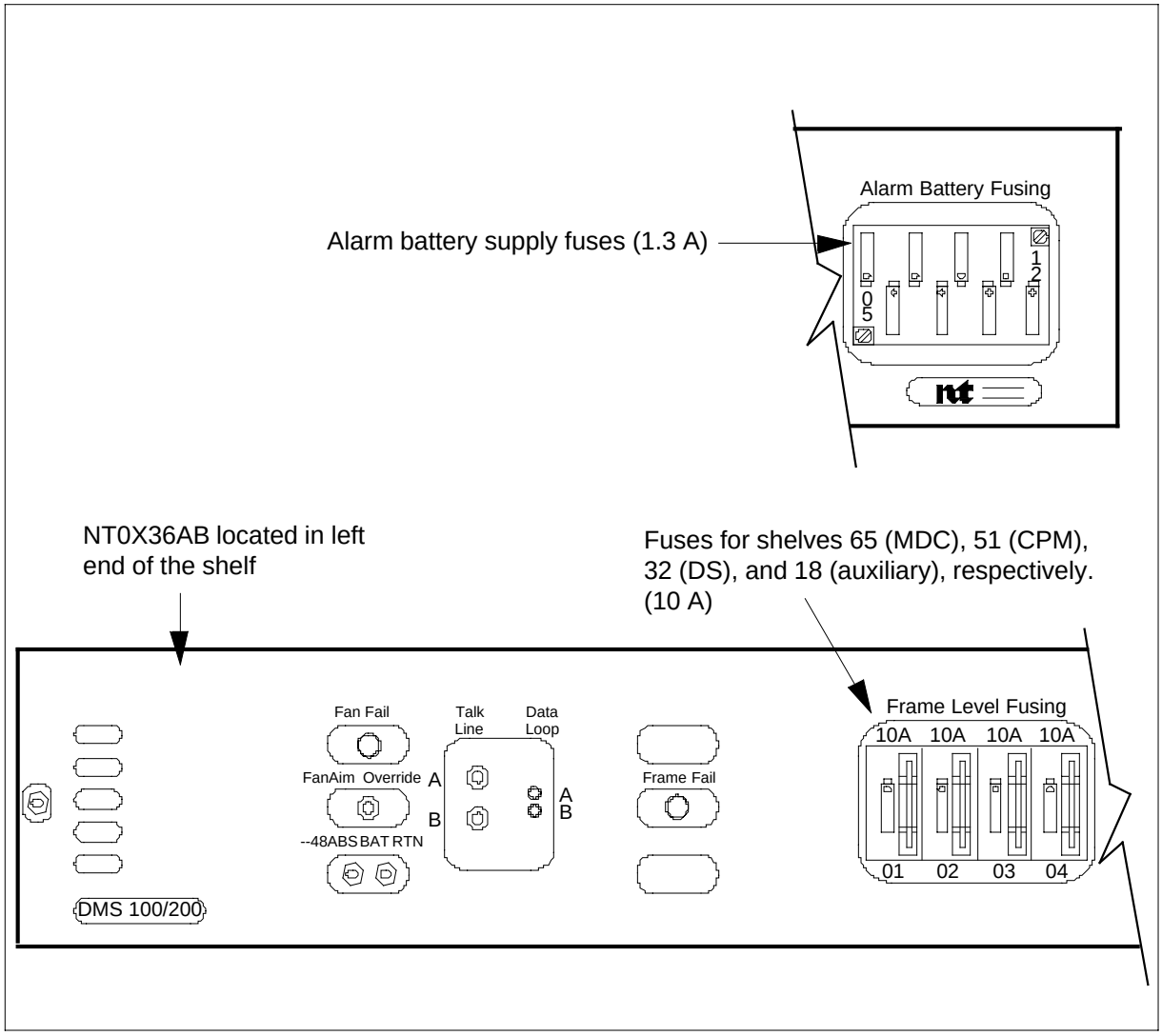
The alarm battery fuse panel has space for a maximum of eight fuses (F05 to F12). The NT0X28AL FSP requires only four ABS fuses (F05 to F08). Dummy fuses occupy positions 09 to 12 because the NT0X28AL FSP requires only four ABS fuses F05 to F08.

Design

The following figure provides a front view diagram of the NT0X28AL FSP shelf.

NT0X28AL (end)

NT0X28AL front view



Note: This diagram is not to scale.

NT0X28AM

Product description

The frame supervisory panel (FSP) contains power control and alarm circuits. These circuits provide interface between the power distribution center (PDC) and the equipment frames of the DMS-100 Group digital switching system. The following provides power control to the common peripheral control equipment (CPCE) frame:

- four circuit breakers (CB)
- one NT0X91AA converter drive and alarm
- one NT0X91AE converter drive and protection circuit pack (CP)

One FSP mounts on each single-bay equipment frame.

The FSP monitors office battery and alarm battery supply (ABS) fuses, cooling or inverter units. If a cooling or inverter unit fails, fan fail indications, frame fail indications, and aisle alarm outputs signal problems.

Converter fail lines connect to the light-emitting diode (LED) indicators on the power converters in the associated frame. A frame fail indication on the FSP front panel and an aisle alarm output monitors these lines. The indication and output monitor these lines if a converter or fuse fails. The converter fail lines operate an LED indicator on the front panel of the FSP. This indicator is below the associated power feed CB and the LED indicator in the shelf power converter.

Four service jacks on the front panel provide access to two telephone pairs and two data pairs. The telephone jacks are TEL-A and TEL-B. The data jacks are DATA-A and DATA-B. When the jacks and the FSP are used together on other frames, the service jacks provide interframe and interaisle communications. The communications occur with connectors on the FSP.

The FSP features a mechanical interlock. This feature has a cover that slides that allows access to two CBs at one time.

Parts

The FSP contains the following parts:

- NT0X91AA-Converter drive and alarm
- NT0X91AE-Converter drive and protection CP
- Front panel control and indicators
- Mechanical interlock

NT0X28AM (continued)

Converter drive and alarm

The FSP uses this CP to monitor all CBs and fuse alarms. The converter drive part of the CP controls the -48 V feeds to the two power converters. The NT0X91AE converter drive does not drive these converters. The alarm part of the NT0X91AA CP receives input from the converter fail bus. The NT0X91AA CP also receives input from the guard contacts of fuses F02 through F04. When the alarm circuit receives an input, the frame fail lamp lights up. The system makes a connection from aisle alarm 1 to aisle alarm 2. Aisle alarm 2 also provides a connection for an end-aisle alarm lamp.

Converter drive and protection circuit pack

The FSP uses this CP to provide power control and protection to the shelves of the CPCE frame. When a CB is closed, the -48V feed cannot be applied to the converter in shelf position 65. Apply this feed if the application of the correct power-up sequence occurs through the ON/OFF, RESET, and CONVERTER DRIVE leads. Several process control block connecting fingers on the NT0X91AE are shortened. This condition makes sure the CBs associated with drive circuits in the NT0X91AA do not trip. Transients that cause these trips occur when you withdraw and insert the NT0X91AE again.

Front panel control and indicators

You can operate the breakers from the front panel. The associated converter fail LED indicator is below the CB that feeds the converter. If a converter fails, a signal on the associated converter fail lead causes the LED to light up. The ABS test jacks are on the front panel and the rear panel of the FSP. Four jacks, two for data and two for telephone, are available for connection. You can connect these jacks to other frames with a connector at the rear of the FSP. After a guard contact operates, fuses F01 to F04 have a mechanical indicator that you can see from the front of the panel. Dummy fuses occupy the fuse positions that are not in use.

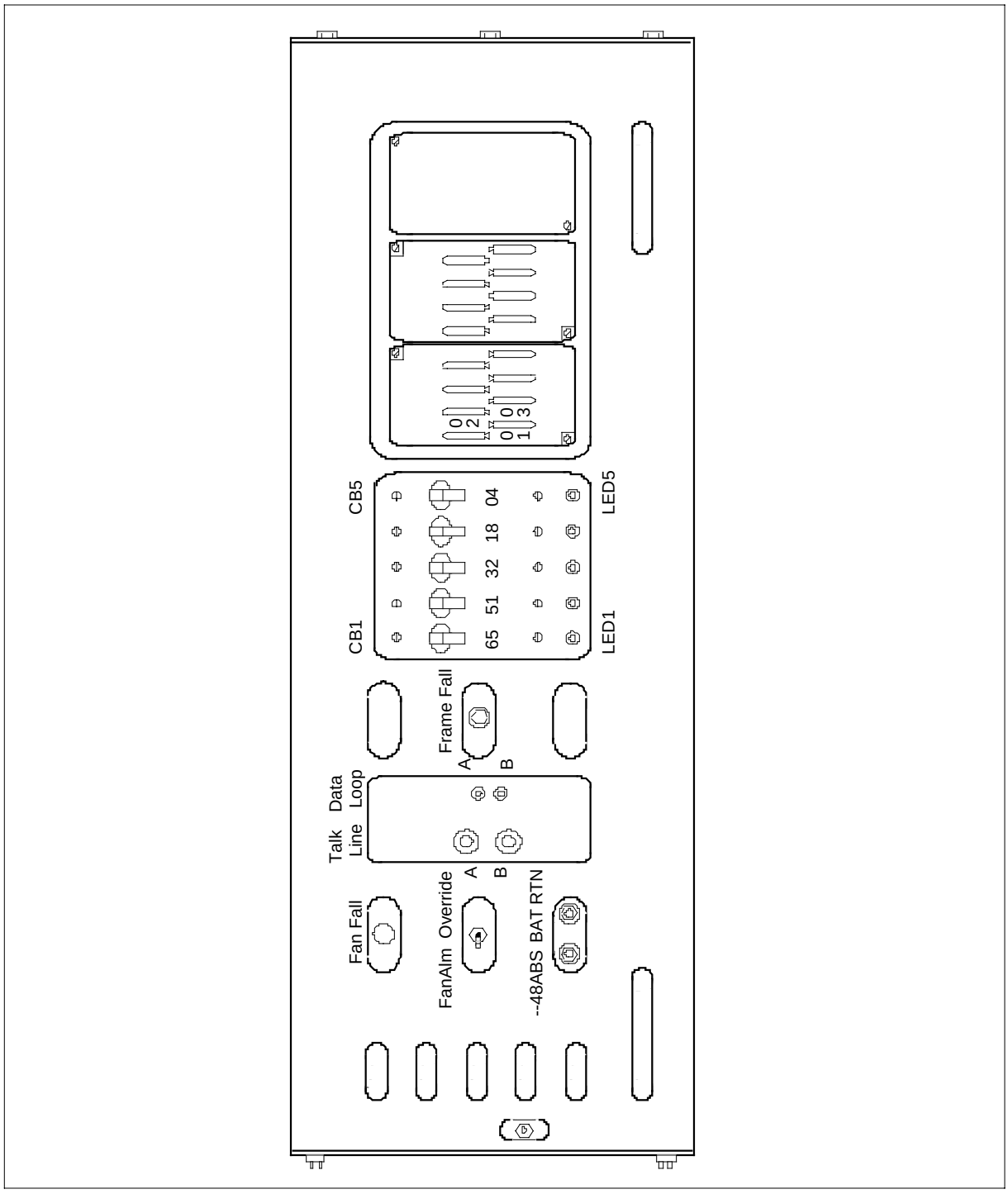
Mechanical interlock

Each frame has a mechanical interlock that surrounds each feed for power converters from the FSP. A block interlock is present for feeds to shelves 65 and 18 with feeds to shelves 51 and 04.

Design

The following figure indicates the design of the FSP.

NT0X28AM front view



Note: This diagram not drawn to scale.

NT0X28AN

Product description

The NT0X28AN frame supervisory panel (FSP) has power control and alarm circuits. These circuits provide interfaces between the power distribution center (PDC) and the MS6E frame of the DMS-100 Family digital switching system.

The NT0X28AN provides alarms that warn you of problems in the MS6E frame. The FSP provides a focal point that monitors the switching system. The FSP also provides test facilities and controls, like those for manual override of an alarm. Four service jacks on the front panel provide access to two telephone pairs and two data pairs. The telephone jacks are TEL-A and TEL-B. The data jacks are DATA-A and DATA-B.

The following parts provide power control to the MS6E equipment frame:

- four circuit breakers (CB)
- four fuses
- one NT0X91AA alarm and converter drive
- one NT0X91AE converter drive and protection circuit pack

The NT0X28AN FSP mounts at shelf position 45 in the MS6E frame.

Parts

The NT0X28AN shelf contains the following parts:

- A0205202-Fuse QFF1A
- A0205210-Dummy fuse QFF3A (provisionable)
- NT0X2844-Message switching 6 equipment FSP assembly
- NT0X91AA-Converter drive and alarm card
- NT0X91AE-Converter drive and protection circuit

Design

The following tables indicate the design of the NT0X28AN. The tables provide information on the application of the CBs and fuses.

NT0X28AN parts

PEC	Slot	Description
A0205202	F01-F04	*Fuse QFF1A* This fuse is a 1.33-A fuse that must be in fuse positions F01-F04. The A0205202 uses a white, P097P235 name disk.
A0205210	F05-F08	*Dummy fuse QFF3A* The A0205210 dummy fuse is in fuse positions F05-F08.
NT0X2844	-	*Message Switching 6 Equipment Frame Supervisory Panel Assembly* The NT0X2844 has four 10-A CBs, CB1, CB2, CB4, and CB5. These ACBs are assigned to shelves 65 and 51, as indicated in the table below.
NT0X91AA	01	*Converter drive and alarm card* The NT0X91AA provides aisle alarm output to the DMS-100 alarm system when any alarm guard contact operates.
NT0X91AE	02	*Converter drive and protection circuit* The NT0X91AE provides power control and protection circuits.

Fuse/terminal assignments (Sheet 1 of 2)

Fuse loc.	Max rating (amps)	Shelf/ABS feed	Comments
CB1	10	65	NT6X07AB 6STA shelf
CB2	10	65	NT6X07AB 6STA shelf
CB3	not filled	-	-
CB4	10	51	NT6X07AB 6STA shelf
CB5	10	51	NT6X07AB 6STA shelf

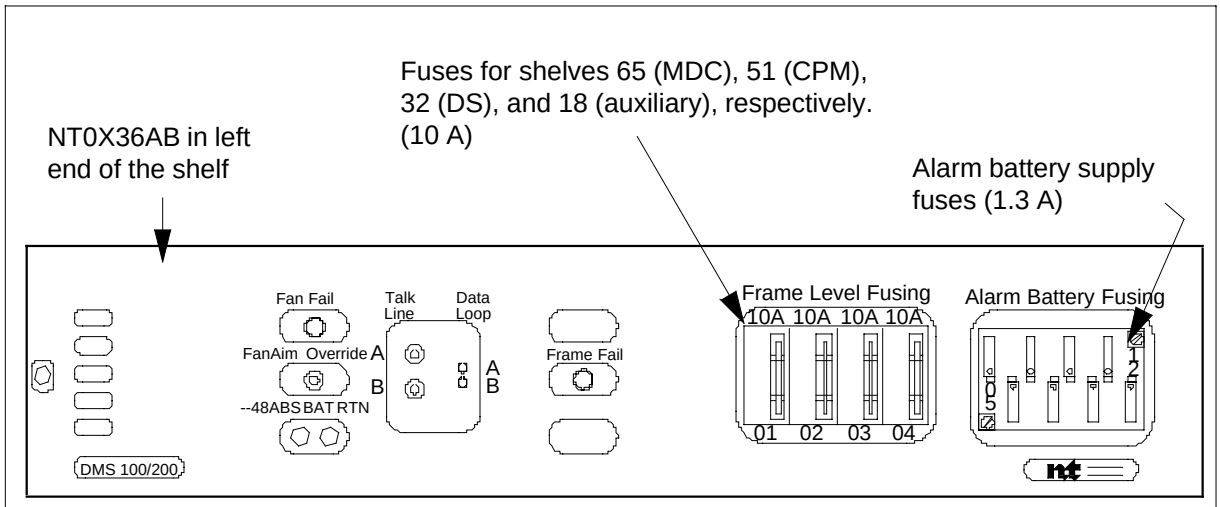
NT0X28AN (end)

Fuse/terminal assignments (Sheet 2 of 2)

Fuse loc.	Max rating (amps)	Shelf/ABS feed	Comments
F01	1.33	ABS	NT0XX91AA Converter drive and alarm card
F02	1.33	ABS	Sisle end lamp ABS
F03	1.33	ABS	ABS jacks, front and rear
F04	1.33	ABS	Fan or inverter alarm switch
F05	Dummy	-	Not used
F06	Dummy	-	Not used
F07	Dummy	-	Not used
F08	Dummy	-	Not used

The following figure indicates the front of the NT0X28AN panel.

NT0X28AN front view



Note: This illustration is not drawn to scale.

NT0X28AP

Produce description

The NT0X28AP frame supervisory panel (FSP) contains power control and alarm circuits. These circuits provide interface between the power distribution center (PDC) and the equipment frames of the DMS-100 family digital switching system. The FSP provides power control to the message switching seven equipment (MS7E) frame, or to the signaling terminal six equipment (ST6E) frame. Six circuit breakers (CB), one NT0X91AA converter drive and alarm, two NT0X91AE converter drive and protection circuit packs (CP) provide power. One FSP mounts on each single-bay equipment frame.

The FSP monitors office battery and alarm battery supply (ABS) fuses, and cooling or inverter units. If a cooling or inverter unit fails, fan fail indications, frame fail indications and aisle alarm outputs help to target problems. With the ABS fuses, fuse 1 powers the alarm circuits of the NT0X91AA converter drive and alarm CP. This fuse powers the frame fail lamp, the light-emitting diode (LED) indication near to each CB. This fuse also powers the converter fail LED indication on each associated power converter. Fuse 2 powers the frame fail lamp. Fuse 3- powers toll break-in (TB) 2/8 for end-aisle lamp power when correct. Fuse 4 powers TB2/10 for the fan switch alarm loop. Fuse 5 powers the ABS test jacks on the front and the back of the FSP.

Converter fail lines connect to the LED indicators on the power converters in the associated frame. These lines are monitored for a converter or fuse failure. A frame fail indication on the FSP front panel and an aisle alarm output monitor the line. The converter fail lines operate a LED indicator on the front panel of the FSP below the associated power feed CB. The converter fail lines operate an LED indicator in the CP power converter.

Four service jacks on the front panel provide access to two telephone jacks and two data jacks. The telephone jacks are TEL-A and TEL-B. The data jacks are DATA-A and DATA-B. When the jacks and the FSP are used together on other frames, the jacks and FSP provide interframe and interaisle communications. The communications occur through connectors on the FSP.

The FSP features a mechanical interlock. This feature contains a small sliding cover that allows access to three CBs at one time.

Parts

The FSP contains a mechanical interlock, front panel control and indicators. The FSP contains the NT0X91AA converter drive and alarm CP and the NT0X91AE converter drive and protection CP.

NT0X28AP (continued)

Mechanical interlock

Each frame has a mechanical interlock that surrounds all feeds for power converters from the FSP. With the MS7E frame application, the system provides a block interlock. This interlock is for the feed to CP 51 (slot 01). This interlock is also for both feeds to shelf 18 with the feed to shelf 51 (slot 25). This interlock is also for both feeds to shelf 32. With the ST6E frame application, the system provides a block interlock. This interlock is for the feeds to slot 1 of CPs 51, 32, and 18. The feeds go to slot 25 of the same CPs.

Front panel control and indicators

You can operate the breakers from the front panel. The associated converter fail LED indicator is below the CB that feeds the converter. If a converter fails, a signal on the associated converter fail lead causes the LED to light up. The ABS test jacks are on the front panel and the back panel of the FSP. Four jacks, two for data and two for telephone, can connect to other frames. You can connect these jacks on the back of the FSP. Fuses 1 to 4 have a mechanical indicator. You see this indicator from the front of the panel when a guard contact occurs. Dummy fuses occupy positions that are not in use.

Converter drive and alarm

The FSP uses this CP to monitor all CBs and fuse alarms. The converter drive part of the CP controls the -48V feeds to the two power converters. The NT0X91AE converter drive does not drive these converters. The alarm part of the NT0X91AA converter drive receives inputs from the converter fail bus. The alarm receives input from the guard contacts of fuses 2 to 4. When the alarm circuit receives an input, the frame fail lamp lights. The system connects aisle alarm 1 to aisle alarm 2. Alarm 2 provides a connection for an end-aisle alarm lamp.

Converter drive and protection converter drive

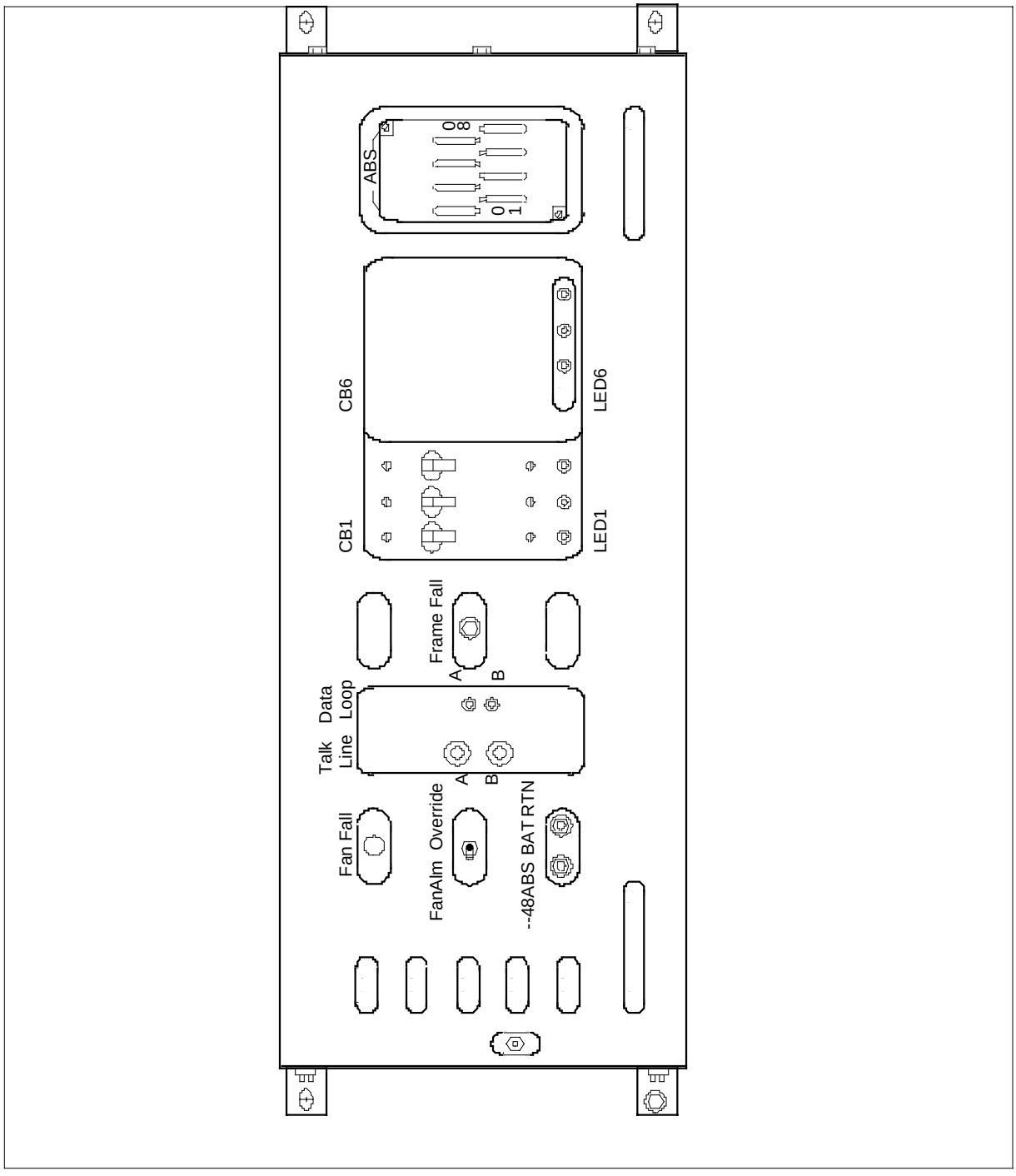
The FSP uses this converter drive to provide power control and protection to the shelf of the frame. When a CB is closed, you cannot apply the -48V feed to the converter in CP position 65. This action cannot occur unless you apply the correct power-up sequence through the ON/OFF, RESET, and CONVERTER DRIVE leads. Several printed circuit board connecting fingers on the NT0X91AE are shortened. The shortened fingers make sure the CBs associated with drive circuits in the NT0X91AA do not trip. Transients cause the trip when the NT0X91AE withdraws and inserts again.

Design

The following figure indicates the design of the FSP.

NT0X28AP (end)

NT0X28AP parts



NT0X28AS

Product description

The NT0X28AS frame supervisory panel (FSP) is the subset of the remote control equipment (RCE) frame. The RCE frame is the subset of the Remote Switching Center that has the remote control cluster module (NT6X12CA). The frame can have a maximum of two remote maintenance module shelves (NT6X13AB).

This FSP includes a talk battery filter, frame fail lamp, means to power the end aisle lamp, and alarm battery supply (ABS). This FSP includes distribution fuses, additional jacks and four jacks. These four jacks divide in two pairs of jacks. The data jacks are DATA-A and DATA-B. The telephone jacks are TEL-A and TEL-B. These jacks provide front and rear access to the -48V dc alarm battery supply. Fuses that are not fuses F05-F08 are ABS distribution fuses. This FSP responds when a fuse operates or other alarm condition occurs. The FSP closes the aisle alarm loop. The FSP lights the frame fail lamp to respond. The aisle alarm loop closes if alarm battery supply does not reach the FSP.

The NT0X28AS includes a circuit breaker and a light-emitting diode (LED) for each power converter controlled. If the power converter does not operate, this LED and the LED on the power converter glow. The FSP includes a mechanical interlock feature with a cover that slides to prevent the accidental manual trip of circuit breakers. The cover does not interfere with automatic breaker trip, does not slide automatically, and can slide manually.

Parts

The NT0X28AS FSP contains the following parts:

- NT0X91AA-alarm and converter drive circuit pack (CP)
- NT0X91AE-alarm drive and protective circuit network

Alarm and converter drive circuit pack

The NT0X28AS uses the NT0X91AA to monitor all circuit breakers and fuse alarms. The converter drive part of the circuit pack controls the -48V dc feeds to the two power converters. The NT0X91AE does not drive these converters. The alarm part of the NT0X91AA circuit pack receives inputs from the converter fail bus. The pack also receives inputs from the guard contacts of fuses F02-F04. When the alarm circuit receives an input, the frame fail lamp lights. The system makes a connection from aisle alarm 1 to aisle alarm 2. Aisle alarm 2 also provides a connection for an end aisle alarm lamp.

Alarm drive and protective circuit network

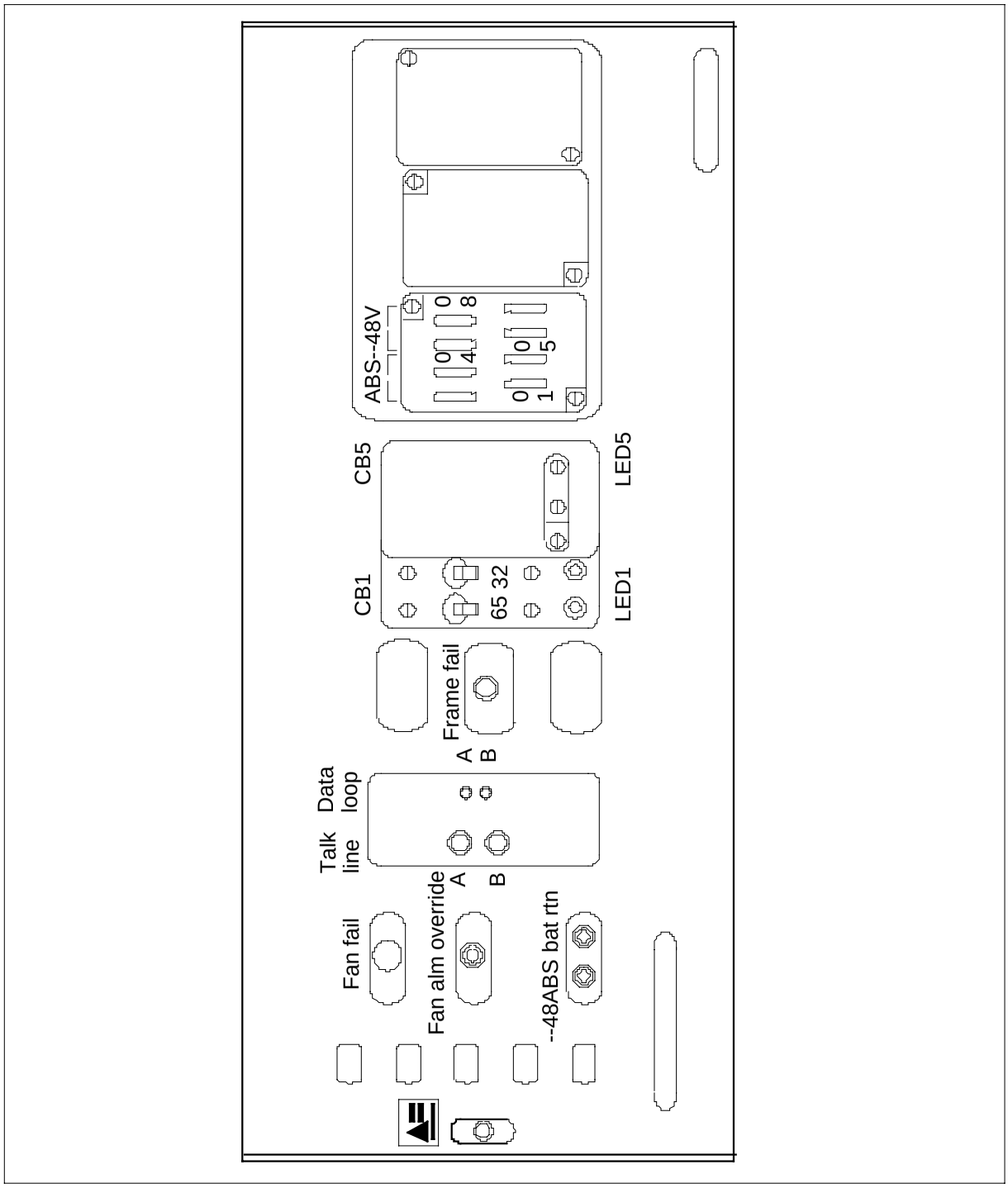
The uses the NT0X91AE to provide power control and protection to the shelves of the remote control equipment frame. When a circuit breaker is closed, you cannot apply the -48V dc feed to the power converter in shelf position 65. Apply the feed if you apply the correct power-up sequence through the ON/OFF, RESET, and CONVERTER DRIVE leads. Several printed circuit board connecting fingers on the NT0X91AE are shortened. These fingers make sure the circuit breakers associated with the drive circuits in the NT0X91AA do not trip. Transients or other power surges cause a trip when you withdraw and insert the NT0X91AE again.

Design

The following figure indicates the design of the NT0X28AS frame supervisory panel.

NT0X28AS (end)

NT0X28AS parts



NT0X28EB

Product description

The NT0X28EB frame supervisory panel (FSP) is on the ISDN common peripheral equipment (CPEI) frame. This FSP includes a frame fail lamp and a means to power the end aisle lamp. The FSP includes alarm battery supply distribution fuses, and the four jacks. The data jacks are DATA-A and DATA-B. The telephone jacks are TEL-A and TEL-B. The FSP also includes additional jacks that provide front and rear access to the alarm battery supply. The NT0X28EB responds a fuse that operates or other alarm condition. The NT0X28EB closes the aisle alarm loop and lights the frame fail lamp to respond. The aisle alarm loop closes if alarm battery supply does not reach the FSP.

The NT0X28EB includes circuits for a parallel, redundant dc supply of -48V. The supply is to the 20 NTBX02AA data channel handlers in the frame. These circuits improves product reliability.

The NT0X28EB includes a circuit breaker and an LED for each converter controlled. If the converter does not operate, this LED and the LED on the converter glow. This FSP includes a mechanical interlock feature with a cover that slides to prevent the accidental, manual trip of circuit breakers. The cover does not interfere with automatic breaker trip, does not slide automatically, and can slide manually.

Parts

The NT0X28EB FSP contains the following parts:

- NT0X91AA-alarm and converter drive circuit pack (CP)
- NT0X91AE-alarm drive and protective circuit network

Alarm and converter drive circuit pack

The NT0X28EB uses the NT0X91AA to monitor all circuit breakers and fuse alarms. The converter drive part of the circuit pack controls the -48V dc feeds to the two power converters. The NT0X91AE does not drive these converters. The alarm part of the NT0X91AA circuit pack receives inputs from the converter fail bus. This alarm part receives inputs from the guard contacts of fuses F02-F04. When the alarm circuit receives an input, the frame fail lamp lights. The system connects aisle alarm 1 to aisle alarm 2. Aisle alarm 2 provides a connection for an end aisle alarm lamp.

Alarm drive and protective circuit network

The NT0X28EB uses the NT0X91AE to provide power control and protection to the shelves of the CPEI frame. When a circuit breaker is closed, the system cannot apply the -48V dc feed to the converter in shelf position 65. Apply this

NT0X28EB (continued)

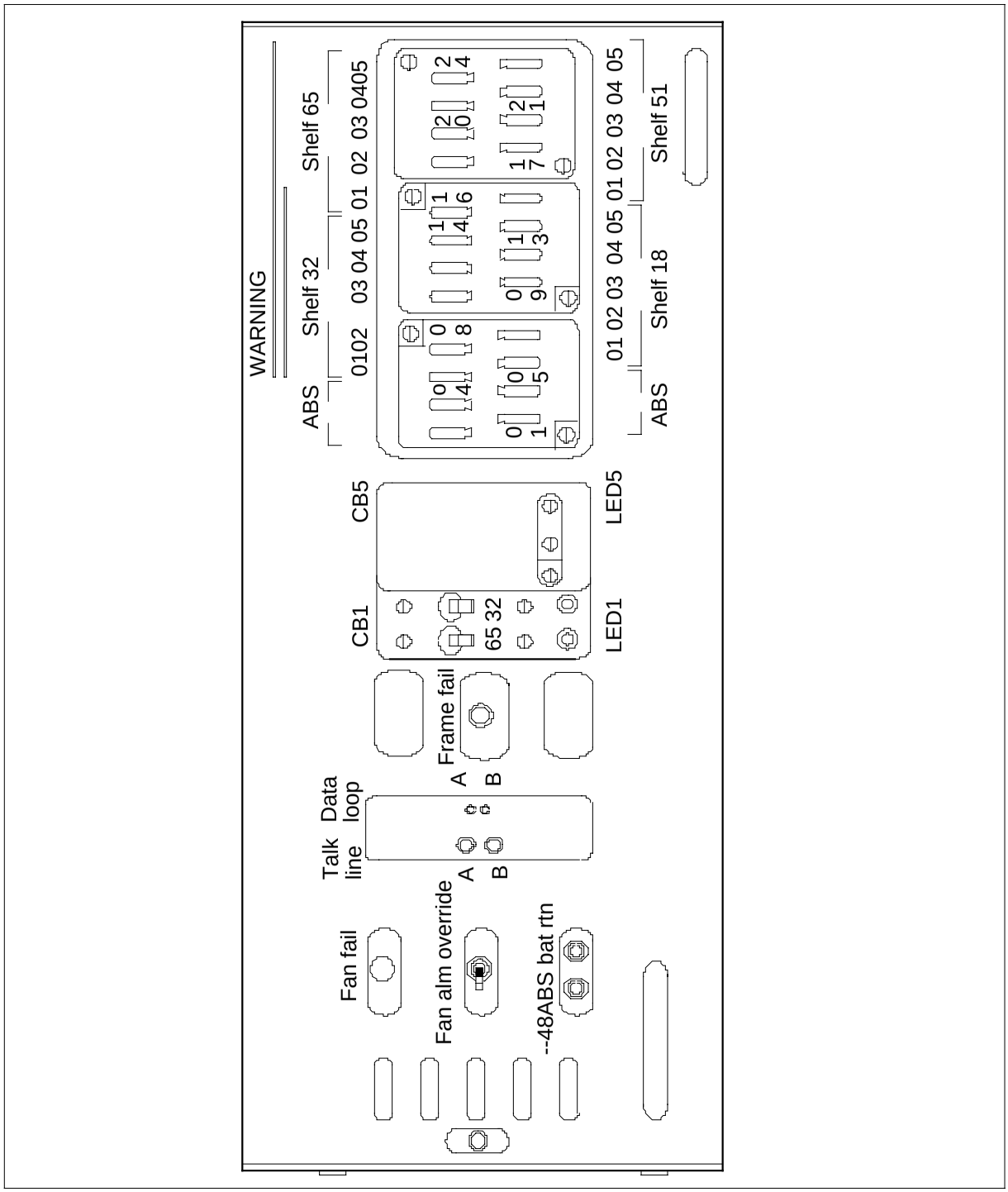
feed when you apply the correct power-up sequence through the ON/OFF, RESET, and CONVERTER DRIVE leads. Several printed circuit board connecting fingers on the NT0X91AE are shortened. These fingers make sure circuit breakers associated with the drive circuits in the NT0X91AA do not trip. Transients or other power surges cause the trip when you withdraw or insert the NT0X91AE again.

Design

The following figure is a front view of the NT0X28EB frame supervisory panel. Circuit cards in the FSP do not appear in this figure.

NT0X28EB (end)

NT0X28EB parts



NT0X35CC

Product description

The cabling cabinet (NT0X35CC) offers additional cabling space for ABAM cabling in an HSI and ENET application. Heavy input/output is required in HSI and ENET applications.

The NT0X35CC cabling cabinets provide the customer with the flexibility to pre-cable an office with DS-1 and DS512 cables. Cable entry can be in an overhead or raised floor configuration.

When the application requires a cabling unit, either side of an ENET or HSI product provides a cabling cabinet. This arrangement appears in the figure on page 3.

Front and back door complement the streamline product image. You can remove each door panel. The company can ship the cabinet to the site with the door panels installed.

A provisionable horizontal cable duct contains power cables. The horizontal cable duct makes sure electromagnetic compatibility in a lineup is present. The cable duct makes sure compatibility when the NT9X95AA cabinet interfaces with other cabinets in a central office environment is present.

When you use the NT9X95AA cabinets, with the NT0X35CC cabinet, the unit supports ENET and HSI products. The number of cabling cabinets you require depends on the application.

Parts

The cabling cabinet contains the following parts:

- NT0X3510-one welded cabling structure
  - — P0732809-one right side member
  - — P0732810-one left side member
  - — NT0X3527-base plate assembly
    - – P0734265-one base plate
  - — P0732808-one top plate
  - — P0732694-one panel support
  - — P0732812-one central truss brace
  - — P0732811-two diagonal truss braces
- NT0X3528-base panel support assembly
  - — P0733864-base panel support
- P0732740-anchor channel front
- P0733138-anchor channel rear
  - — P0732739-five ty-wrap brackets
- NT0X3526-(provisionable) *door panel assembly, maple brown (quantity two)*
  - — NT0X3525-welded door panel assembly, maple brown (quantity two)
- NT0X3522-(provisionable)*door panel assembly, gray (quantity two)*
  - — NT0X3521-welded door panel assembly, gray (quantity two)
    - – P0732698-cosmetic door panel (quantity two)
    - – P0732699-lower panel support (quantity two)
    - – P0732700-upper panel support (quantity two)
    - – P0732701-central panel support (quantity two)
- NT0X3523-(provisionable) *horizontal cable duct assembly*
  - — NT0X3524-bottom member assembly
    - – P0732693-*L* member
  - — NT0X3517-top member assembly
    - – P0732693-*L* member
  - — P0731046-duct end support (quantity two)

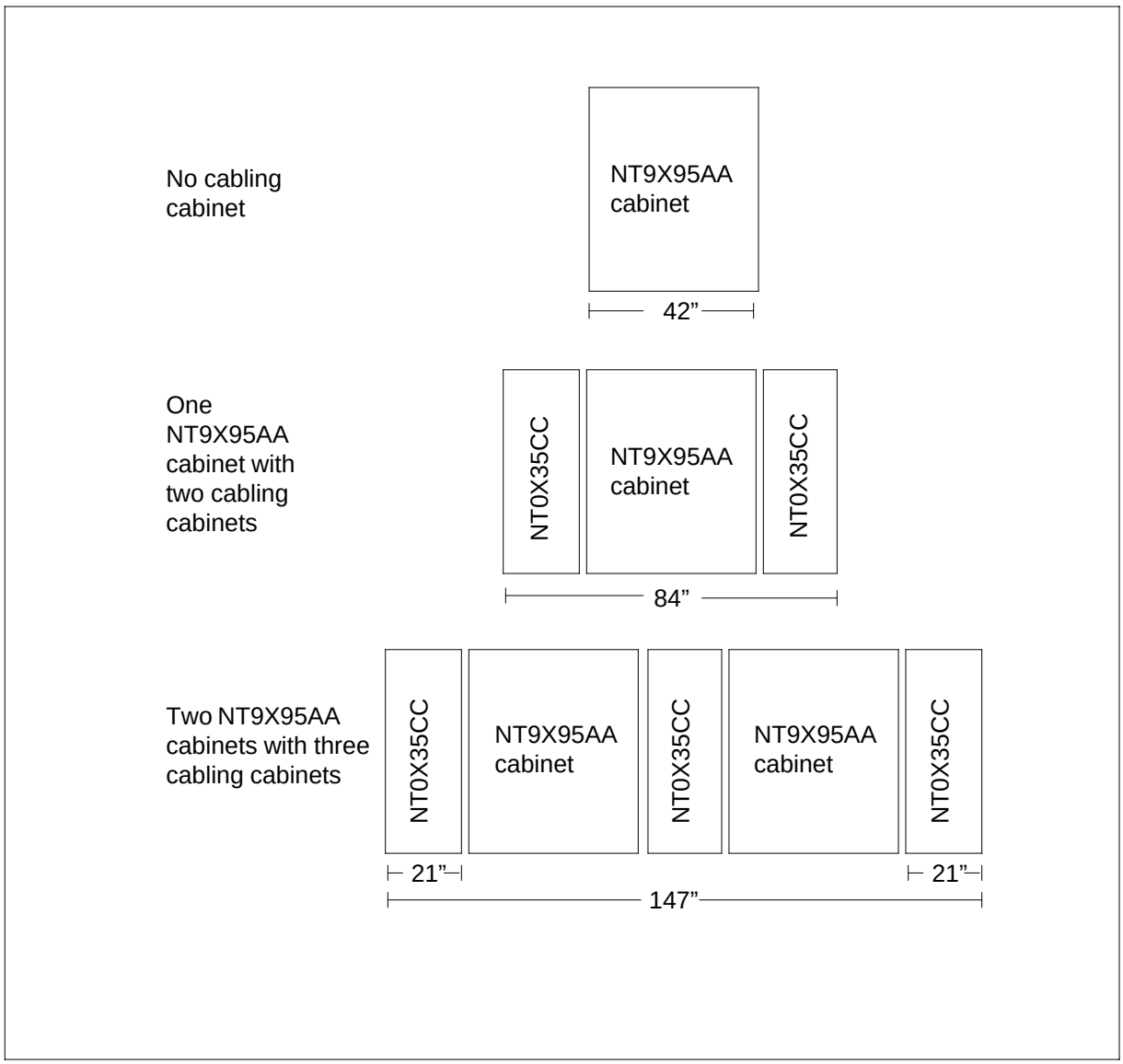
NT0X35CC (end)

- NT0X35BD-(provisionable) cable trough assembly, maple brown (quantity one) (non-precable)
- NT0X35BK-(provisionable) cable trough assembly, gray (quantity one) (non-precable)

Design

The design of the NT0X35CC cabling cabinet in relation to the NT9X95AA cabinet appears in the following figure.

Cabling cabinet provisioning



NT0X40

Product description

This type of frame supervisory panel (FSP) detects alarm inputs from the power distribution center (PDC) and generates alarm outputs to the office alarm unit (OAU). The FSP also monitors and distributes the alarm battery supply.

The features of the NT0X40 include the following:

- accepts fuse guard contact alarm inputs from a maximum of ten fuse panels
- monitors three alarm battery supplier (ABS) fuse guard inputs
- provides a frame fail indicator lamp on the front panel
- provides three two-wire alarm outputs (ABS, PDC, and aisle) to the OAU
- provides aisle alarm multiple connections to succeeding frames
- accommodates interframe communication cables with cable connectors for two data and two telephone pairs, multiplied to OAU and succeeding frames
- distributes ABS and battery return to a maximum of three frame line-ups

Location

The FSP is in the PDC in shelf position 45.

Functional description

The FSP contains two fuse alarm circuits. Each circuit contains relays K1, K2, and associated circuits on a plug-in circuit board. Each circuit contains fuses F-01, F-02, and F-03. The F-01 fuse protects the ABS -48V battery feed. The F-02 fuse protects relay K1 on board A. The F-03 fuse protects alarm input from fuse alarm board B.

Functional blocks

On fuse alarm board A, relay K2 monitors the following:

- fuse guard alarm contact input from fuse panel 62, 54, 41, 33, and 25

  Note: If any one of the fuses on these panels blows, the system applies a -48V (A) to the associated alarm input.

- the normally-open (NO) fuse guard contacts of fuses F-02 and F-03
- the fuse of the filter unit A supply
- the alarm input from fuse alarm board B

NT0X40 (continued)

On fuse alarm board B, relay K2 monitors the following:

- fuse guard alarm contact input from fuse panels 58, 50, 37, 29, and 21

  Note: If any one of the fuses on these panels blows, the system applies -48V (A) to the associated alarm input.

- the fuse of filter unit B supply

Operation of K2 on board B operates K2 on board A through the alarm input mentioned above.

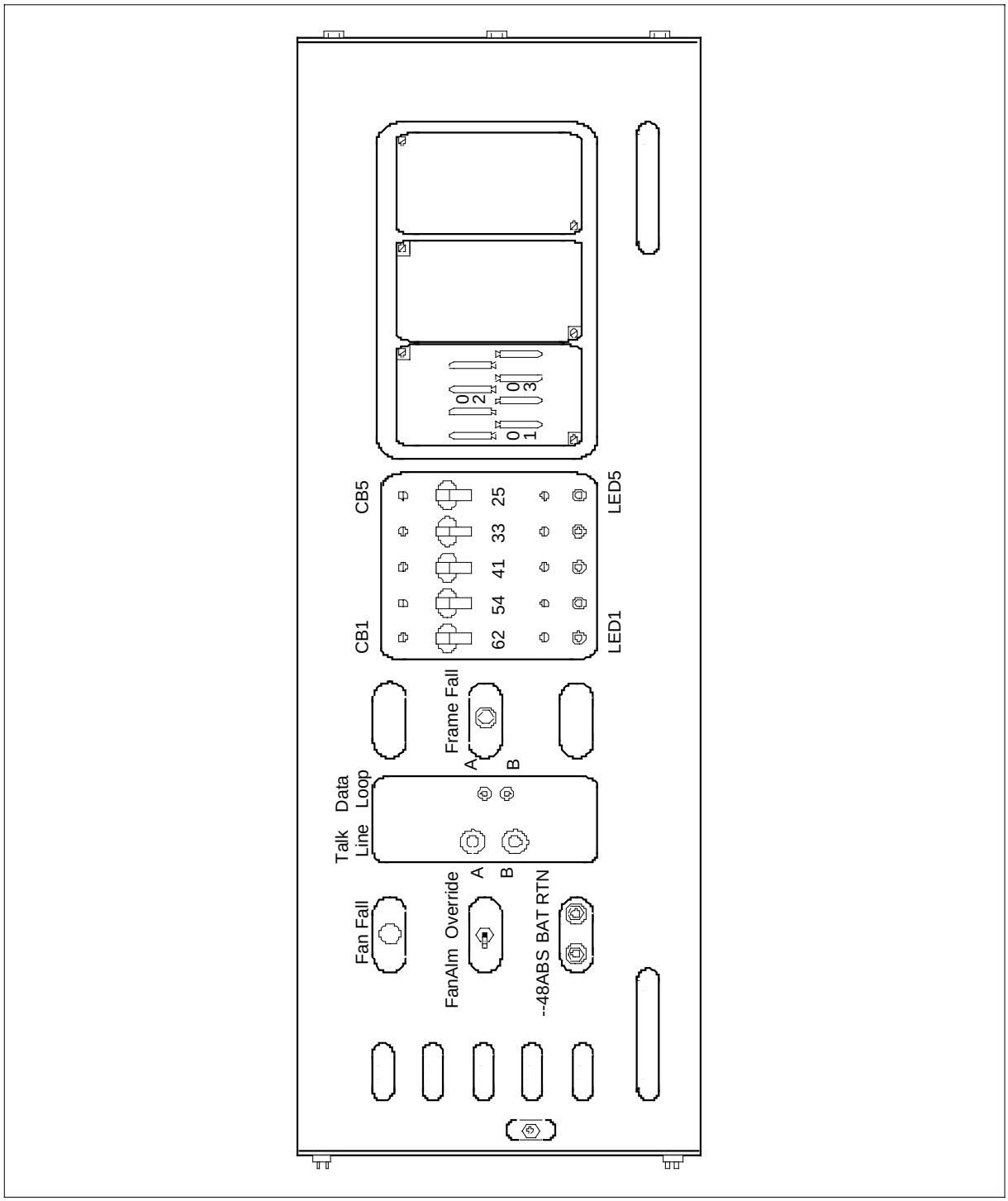
Relay K1 on board A monitors fuses F-01 and F-02 on the FSP. Relay K1 holds as long as both fuses are not broken.

The inputs produce different groups of ABS, PDC, and aisle alarm inputs to the OAU. The inputs also produce frame fail lamp indications on the FSP panel, depending on the alarm condition at the input. The Technical Data section provides these conditions and lamp indications.

Design

The FSP front view design appears in the following figure.

NT0X40 FSP front view



NT0X40 (continued)

Technical data

This section provides technical specifications for the FSP. The specifications include power requirements, environmental conditions, equipment dimensions, and alarm input condition specifications.

Power requirements

The FSP power requirements appear in the following table.

Power requirements

Battery voltage	-42.7 V to -55.8 V (dc)
Fusing (F-02, F-03)	1-1/3 A
ABS Feed Current (F-01)	10 A maximum

Environmental conditions

The following table indicates that the FSP performs under environmental conditions.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 °C to 30 °C (50 °F to 86 °F)	5 °C to 49 °C (41 °F to 120.2 °F)
Relative humidity	20% to 55%	20% to 80%

Note: A relative humidity of 80% is expected at an ambient temperature of 21 °C (69.8 °F) maximum. At an ambient temperature of 49 °C (120.2 °F), the relative humidity is expected to be 30% maximum.

Equipment dimensions

The FSP dimensions are 127 mm (5 in) in height, 610 mm (24 in) in width, and 280 mm (11 in) in depth.

Alarm input condition specifications

The following table specifies alarm input conditions as opposed to the output to the OAU.

Alarm imput specifications

	Alarm outputs							
	Alarm relay state			**Aisle**	**PDC**	**ABS**		**Frame**
Input alarm condition	**K1A**	**K2A**	**K2B**	**K1A**	**K2A**	**K2A**	**K1A**	**fail lamp**
Normal (no alarm)	E	N	N	O	O	O	O	OFF
PDC fuse guard alarm								
A supply fuse	E	E	N	O	C	C	O	ON
B supply fuse	E	E	E	O	C	C	O	ON
ABS fuse (F01)								
(No ABS from PDC)	N	N	N	C	C	C	C	OFF
F02 fail								
(No ABS to fuse alarm PCB A)	N	E	N	C	C	C	C	ON
F03 fail								
(No battery for alarm I/P from fuse alarm PCB B)	E	E	N	O	C	C	O	ON

Note: Legend: E = alarm relay operated N = alarm relay non-operated O = alarm output contacts open C = alarm output contacts closed

NT0X42AA

Product description

The NT0X42AA power distribution center frame (PDC) provides an interface. This interface is between the -48V (nominal) office batteries and each load in an office of the DMS-100 Family of products.

The NT0X42AA PDC frame contains a maximum of ten fuse panels and a frame supervisory panel (FSP). A standard DMS frame contains the PDC frame. The frame power distribution is 200W.

The level of the holes in the vertical supports of the frames identify the panel/shelf positions. Position 1 is the first hole at the bottom. See the figure titled "NT0X42AA parts" in this section.

Parts

The NT0X42AA contains the following parts:

- NT0X40AB-FSP
- Fuse distribution panel:
  - — NT0X42AB-A-feed
  - — NT0X42AC-B-feed
- NT0X42AD-Filler panel
- Ground panel:
  - — NT0X42AE-Top feed
  - — NT0X42AF-Bottom feed
- NT0X42AG-Filter panel
- NT0X42AH-Filler panel

Frame supervisory panel

The NT0X40AB FSP detects alarm inputs from the fuse shelves and generates alarm outputs to the office alarm unit (OAU).

The feed for the FSP originates at busbar A. The feed provides an alarm battery supply (ABS) for the alarm circuits and lamps of the other DMS frames.

Fuse distribution panels

The fuse distribution panels also connect to A-feed and B-feed. Panels in positions 62, 54, 41, 33, and 25 are on A-feed. Refer to the figure. The panels in positions 58, 50, 37, 29, and 21 are on B-feed. Feeds are distributed through busbars in the frame.

Each fuse panel has 15 fuse blocks, to which the company can assign different values of fuses. For identification purposes, the 15 separate fuses have numbers from 00 to 14. The position number of the panel appears before the fuse number. For example, 62F00 identifies the first fuse on the panel in position 62.

If any fuse on the panel blows, the fuse alarm (FA) lamp on that panel lights. If a fuse blows, the system sends a signal is to the FSP (position 45) to trigger other alarm circuits. The FA is on the left side of the panel.

Filler panels

The NT0X42AD filler panels cover shelves that are not in use. These shelves are at positions 21, 25, 29, 33, 37, and 41 in the PDC.

The NT0X42AH filler panel conceals a compartment that stores spare fuses. This compartment is at shelf position 05 in the PDC.

Ground panel

The ground panel contains the common battery return busbar. Two return cables connect to battery cables. The cables, at the sides of the frame, connect to a common return ground plate in the ground panel. This plate provides return connections for fused feeds.

Filter panel

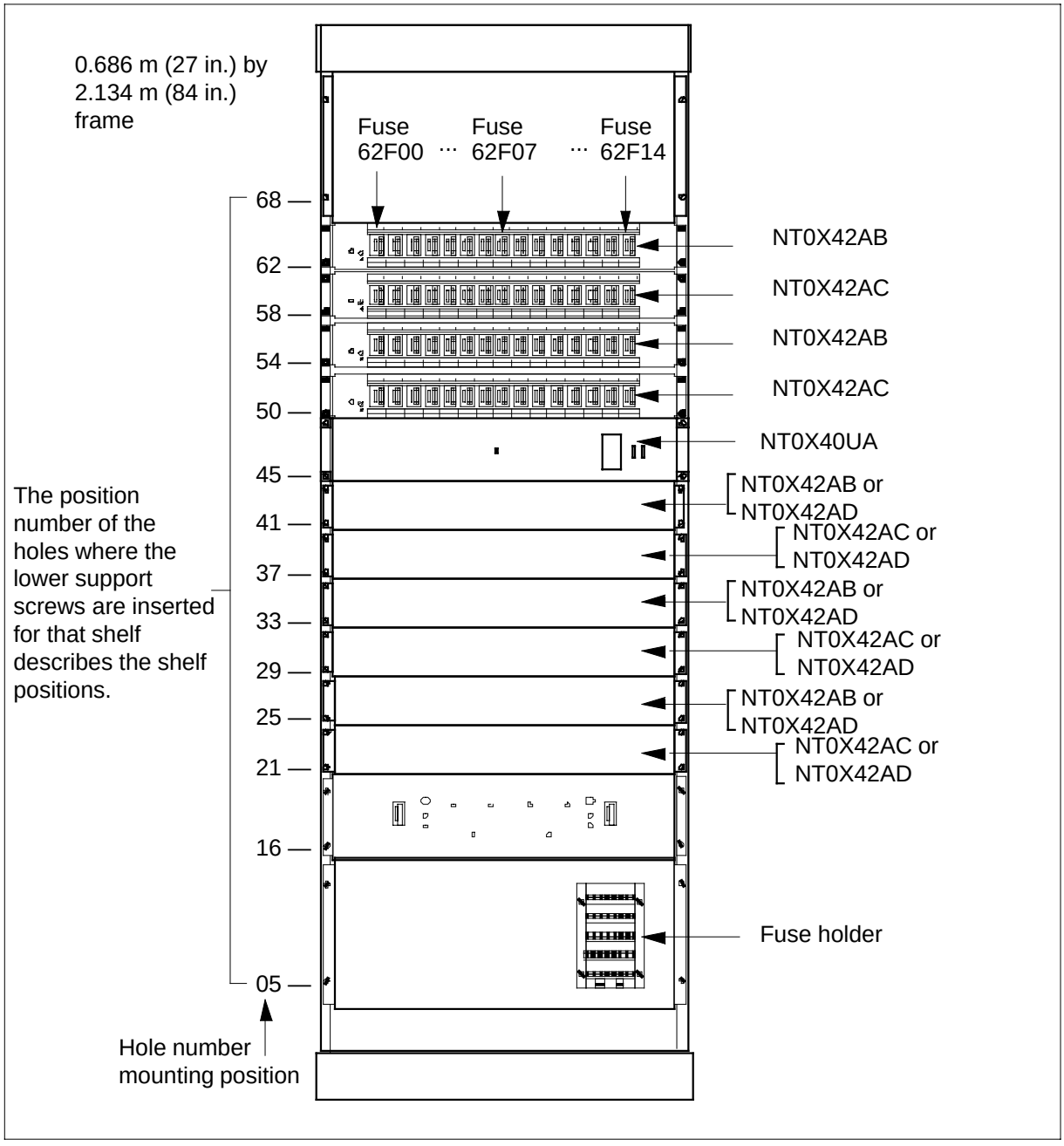
The NT0X42AG filter panel contains two noise and transient suppression capacitors. Each capacitor has a fuse, alarm lamp, and associated circuit.

Design

The design of the NT0X42AA appears in the following figure.

NT0X42AA (end)

NT0X42AA parts



Note: This diagram not drawn to scale.

NT0X42AB

Product description

The NT0X42AA power distribution center (PDC) frame uses the NT0X42AB A-feed fuse distribution panels, also known as fuse panels. The NT0X42AC B-feed fuse panels use the NT0X42AB A-feed fuse distribution panels in an alternating pattern. The NT0X42AB and AC fuse panels are installed in pairs. A minimum of two pairs and a maximum of five pairs are installed.

Count the holes in the vertical supports of the frames from the bottom to identify the positions of the panel/shelf. To determine the position of a shelf, locate the lowest hole in the frame corresponding to that shelf.

In the minimum configuration, NT0X42AB A-feed fuse panels are mounted in shelf positions 62 and 54 and the B-feed fuse panels are mounted at positions 58 and 50.

A standard, fully-equipped PDC frame consists of 10-fuse panels for dc feeds to DMS shelves and frames. Panels in positions 62, 54, 41, 33, and 25 are on A-feed. Panels in positions 58, 50, 37, 29, and 21 are on B-feed. Feeds are distributed through busbars in the PDC frame.

Parts

The NT0X42AB fuse distribution panel A-feed contains 15 fuse blocks.

Fuse blocks

A fuse distribution panel contains 15 fuse blocks. For identification purposes, the 15 fuses are allocated numbers from 00 to 14. The position number of the panel followed by the letter F, precedes the fuse number. For example, the first fuse on the left on the top panel in the NT0X42AA PDC frame can be 62F00. This design appears in the figure titled "NT0X42AB design”.

If any fuse on the panel blows, the fuse alarm (FA) lamp on that panel lights. The system sends a signal to the frame supervisory panel (FSP) (position 45 in the PDC frame) to trigger other alarm circuits.

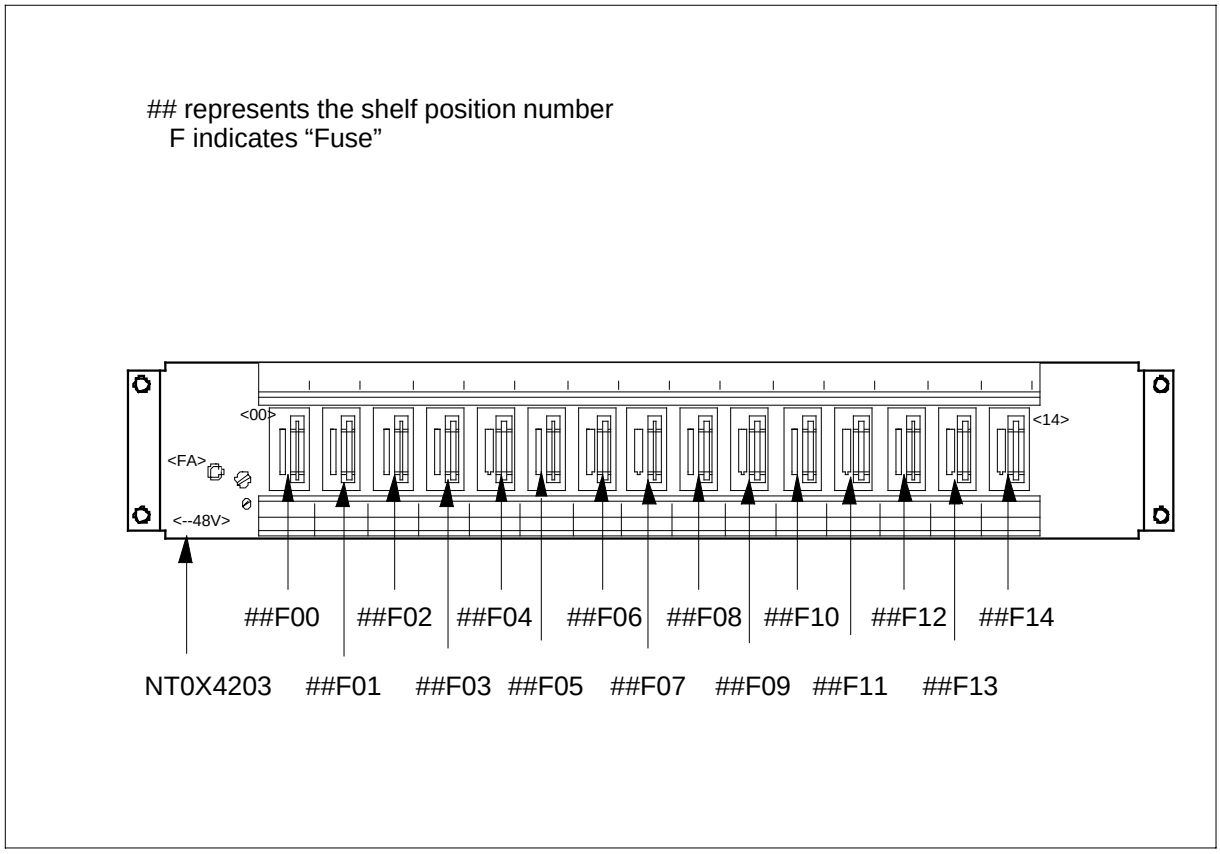
The maximum rate for any fuse block, for PDC battery feeds rated at 20 C, is 600 A. The maximum rate also can be 1.5 times the maximum correct continuous feeder current demand.

Design

The design of the NT0X42AB appears in the following figure.

NT0X42AB (end)

NT0X42AB design



Note: This diagram not drawn to scale.

NT0X42AC

Product description

The NT0X42AA power distribution center (PDC) frame uses the NT0X42AC B-feed fuse distribution panels, also known as fuse panels. The NT0X42AB A-feed fuse panels use the NT0X42AC B-feed fuse panels in an alternating pattern. The NT0X42AB and AC fuse panels are installed in pairs. A minimum of two pairs and a maximum of five pairs are installed.

Count the holes in the vertical supports of the frames from the bottom to identify Panel/shelf positions. Locate the lowest hole in the frame corresponding to the shelf to determine the position of a shelf.

In the minimum configuration, NT0X42AC B-feed fuse panels are mounted in shelf positions 58 and 50. The corresponding A-feed fuse panels are mounted at positions 62 and 54.

A standard, complete equipped PDC frame consists of 10 fuse panels for dc feeds to DMS shelves and frames. Panels in positions 58, 50, 37, 29, and 21 are on B-feed. Panels in positions 62, 54, 41, 33, and 25 are on A-feed. The system distributes feeds through busbars in the PDC frame.

Parts

The fuse distribution panel, B-feed contains 15 fuse blocks.

Fuse blocks

A fuse distribution panel contains 15 fuse blocks. The 15 fuses are allocated numbers from 00 to 14 for identification. The position number of the panel, followed by the letter F, precedes the fuse number. For example, the first fuse on the left on the top panel in the NT0X42AA PDC frame can be 62F00. This design appears in the following figure.

If any fuse on the panel blows, the fuse alarm (FA) lamp on that panel lights. The system sends a signal to the frame supervisory panel (FSP) (position 45 in the PDC frame) to trigger other alarm circuits.

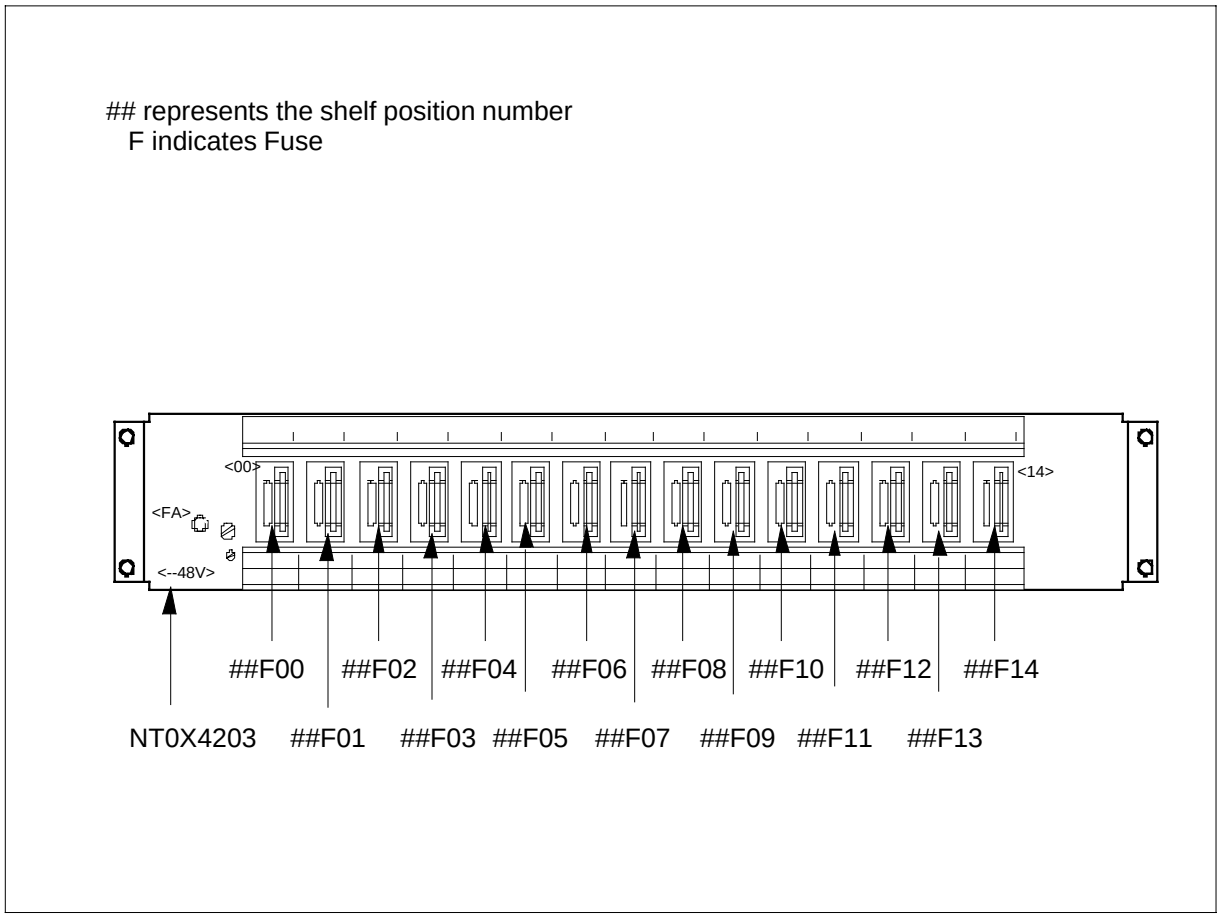
The maximum rate for any fuse block, for PDC battery feeds rated at 20 C, is 600A. The maximum rate also can be 1.5 times the maximum correct continuous feeder current demand.

Design

The design of the fuse distribution panel, B-feed, appears in the following figure.

NT0X42AC (end)

NT0X42AC design



Note: This diagram not drawn to scale.

NT0X42AE

Product description

The NT0X42AE ground panel top-feed is the most often used ground panel in the NT0X42AA power distribution center (PDC) frame. The top-feed ground plate accepts battery return cables A and B through the top of the frame. When the battery return cables connect to the battery busbars at the bottom of the PDC, the ground panel accepts cables from the bottom.

The ground panel also provides return connections for each fused feed.

The ground panel mounts in the top of the frame at hole 68. Hole 68 is approximately 68 in. from the base of the frame. Refer to the figure titled "NT0X42AE parts".

Parts

The ground panel consists of a NT0X4202 common ground plate (panel assembly) that mounts on a NT0X4222 bus bar assembly. Refer to the figure titled "NT0X42AE rear view".

Design

The following table describes the two most important parts of the NT0X42AE ground panel, top-feed.

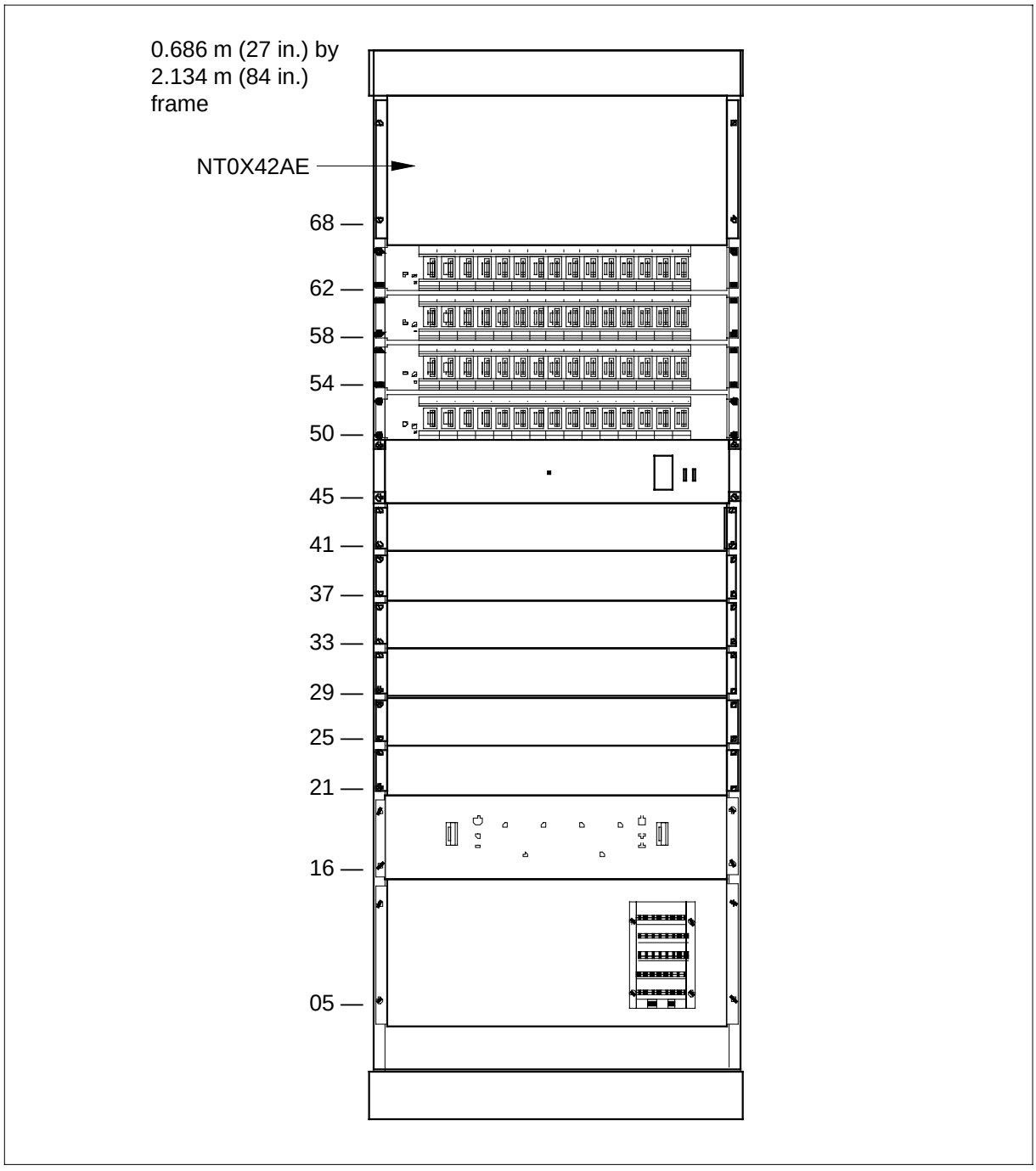
NT0X42AE parts

PEC	Slot	Description
NT0X4202		*Panel assembly* The two battery return cables and each fused feed attach to the threaded studs on the ground plate for grounding. A washer and nut fasten the cables and feeds to the studs and ground plate. The current capacity for the battery cables is 400 A.
NT0X4222		*Bus bar assembly* The busbar assembly provides a mounting for the panel assembly in the PDC at position 68.

The position of the ground panel in the NT0X42AA frame appears in the following diagram.

NT0X42AE (continued)

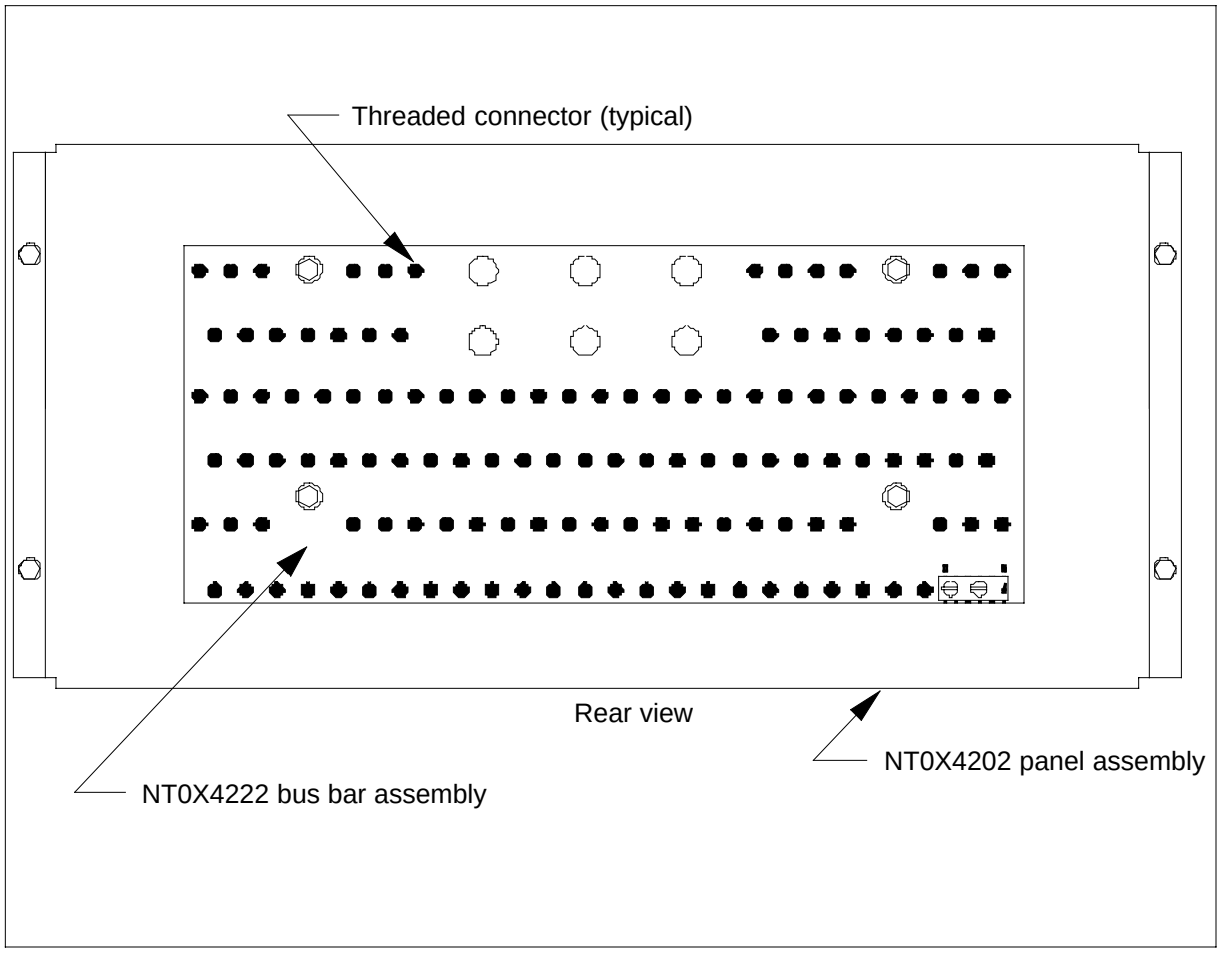
NT0X42AA frame



The ground panel appears in the following diagram.

NT0X42AE (end)

NT0X42AE rear view



Note: This diagram not drawn to scale.

NT0X42AF

Product description

The battery and return cables normally route through the top of the NT0X42AA power distribution center (PDC) frame. These cables connect to the top ends of the battery busbars. Power cabling can travel through under-floor ducts or raised floors. This PDC allows the battery and return cables to connect to the bottom ends of the battery busbars. This ability is one feature of the PDC. In this bottom feed setup, the ground plate is inverted and allows cabling from the bottom. The NT0X42AF ground panel, bottom feed, is the reverse of the NT0X42AE ground panel.

The ground panel provides battery cabling and return connections for each fused feed.

The ground panel mounts in the top of the frame at hole 68, approximately 68 in. from the base of the frame. Refer to the figure titled “NT0X42AA frame”.

Parts

The ground panel, bottom-feed contains a NT0X4222 bus bar assembly that mounts on a NT0X4202 panel assembly. Threaded studs are inserted in the bus bar assembly.

Design

The following table describes the ground panel, bottom-feed parts.

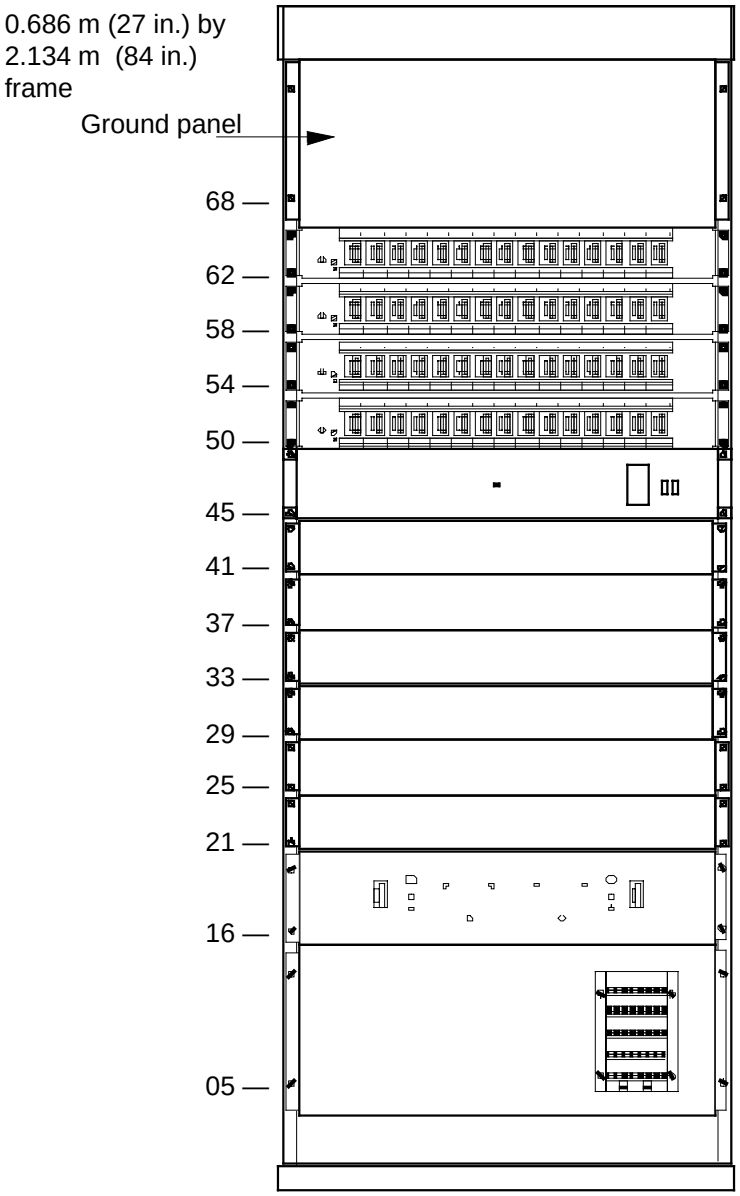
Ground panel, bottom-feed parts

PEC	Slot	Description
NT0X4202		*Panel Assembly* Two battery return cables and each fused feed attach to threaded studs on the ground plate (panel assembly) for grounding. A washer and nut fasten the cables and feeds to the studs and ground plate. The current capacity for the battery cables is 400 A.
NT0X4222		*Busbar Assembly* The busbar assembly provides a mount for the panel assembly in the PDC at position 68.

The positions of ground panel in the PDC frame appears in the following diagram.

NT0X42AF (continued)

NT0X42AA frame

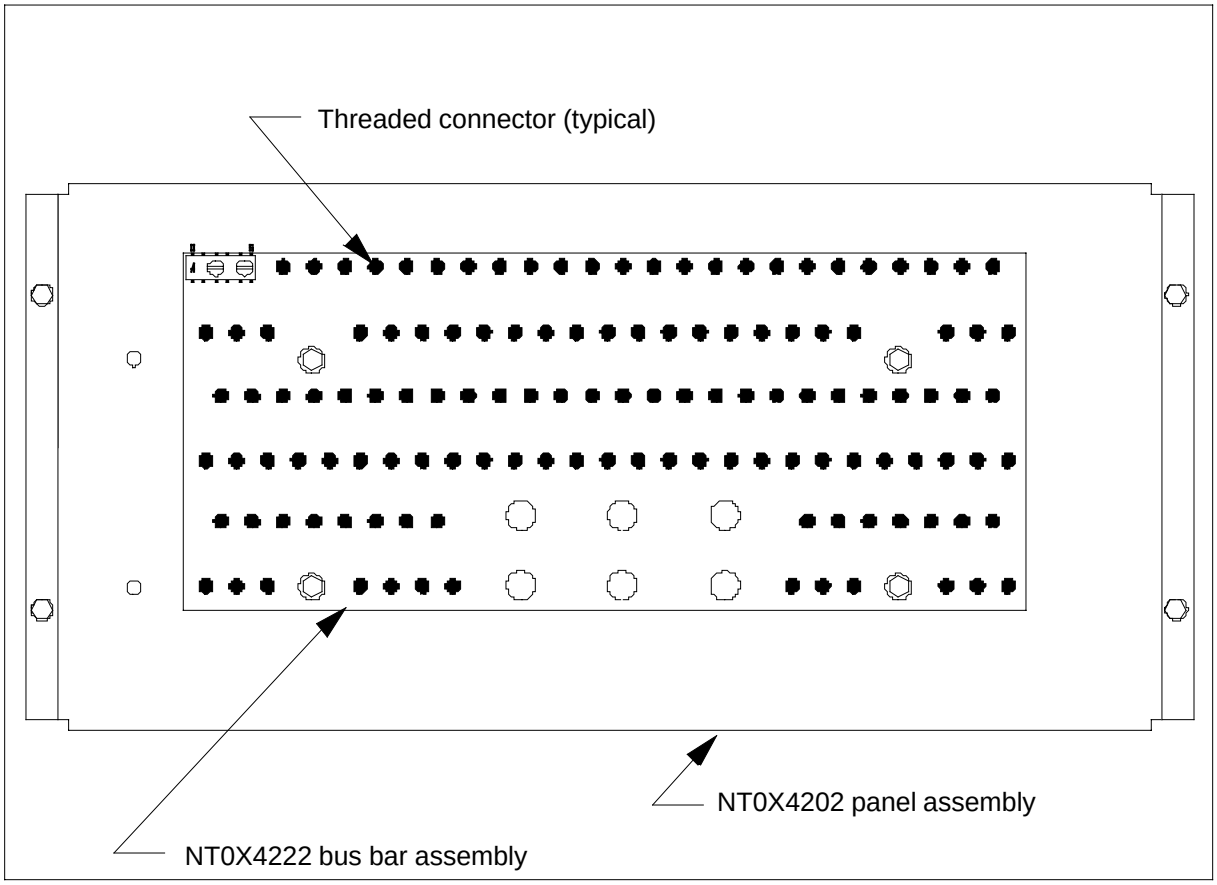


NT0X42AF (end)

Note: This diagram is not drawn to scale.

A rear view of a standard NT0X42F appears in the following figure.

NT0X42AF rear view



Note: This diagram is not drawn to scale.

NT0X42AG

Product description

The NT0X42AG filter panel unit is standard equipment on the NT0X42AA power distribution center (PDC) frame. This filter panel unit mounts at shelf position 16, as the figure on page 2 indicates. The filter panel provides noise and transient suppression components.

The NT0X42AG filter panel contains two noise and transient capacitors. Each transient capacitor has a fuse, alarm lamp and associated circuits. The negative side of one capacitor (C1) connects to the battery bus-A through filter unit fuse-A. The other capacitor (C2) connects to the battery through fuse-B.

If C1 fails and produces a short circuit, fuse-A blows. The fuse guards are normally open. When fuse-A blows, the fuse guards close and make contact. This event causes the system to send a signal to the NT0X28AF frame supervisory panel (FSP). This signal triggers other alarm circuits in the PDC frame. If C2 fails, the system response is like the response for the for C1.

The C1 and C2 provide a maximum capacitance of 36 000µF for suppression of noise of a maximum volume of 56 dBrnC. The NT0X42AG filter panel occupies position 16 in the NT0X42AA or NT0X42UA PDC frame.

Parts

The filter panel unit contains the following parts:

- capacitors, 36 000µF
- fuses, -48V/10A
- fuse alarms, FA A and FA B

Capacitors

Two capacitors provide noise and transient suppression. The capacitor that connects through fuse A to battery bus-A is labeled C1. The capacitor that connects to battery bus-B through fuse B is labeled C2.

Fuses

Capacitor C1 connects through fuse A to battery bus-A. Capacitor C2 connects to battery bus-B through fuse B. If a capacitor fails and produces a short circuit, the fuse blows. The fuse guards are normally open. When a fuse blows, the fuse guards close and make contact. The contact causes the system to send a signal to the FSP, which signals other alarm circuits.

Fuse alarms

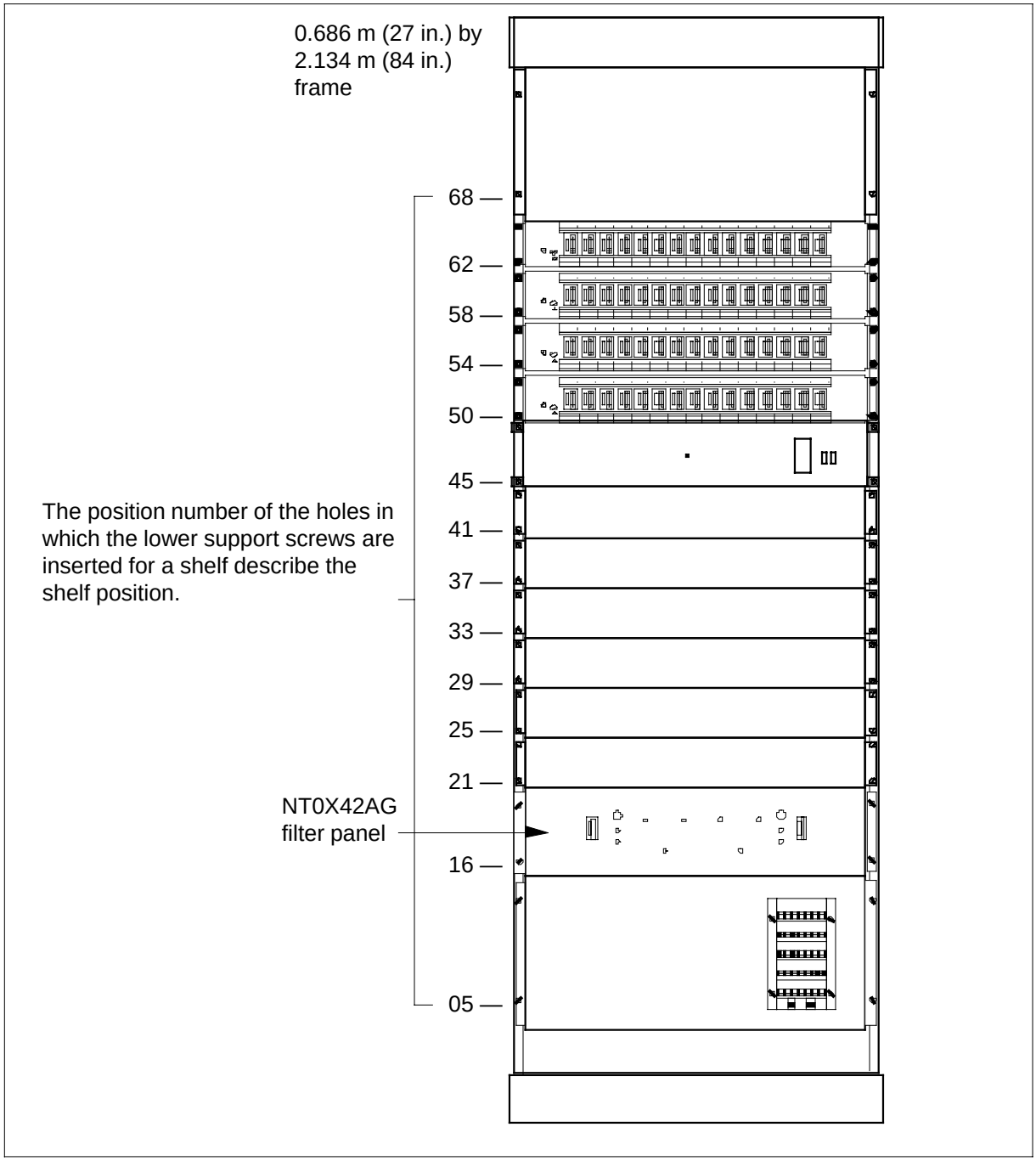
Two fuse alarms (FA) are present, one for fuse A and one for fuse B. The fuse alarm lamp lights when a capacitor fails and results in a short circuit.

NT0X42AG (continued)

Design

The location of the filter panel in the PDC frame appears in the following figure.

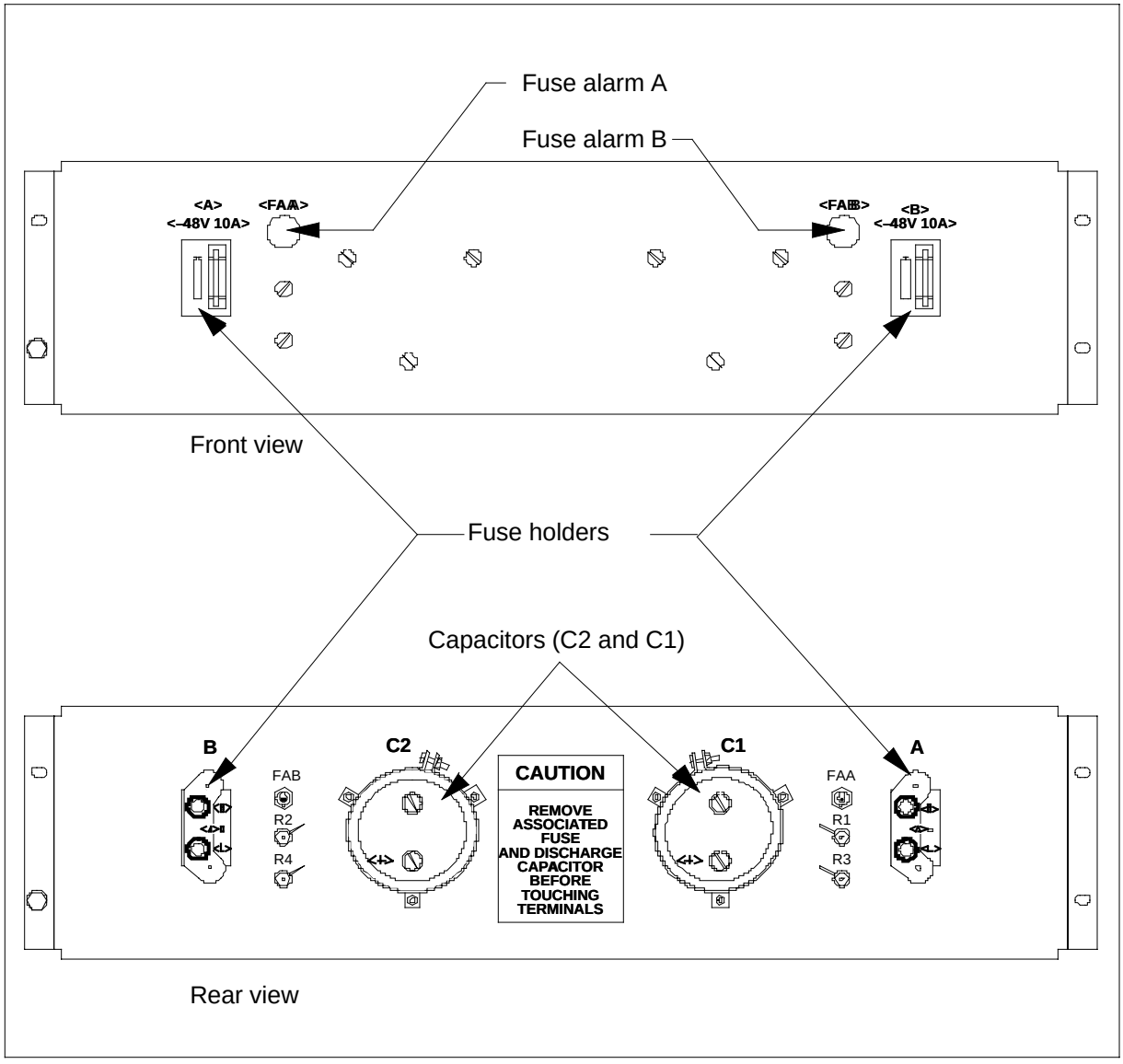
NT0X42AA frame



Note: This diagram is not drawn to scale.

The following diagram provides a detailed front and rear view of the filter panel.

NT0X42AG front and rear views



Note: This diagram is not drawn to scale.

NT0X42UA

Product description

The NT0X42UA power distribution center (PDC) frame is the Underwriters' Laboratory (UL)-approved version of the NT0X42AA PDC.

The NT0X42UA PDC is like the NT0X42AA PDC, electrically and physically, with the following exceptions:

- The fuse holders in the UA PDC have longer terminal studs.
- All frame components in the UA PDC, which include lamps, lamp containers and fuse holders, are replaced with UL-approved components.
- All double-connections on the battery return plate studs in the UA PDC (a maximum of 166 ground terminations) are removed.
- The use of Bellville washers eliminates all loose pressure connections in the UA PDC.

The NT0X42UA PDC provides an interface between the -48V (nominal) office batteries and each load in DMS-100 offices.

The NT0X42UA PDC frame contains a maximum of ten fuse panels. A standard DMS frame houses a frame supervisory panel (FSP). The frame power distribution is 200W.

The level of the holes in the vertical supports of the frames indicates the panel/shelf positions. Position 1 is the first hole at the bottom.

Operating company personnel can mount the NT0X42AU ISDN fuse panel assembly in the NT0X42UA PDC. Operating company personnel can only perform this action with an access/resource module of the digital packet network in DMS-100 ISDN offices. The NT0X42AU fuse panel holds a maximum of six fuses with ratings that range from 35A to 60A. The first panel mounts at position 21 of the PDC frame and the second mounts at position 29.

In isolated system ground (ISG) offices, operating company personnel can mount ISG logic return equalizer busbar assembly NT0X42AT in position 05 of the NT0X42UA PDC. The NT0X42UE ground panel is for ISG offices. Operating company personnel must mount ground panel NT0X42UE in position 68.

Parts

The PDC contains the following parts:

- NT0X40AB-FSP
- Fuse distribution panels:
  - — NT0X42UB-A-feed
  - — NT0X42UC-B-feed
- NT0X42AD-Filler panel
- Ground panel:
  - — NT0X42UE-Top feed
  - — NT0X42UF-Bottom feed
- NT0X42UG-Filter panel
- NT0X42AH-Filler panel

Frame supervisory panel

The NT0X40AB FSP detects alarm inputs from the fuse shelves and generates alarm outputs to the office alarm unit (OAU).

The feed for the FSP originates at busbar A. The feed provides an alarm battery supply (ABS) for the alarm circuits and lamps of the other DMS frames.

Fuse distribution panels

The fuse panels alternately connect to A-feed and B-feed. Panels in positions 62, 54, 41, 33 and 25 are on A-feed. Panels in positions 58, 50, 37, 29 and 21 are on B-feed. Feeds are distributed through busbars in the frame.

Each fuse panel has 15 fuse blocks that can contain different values of fuses. For identification purposes, the 15 fuses are numbered from 00 to 14. The position number of the panel precedes each fuse number. For example, 62F00 identifies the first fuse on the panel in position 62.

If any fuse on the panel blows, the alarm lamp (FA) on that panel lights. The system sends a signal to the FSP (position 45) to trigger other alarm circuits.

Filler panels

The NT0X42AD filler panels cover shelves that are not in use. The operating company personnel can mount fuse panels in these shelves. The shelves are at positions 21, 25, 29, 33, 37 and 41 in the PDC.

The NT0X42AH filler panel conceals a compartment that stores spare fuses. The NT0X42AH filler panel is in shelf position 05 in the PDC.

NT0X42UA (continued)

Ground panel

The ground panel contains the common battery return busbar. Two return cables are paired to battery cables that mount at the sides of the frame. These return cables connect to a common return ground plate in the ground panel. This plate also provides return connections for each fused feed.

Filter panel

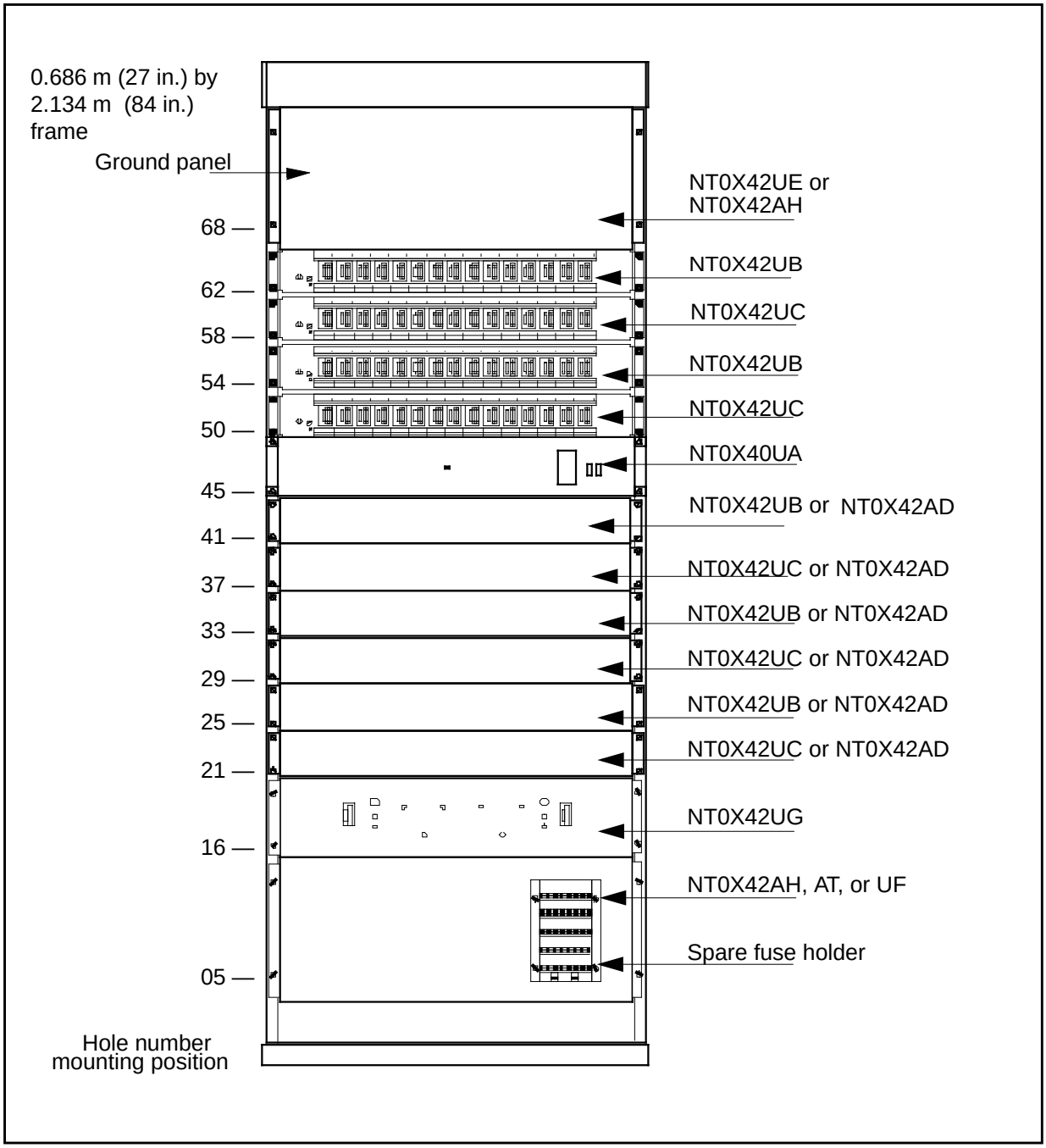
The NT0X42UG filter panel contains two noise and transient suppression capacitors. Each capacitor has a fuse, alarm lamp and associated circuits.

Design

The following diagram displays the design of the NT0X42UA.

NT0X42UA (end)

NT0X42UA parts



Note: This diagram is not drawn to scale.

NT0X42UB

Product description

The NT0X42UA power distribution centre (PDC) frame uses the NT0X42UB Underwriters Laboratory (UL)-approved A-feed fuse distribution panels. The term fuse panels can refer to the NT0X2UB UL-approved A-feed fuse distribution panels. The NT0X42UA is the UL-approved version of the NT0X42AA PDC.

The NT0X42UB panels are used in an alternating pattern with NT0X42UC UL-approved B-feed fuse panels. The NT0X42UB and UC fuse panels are installed in pairs with a minimum of two pairs and a maximum of five pairs.

The level of the holes in the vertical supports of the frames identify the panel/shelf positions. The numbers begin at the bottom of the frames. To determine the position of a shelf, locate the lowest hole in the frame that corresponds to that shelf.

In the minimum configuration, NT0X42UB A-feed fuse panels are in shelf positions 62 and 54. The associated B-feed fuse panels are in positions 58 and 50.

A fully-equipped PDC frame normally contains 10 fuse panels for DC feeds to DMS shelves and frames. Panels in positions 62, 54, 41, 33 and 25 are on A-feed. Panels in positions 58, 50, 37, 29 and 21 are on B-feed. The feeds are distributed through busbars in the PDC frame.

Note: Operating company personnel can mount the NT0X42AU ISDN fuse panel assembly in the NT0X42UA PDC. Operating company personnel can only perform this action in offices with an access/resource module of the digital packet network in DMS-100 ISDN offices. The NT0X42AU fuse panel holds a maximum of six fuses with ratings that range from 35 A to 60 A. The first panel is in position 21 of the PDC frame and the second is in position 29.

Parts

The A-feed fuse distribution panel contains 15 fuse blocks.

Fuse blocks

A fuse distribution panel has 15 fuse blocks. For identification purposes, the 15 fuses are numbered from 00 to 14. The position number of the panel, followed by the letter F, precedes each fuse number. For example, the first fuse on the left of the top most panel in the NT0X42UA PDC frame is labeled 62F00. Refer to the figure on page 2 for a visual representation of this scheme.

If a fuse on the panel blows, the alarm fuse (FA) lamp on that panel lights. The system sends a signal to the frame supervisory panel (FSP), in position 45 of the PDC frame, to trigger other alarm circuits.

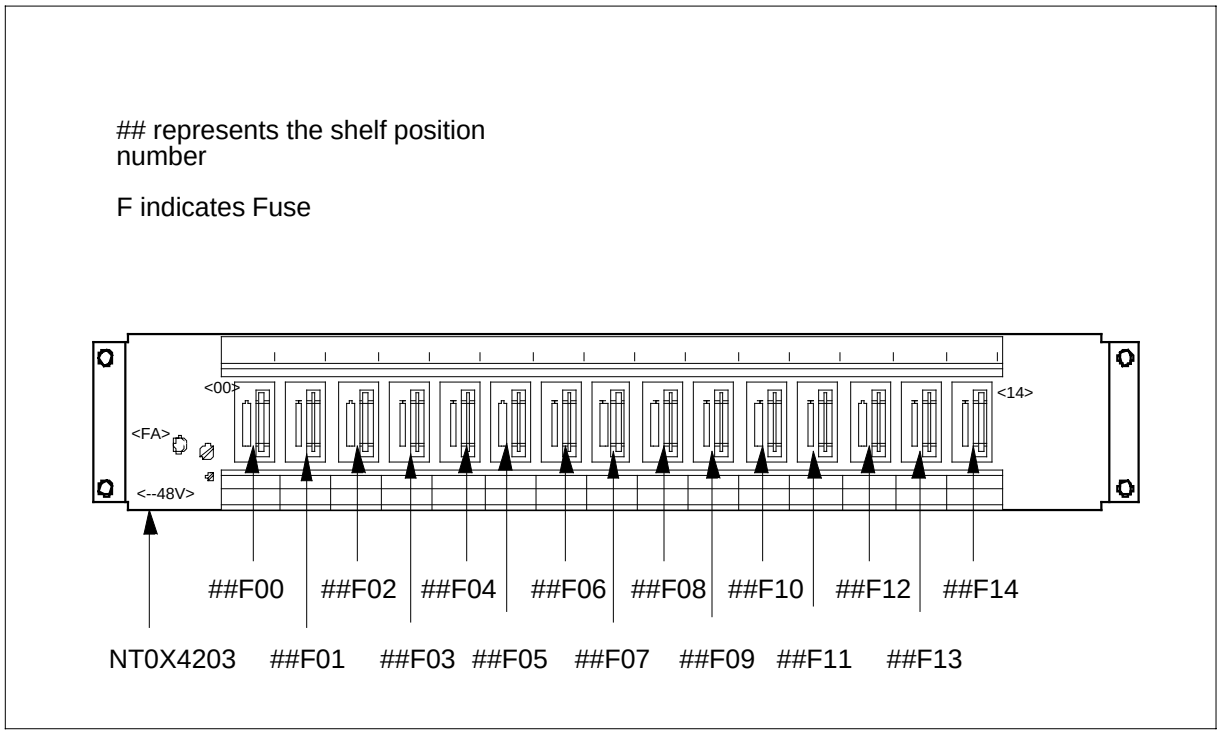
The maximum rating for any fuse block is 600A or 1.5 times the maximum continuous feeder current demand. The rating applies to PDC battery feeds rated at 20 C

Fuse holders in the UL-approved NT0X42UB panel have longer terminal studs than the fuse holders in the NT0X42AB panel. Each fuse holder is UL-approved.

Design

The following diagram displays the design of the NT0X42UB.

NT0X42UB design



Note: This diagram is not drawn to scale.

NT0X42UC

Product description

The NT0X42U power distribution center (PDC) frame uses the B-feed fuse distribution panel. The term fuse panels can refer to the NT0X42UB UL-approved A-feed fuse distribution panels. The PDC frame uses the NT0X42UC panels in an alternating pattern with NT0X42UB A-feed fuse panels. The NT0X42UC and UB fuse panels are installed in pairs with a minimum of two pairs and a maximum of five pairs.

The level of the holes in the vertical supports of the frames identifies the panel/shelf positions. The numbers begin at the bottom of the vertical supports. To determine the position of a shelf, locate the lowest hole in the frame that corresponds to the shelf.

In the minimum configuration, NT0X42UC B-feed fuse panels are in shelf positions 58 and 50. The associated A-feed fuse panels mount in positions 62 and 54.

A complete equipped PDC frame normally contains 10 fuse panels for DC feeds to DMS shelves and frames. Panels in positions 58, 50, 37, 29 and 21 are on B-feed. Panels in positions 62, 54, 41, 33 and 25 are on A-feed. The feeds are distributed through busbars in the PDC frame.

Note: Operating company personnel can mount the NT0X42AU ISDN fuse panel assembly in the NT0X42UA PDC. The operating company can perform this action only for offices with an access/resource module of the digital packet network in DMS-100 ISDN offices. The NT0X42AU fuse panel holds a maximum of six fuses with ratings that range from 35 A to 60 A. The first panel is in position 21 in the PDC frame and the second is in position 29.

Parts

The B-feed fuse distribution panel contains 15 fuse blocks.

Fuse blocks

A fuse distribution panel has 15 fuse blocks. For identification purposes, the 15 fuses are numbered from 00 to 14. The position of the panel, followed by the letter F, precedes each fuse number. For example, the first fuse on the left of the top panel in the NT0X42UA PDC frame is 62F00. Refer to the figure titled "NT0X42UC parts" for a display of this design.

If a fuse on the panel blows, the alarm fuse (FA) lamp on that panel lights. The system sends a signal to the frame supervisory panel (FSP), position 45 in the PDC frame, to trigger other alarm circuits.

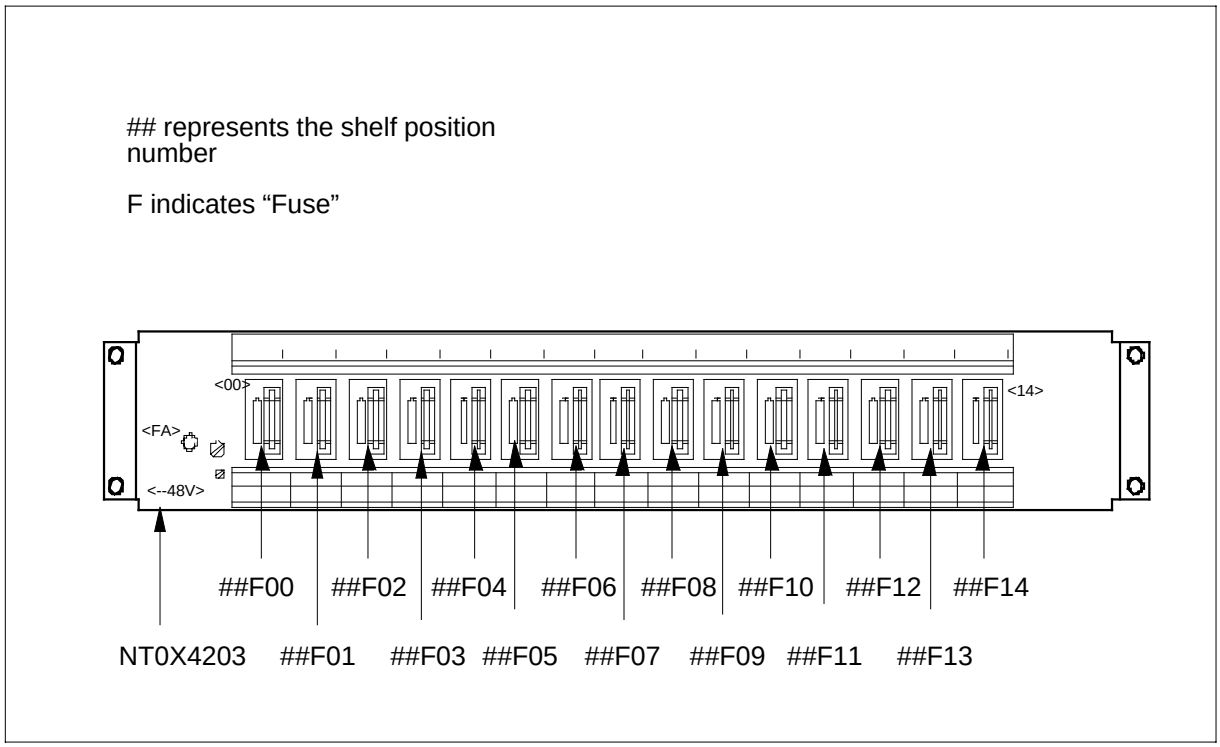
The maximum rating for a fuse block is 600 A or 1.5 times the maximum continuous feeder current demand. The rating applies to PDC battery feeds that have a rating of 20 C.

Fuse holders in the Underwriters Laboratory (UL)-approved NT0X42UC panel have longer terminal studs than the fuse holders in the NT0X42AC panel. Each fuse holder is UL-approved.

Design

The following diagram displays the design of the B-feed fuse distribution panel.

NT0X42UC parts



Note: This diagram is not drawn to scale.

NT0X42UE

Product description

The NT0X42UE ground panel, top feed, is the Underwriters' Laboratory (UL)-approved version of the NT0X42AE ground panel. The UL-approved NT0X42UA power distribution center (PDC) frame uses the NT0X42UE ground panel.

The top-feed ground plate accepts battery return cables A and B through the top of the frame. When the battery return cables connect to the battery busbars at the bottom of the PDC, the ground panel accepts cables from the bottom.

The ground panel also provides return connections for each fused feed.

The ground panel is in the top of the frame at hole 68 and is approximately 68 in. from the base of the frame. Refer to the figure titled "NT0X42UA parts".

Operating company personnel can mount an isolated system ground (ISG) logic return equalizer busbar assembly NT0X42AT in position 05 of the NT0X42UA PDC. This installation applies to ISG offices. The ground panel must be in position 68 for ISG offices.

Parts

The ground panel contains a NT0X4202 common ground plate (panel assembly) that mounts on a NT0X4225 busbar assembly. Refer to the figure on page 3.

Design

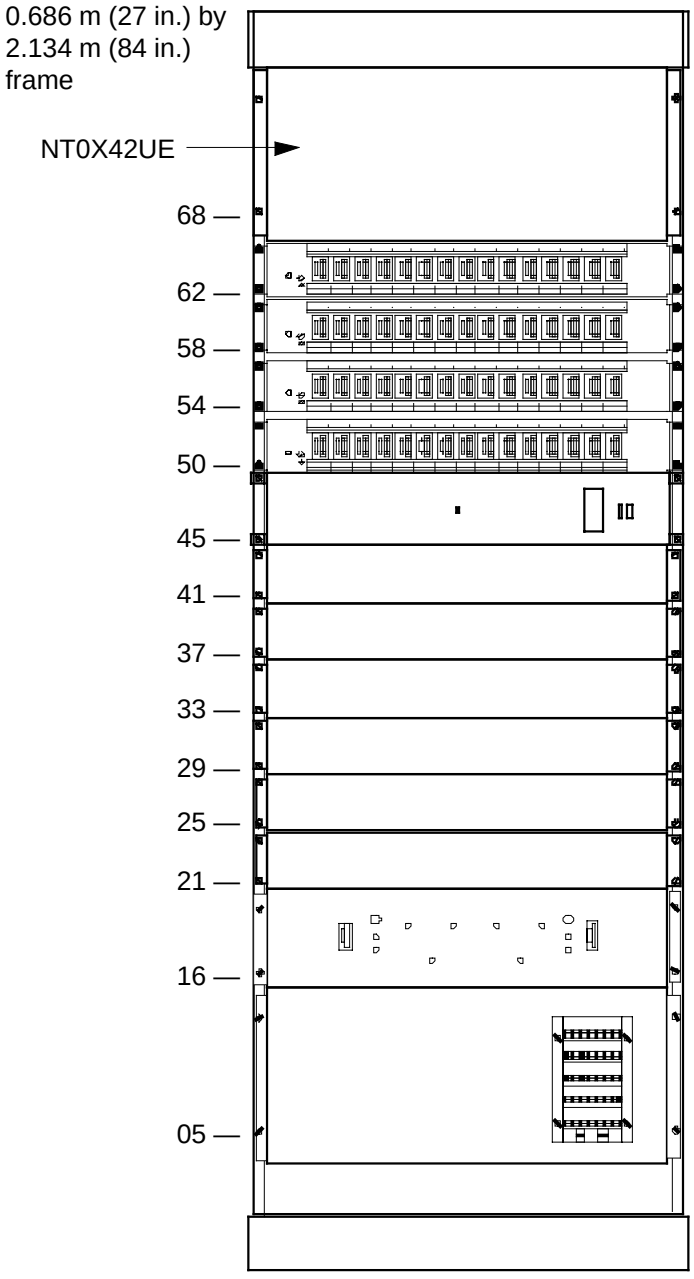
The two main parts of the NT0X42UE appear in the following table.

NT0X42UE parts

Heading	Heading	Heading
NT0X4202	N/A	*Panel assembly* Two battery return cables and each fused feed attach to threaded studs on the ground plate (panel assembly) for grounding. A washer and nut fasten the cables and feeds to the studs and ground plate. The current capacity for the battery cables is 400 A.
NT0X4225	N/A	*Busbar assembly* The busbar assembly provides a mount for the panel assembly in the PDC at position 68.

The following diagram displays the position of the ground panel in the NT0X42UA frame.

NT0X42UA parts

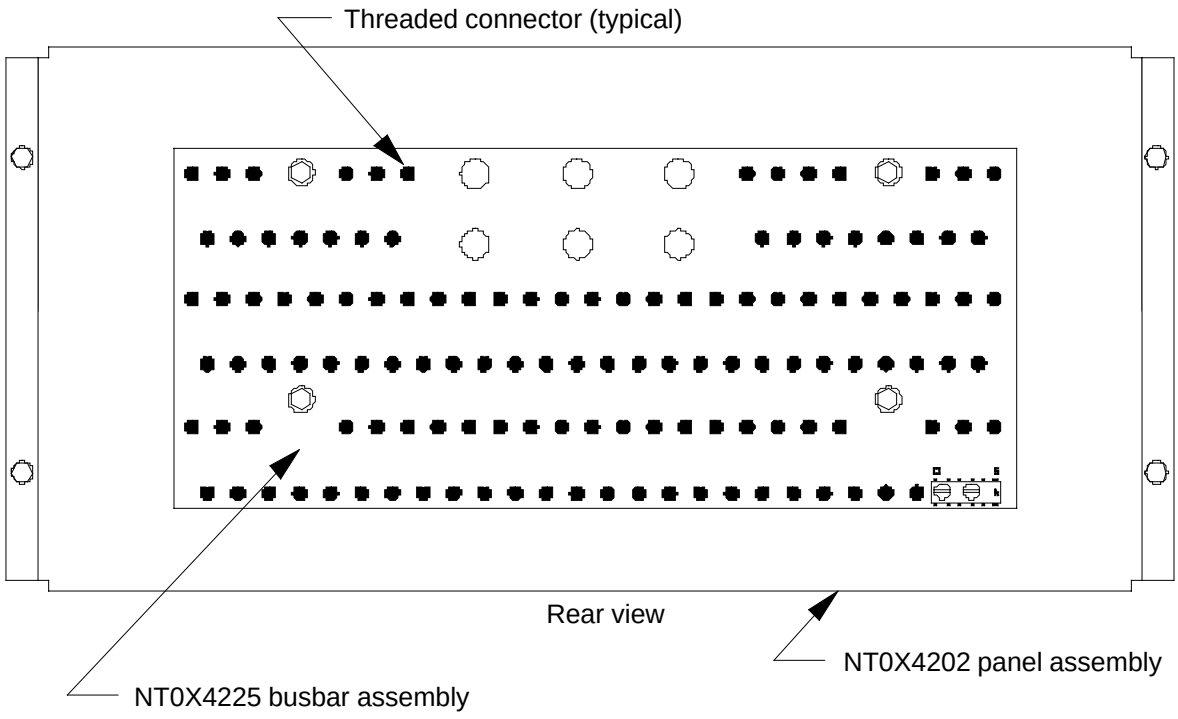


Note: This diagram is not drawn to scale.

NT0X42UE (end)

The following diagram displays the ground panel.

NT0X42UE rear view



Note: This diagram is not drawn to scale.

NT0X42UF

Product description

The NT0X42UF ground panel, bottom feed is the Underwriters' Laboratory (UL)-approved version of the NT0X42AF ground panel. The UL-approved NT0X42UA power distribution center (PDC) frame uses the NT0X42UF ground panel.

The battery and return cables route through the top of the NT0X42UA PDC frame and connect to the top ends of the battery busbars. Power cabling can travel through under-floor ducts or raised floors. In this event, the battery and return cables can connect to the bottom ends of the battery busbars. In this bottom feed setup, the ground plate allows cables from the bottom. The ground panel, bottom feed is the reverse of the NT0X42AF ground panel.

The ground panel also provides return connections for each fused feed.

The ground panel is on the top of the frame at hole 68 and is approximately 68 in. from the base of the frame. Refer to the figure titled "NT0X42UA frame".

Parts

The NT0X42UF ground panel, bottom-feed contains an NT0X4225 bus bar assembly which mounts on an NT0X4202 panel assembly. Threaded studs are inserted in the bus bar assembly.

Design

The following table describes the main parts of the NT0X42UF.

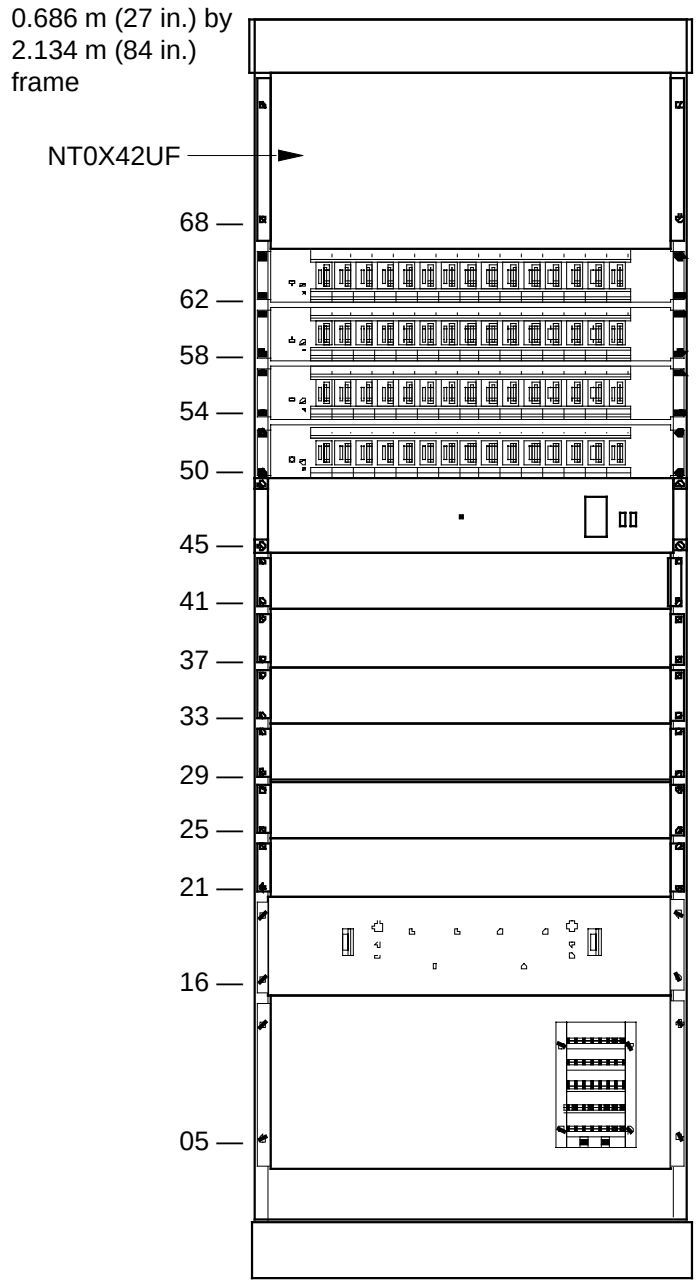
NT0X42UF parts

PEC	Slot	Description
NT0X4202	N/A	*Panel assembly* Two battery return cables and each fused feed attach to threaded studs on the ground plate (panel assembly) for grounding. A washer and nut fasten the cables and feeds to the studs and ground plate. The current capacity for the battery cables is 400 A.
NT0X4225	N/A	*Busbar assembly* The busbar assembly provides a mount for the panel assembly in the PDC at position 68.

The following diagram displays the positions of the ground panel in the NT0X42UA frame.

NT0X42UF (continued)

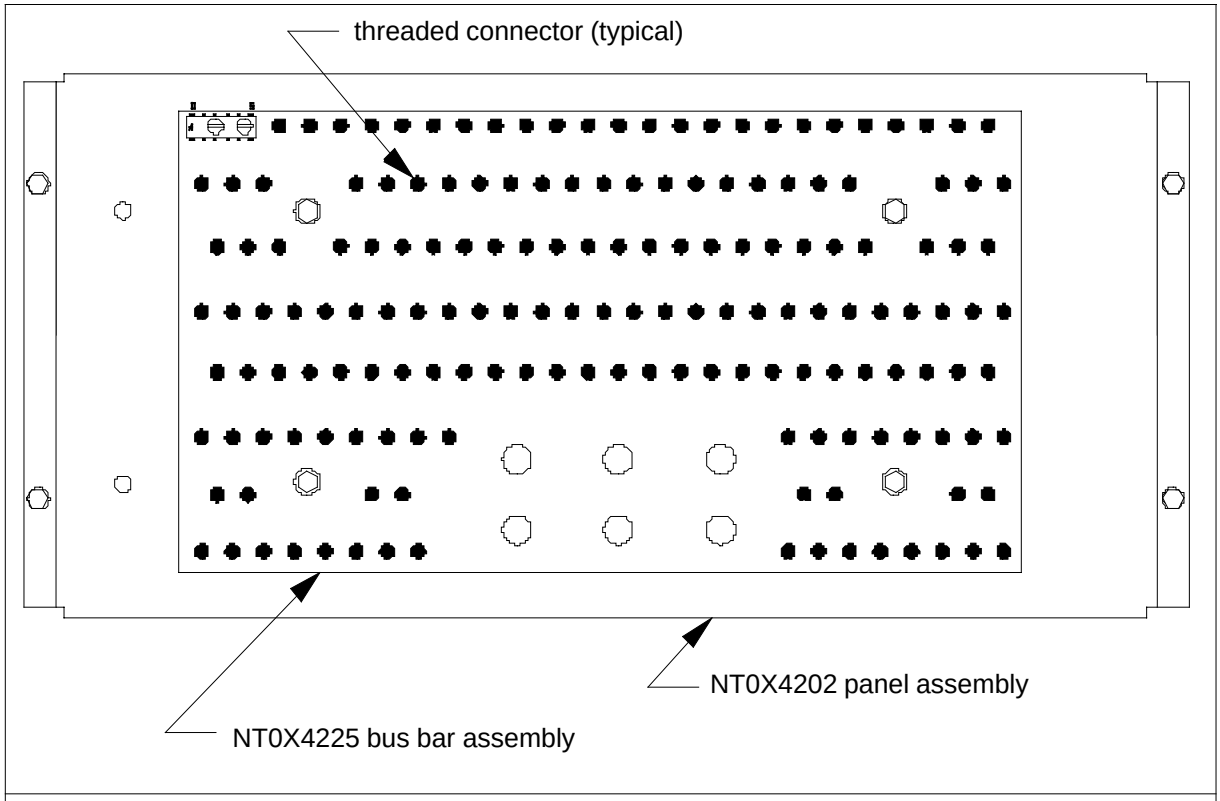
NT0X42UA frame



Note: This diagram is not drawn to scale.

The following diagram displays the rear view of a standard .

NT0X42UF rear view



Note: This diagram is not drawn to scale.

NT0X42UG

Product description

A normal, fully-equipped power distribution center (PDC) frame contains a filter panel. This filter panel suppresses noise and transient suppression components.

The NT0X42UA PDC, the Underwriters Laboratory (UL)-approved version of the NT0X42AA PDC, uses a NT0X42UF filter panel. The NT0X42UF is the UL-approved version of the NT0X42AG filter panel. The fuse holders in the UL-approved filter panel have longer terminal studs than the terminal studs in the NT0X42AG panel. Each fuse holder is UL-approved.

The NT0X42UF filter panel contains two noise and transient capacitors that have a fuse, alarm lamp, and associated circuit. The negative side of one capacitor (C1) connects to the battery bus-A through filter unit fuse-A. Capacitor C2 connects to the battery through fuse-B.

If C1 fails, fuse A blows. The C1 fails when the C1 produces a short circuit. The fuse guard that is normally open, closes to make contact. A signal is sent to the NT0X28AF frame supervisory panel (FSP). This signal triggers other alarm circuits in the PDC frame. If C2 fails, the system response is the same as the system response for C1.

The C1 and C2 provide a maximum capacity of 36 000 µF to suppress noise to a maximum of 56 dBrnC. The NT0X42UF filter panel occupies position 16 in the NT0X42UA PDC frame.

Parts

The UL-approved filter panel unit shelf contains the following parts:

- capacitors, 36 000 µF
- fuses, -48V/10A
- fuse Alarms, FA A and FA B

Capacitors

Two capacitors provide noise and transient suppression. The capacitor that connects through fuse A to battery bus-A is labeled C1. The capacitor C2 that connects to battery bus-B through fuse B is labeled C2.

Fuses

Capacitor C1 connects through fuse A to battery bus A. Capacitor C2 connects to battery bus-B through fuse B. If a capacitor fails, the fuse blows. The capacitor fails when the capacitor produces a short circuit. The fuse guards that

are normally open, make contact. The system sends a signal to the FSP. The FSP signals other alarm circuits.

Fuse alarms

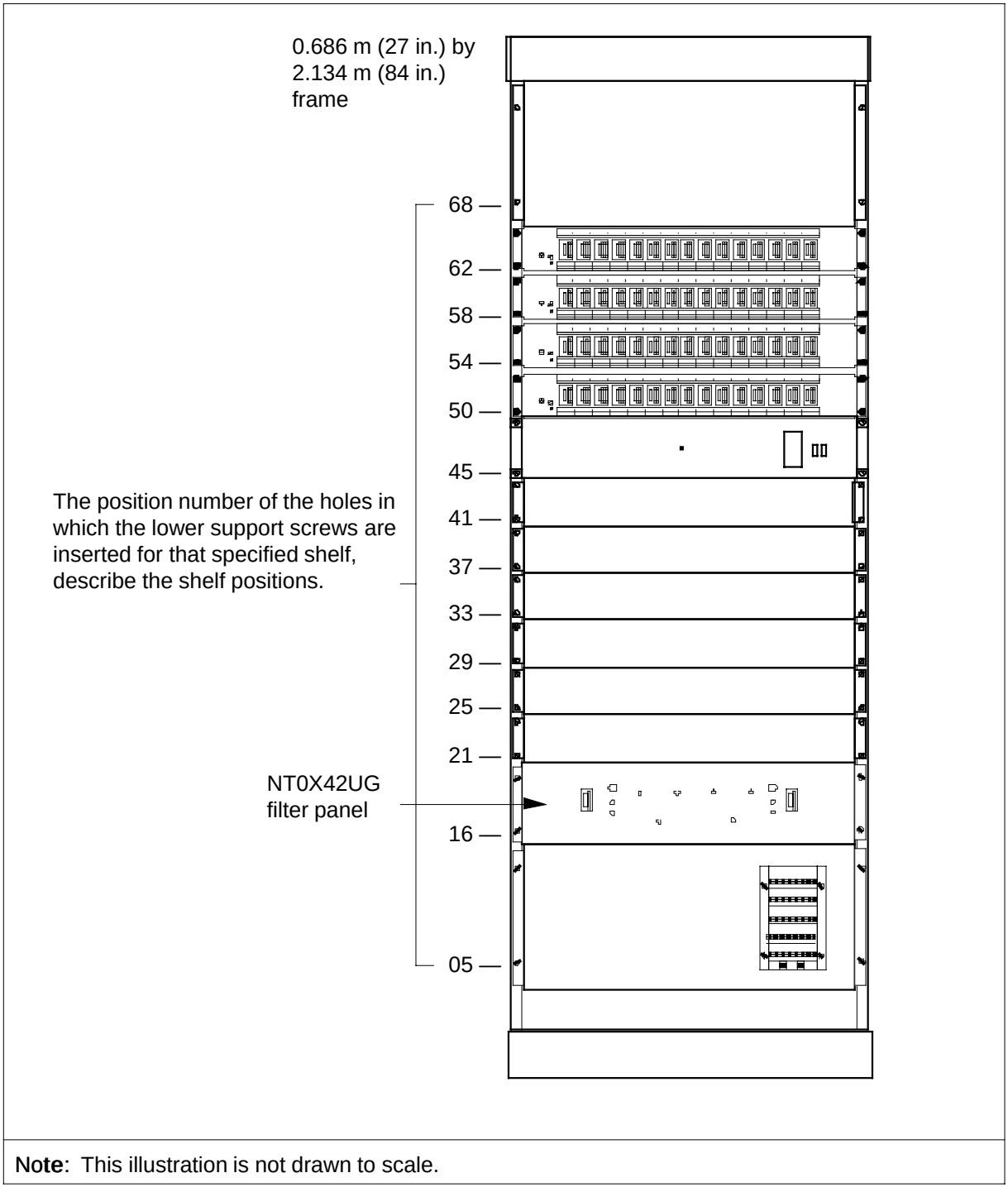
Two fuse alarms (FA) can occur. One alarm is for fuse A. The other alarm is for fuse B. The fuse alarm lamp lights when a capacitor fails, which results in a short circuit.

Design

The location of the filter panel in the NT0X42UA frame appears in the following example.

NT0X42UG (continued)

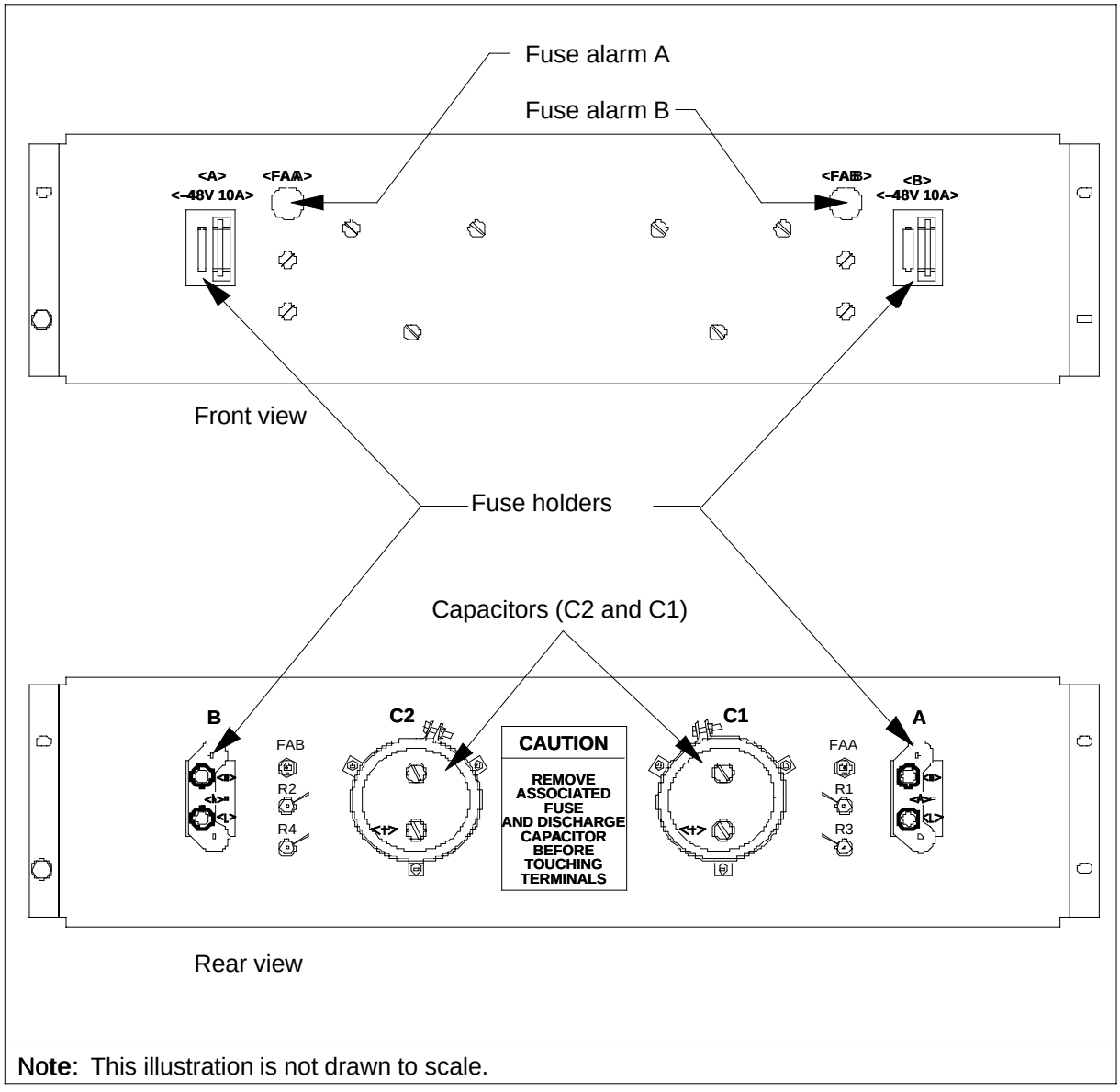
NT0X42UF frame



Note: This illustration is not drawn to scale.

The following figure provides a detailed front and rear view of the NT0X42UG.

NT0X42UG front and rear views



Note: This illustration is not drawn to scale.

NT0X43AD

Product description

The NT0X43AD enhanced input/output (I/O) equipment frame provides a rack in which data management equipment is mounted. This data management equipment normally contains the following features:

- an input/output control (IOC) shelf
- storage devices, like a tape or hard disk unit
- a data flow controlling device, called the distributed processing peripheral (DPP)

Parts

The completely equipped improved input/output (I/O) equipment frame contains groups of the following parts:

- NT0X28AL-Frame supervisory panel (FSP)
- NT0X44AA-Magnetic tape drive (MTD) unit Hewlett Packard
- NT0X44AB-MTD unit (Cook)
- NT0X44BB-International MTD unit (Cook)
- NT0X87AA-Inverter unit
- NT1X60AB-Data set shelf
- NT1X61AB-I/O control shelf
- NT1X61AD-I/O control shelf
- NT3X95AA-Stratum II remote oscillator shelf
- NT3X95AB-Stratum II remote oscillator shelf
- NT3X95BA-Stratum 2.5 remote oscillator shelf
- NT3X95BB-Stratum 2.5 remote oscillator shelf
- NT4X00AA-Disk drive unit (DDU) shelf
- NT4X00AB-DDU shelf
- NT4X00AC-DDU shelf
- NT4X00AF-Dual DDU shelf
- NT5X08AC-Data set shelf
- NT8X48AA-DPP
- NT8X48AB-DPP

- NT8X48BA-DPP
- NT8X48AD-DPP

Frame supervisory panel

The NT0X28AL FSP contains power control and alarm circuits. These circuits provide interfaces between the I/O equipment frame and the PDC in the digital switching system. The following circuit packs contain power control and alarm circuits:

- NT0X91AE (power control and alarm)
- NT0X91AA (alarm and converter drive)
- NT0X91AD (converter drive and protection circuit)
- NT0X91AE (converter drive and protection circuit)

The NT0X28AL FSP uses four power feeds and fuses to protect the power control and alarm circuits.

Magnetic tape drive unit

The NT0X43AD frame can use the following three types of tape drives:

- Hewlett Packard MTD unit (NT0X44AA)
- Cook MTD unit (NT0X44AB)
- Cook international MTD unit (NT0X44BB)

Tapes store customer information.

Inverter unit

The NT0X87AA inverter converts -48V (nominal) input dc to 117V, 60 Hz ac output to supply additional devices. These devices include:

- teleprinters
- cooling fans
- MAP terminals

The power distribution center (PDC) supplies the -48V input voltage.

Data set shelf

The data set shelf contains modems. These modems allow the local switching system to communicate to remote systems or peripherals over dial-up or dedicated lines.

NT0X43AD (continued)

I/O control shelf

The IOC provides an interface between a pair of central message controllers (CMC) and a maximum of nine microprocessor-based device controllers (DC). The IOC relays central control-generated messages by way of the CMC to I/O device controllers. The IOC accepts messages from DCs for transmission to the central control. The DMS-100 Family can handle a maximum of six pairs of IOCs.

Stratum II or 2.5 oscillator shelf

The NT3X95AA remote oscillator shelf stores the NT3X16AA Stratum II oscillator and interface card. The interface card is part of the synchronized master clock system. This clock system provides a clock frequency signal that controls circuit timing in the peripherals.

The NT3X16AA card operates with the NT3X15DA Stratum II synchronizable master clock oscillator card. The NT3X16AA card also operates with the NT3X14 synchronized master clock counter card (controller).

The NT3X95AA shelf stores four NT3X16AA cards. One card is active. One card is inactive. Two cards are in hot standby mode. The user places in service the cards that are in hot standby mode.

The NT3X14 synchronizable master clock counter card distributes the 10.2400 MHz clock signal that an associated NT3X15 card generates. The NT3X14 card acts as an interface between the NT3X15 and the CPU.

The NT3X14 generates and distributes frame pulse signals to the CMC and the office peripherals.

The NT3X14 generates a time-of-day clock. The NT3X14 monitors master oscillator and frame pulse generators for failure. If a failure occurs, the NT3X14 activates a second NT3X14/NT3X15 pair.

The NT3X15 synchronizable master clock oscillator card uses an associated NT3X14 to distribute a 10.2400 MHz signal to the CMC and office peripherals.

Single or dual DDU

The DDU stores and retrieves customer information. The DDU contains a hard disk and the immediate hardware and software components.

In many DMS-100 Family functions, like automatic message accounting (AMA), hard disks replace tape units as the main storage device.

DPP

The DMS-100 Family DPP is an AMA transmitter that provides an automatic message accounting teleprocessing system (AMATPS) interface. The AMA transmitter provides this interface between DMS-100 Family switches and a host office collector (HOC).

The DPP allows a direct teleprocessing link with the HOC to manage AMA data. Enhanced hardware and software capabilities specified for data collectors and AMA transmitters enable this process. These capabilities conform to Bell Communications Research (Bellcore) TR-TSY-000385 specifications.

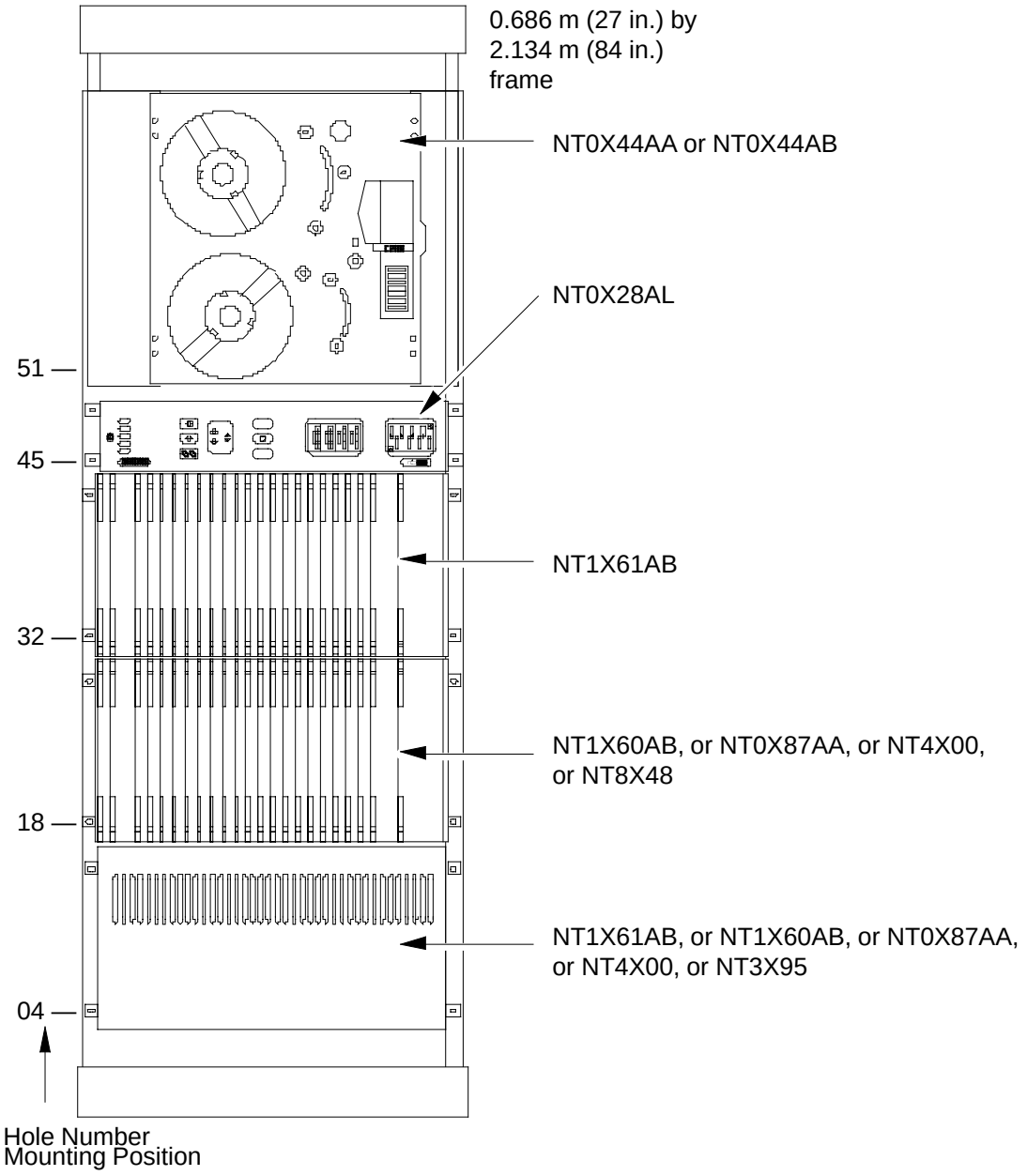
The DPP offers maintenance and communications through the DMS-100 MAP terminal. The DMS-100 MAP terminal provides a known platform for personnel. This platform allows personnel to perform operations, administration, and maintenance functions. The DPP can use different sizes of storage disk.

Design

The design of the NT0X43AD appears in the following figure.

NT0X43AD (end)

NT0X43AD parts



Note: This drawing is not to scale.

NT0X44AA

Product description

The NT0X44AA magnetic tape drive (MTD) unit [Hewlett-Packard(HP)] stores customer information for the operation of the DMS-100 Family of digital switches. For example, the automatic message accounting system (AMA) uses the tape unit, or a hard disk unit, to store call accounting information.

The NT0X44AA MTD unit is mounted on the NT0X43AC magnetic tape center frame and uses a reel-to-reel format. Refer to the following figure.

Parts

The NT0X44AA contains the tape drive, the control panel, and the tape reels. You can remove the tape reels.

Design

A description of the NT0X44AA controls and indicators appears in the following table. The figure that follows the table shows the NT0X44AA.

NT0X44AA controls and indicators (Sheet 1 of 2)

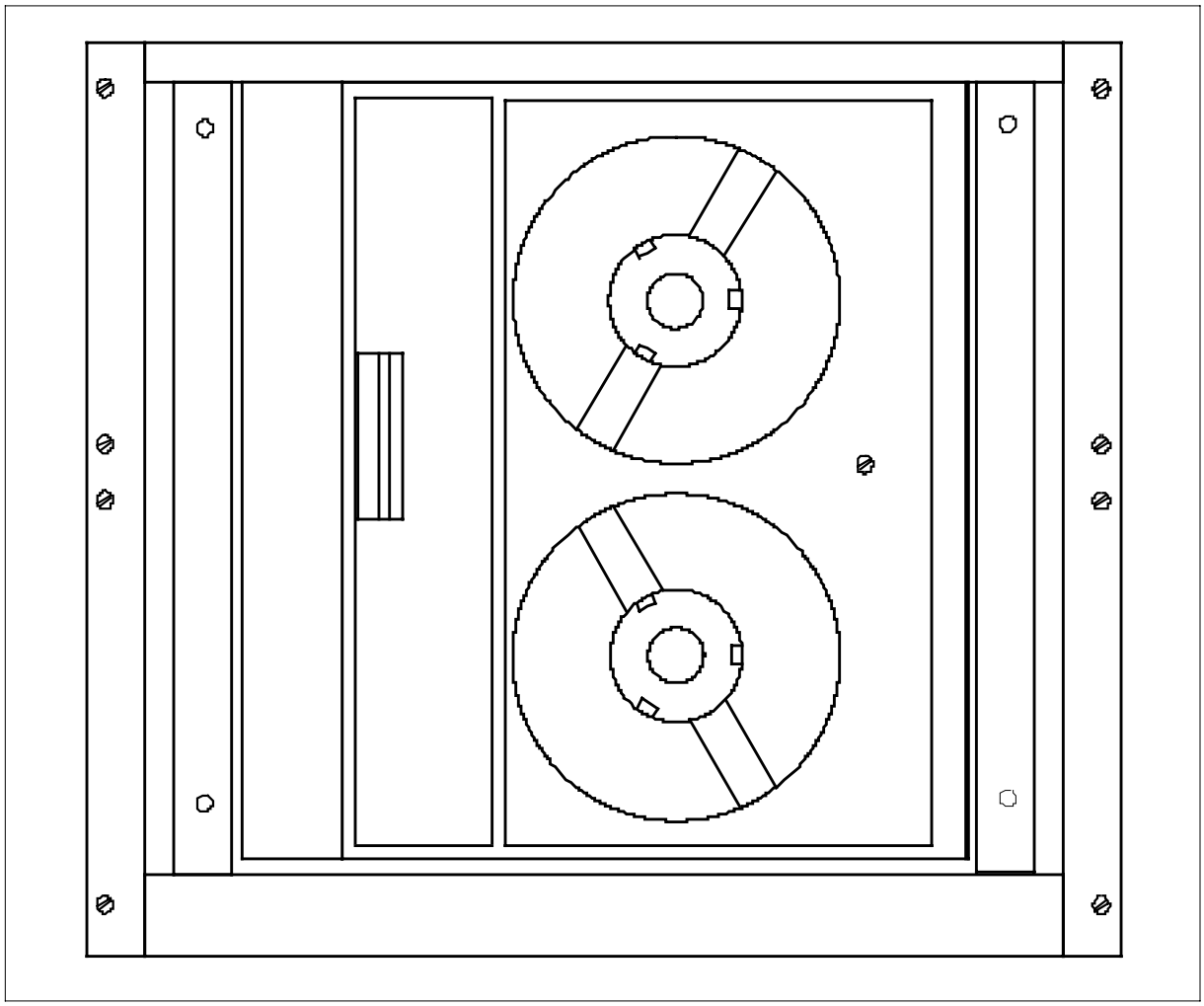
Control	Type	Function
RESET	Switch and indicator	To stop tape travel, remove tape unit from ON LINE status. Stop loadpoint search.
REWIND	Switch and indicator	Press to rewind the tape. Tape rewinds until tape reaches the loadpoint-start of tape (BOT) tab. The tape stops. To unload the tape, press REWIND when the tape reaches the loadpoint. The tape rewinds until the end of the tape runs off the take-up reel.
ON LINE	Switch and indicator	To put the tape unit under system control, press ON LINE. The indicator lights up when the system controls the tape unit.
LOAD	Switch and indicator	Use this control to initiate a loadpoint search.
WRITE ENABLE	Indicator	Indicates when the MTU is in write mode. If a tape reel with a write ring installed is on the MTU, this indicator lights up.

NT0X44AA (end)

NT0X44AA controls and indicators (Sheet 2 of 2)

Control	Type	Function
LOCAL INHIBIT	Indicator	Refer to Section 0310 of the NT Installation Manual 925 for a description of this control.
POWER	ON-OFF toggle switch	Connects/disconnects power to the MTD unit.

NT0X44AA front view



NT0X44AB

Product Description

The NT0X44AB magnetic tape drive unit (MTU) (Cook) stores customer information for the operation of the DMS-100 Family of digital switches. For example, the automatic message accounting system (AMA) uses the tape unit, or a hard disk unit, to store call accounting information.

The NT0X44AB MTU is mounted on the NT0X43AC magnetic tape center frame and uses a reel-to-reel format. Refer to the following figure.

Parts

The NT0X44AB contains the tape drive, the control panel, and the tape reels. You can remove the tape reels.

Design

A description of the controls for the NT0X44AB MTU appear in the following table.

NT0X44AB controls and indicators (Sheet 1 of 2)

Control	Type	Function
POWER	ON-OFF toggle switch	This connects/disconnects power to the MTU.
LOAD	Switch and indicator	Press LOAD to cause the MTU to put tension on the tape and raise the arms to the null position. Press LOAD again to initiate a loadpoint search.
ON LINE	Switch and indicator	To put the tape unit under system control, press ON LINE. The indicator lights up when the system controls the tape unit.
REWIND	Switch and indicator	Press to rewind the tape. Tape rewinds until switch senses the loadpoint-start of tape (BOT) tab. The tape slows to a stop, and moves forward slowly to the loadpoint. At loadpoint, the tape stops. To unload the tape, when the tape is at the loadpoint, press REWIND. The tape rewinds until the end of the tape runs off the take-up reel. Power stops to each motor.

NT0X44AB (continued)

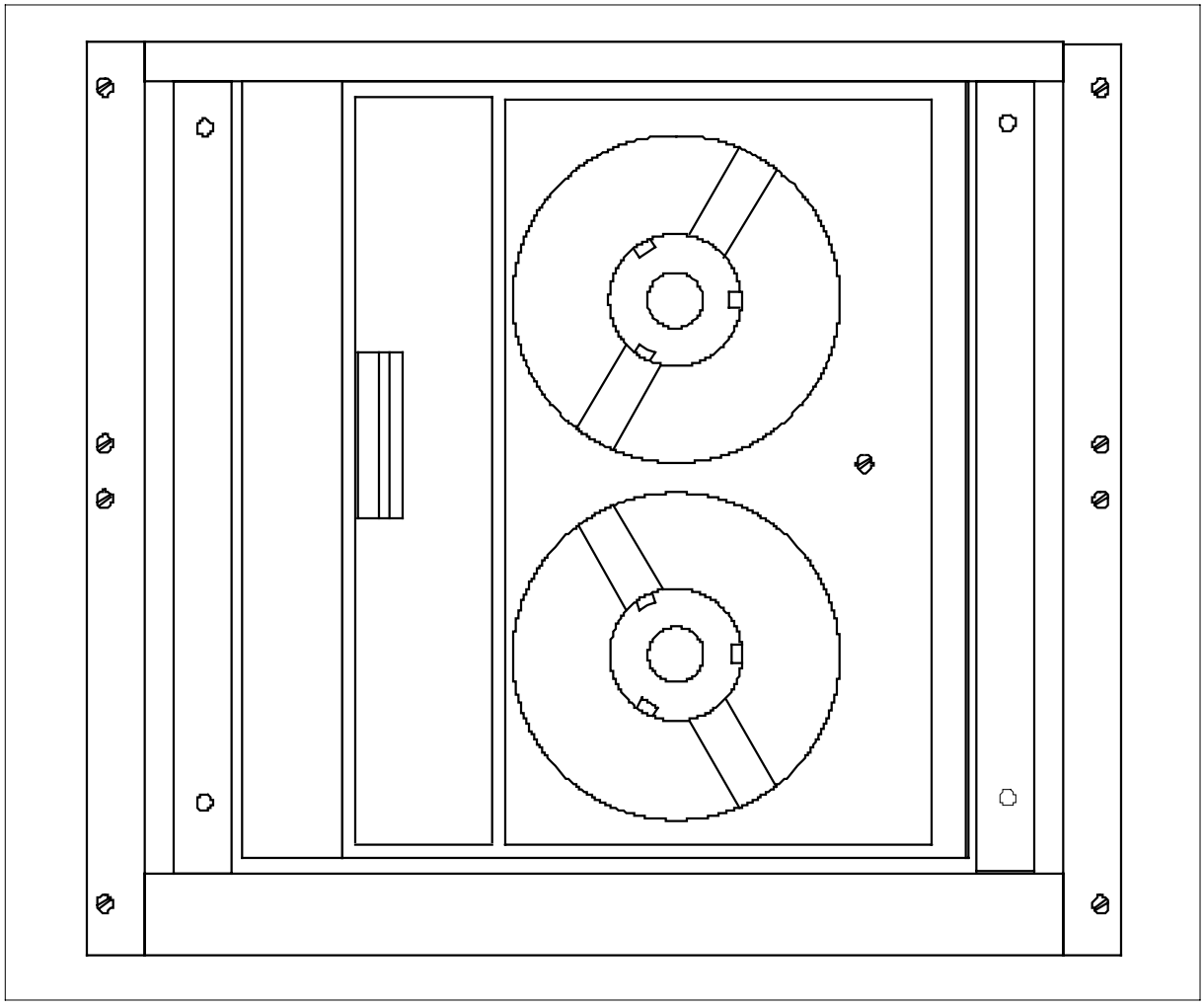
NT0X44AB controls and indicators (Sheet 2 of 2)

Control	Type	Function
FORWARD	Switch and indicator	Use this control to initiate forward tape movement until the following actions stop the movement: • a second switch (FORWARD) activated • End-of-tape (EOT) marker detected • REVERSE or REWIND operated
REVERSE	Switch and indicator	Use this control to reverse the tape movement until the following actions stop the movement: • a second switch (REVERSE) activated • BOT marker detected • FORWARD or REWIND operated
WRITE ENABLE	Indicator	Indicates when the MTU is in write mode. If a tape reel with a write ENABLE ring installed is on the MTU, this indicator lights up.

The design of the NT0X44AB appears in the following figure.

NT0X44AB (end)

NT0X44AB front view



Note: This diagram is not drawn to scale.

NT0X44BB

Product Description

The NT0X44BB international magnetic tape drive unit (MTU) (Cook) stores customer information for the operation of the DMS-100 Family of digital switches. For example, the automatic message accounting system (AMA) uses the tape unit, or a hard disk unit, to store call accounting information.

The NT0X44BB international MTU is on the NT0X43AD input/output equipment (IOE) frame and uses a reel-to-reel format.

Parts

The NT0X44BB contains the following parts:

Design

A description of the controls for the NT0X44BB appears in the following table.

NT0X44BB controls and indicators (Sheet 1 of 2)

Control	Type	Function
POWER	ON-OFF toggle switch	This connects/disconnects power to the MTU.
LOAD	Switch and indicator	Press LOAD to cause the MTU to put tension on the tape and raise the arms to the null position. Press LOAD again to initiate a loadpoint search.
ON LINE	Switch and indicator	To put the tape unit under system control, press ON LINE. The indicator lights up when the system controls the tape unit.
REWIND	Switch and indicator	Press REWIND to rewind the tape. Tape rewinds until the switch senses the loadpoint-start of tape (BOT) tab. The tape slows to a stop, and moves forward slowly to the loadpoint. At loadpoint, the tape stops. To unload the tape, when the tape reaches the loadpoint, press REWIND. The tape rewinds until the end of the tape runs off the take-up reel. Power stops to the motors.

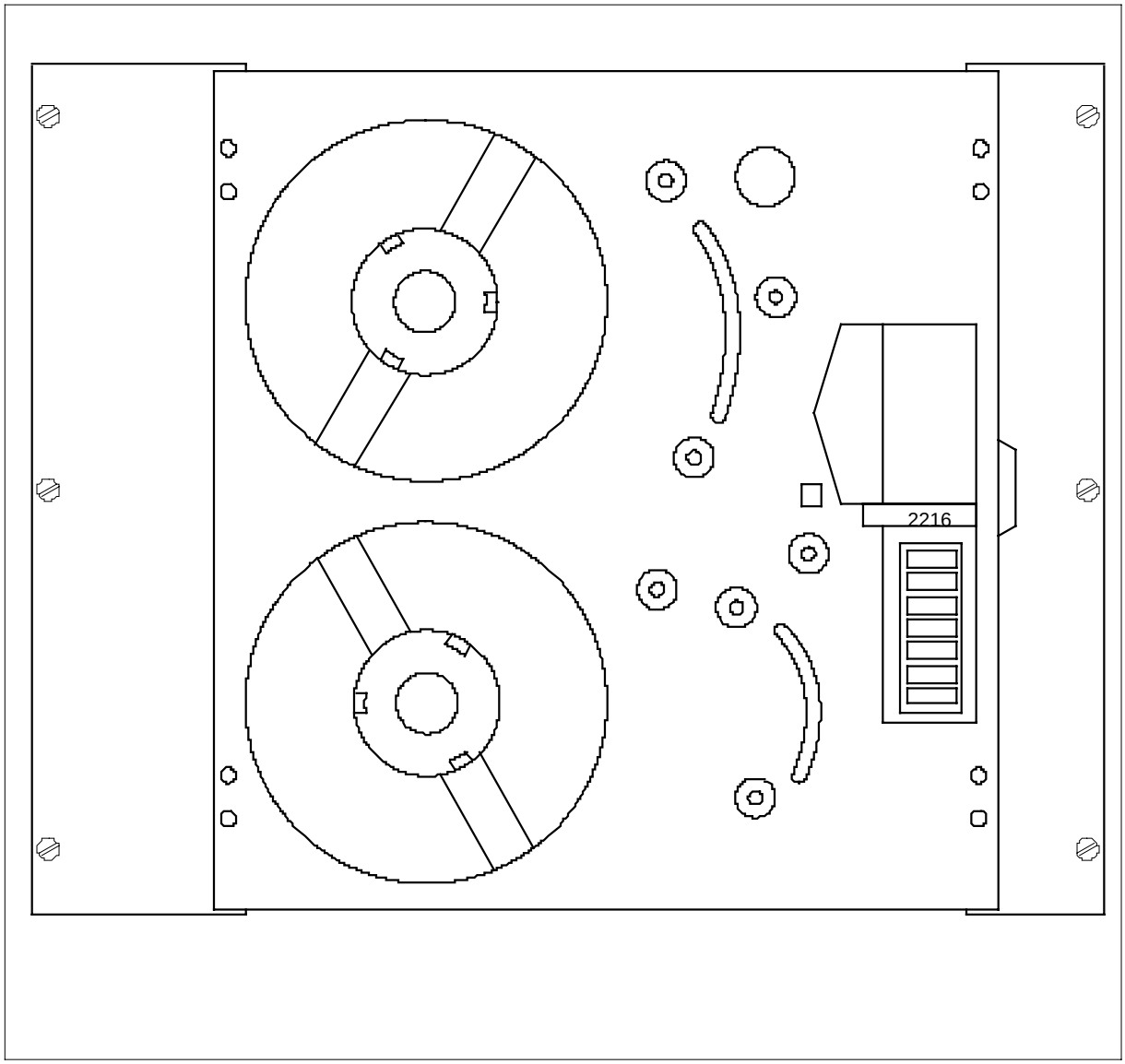
NT0X44BB controls and indicators (Sheet 2 of 2)

Control	Type	Function
FORWARD	Switch and indicator	Use FORWARD to initiate forward tape motion until the following actions stop the motion: • a second switch (FORWARD) activated • End-of-tape (EOT) marker detected • either REVERSE or REWIND operated
REVERSE	Switch and indicator	Use this control to reverse the tape motion until the following actions stop the motion: • a second switch (REVERSE) activated • BOT marker detected • FORWARD or REWIND operated
WRITE ENABLE	Indicator	This control indicates when the MTU is in write mode. If a tape reel with a write ENABLE ring installed is on the MTU, this indicator lights up.

The design of the NT0X44AB appears in the following figure.

NT0X44BB (end)

NT0X44BB front view



Note: This diagram is not drawn to scale.

NT0X46AB

Product Description

The system can configure the NT0X46AB frame as a trunk module equipment frame or a digital carrier equipment frame.

The trunk module equipment (TME) frame stores trunk modules, maintenance trunk modules, and an alarm cross-connect unit. Subject to specified limits, the TME frame can have a digital carrier module or digital echo suppressor module.

The following module groups avoid overload of the power supply of the trunk module equipment frame:

- five trunk module shelves in positions 65, 51, 32, 18, and 04
- four trunk module shelves and one maintenance trunk module shelf
- three trunk module or maintenance trunk module shelves with another maintenance trunk module shelf in position 51. One alarm cross-connect unit shelf in position 65. The specified module group appears in the figure on page 5 that illustrates the TME frame design.
- two trunk module or maintenance trunk module shelves and one digital carrier module shelf. Another maintenance trunk module shelf is in position 51. One alarm cross-connect unit shelf in position 65

The following types of trunk modules can appear in the trunk module equipment frame:

- NT2X52AE, NT2X52AM-trunk module, 2-wire
- NT2X52AF, NT2X52AN-trunk module, 4-wire
- NT2X52AG, NT2X52AP-trunk module, 8-wire
- NT2X52AD, NT2X52AR-trunk module, 8-wire with access
- NT2X52CC-international trunk module, 8-wire with access

The 2-wire trunk module appears in the figure titled “NT0X46AB trunk model equipment frame parts” that illustrates the TME frame design.

The digital carrier equipment (DCE) frame stores digital carrier modules and digital echo suppressor modules. A standard DCE frame can mount four digital carrier module shelves. The frame can have two digital carrier module shelves and two trunk module or maintenance trunk module shelves.

NT0X46AB (continued)

Parts

The NT0X46AB has the following parts:

The trunk module equipment frame and the digital carrier equipment frame has the NT0X82AB frame supervisory panel (FSP).

Frame supervisory panel

The NT0X82AB FSP has power control and alarm circuits. These circuits provide interface between the power distribution center and the NT0X46AB frame. This FSP uses circuit breakers to protect the power control circuits. This FSP uses fuses to protect the alarm circuits.

Trunk module equipment frame

The trunk module equipment frame contains the parts described below.

Trunk module

A trunk module uses a single duplicated speech and messaging link to connect a maximum of 30 analog trunks to switching network ports. Thirty channels accommodate pulse code modulation signals. The system uses channel 0 for messaging. The system does not use channel 16.

The NT2X52AE represents the different trunk modules that the TME frame can use. The NT2X52AE trunk module contains a common control section and a maximum of 15 interchangeable trunk interface cards. Each trunk card has one or two trunk interface circuits. The interface circuits match the speech transmission characteristics and signaling methods of the trunk facility that connect to the trunk end.

Two pairs of common buses link the common control and trunk interface circuits in the trunk mode. The pair XPAM/RPAM carries pulse amplitude modulated analog speech samples. The pair XDAT/RDAT carries digital data. Both pairs of buses provide 30 two-way, time-division multiplexed transmission paths.

Maintenance trunk module

You must have the NT2X58CA maintenance trunk module to support the alarm cross-connect unit.

The maintenance trunk module accepts analog trunks, digital service circuits, or both. The maintenance trunk module processes the signals to a common pulse code modulation (PCM) format. The maintenance trunk module has four common control circuit cards. These circuit cards provide interface with duplicated transmit and receive paths to the digital switching networks. Each path carries a data stream that consists of 32 multiplexed PCM channels at a

rate of 2.56 Mbit/s. Different interchangeable trunk and service circuit cards provide interface between each channel and test trunks or service circuits. These cards can have the following features:

- analog or digital service circuits
- transmission test trunks to apply test conditions or diagnostic tests
- alarm detection or activation circuits
- signaling information circuits

For example, maintenance trunk modules can have dual-tone multifrequency receivers and transmission test circuits. Transmision test circuits perform frequency and level measurements associated with office and facility maintenance.

Alarm cross-connect unit (AXU)

The trunk module equipment frame includes the NT3X89AA alarm crosspoint field shelf. This shelf acts as part of an alarm system for a large office. Each office must have one AXU shelf. The AXU requires a primary alarm maintenance trunk module, like NT2X58CA, NT2X58AL, or NT2X58AT. The AXU and the primary alarm maintenance trunk module function as a pair. The AXU and the primary alarm maintenance trunk module must be on the same frame together. To limit cable congestion and reduce drop lengths, locate the AXU in position 65 and the maintenance trunk module in position 51. Position 65 has the secondary alarm maintenance trunk module. This module uses a different power feed from the primary alarm maintenance trunk module.

Digital carrier equipment frame

The digital carrier equipment frame has the following parts.

Digital carrier module

The digital carrier module (DCM) occupies one shelf. The DCM functions as the interface between the following:

- a maximum of five 24-channel, 1.544 Mbit/s DS-1 carrier systems
- a maximum of four 32-channel, 2.56 Mbit/s DS30 duplicated links (ports) of the DMS network

The DCM performs the basic functions to convert signals between DS-1 and DS30 formats. The DCM functions as an interface for the DS-1 A-bit/B-bit signaling method and the DS30 SD/scan method.

Three DCM configurations are available. The DCM-B version (NT2X31AJ) provides the basic interface functions. The DCM-S version (NT2X31AE) provides clock synchronization and the basic function. The DCM-R version

NT0X46AB (continued)

(NT2X31AF) functions as interface for a maximum of four DS-1 carrier systems and a remote line module link. The DCM-R version can provide interface for a maximum of five remote line module links. The DCM-R version can provide interface for any group of five DS-1 carrier systems and remote line module links. The operating company can equip the DCM-R version with clock synchronization circuits.

Subject to specified limits, the TME frame can have a digital carrier module or digital echo suppressor module.

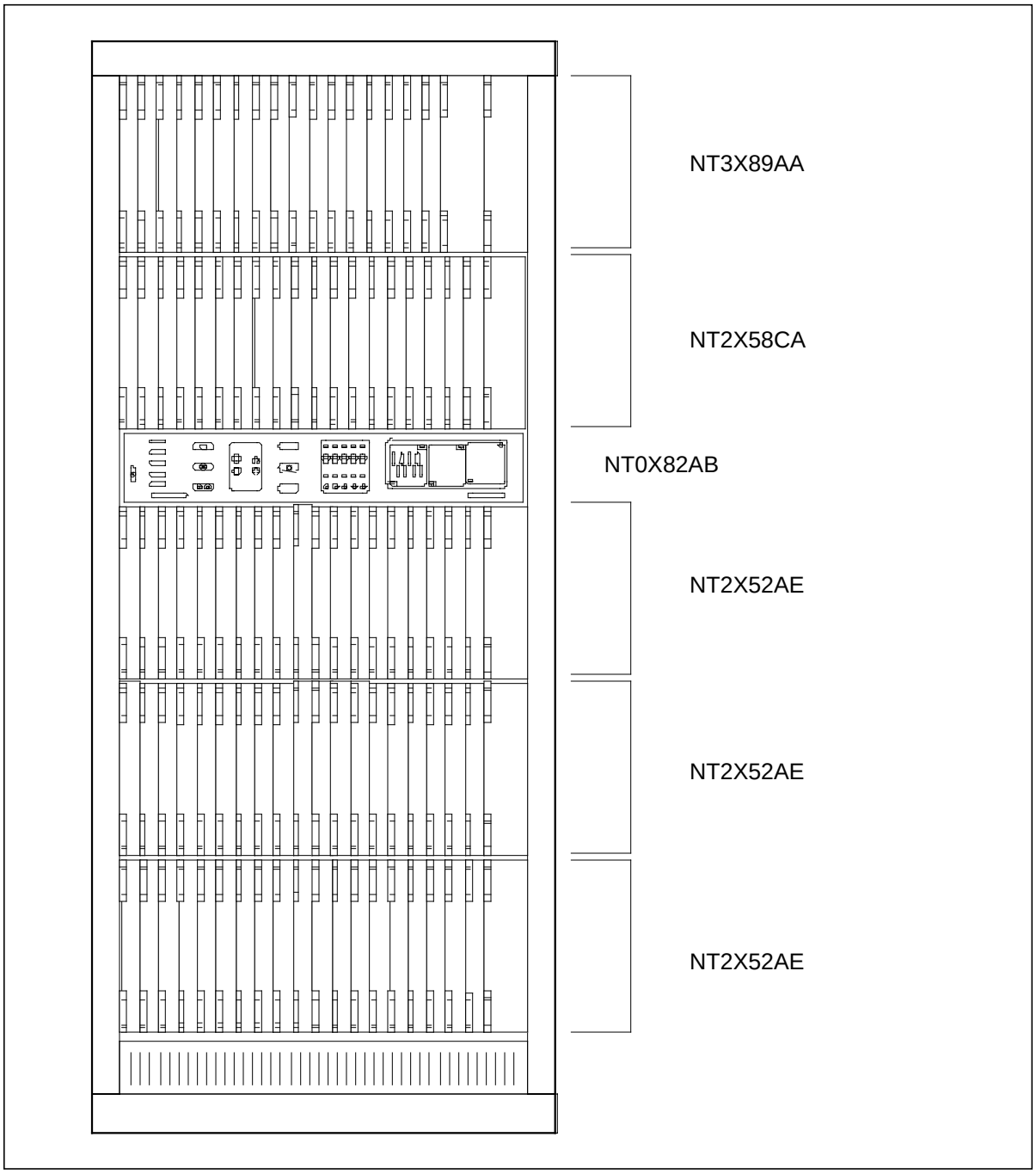
Digital echo suppressor

The digital echo suppressor (DES) is a digital carrier module DCM-B. Six DES service circuit cards replace five DS-1 line cards or the DES. You can operate the DES with vocal commands. The DES monitors speech signals on the transmit and receive paths between connected trunk circuits. The DES automatically applies signal attenuation to reduce echo effects on long distance trunks. The available DES modules are the NT2X12AA, NT2X12AB, and NT2X12AD.

Design

A possible design of the trunk module equipment frame appears in the following figure.

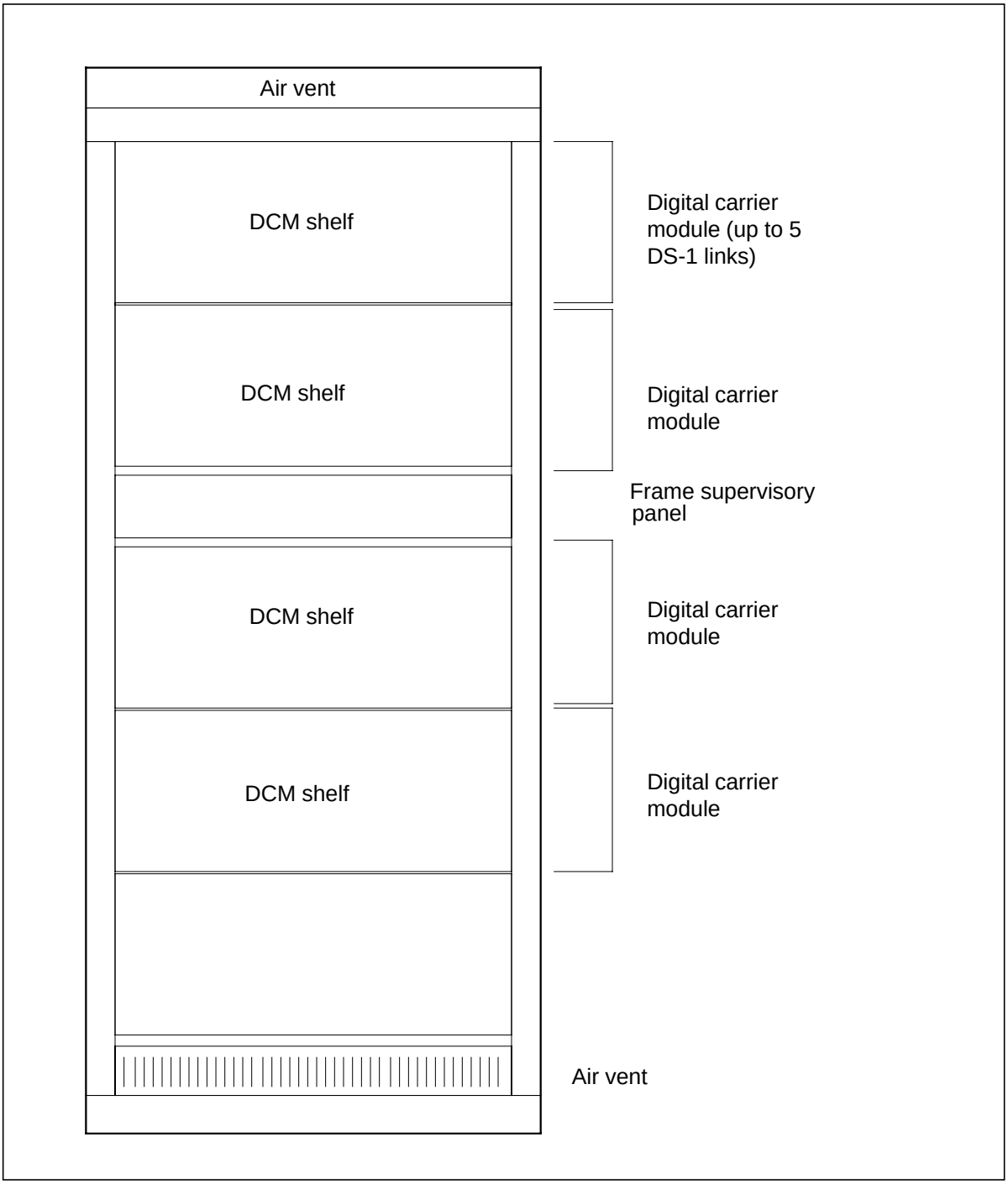
NT0X46AB trunk model equipment frame parts



A possible design of the digital carrier equipment frame appears in the next figure.

NT0X46AB (end)

Digital carrier equipment frame parts



Note: This diagram is not drawn to scale.

NT0X51AC

Product description

The NT0X51AC alarm card monitors and reports alarms for the cabinetized power distribution center (CPDC). This card operates with an input battery voltage of -48V or -60V.

The NT0X51AC comes with the NTMX26CE frame supervisory panel (FSP).

Functional description

The NT0X51AC alarm card performs the following primary functions:

- monitor and detect inverter failure
- monitor and detect electrically tripped circuit breakers
- monitor the alarm battery supply (ABS) line for loss of power

Functional blocks

The NT0X51AC has the following functional blocks:

- fault input lines
- alarm outputs
- alarm battery supply input line

Fault input lines

This block has four FFAIL inputs through pins one to four. High voltage diodes isolate pins 1 to 3. This isolation prevents the pins feedback from the other inputs. The diodes do not isolate pin 4 because the feedback lights the frame-fail lamp and the end-guard lamps. The lamps lights if an alarm condition occurs, except ABS failure. A voltage of -39V to -72V with a maximum current of 17 mA at one pin activates the alarm mode. Connect the battery return to pin 9 (L±). The system deactivates the alarm. The voltage must fall below -5V for the system to activate the alarm again.

Alarm outputs

This block has three electrically isolated output alarms. The alarms operate as follows:

- The system shorts the AISALM contacts when the system activates a minimum of one FFAIL input. The system shorts the AISALM contacts when the ABS line drops below -5V, or both.
- The system shorts the PDCALM contacts when the system activates a minimum of one FFAIL input.
- The system shorts the ABSALM contacts when the ABS line does not rise above -39V or drop below -5V.

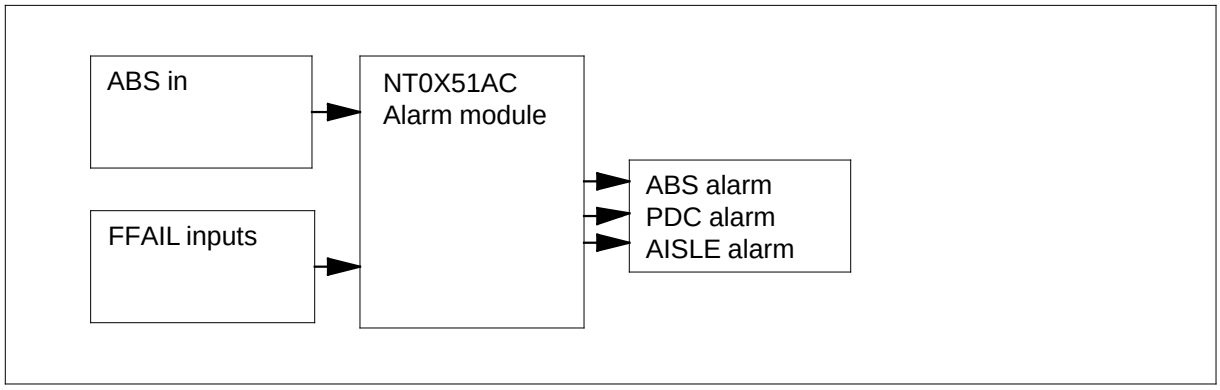
NT0X51AC (continued)

Alarm battery supply input line

This input line deactivates the alarm if the voltage at pin 12 (L-ABS1) is between -39V and -72V. Connect the battery return to pin 9 (L±). The system deactivates the alarm. The voltage must fall under -5V for the system to activate the alarm again.

The relationship between the functional blocks appears in the following figure.

NT0X51AC functional blocks



Signaling

Pin-outs

The following table lists the pin-outs for the NT0X51AC.

Connector J1

Pin	Signal	Pin	Signal
1	FEEDF1-2	7	PDCALM2
2	FEEDF1-2	8	PDCALM1
3	SPARE	9	BR
4	FEEDF2	10	ABSALM2
5	AISALM2	11	ABSALM1
6	AISALM1	12	-48V/-60V

Technical data

Power requirements

Input

The small input voltage for the NT0X51AC is -48V or -60V. A range from -39V to -75V is acceptable. The maximum input current is 17mA for each input line.

NT0X56

Product description

The speech link connector (SLC) frame provides an interface between the NT0X48 or NT5X13 network modules (NM) in the network frame (NET). The SLC frame provides an interface between the peripheral modules (PM) of the DMS-100 Family of digital switching systems.

The addition of connector panels and new patch cord connections can cause system growth. Current patch cord connections can require a new assignment during extensions. This growth depends on job conditions. Community of interest and feature characteristics of the growth terminals are examples of job conditions.

The SLC organizes cabling so that expansion of the DMS system can occur quickly and easily. Cabling procedures make sure that cable procedures do not have to occur during office growth and system change. The NM-to-speech link cabling is one directional for reduced cross-talk. The PM-to-SLC cabling is two directional for maximum hardware use.

The NT0X56 has the following primary use features:

- uses completed connectorized distribution frame with one-sided operation and two directional, polarized patch cords to provide maximum hardware use
- allows transfer of traffic to a new NM during system growth
- allows assignment of PM speech link ports to network ports
- provides control of system configuration
- simplifies trunk and line assignment procedures without network assignments
- uses cable sizes correctly: 16 pairs from the NM, ten pairs from the PM

Parts

The NT0X56 has PSL and NSL connector panels, NSL and PSL speech link ports, and patch cords.

PSL and NSL connector panels

A speech link connector frame has two groups of connector panels. The first group contains Network-to-SLC panels (NSL). The second group contains SLC-to-PM panels (PSL).

A standard DMS-100 frame contains NSL and PSL panels mounted in a horizontal position. The panels alternate to minimize the length of the patch

cords. In small DMS-100 Family systems, a single frame can have both planes of a duplicated network. A full-size DMS-100 require a maximum of four frames of panels for each plane.

NSL speech link ports

The 64 speech link ports (0 to 63) from each NM appear on each NSL jack panel. The 64 speech link ports appear as 16 groups of four ports each.

PSL speech link ports

On each PSL, the speech link ports appear in a horizontal position in 16 groups of five ports. The PMs have trunk modules (TM), line modules (LM), or digital carrier modules (DCM). Each group of five ports interfaces with the same number of ports on any PM.

Patch cords

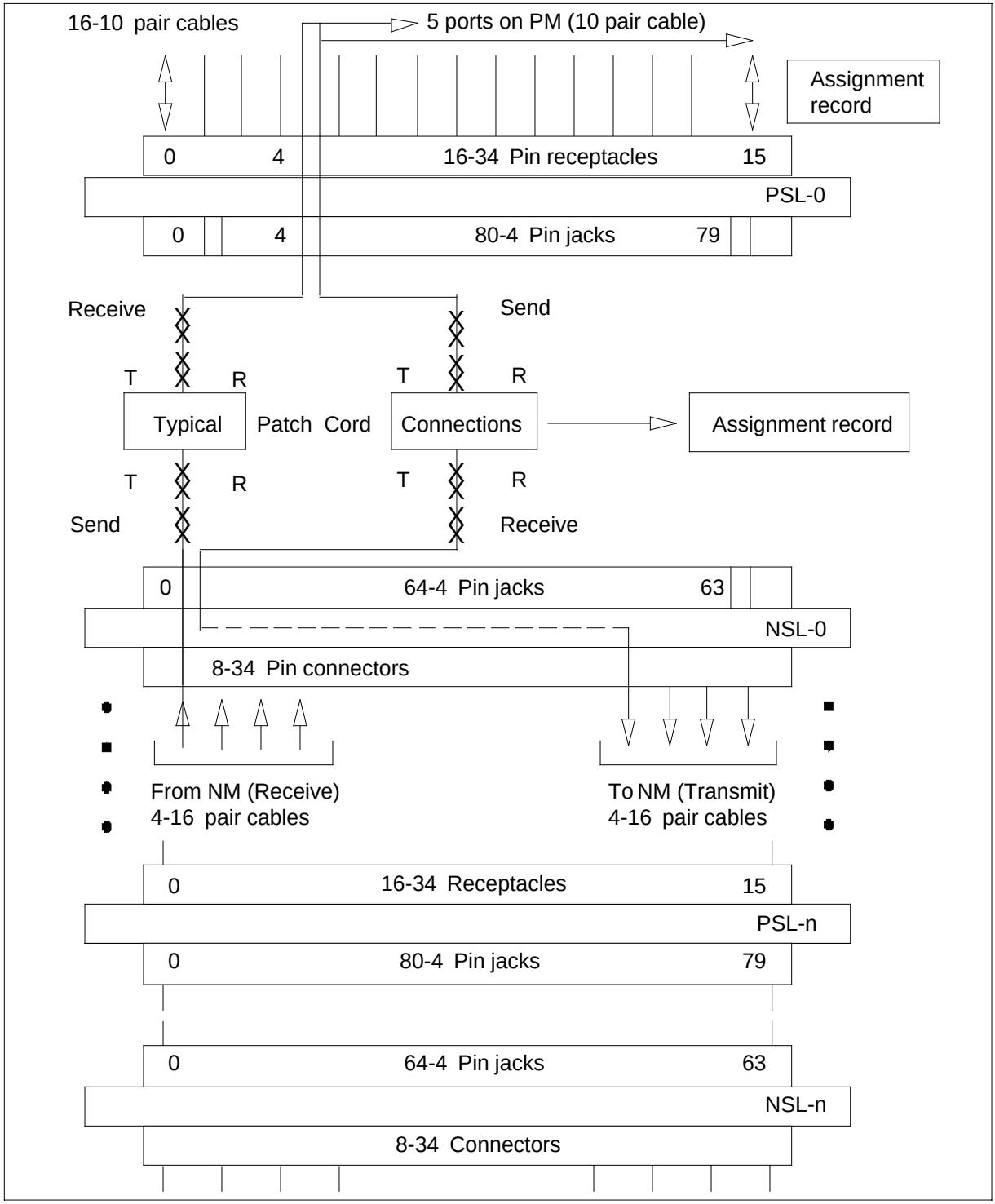
Connectorized, four-wire patch cords connect a normal port (0) on the NSL panel to a port (four) on the PSL-0 panel. Nortel Networks uses these patch cords to engineer the pattern of interconnection to meet system configuration requirements. Patch cords have different lengths and types.

Design

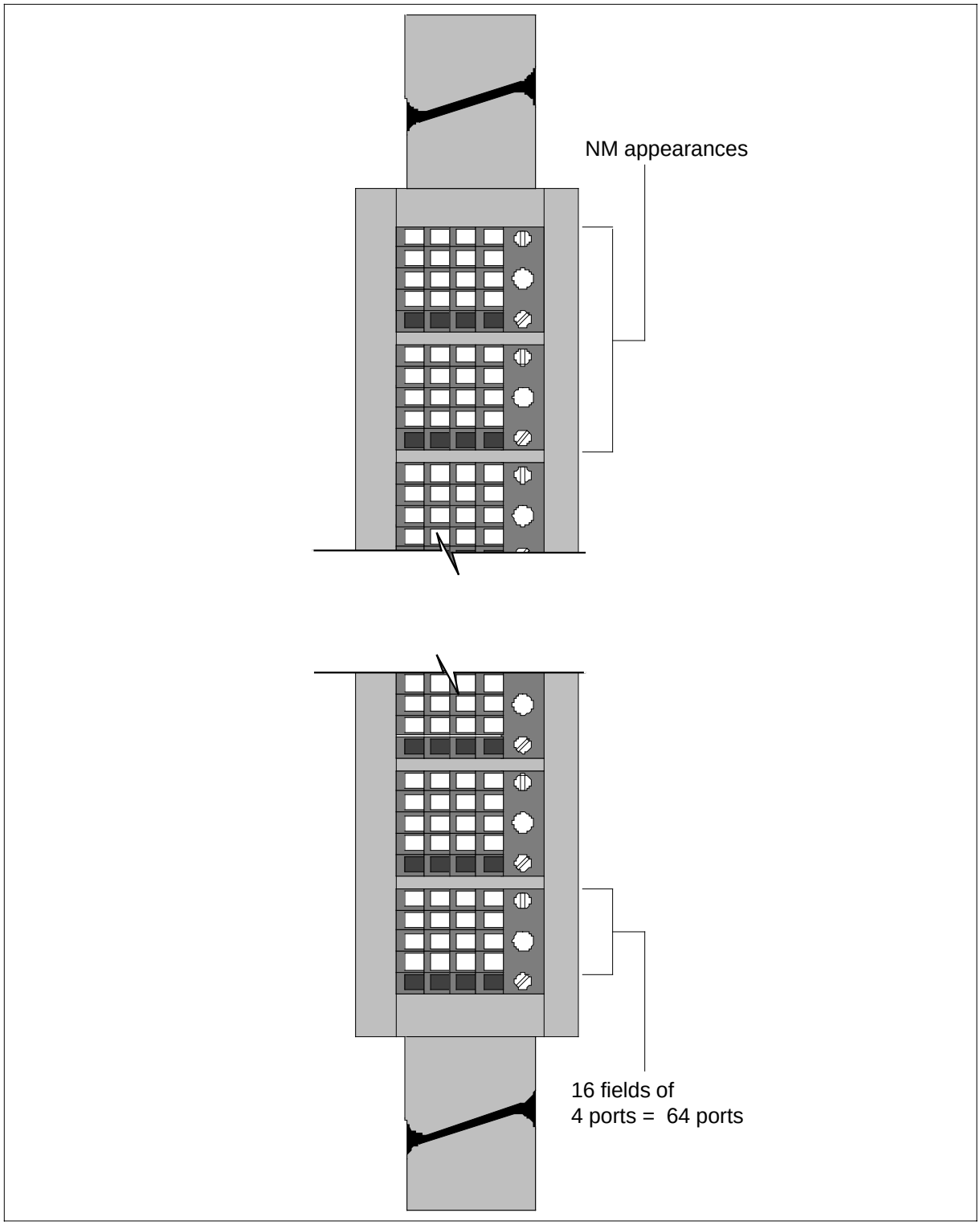
The design of the NT0X56 appears in the following example.

NT0X56 (continued)

NT0X56 parts of the speech link connecting frame

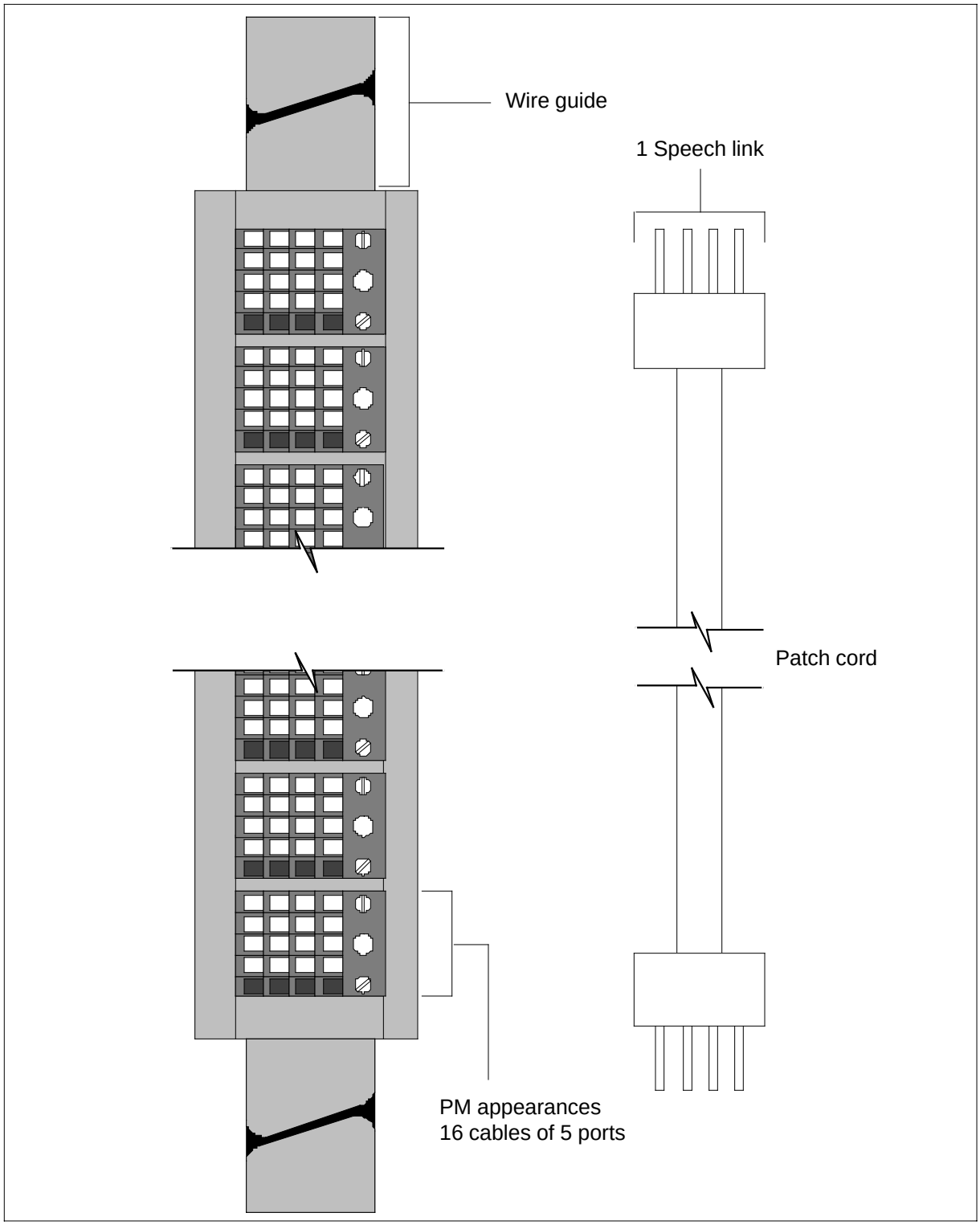


NT0X56 front view of NSL panel

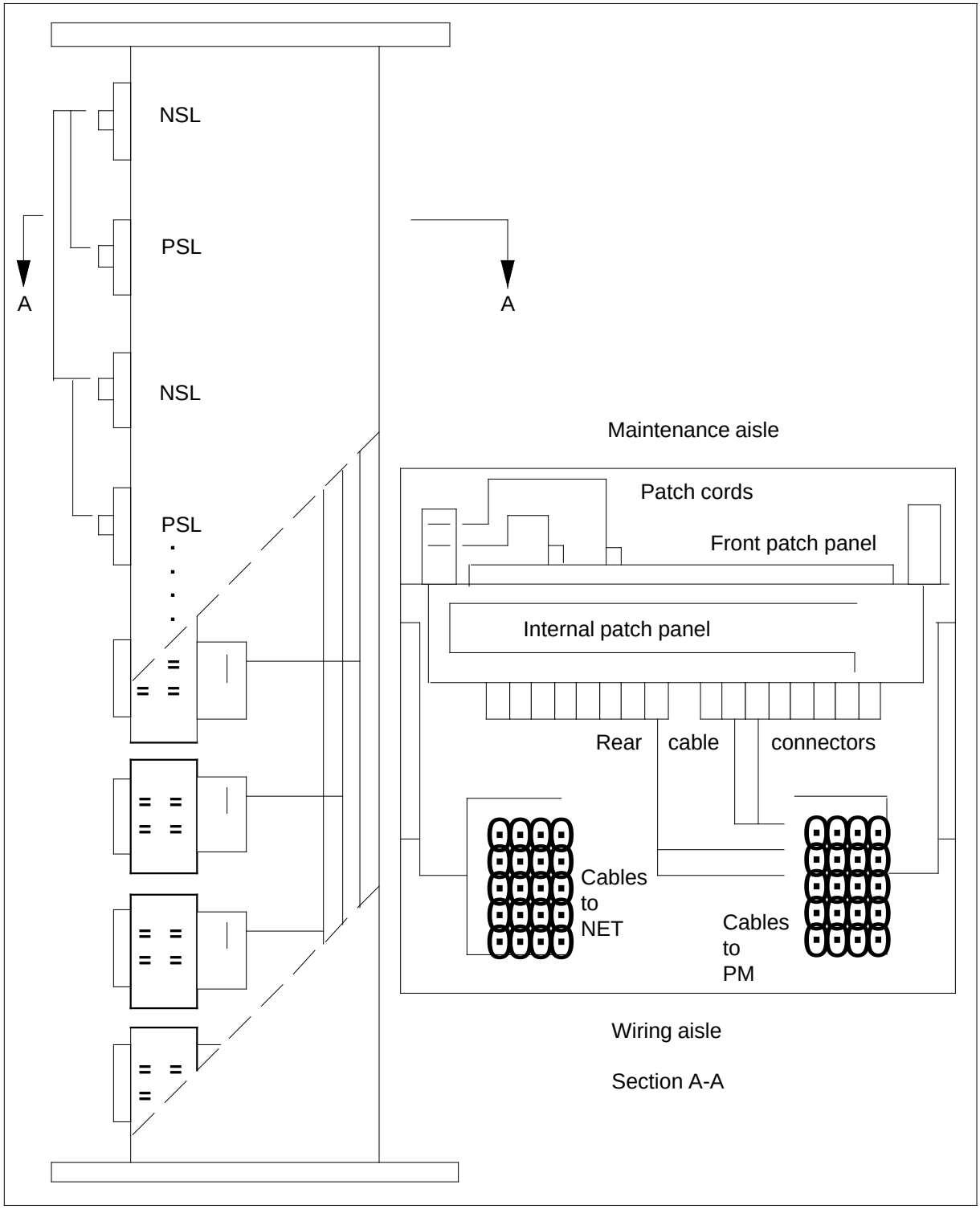


NT0X56 (continued)

NT0X56 front view of PSL panel and patch cord



NT0X56 typical SLC frame, side view



NT0X56 (continued)

Technical data

The technical data section provides specifications for the NT5X92 power requirements, equipment dimensions, and environmental conditions.

Power requirements

The SLC acts as a distribution frame. The SLC does not require an electrical supply. The following paragraph describes the electrical order of the cables and patch cords used as connections in the SLC.

NSL panel

The system routes receive and transmit speech links through separate 16-pair cables, four receive and four transmit. This process appears in a diagram in figure titled “NT0X56 front view of NSL panel.” At a normal port (0), both directions of transmission merge. Each port appearance carries two-way transmission.

The NSL panel uses eight 34-pin, panel-mounted connectors to receive cables from NET. The NSL panel uses 64-pin, bifurcated, cantilevered, female groups for four-pin male patch cords.

PSL to PM

A normal port (four) accepts two-way transmission paths through the patch cords from the NSL panel. The transmission paths from the PSL panel to the PM appear in groups of five ports. Each group of five ports connects to ten-pair, two directional cables. A single cable sheath has the receive and transmit paths. The cable routes to the designated PM frame or shelf. Maintain assignment records of the PM connection.

The PSL panel uses 16 34-pin, panel-mounted connectors to receive cables from the PM. The PSL panel uses 80 four-pin, bifurcated, female groups for four-pin male patch cords.

Patch cords

The patch cords have two twisted pairs. The patch cords connect with both directions of transmission at the same time. A signal indicator change from transmit pair to receive pair and from receive pair to transmit pair occurs in the patch cord. Maintain assignment records of the patch cords. The patch cord plugs are four-pin, polarized connectors. The plugs mate with the female

sockets on the NSL and PSL panel jackfields. Select patch cords from the types and lengths that appear in the following table.

Patch cords

NSL panel	PSL panel	Part no. range	Length range	No. types
NT0X56AB	NTX056AC	A0265763 to A0265822	0.15m (6 in.) to 9.14m (30 ft)	60
NT0X56AB or NT0X56BB	NT0X56BC or NT0X56AC	A0289630 to A0269640	0.61m (2 ft) to 9.14m (30 ft)	11
NT0X56BB	NT0X56BC	A0289611 to A0289621	0.61m (2 ft) to 9.14m (30 ft)	11

Equipment dimensions

The SLC frame dimensions are 2134 mm (84 in.) in height, 457 mm (18 in.) in depth, and 686 mm (27 in.) in width.

The NSL and PSL panel dimensions are 89 mm (3.5 inches) in height, 203 mm (8 in.) in depth, 660 mm (26 in.) in width, and 4.5 kg (10 lb) in weight.

Environmental conditions

The NT2X43 performs under limited environmental controls. An example of this process appears in the following table.

Environmental conditions

Condition	Operating range	Short-term range
Temperature	10°C to 30°C	5°C to 49°C
	50°F to 86°F	41°F to 120.2°
Relative humidity	20% to 55%	20% to 80%

Note: A normal humidity of 80% is expected for an ambient temperature of 21°C (69.8°F) maximum. At an ambient temperature of 49°C (120.2°F), a normal humidity of 30% maximum is expected.

NT0X57

Product description

The MAP terminal provides a man-machine interface (MMI) between operating company personnel and the DMS-100 Family of Digital Multiplex Switching (DMS) systems. Use the MAP controls and displays to start the maintenance, tests, and administration functions.

The MAP terminal has the following primary use functions:

- provides a functional configuration for tasks that requires you to sit and stand
- uses a drop surface for the terminal keyboard to promote correct arm and hand positions. Uses a drop surface to minimize operator fatigue
- provides both hands-free and handset operation. Provides automatic dialing of a maximum of 31 numbers on the Logic telephone set
- uses a plug-ended assembly for the MAP terminal to make transfer easy
- prints or stores data that appears on the visual display unit (VDU) for hard-copy and log purposes.
- interfaces through the system software to provide screen displays for the tasks performed from the position
- displays general system state until you use programmed function keys to request additional detailed information
- include a jack panel on the position. The panel is for direct access to system test trunks when you use portable test equipment at the position
- provides storage for user documentation

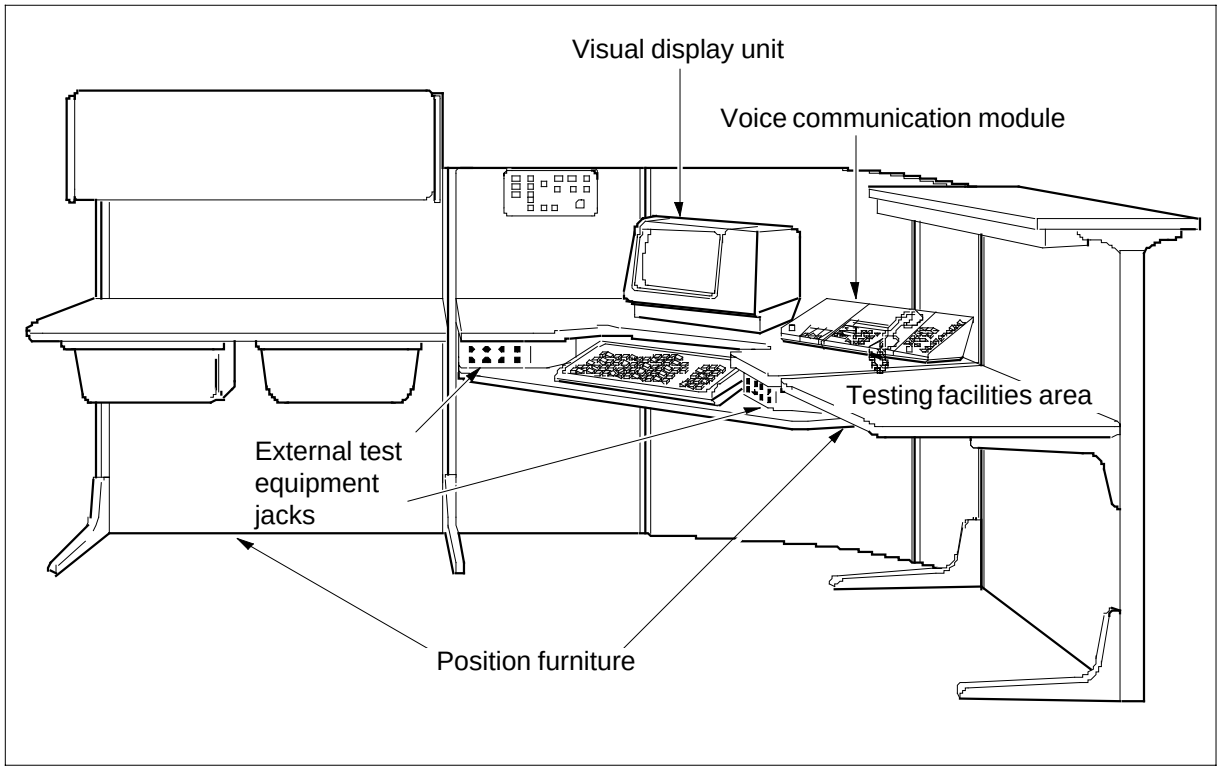
Location

A MAP terminal location is flexible. The MAP terminal location requires 110V (ac) power and telephone (voice and data) interfaces to the DMS system.

Functional description

The MAP terminal is a MMI that has four basic components. The components include a VDU, a voice communication module, test facilities, and position furniture. Examples of these components appear in the following figure.

NT0X57 maintenance and administration position



Visual display unit

The VDU is the major MMI to the DMS system. Operator entries to the system occur through the VDU keyboard. The interface between the VDU and DMS system occurs through a device controller (DC) and the DMS input/output controller (IOC).

The VDU provides all visual displays, like alarm indications and test results. The basic maintenance system output consists of a short state display that describes the alarm conditions in each maintenance subsystem. The system state display appears in the top three lines of the VDU screen. The first line contains maintenance subsystem headers. The second line has subsystem state indications. The third line has alarm state indications. You can operate correct keys on the MAP keyboard for additional information.

Voice communication module

The voice communication module provides the operator with all standard telephone links in and out of the office. The type and number of communication links depends on the office. The Logic series type of terminal acts as the basis of the communication module. The Logic series type of

NT0X57 (continued)

terminal provides handset, headset, or loudspeaking (hands-free) modes of operation for each line. The Logic telephone set has the following features:

- a Digitone dial
- nine (Logic 10) or 19 (Logic 20) line buttons or optional features buttons
- a hold button
- a headset selector switch

The automatic dial can store a maximum of 31 numbers. Use a single key to label and dial these numbers.

Test facilities

The voice communication module provides small signal ac access to the test trunks. Three double jacks provide direct links. These double jacks are mounted on the side of the table surface. The jacks provide direct links from the portable test equipment to the test trunks.

Position furniture

The position furniture is a module system that provides 1.8 square m (20 square feet) of table surface. You can position the table surface for use when you stand or sit. You can subdivide the furniture into three units. These three units include the corner terminal space, the storage unit, and the counter unit. The storage unit has drawers and shelves. You can order each unit separately or together to begin different configurations. You can order separate shelves for the storage unit.

Open or closed shelves above or below, or above and below, the work surface provide document storage space. A counter over one work surface provides a work area for the operator and other personnel that interact with you. The counter provides additional shelf space. The terminal platform that sits on the corner table surface minimizes the sliding friction of the terminal. This position allows you to adjust viewing distance and position easily. Place the VDU keyboard on a dropped surface. You can remove or adjust the keyboard. Optional built-in lighting lights the work surface.

Technical data

This section describes the technical requirements for the following features:

- maintenance trunk module (MTM) interface
- local talk line interface
- communication lines interface

- DC
- communication module

This following section describes power requirements and required environmental controls.

Maintenance trunk module interface

The MTM interface includes jack-ended trunks, 101 test lines (toll only), and communication trunks (toll only). Each position for trunk tests and general maintenance functions has three jack-ended trunks. For jack-ended trunks, the jack field on the MAP terminal connects trunks to a four-wire trunk circuit (NT2X88AA). The NT2X88AA connects through the main distribution frame (MDF).

The 101 test lines that appear on the Logic telephone set multiply to every MAP terminal used for trunk tests. These trunk tests use communication trunk circuits (NT2X67AA). The number of 101 test lines in an office depends on the needs of the operating company.

The Logic telephone set terminates the communication trunks (toll only) used for trunk tests at the MAP terminals. Operating company personnel use the trunks to start calls. Two trunks associate with each MAP terminal used for trunk test functions.

Local talk line interface

The talk line associated with the telephone jacks on the frame supervisory panel (FSP) arrives at the MAP terminal. The talk line terminates on the Logic telephone set.

Communication lines interface

Use A key telephone system to terminate tie lines and normal office telephone lines at the Logic telephone set.

Device controller

The distance between the DC and the MAP terminal determines the type of interface between the VDU and the DC. The DC (multiterminal NT1X67AA)

NT0X57 (continued)

provides four two-directional interfaces with the following programmable characteristics:

- For MAP terminals at maximum of 15 m (150 ft.), the system uses a standard Electronic Industry Association (EIA) RS-232 interface.
- For MAP terminals at a maximum of 360 m (1200 ft.), the system uses a loop current interface.
- For remote MAP terminals, the distance exceeds 360 m (1200 ft.), the system can use standard data sets. These data sets operate at 300 b/s or 1200 b/s.

Video display unit

The VDU must have the following characteristics:

- For general maintenance and trunk test functions, the terminal must operate at a minimum of 1200 b/s. All other positions, like remote, service analysis, can operate at a minimum of 300 b/s.
- The screen dimensions must be 80 characters by 24 lines.
- The keyboard requirements include the following:
  - — a basic QWERTY keyboard
  - — a cursor that operating company personnel can address
  - — protect and not protected mode or erase from cursor position to the end of the line
  - — a keyboard that you can remove
- The communication interface requirements include EIA and current loop.

Recommended features include:

- a number cluster
- upper and lower case characters
- a slave printer interface with an associated function key

Recommended display highlighting features include:

- inverse video
- multilevel video
- blinking video
- underline

Voice communication module

The voice communication system of the MAP terminal depends on Logic 10 or Logic 20 key telephone set. Components associated with the Logic telephone set series include the following:

- QDM3A1 Logic Dialler
- QUS1C Logic Hands-Fee Unit
- Venture 1 Headset or an equivalent headset

Power requirements

The power requirements for the NT0X57 appear in the following table.

Power requirements

Component	Requirements
VDU	The maximum VDU power drain allowed is 200 watts. When the MAP terminal functions for general maintenance functions, the MAP terminal must run on an required ac supply. Each necessary position requires a DMS inverter mounted on a frame. The power drain of the MAP terminal and necessary light must be a minimum of 200 watts for each inverter.
Voice communication module	The voice communication module requires a non-essential ac source that uses an NE2012B transformer or equivalent power supply. The hands-free unit and the autodial unit use this ac power.
Light	The light features on the MAP terminal must appear on a necessary ac supply. The light must appear when that light is the light source in the work area. The light power requirement is 60 watts.

NT0X57 (end)

Environmental controls

The MAP terminal functions under environmental controls appear in the following table.

Ambient conditions

Duration	Operating range	Short-term range
Temperature	10°C to 30°C (50°F to 86°F)	5°C to 49°C (41°F to 120.2°F)
Relative humidity	20% to 55%	20% to 80%

NT0X63LA

Product description

The NT0X63LA alarm control and display (ACD) panel is a modular, low power peripheral alarm device. The NT0X63LA is part of the DMS-100 Family Low Power Alarm (LPA) system. The NT0X63LA provides function switches (for example, audible alarm disable), visual alarm indications, and the relays to support these alarm functions.

The NT0X63LA replaces the following units: NT0X63AA, NT0X63AC, NT0X63AD, NT0X63AE, NT0X63AF, and NT0X63KA.

You can combine the NT0X63LA with the following (older alarm system) products: NT0X63AA, NT0X63AB, NT0X63AC, NT0X63AD, NT0X63AE, NT0X63AF, and NT0X63KA.

Functions

The NT0X63LA panel provides the following functions:

- visual indication of DMS and non-DMS alarm conditions
- data loop function control switches
- alarm function switches
- piezo-electric buzzer for the common audible (CA) alarm

Panel controls and indicators

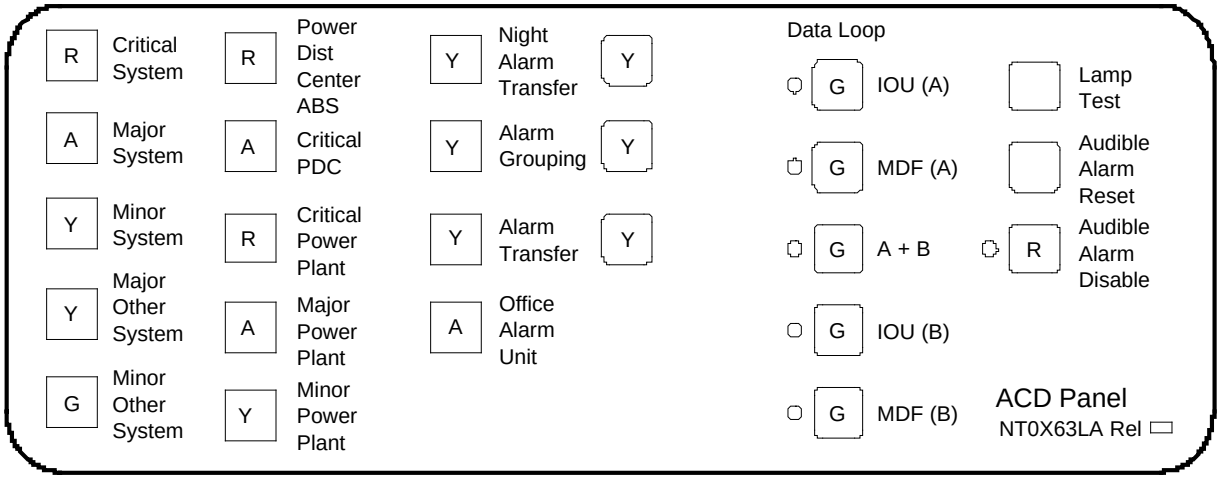
The NT0X63LA panel contains the following:

- eleven light emitting diode (LED) alarm indicators for DMS and non-DMS alarm conditions
- function switches and LED indicators for the following:
  - — night alarm transfer
  - — alarm grouping
  - — alarm transfer
- lamp test, audible alarm reset, and audible alarm disable switches
- data loop function control switches

The following illustration shows a front view of the NT0X63LA alarm control and display panel.

NT0X63LA (continued)

LP alarm control and display panel

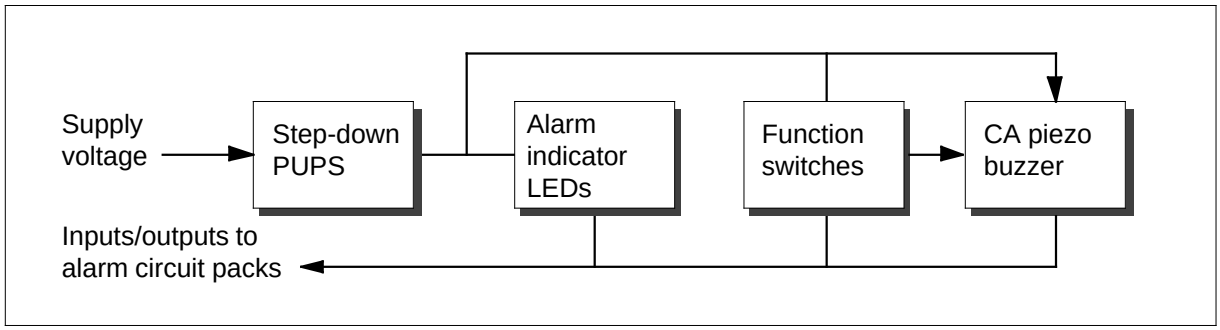


Legend: Lamp A = amber
Lamp G = green
Lamp R = red
Lamp Y = yellow

Functional blocks

This section provides an illustration and descriptions of the main functional blocks of the NT0X63LA panel.

NT0X63LA functional blocks



PUPS

The point-of-use power supply (PUPS) converts the alarm battery supply (ABS) voltage to a filtered 5V supply for the other circuits on the panel. The 5V supply provides the following:

- isolated system grounding (ISG) for the internal logic circuits
- reduced power requirement for the panel
- common panel design for North American and international offices

LEDs

There are 14 high-brightness LED arrays for visual indication of individual alarm conditions. There are six other LEDs that indicate operation of the locking touch pad switches. Illumination of an LED indicates an active circuit or the existance of an alarm condition.

Piezo buzzer

The piezo buzzer is a standard piezo-electric device that activates to alert personnel of an alarm condition. The buzzer sounds until one of the following occurs:

- the alarm condition does not exist
- you operate the alarm reset switch
- you enter the SIL command at the MAP terminal
- you operate the audible alarm disable switch

Function switches

The NT0X63LA contains carbon pad switches for the following functions:

- night alarm transfer
- alarm grouping
- alarm transfer
- data loop control (DLC)
  - — odd-numbered aisles DLC circuit
  - — even-numbered aisles DLC circuit
  - — combination switch (A + B)
  - — MDF (A) connection DLC circuit
  - — MDF (B) connection DLC circuit
- lamp test

NT0X63LA (continued)

- audible alarm disable
- audible alarm reset

A green LED beside each data loop control switch lights when you operate the switch.

The audible disable switch deactivates only the CA buzzer on the NT0X63LA. A red LED beside the switch lights when you operate the switch.

The lamp test switch activates control circuits (OAU cards) and DMS alarm software to verify that the LEDs and the alarm circuits that light the LEDs function.

Pin descriptions

The following table contains pin descriptions for the NT0X63LA panel.

Interface connectors (C00/C01) pinouts (Sheet 1 of 2)

Pin number	Signal label	Description
1	FGND	frame ground
2	BR(1)	battery return (1) / GRD (1)
3	-48SP	ABS (SP): -48V or -60V
4	Spare	no connect
5	CA	common audible alarm (ACD buzzer)
6	AAR	audible alarm reset switch
7	BIOC	data loop - even aisles
8	A+B	odd + even data loop combination switch
9	AIOC	data loop - odd aisles
10	AR	alarm transfer signal
11	AT	alarm transfer LED
12	TTC	night alarm transfer switch
13	PDC	critical power distribution center failure LED
14	MJPP	major power plant LED

Interface connectors (C00/C01) pinouts (Sheet 2 of 2)

Pin number	Signal label	Description
15	OAU	OAU shelf failure LED
16	MNOS	minor other system (non-DMS) LED
17	MNS	minor DMS failure LED
18	CRS	critical DMS failure LED
19	Spare	no connect
20	BR(2)	battery return (2)/GRD(2)
21	-48V(2)	ABS (2): -48V or -60V
22	-48V(1)	ABS (1): -48V or -60V
23	Spare	no connect
24	AD	alarm disable signal
25	Spare	no connect
26	BMDF	data loop - MDF (B)
27	AMDF	data loop - MDF (A)
28	RAR	alarm transfer switch (TTC chime also rings)
29	TA	alarm transfer signal
30	AG	alarm grouping switch
31	LT	lamp test switch
32	MNPP	minor power plant LED
33	CRPP	critical power plant LED
34	ABS	power distribution center ABS failure LED
35	MJOS	major other system (non-DMS) LED
36	MJS	major DMS failure LED
37	Spare	no connect

NT0X63LA (end)

Power requirements

The maximum power requirement for the NT0X63LA is 10.7 watts. The total power dissipation for the panel is 1.6 watts or 5.44 BTU.

To calculate the maximum cable length for panels multipled on the same link, use the following equation.

Note: For installations with -48V, the resultant number cannot exceed six. For installations with -60V, the resultant number cannot exceed 15.

maximum cable length = V_{DROP}^{max} / (AWG_{RES} X .25A)

where

V_{DROP}^{max}
is the maximum voltage drop; 6Vdc (domestic) or 15Vdc (international)

AWG_{RES}
is the resistance; 0.02567 ohms per foot or 0.0842 ohms per meter

The following table lists power requirements for the NT0x63LA.

Item	Minimum	Nominal	Maximum	Comments
A/B battery feed	-42.75V	-48.0V	-55.8V	-48V offices - domestic
A/B battery feed	-52.0V	-60.0V	-72V	-60V offices - international
supply noise		500 mV		
Supply current	190mA	30mA	250 mA	
Panel operation	36V dc		75V dc	
Panel current draw	80mA		2515mA	at 5V dc

A resettable fuse will open if there is an electrical short circuit. To restore operation to the panel, disconnect the C00 cable for 30 seconds. If the panel does not return to service, contact your next level of support.

NT0X63LB

Product description

The NT0X63LB alarm display (AD) panel is a modular, low power peripheral alarm device. The NT0X63LB is part of the DMS-100 Family Low Power Alarm (LPA) system. The NT0X63LB provides an audible alarm reset switch, visual alarm indications, and the relays to support these alarm functions.

The NT0X63LB replaces the NT0X63AB AD panel. You can combine the NT0X63LB with the following (older alarm system) products: NT0X63AA, NT0X63AB, NT0X63AC, NT0X63AD, NT0X63AE, NT0X63AF, and NT0X63KA.

Functions

The NT0X63LB panel provides the following functions:

- visual indication of DMS and non-DMS alarm conditions
- data loop function control switches
- audible alarm reset

Panel controls and indicators

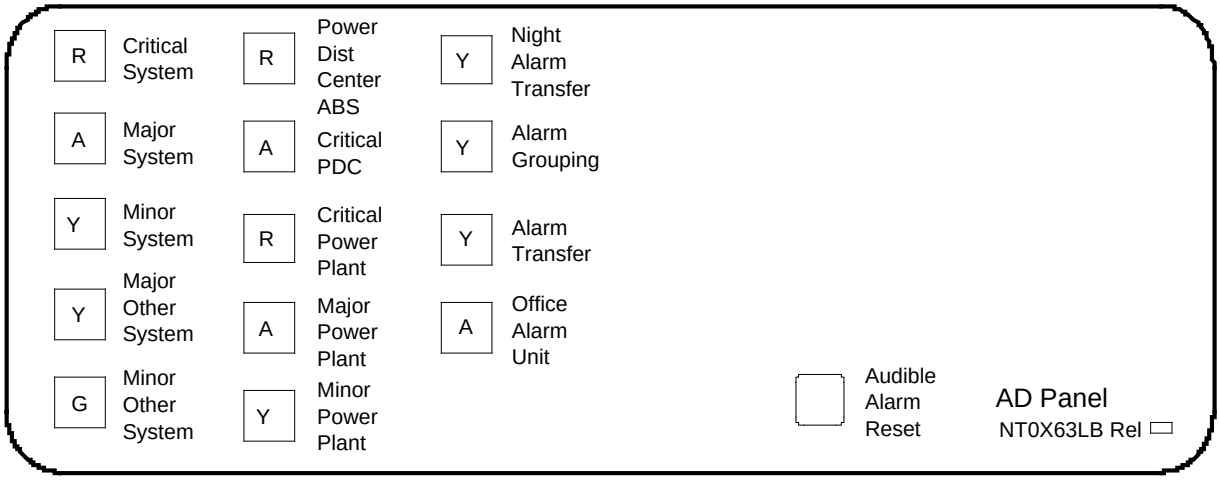
The NT0X63LB panel contains the following:

- eleven light emitting diode (LED) alarm indicators for DMS and non-DMS alarm conditions
- LED indicators for the following:
  - — night alarm transfer
  - — alarm grouping
  - — alarm transfer
- audible alarm reset switch

The following illustration shows a front view of the NT0X63LB alarm display panel.

NT0X63LB (continued)

LP alarm display panel

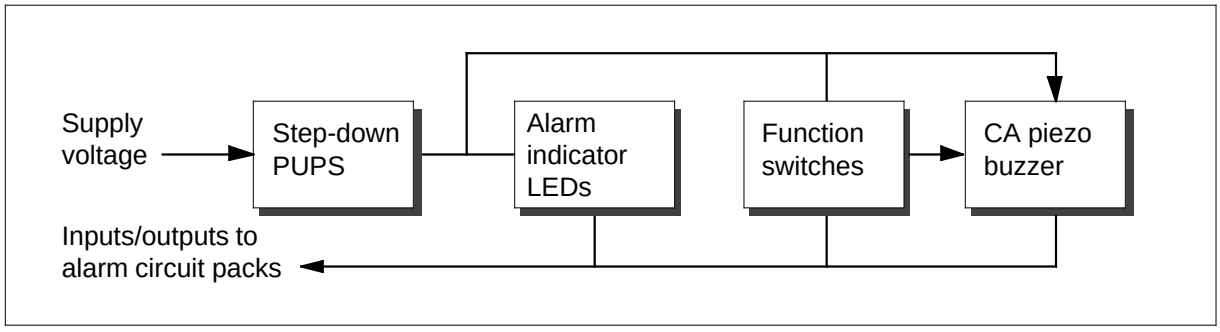


Legend: Lamp A = amber
Lamp G = green
Lamp R = red
Lamp Y = yellow

Functional blocks

This section provides an illustration and descriptions of the main functional blocks of the NT0X63LB panel.

NT0X63LB functional blocks



PUPS

The point-of-use power supply (PUPS) converts the alarm battery supply (ABS) voltage to a filtered 5V supply for the other circuits on the panel. The 5V supply provides the following:

- isolated system grounding (ISG) for the internal logic circuits
- reduced power requirement for the panel
- common panel design for North American and international offices

LEDs

There are 14 high-brightness LED arrays for visual indication of individual alarm conditions. Illumination of an LED indicates an active circuit or the existance of an alarm condition.

Piezo buzzer

The piezo buzzer and the related AD switch circuit are present on the NT0X63LB, but are not used.

Function switches

The NT0X63LB contains a carbon pad switch for the audible alarm reset function.

Pin descriptions

The following table contains pin descriptions for the NT0X63LB panel.

Interface connectors (C00/C01) pinouts (Sheet 1 of 3)

Pin number	Signal label	Description
1	FGND	frame ground
2	BR(1)	battery return (1) / GRD (1)
3	-48SP	ABS (SP): -48V or -60V
4	Spare	no connect
5	CA	common audible alarm (ACD buzzer)
6	AAR	audible alarm reset switch
7	BIOC	data loop - even aisles
8	A+B	odd + even data loop combination switch
9	AIOC	data loop - odd aisles

NT0X63LB (continued)

Interface connectors (C00/C01) pinouts (Sheet 2 of 3)

Pin number	Signal label	Description
10	AR	alarm transfer signal
11	AT	alarm transfer LED
12	TTC	night alarm transfer switch
13	PDC	critical power distribution center failure LED
14	MJPP	major power plant LED
15	OAU	OAU shelf failure LED
16	MNOS	minor other system (non-DMS) LED
17	MNS	minor DMS failure LED
18	CRS	critical DMS failure LED
19	Spare	no connect
20	BR(2)	battery return (2)/GRD(2)
21	-48V(2)	ABS (2): -48V or -60V
22	-48V(1)	ABS (1): -48V or -60V
23	Spare	no connect
24	AD	alarm disable signal
25	Spare	no connect
26	BMDF	data loop - MDF (B)
27	AMDF	data loop - MDF (A)
28	RAR	alarm transfer switch (TTC chime also rings)
29	TA	alarm transfer signal
30	AG	alarm grouping switch
31	LT	lamp test switch
32	MNPP	minor power plant LED
33	CRPP	critical power plant LED

Interface connectors (C00/C01) pinouts (Sheet 3 of 3)

Pin number	Signal label	Description
34	ABS	power distribution center ABS failure LED
35	MJOS	major other system (non-DMS) LED
36	MJS	major DMS failure LED
37	Spare	no connect

Power requirements

The maximum power requirement for the is 10.7 watts. The total power dissipation for the panel is 1.6 watts or 5.44 BTU.

To calculate the maximum cable length for panels multipled on the same link, use the following equation.

Note: For installations with -48V, the resultant number cannot exceed six. For installations with -60V, the resultant number cannot exceed 15.

maximum cable length = V_{DROP}^{max} / (AWG_{RES} X .25A)

where

V_{DROP}^{max}
is the maximum voltage drop; 6Vdc (domestic) or 15Vdc(international)

AWG_{RES}
is the resistance; 0.02567 ohms per foot or 0.0842ohms per meter

The following table lists power requirements for the NT0X63LB.

(Sheet 1 of 2)

Item	Minimum	Nominal	Maximum	Comments
A/B battery feed	-42.75V	-48.0V	-55.8V	-48V offices - domestic
A/B battery feed	-52.0V	-60.0V	-72V	-60V offices - international
supply noise		500 mV		
Supply current	190mA	30mA	250 mA	

NT0X63LB (end)

(Sheet 2 of 2)

Item	Minimum	Nominal	Maximum	Comments
Panel operation	36V dc		75V dc	
Panel current draw	80mA		2515mA	at 5V dc

A resettable fuse will open if there is an electrical short circuit. To restore operation to the panel, disconnect the C00 cable for 30 seconds. If the panel does not return to service, contact your next level of support.

NT0X63MA

Product description

The NT0X63MA central alarm display (CAD) panel is a modular, low power peripheral alarm device. The NT0X63MA is part of the DMS-100 Family Low Power Alarm (LPA) system. The NT0X63MA provides function switches (for example, night alarm transfer switch), visual alarm indications, and the relays to support these alarm functions.

The NT0X63MA replaces the NT0X64AA and NT0X64AB exit alarm panels, and the NT5X72AA and NT5X72AB central alarm panels. The fuse alarm function on the NT5X72AA is not included because the NT0X63MA has a resettable fuse device to protect its circuits from overloads. However, a relay circuit such as the signal FA-ALM alarm is included. This relay circuit can be datafilled as an SD point to indicate if the panel fails. If this alarm is used, Nortel Networks recommends to datafill the alarm as a minor other system type alarm.

You can combine the NT0X63MA with the following (older alarm system) products: NT0X64AA, NT0X64AB, NTRX64AA, NT5X72AA, and NT5X72AB.

Functions

The NT0X63MA CAD panel provides the following functions:

- routes alarm signals from customer-configured cross-connected locations to one of 15 LED alarm indicators
- silences the audible alarm piezo buzzer or disables the buzzer on the panel (on NT5X72AA/AB)
- visually indicates audible alarm deactivation
- visually indicates trunk test center (TTC) and power plant alarm conditions
- activates or deactivates the night alarm transfer (NAT) and alarm grouping (AG) functions
- visually indicates activation of night alarm transfer and alarm grouping functions

NT0X63MA (continued)

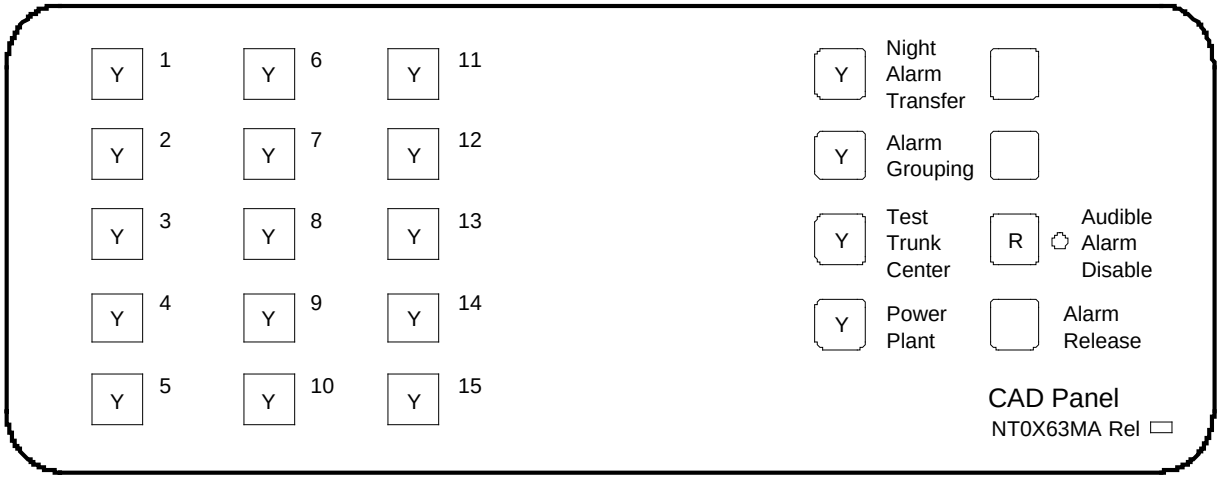
Panel controls and indicators

The NT0X63MA contains the following:

- fifteen light emitting diode (LED) alarm indicators for separate floors or areas
- LED indicators for the following:
  - — night alarm transfer
  - — alarm grouping
  - — TTC alarm
  - — power plant alarm
- night alarm transfer and alarm grouping function switches
- alarm release (AR) and audible alarm disable (AAD) switches for the piezo buzzer on the panel
- separate power supply paths for the floor or area alarm indication LEDs numbered 1 through 12

The following illustration shows a front view of the NT0X63MA CAD panel.

NT0X63MA central alarm display panel

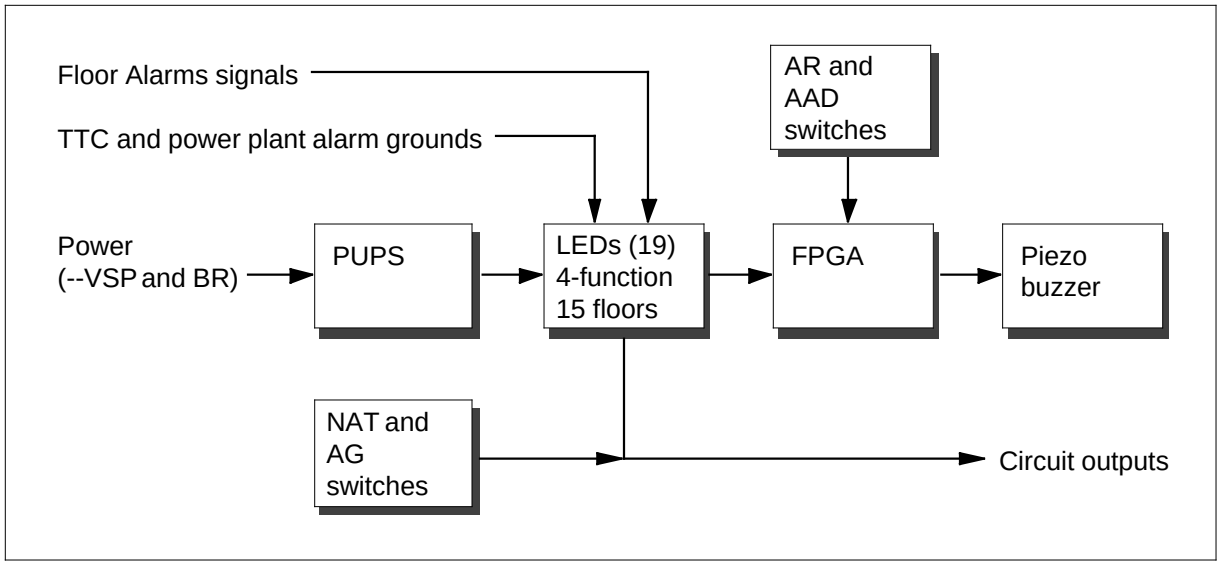


Legend: Lamp R = red
Lamp Y = yellow

Functional blocks

This section provides an illustration and descriptions of the main functional blocks of the NT0X63MA CAD panel.

NT0X63MA functional blocks



PUPS

The point-of-use power supply (PUPS) on the NT0X63MA is the same as the PUPS for the NT0X63LA alarm control and display (ACD) and NT0X63LB alarm display (AD) panels. The PUPS converts the alarm battery supply (ABS) voltage to a filtered 5V supply. The 5V supply provides the following:

- isolated system grounding (ISG) for the internal logic circuits
- reduced power requirement for the panel
- common panel design for North American and international offices

LEDs

The panel has 19 high brightness LED arrays. Illumination of an LED indicates an active circuit or the existance of an alarm condition.

Piezo buzzer

The piezo buzzer is a standard piezo-electric device that activates to indicate an alarm condition. The buzzer sounds until one of the following ocurs:

- the alarm condition does not exist
- you operate the alarm reset switch
- you enter the SIL command at the MAP terminal
- you operate the audible alarm disable switch

NT0X63MA (continued)

FPGA

The field programmable gate array (FPGA) contains the control circuits to activate the piezo buzzer (continuous audible alarm indication). On power up, the firmware downloads automatically from a serial programmable read-only memory (SPROM) device. The FPGA requires a 4-kHz clock signal.

Function switches

The NT0X63MA contains carbon pad switches for the following functions:

- night alarm transfer
- alarm grouping
- audible alarm disable
- audible alarm reset

Pin descriptions

The following table contains pin descriptions for the NT0X63MA CAD panel.

Interface connectors (C00/C01) pinouts (Sheet 1 of 2)

Pin number	Signal label	Description
1	FGND	frame ground
2	-48V	-VSP source power
3	BR	battery return
4	AG	alarm grouping signal
5	EP-PWR	exit panel - power plant
6	EPGDF15	exit panel - battery return for Zone 15
7	EPGDF13	exit panel - battery return for Zone 13
8	EPGDF12	exit panel - battery return for Zone 12
9	EPGDF11	exit panel - battery return for Zone 11
10	EPGDF10	exit panel - battery return for Zone 10
11	EPGDF9	exit panel - battery return for Zone 9
12	EPGDF8	exit panel - battery return for Zone 8
13	EPGDF7	exit panel - battery return for Zone 7

Interface connectors (C00/C01) pinouts (Sheet 2 of 2)

Pin number	Signal label	Description
14	EPGDF6	exit panel - battery return for Zone 6
15	EPGDF5	exit panel - battery return for Zone 5
16	EPGDF4	exit panel - battery return for Zone 4
17	EPGDF3	exit panel - battery return for Zone 3
18	EPGDF2	exit panel - battery return for Zone 2
19	EPGDF1	exit panel - battery return for Zone 1
20	BR	battery return
21	-48V	-VSP source power
22	FA-ALM	panel failure alarm
23	TTC	night alarm transfer signal
24	EP-TTP	exit panel - trunk test center
25	EPGDF14	exit panel - battery return for Zone 14
26	EP48F12	exit panel - -VSP path for Zone 12
27	EP48F11	exit panel - -VSP path for Zone 11
28	EP48F10	exit panel - -VSP path for Zone 10
29	EP48F9	exit panel - -VSP path for Zone 9
30	EP48F8	exit panel - -VSP path for Zone 8
31	EP48F7	exit panel - -VSP path for Zone 7
32	EP48F6	exit panel - -VSP path for Zone 6
33	EP48F5	exit panel - -VSP path for Zone 5
34	EP48F4	exit panel - -VSP path for Zone 4
35	EP48F3	exit panel - -VSP path for Zone 3
36	EP48F2	exit panel - -VSP path for Zone 2
37	EP48F1	exit panel - -VSP path for Zone 1

NT0X63MA (end)

Power requirements

The maximum power requirement for the NT0X63MA is 2 watts. The total power dissipation for the panel is 0.5 watts or 1.7 BTU.

The following table lists power requirements for the NT0X63MA.

Item	Minimum	Nominal	Maximum	Comments
A/B battery feed	-42.8V	-48.0V	-55.8V	-48V offices
A/B battery feed	-52.0V	-60.0V	-72V	-60V offices
Alarm signal inputs	-42.8V dc		72V dc	
supply noise		200 mV		each circuit at 5 mA
Supply current	90 mA		380 mA	

NT0X63MB

Product description

The NT0X63MB audible alarm cutoff (ACO) panel is a modular, low power peripheral alarm device. The NT0X63MB is part of the DMS-100 Family Low Power Alarm (LPA) system. The NT0X63MB provides the capability to disable or open the path between the alarm control circuits and the audible panels connected to the NT0X63MB.

The NT0X63MB ACO panel replaces and is backwards compatible with the NT5X86AA, NT5X86AB, and NT5X86AD ACO panels.

Functions

The NT0X63MB provides the following:

- three circuits with four signal paths each, to replace the NT5X86 (older alarm system) panel that has six circuits with two signal paths each
- visual indication when the normally-closed alarm disable (audibles cutoff) circuit activates
- operation in -48V and -60V offices

Panel controls and indicators

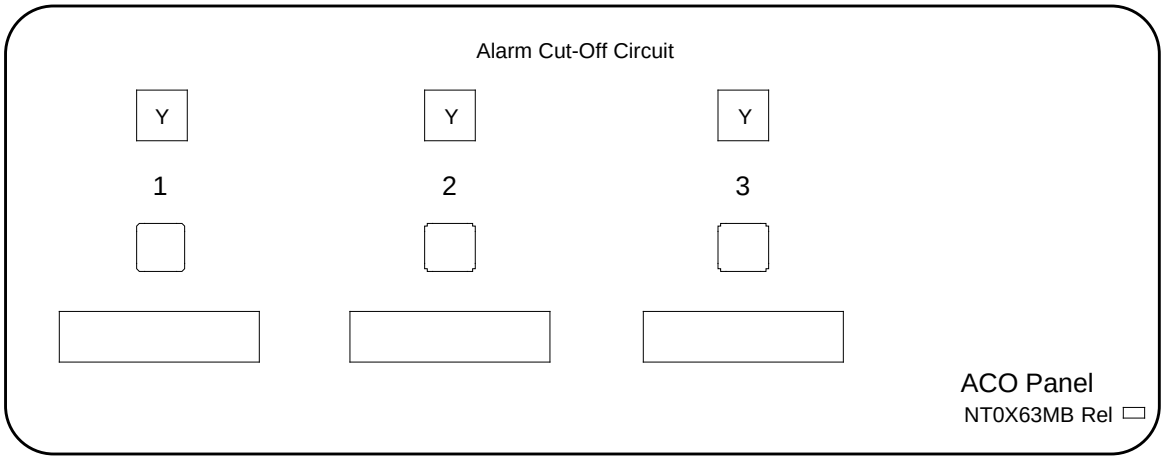
The NT0X63MB contains the following:

- three touch pad activation switches that control disconnect circuits for audible panels
- light emitting diode (LED) activation indicators for the three audibles cutoff switches

The following illustration shows a front view of the NT0X63MB ACO panel.

NT0X63MB (continued)

NT0X63MB alarm cutoff panel

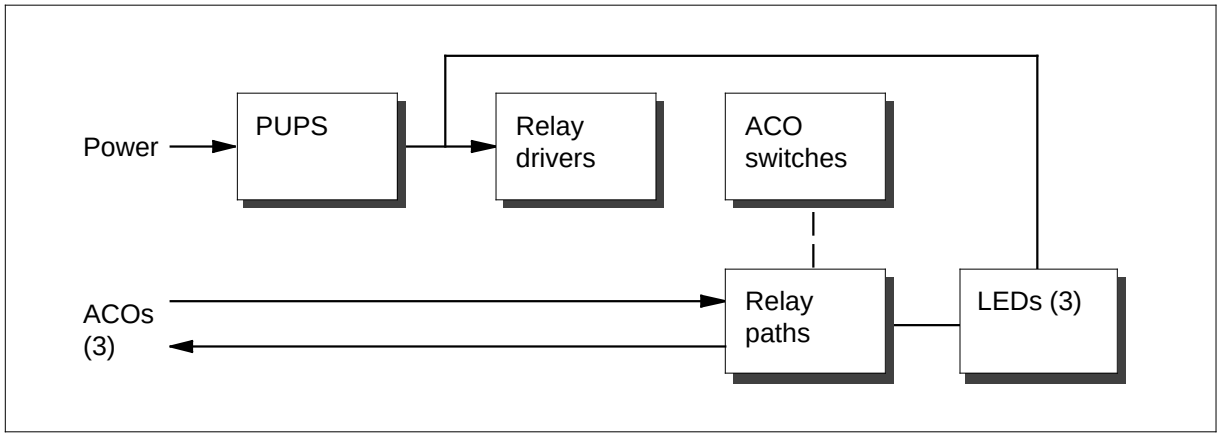


Legend: Lamp Y = yellow

Functional blocks

This section provides an illustration and descriptions of the main functional blocks of the NT0X63MB.

NT0X63MB functional blocks



PUPS

The point-of-use power supply (PUPS) on the NT0X63MB is the same as the PUPS for the NT0X63LA alarm control and display (ACD) and NT0X63LB

alarm display (AD) panels. The PUPS converts the alarm battery supply (ABS) voltage to a filtered 5V supply. The 5V supply provides the following:

- isolated system grounding (ISG) for the internal logic circuits
- reduced power requirement for the panel
- common panel design for North American and international offices

LEDs

The panel has three high brightness LED arrays. Illumination of an LED indicates an active circuit.

Function switches

The NT0X63MB contains three carbon pad switches. You can use these switches to activate or deactive the connected alarm cutoff relays.

Pin descriptions

The following tables contains pin descriptions for the NT0X63MB ACO panel.

Interface connectors (C00/C01) pinouts (Sheet 1 of 3)

Pin number	Signal label	Description
1	FGND	frame ground
2	BR	battery return (signal GND)
3	-VSP	power (-36V to -72V)
4	FA-ALM	panel failure alarm
5	spare	no connect
6	AB3-IN	alarm batery input - circuit 3
7	MN3-IN	minor alarm input - circuit 3
8	MJ3-IN	major alarm input - circuit 3
9	CR3-IN	critical alarm input - circuit 3
10	spare	no connect
11	AB2-IN	alarm battery input - circuit 2
12	MN2-IN	minor alarm input - circuit 2

NT0X63MB (continued)

Interface connectors (C00/C01) pinouts (Sheet 2 of 3)

Pin number	Signal label	Description
13	MJ2-IN	major alarm input - circuit 2
14	CR2-IN	critical alarm input - circuit 2
15	spare	no connect
16	AB1-IN	alarm battery input - circuit 1
17	MN1-IN	minor alarm input - circuit 1
18	MJ1-IN	major alarm input - circuit 1
19	CR1-IN	critical alarm input - circuit 1
20	BR	battery return (signal GND)
21	-VSP	power (-36V to -72V)
22	spare	no connect
23	spare	no connect
24	AB3-OUT	alarm battery output - circuit 3
25	MN3-OUT	minor alarm output - circuit 3
26	MJ3-OUT	major alarm output - circuit 3
27	CR3-OUT	critical alarm output - circuit 3
28	spare	no connect
29	AB2-OUT	alarm battery output - circuit 2
30	MN2-OUT	minor alarm output - circuit 2
31	MJ2-OUT	major alarm output - circuit 2
32	CR2-OUT	critical alarm output - circuit 2
33	spare	no connect
34	AB1-OUT	alarm battery output - circuit 1
35	MN1-OUT	minor alarm output - circuit 1

Interface connectors (C00/C01) pinouts (Sheet 3 of 3)

Pin number	Signal label	Description
36	MJ1-OUT	major alarm output - circuit 1
37	CR1-OUT	critical alarm output - circuit 1

PCBA to facia connections

Pin number	Signal label	Description
1	+5V	common anode supply voltage
2	spare	no connect
3	ACO-1L	LED indicator -circuit 1
4	ACO-1S	function switch -circuit 1
5	spare	no connect
6	ACO-2L	LED indicator -circuit 2
7	ACO-2S	function switch -circuit 2
8	spare	no connect
9	ACO-3L	LED indicator -circuit 3
10	ACO-3S	function switch -circuit 3
11	spare	no connect
12	spare	no connect

Power requirements

The maximum power requirement for the NT0X63MB is 2 watts. The total power dissipation for the panel is 0.5 watts or 1.7 BTU.

NT0X63MB (end)

The following table lists power requirements for the NT0X63MB.

Item	Minimum	Nominal	Maximum	Comments
A/B battery feed	-43.8V	-48.0V	-55.8V	-48V offices
A/B battery feed	-52.0V	-60.0V	-72V	-60V offices
panel operation	- 36.0Vdc		-72V dc	
supply noise		200 mV		each circuit at 5 mA
Supply current	30 mA	50 mA	90 mA	

NT0X66CA

Product description

The NT0X66CA audible alarms panel (AAP) is a modular, low power peripheral alarm device. The NT0X66CA is part of the DMS-100 Family Low Power Alarm (LPA) system. The NT0X66CA generates all audible alarm indications required by the DMS office except for the 2900-Hz buzzer, which the NT0X63 panel generates.

The NT0X66CA replaces the following units: NT0X61AA, NT0X61AB, NT0X61AC, NT0X66AA, NT0X66AB, NT0X66BA, and NT0X66KA.

You can combine the NT0X66CA with any of the (older) alarm system units listed in the previous paragraph with the same office configuration. However, the NT0X66CA input signals must be driven from separate SD points. If the NT0X66CA input signals are combined on the same SD points, the large inductive voltages of the older mechanical units will damage the NT0X66CA panel.

Functions

The NT0X66CA panel provides the following audible alarms:

- critical bell (CR-AUDIO)
- major chime (MJ-AUDIO)
- alarm battery ringer (AB-AUDIO)
- minor alarm ringer (MA-AUDIO)
- trunk test center (TTC) chime, two modes (TTC-AUDIO)

NT0X66CA (continued)

You use the NT0X66CA panel in one of the following modes:

- unique audibles alarms, mode 1 generates:
  - CR-AUDIO
  - MJ-AUDIO
  - AB-AUDIO
  - MA-AUDIO for TTC-AUDIO also
- unique chime audible alarm, mode 2 generates:
  - TTC-AUDIO
  - CR-AUDIO
  - MJ-AUDIO
  - AB-AUDIO
  - MA-AUDIO

Components

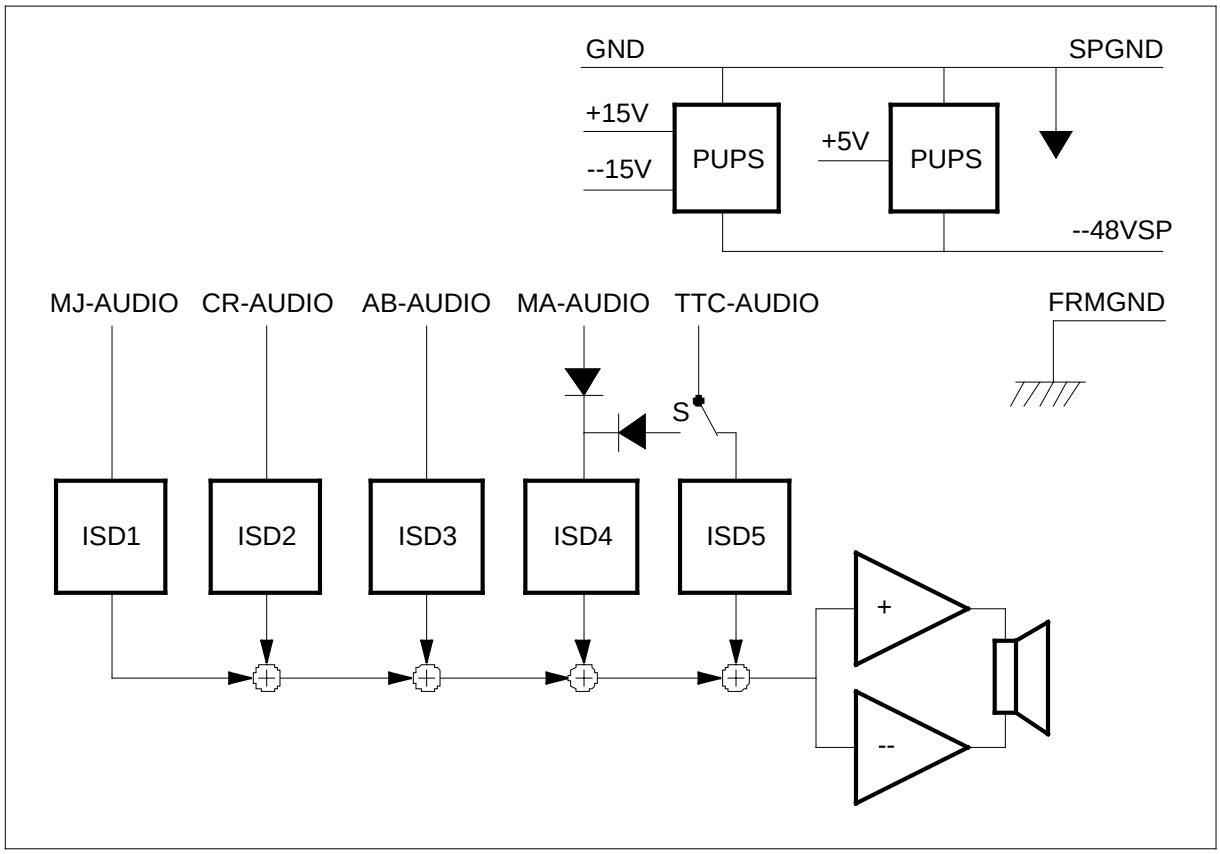
The NT0X66CA panel contains the following:

- mid-range 8-ohm speaker
- digital circuits that allow the unit to provide the following:
  - unique tones
  - trunk test center (TTC) chimes
- a toggle switch at the bottom of the panel housing to move between modes 1 and 2

Functional blocks

This section provides an illustration and descriptions of the main functional blocks of the NT0X66CA panel.

NT0X66CA functional blocks



The TTC-AUDIO functional block includes a two-position switch for manual selection of ringer or chime sounds.

PUPS

One point-of-use power supply (PUPS) provides the +5V source to power ISD (information storage device) generators. The other PUPS provides the +15V and -15V sources for the power amplifier.

Sound generators

The ISD generators produce the following distinct alarm indications (sounds):

- critical bell (260-Hz chime struck at 60 IPM)
- major chime (450-Hz chime struck at 200 IPM)
- alarm battery ringer (1000-Hz tone modulated by 20-Hz)
- minor alarm ringer (800-Hz tone modulated by 20-Hz)
- trunk test center (TTC) chime (600-Hz chime struck at 120 IPM)

NT0X66CA (continued)

Pin descriptions

The following table contains pin descriptions for the NT0X66CA panel. All connections are dc signals and all signals are analog.

Interface connectors (C01/C02) pin descriptions

Pin number	Signal label	Description
1	-48VSP/-60VSP	Office battery voltage, unfiltered
2	SPGND	office battery return, unfiltered
3	MJ-AUDIO	major audio: SPGND = on, floating = off
4	MA-AUDIO	minor alarm audio: SPGND = on, floating = off
5	TTC-AUDIO	TTC audio: SPGND = on, floating = off
6	AB-AUDIO	alarm battery audio: SPGND = on, floating = off
7	CR-AUDIO	critical audio: SPGND = on, floating = off
8	FRMGND	frame ground

Audible output characteristics

The following table lists the audible output characteristics of the NT0X66CA.

Source	Minimum (dB_A)	Nominal (dB_A)	Maximum (dB_A)	Comments
MJ-AUDIO	75	80	85	Mode 1
CR-AUDIO	75	80	85	Mode 1
AB-AUDIO	75	80	85	Mode 1
MA-AUDIO	75	80	85	Mode 1
TTC-AUDIO	75	80	85	Mode 2 (chime sound)
TTC-AUDIO	75	80	85	Mode 2 (ringer sound)

Power requirements

The maximum power dissipation for the panel is 50 watts or 170 BTU. This occurs when you use it as a unique audibles alarm panel (mode 1) and all four alarm indications sound.

NT0X66CA (end)

The following table lists power requirements for the NT0X66CA.

Item	Minimum	Nominal	Maximum	Comments
Battery voltage	-42.8V	-48.0V	-55.8V	-48V offices
battery voltage	-52.0V	-60.0V	-72V	-60V offices
Supply current	0.7A	1.1A	1.4A	mode 1, four sounds generated

NT0X70AC

Product description

The trunk module (TM) processor card (NT0X70AC) controls or performs the operations on a trunk module shelf. The TM processor card contains a microprocessor driven by read only memory (ROM) firmware and two random access memory (RAM) devices. One RAM stores program information and the second RAM stores operational information. Operational information includes connection information for pulse code modulation (PCM) channel-to-trunk assignments. The second RAM includes circuits that generate the clock signal, check parity and perform synchronization.

The only difference between the NT0X70AC and the NT0X70AA is that the dynamic memory has been increased from 16 kbyte to 32 kbyte.

Location

The NT0X70AC is in one card position in a trunk module (TM) or a maintenance trunk module (MTM).

Functional description

The NT0X70AC performs the following functions:

- intelligent buffer for commands and control data for the TM and MTM
- input output (I/O) ports for internal and external use (external through a test card)

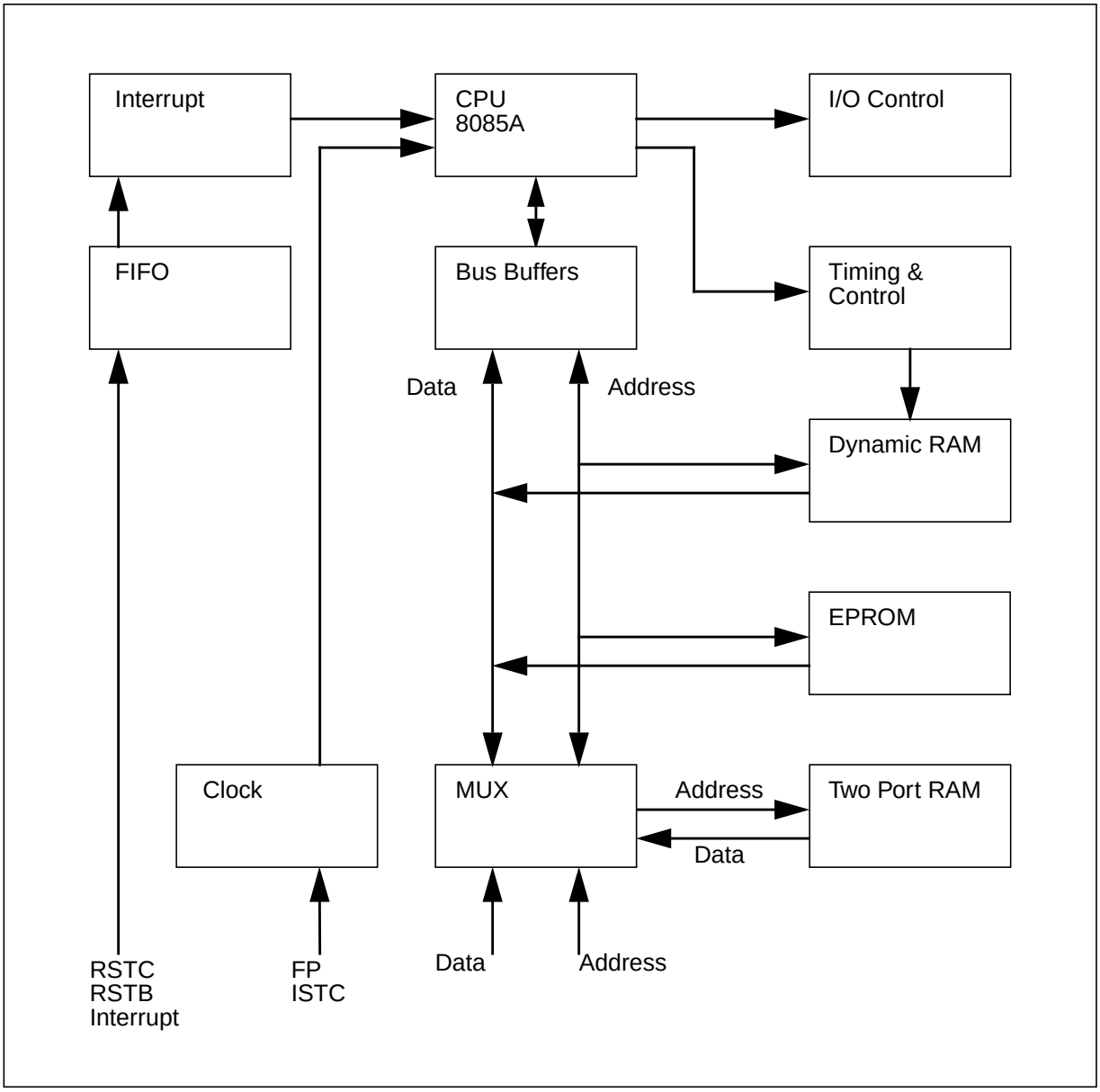
Functional blocks

The NT0X70AC contains the following functional blocks:

- central processing unit (CPU)
- EPROM
- dynamic random access memory (DRAM)
- two port buffer RAM
- first-in, first-out (FIFO) interrupt stack
- control logic

The relationship between the blocks appear in the next figure.

NT0X70AC functional blocks



CPU

The CPU contains an 8-bit 8085 microprocessor that operates at a frequency of 5.12 MHz.

EPROM

The erasable, programmable read only memory (EPROM) has 4 kbyte of firmware memory.

NT0X70AC (end)

DRAM

The program space for the processor contains nine of dynamic random-access memory (DRAM) devices, each with 32 kbyte of memory.

Two port RAM

A 1 kbyte two port memory between the NT0X70AC and the other TM and MTM cards is provided by static RAM, multiplexers and bus buffers.

First-in first-out interrupt stack

Two TTL 16 kbyte-by-4-bit FIFO's provide a FIFO stack for interrupts. The output ready line of the FIFO activates the interrupt line of the CPU, and also loads the interrupt vector to the CPU.

Dynamic memory parity

Parity is provided to detect single bit errors in the DRAM. A read parity error is latched in Flip-Flop, and causes a TRAP interrupt of the CPU.

I/O port support

Support for off card I/O ports is provided via I/O maps, CPU address and data buss.

Technical data

Power requirements

The NT0X70AC uses ±5V and +12V supply voltages.

NT0X71CA

Product Description

The NT0X71CA front and rear door kit operates on the NT0X25AA and AH frames. The front and rear doors are the primary parts of the kit.

Note: Install the other two kits NT0X73AK (End panel frame kit) and NT0X73AJ (End guard frame kit), with the NT0X71CA.

Each door has a hollow area to accept labels for the frame. Shelf labels are available on the inside of the front door. Doors have a ground cable connection and a door restraint strap. The strap does not allow the door to open more than 135 degrees.

Note: A 7 ft. frame with the NT0X71CA installed is 23.6 in. (600 mm) from front to rear. The NT0X71CA adds 2.8 in. (71 mm) to the front and rear of the frame.

This information allows access to a line card in the right drawer of a line shelf. From one vertical edge, you can hinge the front doors. To access this drawer, use a hinge to open the right front door and the left front door of the opposite frame. Place a hinge at the center of the frame. To access items other than the right line drawer, use hinge points. Place hinge points at the outside edge of the frame to open doors.

Note: Each kit has a common front door.

The front doors at the height of the line concentrating equipment (LCE) shelves allow for air ventilation. Air ventilation occurs at the height of the cooling unit for frames with cooling units.

Use single hinged doors at the rear of the frame. The doors open at the height of the LCE shelf baffle inlets/outlets.

Note: Each kit has one common rear door.

Adapters are available to attach the doors to the frames. The adapters use current features on the frame for location and attachment.

The front toe adapter has a 3 in. (76 mm) high by 4 in. (101.6 mm) deep toe hollow area from the door face. This deep toe hollow area aligns with cabinetized type switches. This hollow area allows the frame to stand on a single row of tiles in raised floor applications.

NT0X71CA (continued)

The bottom rear adapter has a large opening at the bottom. To access this opening, remove a knockout to increase the cable volume. You can run the cable volume from the frame to the under-floor area.

The top adapters have hinge tabs and a latch in the adapter. Vents in the top of the adapter allow cool air to flow in and out of the enclosure. The top adapters features allow you to mount the alarm lamp with the attached wires to the frame supervisory panel (FSP).

Parts

The NT0X71CA has of the following parts:

The NT0X71CA is one kit of three kits. You need all three kits to assemble the door, end panel, and end guard packaging on the NT0X25AA or AH frames. The NT0X71CA has front doors, rear doors, and all the necessary mounting hardware. Refer to table NT0X71CA front and rear door kit for additional information on the parts.

Design

The main parts of the NT0X71CA kit appear in the following table. The design of the NT0X71CA front and rear door kit appears in the following table.

NT0X71CA front and rear door kit (Sheet 1 of 2)

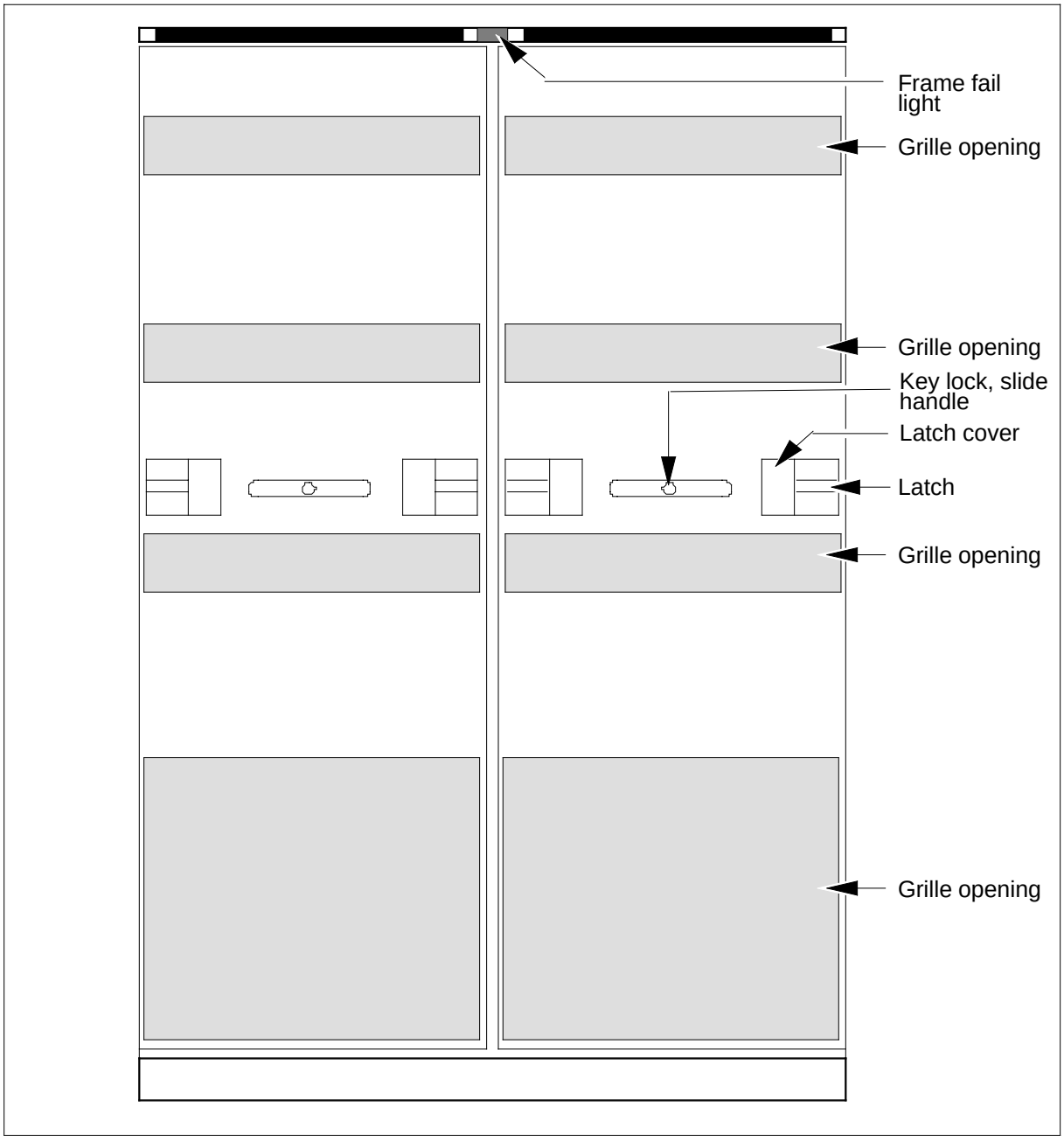
Quantity	PEC	CPC	Description
2	NT0X7527	B0242612	Door assembly, front, gray
1	NT0X7528	B0242613	Door assembly, left rear, gray
1	NT0X7529	B0242614	Door assembly, right rear, gray
1	NT0X7530	B0242615	Adapter assembly, top front
1		P0809506	Adapter, top rear
2		P0808852	Adapter, bottom
14		P097F812	Screw, .213-24 x .375 STL 289F

NT0X71CA front and rear door kit (Sheet 2 of 2)

Quantity	PEC	CPC	Description
4		A0382381	Connector terminal lug disconnect, bent
4		P0127312	Screw, machine
2		P0559409	Screw, tapping
2		P0725885	Pin, Cotter, extended prong, .125
1		P0809234	Cover, lamp, back
8		P0613379	Screw, Taptite, 5/16-18 x 1/2

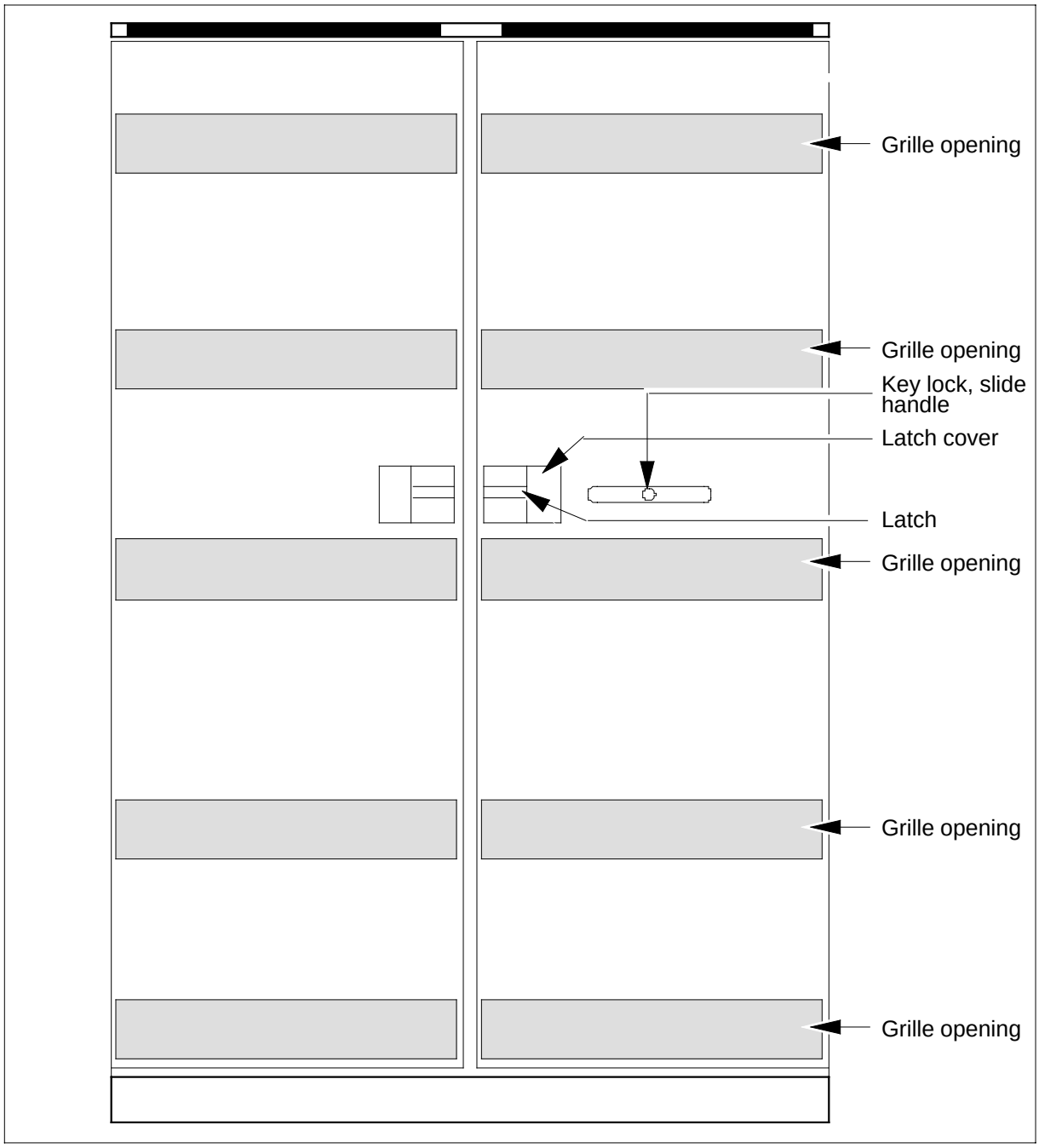
NT0X71CA (continued)

Normal front view of NT0X71CA door kit



Note: This diagram is not drawn to scale

Normal rear view of NT0X71CA door kit



Note: This diagram is not drawn to scale

NT0X73AJ

Product Description

Use the NT0X73AJ End guard frame kit on the NT0X25AA or AH frames.

> ***Note:*** Install other kits NT0X71CA (Front and rear door kit) and NT0X73AK (End panel frame kit) with the NT0X73AK.

End guards cover the area from the top of the frame to approximately 3 in. (76 mm) above the floor. The 3 in. space above the floor applies to equipment that is 24 in. (609.6 mm) deep. This space allows the removal of floor tiles in raised floor applications. End guards for positions immediately to the right of an line concentrating equipment (LCE) allow card line access. These End guards swing away for line card access.

Parts

The NT0X73AJ has the following parts:

The NT0X73AJ is one kit of three kits. You need these kits to assemble the door, end panel, and end guard packaging on the NT0X25AA or AH frames. The NT0X73AJ has an end guard and all the necessary hardware for mounting. Refer to Table NT0X73AJ End panel frame kit for additional information of the parts.

Design

The following table describes the main components of the NT0X73AJ kit. The design of the NT0X73AJ appears in the figure that follows this table. Use the End guard frame kit on a normal NT0X25AA or AH frame.

The NT0X73AJ End guard frame kit includes the NT1X69AB End guard assembly. This assembly provides an end aisle lamp and spare fuse holder.

NT0X73AJ End guard frame kit (Sheet 1 of 2)

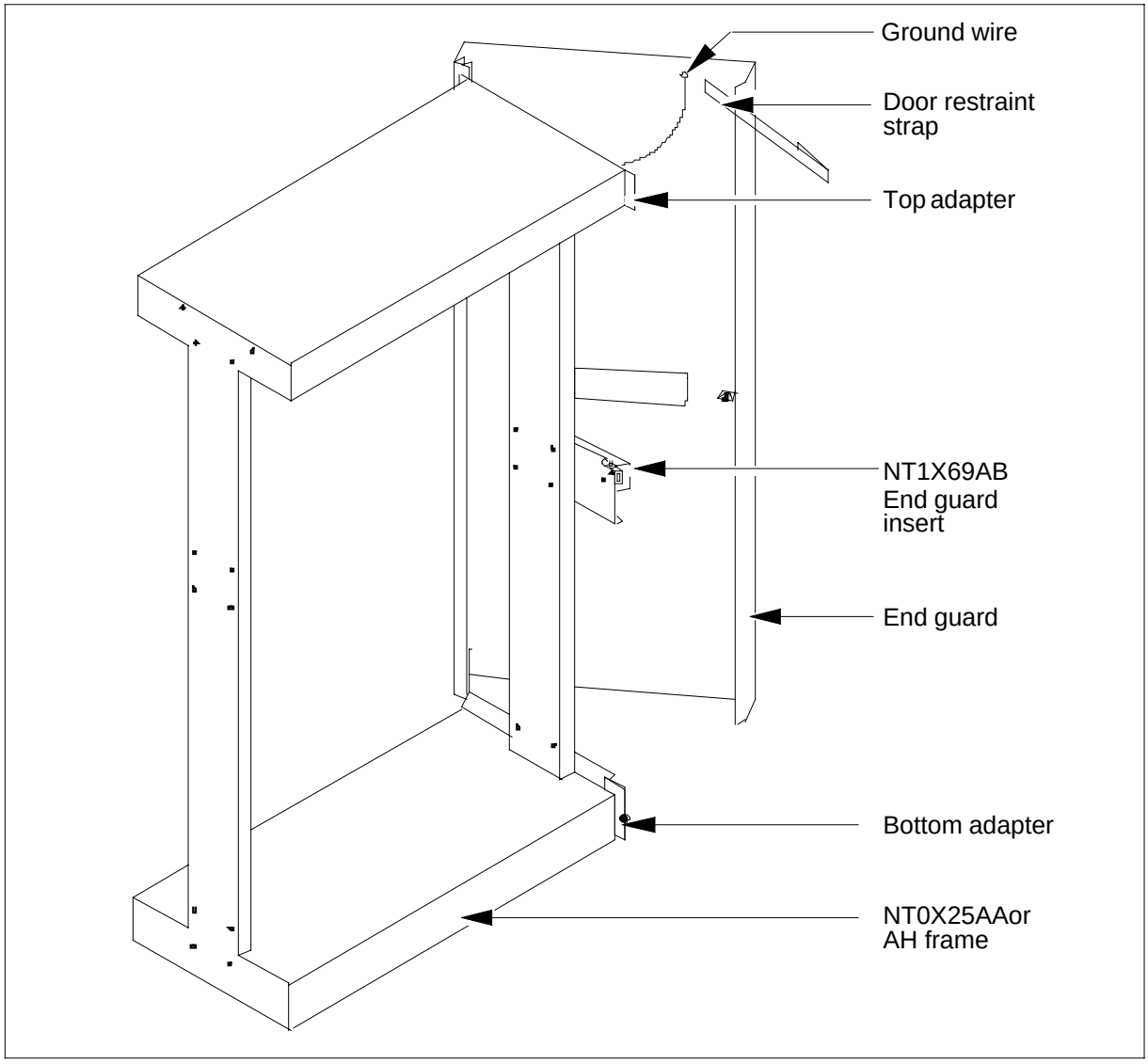
Quantity	PEC	CPC	Description
1		P0808765	Bottom adapter assembly
1		P0808766	End guard, 24 in. assembly
1	NT0X7124	B0242603	Ground cable
2		P0423633	Washer, lock, ext. tooth .168 x .381 x .023

NT0X73AJ End guard frame kit (Sheet 2 of 2)

Quantity	PEC	CPC	Description
2		P0627369	Nut & washer, Hex assembly
1		A0326703	Connector terminal lug disconnect, bent
4		P097F813	Screw, .216-24 x .500 STL 289F
1		P0809510	Bracket, mounting
1		A0634737	Latch, slam-action, floating keeper
2		P0661457	Screw, Hex washer head
1		P0725885	Pin, Cotter, extended prong, .125 diameter
4		P0125952	Nut, 289A finish, .138-32
1		P0808853	Strap, door restraint
1		P0808764	Adapter assembly, top
6		P097F812	Screw, .216-24 x .375 STL 289F

NT0X73AJ (end)

Typical diagonal view of NT0X73AJ end guard kit (installed)



Note: This diagram is not drawn to scale

NT0X73AK

Product Description

Use the NT0X73AK End panel frame kit on the NT0X25AA or AH frames. Most of this kit is blank end panels.

Note: Install other kits NT0X71CA (Front and rear door kit) and NT0X73AJ (End guard frame kit) with the NT0X73AK.

End panels for positions immediately to the right of a line concentrating equipment (LCE) frame are designed for line card access. These panels swing out of the way for line card access.

Parts

The NT0X73AK has the following parts:

The NT0X73AK is one kit of a total of three kits. You must have these kits to assemble the door, end panel, and end guard packaging on the NT0X25AA or AH frames. The NT0X73AK has an end panel and all the hardware that you need for mounting. Refer to table NT0X73AK End panel frame kit for a detailed description of the parts.

Design

The following table describes the main components that comprise the NT0X73AK kit. The figure that follows this table shows the design of the NT0X73AK End panel frame kit. This design is for a normal NT0X25AA or AH frame.

The NT0X73AK End panel frame kit is a blank panel. This kit does not include the NT1X69AB End guard assembly.

NT0X73AK End panel frame kit (Sheet 1 of 2)

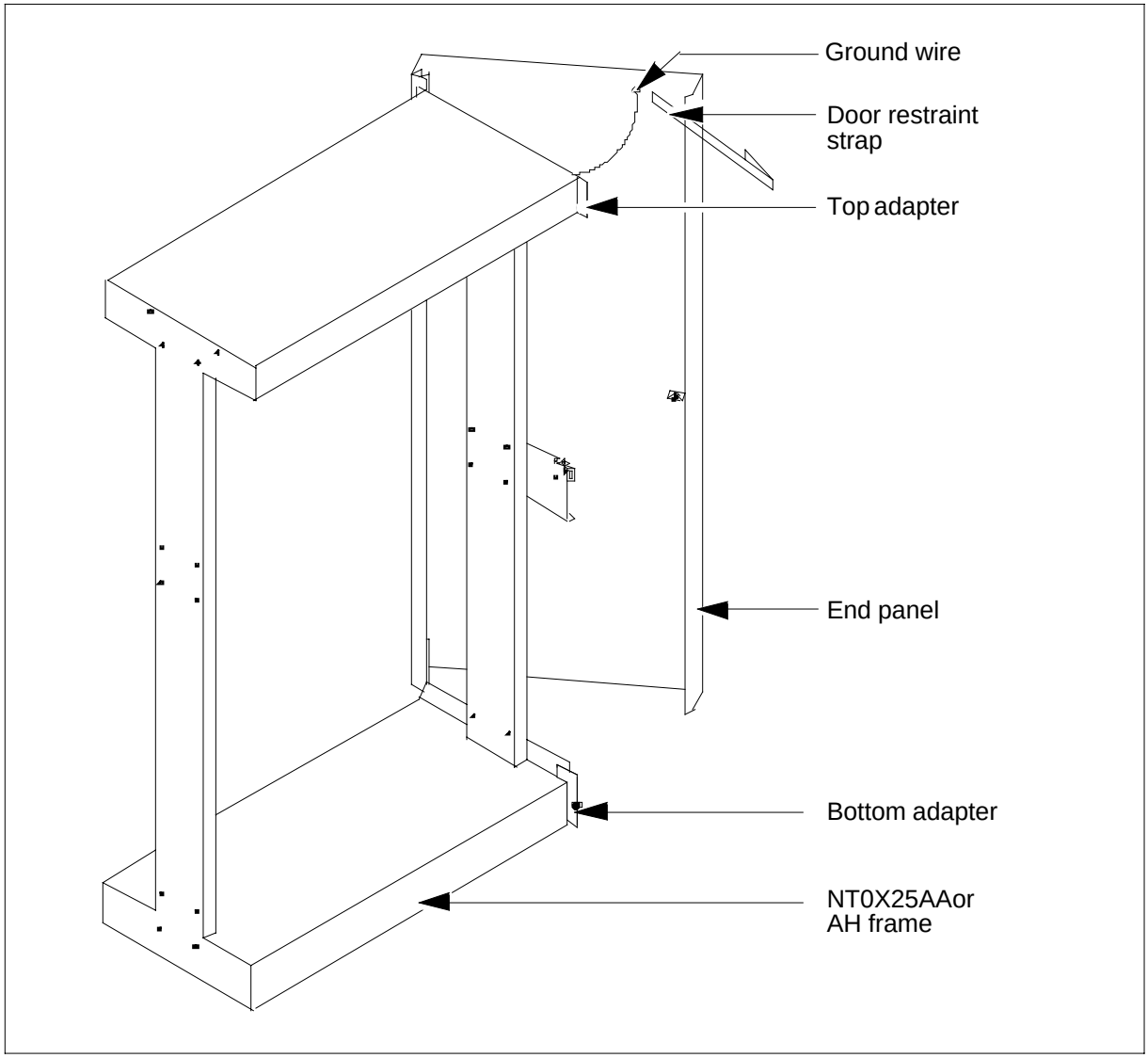
Quantity	PEC	CPC	Description
1		P0808765	Bottom adapter assembly
1		P0808767	End panel, 24-in. assembly
1	NT0X7124	B0242603	Ground cable
2		P0423633	Washer, lock, ext. tooth .168 x .381 x .023

NT0X73AK (continued)

NT0X73AK End panel frame kit (Sheet 2 of 2)

Quantity	PEC	CPC	Description
2		P0627369	Nut & washer, Hex assembly
1		A0326703	Connector terminal lug disconnect, bent
10		P097F812	Screw, .216-24 x .375 STL 289F
1		P0809510	Bracket, mounting
1		A0634737	Latch, slam-action, floating keeper
2		P0661457	Screw, Hex washer head
1		P0725885	Pin, Cotter, extended prong, .125 diameter
4		P0125952	Nut, 289A finish, .138-32
1		P0808853	Strap, door restraint
1		P0808764	Adapter assembly, top

Typical diagonal view of NT0X73AK end panel kit (installed)



Note: This diagram is not drawn to scale

NT0X82AB

Product Description

The NT0X82AB frame supervisory panel (FSP) contains power control and alarm circuits. The power control and alarm circuits provide interface between the following parts of the DMS-100 group digital switching system:

- the power distribution center (PDC)
- the peripheral module (PM) frame

The FSP uses circuit breakers (CB) to protect the power control circuits. The FSP uses fuses to protect the alarm circuits.

The FSP contains three different types of circuit packs (CP):

- the NT0X91AA converter drive and alarm
- the NT0X91AB converter drive
- the NT0X91AD converter drive

  The FSP uses the NT0X91AA converter drive to monitor all CB and fuse alarms.

Parts

The NT0X82AB has the following parts:

CP feed selection

Selection of the -48V power feeds to CPs 18, 51 and 65 the NT0X82AA FSP occurs in same method as the NT0X82AA. Selection of the link identification (A through F) is done in the same method. The same limits apply to power feeds to the following:

- maintenance trunk modules (MTM)
- office alarm units (OAU)
- digital carrier modules (DCM)
- talk battery supplies to trunk modules (TM)

Front panel controls and indicators

Circuit breakers 1 to 5 are manually operated from the front panel. The associated converter fail light-emitting diode (LED) indicator is below the CB that feeds the converter. If converters fail, a signal on the associated converter fail lead causes the LED to activate.

The fuses have a mechanical indicator that appears from the front of the panel when a guard has operated. Fuse positions 4 through 8, and 14 through 16 are not connected.

Converter drive and alarm

The FSP uses the converter drive and alarm to monitor all CBs. The FSP uses the converter drive and alarm to monitor fuse alarms. The CP has two parts: a converter drive and an alarm. The converter drive part of the CP contains two power control circuits. One of the power control circuits provides power control through CB 5 to CP 04 of the PM frame. At the same time, the other power control circuit is not in use. The NT0X91AA converter drive and alarm power-up sequence is the same as the NT0X91AD converter drive.

The alarm part of the CP receives input from the guard contacts of the CBs 1 through 5. The alarm part of the CP receives input from the fuses (1, 2, 3, 5, and 9 through 13).

Converter drives

The FSP uses one of each type of the converter drives that provide power control and protection. The converter drives provide control and protection to shelves 18, 32, 51, and 65 of the PM frame through CB 1 through CB 4. Refer to the figure titled "NT0X82AB parts." Each converter drive provides two power control circuits.

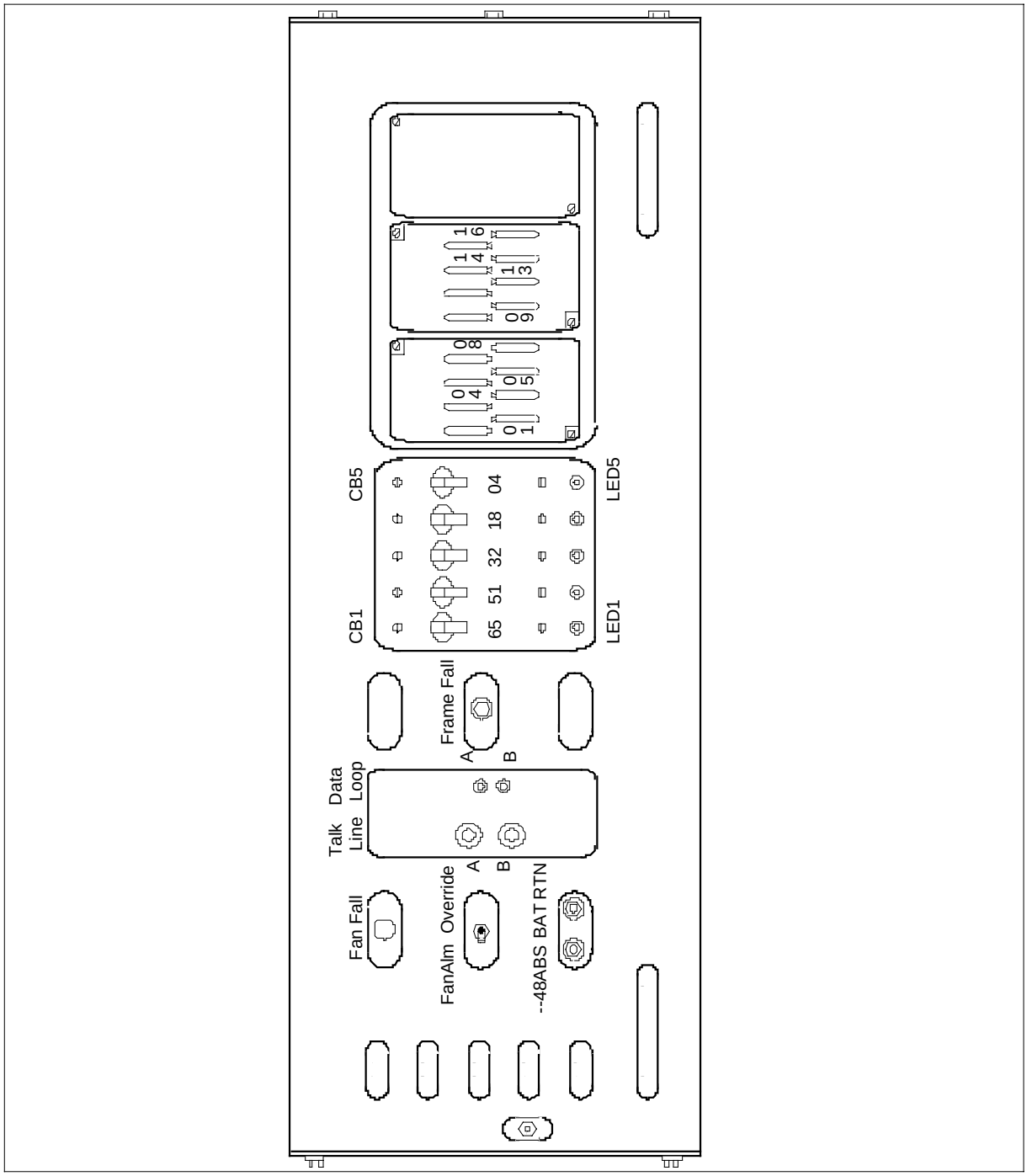
The fuses have a mechanical indicator that appears from the front of the panel when a guard has operated. Fuse positions 4 through 8, and 14 through 16 are not connected.

Design

The design of the FSP appears in the following figure.

NT0X82AB (end)

NT0X82AB parts



Note: This diagram is not drawn to scale

NT0X84AA

Product Description

Use the NT0X84AA cage filler panel assembly to fill empty shelf positions in the NT8X01BB outside plant module (OPM) frame. Perform this action to satisfy forced air cooling requirements.

You can use the cage filler panel assembly in the NT9X05AB enhanced network (ENET) cabinet. The ENET cabinet houses a maximum of four ENET shelves, a frame supervisory panel, and a cooling unit.

Parts

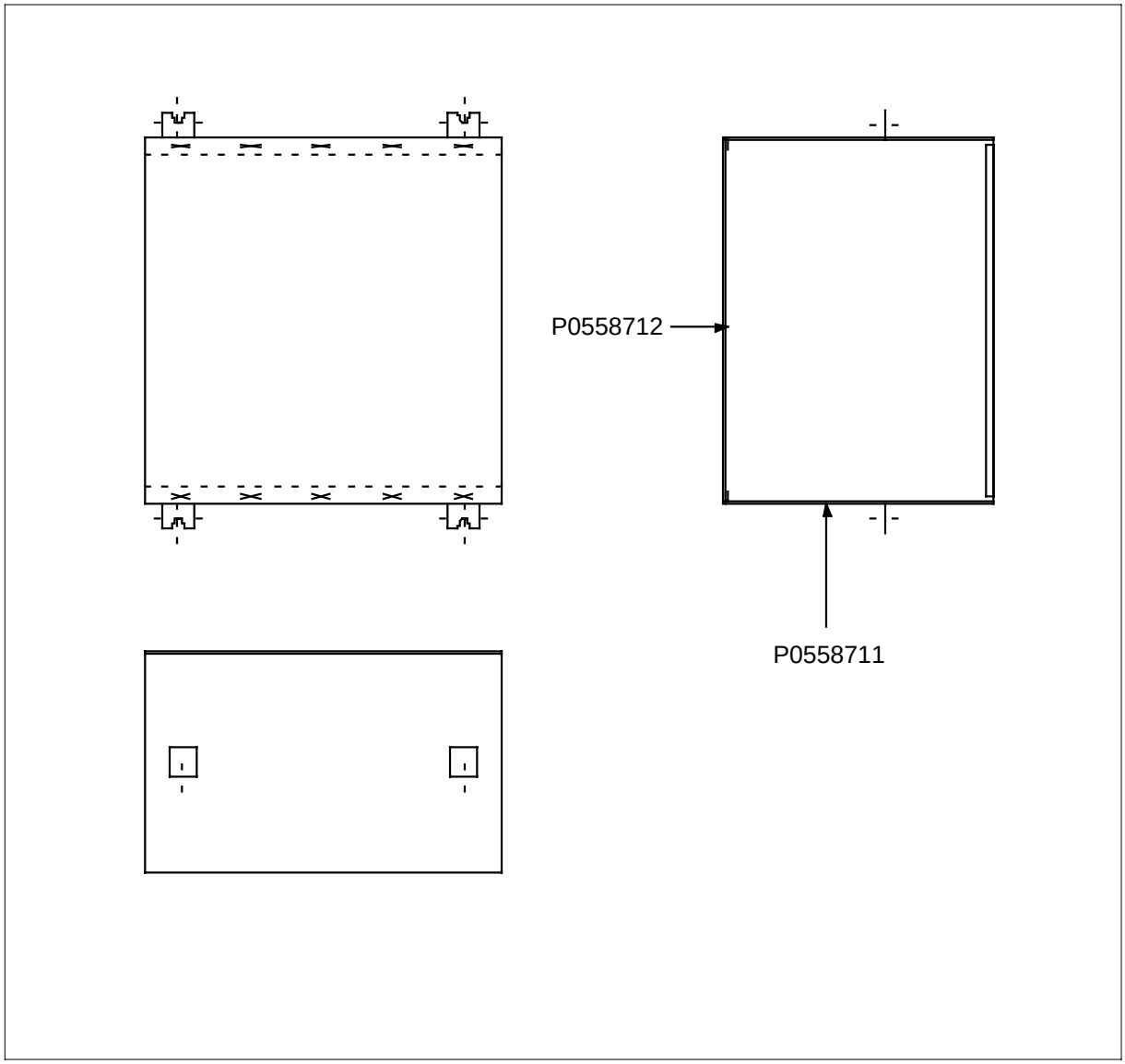
The cage filler panel assembly is available in a brown finish. There are no attachments or components for the cage filler panel assembly.

Design

The design of the cage filler panel assembly appears in the following figure.

NT0X84AA (end)

NT0X84AA parts



NT0X87AA

Product description

The NT0X87AA dc-to-ac inverter module supplies 117-V, 60-MHz ac to auxiliary devices. These auxiliary devices are associated with the DMS-100 Family of digital switching systems. The switching systems include teleprinters, cooling fans, and MAP terminals.

Input voltage to the NT0X87AA is a small -48V dc. The system supplies this input voltage through the power distribution center (PDC). When the PDC supplies -48V (small) and battery return (BR) to the inverter input, the control section of the inverter activates. When the main input circuit breaker (CBI) is set to ON, the switching inverter operates after 1 s. This delay makes sure that control circuits operate correctly. This action must occur the inverter section receives power.

Parts

The NT0X87AA has the following main parts:

- input filter
- SCR inverter
- ferroresonant transformer
- output filter
- control circuit power
- inverter control
- transfer control
- transfer switch
- current sense
- low voltage monitor
- ac output receptacles
- test jacks

NT0X87AA (continued)

Design

Descriptions of the primary parts of the NT0X87AA appear in the following table.

NT0X87AA parts (Sheet 1 of 3)

PEC	Slot	Description
-	-	*AC output receptacles* Receptacle J1 provides access to the motor drive output. Receptacles J2, J3, and J4 provide access to the normal 117-V, 60-Hz output.
-	-	*Control circuit power* This circuit plugs in to, the NTOX87AA converter. This circuit is part of the NT0X87AA inverter. This control circuit activates when it receives -48 V. This control circuit activates before CB1 is set to ON. The circuit generates a steady control signal that the system applies to the inverter and transfer controls.
-	-	*Current sense* This circuit monitors the output current to J1 (output jack 1. This jack is one assigned for motor drive output). This circuit detects if an active high-current device is present. When this device is present, transfer switch action can occur.
-	-	*Ferroresonant transformer* This transformer has several functions. This transformer has four windings: • primary winding, which provides balanced center-tapped load for the inverter • starting winding, which supplies not regulated high current for the motor starting surge • output winding, which supplies the normal 117-V, 60 -Hz output • ferroresonant winding which, with the output filter, provides voltage regulation for the winding. Ferroresonant winding produces a low-distortion sinewave output

NT0X87AA parts (Sheet 2 of 3)

PEC	Slot	Description
-	-	*Inpu t filter* The input filter is a Pi type filter. This filter reduces the noise that is fed back to the battery to an acceptable level.
-	-	*Inverter control* The inverter control provides steady 60-Hz pulses to drive the gates of the silicon control rectifier (SCR). The inverter control provides a smooth start of the ferroresonant circuit.
-	-	*Low voltage monitor* The low voltage monitor continuously checks the output voltage from the inverter. An output voltage that falls below a threshold level activates the external alarm system. The front panel alarm lamp lights (if -48V dc input continues to be present).
-	-	*Output filter* This filter and the ferroresonant transformer provide voltage regulation and reduce harmonic distortion in the inverter output waveform.
-	-	*SCR inverter* The SCR inverter switches the dc power from the input source at a rate of 60 Hz. The switching (on/off) of the SCR generates an alternating current. The system applies the alternating current to the input of the ferroresonant transformer.
-	-	*Test jacks* The test jacks that are mounted on the faceplate of the converter provide test points (TP1-TP4) for reference purposes. These test jacks give approximate measurements. You can verify the -48V input and BR at TP1 and TP2. You can verify the 117-V, 60-Hz output at TP3 (neutral) and TP4.
-	-	*Transfer control* This circuit controls the operation of the transfer switch.

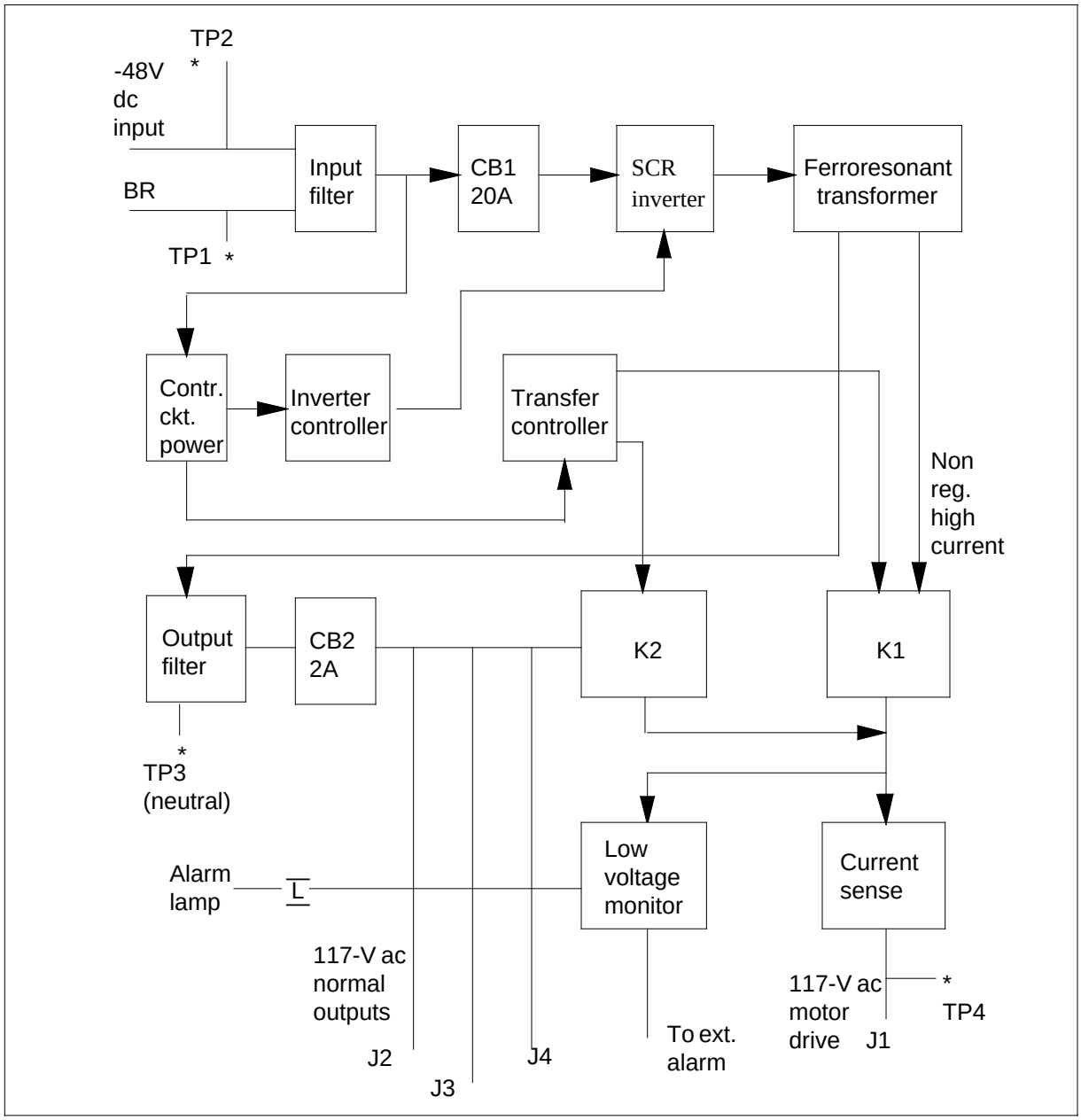
NT0X87AA (continued)

NT0X87AA parts (Sheet 3 of 3)

PEC	Slot	Description
-	-	*Transfer switch* Two solid state switches (K1 and K2) comprise the transfer switch. The transfer control circuit drives the solid state switches. When you connect a load to the motor drive output, and the high-current device is on, ac power is received. The starting winding of the ferroresonant transformer supplies this power. Approximately 0.8 s later, the transfer control circuit activates the transfer switch. The normal output winding of the transformer supplies the motor drive output.

A simplified block diagram that indicates the electrical flow in the unit appears in the following figure.

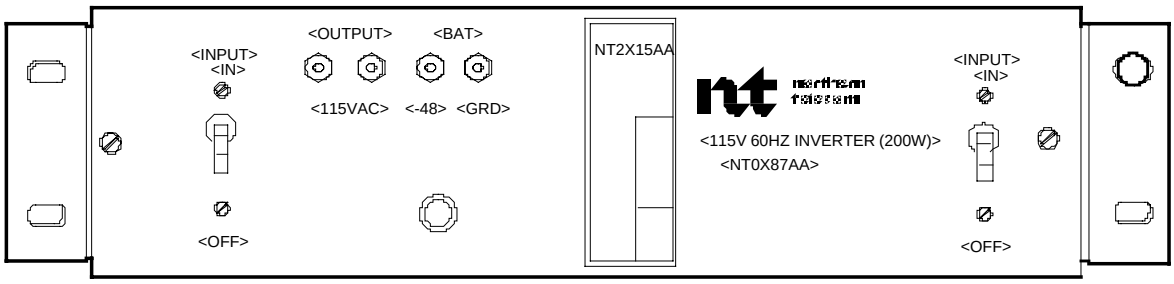
NT0X87AA simplified block diagram



The front panel of the inverter unit appears in the following figure.

NT0X87AA (end)

NT0X87AA front view



Note: This diagram is not drawn to scale.

NT0X88AB

Product description

The NT0X88AB frame supervisory panel (FSP) receives feeder cables from the power distribution center fuse. The FSP uses local fuses to distribute dc power to the shelves in the NT0X02AB frame.

The NT0X88AB receives the alarm battery supply (ABS) multiple feeder from the ABS fuse in the power distribution center (PDC). The NT0X88AB routes the ABS through internal fuses to the frame alarm circuits.

The NT0X88AB FSP is at shelf position 45 in the NT0X02AB frame.

Parts

The NT0X88AB shelf contains the following parts:

- A0205202-Fuse QFF1A
- A0205203-A0205209 Fuses. These fuses can be provisioned.
- A0205210-Dummy fuse QFF3A. This fuse can be provisioned.
- NT0X8800-MIS FSP assembly
- NT0X91AA-Converter drive and alarm card

Design

The design of the NT0X88AB shelf appears in the following table.

NT0X88AB parts (Sheet 1 of 2)

Heading	Heading	Heading
A0205202	F01-F03	*Fuse QFF1A* Fuse QFF1A is a 1.33-A fuse. Install this fuse in fuse positions F01, F02, and F03. You can use this fuse in any of the fuse positions that remain. You cannot use this fuse in F04, in which a dummy fuse is installed. The A0205202 uses a white, P097P235 designation disk.
A0205202-A0205209	F05-F24	*Fuse* Refer to the Fuse and designation discs table for additional information.
A0205210	F04	*Dummy fuse QFF3A* Install the A0205210 dummy fuse in fuse position 04 and other fuse holders not in use.

NT0X88AB (continued)

NT0X88AB parts (Sheet 2 of 2)

Heading	Heading	Heading
NT0X8800	-	*MIS frame FSP panel assembly* The NT0X8800 has two 10-A circuit breakers, the CB1 and CB2. You can assign these circuit breakers to equipment mounted in the NT0X02AB frame.
NT0X91AA	01	*Converter drive and alarm card* Provides aisle alarm output to the DMS-100 alarm system when an alarm guard contact operates.

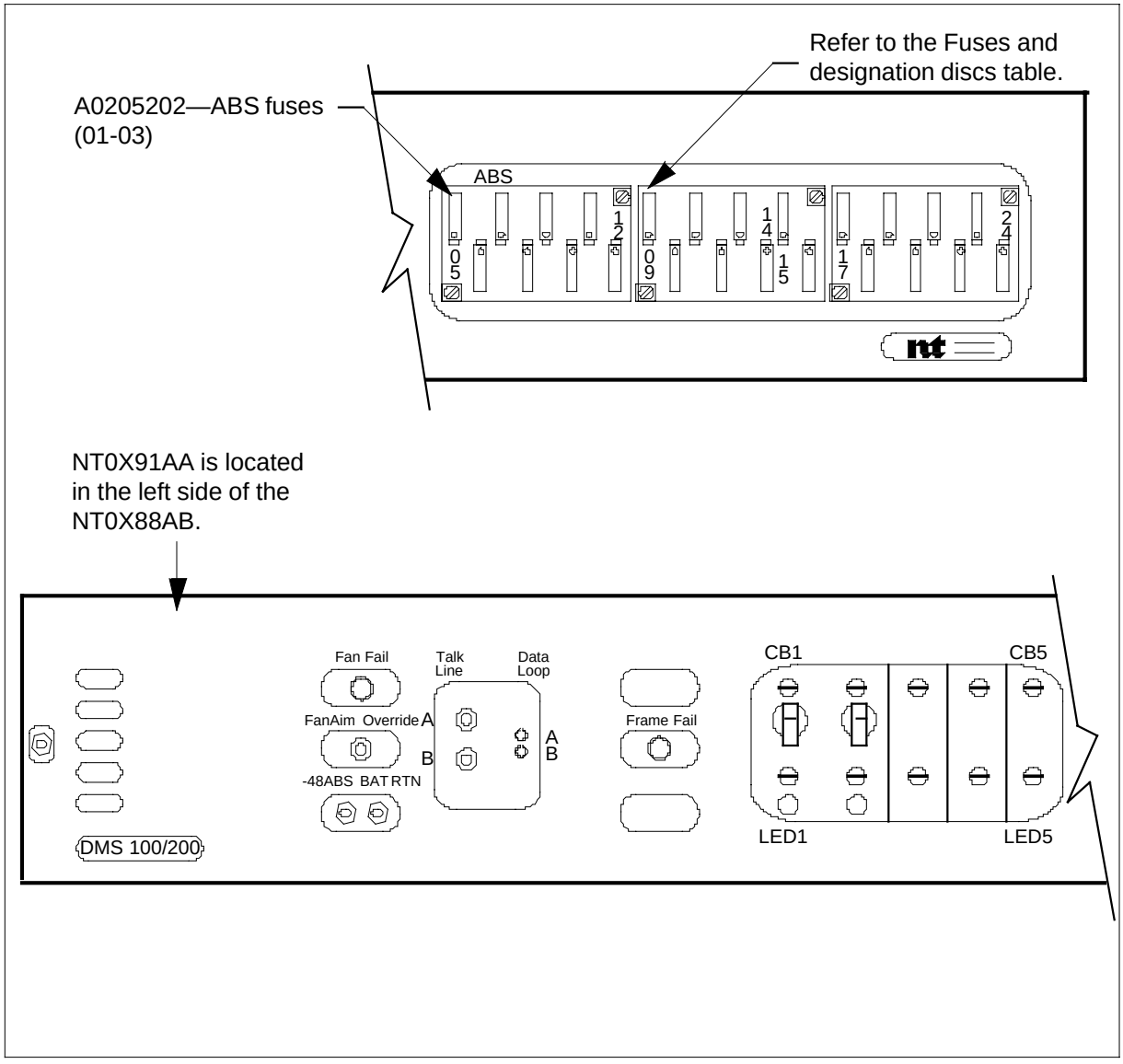
Information on the fuses and the associated designation discs appear in the following table.

Fuses and designation discs

Fuse rating (amps)	Fuse type	PEC	Designation disc Color PEC
0.18	QFF1E	A0205206	Y P097P239
0.25	QFF1F	A0205207	V P097P240
0.50	QFF1G	A0205208	R P097P241
0.75	QFF1H	A0205209	BR P097P242
1.33	QFF1A	A0205202	WH P097P235
2.0	QFF1B	A0205203	O P097P236
3.0	QFF1C	A0205204	BL P097P237
5.0	QFF1D	A0205205	G P097P238

The front of the panel appears in the following figure.

NT0X88AB front view



NT0X88AD

Product description

The NT0X88AD frame supervisory panel (FSP) receives feeder cables from the power distribution center fuse. The NT0X88AD uses local fuses to distribute dc power to the shelves in the NT0X02AB remote service equipment (RSE) frame.

The NT0X88AD receives the alarm battery supply (ABS) multiple feeder from the ABS fuse in the power distribution center (PDC). The NT0X88AD routes the ABS through internal fuses to the frame alarm circuits.

The RSE frame uses the NT0X88AD FSP when the RSE frame operates in a remote line module office. The NT0X88AD FSP is at shelf position 45.

Parts

The NT0X88AD shelf contains the following parts:

- A0205202-Fuse QFF1A
- A0205203-A0205209 Fuses. These fuses can be provisioned.
- A0205210-Dummy fuse QFF3A. This fuse can be provisioned.
- NT0X8820-RSE FSP assembly
- NT0X91AA-Converter drive and alarm card
- NT0X91AD-Converter drive and protection circuit

Design

The design of the NT0X88AD shelf appears in the following table.

NT0X88AD card (Sheet 1 of 2)

Card PEC	Slot	Description
A0205202	F01-F03	*Fuse QFF1A* Fuse QFF1A is a 1.33-A fuse. Install this fuse in fuse positions F01, F02, and F03. You can use this fuse in the fuse positions that remain, except in F04. Position F04 contains a dummy fuse. The A0205202 uses a white, P097P235 designation disk.
A0205202-A0205209	F05-F16	*Fuse* Refer to the Fuses and designation discs table for additional information.

NT0X88AD card (Sheet 2 of 2)

Card PEC	Slot	Description
A0205210	F04	*Dummy fuse QFF3A* Install the A0205210 dummy fuse in fuse position 04, and in other fuse holders that are not used.
NT0X8820	-	*RSE frame FSP panel assembly* The NT0X8820 has four 10-A circuit breakers, CB1 through CB4. You can assign these circuit breakers to equipment mounted in the NT0X02AB frame.
NT0X91AA	01	*Converter drive and alarm card* The NT0X91AA provides aisle alarm output to the DMS-100 alarm system when an alarm guard contact operates.
NT0X91AD	02	*Converter drive and protection circuit* The NT0X91AD provides power control and protection circuits.

Information on the fuses and the associated designation discs appear in the following table.

Fuses and designation discs

Fuse rating (amps)	Fuse type	PEC	Designation disc Color	PEC
0.18	QFF1E	A0205206	Y	P097P239
0.25	QFF1F	A0205207	V	P097P240
0.50	QFF1G	A0205208	R	P097P241
0.75	QFF1H	A0205209	BR	P097P242
1.33	QFF1A	A0205202	WH	P097P235
2.0	QFF1B	A0205203	O	P097P236
3.0	QFF1C	A0205204	BL	P097P237
5.0	QFF1D	A0205205	G	P097P238

NT0X88AD (continued)

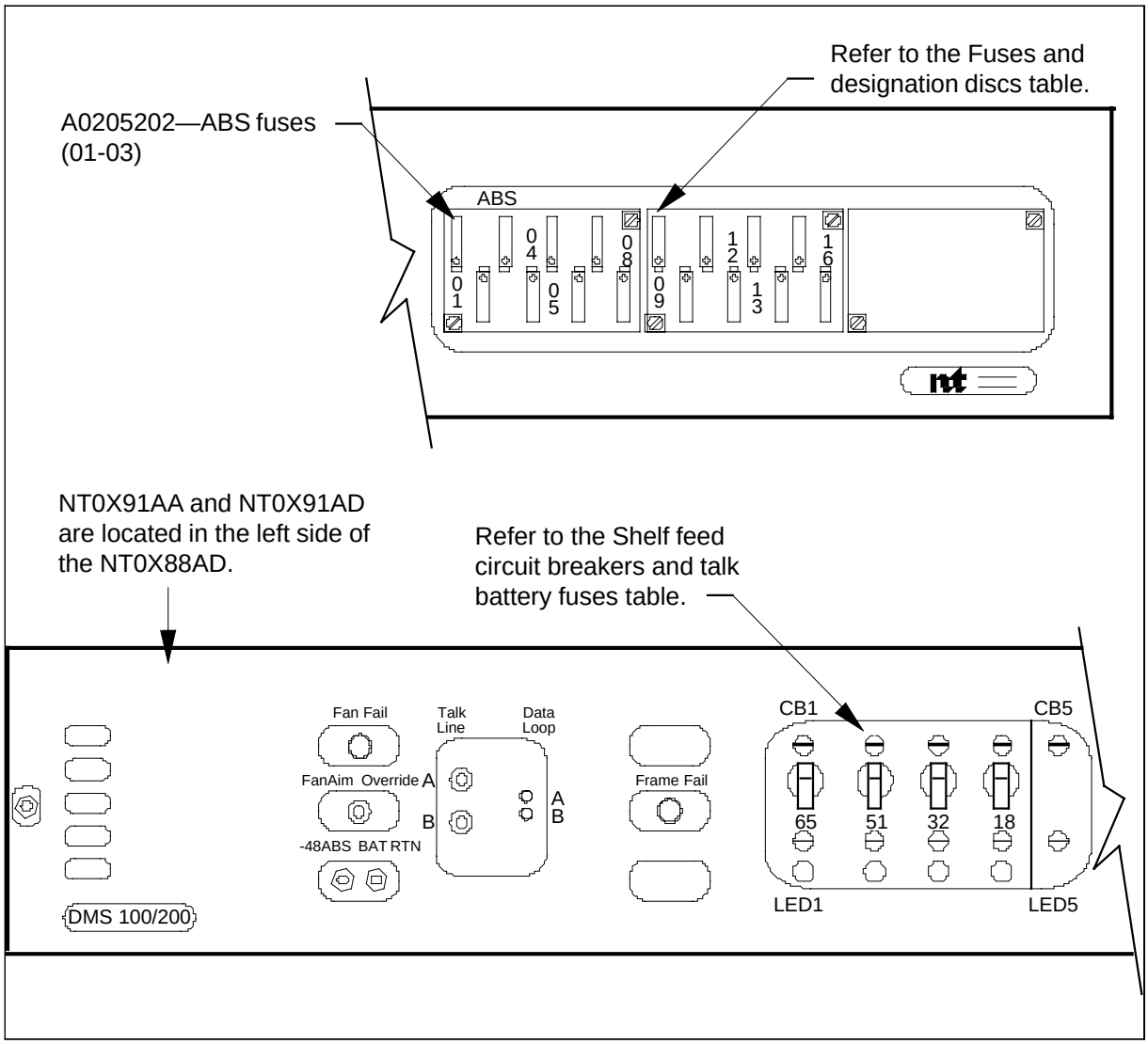
Information on the shelf feed and the shelf talk battery appears in the following table. This information applies when the NT0X88AD supplies talk battery to NT2X58 remote service module shelves.

Shelf feed circuit breakers and talk battery fuses

	Shelf feed				**Shelf talk battery**	
RSM shelf POS	**CB rating**	**Loc**	**Term ID**	**Fuse rating**	**Loc**	**Term ID**
65	10A	CB1	TB1-12	1.33	F12	TB2-10
51	10A	CB2	TB1-11	1.33	F11	TB2-9
32	10A	CB3	TB1-10	1.33	F10	TB2-8
18	10A	CB4	TB1-9	1.33	F09	TB2-7

The front of the NT0X88AD panel appears in the following table.

NT0X88AD front view



NT0X88AE

Product description

The NT0X88AE frame supervisory panel (FSP) receives feeder cables from the power distribution center fuse. This FSP uses local fuses to distribute dc power to the shelves in the NT0X02AB miscellaneous equipment (MIS) frame.

The NT0X88AE receives the alarm battery supply (ABS) multiple feeder from the ABS fuse in the power distribution center (PDC). The NT0X88AE routes the ABS through internal fuses to the frame alarm circuits.

The NT0X88AE FSP is used in the NT0X02AB miscellaneous equipment frame when equipment in the frame requires 10A, filtered -48V circuit breakers. The NT0X88AE is at shelf position 45.

Parts

The NT0X88AE shelf contains the following parts:

- A0205202-Fuse QFF1A
- A0205203-A0205209 Fuses. These fuses can be provisioned
- A0205210-Dummy fuse QFF3A. These fuses can be provisioned
- NT0X8833-10A filtered MIS frame FSP assembly
- NT0X91AA-Converter drive and alarm card

Design

The design of the NT0X88AE appears in the following table.

NT0X88AE parts (Sheet 1 of 2)

Card PEC	Slot	Description
A0205202	F01-F03	*Fuse QFF1A* Fuse QFF1A is a 1.33-A fuse. Install this fuse in fuse positions F01, F02, and F03. You can use this fuse in the fuse positions that remain, except in F04. Position F04 contains a dummy fuse. The A0205202 uses a white, P097P235 designation disk.
A0205202-A0205209	F05-F16	*Fuse* Refer to the Fuses and designation discs table for additional information.

NT0X88AE parts (Sheet 2 of 2)

Card PEC	Slot	Description
A0205210	F04, and F5-F16 as needed	*Dummy fuse QFF3A* Install the A0205210 dummy fuse in fuse position 04, and in other fuse holders that are not in use.
NT0X8833	-	*10-A filtered MIS frame FSP panel assembly* The NT0X8833 has two 10-A circuit breakers, CB1 and CB2. You can assign these circuit breakers to equipment mounted in the NT0X02AB frame. You can assign CB1 to miscellaneous circuits. A remote test line requires a 10-A, filtered -48V supply.
NT0X91AA	01	*Converter drive and alarm card* The NT0X91AA provides aisle alarm output to the DMS-100 alarm system when an alarm guard contact operates.

Information on the fuses and the associated designation discs appear in the following table.

Fuses and designation discs

Fuse rating			Designation disc	
(amps)	Fuse type	PEC	color	PEC
0.18	QFF1E	A0205206	Y	P097P239
0.25	QFF1F	A0205207	V	P097P240
0.50	QFF1G	A0205208	R	P097P241
0.75	QFF1H	A0205209	BR	P097P242
1.33	QFF1A	A0205202	WH	P097P235
2.0	QFF1B	A0205203	O	P097P236
3.0	QFF1C	A0205204	BL	P097P037
5.0	QFF1D	A0205205	G	P097P038

NT0X88AE (continued)

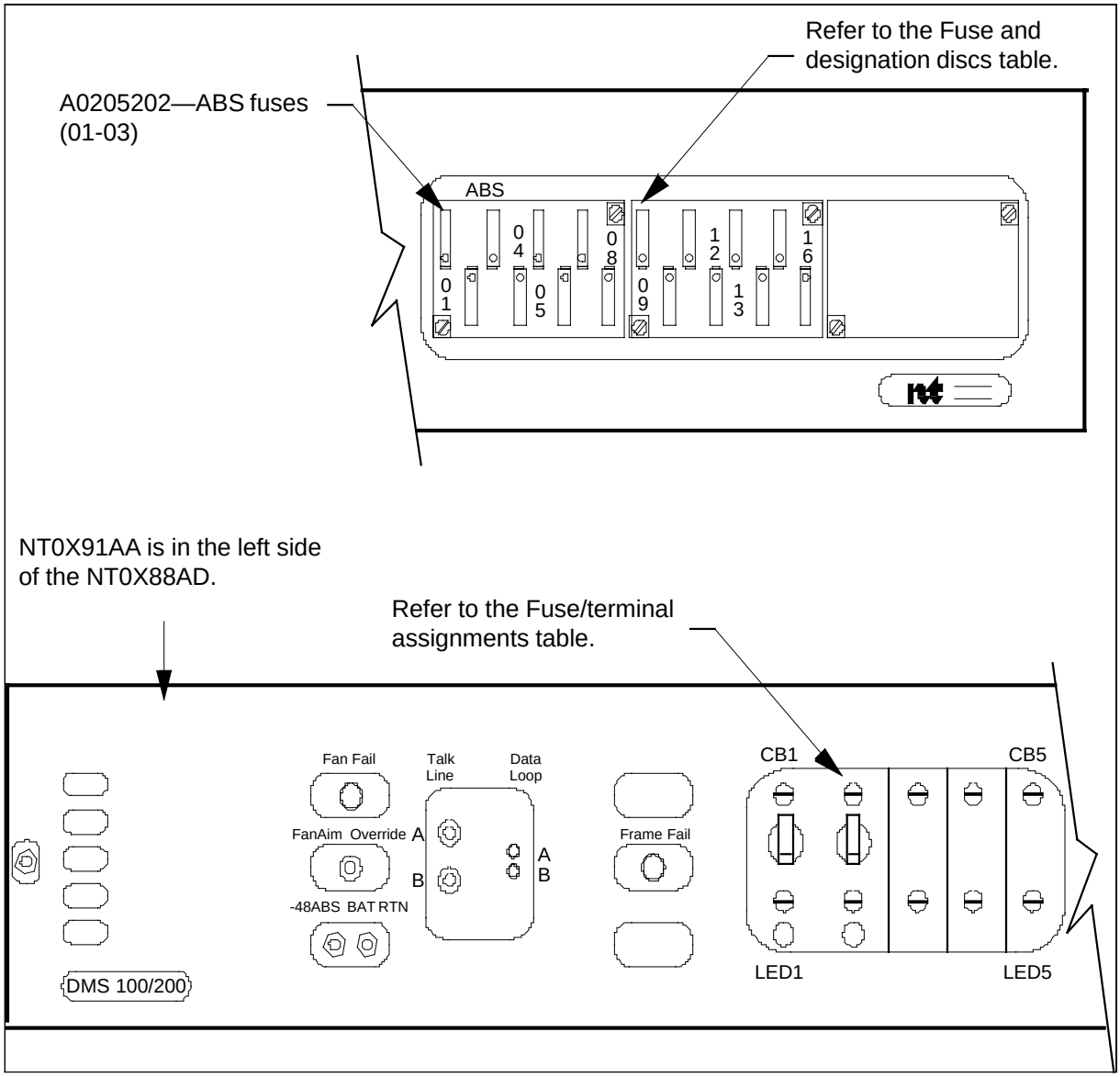
Information on the FSP fuse/terminal assignments appears in the following table.

Fuse/terminal assignments

Fuse loc.	Max rating (amps)	PDC feed	FSP terminal	Comments
CB1	10 Fixed	A	TB1-12	ROTL or miscellaneous circuits that require talk battery
CB2	10 Fixed	B	TB1-11	Miscellaneous circuits
F01	1.33 Fixed	ABS		-Alarm battery to PC card
F02	1.33 Fixed	ABS	TB3-11	Alarm battery end AIS LP
F03	1.33 Fixed	ABS		-Alarm battery FSP j acks
F04	Dummy	ABS		-Not in use
F05	5	A	TB2-1	Miscellaneous circuits
F06	5	A	TB2-2	Miscellaneous circuits
F07	5	A	TB2-3	Miscellaneous circuits
F08	5	A	TB2-4	Miscellaneous circuits
F09	5	A	TB2-7	Miscellaneous circuits
F10	5	A	TB2-8	Miscellaneous circuits
F11	5	B	TB2-9	Miscellaneous circuits
F12	5	B	TB2-10	Miscellaneous circuits
F13	5	B	TB3-7	Miscellaneous circuits
F14	5	B	TB3-8	Miscellaneous circuits
F15	5	B	TB3-9	Miscellaneous circuits
F16	5	B	TB3-10	Miscellaneous circuits

The front of the NT0X88AE panel appears in the following figure.

NT0X88AE front view



NT0X88AF

Product description

The NT0X88AF frame supervisory panel (FSP) receives feeder cables from the power distribution center fuse. The FSP uses local fuses to distribute dc power to the shelves in the NT0X02AB miscellaneous equipment (MIS) frame.

The NT0X88AF receives the alarm battery supply (ABS) multiple feeder from the ABS fuse in the power distribution center (PDC). The NT0X88AF routes the ABS through internal fuses to the frame alarm circuits.

Use NT0X88AF the FSP for remote module equipment (RME) frame-mounted equipment. Use this FSP for MIS equipment mounted on a frame that requires filtered (talk) battery. The NT0X88AF is at shelf position 45.

Parts

The NT0X88AF shelf contains the following parts:

- A0205202-Fuse QFF1A
- A0205203-A0205209 Fuses. These fuses can be provisioned.
- A0205210-Dummy fuse QFF3A. This fuse can be provisioned.
- NT0X8843-MIS frame FSP assembly
- NT0X91AA-Converter drive and alarm card

Design

The design of the NT0X88AF shelf appears in the following table.

NT0X88AF parts (Sheet 1 of 2)

Card PEC	Slot	Description
A0205202	F01-F03	*Fuse QFF1A* Fuse QFF1A is a 1.33-A fuse. Install this fuse in fuse positions F01, F02, and F03. You can use this fuse in the fuse positions that remain, except in F04. Position F04 contains a dummy fuse. The A0205202 uses a white, P097P235 designation disk.
A0205202-A0205209	F05-F24	*Fuse* Refer to the Fuses and designation discs table for additional information.

NT0X88AF parts (Sheet 2 of 2)

Card PEC	Slot	Description
A0205210	F04, and F5-F24 as needed	*Dummy fuse QFF3A* Install the A0205210 dummy fuse in fuse position 04, and other fuse holders that are not used.
NT0X8833	-	*10-A filtered MIS frame FSP panel assembly* The NT0X8833 has two 10-A circuit breakers, CB1 and CB2. You can assign these circuit breakers to equipment mounted in the NT0X02AB frame. You can assign CB1 to miscellaneous circuits. A remote test line requires a 10-A, filtered -48V supply.
NT0X91AA	01	*Converter drive and alarm card* The NT0X91AA provides aisle alarm output to the DMS-100 alarm system when an alarm guard contact operates.

Information on the fuses and the associated designation discs appear in the following table.

Fuses and designation discs

Fuse rating (amps)			Designation disc	
	Fuse type	PEC	Color	PEC
0.18	QFF1E	A0205206	Y	P097P239
0.25	QFF1F	A0205207	V	P097P240
0.50	QFF1G	A0205208	R	P097P241
0.75	QFF1H	A0205209	BR	P097P242
1.33	QFF1A	A0205202	WH	P097P235
2.9	QFF1B	A0205203	O	P097P236
3.0	QFF1C	A0205204	BL	P097P037
5.0	QFF1D	A0205205	G	P097P038

NT0X88AF (continued)

Information on the FSP fuse/terminal assignments appears in the following table.

Fuse/terminal assignments (Sheet 1 of 2)

Fuse loc.	Max rating (amps)	PDC feed	FSP terminal	Comments
CB1	10 Fixed	A	TB1-12	Miscellaneous circuits that require talk battery
CB2	10 Fixed	B	TB1-11	Miscellaneous circuits that require talk battery
F01	1.33 Fixed	ABS	TB1-14	Alarm battery to PC card
F02	1.33 Fixed	ABS	TB3-11	Alarm battery end AIS LP
F03	1.33 Fixed	ABS		-Alarm battery FSP jacks
F04	Dummy	ABS		-Not used
F05	5	A	TB2-1	Miscellaneous circuits that require talk battery
F06	5	A	TB2-2	Miscellaneous circuits that require talk battery
F07	5	A	TB2-3	Miscellaneous circuits that require talk battery
F08	5	A	TB2-4	Miscellaneous circuits that require talk battery
F09	5	A	TB2-7	Miscellaneous circuits that require talk battery
F10	5	A	TB2-8	Miscellaneous circuits that require talk battery
F11	5	B	TB2-9	Miscellaneous circuits that require talk battery
F12	5	B	TB2-10	Miscellaneous circuits that require talk battery
F13	5	B	TB3-7	Miscellaneous circuits that require talk battery
F14	5	B	TB3-8	Miscellaneous circuits that require talk battery
F15	5	B	TB3-9	Miscellaneous circuits that require talk battery
F16	5	B	TB3-10	Miscellaneous circuits that require talk battery
F17	1.33	B	TS1-1	Miscellaneous circuits that require talk battery*
F18	1.33	B	TS1-2	Miscellaneous circuits that require talk battery*

Note: * The TS1 pins have a limited current carrying capacity. Fuses in locations F17-F24 must not have a rate higher than 1.33A.

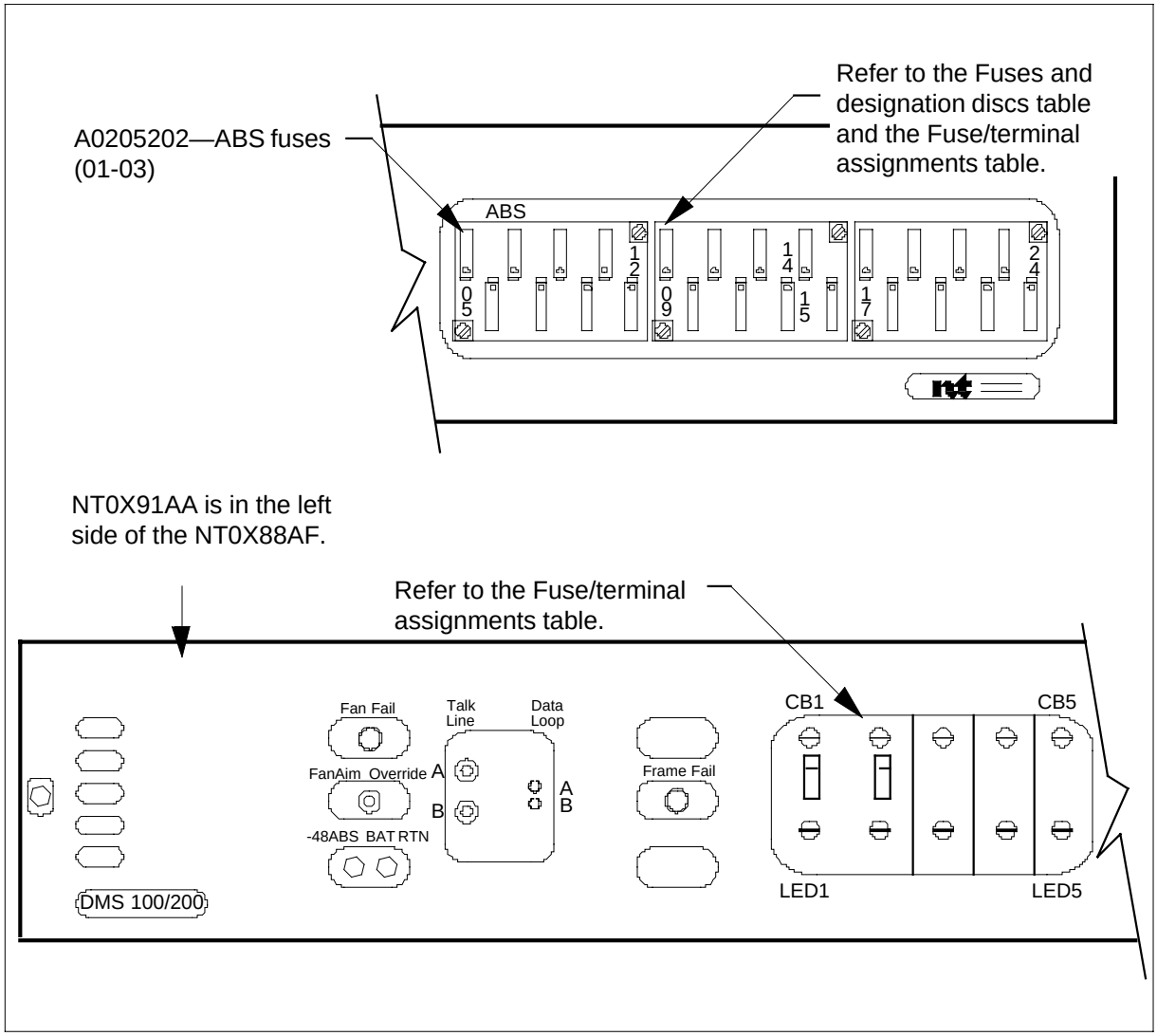
Fuse/terminal assignments (Sheet 2 of 2)

Fuse loc.	Max rating (amps)	PDC feed	FSP terminal	Comments
F19	1.33	B	TS1-3	Miscellaneous circuits that require talk battery*
F20	1.33	B	TS1-4	Miscellaneous circuits that require talk battery*
F21	1.33	B	TS1-5	Miscellaneous circuits that require talk battery*
F22	1.33	B	TS1-6	Miscellaneous circuits that require talk battery*
F23	1.33	B	TS1-7	Miscellaneous circuits that require talk battery*
F24	1.33	B	TS1-8	Miscellaneous circuits that require talk battery*
Note: * The TS1 pins have a limited current carrying capacity. Fuses in locations F17-F24 must not have a rate higher than 1.33A.				

The front of the NT0X88AF panel appears in the following figure.

NT0X88AF (end)

NT0X88AF front view



NT0X91AA

Product description

The NT0X91AA frame supervisory panel (FSP) drive and alarm circuit pack operates relay contacts in response to different alarm inputs. This pack activates the frame failure alarm and the aisle alarm loop. The drive circuit of the NT0X91AA supplies -48 V to the power converters in response to reset inputs.

Functional description

Functional blocks

The NT0X91AA contains the following functional blocks:

- alarm circuit
- drive circuit

Alarm circuit

If alarm input is not present, resistor R3 keeps transistor Q1 in the OFF position. Transistor Q2 is in the OFF position. This setting allows Q3 to be ON. Relay K1 opens the contacts. The contacts are normally closed. In this configuration, the frame fail lamp is OFF. The aisle alarm loop is open.

When the system applies -48 V nominal voltage to any of the six inputs marked -48 V FUSEGD, current flows through R5. Transistor Q2 changes to ON. This action changes Q3 to OFF. Relay K1 closes. This action lights the frame alarm lamp, and closes the aisle alarm loop. Each -48 V FUSEGD input normally connects to the alarm contact of a fuse or circuit breaker. The system can use any source of -48 V. Diodes D1 to D6 isolate the inputs to avoid direct connection between alarm contacts of fuses fed from separate -48V buses. Only fuses that operate at -48V nominal voltage can use these alarm inputs.

Fuses on the ±24V bus use the input marked 24 V FUSEGD. If the system applies a nominal ±24 V to this pin, transistor Q1 changes to ON. This setting causes Q2 to change to ON, and Q3 to change to OFF. This event operates the alarm relay.

The input LEDPWR connects to the converter-fail light-emitting diodes (LED) on the converter faceplate. When any of the LEDs are ON, the LED current moves through R1 and R3. The LEDs in an ON state indicate a converter failure. The voltage drop across R3 is enough to change Q1 to ON. This setting operates the alarm relay.

Transistor Q4 operates the fan fail lamp. When the cooling unit detects a fan failure, the system applies -48 V to pin 8. Transistor Q4 changes to ON. The fan fail lamp glows. An override switch connection is normally present

NT0X91AA (end)

between pins 9 and 12. Diode D8 sets Q3 to OFF. This setting operates the alarm relay. The fan alarm override switch on the FSP face plate breaks the connection between pins 9 and 12 to override the fan alarm. The fan fail lamp glows. This event does not activate the main alarm because the link through the D8 is not present.

Capacitor C1 prevents radio frequency (RF) instability.

Drive circuit

Transistor Q5 controls the drive to one of the power converters. When you press the converter reset button, the system applies a ground to the RESET A input. This action changes Q5 to ON. The system provides the DRIVE signal (-48 V) to the converter over the collector of Q5.

Capacitor C2 prevents high frequency instability.

Transistor Q6 and associated components use a similar method to control the second power converter.

NT0X91AE

Product description

The converter drive and protect (NT0X91AE) circuit pack contains five transistors which trip the frame supervisory panel (FSP) circuit breakers in response to reset inputs. Two additional transistors supply -48V drive to the power converters.

Functional description

When the circuit breaker is set to the on position, transistor Q1 is turned to the on position through resistors R3 and R4. Current then flows in the circuit breaker trip coil. When current is in the circuit breaker trip coil, the circuit breaker is immediately set to the off position. As a result it is not possible to supply power to the back panel before a power converter is plugged in. Diode D1 protects transistor Q1 from voltage spikes caused by the switching of the circuit breaker.

After a power converter is plugged in, switched to the on position, and the reset button is pressed, the circuit breaker can be set to the on position. When the power converter output voltage is at nominal value, the low voltage monitor relay closes, holding transistor Q1 in the off position, even after the reset button is released. This is the normal operating condition and is maintained indefinitely.

If the power converter output decreases caused by overloading or failure, the low voltage monitor R3, R4 and the circuit breaker are tripped. If the power converter is switched to the off position, the circuit breaker trip coil is operated directly.

Use transistor Q2 in the same way as transistor Q1 to control a second power converter and circuit breaker. Transistors Q3, Q4 and Q5 operate in the same way and are used to control up to three additional circuit breakers. Transistors Q3, Q4 and Q5 are on other FSP circuit packs.

Transistors Q6 and Q7 provide the drive outputs to the power converters. Capacitors C1 and C2 prevent high frequency instability.

NT0X91KA

Product description

The NT0X91KA frame supervisory panel (FSP) drive and alarm circuit pack is the -60V version of the NT0X91AA. These cards operate relay contacts in response to different alarm inputs. These alarms activate the frame failure alarm and the aisle alarm loop. The drive circuit supplies -60 V to the enable circuits of the power converters in response to reset inputs.

Functional description

Functional blocks

The NT0X91KA contains the following functional blocks:

- alarm circuit
- drive circuit

Alarm circuit

If alarm input is not present, resistor R3 keeps transistor Q1 in the OFF position. Transistor Q2 is in the OFF position. This event causes transistor Q3 to be ON. Relay K1 opens the contacts. The contacts are normally closed. In this configuration, the frame fail lamp is OFF. The aisle alarm loop is open.

When the system applies -60V nominal voltage to any of the six inputs marked -60V FUSEGD, current flows through resistor R5. Transistor Q2 changes to ON. This action changes Q3 to OFF. Relay K1 closes. This event lights the frame alarm lamp, and closes the aisle alarm loop. Each -60V FUSEGD input normally connects to the alarm contact of a fuse or circuit breaker. The system can use any source of -60 V. Diodes D1 to D6 isolate the inputs to avoid direct connection between alarm contacts of fuses fed from separate -60V buses. You can use these alarm inputs only for fuses that operate at -60V nominal voltage.

Fuses on the ±24V bus use the input marked 24V FUSEGD. If the system applies a nominal ±24 V to this pin, transistor Q1 changes to ON. This setting causes transistor Q2 to change to ON. Transistor Q3 changes to OFF. This event operates the alarm relay.

The input LEDPWR connects to the converter-fail light-emitting diodes (LED) on the converter faceplate. When any of the LEDs are on, the LED current moves through R1 and R3. The LEDs in an ON state indicate a converter failure. The voltage drop across R3 is enough to change transistor Q1 to ON. This event operates the alarm relay.

Transistor Q4 operates the fan fail lamp. When the cooling unit detects a fan failure, the system applies -60 V to pin 8. Transistor Q4 changes to ON. The fan fail lamp glows. An override switch connection is normally present

between pins 9 and 12. Diode D8 sets Q3 to OFF, and the alarm relay operates. The fan alarm override switch on the FSP faceplate breaks the connection between pins 9 and 12. This action overrides the fan alarm. The fan fail lamp glows. The main alarm does not activate because the link to D8 is not present.

Capacitor C1 prevents radio frequency (RF) instability.

Drive circuit

Transistor Q5 controls the drive to one of the power converters. When you press the converter reset button, the system applies a ground to the RESET A input. This event changes Q5 to ON. The system supplies the -60V DRIVE signal to the converter over the collector of Q5.

Capacitor C2 prevents high frequency instability.

Transistor Q6 and associated components provide the same function as transistor Q5 to control the second power converter.

2 NT1Xnnaa

NT1X00AA through NT1X90BA

NT1X00AA

Product description

The card for the NT1X00AA 102 test trunk circuit pack provides a 1004-Hz digital tone or a quiet termination for maintenance applications. These applications are in a DMS-100 office. The card contains one test circuit that can connect to one or two trunks.

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The digital tone is in a ROM circuit. The MTM controller controls the digital tone through the trunk logic circuits (TLC). The TLCs serve as buffers for control and data signals between the MTM and the NT1X00AA.

Functional blocks

The following functional blocks make up the NT1X00AA

- two identical TLCs
- address counter
- ROM circuit
- output buffer

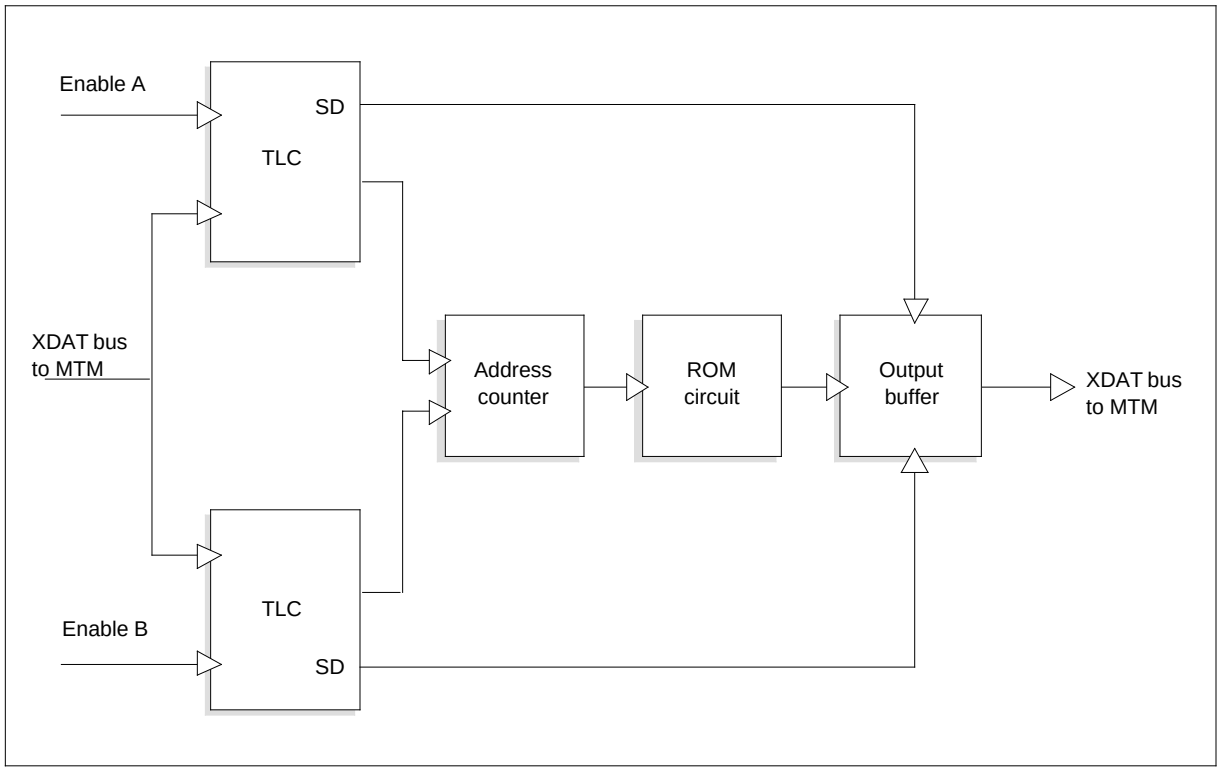
The TLC receives a signal on one of the allow lines to indicate that the TLC must start the required test. The TLC passes the request to the address counter. The address counter activates the ROM to issue the test tone. The system sends ROM output to the output buffer. The output buffer converts the parallel data to serial data. The TLC uses the signal distribution (SD) point to send the digital tone over the transmit data (XDAT) bus. The TLC can use the SD to select a quiet termination. When the SD point is active, the system sends the tone. When the SD point is not active, the test circuit ends in a quiet termination.

The standard test sequence follows:

- SD=0 (no tone) for 200 ms
- SD=1 (tone present) for 9 s
- SD=0 (no tone) until disconnected or SD=1 is programmed

The relationship between the functional blocks appears in the following figure.

NT1X00AA functional blocks



Technical data

The NT1X00AA provides a tone of 1004 Hz ±0.02 Hz at 0 dBm ±0.01 dB. The level stability is zero variation.

The quiet termination condition provides a code for zero pulse code modulation (PCM).

Power requirements

The power requirements for the NT1X00AA appear in the following table.

Power requirements

Voltage	Current
±5 V	520 mA
±12 V	7 mA
-15 V	3 mA

NT1X00AB

Product description

The NT1X00AB 102 test trunk card provides a 1004 Hz digital tone or a quiet termination for maintenance applications. These applications are in a DMS-100 office. The card contains one test circuit that can connect to one or two trunks.

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The digital tone is in a ROM circuit. The MTM controller controls the digital tone through the trunk logic circuits (TLC). The TLCs serve as buffers for control and data signals between the MTM and the NT1X00AB.

Functional blocks

The following functional blocks make up the NT1X00AB:

- two identical TLCs
- address counter
- ROM circuit
- output buffer

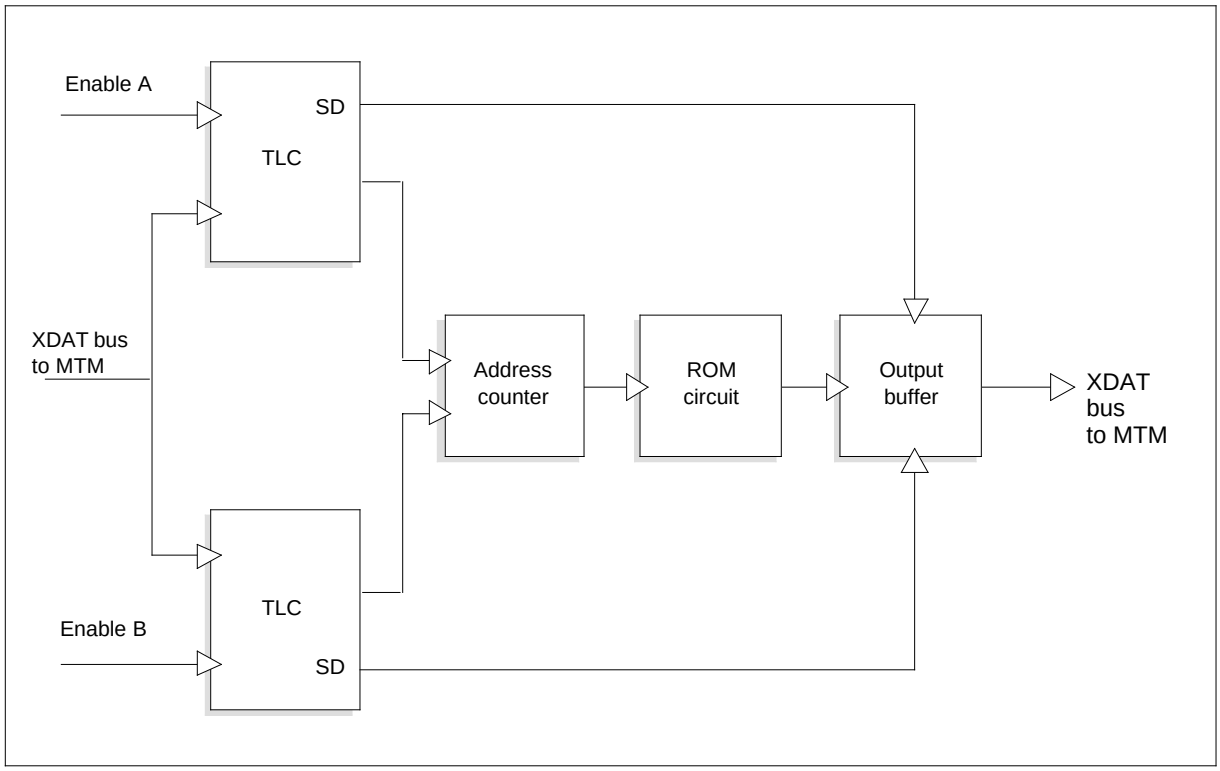
The TLC receives a signal on one of the allow lines. The signal indicates that the TLC must start the required test. The TLC passes the request to the address counter. The address counter activates the ROM to issue the test tone. The system sends the ROM output to the output buffer. The output buffer converts the parallel data to serial data. The TLC uses the signal distribution (SD) point to send the digital tone over the transmit data (XDAT) bus, or to select a quiet termination. When the SD point is not active, the test circuit ends in a quiet termination. The contains scan points to verify that the SD point is correctly set.

The standard test sequence follows:

- SD=0 (no tone) for 200 ms
- SD=1 (tone present) for 9 s
- SD=0 (no tone) until disconnected or SD=1 is programmed

The relationship between the functional blocks appears in the following figure.

NT1X00AB functional blocks



Technical data

The NT1X00AB provides a tone of 1004 Hz ±0.02 Hz at 0 dBm ±0.01 dB. The level stability is zero variation.

The quiet termination condition provides a code for zero pulse code modulation (PCM).

Power requirements

The power requirements for the NT1X00AB appear in the following table.

Power requirement

Voltage	Current
±5 V	520 mA
±12 V	7 mA
-15 V	3 mA

NT1X00AC

Product description

The NT1X00AC receiver off-hook tone card provides a receiver off-hook (ROH) digital tone or a quiet termination for maintenance applications. These applications are in a DMS-100 office. The card contains one test circuit that can connect to one or two trunks.

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The digital tone is in a ROM circuit. The MTM controller controls the digital tone through the trunk logic circuits (TLC). The TLCs serve as buffers for control and data signals between the MTM and the NT1X00AC.

Functional blocks

The following functional blocks make up the NT1X00AC

- two identical TLCs
- address counter
- ROM circuit
- output buffer

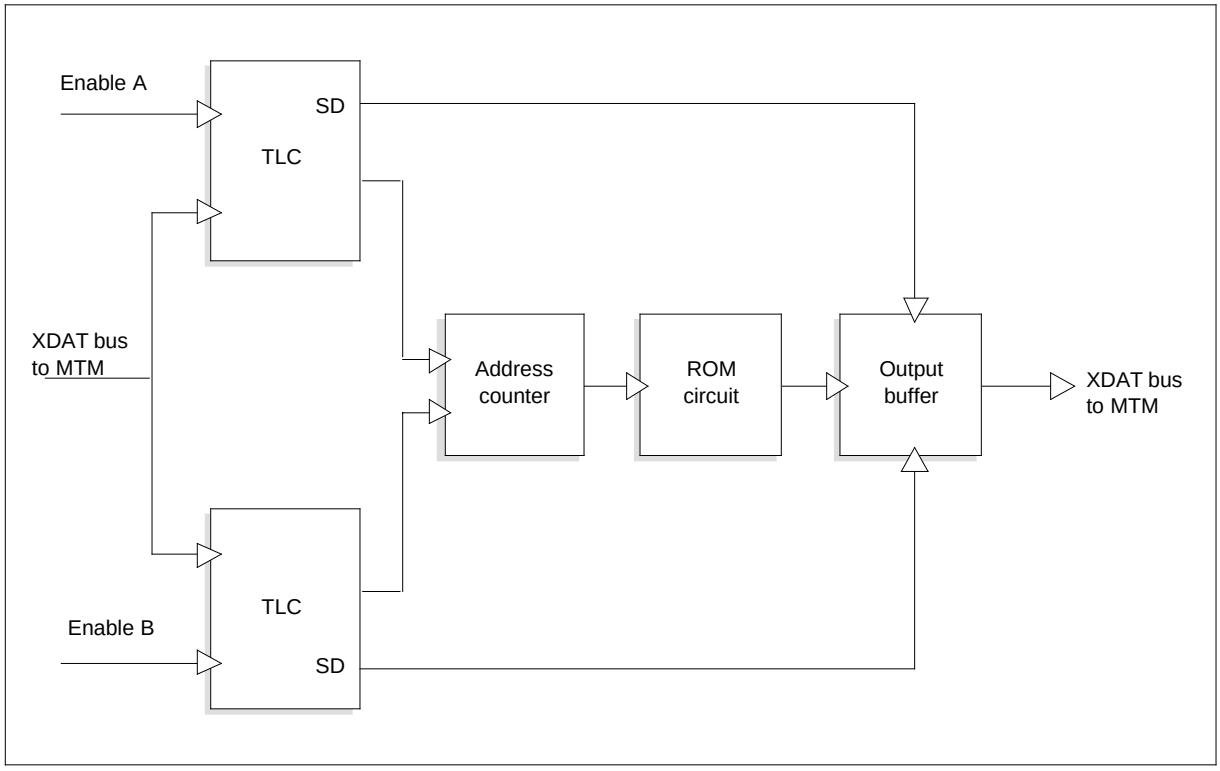
The TLC receives a signal on one of the enable lines. The signal indicates the TLC must start the required test. The TLC passes the request to the address counter. The address counter activates the ROM to issue the test tone. The system sends ROM output to the output buffer. The output buffer converts the parallel data to serial data. The TLC uses the signal distribution (SD) point to send the digital tone over the transmit data (XDAT) bus. The TLC can use the SD point to select a quiet termination. When the SD point is active, the system sends the tone. When the SD point is not active, the test circuit ends in a quiet termination. The NT1X00AC contains scan points to verify that the SD point is correctly set.

The standard test sequence follows:

- SD=0 (no tone) for 200 ms
- SD=1 (tone present) for 9 s
- SD=0 (no tone) until disconnected or SD=1 is programmed

The relationship between the functional blocks appears in the following figure.

NT1X00AC functional blocks



Technical data

The NT1X00AC provides an ROH tone. The ROH tone combines tones of 1404 Hz, 2060 Hz, 2452 Hz and 2604 Hz, at a level of -6.25 dBm for each frequency. This action creates a total level of 0.4 dBm. The total harmonic distortion is -24 dBm.

The quiet termination condition provides a code for zero pulse code modulation (PCM).

Power requirements

The power requirements for the NT1X00AC appear in the following table.

Power requirements

Voltage	Current
+5 V	520 mA
+12 V	7 mA
-15 V	3 mA

NT1X00AD

Product description

The NT1X00AD receiver off-hook tone card provides a receiver off-hook (ROH) digital tone or a quiet termination for maintenance applications. The applications are in a DMS-100 office. The card can contain one test circuit that can connect to one or two trunks.

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The read-only memory (ROM) circuit contains the digital tone. The MTM controller controls the digital tone through the trunk logic circuits (TLC). The TLCs serve as buffers for control and data signals between the MTM and the NT1X00AD.

Functional blocks

The NT1X00AD contains the following functional blocks:

- two identical TLCs
- address counter
- ROM circuit
- output buffer

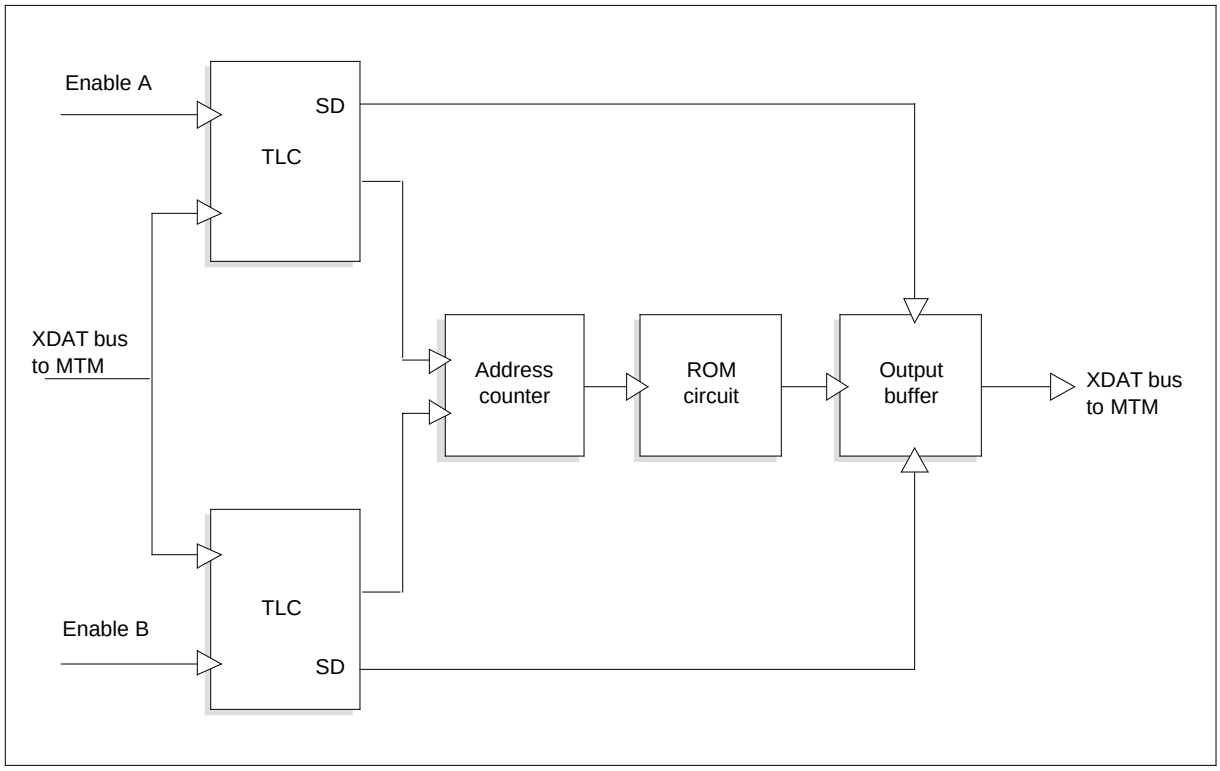
The TLC receives a signal on one of the allow lines. The signal indicates the TLC must start the required test. The TLC passes the request to the address counter. The address counter activates the ROM to issue the test tone. The system sends ROM output to the output buffer. The output buffer converts the parallel data to serial data. The TLC uses the signal distribution (SD) point to send the digital tone over the transmit data (XDAT) bus. The TLC also uses the SD point to select a quiet termination. If the SD point is active, the system sends the tone out. If the SD point is not active, the test circuit ends in a quiet termination.

The standard test sequence is as follows:

- SD=0 (no tone) for 200 ms
- SD=1 (tone present) for 9 s
- SD=0 (no tone) until disconnected or SD=1 is programmed

The relationship between the functional blocks appears in the following figure.

NT1X00AD functional blocks



Technical data

The NT1X00AD provides an ROH tone. The ROH tone combines tones of 1404 Hz, 2060 Hz, 2452 Hz and 2604 Hz, at a level of -6.25 dBm for each frequency. This action creates a total level of 0.4 dBm. The total harmonic distortion is -24 dBm.

The quiet termination condition provides a zero pulse code modulation (PCM) code.

Power requirements

The power requirements for the NT1X00AD appear in the following table.

Power requirements

Voltage	Current
+5 V	520 mA
+12 V	7 mA
-15 V	3 mA

NT1X00AE

Product description

The NT1X00AE international 102 test trunk card provides a 1020 Hz digital tone or a quiet termination for maintenance applications. The maintenance applications are for a DMS-100 office. The card contains one test circuit that connects to one or two trunks. The NT1X00AE is designed for international 102 test trunks.

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The read-only memory (ROM) circuit contains the digital tone. The MTM controller controls the digital tone through the trunk logic circuits (TLC). The TLCs act as buffers for control and data signals between the MTM and the NT1X00AE.

Functional blocks

The NT1X00AE contains the following functional blocks:

- two identical TLCs
- address counter
- ROM circuit
- output buffer

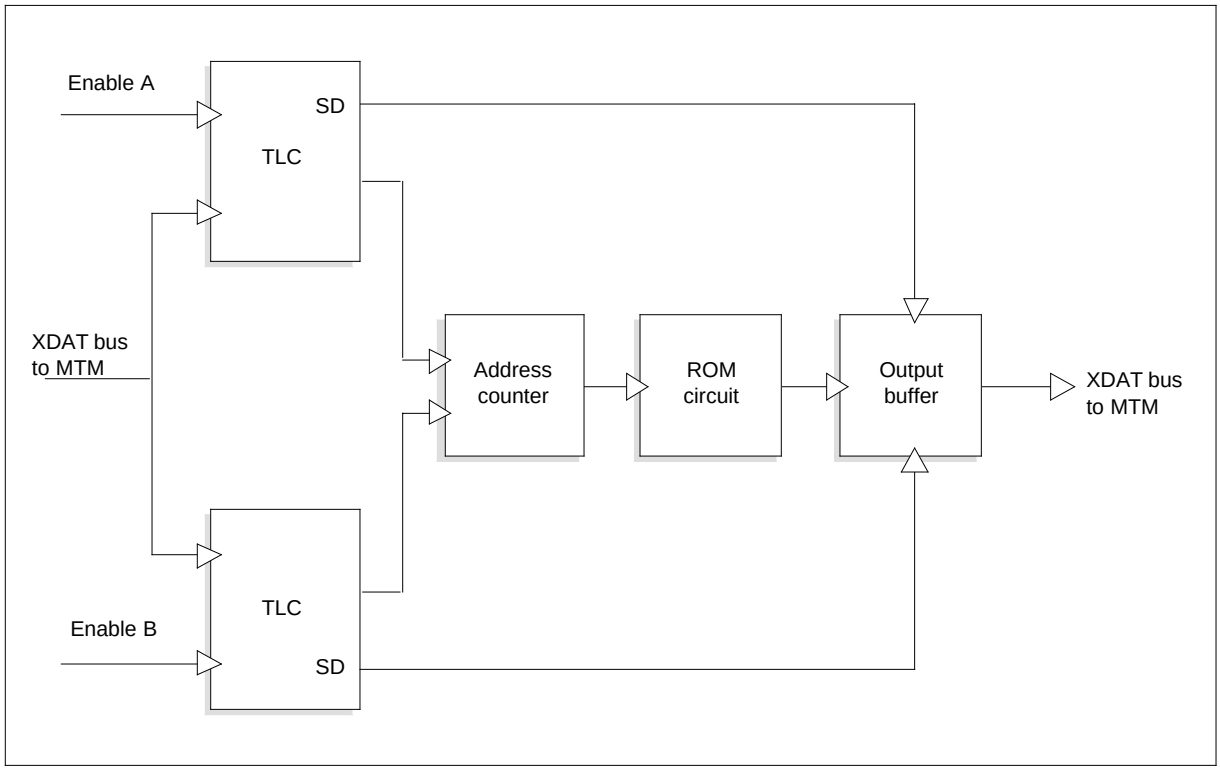
The TLC receives a signal on one of the enable lines. The signal indicates the TLC must start the required test. The TLC sends the request to the address counter. The address counter activates the ROM to issue the test tone. The system sends the ROM output to the output buffer. The output buffer converts the parallel data to serial data. The TLC uses the signal distribution (SD) point to send the digital tone over the transmit data (XDAT) bus. The TLC also uses the SD to select a quiet termination. If the SD point is active, the system sends the the tone out. If the SD point is not active, the test circuit ends in a quiet termination.

The standard test sequence is as follows:

- SD=0 (no tone) for 200 ms
- SD=1 (tone present) for 9 s
- SD=0 (no tone) until disconnected or SD=1 is programmed

The relationship between the functional blocks appears in the following figure.

NT1X00AE functional blocks



Technical data

The NT1X00AE provides a tone of 1020 Hz ±0.02 Hz at -10 dBm ±0.01 dB. The level stability is zero variation.

The quiet termination condition provides a zero pulse code modulation (PCM) code.

Power requirements

The following table lists the power requirements for the NT1X00AE .

Power requirements

Voltage	Current
+5 V	520 mA
+12 V	7 mA
-15 V	3 mA

NT1X00AF

Product description

The NT1X00AF 102 terminating -10dB test line card provides a 1004-Hz digital tone or a quiet termination for maintenance applications. The maintenance applications are for a DMS-100 office. The card contains one test circuit that connects to one or two trunks. The NT1X00AF is designed to terminate a 102 test trunk at a -10dB level.

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The read-only memory (ROM) circuit contains the digital tone. The MTM controller controls the digital tone through the trunk logic circuits (TLC). The TLCs serve as buffers for control and data signals between the MTM and the .

Functional blocks

The NT1X00AF contains the following functional blocks:

- two identical TLCs
- address counter
- ROM circuit
- output buffer

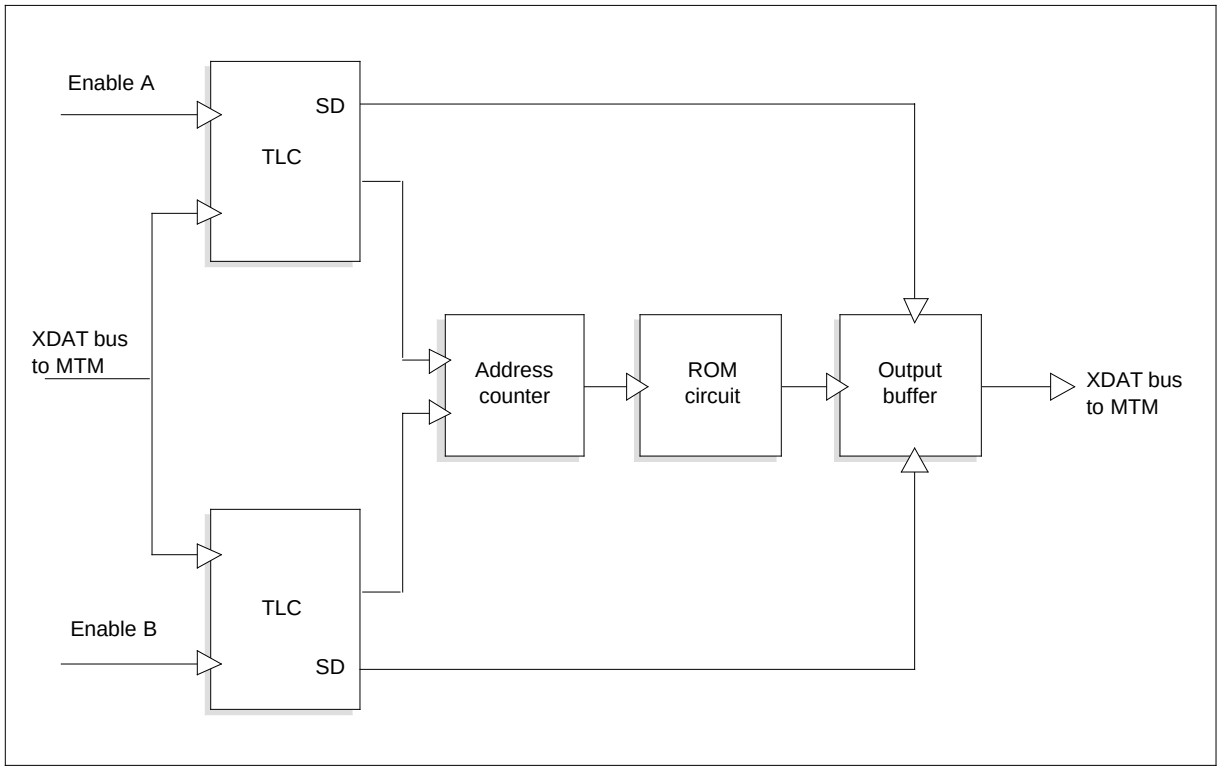
The TLC receives a signal on one of the enable lines. The signal indicates the TLC must start the required test. The TLC sends the request to the address counter. The address counter activates the ROM to issue the test tone. The system sends the ROM output to the output buffer. The output buffer converts the parallel data to serial data. The TLC uses the signal distribution (SD) point to send the digital tone over the transmit data (XDAT) bus. The TLC uses the SD to select a quiet termination. If the SD point is active, the system sends the tone out. If the SD point is not active, the test circuit ends in a quiet termination.

The standard test sequence is as follows:

- SD=0 (no tone) for 200 ms
- SD=1 (tone present) for 9 s
- SD=0 (no tone) until disconnected or SD=1 is programmed

The relationship between the functional blocks appears in the following figure.

NT1X00AF functional blocks



Technical data

The NT1X00AF provides a tone of 1004 Hz ±0.02 Hz at -10 dBm ±0.01 dB. The level stability is zero variation.

The quiet termination condition provides a zero pulse code modulation (PCM) code.

Power requirements

The following table lists the power requirements for the NT1X00AF.

Power requirements

Voltage	Current
+5 V	520 mA
+12 V	7 mA
-15 V	3 mA

NT1X00AG

Product description

The NT1X00AG 102 terminating -20dB test line card provides a 1004 Hz digital tone or a quiet termination. The test card provides these features for maintenance applications in a DMS-100 office. The card contains one test circuit that connects to one or two trunks. The NT1X00AG is designed to terminate a 102 test trunk at a -20dB level.

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The read-only memory (ROM) circuit contains the digital tone. The MTM controller controls the digital tone through the trunk logic circuits (TLC). The TLCs act as buffers for control and data signals between the MTM and the NT1X00AG.

Functional blocks

The NT1X00AG contains the following functional blocks:

- two identical TLCs
- address counter
- ROM circuit
- output buffer

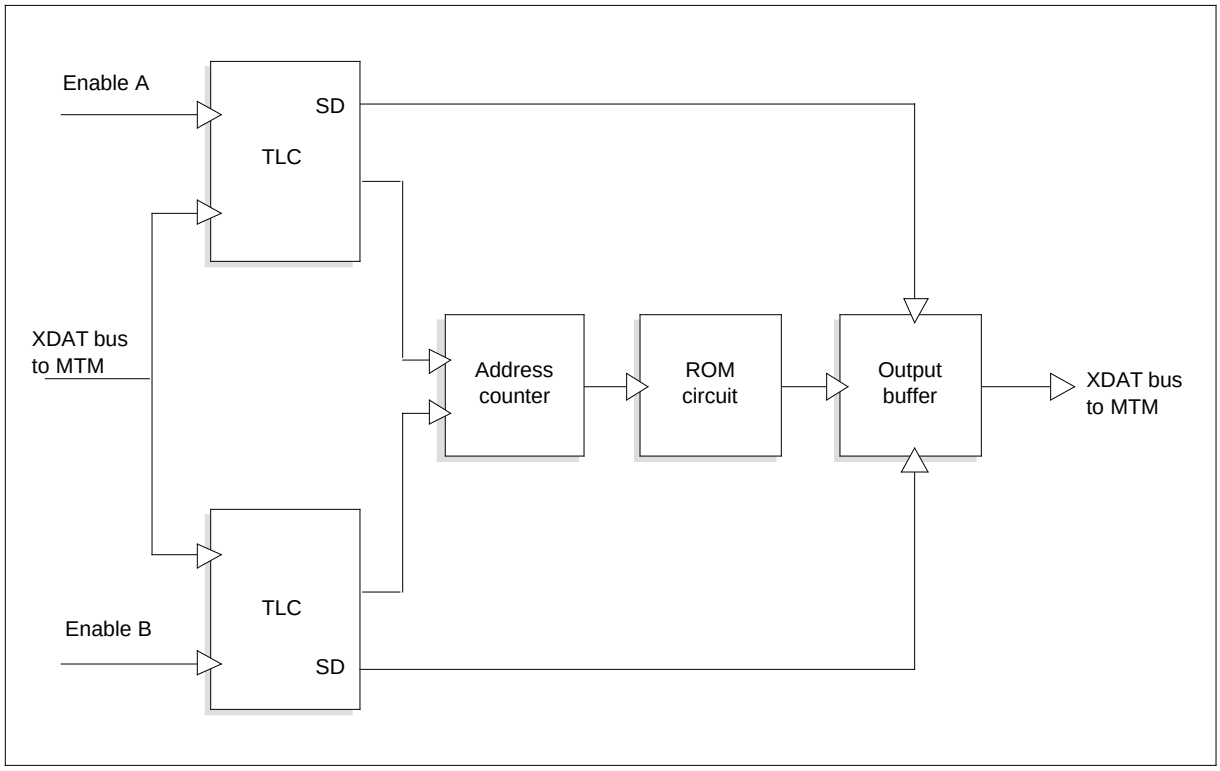
The TLC receives a signal on one of the enable lines. The signal indicates the TLC must start the required test. The TLC sends the request to the address counter. The address counter activates the ROM to issue the test tone. The system sends the ROM output to the output buffer. The output buffer converts the parallel data to serial data. The TLC uses the signal distribution (SD) point to send the digital tone over the transmit data (XDAT) bus. The TLC also uses the SD to select a quiet termination. If the SD point is active, the system sends the tone out. If the SD point is not active, the test circuit ends in a quiet termination.

The standard test sequence is as follows:

- SD=0 (no tone) for 200 ms
- SD=1 (tone present) for 9 s
- SD=0 (no tone) until disconnected or SD=1 is programmed

The relationship between the functional blocks appears in the following figure.

NT1X00AG functional blocks



Technical data

The NT1X00AG provides a tone of 1004 Hz ±0.02 Hz at -20 dBm ±0.01 dB. The level stability is zero variation.

The quiet termination condition provides a zero pulse code modulation (PCM) code.

Power requirements

The following table lists the power requirements for the NT1X00AG.

Power requirements

Voltage	Current
+5 V	520 mA
+12 V	7 mA
-15 V	3 mA

NT1X00AH

Product description

The NT1X00AH 102 terminating -15dB test line card provides a 1004 Hz digital tone or a quiet termination. The test card provides these features for maintenance applications in a DMS-100 office. The card contains one test circuit that can connect to one or two trunks. The NT1X00AH is designed to terminate a 102 test trunk at a -15dB level.

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The read-only memory (ROM) circuit contains the digital tone. The MTM controller controls the digital tone through the trunk logic circuits (TLC). The TLCs act as buffers for control and data signals between the MTM and the NT1X00AH.

Functional blocks

The NT1X00AH contains the following functional blocks:

- two identical TLCs
- address counter
- ROM circuit
- output buffer

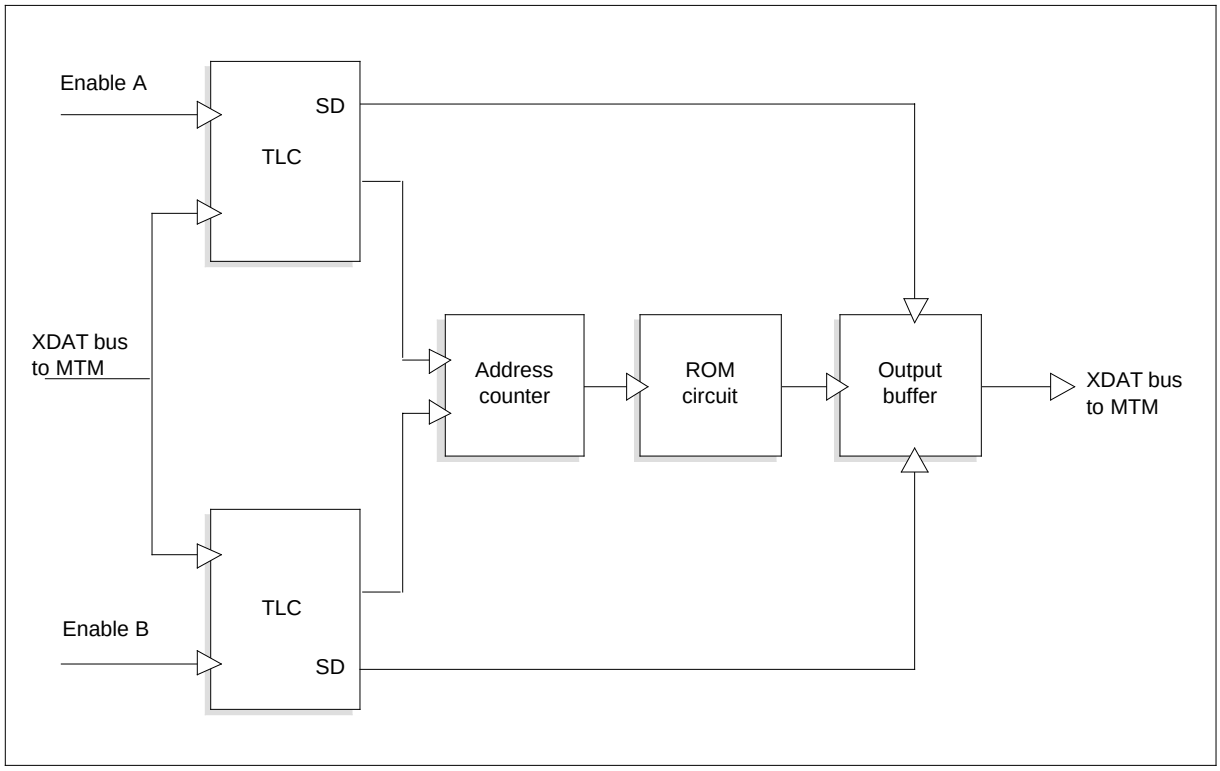
The TLC receives a signal on one of the enable lines. The signal indicates the TLC must start the required test. The TLC sends the request to the address counter. The address counter activates the ROM to issue the test tone. The system sends the ROM output to the output buffer. The output buffer converts the parallel data to serial data. The TLC uses the signal distribution (SD) point to send the digital tone over the transmit data (XDAT) bus. The TLC also uses the SD to select a quiet termination. If the SD point is active, the system sends the tone out. If the SD point is not active, the test circuit ends in a quiet termination.

The standard test sequence is as follows:

- SD=0 (no tone) for 200 ms
- SD=1 (tone present) for 9 s
- SD=0 (no tone) until disconnected or SD=1 is programmed

The relationship between the functional blocks appears in the following figure.

NT1X00AH functional blocks



Technical data

The NT1X00AH provides a tone of 1004 Hz ±0.02 Hz at -15 dBm ±0.01 dB. The level stability is zero variation.

The quiet termination condition provides a zero pulse code modulation (PCM) code.

Power requirements

The following table lists the power requirements for the NT1X00AH.

Power requirements

Voltage	Current
+5 V	520 mA
+12 V	7 mA
-15 V	3 mA

NT1X31AA

Product description

The NT1X31AA conference circuit card processes three-party conference calls for the DMS-100. Each card can accommodate two three-party conference calls.

Location

The NT1X31AA occupies one card position in the maintenance trunk module (MTM) or trunk module (TM). Six trunks are connected to the card.

Functional description

To process conference calls, the NT1X31AA switches speech samples at the pulse code modulation (PCM) rate between the conference parties. The card samples all three parties. The largest sample, which corresponds to the talking party, is sent to the other two parties. The parties involved do not hear the switching because the sampling rate is too high.

Functional blocks

Both conference circuits on the NT1X31AA contains the following functional blocks:

- three identical trunk logic circuits (TLC)
- comparator

TLC

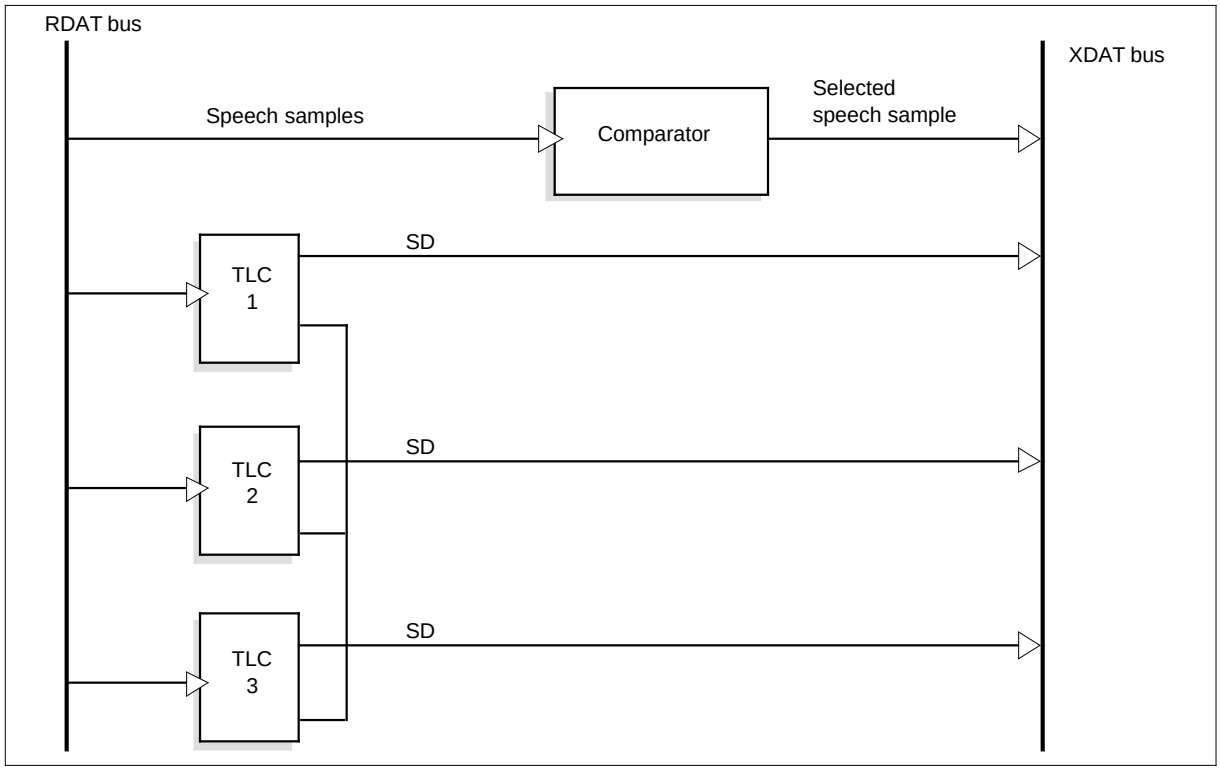
Each TLC provides timing signals to one of the three ports in the conference circuit. Each TLC has a signal distribution (SD) point. The SD point is monitored through the transmit data (XDAT) bus to verify the connections between PCM channels and conference circuit ports.

Comparator

The speech samples from each of the three parties enter the card through the receive data (RDAT) bus. The speech samples are sent to the comparator circuit. The comparator compares the samples from two of the parties. The comparator sends the largest sample through the XDAT bus to the third party. This comparison occurs for each of the three parties. The switching of speech samples takes place at the PCM sampling rate. The parties involved do not hear the speech samples.

The relationship between the functional blocks appears in the following figure.

NT1X31AA functional blocks



Technical data

Dimensions

The dimensions of the NT1X31AA circuit card are as follows:

- height: 317 mm (12.5 in.)
- depth: 254 mm (10 in.)

Power requirements

The following table lists the power requirements for the NT1X31AA.

Power requirements

Voltage	Current
+5 V	520 mA
+12 V	25 mA
-15 V	7 mA

NT1X33AA

Product description

The NT1X33AA processor interface (PI) administers the central message controller (CMC) end of the central processor (CP) to CMC interface. The processor interface allows the CMC to appear on the data port of each CP.

A data port extender card (NT1X51AA) in the CP shelf provides an interface between the CP and the two CMCs. The extender card recognizes when a CMC is addressed and enables communication between the CP and the addressed CMC.

The ROM sequencer drives the NT1X33AA.

Location

The NT1X33AA resides in the CMC.

Functional description

The NT1X33 extends the read or write operations to the rest of the CMC cards. The NT1X33 completes the read or write sequence to the CP. The NT1X33AA calculates the odd parity bit over address and data on write operations. The NT1X33 informs the CP if a parity error is present. The state of the CPs and the CMC determines if the NT1X33AA can selectively communicate with CPs.

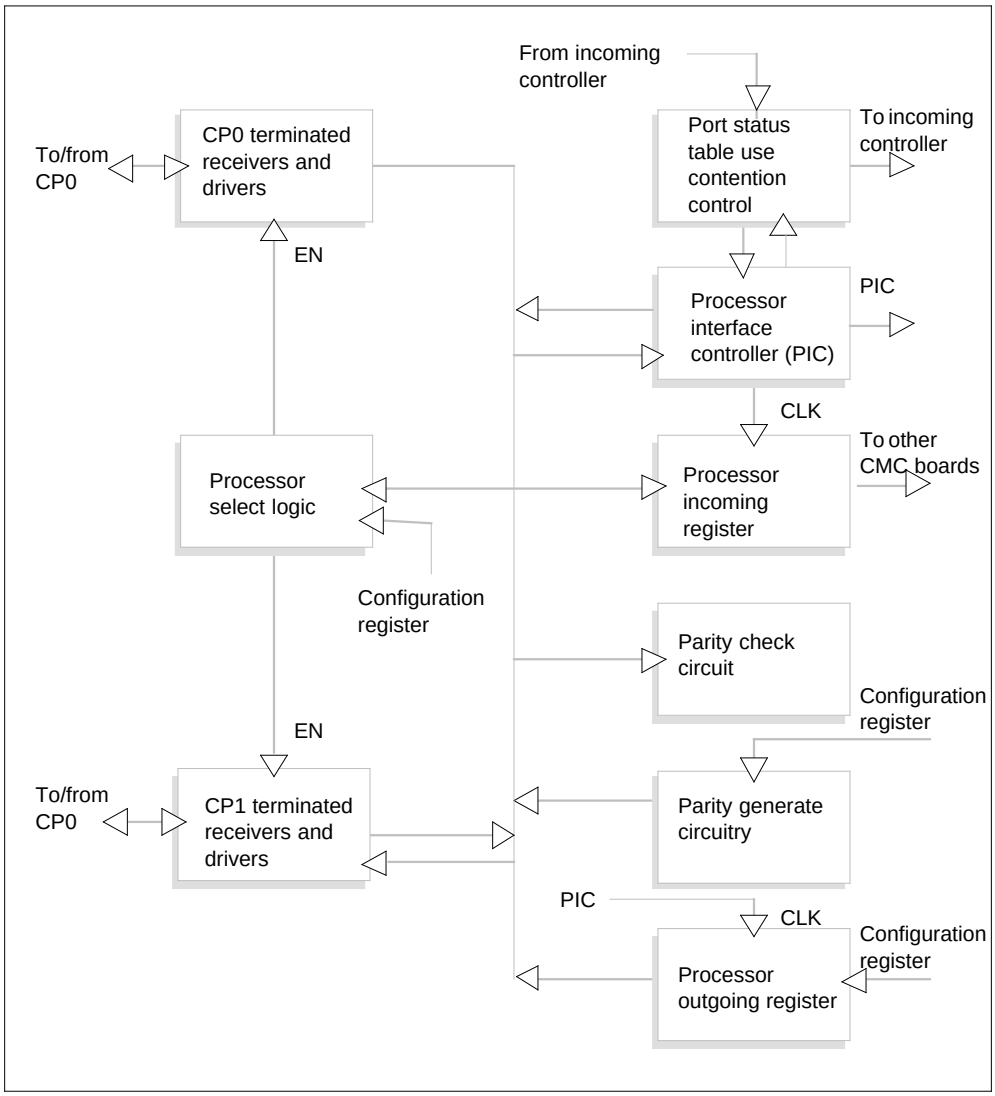
Functional blocks

The NT1X33AA contains the following functional blocks:

- CP0 terminated receivers and drivers (TRD0)
- CP1 terminated receivers and drivers (TRD1)
- processor select logic (PSL)
- port status table use contention control (PUCC)
- processor interface controller (PIC)
- processor incoming register (PIR)
- parity check circuit (PCC)
- parity generate circuit (PGC)
- processor outgoing register (POR)

The functional relationship between blocks appears in the following figure.

NT1X33AA functional blocks



CP0 terminated receivers and drivers

The TRD0 circuit terminates the bus from the CMC interface card to CP0. This bus includes a bidirectional data bus, a one-directional address bus and control signals. The control signals are parity, input/output (I/O) synchronization, read, write, reset, processor sync, activity dunit, and I/O interrupt.

The bus uses twisted pair leads. One side carries the signal and the other side carries the backplane ground. The processor select logic circuits control the bus.

NT1X33AA (continued)

CP1 terminated receivers and drivers

The CP1 terminated receivers and drivers (TRD1) circuit terminates the bus from the CMC interface card to CP1. The TRD1 functions like the TRD0.

Processor select logic

The PSL enables the TRD0 and TRD1 circuits. The following conditions determine if TRD0 and TRD1 can be enabled:

- CMCMODE (online or offline)
- activity status of the CP
- a read signal is present
- synchronization status of the CP (in or out of synchronization)

The active CP normally drives the CMC and is online. If the CPs operate in synchronization, only the TRD that connects to the active CP can receive information. Both TRDs can drive information back to both CPs. This information is the data lines, the dunit line and I/O interrupt line. If the two CPs are out of synchronization, only the TRD that connects to the active CP can drive information back.

The inactive CP drives an offline CMC. If the CPs operate in synchronization, only the TRD that connects to the inactive CP can receive information. Both TRDs can drive information back to both CPs. If the CPs are out of synchronization, only the TRD that connects to the inactive CP can drive information back.

Port status table use contention control

The PUCC regulates access to the port status table (PST) between the CP and the incoming controller (IC). The CP accesses the PST to initialize and update the PST and the IC to determine the ports to scan. To use the PST, the CP or IC must request permission from the PUCC. If the CP and IC post requests at the same time for the PST, the CP has priority.

Processor interface controller

The PIC follows standard data port protocol in communications with the CP. The sequencer receives input data from the register and multiplexer. The PIC differentiates between a PST write and non-PST write operation. The PIC differentiates between a PST read, a message buffer read and other types of read operation.

Processor incoming request

The PIR register stores the address and data information from the CP for the CMC to use. The PIC clocks the address and data information to the PIR

registers. The PIC performs this function when a read or write operation occurs for the CMC.

Parity check circuit

The PCC calculates the odd parity for the address and data the PCC receives from the CP in a write operation. The PCC compares the calculated parity with the odd parity bit the CP presents. If the received and calculated parity are the same, the write operation occurs. If the received and calculated parity are different, the external write operation is completed to the CP. The internal write operation does not complete.

If a parity error occurs, a parity interrupt is posted to the CP. The write operations are treated as if parity errors are present until the CP clears the parity interrupt. Two types of operations are not treated as if parity errors are present. These include:

- the operations that clear the parity interrupt
- the operations that make the CMC maintenance busy, or if the CMC is already maintenance busy

Parity generate circuit

The PGC calculates the odd parity bit for transmission to the CP in a read operation. The CFR2 can be manipulated to invalidate the parity that transmits to the CP. This feature is for test purposes only.

Processor outgoing register

The POR receives the data and parity status line from the CMC on a read operation. The POR consists of six buffers. Three (POR0) are assigned to TRD1 and three (POR1) are assigned to TRD1. If a synchronization signal and a read signal are present, POR0 and POR1 are enabled. If these signals are not present, the CPs and the CMCMODE signal activity modes determine how the POR0 and POR1 are enabled. If the CPs are out of synchronization, the offline CMC responds to the inactive CP and the online CMC responds to the active CP.

Signaling

The interface to the CMC side of the processor interface (PI) contains incoming data, address, control signal buses and outgoing data buses. The sequencer action of the PI causes the buses to operate in synchronization. The cabling is twisted pair. One half of the pair carries the ground and the other half carries the signal.

NT1X33AA (end)

Protocol

Communications between the CMC and the CP follow standard data port protocol.

Technical data

Power requirements

The input power to this card is fused to the paddle board with an axial lead fuse. A light-emitting diode (LED) mounted on the faceplate of a visual fuse alarm circuit indicates when a fuse is open.

The NT1X33AA operates with +5V at 3.8A (standard).

NT1X35

Product description

The NT1X35 central message controller interface card is in the central message controller (CMC) shelf.

The NT1X35 handles the message transfer sequence for all messages from a peripheral processor to the central processor (CP). These messages are incoming messages. The controller can store a variable length message a maximum of 256 bytes. Each byte has eight bits. The controller validates the checksum of the message and reports errors during the message transfer sequence.

The incoming controller (IC) can scan for incoming messages on 70 peripheral ports. The sequencer drives the IC.

Functional description

Functional blocks

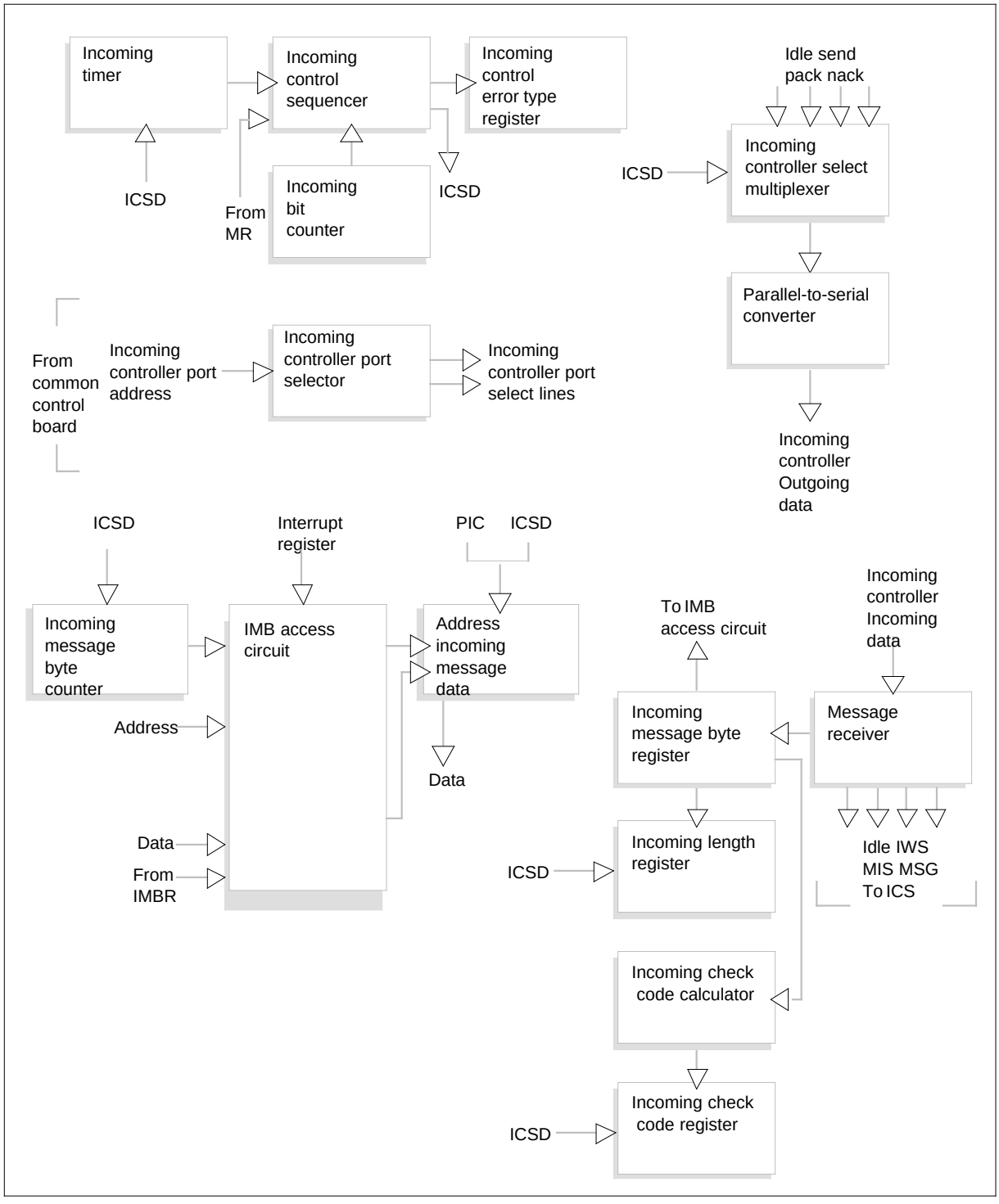
The NT1X35 contains the following functional blocks:

- incoming controller sequencer (ICS)
- incoming timer (IT)
- incoming controller error type register (ICETR)
- incoming bit counter (IBC)
- incoming controller select multiplexer (ICSM)
- parallel-to-serial converter (PSC)
- incoming message byte counter ((IMBC)
- incoming message buffer access circuit (IMBAC)
- incoming message buffer (IMB)
- message receiver (MR)
- incoming message byte register (IMBR)
- incoming length register (ILR)
- incoming check code calculator (ICC)
- incoming check code register (ICCR)
- incoming controller port selector (ICPS)

The following figure shows the relationship of these parts.

NT1X35 (continued)

NT1X35 functional blocks



Incoming controller sequencer

The ICS handles the message transfer sequence from a peripheral to the CP. The ICS outputs information to other functional blocks as incoming controller sequence data (ICSD).

Incoming timer

The IT scans a peripheral port for 40 &0xb5;s during a scan sequence and waits for a MAY I SEND (MIS), I WILL SEND (IWS) or an IDLE message.

Incoming controller error type register

As the ICETR performs the message transfer sequence with the peripheral. The ICETR checks the stages of the message transfer sequencer. The ICETR checks for problems in the message transfer sequencer protocol.

Incoming bit counter

The IBC informs the sequencer at which bit of the byte the sequencer works. The output of the IBC determines the bit relationship of the IC incoming data stream.

Incoming controller select multiplexer

The ICSM determines which of the four control messages to send on the IC outgoing data stream to a peripheral. The four control messages are IDLE, SEND, POSITIVE ACKNOWLEDGMENT (PACK) and NEGATIVE ACKNOWLEDGMENT (NACK).

Parallel-to-serial converter

The PSC feeds a data stream forward to the peripheral interface card.

Incoming message byte counter

The IMBC keeps track of the number of the incoming message byte. This message byte is received for the ICS. The message byte provides the incoming message buffer (IMB) with the address required to write a byte of incoming message data into the IMB.

Incoming message buffer access circuit

The IMBAC gives the IMBC address lines and incoming message bytes access to the outgoing message buffer to write the outgoing message buffer. The IMBAC gives the CP address lines and the CP data lines the ability to read or write the outgoing message buffer (OMB).

Incoming message buffer

The IMB stores the incoming message bytes.

NT1X35 (end)

Message receiver

The MR receives the serial IC incoming data stream and decodes four message types: IDLE, MIS, IWS and MESSAGE (MSG).

Incoming message byte register

The IMBR latches in the most important eight bits of the incoming message byte.

Incoming length register

The ILR stores the length of the incoming data message. The outputs of the ILR are compared to the values of the IMBC. When these two values are equal, the comparator signals the ICS that this byte of the incoming message is the last one.

Incoming check code calculator

The ICC adds a message byte of data to a running binary sum of the previous bytes of data.

Incoming check code register

The ICCR stores the last byte of the incoming message and the checksum for the entire message from the ICC. If the checksums are equal, a checksum signal is sent to the ICS.

Incoming controller port selector

The ICPS selects the ports for the IC.

Technical data

Power requirements

The input power to this card is fused to the paddle board with an axial lead fuse. A light-emitting diode (LED) mounted on the faceplate of a visual fuse alarm circuit indicates when a fuse is open.

NT1X36AA

Product description

The NT1X36AA central message controller (CMC) peripheral interface card provides a link for data and control messages. The link occurs between the DMS-100 switch CMC and the peripheral controllers that perform network or input/output (I/O) functions.

The card contains five separate and identical circuits.

Location

The card occupies one position in the CMC shelf.

Functional description

The NT1X36AA card uses signal conversions, data alignment, and gates to receive and send data from the CMC and the peripheral controllers. The card interacts with the CMC controller with five serial data lines, 12 control lines and three clock lines. The card interacts with the peripheral controller and uses a maximum of five pairs of one-directional, serial, ac-coupled lines. A biphase transmission code with a biphase code violation indicates the frame pulse.

Functional blocks

Each circuit in the NT1X36AA contains the following functional blocks:

- logic gate
- DATA gate
- frame pulse inserter
- transistor-transistor logic (TTL)/biphase converter
- biphase driver
- biphase receiver
- clock extractor
- frame pulse extractor
- biphase/TTL converter
- phase aligner
- two AND gates

Logic gate

The logic gate receives port selection signals from the CMC incoming (IC) and outgoing (OG) controller ports. The logic gate uses a port select signal to determine which peripheral port receives the data.

NT1X36AA (continued)

DATA gate

The DATA gate receives 2.56 Mbps TTL format data and idle messages from the CMC IC and OG controllers. The following table lists the messages and their meanings.

Idle messages

Message	Meaning
Low priority idle	Continuously transmits over serial links when data does not transmit.
High priority idle	Transmits to peripherals. Indicates that only high priority data be sent to the CMC.
May I send (MIS)	Indicates a request to transmit data.
Send	Indicates data ready to be received.
Positive acknowledge (PACK)	Acknowledges successful data transmission.
Negative acknowledge (NACK)	Indicates data transmission not successful.
Data message	Indicates the start of a data message.
I will send (IWS)	Informs the CMC that the peripheral cannot accept a message from the CMC

Frame pulse inserter

The frame pulse inserter receives data from the DATA gate and inserts a 125 ms frame pulse signal. The frame pulse inserter sends the data to the TTL/biphase converter.

TTL/biphase converter

The TTL/biphase converter changes the data from a TTL format to a biphase signal format.

Biphase driver

The biphase driver receives the converted data from the TTL/biphase converter. The biphase driver uses control lines to send the data to the peripheral controller at a 2.048 Mbps rate. The driver divides the frame pulse into 32 10-bit channels. The driver inserts consecutive 8-bit data bytes into

consecutive 10-bit channels to transmit the data. Bit 1 is for a reset code and bit 0 is for the frame pulse.

Biphase receiver

The biphase receiver accepts 2.56 Mbps biphase data from the incoming path of the peripheral port and sends the data to the clock extractor.

Clock extractor

The clock extractor removes the clock signal from the data. The clock signal is aligned with the CMC clock and sends the data to the frame pulse extractor.

Frame pulse extractor

The frame pulse extractor receives the data from the clock extractor. The frame pulse extractor removes the 125µs frame pulse and sends the data to the biphase/TTL converter.

Biphase/TTL converter

The biphase/TTL converter changes biphase data received from the frame pulse extractor to TTL format.

Phase aligner

The phase aligner receives the data from the biphase/TTL converter and aligns the data to the CMC clock. The phase aligner sends the data to the AND gates for transmission to the CMC IC or CMC OG controller.

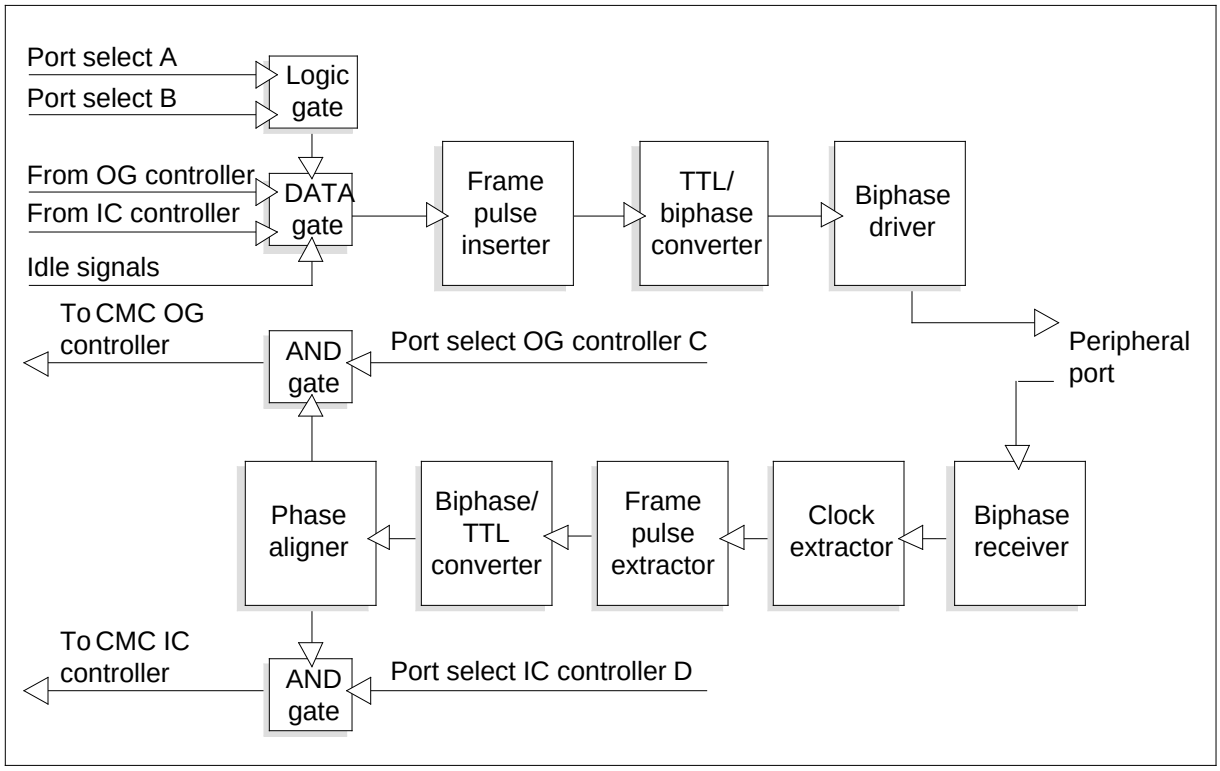
AND gate

The AND gates receive data from the phase aligner and the peripheral port select. If both signals are present, the gates send the data to the CMC OG or CMC IC controller.

The relationship between the functional blocks appears in the following figure.

NT1X36AA (continued)

NT1X36AA functional blocks



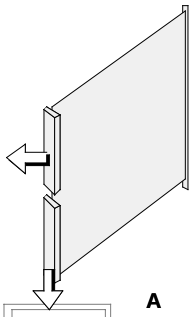
Signaling

Pin outs

The pin-out diagram for NT1X36AA the appears in the following figure.

NT1X36AA pin outs

	A	B
1A 1B	GND	GND
2A 2B	+5 V	+5 V
3A 3B	+5 V	+5 V
4A 4B	+5 V	+5 V
5A 5B	GND	GND
6A 6B	–5 V	–5 V
7A 7B	GND	GND
8A 8B		
9A 9B	GND	GND
10A 10B		
11A 11B	GND	ICBS-
12A 12B		
13A 13B		
14A 14B		
15A 15B		
16A 16B		
17A 17B		
18A 18B		
19A 19B		
20A 20B	GND	GND
21A 21B		GND
22A 22B		GND
23A 23B		
24A 24B		
25A 25B	GND	OCBS–
26A 26B		
27A 27B		
28A 28B		
29A 29B		
30A 30B	ISPS2–	ICPS1–
31A 31B		
32A 32B		
33A 33B	ICPS0–	ICOD–
34A 34B	ICID–	OCPS2-
35A 35B	OCPS1-	OCPS0-
36A 36B	IC-	OCOD-
37A 37B	RC0-	RC1-
38A 38B	RC2-	RC3-
39A 39B	FPIN5-	OCID-
40A 40B	PC390O0-	PC195-



	A	B
41A 41B	GND	GND
42A 42B	OBIPIN+	OBIPIN-
43A 43B	OBIPOUT+	OBIPOUT-
44A 44B		
45A 45B	1BIPIN+	1BIPIN-
46A 46B	1BIPOUT+	1BIPOUT-
47A 47B		
48A 48B		
49A 49B		
50A 50B	GND	GND
51A 51B	GND	GND
52A 52B		
53A 53B		
54A 54B		
55A 55B		
56A 56B		
57A 57B		
58A 58B		
59A 59B		
60A 60B	GND	GND
61A 61B	GND	GND
62A 62B		
63A 63B		
64A 64B		
65A 65B		
66A 66B		
67A 67B		
68A 68B		
69A 69B		
70A 70B	GND	GND
71A 71B	GND	GND
72A 72B		
73A 73B		
74A 74B		
75A 75B		
76A 76B		
77A 77B		
78A 78B		
79A 79B		
80A 80B	GND	GND

NT1X36AA (end)

Technical data

The cable attached to the NT1X36AA is a 26-gauge tight twist cable with 90- to 110W impedance. The twist cable has a maximum attenuation of 17 dB at 2.56 MHz. The maximum cable length from the CMC to the peripherals is 61 m (200 ft).

The receiver for the card has

- a receiver sensitivity of 0.25V peak to peak
- a maximum input voltage of 3.2V peak to peak
- a minimum 500Vdc input/output isolation through the transformer

Dimensions

The dimensions for the NT1X36AA are as follows:

- height: 31.75 cm (12.5 in.)
- depth: 24.5 cm (10 in.)
- width: 1.27 cm (0.5 in.)

Power requirements

Power status indicators on the faceplate glow if the supply to the +5V or -5V fuses is interrupted. The following table lists the power requirements for the NT1X36AA.

Power requirements

Voltage	Current	Tolerance
+5 V	2.5 A	+4.75 V to +5.25 V
-5 V	0.1 A	-4.75 V to -5.25 V

Product description

The common control (CC) card administers the activity between the incoming controllers (IC) and outgoing controllers (OC).

Registers in the CC card store the status of the central message controller (CMC) as the central processor (CP) determines. The IC and OC use these registers in message transfer sequences.

The CC logs the interrupts that the IC and OC post during a message transfer sequence (MTS) and forwards the interrupts to the CP. Primary clocking and timing signals for the CMC are taken from the CC card.

Functional description

Functional blocks

The NT1X37AA contains the following functional blocks:

- read/write locations accessible by the central processor
- outgoing message buffer (OMB)
- incoming message buffer (IMB)
- port status table (PST)
- command register (CDR)
- maximum port count register
- offline port address register (OPAR)
- readable locations
- configuration register
- peripheral reset register (PRR)
- message mode register (MMR)
- interrupt register
- mask register
- mask interrupt register
- read only locations
- parity error interrupt register
- clock interrupt
- outgoing controller error type register
- incoming controller error type register

NT1X37AA (continued)

- port counter (PC)
- address strap
- parity strap
- message transfer attempted flag
- clock generation
- outgoing port address register
- port use contention control

Port status table

The CP and IC access the PST to read and write the status of the 70 peripheral ports.

Command register

The CP uses the CDR to instruct the CMC to execute one of 39 commands.

Offline port address register

The OPAR contains the address in the PST that the CMC uses when the CMC is in an offline mode. The address in OPAR is the address that the IC and OC use when the CMC is offline.

Peripheral reset register

The active PRR informs the OC when a peripheral reset operation occurs. When the PRR clears, the PRR informs the OC when a message transfer to a peripheral occurs.

Message mode register

The active MMR indicates to the CMC to send the message in the OMB simplex. When the MMR clears, the MMR indicates to the CMC to send the message in the OMB duplex.

Port counter

The IC uses the PC to keep track of the port under examination.

Clock generation

Retiming flip-flops produce different frequencies and phases of clocks and framing pulses for other circuits in the CMC to use.

Outgoing port address register

The outgoing port address register stores the port number specified in the OMB.

Port use contention control

Each controller requests to use a port from the port use contention control. The peripheral is half duplex. The OC and the IC cannot use the port at the same time.

Signaling and timing

Different maintenance test points are located in the CC card to help locate card faults.

Technical data

Power requirements

The NT1X37AA has the following power requirements:

- current: +5V
- voltage: 1.8A (normal)

Pins labeled GND are logic circuit ground and are different from frame ground and battery return.

The common control card operates in duplex mode and limits the allocation of duplex pairs. Duplex messages are sent over two separate peripheral cards in the CMC.

NT1X44

Product description

The NT1X44 stack card provides the register and stack functions of the processor. The NT1X44 is a four layer card that conforms to DMS common features.

This description covers the following card codes:

- 1 Kword stack card-NT1X44AA
- 1 Kword stack card, ESD faceplate-NT1X44BA
- 4 Kword stack card, ESD faceplate-NT1X44BB
- 1 Kword stack SPIE card-NT1X44Y

Functional description

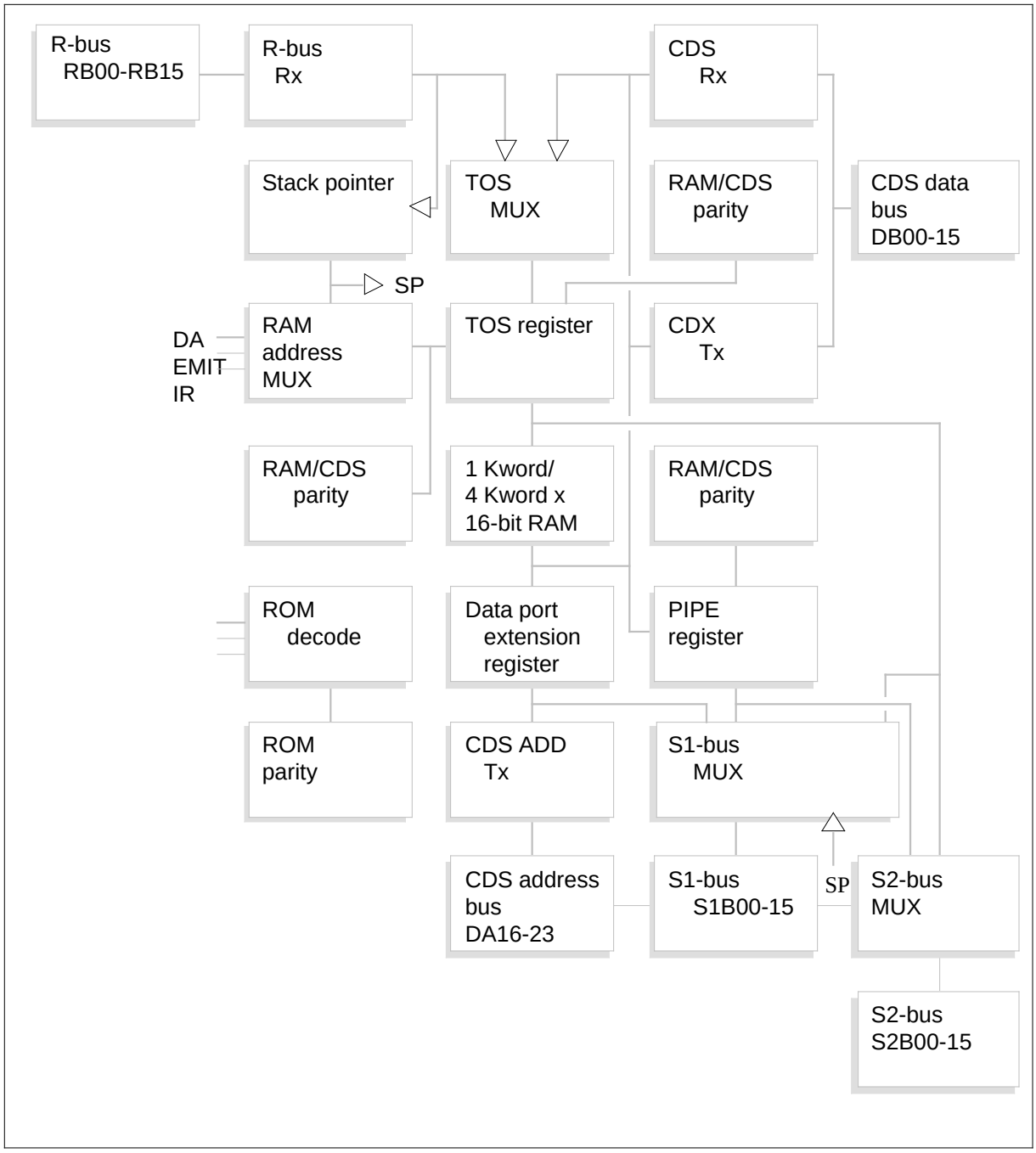
Functional blocks

The NT1X44 contains the following functional blocks:

- stack pointer
- RAM address multiplexer (MUX)
- RAM stack
- data port extension register
- most significant (MS) byte data store (DS) address drivers
- pipe register
- top-of-stack (TOS) register
- S1-bus MUX
- S2-bus MUX
- DS data drivers
- DS data receivers
- TOS MUX
- Result-bus (R-bus) receivers
- ROM decode
- ROM parity
- RAM/DS parity

The relationship between the functional blocks appears in the following figure.

NT1X44 functional blocks



NT1X44 (continued)

Stack pointer

The stack pointer is a 9-bit up/down counter (12 bits for 4 Kword stack) under microcode control. The stack pointer provides one of the four methods to address the RAM stack.

RAM address multiplexer

The RAM address MUX provides four methods to address the RAM stack under microcode control.

RAM stack

The RAM stack is a 1 Kword by 16 bit high speed memory with a 1-bit parity.

Data port extension register

The data port extension register is an 8-bit register. The data port extension register is loaded from the MS byte of the RAM/CDS bus under microcode control.

This register forms the MS byte of the 24-bit DS address. This register can be loaded in parallel with DA. Refer to arithmetic and logic function (ALF) board NT1X45.

Most significant byte data store address drivers

The MS byte DS address driver distributes the MS byte of the 24-bit address on the processor backplane.

Pipe register

The pipe register is a 16-bit register used as one of two source registers in arithmetic or logical operations.

The pipe register is loaded with data from the RAM stack or data store under microcode control. This register has a secondary function as a left-shift register that holds the multiplicand in a multiply operation.

Top-of-stack register

The processor uses the TOS register in four operations:

- as the top of stack to make sure of fast access to an element in arithmetic or logical operations
- as the data to store register on writes to RAM or DS
- to communicate data between processors when the processors run as a matched pair
- as a general purpose register with a different microcode bit to control loading

S1-bus multiplexer

The S1-bus MUX multiplexes the TOS register, pipe register, DA extension register and the stack pointer on the tristate S1-bus.

S2-bus multiplexer

The S2-bus MUX multiplexes the TOS register and the pipe register on the tristate S2-bus.

Data store data drivers

The DS data drivers distribute data from the 16-bit data port data bus on the processor backplane.

Data store data receivers

The DS data receivers provide hysteresis reception of data from the 16 bit bidirectional DS data bus.

Top-of-stack multiplexer

The TOS MUX selects one of two sources of data to load in the TOS register. The data sources are the DS/RAM or the R-bus. The selection of data is under microcode control.

Result-bus receiver

The R-bus receiver provides hysteresis reception of data from the 16-bit R-bus.

ROM decode

The ROM decode decodes the microcode ROM information and distributes control signals to areas of logic decoded for control.

ROM parity

The ROM parity generates a single-level parity bit of the seven microcode ROM bits received on the card.

RAM/DS parity

The RAM/DS parity generates parity and checks over address and data for both the RAM stack and the DS.

Parity checking is inhibited for page #FF of the DS.

NT1X46EA

Product description

The NT1X46EA system uses the improved load-route read-only memory (ROM) card for the 40 MHz central controller in the DMS-100 NT40. This ROM card is different from the previous version, NT1X46DA. This ROM card adds firmware to allow use of all load routes.

Functional description

The NT1X46EA provides the microstore and microstore addressing functions of the central processor.

Functional blocks

The NT1X46EA contains the following functional blocks.

- data jump register
- page register
- chapter register
- subroutine register
- ROM address multiplexer
- PROM microstore
- ROM data register
- ROM decode block
- ROM parity block
- reset address buffer

Data jump register

The data jump register is a 4-bit register. This register can multiplex to the least important 4 bits of the ROM address. This action provides a data jump ability.

Page register

The page register is a 2-bit register that allows access to the microstore in a single chapter. The page register has a bypass feature. The bypass feature overrides the microstore pipeline. This feature allows the system to define and execute the page jump in one step.

Chapter register

The chapter register is a single bit register that controls access between the two microstore chapters.

Subroutine register

The subroutine register is a 12-bit register that holds the return address of a microstore subroutine.

ROM address multiplexer

The 13-bit ROM address multiplexer is implemented with high-drive buffers. The multiplexer allows termination of the address lines. The multiplexer improves noise immunity under high load and capacitance conditions.

PROM microstore

The PROM microstore is a total of eight kbyte by 40-bit words. The PROM micro divides into two chapters of four pages each, with 1 Kword of storage in each page.

ROM data register

The ROM data register latches the data bits that the NT1X46EA card requires from the PROM output data register. Boards in the NT40 CPU use the PROM register.

ROM decode block

The ROM decode block decodes the latched microstore PROM data and distributes the control signal for onboard use.

ROM parity block

The ROM parity block performs a parity check on the PROM address and data. The ROM parity block sends the single-bit parity signal to the maintenance card NT1X48.

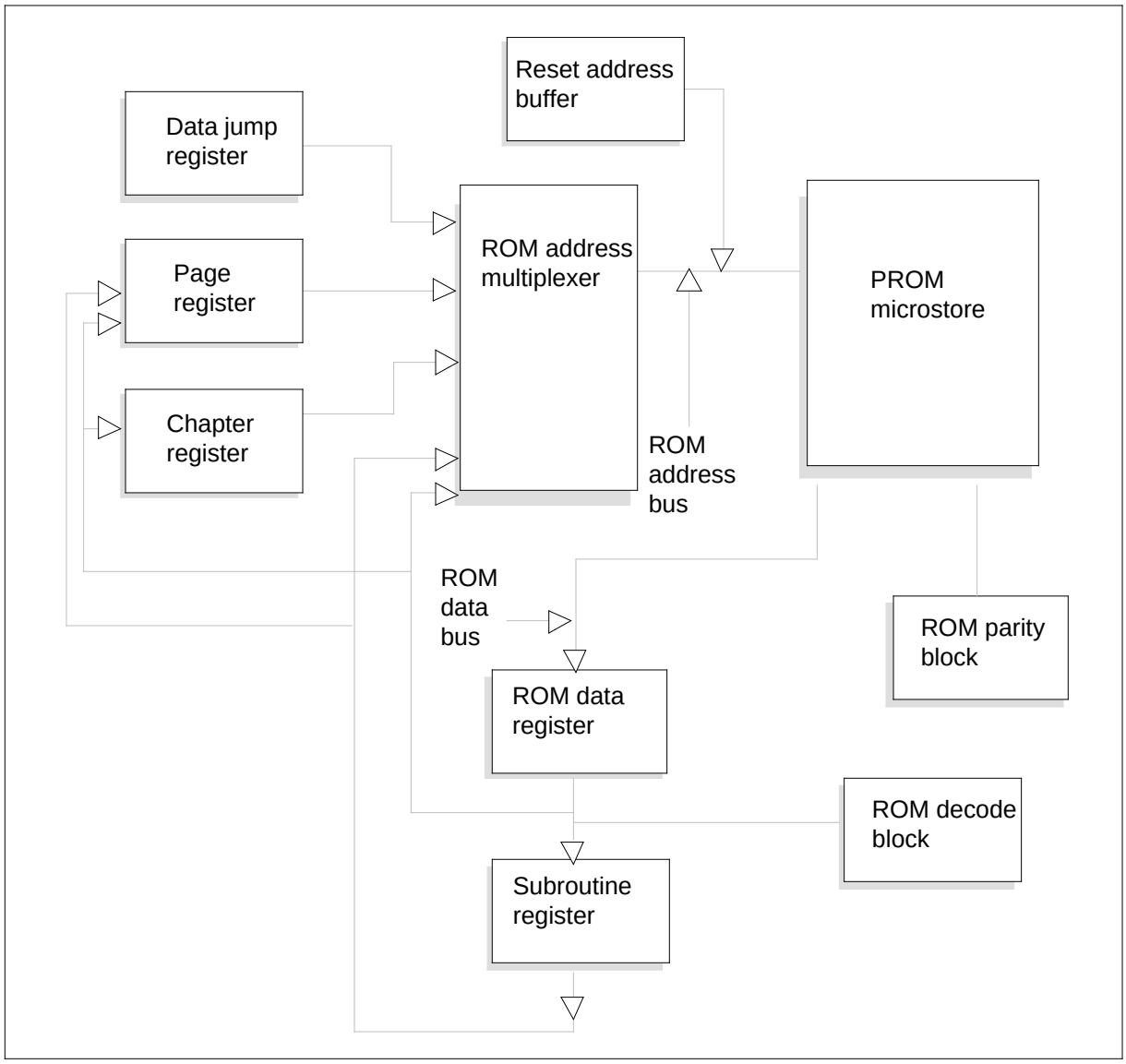
Reset address buffer

The reset address buffer supplies the CPU reset address. The system uses the reset address to reset the CPU.

The relationship of the functional blocks appears in the following figure.

NT1X46EA (end)

NT1X46EA functional blocks



Technical data

Power requirements

The nominal supply voltage for the NT1X46EA is +5V. The standard supply current is 3.5A.

NT1X47

Product description

The timing and control card provides the microcycle source and microstore decoding functions of the processor. This card has four layers and conforms to DMS common features.

The following versions of this card are available:

- NT1X47AA Processor timing and control
- NT1X47BA The same as NT1X47AA, with ESD faceplate
- NT1X47BB Processor timing and control, compatible with NT1X43BD Improved pipe and ESD faceplate
- NT1X47YA Processor timing and control SP1E
- NT1X47YB Processor timing and control SP1E, compatible with NT1X43BD Improved pipe.

Functional description

The NT1X47 provides the microcycle source and the microstore decoding functions of the processor.

Functional blocks

The NT1X47 contains the following functional blocks:

- clock generation
- program port clock delay
- microcycle clock control
- microcycle clock drivers
- digital timers
- clock interrupt register (CIR)
- ROM decode
- register destination decode
- register source decode
- flag selection
- data bus receivers
- status control register
- data bus drivers
- interrupt logic

NT1X47 (continued)

- hexadecimal display
- reset register
- reset sequencer
- ROM parity

The relationship between these parts appears in the Functional blocks figure.

Clock generation

A 36 MHz crystal oscillator provides the free-running 18 MHz CLK22 signal that drives clocks. When the system detects a defective clock, an automatic clock sensing mechanism selects the source clock from the mate processor. If an offline, manual, or power reset occurs, the processor must use the clock source of the processor.

A controlled clock switch is provided for test purposes.

Program port clock delay

The program port clock delay introduces a single CLK25 period delay into the release of a wait state. This action occurs if the program port causes the the wait state.

Microcycle clock control

Place the clock in a temporary wait state to synchronize the microcycle clock CLK50. A pair of synchronization signals are added to the microcycle clock control. This addition accommodates the improved program port control.

Microcycle clock drivers

Microcycle clock drivers provide distribution of the microcycle clock.

Digital timers

Digital timers provide all of the timeouts in the central processor (CP).

Clock interrupt register

The CIR is a 4-bit counter that sets the clock interrupt period. The inputs of the CIR are configured through pin straps when the system is connected. The S1-bus can read the CIR register and the output from the counter for control purposes.

ROM decode

The ROM decode decodes the ROM data register and distributes the control signals.

Register destination decode

The register destination decode decodes the ROM data register. The register destination decode distributes the register clocks and register clock enables through the processor.

Register source decode

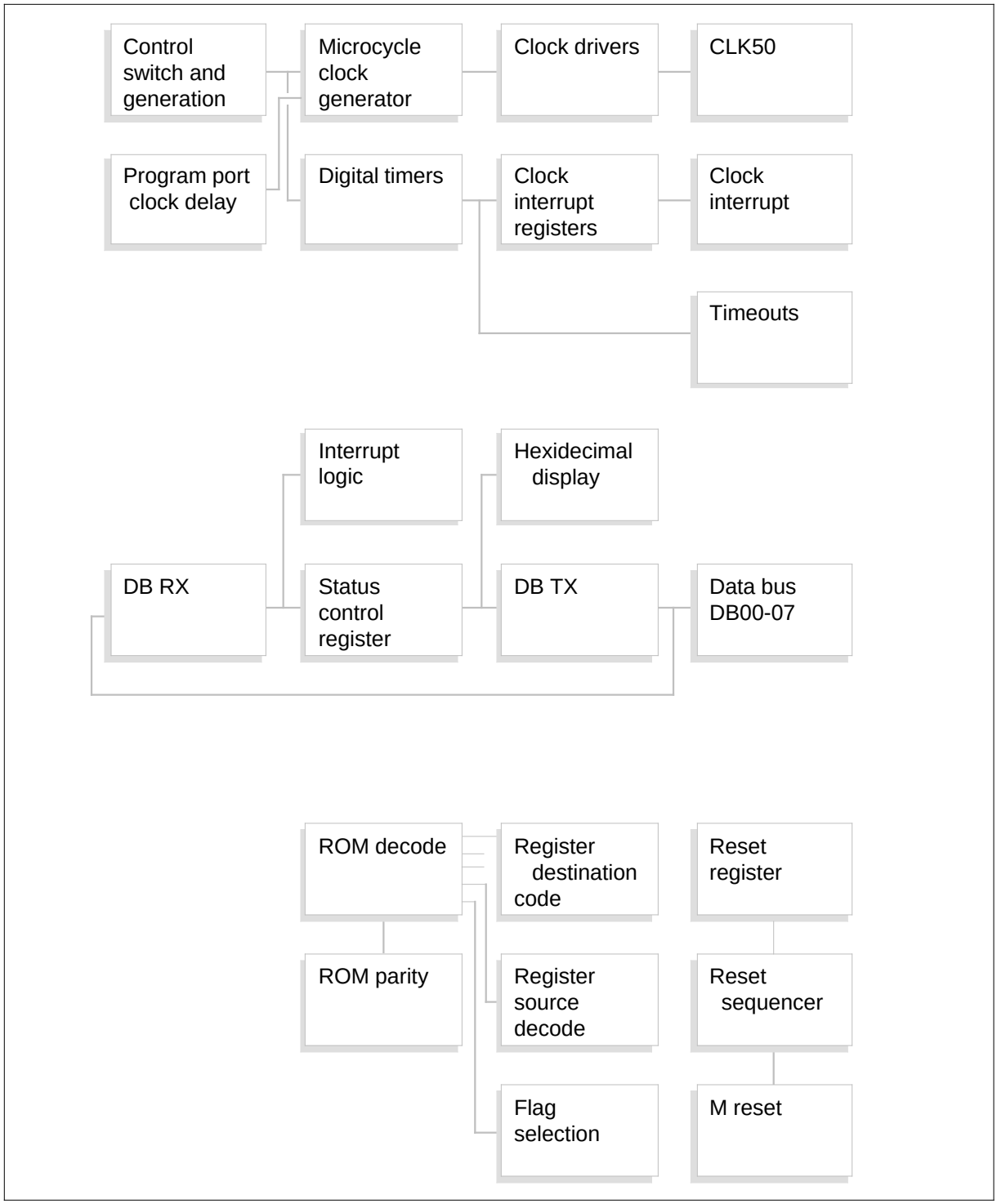
The register source decode decodes the ROM data registers. The register source decode distributes the register enable signals through the processor.

Flag selection

Two registers provide flag generation and selection. The outputs from both registers are multiplexed and selected under microprogram control. This action generates a single signal. Use this signal for conditional branching.

NT1X47 (continued)

NT1X47 functional blocks



Data bus receivers

Data bus receivers provide hysteresis reception of the least significant (LS) byte of the data bus.

Status control register

The NT1X47 contains bits 0 to 5 of the status control register. All eight bits (six used) are loaded from and read to the LS byte of the data bus.

Data bus drivers

Data bus drivers distribute the LS byte of the status control register to the data bus.

Interrupt logic

Three cards contain the interrupt register. One of the registers is the NT1X47. The debug and clock levels are on this card. The interrupt mask register (IRM) and the interrupt request register (IRQ) are provided.

The IRM is loaded from the data bus as a memory location destination. A multiplexing buffer on the output allows read operations to the data bus for control purposes.

The system multiplexes the IRQ to the data bus to read for control purposes.

Hexadecimal display

The system uses two hexadecimal displays as maintenance indicators. The displays appear as a write-only memory location on the data bus. The no read facility is provided.

Reset register

The reset register allows the processor to execute a reset sequence in response to re-initialization. The system multiplexes the register onto the data bus to allow read operations for control purposes.

Reset sequencer

A reset sequencer is a 6-bit recirculating register. The system normally clears the reset sequencer when a reset condition is not present. The release of the clear allows the system to clock the register at CLK25 rate. This action generates a sequence that stops the processor, issues a master reset and starts the microcycle clock.

The last stage of the sequencer inhibits the clock of the sequencer. This action locks out a repeat of the reset mechanism until the reset register clears the reset stimuli.

NT1X47 (end)

ROM parity

The ROM parity performs a single-level parity generation of the seven PROM data bits latched on this board.

Signaling

Timing points

The four timing points that are tapped appear in the following table.

NT1X47 timing points

Points	Period	Purpose
704clk	7.04 µs	when the two processors go to synchronization
TOUT+	12.5 µs	for timing out the data or program ports
CLK12.5	12.5 ns maximum, adjustable in 0.8 increments	provides the clock interrupts
STTOUT	0.8 s	a recovery mechanism with an insane active processor

NT1X50AB

Product description

The NT1X50AB data port extender provides a buffer between the processor and external memory devices.

The NT1X50AB is a double-sided card that conforms to DMS common features.

Functional description

The NT1X50AB provides transistor-transistor logic (TTL) to balanced line level shifting to the memory. The NT1X50AB provides a balanced line to a TTL level shift from the memory to the processor.

Functional blocks

The NT1X50AB contains the following functional blocks:

- differential address line drivers that have one direction
- differential bidirectional drivers and receivers
- differential control drivers and receivers that have one direction
- TTL to control bus direction and inhibit control signals

Differential address line drivers that have one direction

Differential address drivers accept TTL input signals. These drivers transmit differential address signals over a twisted pair of wires to the memory shelf where these lines terminate. The system enables the address drivers.

Differential bidirectional drivers and receivers

The system enables the differential data receivers. The system disables the differential data drivers when the system issues a read store. When the store completes the read, the system removes the wait state in the processor. The data bus returns to the normal state, write cycle.

Differential control drivers and receivers that have one direction

The extender receives the signals. The extender transmits the signals to the external memory device as differential control signals. These signals follow:

- read store (RS)
- write store (WS)
- active (ACT+)
- data port reset (DRESET)

NT1X50AB (end)

TTL logic to control bus direction and inhibit control signals

The configuration register inhibits read and write operations to the external memory devices. The configuration register does not allow the memory devices to receive EDUNIT. The processor maintenance can set the configuration register. This operation does not require the bus protocol signals. This operation can occur during bus failure.

NT1X51AA

Product description

The NT1X51AA central message controller (CMC) interface card is a special data port extender card in the shelf of the central processor (CP).

The NT1X51AA performs four functions:

- interfaces the CP with two CMCs
- acts as a bus extension of the single-ended, tristate busing scheme used in the CP and between the CP and CMCs
- decodes the address of an addressed CMC and allows communication between the CP and the CMC
- blocks or allows communication between a CMC and a CP

Functional description

The CMC interface contains two circuits. One circuit is present for each port to the CMCs.

Functional blocks

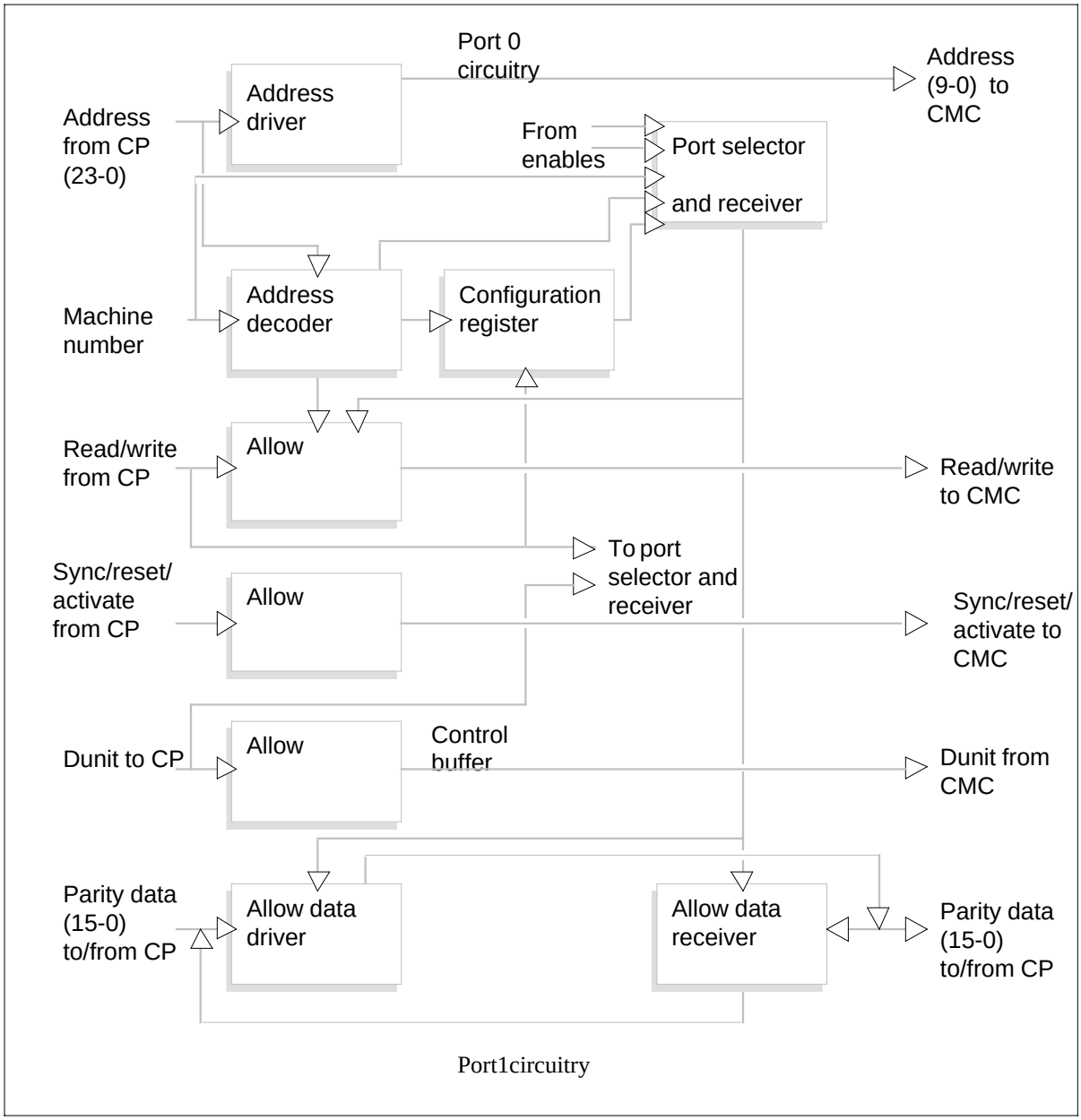
The CMC card contains the following functional blocks:

- address drivers
- address decoder
- configuration register (CR)
- port selector and enable (PSE)
- central buffer (CB)
- data drivers (DD)
- data receiver (DR)

The relationship of these parts appears in the following figure.

NT1X51AA (continued)

NT1X51AA functional blocks



Address drivers

The address driver receives the 24 tristate address lines from the CP backplane. The address driver feeds address bits (0-9) that have one direction to the CMC through a cable connection.

Address decoder

The address decoder consists of three address decoding circuits. One circuit decodes the address of CMC 0. One circuit decodes the address of CMC 1. One circuit decodes the address of the configuration register.

Configuration register

The CR enables or blocks the DUNIT and IOINT signals to the CP.

Port selector and enable

The PSE controls the direction of the tristate bus between the CMCs and the CPs. The PSE controls the read and write signals on the CMC interface port to the CMC.

Central buffer

The CB buffers the control leads between the CP and the CMC.

Data drivers

The PSE can enable the tristate DDs. The tristate DDs can forward the bidirectional data bus lines (0-15) from the CP to the CMC.

Data receiver

The PSE can enable the tristate DRs. The tristate DRs can forward the bidirectional data bus and parity bus from the CMC to the CP.

Technical data

Power requirements

The NT1X51AA has the following power requirements:

- voltage: +5V
- current: 2.2A

The input power to this card is fused on the paddle board with an axial lead fuse. A visual fuse alarm circuit for this fuse includes a light-emitting diode (LED). The LED is on the faceplate to indicate when a fuse is open.

NT1X54AA

Product description

The NT1X54AA jack-ended trunk circuit pack allows tests of trunks and lines. Tests occur with portable test equipment from the MAP terminal. The card contains two different test circuits. Each test circuit provides T-lead, R-lead, T1-lead, and R1-lead. These leads are for use with DMS-100, DMS-200 and combined DMS-100/DMS-200 switches.

Location

The card occupies one card position in a maintenance trunk module (MTM) or a four-wire or eight-wire trunk module (TM).

Functional description

The NT1X54AA card provides normal trunk circuit processing. The NT1X54AA converts outgoing pulse amplitude modulation (PAM) samples to voice frequency (VF) signals and incoming VF signals to PAM samples. The VF information does not pass to or come from a trunk. The VF leads connect to test jacks for use with portable test equipment. The system sends PAM samples to the MTM or the TM. The system sends the samples over the transmit pulse amplitude modulation (XPAM) bus. The system receives the samples over the receive pulse amplitude modulation (RPAM) bus.

Functional blocks

The NT1X54AA contains the following functional blocks:

- sampling gate
- digital-analog (D-A) converter
- transmit P-pads
- analog-digital (A-D) converter
- level-adjustment pads
- isolating-limiting circuits
- looparound circuits
- trunk logic circuit (TLC)

Sampling gate

The sampling gate is common to the receive and the transmit circuit. In the transmit direction, the gate samples PAM information from the MTM or TM on the RPAM bus at an 8 kHz rate. The system applies the sampled information to the D-A converter for additional processing. In the receive direction, the gate samples the converted VF information from the A-D converter at an 8 kHz

rate. The gate sends the sampled information to the MTM or to the TM over the XPAM bus.

D-A converter

The D-A converter accepts sampled PAM digital information from the sampling gate. The D-A converter converts the PAM information to VF analog information. The converter amplifies the signal before the converter applies the information to the level-adjustment pads.

Transmit P-pads

The system includes the P-pads of 4, 2 and 1 dB in the transmit circuit. This action compensates for losses. This action produces the actual measured loss for the trunk the system tests. Relays control the pads. The trunk logic circuit operate the relays.

The P-pad settings for applications appear in the table below.

P-pad settings

Application	Pad setting (dB)
Local direct trunk	3
Tandem trunk to analog tandem switch	3
Tandem trunk to digital tandem switch	6
Toll connecting to analog Class 4 switch	5
Toll connecting to digital Class 4 switch	6
Collocated step-by-step (SXS) office	1

A-D converter

The A-D converter accepts VF information from the level-adjustment pad and converts the VR information to PAM information. The converter passes the information to the sampling gate for transmission to the MTM or the TM.

Level-adjustment pads

The transmit and receive circuits contain level-adjustment pads. These pads provide adjustments from 0 dB through 15.75 dB in 0.25dB steps. Miniature

NT1X54AA (continued)

switches control the pads. Select the switches in combinations to produce the full adjustment range. Switch positions appear in the following table.

Level-adjustment pad switch settings

Switch	Segment	Adjustment (dB)
S1 (receive)	3	8.00
S2 (transmit)	2	4.00
	1	2.00
S3 (receive)	3	1.00
S4 (transmit)	2	0.50
	1	0.25

Isolating-limiting circuits

The system provides an isolating circuit in the transmit and the receive direction. The isolating circuit does not allow signals that are not VF to enter or leave the card. The system provides a limiting circuit in the transmit and receive direction. The limiting circuit restricts the signal levels that enter or leave the card.

Looparound circuits

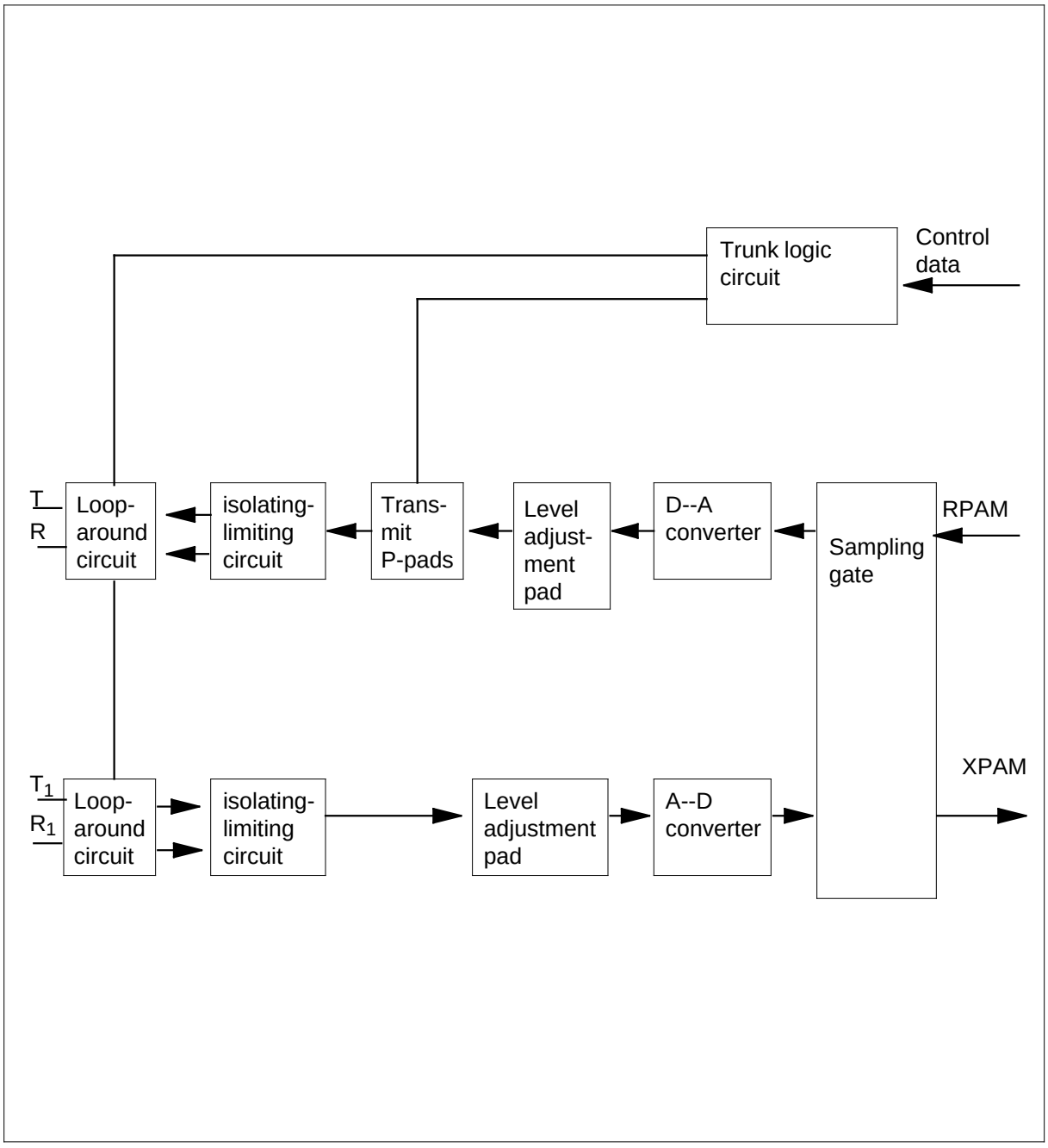
The trunk logic circuit controls a relay. This relay loops the circuits at the T-lead, R-lead, T1-lead, and R1-lead. This action isolates the test trunk circuit from the maintenance test position. This action allows internal tests of the trunk circuit.

TLC

The TLC handles communications and serves as a communications buffer between the NT1X54AA card and the TM. The TLC controls operation of the relays that control the P-pad and the looparound circuit.

The relationship between the functional blocks appears in the following figure.

NT1X54AA functional blocks



NT1X54AA (end)

Technical data

The provides the following transmit and receive levels:

Transmit and receive levels

Level	Value
Maximum transmit level for digital test sequence (DTS) input	+9 dBm
Transmit level range with P-pads set to 0 for DTS input	+9 dBm to -6 dBm
Minimum receive level for DTS output	-12 dBm
Receive level range for DTS input	-12 dBm to +3 dBm
Nominal transmit level for TP3 tests	-6 dBm
Nominal receive level for TP3 tests	0 dBm
Nominal transmit level for TP0 tests	0 dBm + P-pad value
Nominal receive level for TP0 tests	0 dBm

The recommended cable type is NE808A, with an impedance of 0.02 µF for each 1000 ft. The maximum cable length is 760 m (2500 ft).

Dimensions

The following are dimensions for the NT1X54AA circuit card:

- height: 353 mm (13.9 in.)
- depth: 280 mm (10.9 in.)

Power requirements

The NT1X54AA card requires 500 mW of power for each idle trunk circuit.

DANGER

Damage to equipment or loss of service

Use this card on telephone wiring that Northern Telecom protector, catalog number 303M-12AIKE, protects. A 26 AWG copper wire with thermoplastic insulation must be present. The maximum fusing wire that you can use in series with the protector is 26 AWG.

NT1X55

Product description

The NT1X55 disk drive controller provides an interface. The interface is between the input/output controller (IOC) of DMS-100 Family switching equipment and one Priam Winchester disk drive. The Winchester disk subsystem provides high-capacity memory enhancement to the DMS-100 Family switch of 30 Mbytes to 150 Mbytes. The disk controller receives messages in parallel data format. The controller receives messages from the IOC common bus and routes messages to the Winchester disk drive.

The primary usage features of the NT1X55 are as follows:

- controls a maximum of three Priam disks
- maintains backup memory allocation for a map of the drive configuration
- monitors configuration map and disk variables to detect errors
- maintains logs to keep track of activities for the disk system
- incorporates a self-test facility
- provides a light-emitting diode (LED) fuse failure indicator mounted on the front panel

Location

The NT1X55 disk controller occupies one card position in an NT1X61 IOC or an NT2X76 combined central message controller (CMC)/IOC shelf.

Functional description

Divide the disk controller circuit in five major parts:

- an IOC interface,
- a microprocessor core
- a burst error processor (BEP),
- a buffer memory
- a disk interface.

The disk controller design can emulate two virtual controllers, each controller is qualified to control a separate disk drive. The central control (CC) can select one of two virtual controllers. Selection occurs through the terminal number field of the CC to peripheral processor messages. Most commands are performed separately for each virtual controller. These controllers include data transfer between the CC and disk and other disk-related functions. Several maintenance functions apply to the card as a whole and are not only associated with a virtual controller.

NT1X55 (continued)

The disk controller emulates one virtual controller at any time. Outgoing messages are queued on a disk controller basis because the system cannot interrupt the control processor. Outgoing messages are not queued on a virtual controller basis to prevent message rebounds. Higher level CC processes are responsible for queuing messages generated by the virtual controller. A process associated with one virtual controller terminates. The system sends a message that relates to the alternate virtual controller.

In the current application with the DMS-100 Family of switches, one disk drive, and one virtual controller, is in use with a disk controller.

Stored data on the disks are in 1 kbyte sectors that can be addressed separately. The parameters, like cylinder, track number, and sector number access each sector. To avoid software overheads that are not necessary, the disk controller accepts logical addresses. Logical addresses are the volume number and block number. The disk controller converts logical addresses to the address required to access the sector.

The disk controller can control several models of Priam drives. During the initialization of a drive, the disk controller learns parameters of the disk. The disk controller reports the total disk resources available to the file system. The disk controller can partition resources into logic volumes. Each volume has a adjacent set of addresses. The disk controller firmware imposes limits on the number of volumes (32) and the size of the volume (65 456 blocks). The allocate volumes command string assigns the wanted partitions to the drive. When a drive is allocated, you can issue the logical address to access any available block.

To perform the address translation, the disk controller maintains a map for the drive partitioning. Save this configuration map in the buffer memory. The configuration map is written to two reserved disk sectors for nonvolatile backup and drive portability.

When a logical address is received, the address is first converted to an absolute block number. To convert an address, add the volume offset obtained from the configuration map to the block number in question.

Convert the absolute block number in to a address as follows:

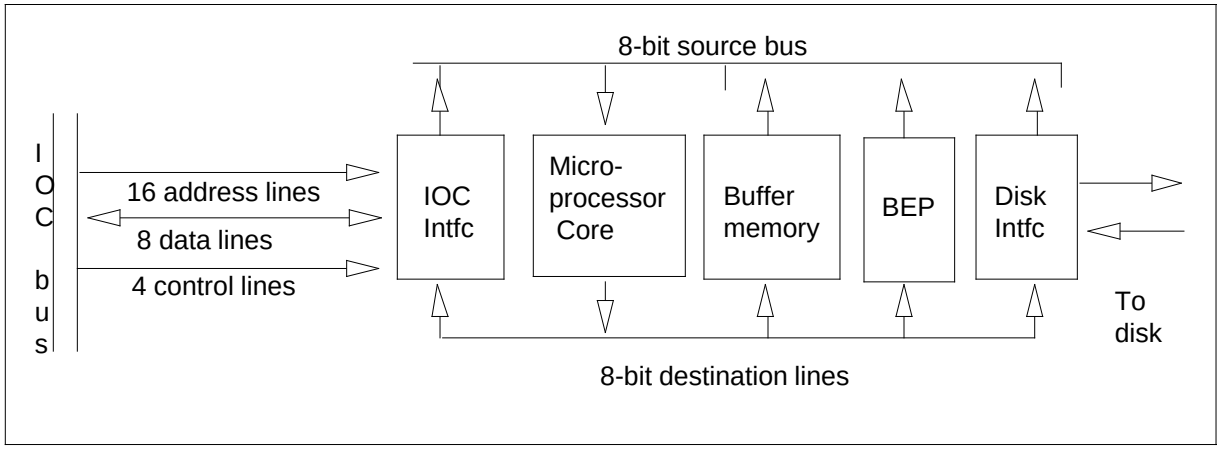
- Divide the number of sectors. The remainder is the sector number.
- Divide the sector number by the number of tracks. The remainder is the track number.
- The quotient from the operation that preceded is the cylinder number.

Before you use the disk drive with DMS-100 Family switches, you must format and allocate the disk drive. The drive is not always arranged for DMS-100 Family use. In this occurrence, attempts to enter data and receive output result in errors. Place a disk drive in a DMS-100 Family shelf. Verify dual in-line package (DIP) switch settings on the drive. The DIP switch settings program the number of sectors for each track. Make sector programming changes before you turn on the drive. The appropriate DIP switch settings appear in the table titled “Disk DIP switch settings”.

Maintenance logs are on a virtual controller on a one for each disk basis. The logs keep track of the activities of the disk system. These activities include the number of error messages sent to the CC or the number of soft data errors.

The relationship with the functional blocks appears in the following figure.

NT1X55 functional blocks for the disk controller



IOC interface

The common IOC input bus to the disk controller and other device controllers comprises 16 address lines that have one direction. The common IOC input bus also comprises eight bidirectional lines, and four control lines that have one direction.

Bits 12 to 15 of the addresses are matched to a 4-bit strap value. This 4-bit strap is for insertion in the slot plug of the disk controller. Bits 10 and 11 identify the disk controller port to which the drive connects. The disk controller has four ports and handles one drive. The disk drive is hardware-wired to respond to port zero. Bits zero to nine select message buffer words and associated status and control registers.

NT1X55 (continued)

The eight data lines send messages to and receive messages from the disk controller. A list of commands the disk controller accepts appears in the following table.

The four control lines carry signals that control read and write sequences and hardware resets.

All central processing unit (CPU) control and data transactions are performed with messages routed through the IOC and central message controller (CMR). Outgoing messages from the CPU have information for different tasks related to data transmission, control interrogation, and maintenance. The system generates incoming messages to the CPU as a result of outgoing messages.

A status register in the IOC interface controls the flow of messages. The IOC can read this 8-bit register separate from the microprocessor of the disk controller at any time. The microprocessor is responsible for loading a latch with seven of the eight bits of data. The additional bit is a separate flag that indicates the state of a sanity timer. The seven bits indicate the state of the disk controller. The seven bits indicate if the disk controller is ready to receive data or transmit data.

Microprocessor core

The microprocessor core includes an arithmetic and logic unit (ALU), sequencing logic, micro program memory, a pipeline latch, and source and destination management.

A bipolar processor that provides control of an 8-bit path for all data control drives the disk controller. Pass data through the ALU to perform all data transfers in the disk controller. Devices that generate data have ports on the source bus and devices that accept data have ports on the destination bus.

Commands (Sheet 1 of 3)

Command	Function
format	This command learns the available capacity of the disk and gives each sector a different address. This command writes timing and synchronization information on the disk.
allocate volumes	This command defines the partitioning or the disk store in logical volumes.

Commands (Sheet 2 of 3)

verify	This command reads all sectors in the specified volume. This command creates a list of defective blocks for or sectors that cannot be read or located. Error correction is not ever invoked. This function allows the file system to map media defects to an error file before the file system uses the volume.
read	This command provides random access to any 1 kbyte block on the disk. The function passes the data back to the central control (CC) in five messages.
write	This command allows the CC to update any 1 kbyte block on the disk.
boot	This command locates the bilge file and sends the file to the CC. Flow control requires a boot-continue command after every message the CC receives. This command starts flow control.
query resources	This command reports the available disk capacity to the CC.
query allocation	This command reports the volume allocation of the disk to the CC.
query logs	This command sends the log records to the CC.
clear log(s)	This command clears all of the log records or this command only clears the record specified.
format blocks	This command fills the data field of a list of sectors (maximum 120) with a specified data pattern.
setroute	This command is a maintenance command which assigns the peripheral processor number and clears the latched sanity flag.
profile	This command returns the specified area of the buffer memory of the disk controller to the CC.
query status	This command returns the drive status map, store status, and signature analysis gate bits to the CC.
dump memory	This command returns the specified area of the buffer memory of the disk controller to the CC.

NT1X55 (continued)

Commands (Sheet 3 of 3)

query vintage	This command reports the firmware vintage, like 1D2 or 1W3.
spin	This command provides a mechanism to start or stop the disk spindle rotation.
selftest	This command allows the CC to test elements of the disk system. This command has a test mode to allow different types of tests to be performed separately.

Burst error processor

The burst error processor (BEP) provides error detection and correction of the data streams to and from the disk. The BEP can check the integrity of the disk resource variables and configuration maps when stored in the buffer memory.

The BEP generates redundancy codes in an internal register array. Check bits are appended to the data. The system writes the data to the disk. The observed error rates for the system are one soft error for each million blocks read. The probability of an error that is not detected is 2×10^{-1} .

The BEP corrects all single burst errors less than 12 bits long. The error burst can be longer than 11 bits, or a double burst can occur. In this occurrence, a limited possibility occurs that data miscorrection is possible for a different valid code word. This miscorrection is the primary reason for an error rate that is not detected. Perform corrections on any block in a maximum of 120 ms for each attempt.

Buffer memory

The buffer memory comprises a 3 kbyte-by-8-bit memory interfaced on the microprocessor buses. The buffer memory stores data which writes to and reads from the disk. The data store is partitioned in twelve 256 byte pages. Three of the 256 byte pages are reserved for disk controller workspace and storing log information. These pages are also reserved to maintain configuration maps and drive variables.

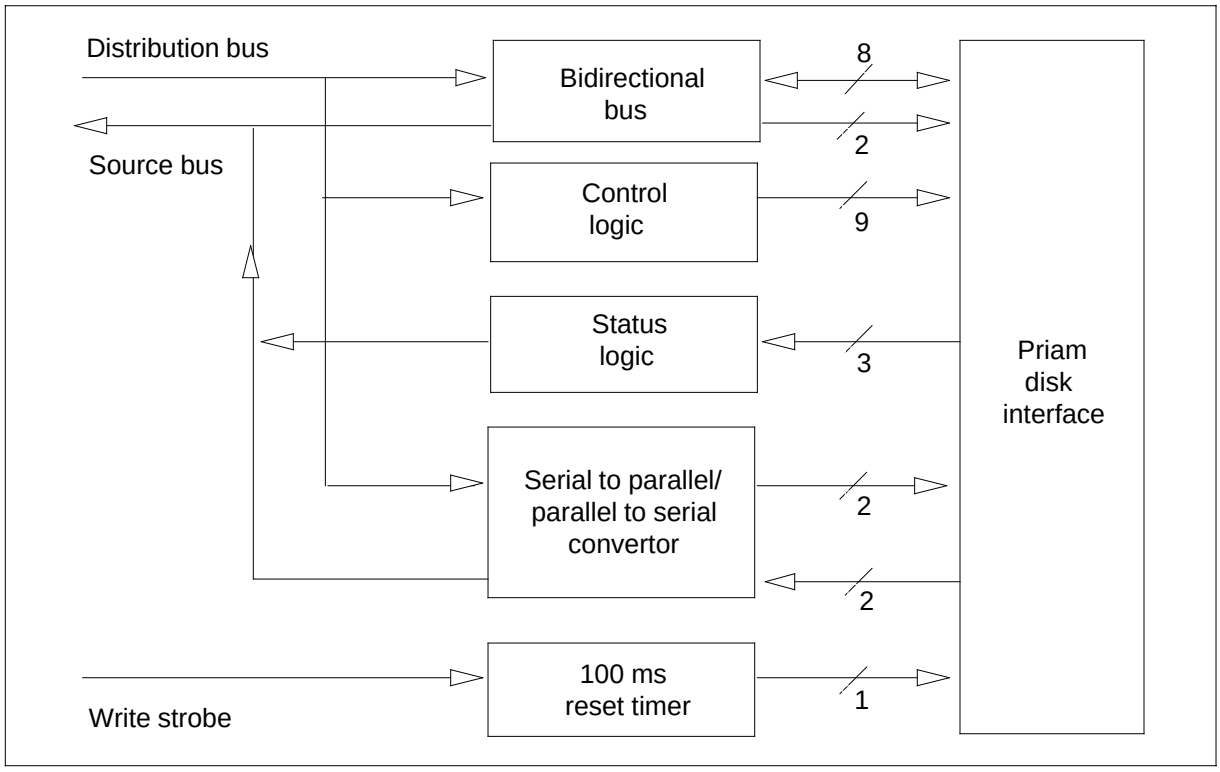
Disk interface

The disk interface can be reduced to the following functional parts:

- a bidirectional bus
- control and status signals
- data conversion signals
- clock switch, synchronization, and reset logic

The relationship with the functional blocks of the disk interface appears in the following figure.

NT1X55 functional blocks for the disk interface



An 8-bit bidirectional bus between the disk controller and the control processor associated with the disk is present. This bidirectional bus sends commands to the disk drive (spin up, spin down, seek restore, reset fault indication). This bus also loads target cylinder addresses, and reads the disk status or the current cylinder address. The bus is in the positive logic mode. Two positive-logic address bits determine the register you write on or the register you read from the disk. Test the bus separate from the disk for maintenance purposes.

Several discrete control and status signals on the interface are present. These signals are required to provide the disk controller with real time control of the disk read and write electronics.

NT1X55 (continued)

The disk control functions appear in the following table.

Disk control functions

Control lines	Number	Function
USEL -	2	selects one of two disks
WGATE-/RGATE	2	enables read and write electronics
HEAD/	3	encoded to select one of eight heads (tracks)
ADD+/AD1+	2	selects target register for bus read and write
DSKRD-/DSKWR-	2	strobes in association with the bidirectional bus

The status line functions appear in the following table.

Status line functions

Status lines	Function
DRDY -	indicates drive is current, servos locked on track
INDEX -	provides a servo pulse from the control track one time in each round
SECTOR -	pulses to indicate the start of each sector

The data conversion logic circuit converts non-return-to-zero (NRZ) serial data. The circuit converts this data from the disk to an 8-bit representation for the disk controller. The circuit converts 8-bit parallel data from the disk controller to NRZ serial data for transmission to the disk.

Three types of synchronization are required during serial input and output operations:

- The first type of synchronization is the rotation of the disk. To accomplish this, poll for an index mark or wait for sector pulses. The system generates both options from the control tracks on the media. Both options provide

complete rotational references separate of any differences in disk motor speed.

- The second type of synchronization is clock synchronization of the disk controller microprocessor to the data clock that the disk generates. This synchronization occurs in the hardware clock switch circuits.
- The third type of synchronization is byte synchronization to the serial data stream. During write operations, a firmware write to the parallel-to-serial converter of the special data synchronization character establishes the byte-synchronization. For the read operation, hardware that waits for the same character performs data sunchronization.

When the system selects a disk, the disk provides a reference clock. If the system asserts the read gate, extract the clock from the encoded data through use of a phase-locked oscillator. If the system does not assert the read gate, derive the clock from the disk media with the servo head. The clock differs in frequency as the motor speed changes. Make sure the firmware runs in synchronization with the disk. The main clock can be switched from the 8 MHz IOC-CLK to the disk-generated REF-CLK (about 8.3 MHz).

The reset timer allows the disk controller to apply a 100 ms reset strobe to the disk drive. To perform this action, assert a single write strobe.

Technical data

This section describes the technical specifications for the disk drive controller. These specification include:

- IOC bus requirements
- disk interface requirements
- disk DIP switch settings
- power requirements
- environmental conditions
- equipment dimensions

IOC bus specifications

Technical data for the IOC bus includes specifications for address lines, control lines, and data lines.

The specifications for the address lines are as follows:

- 16 lines that have one direction with Schottky transition to transition logic (TTL) line drivers and low power Schottky receivers
- terminations of 270 ohms to +5 V and 470 ohms-to-ground

NT1X55 (continued)

The specifications for the control lines are as follows:

- 4 lines that have one direction with open connector Schottky TTL line drivers and low power Schottky hysteresis receivers
- terminations of 270 ohms to +5 V and 470 ohms-to-ground

The specifications for the data lines are as follows:

- 8 bidirectional lines with Schottky TTL line drivers and low power Schottky receivers
- terminations of 270 ohms to +5 V and 470 ohms-to-ground

Disk interface specifications

Disk interface specifications appear in the following table.

Disk interface specifications

Component	Specifications
Data lines	eight bidirectional lines
Data code	NRZ
Address lines	two lines that have one direction
Control lines	12 lines that have one direction
Status logic	three lines that have one direction
Serial interface	two sets of two lines that have one direction
Reset strobe	one line that has one direction
Connecting cables	two with maximum length of 5.49 m (18 ft)
Disk types	Priam 3350-10
	Priam 6650-10
	Priam 15450-10

Disk DIP switch settings

For correct operation with DMS-100 Family equipment, set the DIP switches on the disks as listed in the following table.

Disk DIP switch settings

Group Location				
Single PCB	**Split PCB**	**Switch number**	**Switch function**	**Switch setting**
10 K	1 J	1	Unit Select 1	On
		2	Unit Select 2	Off
		3	Unit Select 3	Off
		4	Unit Select 4	Off
		5	Skip defect protection	On
		6	Write enable	On
		7	Clock transmit	On
		8	Clock phase	On
11 K	9 F	1	1 sector / track	Off
		2	2 sectors / track	On
		3	4 sectors / track	Off
		4	8 sectors / track	Off
		5	16 sectors / track	On
		6	32 sectors / track	Off
		7	64 sectors / track	Off
		8	reserved	Off

NT1X55 (end)

Power requirements

The power requirements appear in the following table.

Power requirements

Type of Power	Amount
Voltages required	+5 V
Current required	4.5 A

Environmental conditions

The disk drive controller performs under limited environmental conditions that appear in the following table.

Ambient Conditions

Condition	Operating range	Short-term range
Temperature	10°C to 30°C	5°C to 49°C
	(50°F to 86°F)	(41°F to 120.2°F)
Relative humidity	20% to 55%	20% to 80%

Note: A relative humidity of 80% is expected at an ambient temperature of 215°C (69.85°F) maximum. At an ambient temperature of 495°C (120.25°F), the relative humidity is expected to be 30% maximum.

Equipment dimensions

The disk drive controller dimensions are:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 213 mm (0.84 in.)
- weight: 820 grams (1.8 lb)

NT1X55FA

Product description

The NT1X55FA disk drive controller provides an interface. This interface is between the input/output controller (IOC) of DMS-100 Family switching equipment and one Priam Winchester disk drive. The Winchester disk subsystem provides a high-capacity memory enhancement to the DMS-100 Family switch. The capacity of the NT1X55FA circuit card is 250 Mbytes. The disk controller receives messages in parallel data format. The disk controller receives these messages from the IOC common bus. The disk controller routes the messages to the Winchester disk drive.

The primary usage features of the NT1X55FA are as follows:

- controls a maximum of three Priam disks
- maintains backup memory allocation for a map of the drive configuration
- monitors configuration map and disk variables to detect errors
- maintains logs to keep track of activities for the disk system
- incorporates a self-test facility
- provides a light-emitting diode (LED) fuse failure indicator on the front panel

Location

The NT1X55FA disk controller occupies one card position in an NT1X61 IOC or an NT2X76 combined central message controller (CMC)/IOC shelf.

Functional description

Divide the disk controller circuit in five major parts:

- an IOC interface
- a microprocessor core
- a burst error processor (BEP)
- a buffer memory
- a disk interface

The design of the disk controller allows the disk controller to copy two virtual controllers. Each controller can control a separate disk drive. The central control (CC) can select one of the two virtual controllers. The selection occurs through the terminal number field of the CC to peripheral processor messages. Most commands are performed separately for each virtual controller. These commands include data transfer between the CC and disk and other

NT1X55FA (continued)

disk-related functions. Several maintenance functions apply to the card as a whole and are not associated with a virtual controller.

The disk controller emulates one virtual controller at any time. You cannot interrupt the control processor. Outgoing messages are queued on a disk controller basis and not on a virtual controller basis. This process allows the controller to avoid message rebounds. Higher level CC processes are responsible for queuing virtual controller-dependent messages. For example, a process associated with one virtual controller terminates. This termination occurs before the system sends a message that relates to the alternate virtual controller.

In the current application with the DMS-100 Family of switches, use one disk drive, and virtual controller, with a disk controller.

Store data on the disks in 1 kbyte sectors that are addressed separately. Parameters, like cylinder, track number, and sector number access each sector. To avoid software overheads that are not necessary, the disk controller accepts logical addresses. A logical address is the volume number and block number. The disk controller converts logical addresses to the physical address required to access the sector.

The disk controller can control several models of Priam drives. During the initialization of a drive, the disk controller learns the parameters of the disk. The disk controller reports the total disk resources available to the file system. The resources are partitioned in to logic volumes. Each volume must contain an adjacent set of addresses. The disk controller firmware imposes limits on the number of volumes (32) and the size of the volume (65 456 blocks). Use the allocate volumes command string to assign the wanted partitioning. Allocate a drive and issue the logical address to access any available block.

To perform the address translation, the disk controller maintains a map for the drive partitioning. The buffer memory saves this configuration map. This configuration map is written to two reserved disk sectors for nonvolatile backup and drive portability.

A logical address is received. The address is first converted into an absolute block number. The disk controller adds the volume offset obtained from the configuration map to the block number in question.

Convert the absolute block number to an address as follows:

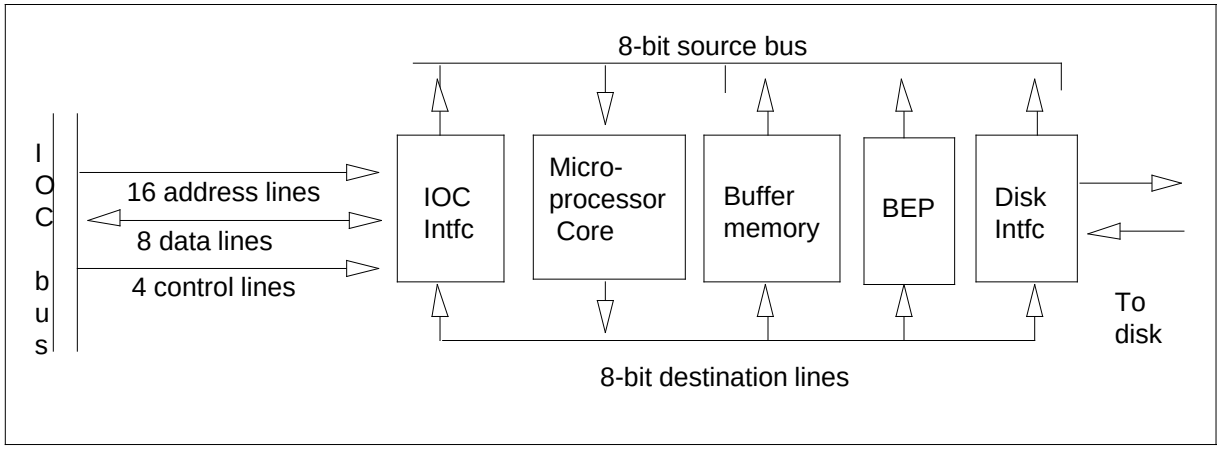
- Divide the number of sectors. The remainder is the sector number.
- Divide the sector number by the number of tracks. The remainder is the track number.
- The quotient from the earlier operation is the cylinder number.

Before you use the disk drive with DMS-100 Family switches, format and allocate the disk drive. If the drive is not arranged for DMS-100 Family use, attempts to enter data and receive output result in errors. When you place a disk drive in a DMS-100 Family shelf, verify the dual inline package (DIP) switch settings on the drive. The DIP switch settings program the number of sectors for each track. Make any changes to sector programming before you power up the drive. The appropriate DIP switch settings appear in the table titled “Disk interface specifications”.

Maintenance logs are on a virtual controller on one for each disk basis. The logs note the activities of the disk system. Activity examples are the number of error messages sent to the CC or the number of soft data errors.

The relationship with the functional blocks appears in the figure that follows.

NT1X55FA functional blocks for the disk controller



IOC interface

The common IOC input bus to the disk controller and other device controllers comprises 16 address lines that have one direction. The IOC input bus also comprises eight bidirectional lines, and four control lines that have one direction.

NT1X55FA (continued)

Bits 12 to 15 of the addresses are matched to a 4-bit strap value. This 4-bit strap value is for the slot into which the disk controller plugs. Bits 10 and 11 identify the disk controller port in which the drive is connected. The disk controller has four ports and handles one drive. The disk controller is hardware-wired to respond to port zero. Bits 0-9 select message buffer words and associated status and control registers.

The eight data lines send messages to and receive messages from the disk controller. A list of commands you programmed the disk controller to accept appear in the following table.

The four control lines carry signals that control read and write sequences and hardware resets.

Messages routed through the IOC and central message controller (CMR), perform all central processing unit (CPU) control and data transactions. Outgoing messages from the CPU contain information for different tasks related to data transmission, control interrogation, and maintenance. The system generates incoming messages to the CPU as a result of outgoing messages.

A status register in the IOC interface controls the flow of messages. The IOC can read this 8-bit register at any time free of the microprocessor of the disk controller. The microprocessor loads a latch with seven of the eight bits of data. The additional bit is a separate flag that indicates the state of a sanity timer. The seven bits indicate the state of the disk controller. An example is if the disk controller is ready to receive data or ready to transmit data.

Microprocessor core

The microprocessor core includes an arithmetic and logic unit (ALU), sequencing logic, micro program memory, a pipeline latch, and source and destination management.

A bipolar processor that provides control of an eight-bit path for all data control drives the disk controller. To perform all data transfers in the disk controller, transfer data through the ALU. Devices that generate data have

ports on the source bus. Devices that accept data have ports on the destination bus.

Commands (Sheet 1 of 2)

Command	Function
format	This command learns the available capacity of the disk, and assigns each sector a different address. This command writes timing and synchronization information on the disk.
allocate volumes	This command defines the partitioning or the disk store in logical volumes.
verify	This command reads all sectors in the specified volume. This command also creates a list of defective blocks for sectors that cannot be read or located. Error correction is not ever invoked. This function allows the file system to map media defects into an error file before the file system uses the volume.
read	This command provides random access to any 1 Kbyte block on the disk. The data passes back to the central control (CC) in five messages.
write	This command allows the CC to update any 1 Kbyte block on the disk.
boot	This command locates the bilge file and sends the file to the CC. The system requires a boot-continue command after every message the CC receives. This command allows the system to start flow control.
query resources	This command reports the available disk capacity to the CC.
query allocation	This command reports the volume allocation of the disk to the CC.
query logs	This command sends the log records to the CC.
clear log(s)	This command clears all of the log records. This command clears the record specified.
format blocks	This command fills the data field of a list of sectors (maximum 120) with a specified data pattern.

NT1X55FA (continued)

Commands (Sheet 2 of 2)

Command	Function
setroute	This command is a maintenance command that assigns the peripheral processor number and clears the latched sanity flag.
profile	This command returns the specified area of buffer memory to the CC. This area of buffer memory belongs to the disk controller.
query status	This command returns the drive status map, store status, and signature analysis gate bits to the CC.
dump memory	This command returns the specified area of buffer memory to the CC. This area of buffer memory belongs to the disk controller.
query vintage	This command reports the firmware vintage, like 1D2 or 1W3.
spin	This command provides a mechanism to start or stop the disk spindle rotation.
selftest	This command allows the CC to test elements of the disk system. This command has a test mode to permit different types of tests to be performed separately.

Burst error processor

The burst error processor (BEP) provides error detection and correction of the data streams to and from the disk. You can use the BEP to check the integrity of the disk resource variables and configuration maps. The processor checks the integrity of these variables when the processor stores the variables in the buffer memory.

The BEP generates redundancy codes in an internal register array. The BEP appends check bits to the written data on the disk. The observed error rates for the system are one soft error for each million blocks read. The probability that an error is not detected is 2×10^{-1}.

The BEP corrects all single burst errors below 12 bits long. The error burst can be over 11 bits, or a double burst can occur. In this occurrence, a limited possibility that a data miscorrection to a different valid code word is present. This miscorrection is the primary reason for an error rate that is not seen. The BEP can perform a correction on any block in a maximum of 120 ms for each attempt.

Buffer memory

The buffer memory comprises a 3 Kbyte-by-8-bit memory interfaced on the microprocessor buses. The buffer memory stores data that you write to and read from the disk. The data store is partitioned into twelve 256 byte pages. Three of the 256 byte pages are reserved for disk controller workspace, storing log information. The pages are also reserved for the maintenance of configuration maps and drive variables.

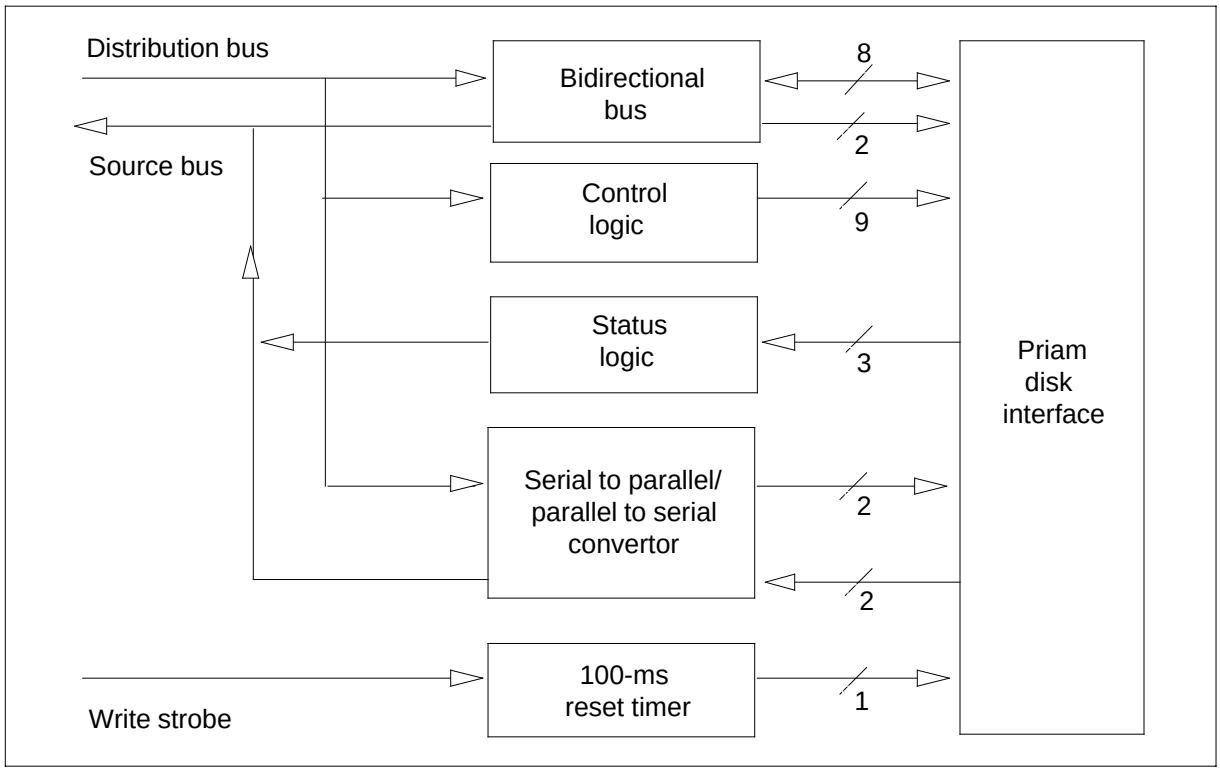
Disk interface

The disk interface can have the following functional parts:

- a bidirectional bus
- control and status signals
- data conversion signals
- clock switch, synchronization, and reset logic

The relationship with the functional blocks of the disk interface appears in the figure that follows.

NT1X55FA functional blocks for the disk interface



NT1X55FA (continued)

The 8-bit bidirectional bus between the disk controller and the control processor associated with the disk performs the following:

- sends commands to the disk drive. The commands are spin up, spin down, seek restore, and reset fault indication
- loads target cylinder addresses
- reads the disk status or the current cylinder address

The bus is in the positive logic mode. Two positive-logic address bits determine that the register writes on or reads from the disk. You can test the bus separate from the disk for maintenance purposes.

Several discrete control and status signals are available on the interface. These signals must provide the disk controller with real time control of the disk read and write electronics.

The disk control functions appear in the following table.

Disk control functions

Control kines	Number	Function
USEL -	2	selects one of two disks
WGATE-/RGATE	2	enables read and write electronics
HEAD/	3	encoded to select one of eight heads (tracks)
ADD+/AD1+	2	selects target register for bus read and write
DSKRD-/DSKWR-	2	strobes in association with the bidirectional bus

The status line functions appear in the following table.

Status line functions

Status lines	Function
DRDY -	indicates drive is current, servos locked on track
INDEX -	provides a servo pulse from the control track one time in each rotation
SECTOR -	pulses to indicate the start of each sector

The data conversion logic circuit converts non-return-to-zero (NRZ) serial data. This circuit converts data from the disk to an 8-bit representation for the disk controller. The circuit converts 8-bit parallel data from the disk controller to NRZ serial data for transmission to the disk.

The three types of synchronization required during serial input and output operations are as follows:

- The first type of synchronization is to the rotation of the disk. Poll an index mark and wait for sector pulses to accomplish this synchronization. You can also wait for sector pulses to accomplish this synchronization. The control tracks on the media generate both types of synchronization. Both types provide total rotational references free of any differences in disk motor speed.
- The second type of synchronization is when the disk generates clock synchronization of the disk controller microprocessor to the data clock. This synchronization occurs in the hardware clock switch circuitry.
- The third type of synchronization is byte synchronization to the serial data stream. During write operations, a firmware write to the parallel-to-serial converter of the special data synchronization character establishes the byte-synchonization. For the read operation, hardware that waits for the same character performs data synchronization.

Select a disk and the disk provides a reference clock. If the system asserts the read gate, a phase-locked oscillator extracts the clock from encoded data. If the system does not assert the read gate, the servo head derives the clock from the disk media. In both occurrences, the clock varies in frequency as the motor speed changes. To make sure the firmware runs in synchronization with the disk, the main clock can be switched from the 8 MHz IOC-CLK. The clock can be switched to the disk-generated REF-CLK (about 8.3 MHz).

The reset timer allows the disk controller to apply a 100 ms reset strobe to the disk drive. The controller applies the strobe through assertion of a single write strobe.

Technical data

This section describes the technical specifications for the disk drive controller that include:

- IOC bus requirements
- disk interface requirements
- disk DIP switch settings
- power requirements

NT1X55FA (continued)

- environmental conditions
- equipment dimensions

IOC bus specifications

Technical data for the IOC bus includes specifications for address lines, control lines, and data lines.

The specifications for the address lines are as follows:

- 16 lines that have one direction with Schottky transition to transition logic (TTL) line drivers and low power Schottky receivers
- terminations of 270 ohms to +5 V and 470 ohms-to-ground

The specifications for the control lines are as follows:

- 4 lines that have one direction with open connector Schottky TTL line drivers and low power Schottky hysteresis receivers
- terminations of 270 ohms to +5 V and 470 ohms-to-ground

The specifications for the data lines are as follows:

- 8 bidirectional lines with Schottky TTL line drivers and low power Schottky receivers
- terminations of 270 ohms to +5 V and 47 ohms-to-ground

Disk interface specifications

Disk interface specifications appear in the following table.

Disk interface specifications (Sheet 1 of 2)

Component	Specifications
Data lines	eight bidirectional lines
Data code	NRZ
Address lines	two lines that have one direction
Control lines	12 unidirectional lines that have one direction
Status logic	three lines that have one direction
Serial interface	two sets of two lines that have one direction
Reset strobe	one line that has one direction
Connecting cables	two with maximum length of 5.49 m (18 ft)

Disk interface specifications (Sheet 2 of 2)

Component	Specifications
Disk types	Priam 3350-10 Priam 6650-10 Priam 15450-10

Disk DIP switch settings

For correct operation with DMS-100 Family equipment, you must set the DIP switches on the disk as indicated in the following table.

Disk DIP switch settings (Sheet 1 of 2)

Group Location				
Single PCB	**Split PCB**	**Switch number**	**Switch function**	**Switch setting**
10 K	1 J	1	Unit Select 1	On
		2	Unit Select 2	Off
		3	Unit Select 3	Off
		4	Unit Select 4	Off
		5	Skip defect protection	On
		6	Write enable	On
		7	Clock transmit	On
		8	Clock phase	On
11 K	9 F	1	1 sector / track	Off
		2	2 sectors / track	On
		3	4 sectors / track	Off
		4	8 sectors / track	Off
		5	16 sectors / track	On
		6	32 sectors / track	Off

NT1X55FA (end)

Disk DIP switch settings (Sheet 2 of 2)

Group Location				
Single PCB	**Split PCB**	**Switch number**	**Switch function**	**Switch setting**
		7	64 sectors / track	Off
		8	reserved	Off

Power requirements

The power requirements appear in the following table.

Power requirements

Type of Power	Amount
Voltages required	+5 V
Current required	4.5 A

Environmental conditions

The disk drive controller performs under limited environmental conditions that appear in the following table.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	10°C to 30°C	5°C to 49°C
	(50°F to 86°F)	(41°F to 120.2°F)
Relative humidity	20% to 55%	20% to 80%

Note: A relative humidity of 80% is expected at an ambient temperature of 21°C (69.8°F) maximum. At an ambient temperature of 49°C (120.2°F), the relative humidity is expected to be 30% maximum.

Equipment dimensions

The disk drive controller dimensions are:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 213 mm (0.84 in.)
- weight: 820 grams (1.8 lb)

NT1X58AA

Product description

The NT1X58AA service trunk module (STM) has two reduced-size versions of the maintenance trunk module (MTM) in a single module. Each STM unit links channels from the network modules (NM) to channels on service circuit cards in the STM. Each STM unit functions as a switching center for control messages. The control module (CM) of the DMS-core and the separate test or service circuit packs exchange these messages. Internally, the STM provides the necessary low-voltage supplies and the connections needed to exchange data. This data exchange occurs between the service circuit packs (CP) and the common control circuits.

Each STM in the module functions as one module. Each has a common control CPs and service packs. The NT4X65AB control section includes network interface (NI), processor, and control CPs that produce and maintain connections. Two buses exchange data between the service CPs (XDAT or RDAT buses are not used). The two buses are maintenance (MAINT) 1 and 2. Each STM in a module has a power converter. Each STM in a module has a maximum of 6 or 7 service CPs. A maximum of 13 service CPs are in a single module.

The STM provides digital and analog looparound provisions. For digital looparound, the RDAT bus loops back to the XDAT bus. The RDAT bus loops back to the RDAT/XDAT connections to the trunk logic circuits (TLC) in the service CPs. The RPAM bus is looped to the XPAM bus for analog looparound. The common control section, which sends messages addressed to the different service cards as necessary, controls both looparounds.

Looparound circuits are in each service card for channel-specific looparound tests. The common control section, which addresses specified test or service cards through their TLC, controls these circuits.

Parts

The STM has service CPs, the NT2X70AD power converter &0xb1;5V and 12V CP, and the NT4X65AB trunk module (TM) control card CP.

Service circuit packs

Maintenance programs reside in the control module of the DMS-core. These programs control the service CPs. The service CPs use the MAINT buses. The software provides the correct control codes and enabling signals. These codes and signals operate in with the service CPs in the STM.

The separate STMs in the STM are reduced in size. Because of this condition, limits apply to the service CPs that are available for use. A maximum of 6 or

NT1X58AA (continued)

7 service CPs for each STM in the module are present. Service CPs (CPs without external connections), not test CPs, are available for use. The service CPs with -12 V, -5 V, +5 V, and +12 V dc power supply requirements can be installed.

Refer to the following table for a list of the service CPs available for use in the STM. The table list the slots in which to install the service CPs.

NT1X58AA parts

PEC	Slot	Description
NT4X65AB	4, 12	TM controllers
NT2X70AD	1, 20	Power converters
NT2X48AB	5-13, 13-18	4-Channel DTMF or MF receiver
NT3X67AA	5-8, 10, 13-16, 18	6-Port conference circuit
NT3X68BA	5-11, 13-18	Tone generator, PRMT/PST/CONF
NT5X29AC	5, 13	Digital tone detector and sender
NT1X31AA	5-8, 10, 13-16, 18	3-Port conference circuit
NT1X00AB	5-11, 13-18	102 Test trunk or receiver-off-hook tone
NT1X90AA	6, 8, 10, 14, 16	Test signal generator
NT2X96AA	7, 9, 11, 15, 17	PCM level meter
NT2X47AB, -AC	6, 8, 10, 14, 16	Transmission test controller
NT2X56AA, -AB	7, 9, 11, 15, 17	TTM digital filter
NT2X75AA	5-11, 13-18	Looparound test line
NT3X02AA	6, 8, 10, 14, 16	Control processor
NT3X03AA	7, 9, 11, 15, 17	Digital signal processor

Note: The NT2X47AB, AC, NT2X56AA, AB are part of the transmission test unit. The NT3X02AA and NT3X03AA are part of TOPS control.

Design

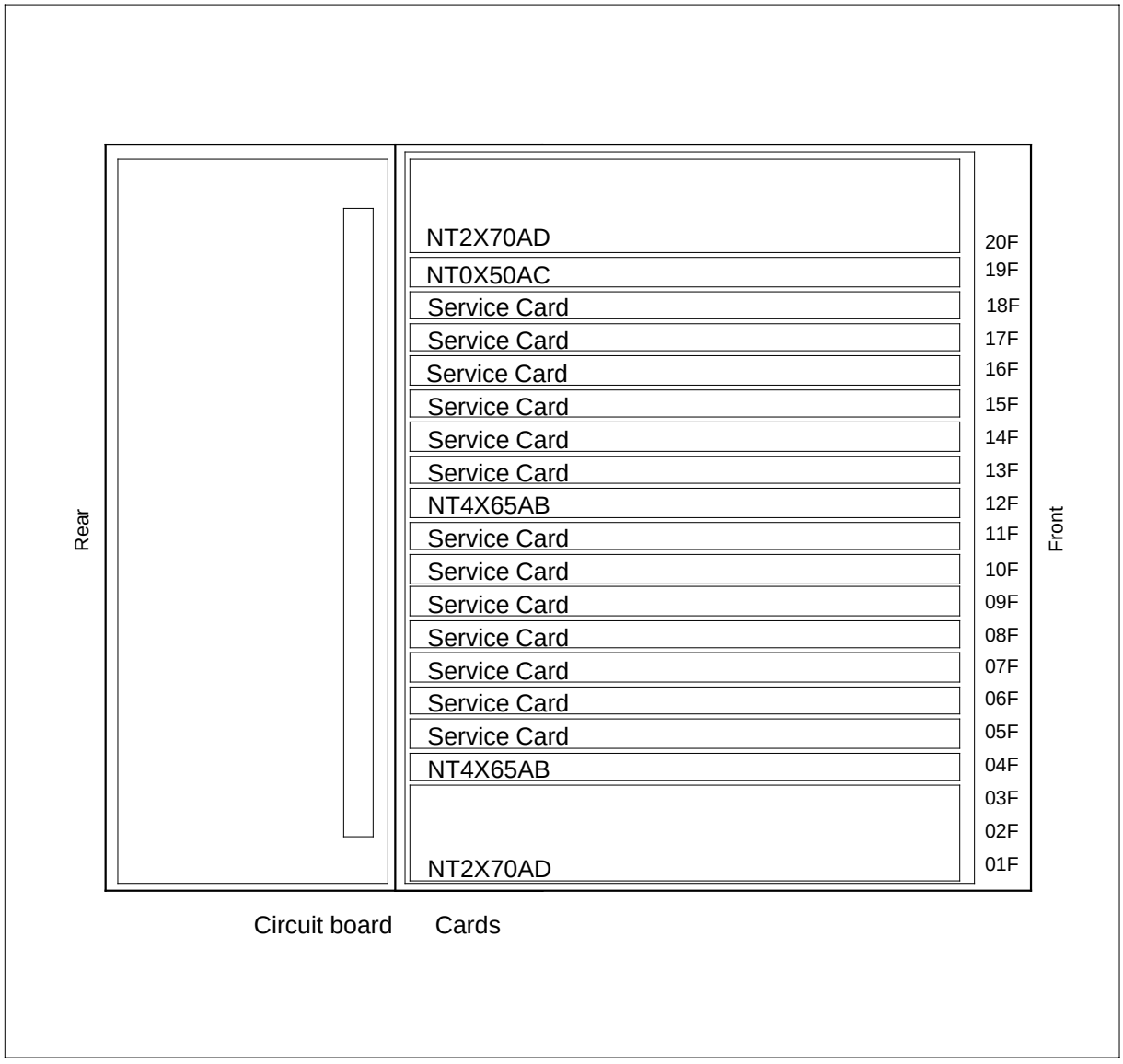
The design of the NT1X58AA appears in the following table and figure.

NT1X58AA part design

PEC	Slot	Description
NT2X70AD	1F, 20F	*Power converter* The power converters (NT2X70AD) convert the -48V dc to the lower voltages (-5V, -15V, +5V, and +15V dc) the CPs need in the module. Two power converters in the STM, one for STM-0 and one for STM-1 are present. The converters include overvoltage and overcurrent protection circuits, light-emitting diode (LED) status indicators, faceplate test jacks and a low-voltage monitor circuit. The power converters also include a low-voltage shutdown alarm.
NT4X65AB	4F, 12F	*Trunk module control card circuit pack* The TM control card CP contains the NI, processing, and control circuits for each STM in an STM module. The NI provides two bi-directional interfaces for the two transmission paths from both network planes. The NI contains message registers, bit and channel timing circuits, parity-checking circuits, and circuits that format data again. The processor performs or controls all operations of the components of the STM accomplish. The processor includes a firmware-driven microprocessor and two RAMs. One RAM stores program information and the other one stores operational information. Operational information includes connection information for PCM channel-to-trunk assignments. The RAM processor includes circuits that generate the clock signal, check parity, and perform synchronization. The control section has the circuit controllers that handle different messages. The control section exchanges information with the processor CP over data and address buses. The control section produces enable signals for the circuits on the service and test CPs.

NT1X58AA (end)

NT1X58AA parts



NT1X61AB

Product description

The input/output controller (IOC) provides an interface between a pair of central message controllers (CMC) and a maximum of nine microprocessor-based device controllers (DC). The IOC relays central control (CC)-generated messages through the CMC to input/output (I/O) DCs. The IOC accepts messages from DCs for transmission to the CC. The maximum number of IOCs that the system can use in the DMS-100 Family is six pairs.

Each IOC can receive and transmit messages on two 2.56 Mbps serial ports to a pair of CMCs (CMC-0, CMC-1). Each IOC can receive and transmit on one parallel data bus to the DCs.

The IOC performs serial-to-parallel and parallel-to-serial conversions on the data to and from DCs in the order given. The IOC performs the standard DMS serial transmission protocol on the serial ports. The IOC interfaces the DCs on an 8-bit parallel bus.

In an idle state, the IOC always monitors the serial ports for message transmission requests. The IOC monitors the DCs for transmission requests, sanity timeouts, and error flag indicators on received messages that are not correct.

The limit of message transmission between the DCs and central processor, through the CMC and IOC, is 256 bytes.

The NT1X61AB IOC has the following important characteristics:

- employs one common control card, which uses low-power Schottky logic
- transmission of messages from the IOC to the DC is asynchronous
- performs checksum integrity checks on all data transfers
- uses a selective reset capability for all DCs
- can receive and transmit maintenance messages through the internal 256 byte memory of the IOC

Parts

The NT1X61AB has DC cards; the NT1X67AB, and a group of the following parts:

- NT0X50AA-Filler faceplate 0.875
- NT0X50AF-Filler faceplate 1.75
- NT0X67AA-IOC terminator

NT1X61AB (continued)

- NT1X55AB-Disk drive controller
- NT1X62AB-I/O controller
- NT1X67-Data link controller
- NT1X68BD-Magnetic tape unit controller
- NT1X89BA-Enhanced multiprotocol controller
- NT2X70AA-Power converter, ±V/12V
- NT6X91AA/AB-Mobile telephone exchange link controller

Design

Descriptions of the parts that comprise the shelf appear in the following table.

NT1X61AB parts (Sheet 1 of 2)

PEC	Slot	Description
NT0X50AA	1F, 5F, 7F, 9F, 11F, 13F, 15F, 17F, 19F, 21F	*Filler faceplate .875* The NT0X50AA fills in circuit pack (CP) slots that are not used.
NT0X50AF	23F	*Filler faceplate 1.75* The NT0X50AF fills in slot 23F on the IOC shelf.
NT0X67AA	22F	*Input/output control terminator circuit pack* The NT0X67AA provides terminating resistors for the parallel bus of the IOC.
NT1X55AB	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Disk drive controller circuit pack* The NT1X55AB provides an interface between the CC and the corresponding disk drive.
NT1X62AB	2F	*I/O message controller circuit pack* The NT1X62AB performs the main activities of the IOC shelf. The NT1X62AB transmits and receives messages on two 2.56 Mbps serial ports, one to each CMC and one parallel port to the DCs. The NT1X62AB performs serial-to-parallel and parallel-to-serial conversions on data. The NT1X2AB performs the transmission protocol on the serial ports.
NT1X67	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Data link controller circuit pack* The NT1X67 provides an interface between the CC and the corresponding I/O device.

NT1X61AB (continued)

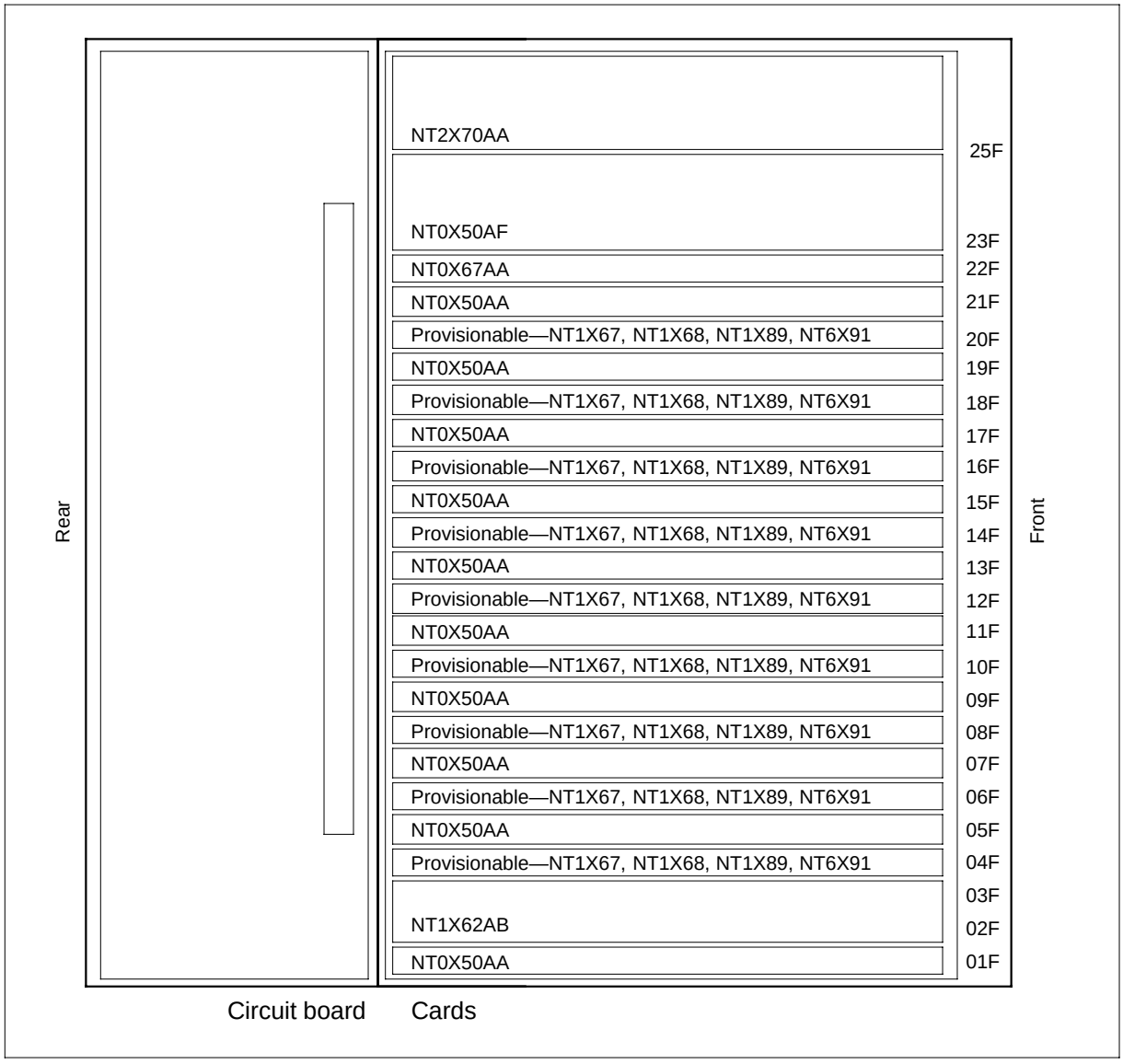
NT1X61AB parts (Sheet 2 of 2)

PEC	Slot	Description
NT1X68BD	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Magnetic tape unit controller circuit pack* The NT1X68BD provides an interface between the CC and the corresponding magnetic tape unit.
NT1X89BA	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Enhanced multiprotocol controller circuit pack* The NT1X89BA is a general purpose data communications board.
NT2X70AA	25F	*Power converter, ±5V/12V* The NT2X70AA provides the IOC shelf with a regulated dc power supply with an output of ±5V or 12V, 40A. Input to the converter comes from a nominal -48V dc office battery.
NT6X91AA or AB	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Mobile telephone exchange link controller circuit pack* The NT6X91 provides a mobile telephone exchange link between the CC and the corresponding peripheral unit.

The design of the NT1X61AB appears in the following figure.

NT1X61AB (end)

NT1X61AB design



NT1X61AD

Product description

The input/output controller (IOC) provides an interface between a pair of central message controllers (CMC) and a maximum of nine microprocessor-based device controllers (DCs). The IOC relays central control (CC)-generated messages through the CMC to input/output (I/O) DCs. The IOC accepts messages from DCs for transmission to the CC. The maximum number of IOCs for use in the DMS-100 Family is six pairs.

Each IOC can receive and transmit messages on two 2.56 Mbps serial ports to a pair of CMCs (CMC-0, CMC-1). Each IOC can receive and transmit on one parallel data bus to the DCs.

The IOC performs serial-to-parallel and parallel-to-serial conversions on the data to and from DCs in the order given. The IOC performs the standard DMS serial transmission protocol on the serial ports. The IOC interfaces the DCs on an 8-bit parallel bus.

In an idle state, the IOC always monitors the serial ports for message transmission requests. The IOC monitors the DCs for transmission requests, sanity timeouts, and error flag indicators on incorrectly received messages.

The limit on message transmission between the DCs and central processor, through the CMC and IOC, is 256 bytes.

The NT1X61AD IOC has the following important characteristics:

- employs one common control card, which uses low-power Schottky logic
- transmission of messages from the IOC to the DC is asynchronous
- performs checksum integrity checks on all data transfers
- uses a select reset capability for all DCs
- can receive and transmit maintenance messages through the internal 256 byte memory of the IOC

Parts

The NT1X61AD contains the DC cards, like the NT1X67AB, and a group of these other parts:

- NT0X50AA-Filler faceplate 0.875
- NT0X50AF-Filler faceplate 1.75
- NT0X67AA-IOC terminator
- NT1X55AB-Disk drive controller

NT1X61AD (continued)

- NT1X62AB-I/O controller
- NT1X67-Data link controller
- NT1X68BD-Magnetic tape unit controller
- NT1X89BA-Enhanced multiprotocol controller
- NT2X70AA-Power converter, ±V/12V
- NT6X91AA/AB-Mobile telephone exchange link controller

Design

Descriptions of the parts that comprise the NT1X61AD shelf appear in the following table.

NT1X61AD parts (Sheet 1 of 2)

PEC	Slot	Description
NT0X50AA	1F, 5F, 7F, 9F,11F, 13F, 15F,17F, 19F, 21F	*Filler faceplate .875* The NT0X50AA fills in circuit pack (CP) slots that are not used.
NT0X50AF	23F	*Filler faceplate 1.75* The NT0X50AF fills in slot 23F on the IOC shelf.
NT0X67AA	22F	*Input/output control terminator circuit pack* The NT0X67AA provides terminating resistors for the parallel bus of the IOC.
NT1X55AB	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Disk drive controller circuit pack* The NT1X55AB provides an interface between the CC and the corresponding disk drive.
NT1X62AB	2F	*I/O message controller circuit pack* The NT1X62AB performs the main activities of the IOC shelf. The NT1X62AB transmits and receives messages on two 2.56 Mbps serial ports, one to each CMC and one parallel port to the DCs. The NT1X62AB also performs serial-to-parallel and parallel-to-serial conversions on data. The NT1X62AB performs the transmission protocol on the serial ports.
NT1X67	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Data link controller circuit pack* The NT1X67 provides an interface between the CC and the corresponding I/O device.

NT1X61AD (continued)

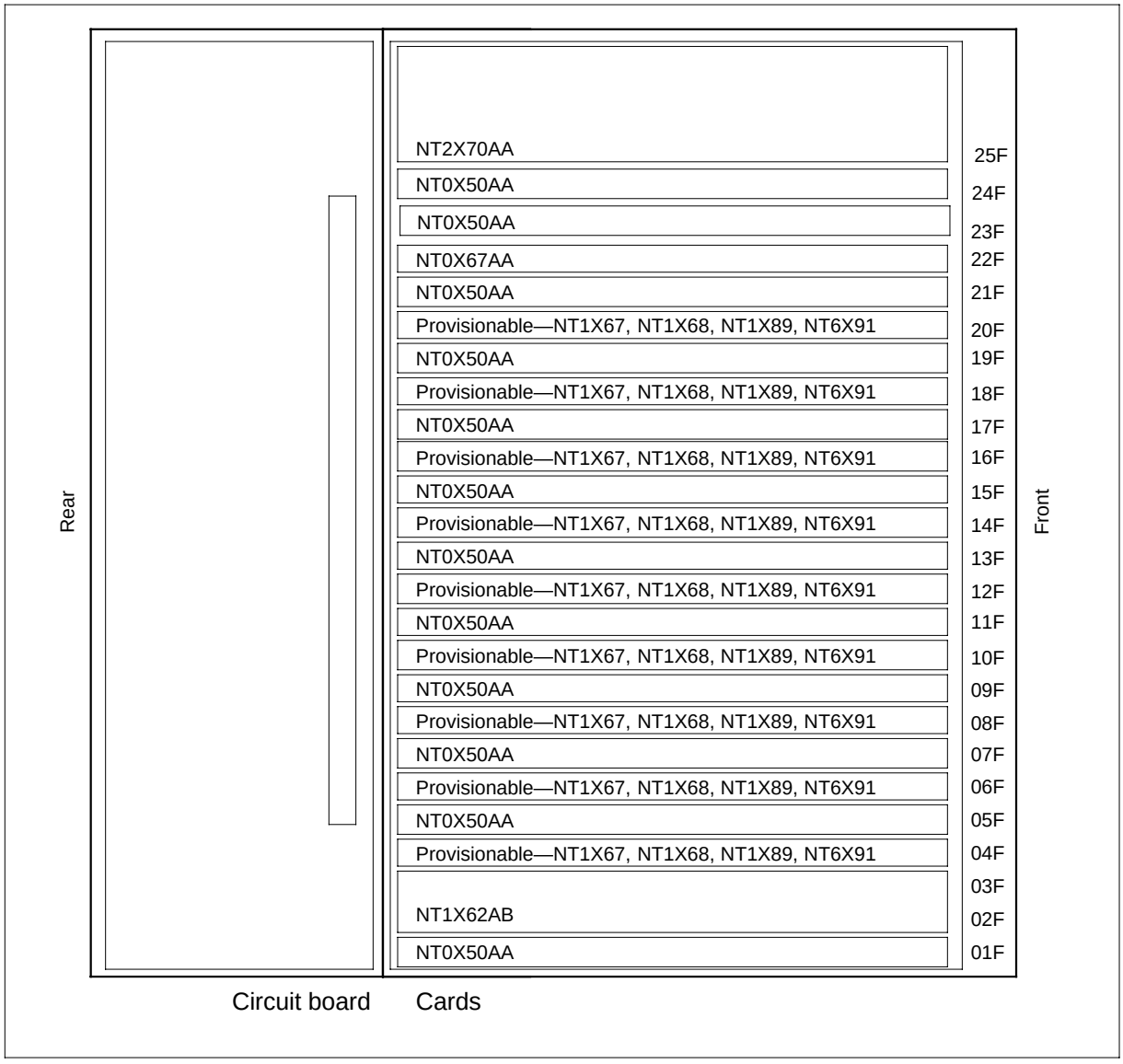
NT1X61AD parts (Sheet 2 of 2)

PEC	Slot	Description
NT1X68BD	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Magnetic tape unit controller circuit pack* The NT1X68BD provides an interface between the CC and the corresponding magnetic tape unit (MTU).
NT1X89BA	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Enhanced multiprotocol controller circuit pack* The NT1X89BA a general purpose data communications board.
NT2X70AA	25F	*Power converter,±5V/12V* The NT2X70AA provides to the IOC shelf a regulated dc power supply with an output of ±5V or 12V, 40A. Input to the converter comes from a nominal -48V dc office battery.
NT6X91AA or AB	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Mobile telephone exchange link controller circuit pack* The NT6X91 provides a mobile telephone exchange link between the CC and the corresponding peripheral unit.

The design of the NT1X61AD appears in the following figure.

NT1X61AD (end)

NT1X61AD design



NT1X61AG

Product description

The input/output controller (IOC) provides an interface between a pair of central message controllers (CMC) and a maximum of nine microprocessor-based device controllers (DCs). The IOC relays central control (CC) generated messages through the CMC to input/output (I/O) DCs. The IOC accepts messages from DCs for transmission to the CC. The maximum number of IOCs available for use in the DMS-100 Family is six pairs.

Each IOC can receive and transmit messages on two 2.56 Mbps serial ports to a pair of CMCs (CMC-0, CMC-1). Each IOC can receive and transmit on one parallel data bus to the DCs.

The IOC performs serial-to-parallel and parallel-to-serial conversions on the data to and from DCs in the order given. The IOC performs the standard DMS serial transmission protocol on the serial ports. The IOC interfaces the DCs on an 8-bit parallel bus.

In an idle state, the IOC always monitors the serial ports for message transmission requests. The IOC monitors the DCs for transmission requests, sanity timeouts, and error flag indicators on incorrectly received messages.

The limit on message transmission between the DCs and central processor, through the CMC and IOC, is 256 bytes.

The NT1X61AG IOC has the following important characteristics:

- employs one common control card, which uses low-power Schottky logic
- transmission of messages from the IOC to the DC is asynchronous
- performs checksum integrity checks on all data transfers
- uses a selective reset capability for all DCs
- can receive and transmit maintenance messages through the use of its internal 256 byte memory

Parts

The NT1X61AG consists of DC cards, like the NT1X67AB, and a group of these other parts:

- NT0X50AA-Filler faceplate 0.875
- NT0X67AA-IOC terminator

NT1X61AG (continued)

- NT1X62AB-I/O controller
- NT2X70AA-Power converter, ±5/12V

Design

Descriptions of the parts that comprise the NT1X61AG shelf appear in the following table.

NT1X61AG parts (Sheet 1 of 2)

PEC	Slot	Description
NT0X50AA	1F, 5F, 7F, 9F,11F, 13F, 15F,17F, 19F, 21F,23F	*Filler faceplate .875* The NT0X50AA fills in circuit pack (CP) slots that are not used.
NT0X67AA	22F	*Input/output control terminator circuit pack* The NT0X67AA provides terminating resistors for the parallel bus of the IOC.
NT1X55AB	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Disk drive controller circuit pack* The NT1X55AB provides an interface between the CC and the corresponding disk drive.
NT1X62AB	2F	*I/O message controller circuit pack* The NT1X62AB performs the main activities of the IOC shelf. The IOC transmits and receives messages on two 2.56 Mbps serial ports, one to each CMC and one parallel port to the DCs. The NT1X62AB performs serial-to-parallel and parallel-to-serial conversions on data. The NT1X62AB performs the transmission protocol on the serial ports.
NT1X67	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Data link controller circuit pack* The NT1X67 provides an interface between the CC and the corresponding I/O device.
NT1X68BD	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Magnetic tape unit controller circuit pack* The NT1X68BD provides an interface between the CC and the corresponding magnetic tape unit (MTU).

NT1X61AG (continued)

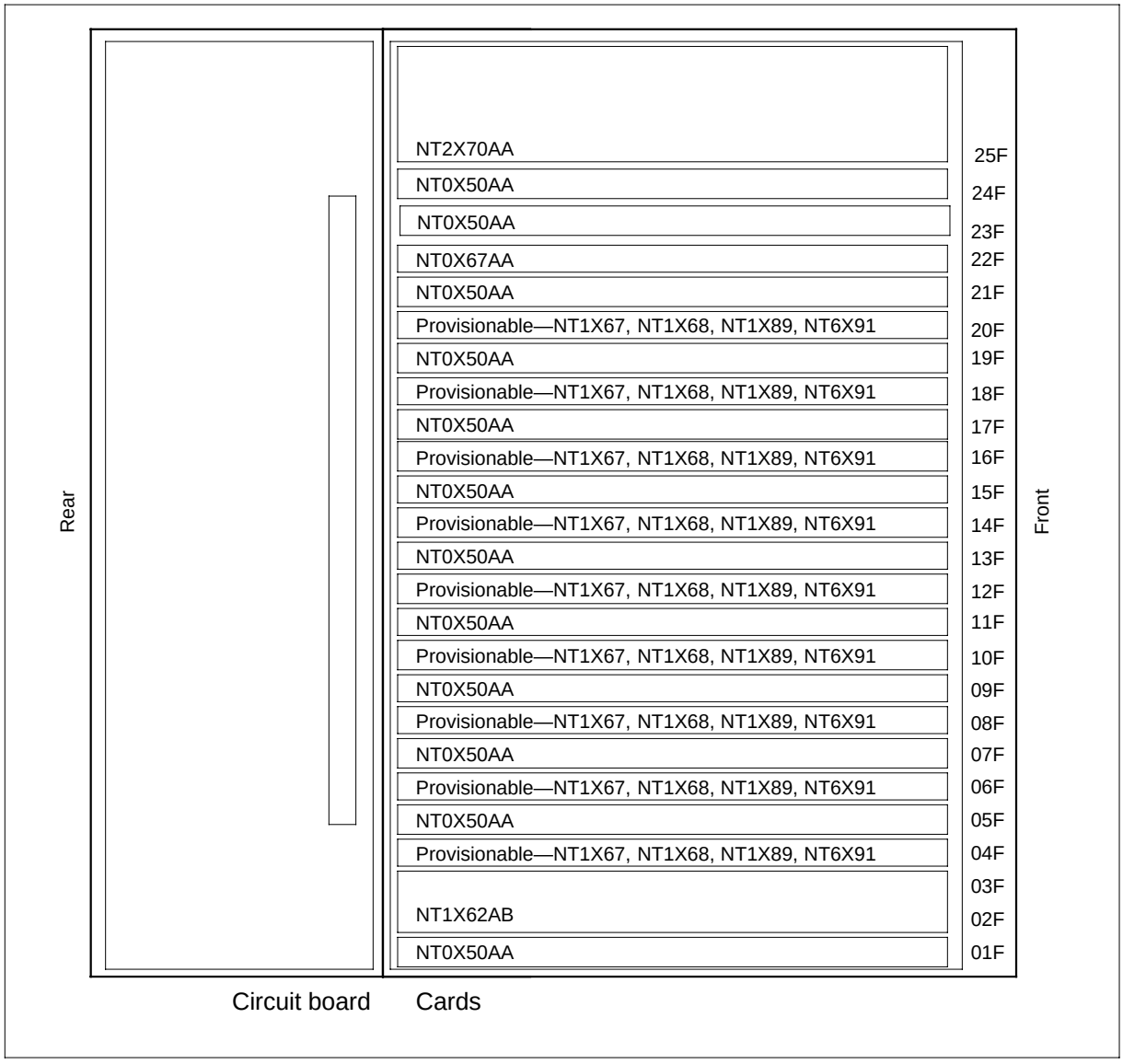
NT1X61AG parts (Sheet 2 of 2)

PEC	Slot	Description
NT1X89BA	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Enhanced multiprotocol controller circuit pack* The NT1X89BA is a general purpose data communications board.
NT2X70AA	25F	*Power converter, ±5V/12V* The NT2X70AA provides to the IOC shelf a regulated dc power supply with an output of ±5V or 12V, 40A. Input to the converter comes from a nominal -48V (dc) office battery.
NT6X91AA or AB	Provisionable: 4F, 6F, 8F,10F, 12F, 14F,16F, 18F, 20F	*Mobile telephone exchange link controller circuit pack* The NT6X91 provides a mobile telephone exchange link between the CC and the corresponding peripheral unit.

The design of the appears NT1X61AG in the following figure:

NT1X61AG (end)

NT1X61AG design



NT1X62AA

Product description

The NT1X62AA input/output controller (IOC) card provides an interface between the device controllers and the central control (CC). The card has serial interfaces to the central control and a parallel interface to the device controllers.

Functional description

The NT1X62AA performs the following functions:

- transmits and receives messages on two 2.56 Mbps serial ports, one port for each central message controller (CMC)
- transmits and receives messages on one parallel port to the device controllers
- performs serial-to-parallel and parallel-to-serial conversions on the data, and initiates the transmission protocol on the serial ports

Functional blocks

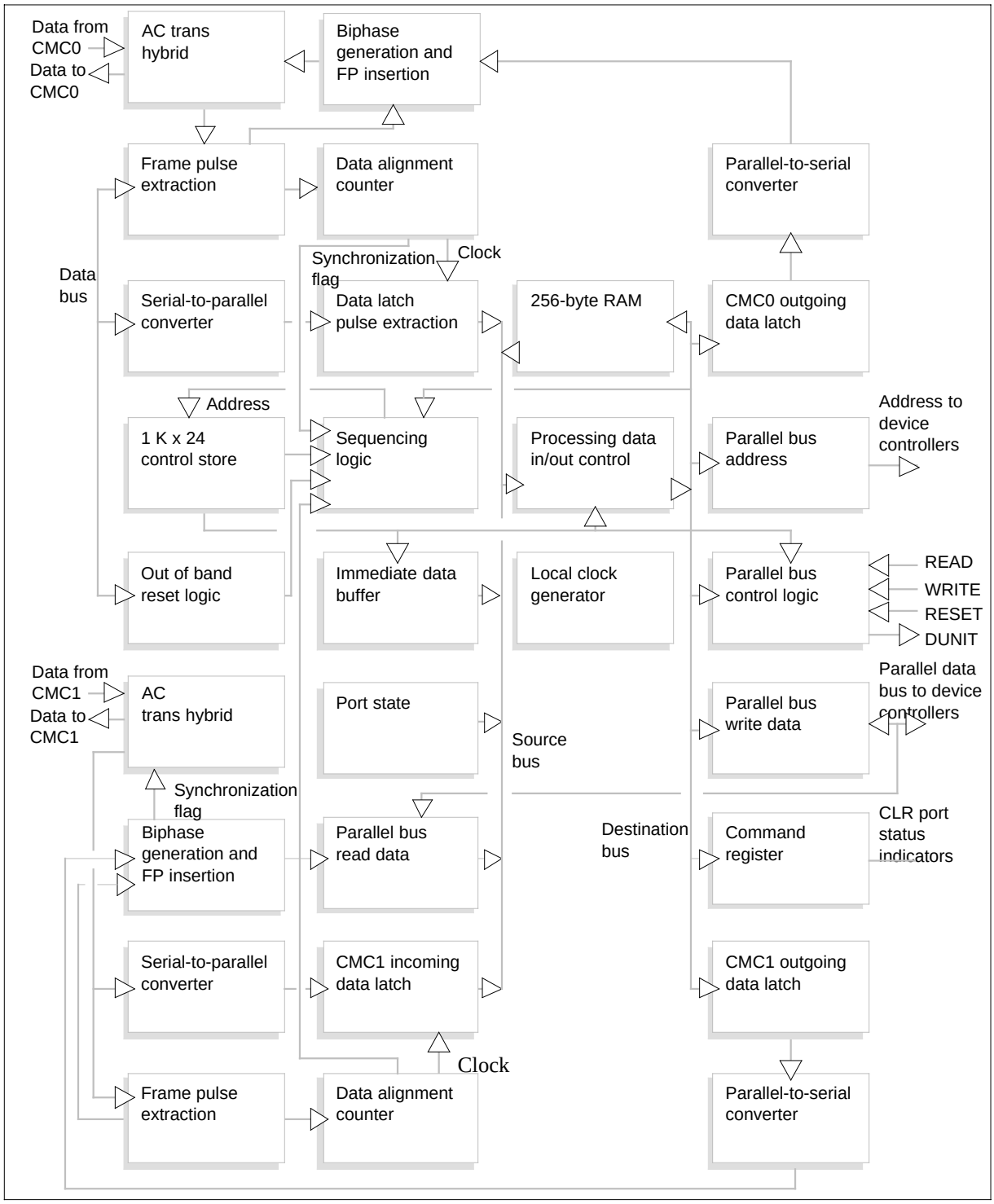
The NT1X62AA has the following functional blocks:

- serial ports logic
- microprocessor
- parallel bus control logic

The functional relationship of these parts appears in the following figure.

NT1X62AA (continued)

NT1X62AA functional blocks



Serial port logic

The serial port logic duplicates to provide an interface to both CMCs.

The serial port logic runs on a clock from received data. The data arrival flag signals between the two asynchronous segments of the logic.

Microprocessor

The microprocessor performs four functions:

- scans the serial ports and device interfaces for transmission requests
- delivers messages from the CC to device controllers and from the device controllers to the CC
- starts the standard DMS input/output system transmission protocol on the serial links
- acts a maintenance center for the IOC subsystem because the microprocessor can receive and generate messages

The microprocessor runs on a crystal clock. The cycle time is 347 ns. When serial port logic duplicates, the cycle can provide an interface to both CMCs.

Parallel bus control logic

The parallel bus control logic controls the flow of data between the device controllers and the message processor. The port control logic can also issue resets to device controllers.

Signaling

This section describes the protocol and timing for the NT1X62AA.

Protocol

Parallel bus protocol

The message processor controls the parallel bus and can perform the following three types of operations:

- read data from a different device controller address location
- write data to a different device controller address location
- reset a device controller

Serial links protocol

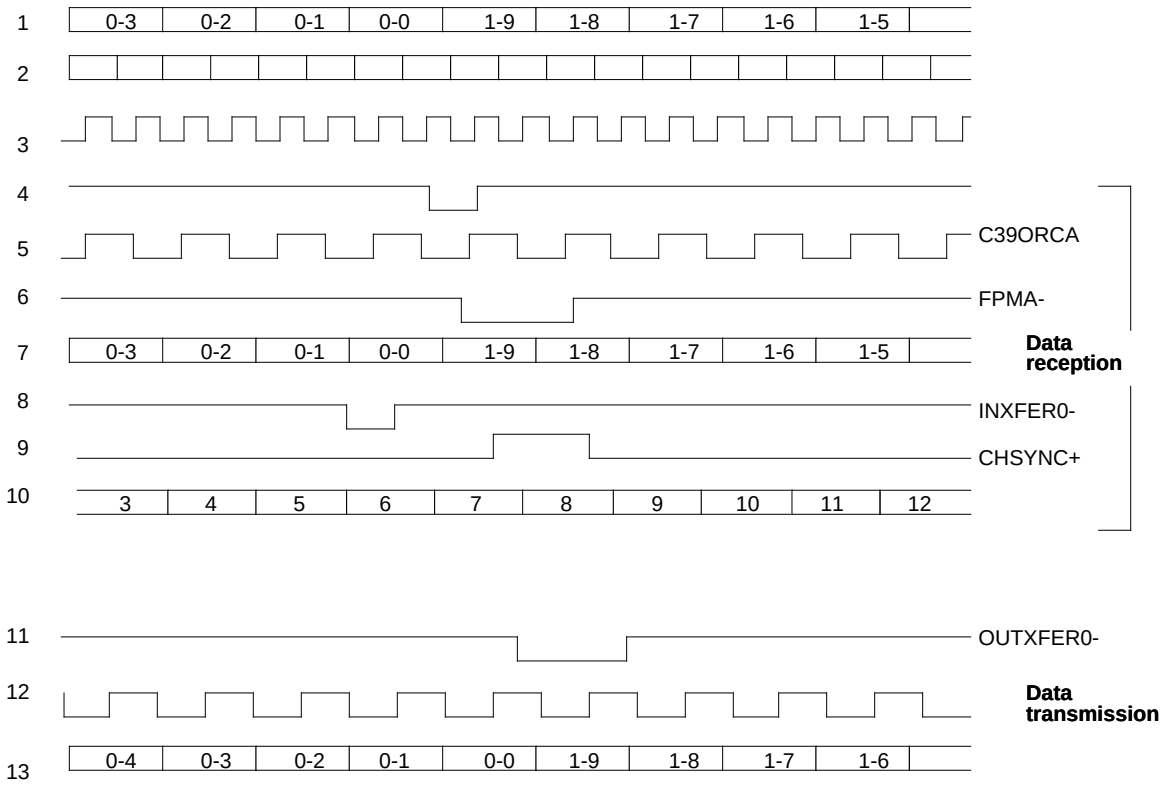
The standard DMS transmission protocol controls the flow of messages over the serial links.

Timing

The timing for the serial port appears in the following figure.

NT1X62AA (continued)

NT1X62AA serial port timing

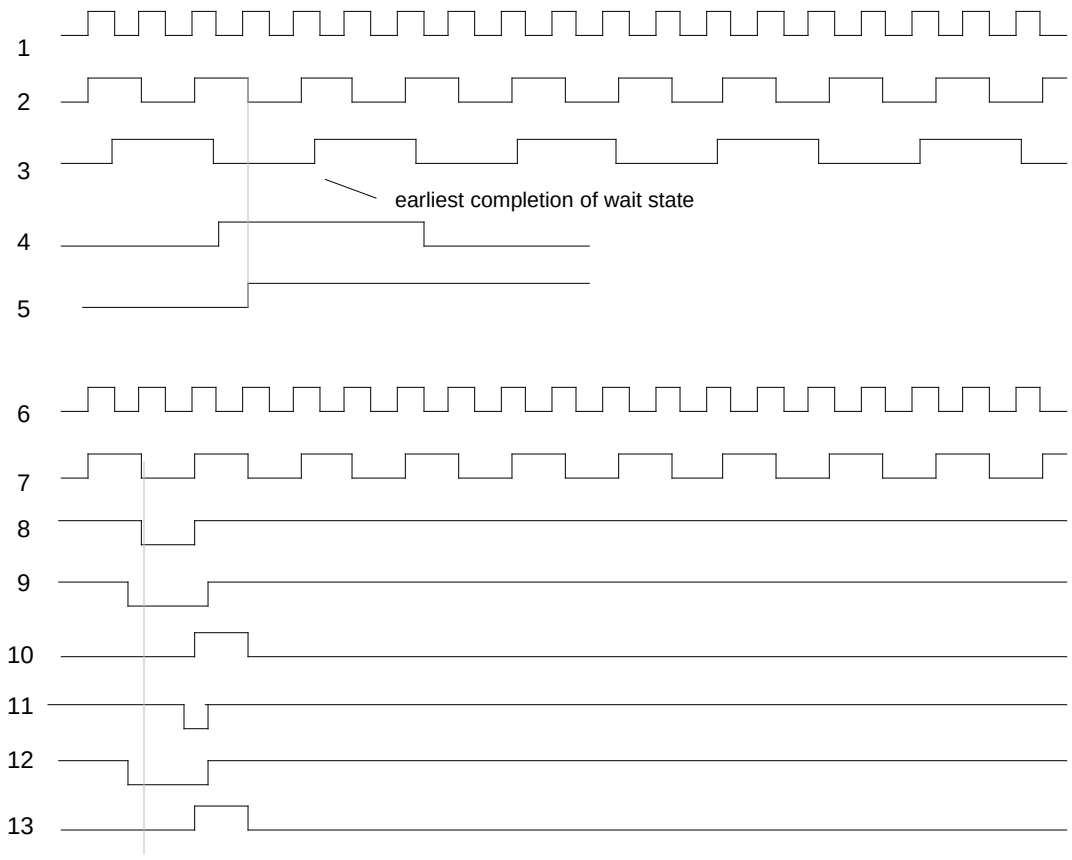


Legend

1. Incoming data (channel and bit)
2. Incoming Biphase
3. Received 195-ns clock
4. Decoded frame pulse
5. Received 390-ns clock
6. Latched frame pulse
7. Data at least significant bit of serial-to-parallel converter
8. Clock to transfer data to read latch
9. Data arrival flag
10. Data alignment counter
11. Data transfer outgoing to P/S converter enable
12. Data transfer clock
13. Serial data to coder (channel to bit)

The timing for the parallel port control appears in the following figure.

NT1X62AA parallel port timing



Legend

1. Oscillator
2. C175+
3. CLK2901+ and CLK2909+
4. Wait-
5. K of 2909 generator
6. Basic 174-ns clock
7. Microprocessor 347-ns clock
8. Microstore read to fxxt control logic
9. Read on bus
10. Digit latched by port control logic
11. Load signal to read data register
12. Write on bus
13. Digit latched by port control logic

NT1X62CB

Product description

The input and output message processor card (IOC) provides an interface between different device controllers and the central control (CC).
The NT1X62CB transmits and receives messages on two serial ports. The NT1X62CB transmits and receives messages on one parallel port to the device controllers. The NT1X62CB performs the DS30 transmission protocol on the central control-side (C-side) serial ports.

The NT1X62CB performs like the current NT1X62CA. To increase strength, the NT1X62CB uses a new DS30 interface. The DS30 interface uses a customized N03 integrated circuit (IC) device and a modified 00B reset circuit.

Location

The IOC shelf has the NT1X62CB.

Functional description

The NT1X62CB performs the following functions:

- transmits and receives messages on two 2.56 Mbps serial ports. The NT1X62CB transmits one message to each CMC.
- the serial ports are to each CME
- performs serial-to-parallel and parallel-to-serial conversions on the data
- performs the DS30 transmission protocol on the serial ports

Functional blocks

The NT1X62CB has of the following functional blocks:

- serial port logic
- microprocessor
- parallel bus control logic

Serial port logic

The serial port logic performs the DS30 interface functions. The customized N03 IC starts this function. The N03 device provides a reliable clock and frame pulse. This action can prevent resets.

Microprocessor

The 8-bit microprocessor performs the following functions:

- scans the serial ports and device interfaces for transmission requests
- delivers messages from the CC to the device controllers and from the device controllers to the CC

- starts the standard DS30 input/output system transmission protocol on the serial links
- acts as a maintenance center for the IOC subsystem because the microprocessor can receive and generate messages

The microprocessor has a 256 byte RAM that stores incoming and outgoing maintenance messages and buffers messages. This RAM buffers messages travel from the serial links to the device controllers for a short time. The microprocessor has port status registers that capture failure signals on the serial ports. Port status registers capture bus control lines on the parallel port.

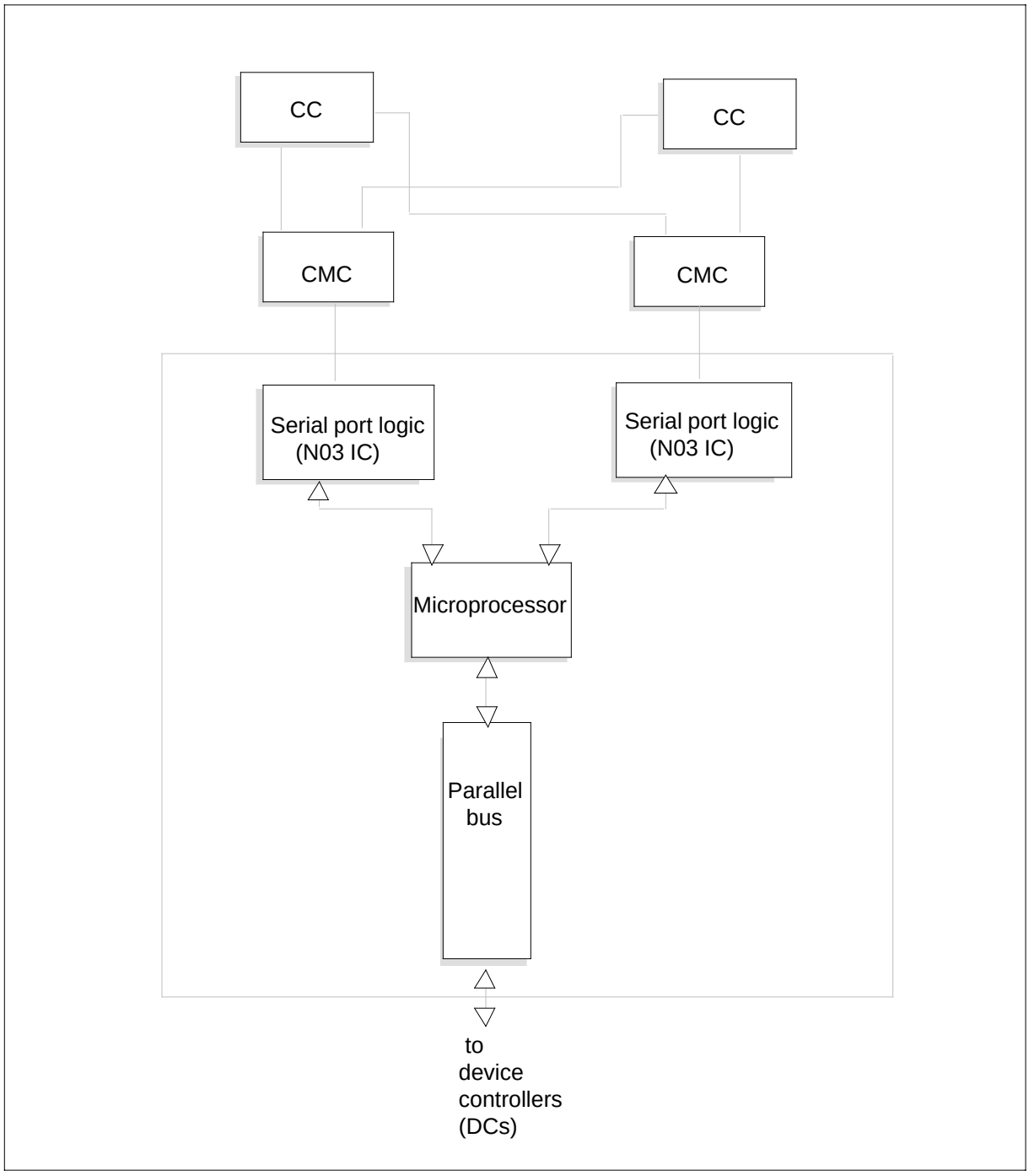
Parallel bus control logic

The parallel bus control logic controls the flow of data between the device controllers and the CMC. The port control logic issues resets to device controllers.

The relationship between the functional blocks appears in the following figure.

NT1X62CB (continued)

NT1X62CB functional blocks



Signaling

Protocol

Parallel bus protocol

The message processor controls the parallel bus and can perform the following operations:

- read data from a different device controller address location
- write data to a different device controller address location
- reset a device controller

Serial links protocol

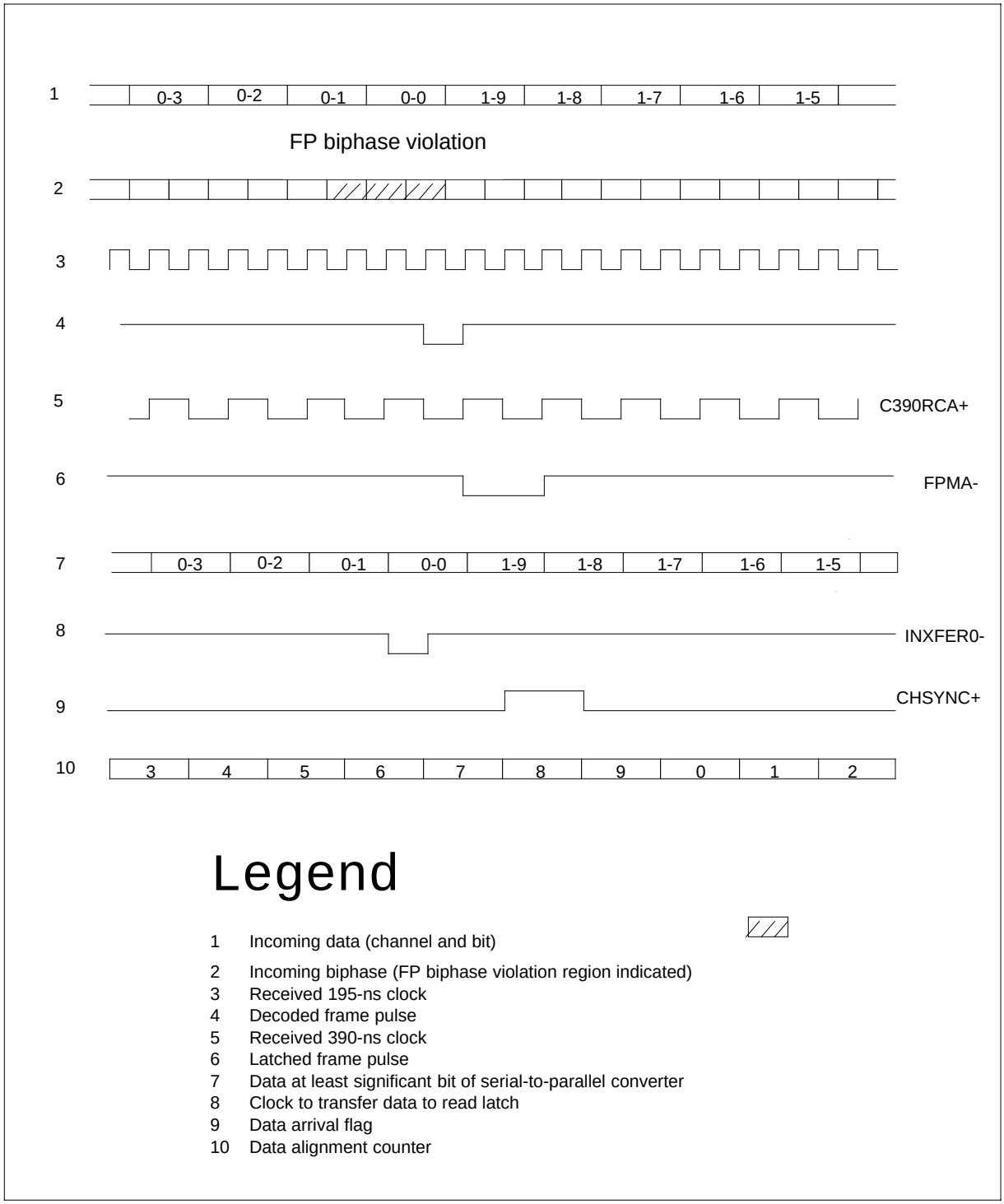
The standard DMS transmission (DS30) protocol controls the flow of messages over the serial links.

Timing

The timing for the serial port appears in the next two figures.

NT1X62CB (continued)

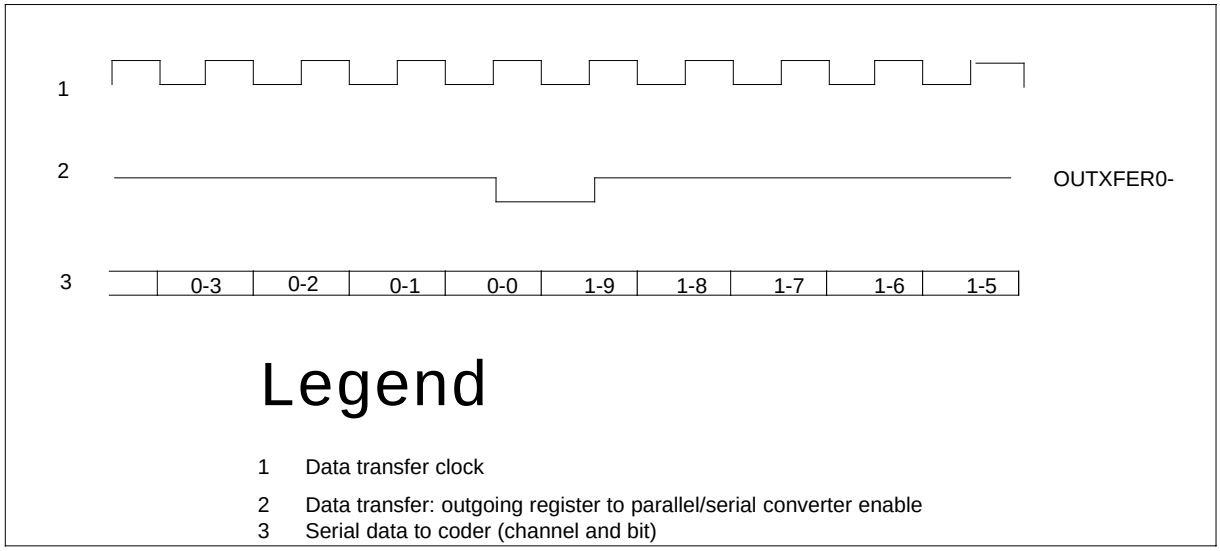
NT1X62CB serial port timing (incoming data)



Legend

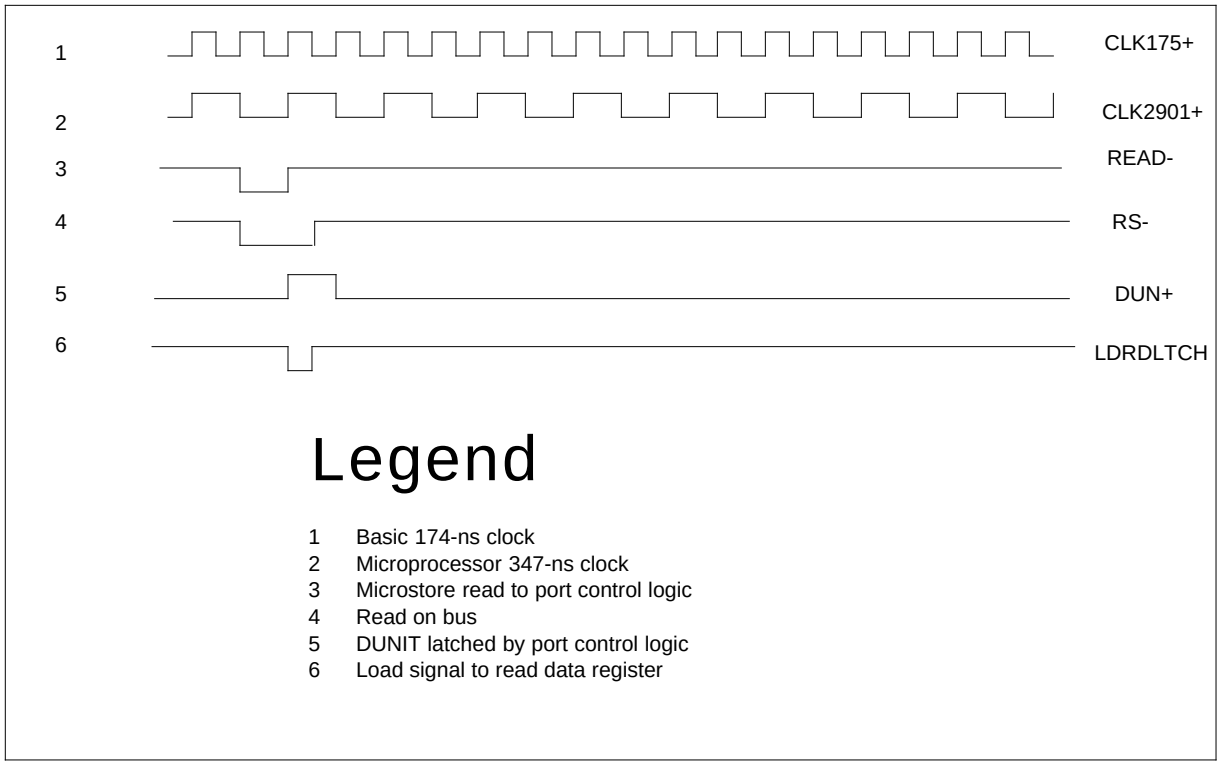
1 Incoming data (channel and bit)
2 Incoming biphase (FP biphase violation region indicated)
3 Received 195-ns clock
4 Decoded frame pulse
5 Received 390-ns clock
6 Latched frame pulse
7 Data at least significant bit of serial-to-parallel converter
8 Clock to transfer data to read latch
9 Data arrival flag
10 Data alignment counter

NT1X62CB serial port timing (outgoing data)



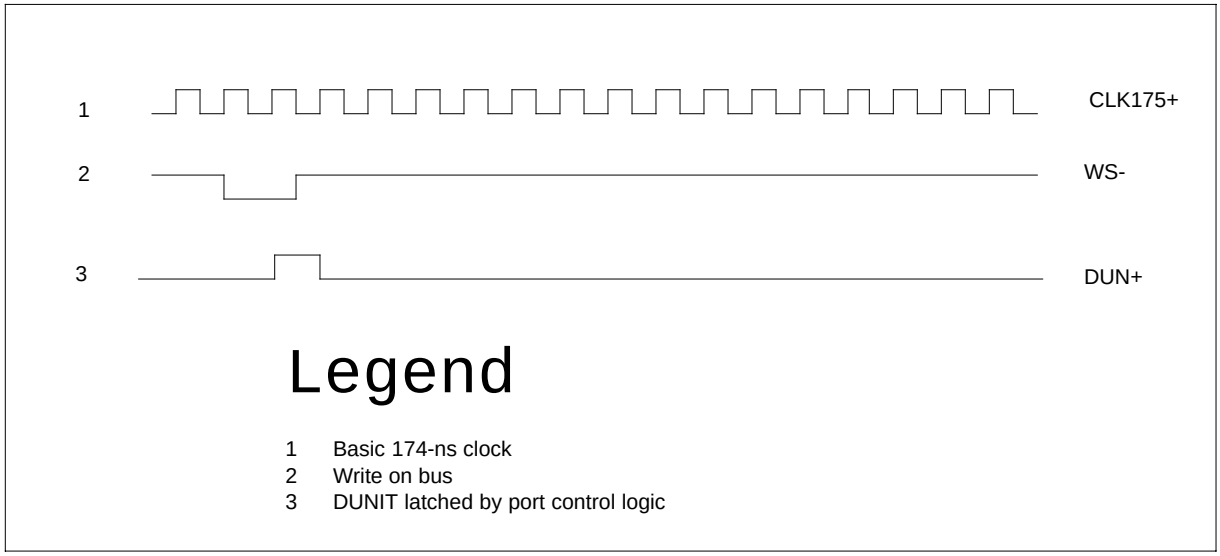
The timing for the parallel port control appears in the following two figures.

NT1X62CB parallel port timing (read cycle)



NT1X62CB (end)

NT1X62CB parallel port timing (write cycle)



Technical data

Power requirements

The required power supply for the is NT1X62CB +5 V.

NT1X67BD

Product description

The echo off line circuit card (NT1X67BD) interfaces input output devices (IOD) or data sets, with the central control (CC) through a input output controller (IOC) and a central message controller (CMC). Messages are transmitted from the CC on the IOC parallel bus.

The NT1X67BD circuit card is an asynchronous controller card. The NT1X67BD circuit card uses four data ports to transmit and receive data to and from the IOD and datalinks. The NT1X67BD circuit card occupies one card position in an IOC shelf or a central message and input output device controller shelf.

Functional description

The NT1X67BD circuit card has four separate ports for peripheral terminal devices. The firmware in this circuit card allows the terminals to communicate at higher speeds on all ports. The current specification requires a single port should not exceed 2400 bps. This alters the processing speed of the complete circuit card. The maximum bits for each second rate a single port in a special application (4800 bps) can support does not change. When a single port on a card exceeds 2400 bps, the following conditions apply:

- The terminal must support the higher bits for each second rate.
- The total of the bits for each second rate for all ports on a single card must not exceed 4800 bps (current loop) or 9600 bps electronic industries association (EIA).
- The NT1X67BD circuit card is used for user interface terminals, not data transfer.

Use the NT1X67BD circuit card in automatic dial back applications and for special editing functions.

Features of the NT1X67BD circuit card are:

- Each of the four data ports can use current loop or EIA interfacing.
- The NT1X67BD circuit card accepts resets for a single port or for all ports.
- The IOC can be used to program the terminal port configurations from a central processing unit (CPU).
- Each port can be set to active or standby. If the port is set to standby, the NT1X67BD circuit card ignores all activity on that port. The system sets input output messages to error.
- Data sets for service remote terminals can be private line or switched network and 300 or 1200 bps limited.

NT1X67BD (continued)

- The A EIA RS-232C interface interfaces data sets.
- Message loop back is available for tests.

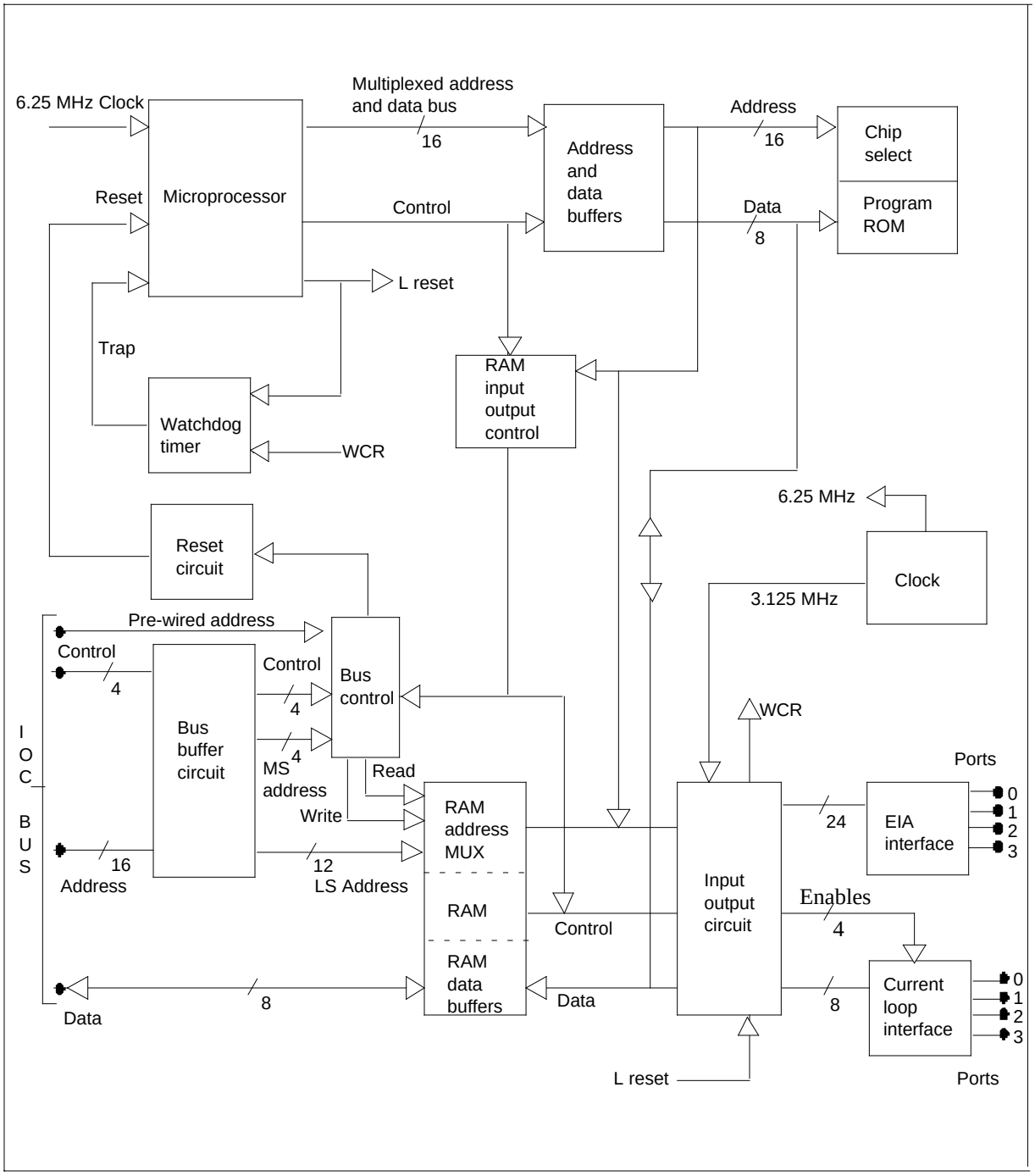
Functional blocks

The NT1X67BD has of the following functional blocks:

- IOC
- microprocessor
- watchdog timer
- random access memory (RAM) input output control
- bus buffer
- bus control
- system RAM
- program read only memory (ROM)
- asynchronous controllers (firmware)
- asynchronous controllers (input output circuit)
- EIA interface
- asynchronous controllers (current loop interface circuit)

The functional relationship between these blocks appears in the following figure.

NT1X67BD functional blocks



NT1X67BD (continued)

Input output controller interface

The IOD bus that communicates with the IOC contains 16 address links, four control links, and eight two way data lines. The functions of the address links are:

- Address bits 12 to 15 select a specified controller or other device on the IOC bus. The signals carried over the lines must match a pre-wired backplane address.
- Address bits 10 and 11 on the controller select a specified peripheral processor associated with a desired port (0 to 3).
- Address bits 0 to 9 select locations in the controller such as outgoing from the CC message buffer and incoming to the CC message buffer, along with the associated control and status registers.

The signals on the four control links control read and write sequences. The eight data links receive and send messages between the IOC and the controller. Messages conform to Digital Multiplex System (DMS) input output message protocol.

Microprocessor

The microprocessor has a multiplexed address and data bus. Firmware instructions located in the program ROM block operate the microprocessor at a rate determine by a crystal-controlled clock. Hardware in the reset circuit or software (if a reset message is decoded) can reset the microprocessor. Firmware in the program ROM performs the reset.

Watchdog timer

The watchdog circuit is a timer that starts each time the microprocessor checks for outgoing messages from the CC. If the microprocessor fails to check for messages for 100 ms, a reset occurs.

RAM input/output control

The RAM input output control circuit provides the read, write, and timing signals for the RAM and input output message cycle. For each new memory or input output cycle started by the microprocessor, the RAM control circuit generates window access (PCYC) to the RAM, followed by window access for bus control to the RAM.

Bus buffer

The bus buffer circuit provides correct buffering and the reversal of IOC address and control signals.

Bus control

The bus control circuit performs the hardware portion of the bus protocol. The bus control circuit matches the four most significant IOC address bus bits with the pre-wired address. If an address match is received, a memory cycle is initiated. When the internal memory cycle is complete by a RAM input output control circuit signal, a bus DUNIT signal is produced. The cycle is completed when the bus read or write is dismissed. An address match and a bus reset can result in an external reset signal being sent to the reset circuit.

System RAM

The system RAM block includes the RAM address multiplexer and the RAM data buffers. The address multiplexer gates the microprocessor address bus to the RAM devices when the control signal from the RAM input output control is high. If the control signal is low, the address multiplexer gates the IOC address bus to the RAM devices. The RAM address multiplexer performs the address translation between the IOC address bus and the local address bus. RAM data buffers act as multiplexers for write data during a RAM write. Separate latches store the read data for the IOC bus and microprocessor enabling the data to remain available until the next respective window.

Program ROM

The program ROM holds firmware instructions that operate the microprocessor.

Asynchronous controllers (firmware)

Four independent peripheral processors each with one IOD port are provided. Each peripheral processor is activated in sequence, under control of the supervision process. With each activation a section of firmware code in the program ROM is processed. The state the peripheral processor is in when activated, determines the code processed. If necessary, after performance of the appropriate actions the state pointer is changed and a different set of firmware instructions are issued the next time the peripheral processor is activated.

States activated by the supervision process are:

- INPUT-obtain a character string from the IOD.
- OUTPUT-output a character string to the IOD.
- ECHO-echo a character to the IOD.
- SEND-wait for an incoming message for the CC to be accepted.

Asynchronous controllers (input/output circuit)

The input output circuit controls the input and output of serial data to the IOD ports. Each port has a universal synchronous/asynchronous

NT1X67BD (continued)

receiver/transmitter (USART) associated with it that performs the serial-to-parallel and parallel-to-serial conversions. The USART also monitors or controls the appropriate interface signals. Each USART has an internal baud rate generator controlled by a common crystal clock.

EIA interface

The EIA interface circuit provides the appropriate level translations and compatibility with the EIA RS-232C specification.

Asynchronous controllers (current loop interface circuit)

The current loop interface circuit provides translation between the current loop port signals and the signals required by the input output circuit. The transmitter is disabled if the current loop circuit is not in use for a specified port. When a port uses the current loop interface, the appropriate EIA signals must be strapped by the current loop cable.

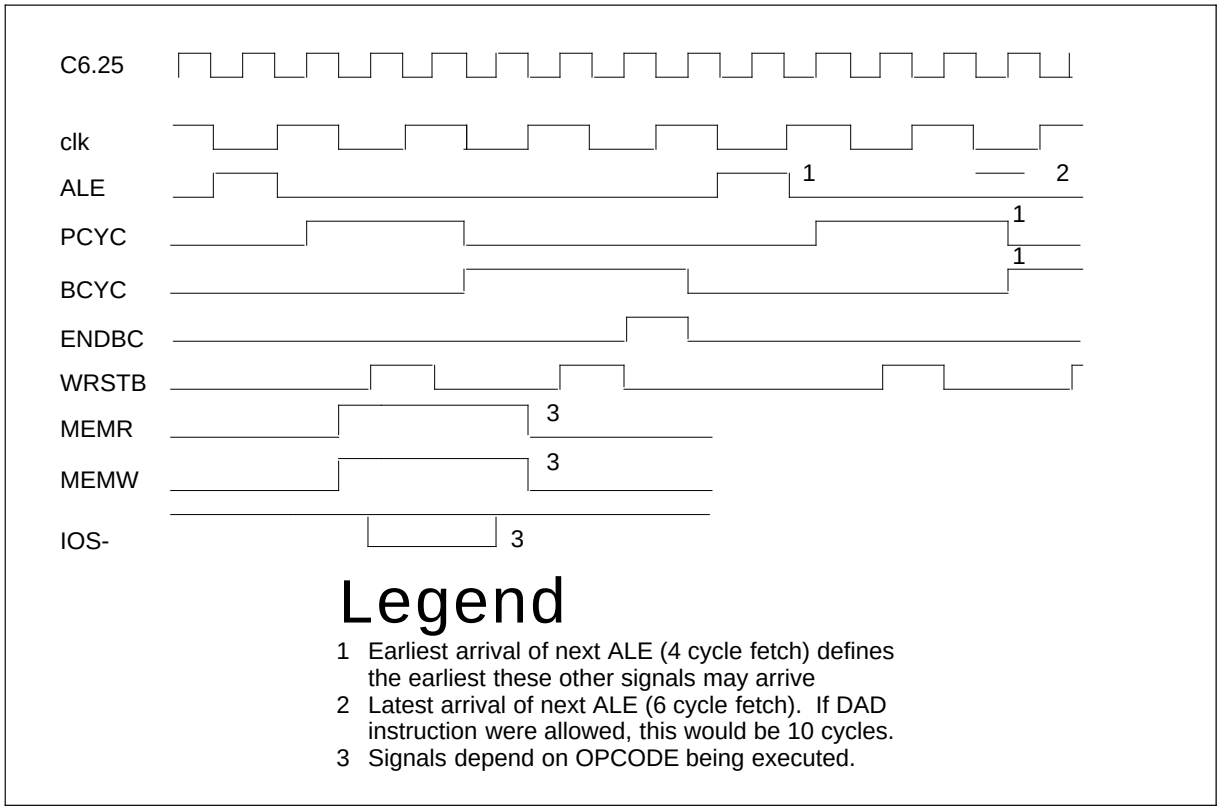
Signaling

This section contains diagrams illustrating control timing for the NT1X67BD circuit card.

Timing

The RAM I/O control timing for the NT1X67BD circuit card appears in the following figure.

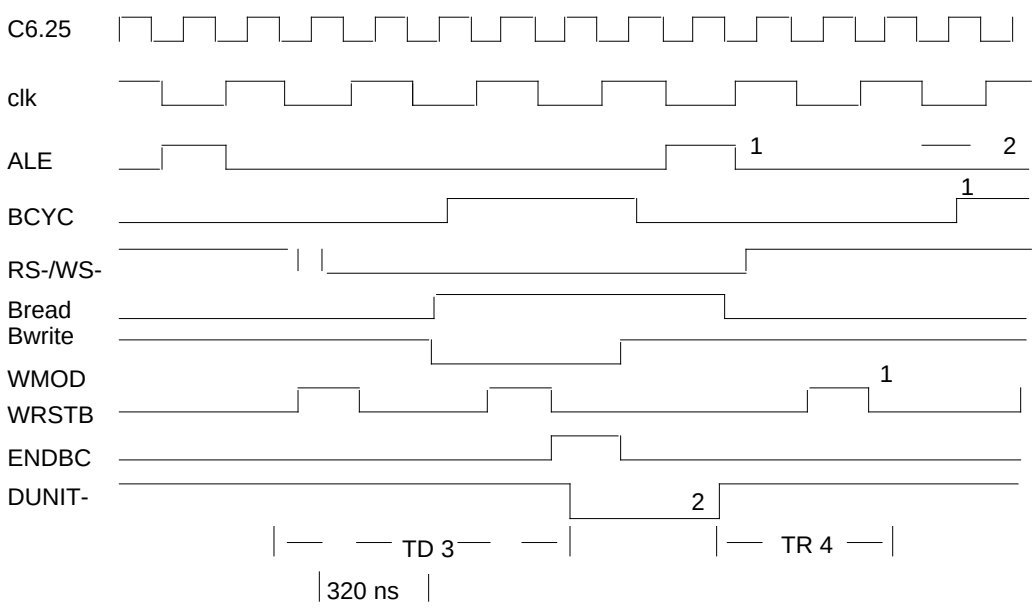
NT1X67BD RAM I/O control timing



The bus control timing for the NT1X67BD circuit card appears in the following figure.

NT1X67BD (continued)

NT1X67BD bus control timing



Legend

1 Earliest arrival of next BCYC
2 IOC response
3 Response time RS fall or WS fall to DUNIT—
374 ns < TD < 2.57 s (includes 10% margin)
4 Response time RS rise or WS rise to DUNIT—
0 < TR < 64 ns (includes 10% margin)

Technical data

This section contains technical data for the NT1X67BD circuit card.

Power requirements

The NT1X67BD requires +5V @ 2.4 A, +12 V @ 25 mA, and –12 V @ 25mA. The NT1X67BD circuit card uses 12.6 W.

IOC bus specifications

The next table contains IOC bus specifications.

IOC bus specifications

Lines	Description
Address lines	16 unidirectional lines with drivers and low power receivers. Terminations of 270 Ω to 5 V and 470 Ω to ground. See note.
Control lines	4 unidirectional lines with open collector line drivers and low power receivers. Terminations of 270 Ω to +5 V and 470 Ω to ground. See note.
Message data lines	8 bidirectional lines with drivers and low power receivers. Terminations of 270 Ω to 5 V and 470 Ω to ground. See note.
Note: External on terminator card.	

Current loop interface

The next table contains current loop interface information.

Current loop interface (Sheet 1 of 2)

Characteristic	Description
Usage	Interface visual display units (VDU) and teleprinter terminals.
Data rate	Up to 1200 baud.
Loop length (controller to terminal)	300 m (984.25 ft).
Mode of operation	4-wire, full duplex with active receiver and transmitter.
Data format	10-bit ASCII code.
Shorts	The maximum current between two loads or between load and ground (referenced to the frame containing the controller) is 60 mA for 10 seconds or less.
Interface signals	Transmit +, transmit -, receive +, receive -.
Transmit circuit	Output current is 18 to 30 mA. Open circuit is 24 V maximum. Loop resistance is 0 to 300 Ω. Terminal receiver drop is 0 to 4 V.

NT1X67BD (end)

Current loop interface (Sheet 2 of 2)

Characteristic	Description
Receive circuit	Output current is 18 to 30 mA. Open circuit is 24 V maximum. Loop resistance is 0 to 300 Ω. Terminal transmitter drop is 0 to 4V.
Circuit enables	EIA circuits CC/CF to CB to CD should be strapped to enable the transmitter and receiver functions when current loop interfacing is used.

NT1X67FA

Product description

The simple message desk interface (SMDI) has the terminal controller (TC). The TC interfaces a maximum of four serial asynchronous input/output devices (IOD) to the central control (CC) through the input/output controller (IOC) and central message controller (CMC).

The TC is based on an 8085 8-bit microprocessor. The TC uses a large-scale integration (LSI) universal synchronous/asynchronous receiver/transmitter (USART) with an internal baud-rate generator. The microprocessor operates in a polling/state environment without interrupts. The microprocessor simulates four separate peripheral processors (PP), one for each serial data port. The TC communicates with the IOC through a shared access buffer for communication and configuration control. Communication with the IODs occurs through an EIA or a current loop interface.

Functional description

The NT1X67FA transmits and receives messages to and from the CC on the IOC parallel bus. The NT1X67FA transmits and receives serial data on four asynchronous data ports. The NT1X67FA performs the following functions:

- performs the required serial-to-parallel translations
- the IOC requires the protocol for communication on the serial ports
- provides a protocol for communication on the serial ports

Standard DMS I/O messages have serial data to or from the IODs. Serial data passes through the IOC.

Functional blocks

The NT1X67FA contains the following functional blocks:

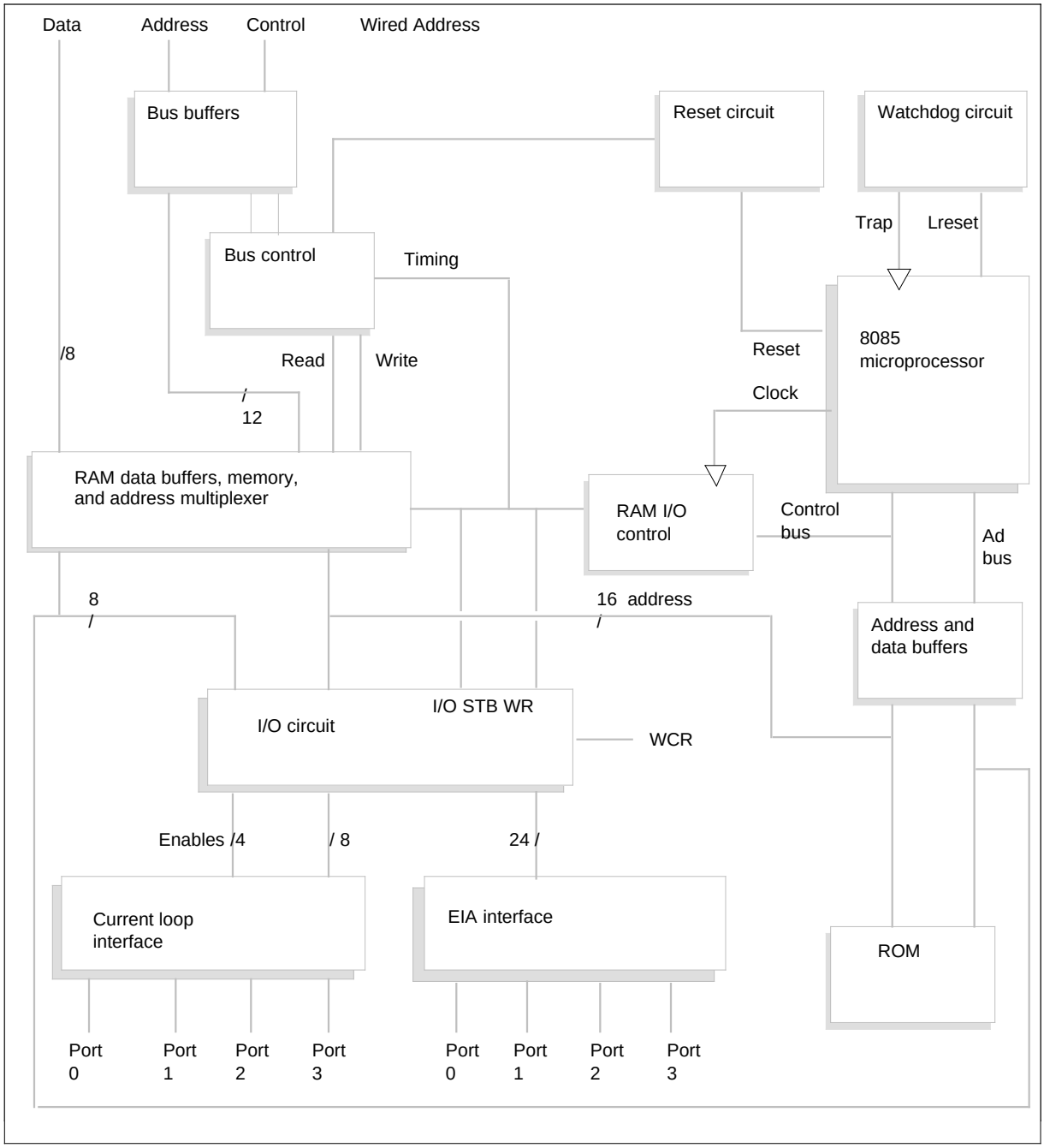
- bus buffers
- reset circuit
- watchdog circuit
- bus control
- 8085 microprocessor
- RAM input/output (I/O) control
- RAM data buffers, memory, and address multiplexer (MUX)
- I/O circuit
- current loop interface

NT1X67FA (continued)

- Electronic Industries Association (EIA) interface
- address and data buffers
- ROM

The functional relationship between these blocks appears in the following table.

NT1X67FA functional blocks



Note: Port 1, 2, and 3 are disabled on. You cannot activate these ports.

NT1X67FA (continued)

Bus buffer
The bus buffer circuit provides appropriate buffering and the inversion of IOC address and control signals.

Reset circuit
The reset circuit hardware can reset the 8085 microprocessor.

Watchdog circuit
The watchdog circuit is timer that starts each time the microprocessor checks for outgoing messages from the CC. If the microprocessor fails to check for messages for 100 ms, a reset occurs.

Bus control
The bus control circuit performs the hardware part of the bus protocol. The circuit matches the four important IOC address bus bits with a prewired address on the back panel. If the circuit detects an address match and receives a bus read or write a memory cycle, the circuit starts a memory cycle. When the internal memory cycle completes, like the RAM I/O control circuit signal ENDBC indicates, the circuit generates a bus DUNIT. The cycle completes and the circuit drops the bus read or write. An address match and a bus reset results in an external reset signaled to the reset circuit.

8085 microprocessor
The 8085 microprocessor has a multiplexed address/data bus that the address and data buffers separate and buffer. The microprocessor operates on firmware instructions in the ROM block at a basic rate that the crystal controlled clock determines. Hardware in the reset circuit (power up or external reset) can reset the microprocessor. The watchdog circuit or software can also reset the microprocessor if the system decodes a reset message.

RAM input/output control
The RAM I/O control circuit provides the read, write and timing signals for the RAM and I/O. For each new memory or I/O cycle the microprocessor starts, the circuit generates window access. The circuit generates window access to the RAM for the microprocessor (during PCYC). The circuit generates a window (BCYC) for the bus control to access the RAM.

RAM data buffers, memory and address multiplexers
The address MUX gates the microprocessor address bus to the RAM devices. This action occurs when the PCYC control from the RAM I/O control is high. When the PCYC control is high, microprocessor window access occurs. If PCYC is not high, the IOC address bus is gated to the RAM devices. The RAM address MUX performs the correct address translation between the IOC address bus and the local address bus.

I/O circuit

The IO circuit controls the input and output of serial data to the IOD ports. Each port contains an associated 2651 USART that performs the serial-to-parallel and parallel-to-serial conversions. The USART monitors or controls the correct EIA interface signals. Each USART has an internal baud rate generator that a common crystal controlled clock controls. The I/O circuit has a register (one bit for each port) to select separate ports for current loop operation instead of EIA. The circuit includes a device address decoder that selects the USARTs, the current loop register. The circuit can also include the watchdog circuit reset (WCR) on a microprocessor I/O operation.

Current loop interface circuit

The current loop interface circuit provides translation between the current loop port signals and the signals the I/O circuit requires. The signal disables the transmitter if the current loop circuit is not used for a specified port. The circuit can use the current loop or EIA interfacing on each port without limits on EIA ports and ports that use a current loop.

Electronic Industries Association interface circuit

The EIA interface circuit provides the appropriate level translations and compatibility with the EIA RS-232C specification.

Address and data buffers

The address and data buffers separate and buffer a multiplexed address/data bus from the microprocessor.

ROM

The read only memory (ROM) holds firmware instructions that operate the microprocessor.

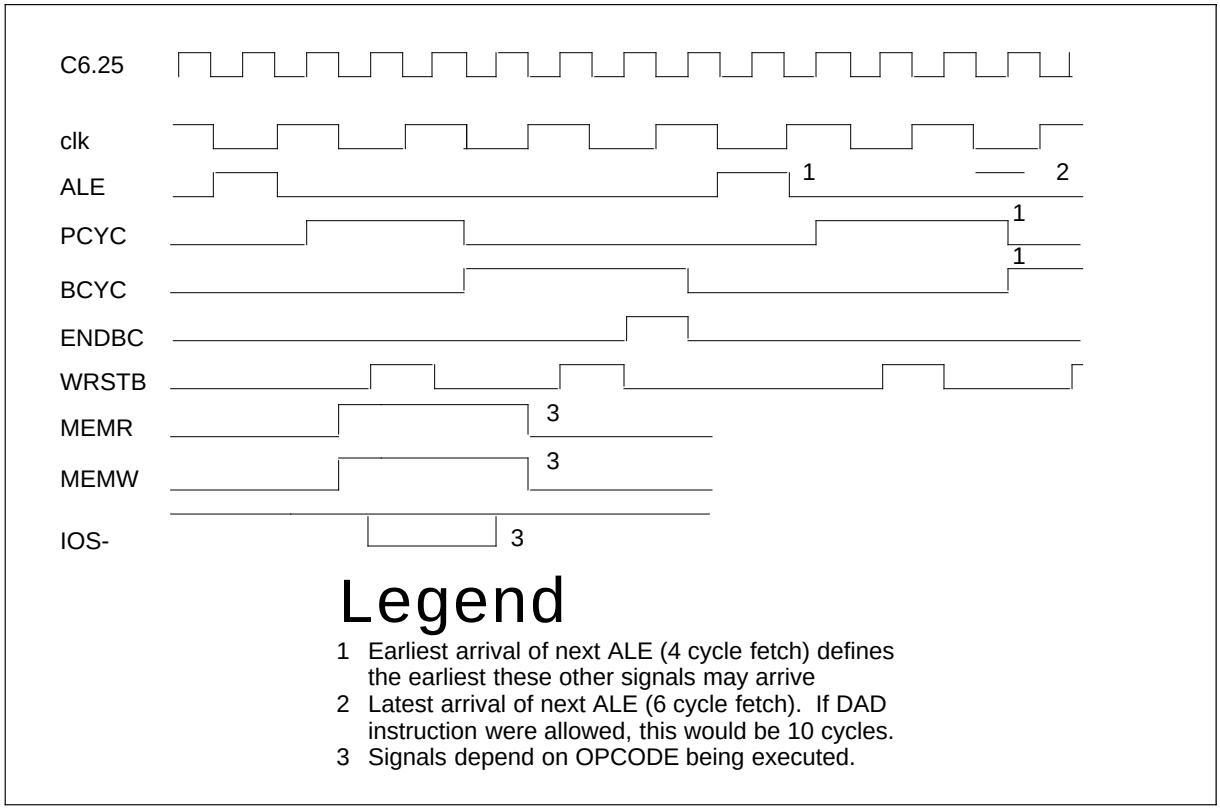
Signaling

Timing

The random access memory (RAM) I/O control timing for the appears in the following figure.

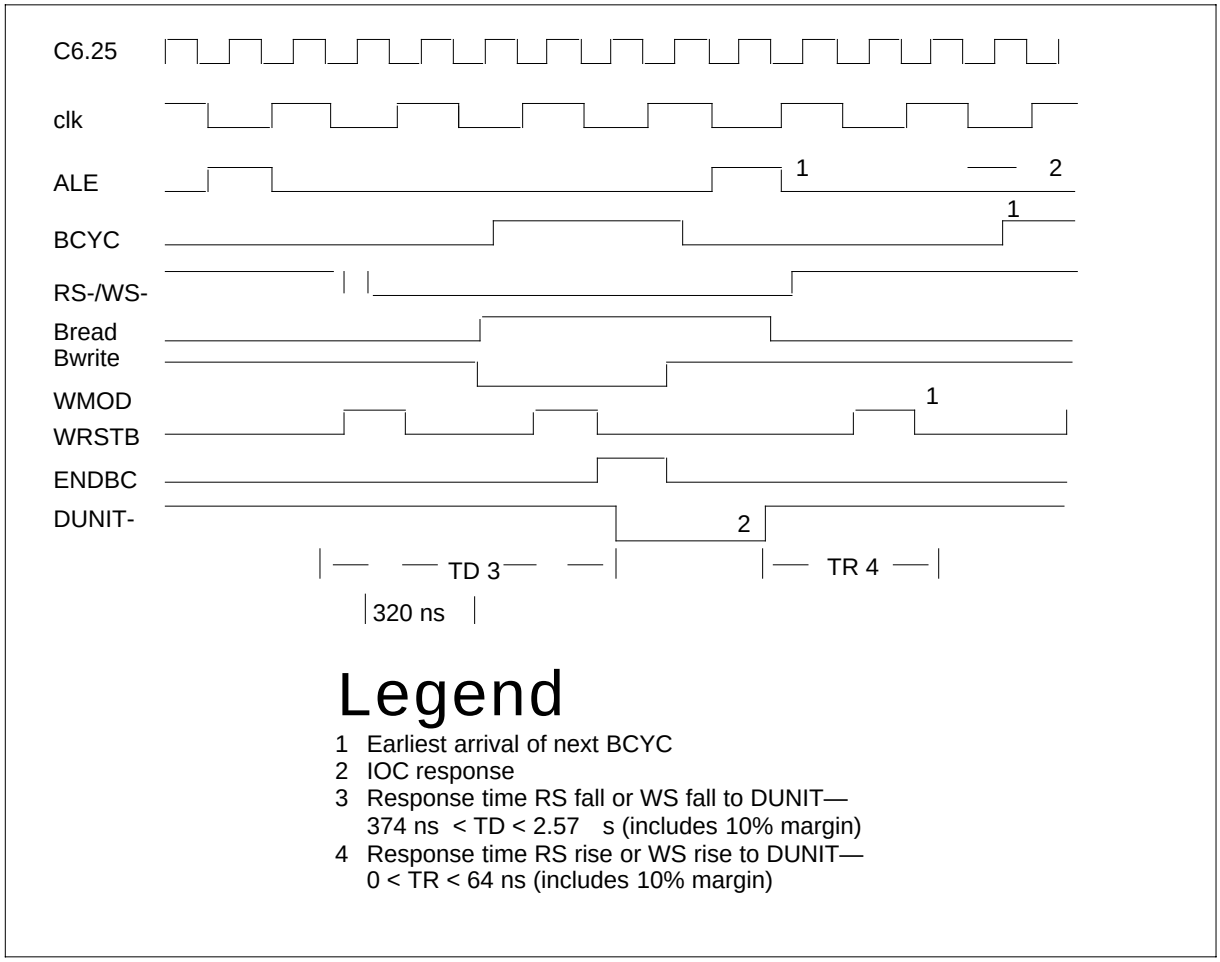
NT1X67FA (continued)

NT1X67FA RAM I/O control timing



The bus control timing for the NT1X67FA appears in the following figure.

NT1X67FA bus control timing



Legend

1 Earliest arrival of next BCYC
2 IOC response
3 Response time RS fall or WS fall to DUNIT—
374 ns < TD < 2.57 s (includes 10% margin)
4 Response time RS rise or WS rise to DUNIT—
0 < TR < 64 ns (includes 10% margin)

Technical data

Power requirements

Each shelf requires 200 W of power, or 20 W for each free-standing data set.

NT1X68AA

Product description

The NT1X68AA magnetic tape interface card provides an interface between an input/output controller (IOC) and an HP7079E 9-track magnetic tape drive. The card receives and sends data and commands from the IOC over the IOC common bus.

Location

The NT1X68AA occupies one card position in the IOC shelf and plugs into the IOC backplane connector.

Functional description

The MTC card connects to the IOC bus with 16 address lines, eight data lines, and four control lines. The card accepts data and address information from the bus. The card uses the microprocessor and memory to send the data or commands to the tape drive. The card accepts data from the tape drive, notifies the IOC of the data. The card also sends the data over the bus to the IOC.

Functional blocks

The NT1X68AA has the following functional blocks:

- address decoder
- read buffer and register
- write buffer and register
- microprocessor
- memory
- flag generator
- interface buffer

Writing data to tape

When the NT1X68AA can accept messages from the IOC, the card sets a ready-to-receive flag. The IOC checks the flag through the IOC bus. The IOC sends the messages on the data lines. The IOC also sends the address of the MTC to which the messages arrive on the address lines. The address from the IOC matches the address of the card strapped on the hardware backpanel. If this information is correct, the MTC can process the message. All other MTCs ignore the message. The messages from the IOC are 256 bytes in length and are sent at a rate of 1 byte every 3.9µs.

When the MTC recognizes an address match, the microprocessor reads the message from the read buffer and decodes the message. If the message is a command message, the microprocessor performs the command immediately.

If the message has data to write to tape, the microprocessor stores the data in the 2048 byte memory.

The microprocessor continues to store the data in the memory until the microprocessor receives a complete tape record. A complete tape record has a maximum of 2048 bytes. When the tape record completes, the MTC encodes the data and writes the data to the tape with the interface buffers.

Recording data from tape

When the IOC requests data on the tape, the CPU sends the MTC a message to transfer a tape record. The tape record transfers from the tape to the memory. When the system loads data to memory, the MTC sets a ready-to-send flag. This flag indicates that the IOC can receive the data. The IOC recognizes the flag and issues a READ signal to the MTC.

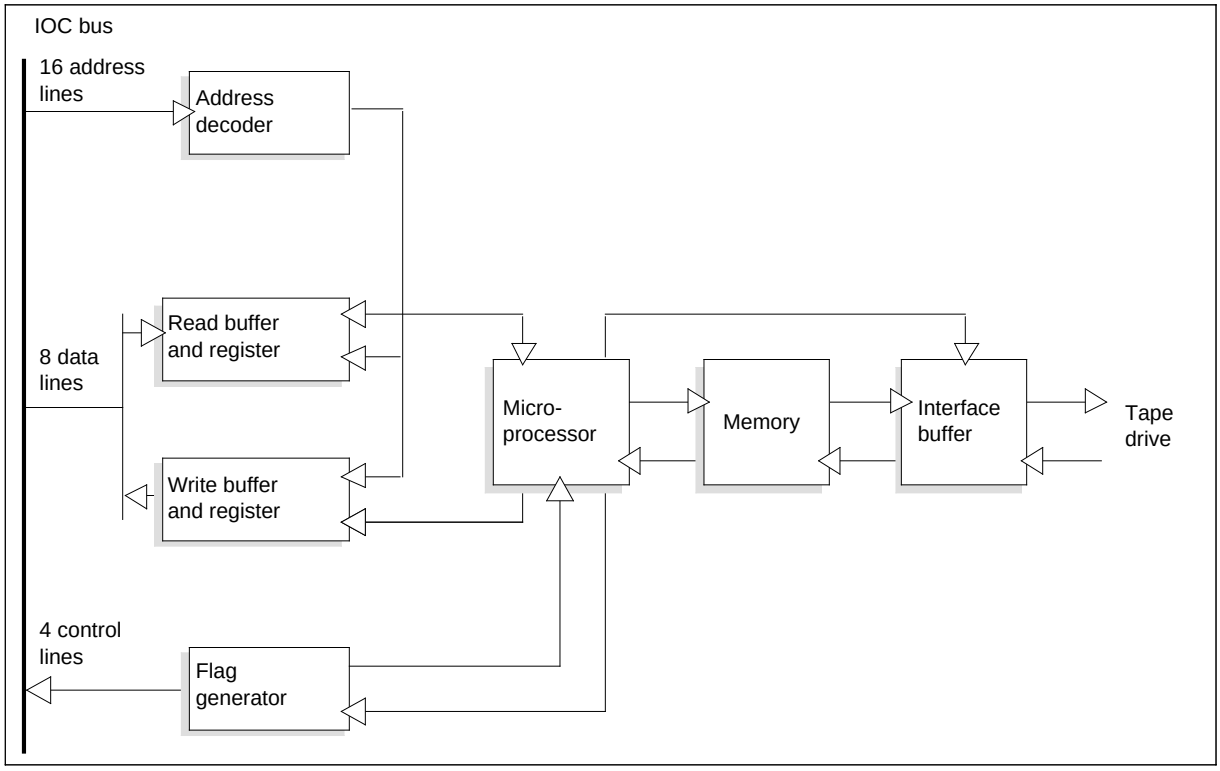
The MTC transfers a byte of the data from the memory to the write register. The MTC sets a DUNIT control signal to indicate that the IOC can read the data. The IOC reads the data and resets the READ signal. When the MTC recognizes that the IOC reset READ signal is reset, the MTC resets the DUNIT signal. The IOC recognizes the DUNIT. The IOC issues another READ signal to start the process again.

After 256 bytes are transferred, the MTC requests the ready-to-send flag. The flag indicates that the MTC can start a new read cycle.

The relationship between the functional blocks appears in the following figure.

NT1X68AA (end)

NT1X68AA functional blocks



Technical data

Ambient conditions

The ambient conditions for the are as follows:

Ambient conditions

	Operating range	Short-term
Ambient temperature	5 °C - 40 C	2 C - 49 °C
Relative humidity	10% - 30%	4% - 50%

Dimensions

The dimensions for the NT1X68AA circuit card appear in the following figure:

- height: 317.5 mm (12.5 in.)
- depth: 254 mm (10 in.)

Power requirements

The requires a voltage of +5 V and current of 3 A.

NT1X68BC

Product description

The Cook 9-Track Tape Controller NT1X68BC provides an interface between an input/output controller (IOC) and an HP7079E 9-track magnetic tape drive. The NT1X68BC circuit card accepts and returns messages to and from the IOC common bus. The NT1X68BC circuit card converts these messages to data transfer and control operations for the tape drive.

Location

The NT1X68BC circuit card is in one card position in the IOC shelf and plugs into the IOC backplane connector.

Functional description

The NT1X68BC circuit card connects to the IOC bus with 16 address lines, eight data lines, and four control lines. The NT1X68BC circuit card accepts data and address information from the IOC common bus. This circuit card uses the microprocessor and memory to send the data or commands to the tape drive. The NT1X68BC circuit card accepts data from the tape drive and notifies the IOC of the data. This circuit card also sends the data over the IOC common bus to the IOC.

Functional blocks

Functional blocks of the NT1X68BC circuit card are:

- address decoder
- read buffer and register
- write buffer and register
- microprocessor
- memory
- flag generator
- interface buffer

Writing data to tape

When the NT1X68BC circuit card accepts messages from the IOC, the circuit card sets a ready-to-receive flag. The IOC checks the flag through the IOC common bus. The IOC sends the messages on the data lines. The IOC also sends the address of the MTC to which the messages arrive on the address lines. The address from the IOC matches the address of the circuit card fastened on the hardware backpanel. If this information is correct, the MTC can process the message. All other MTCs ignore the message. The messages from the IOC are 256 bytes in length and are sent at a rate of 1 byte every 3.9µs.

NT1X68BC (continued)

When the MTC identifies an address match, the microprocessor reads the message from the read buffer and decodes the message. If the message is a command message, the microprocessor performs the command immediately. If the message has data to write to tape, the microprocessor stores the data in the 2048 byte memory.

The microprocessor continues to store the data in the memory until the microprocessor receives a complete tape record. A complete tape record has a maximum of 2048 bytes. When the tape record completes, the MTC encodes the data and writes the data to the tape with the interface buffers.

Recording data from tape

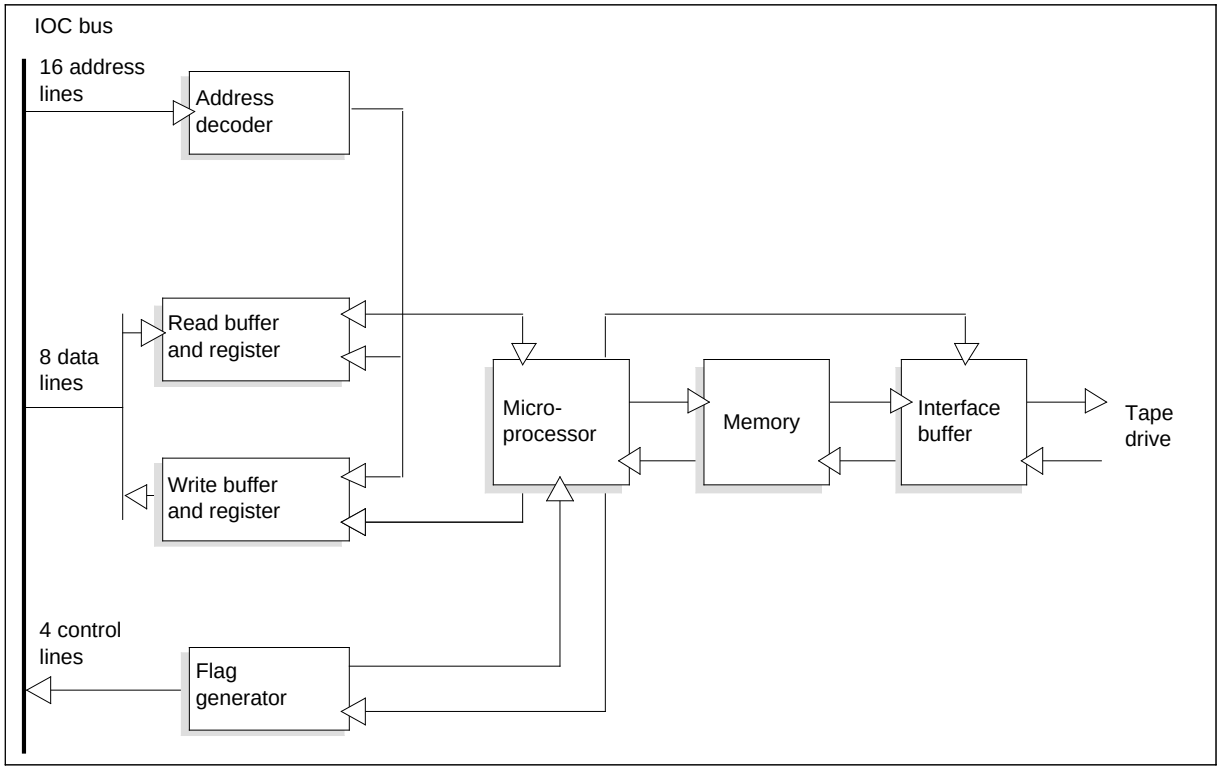
When the IOC requests data on the tape, the central processing unit (CPU) sends the MTC a message to transfer a tape record. The tape record transfers from the tape to the memory. When the system loads data to memory, the MTC sets a ready-to-send flag. This flag indicates the IOC can receive the data. The IOC identifies the flag and issues a READ signal to the MTC.

The MTC transfers a byte of the data from the memory to the write register. The MTC sets a DUNIT control signal to indicate the IOC can read the data. The IOC reads the data and resets the READ signal. When the MTC identifies the IOC reset READ signal is reset, the MTC resets the DUNIT signal. The IOC identifies the DUNIT and issues another READ signal to start the process again.

After 256 bytes are transferred, the MTC requests the ready-to-send flag. The flag indicates the MTC can start a new read cycle.

The relationship between the functional blocks in the NT1X68BC circuit card appear in the next figure.

NT1X68BC functional blocks



Technical data

The next section discusses the technical data for the NT1X68BC circuit card.

Ambient conditions

The ambient conditions for the NT1X68BC circuit card appear in the next table.

Ambient conditions

	Operating range	Short-term
Ambient temperature	5 °C - 40 °C	2 °C - 49 °C
Relative humidity	10% - 30%	4% - 50%

Dimensions

The dimensions for the NT1X68BC circuit card are:

- height: 317.5 mm (12.5 in.)
- depth: 254 mm (10 in.)

NT1X68BC (end)

Power requirements

The NT1X68BC circuit card requires a voltage of +5V and current of 3A.

NT1X75AA

Product description

The NT1X75AA digital recorded announcement (DRA) processor card provides a maximum of 64 recorded announcements or phrases for DMS-100 equipment.

The card operates with the NT1X76 PROM card and the NT1X77 RAM card.

Location

Plug the card in position 5 in an NT2X85AG maintenance trunk module (MTM) shelf.

Functional description

The NT1X75AA selects and retrieves announcements from the NT1X76 and NT1X77 speech memory. The card encodes and decodes the messages for transmission between the speech memory and the central control (CC).

Functional blocks

The NT1X75AA has the following functional blocks:

- enable logic circuit
- microprocessor controller
- encoder/decoder controller
- system RAM
- speech processor
- address latch
- address multiplexer (MUX)
- data latch
- data MUX

Enable logic circuit

The enable logic circuit determines when a channel is an active speech channel. The enable logic circuit signals the system RAM when the MTM sends control data to the microprocessor controller.

Microprocessor controller

The microprocessor controller uses the MTM controller to receive and process control information from the CC. Every 5 ms, the controller checks all 30 pulse code modulation (PCM) speech channels for CC-to-MTM communication.

NT1X75AA (continued)

The microprocessor controller decodes phase IDs from the CC and sends the IDs to the system RAM for storage. The microprocessor controller uses an address bus and a bidirectional data bus to transmit and receive signaling data. The microprocessor controller transmits and receives signaling data to and from the NT1X76 and NT1X77 speech memory.

Encoder/decoder controller

The microprocessor controller controls the encoder/decoder controller. The encoder/decoder controller informs the speech processor which 32 ms speech block the controller uses to record.

System RAM

The system RAM receives phase IDs from the CC and stores the IDs for the microprocessor controller. The RAM receives a signal from the enable logic circuit when the MTM sends control data to the microprocessor controller.

Speech processor

The speech processor reads the NT1X76 and NT1X77 speech memory. The speech processor determines which speech block in the speech memory to play back. In the transmit direction, the speech processor decodes 4-bit adaptive differential pulse code modulation (ADPCM) speech memory to 8-bit PCM data. The speech processor uses a transmit data (XDAT) bus to send the data to the network.

In the receive direction, the speech processor receives 8-bit PCM data from the receive data (RDAT) bus. The speech processor encodes the data to 4-bit ADPCM speech. The processor stores the results in the NT1X76 and NT1X77 speech memory.

Address latch

The address latch receives data from the microprocessor controller and addresses to a maximum of 1 Mbyte (254 s) of speech.

Address MUX

The address MUX receives data from the microprocessor controller and the speech processor. The address MUX determines when the microprocessor controller can access the speech memory. The address MUX has an internal switch. This switch determines if the system uses the NT1X75AA as an 8-circuit, 16-circuit, 24-circuit, or 30-circuit interface.

Data latch

The data latch receives data from the microprocessor controller and sends the data to the NT1X76 and NT1X77 speech memory.

Data MUX

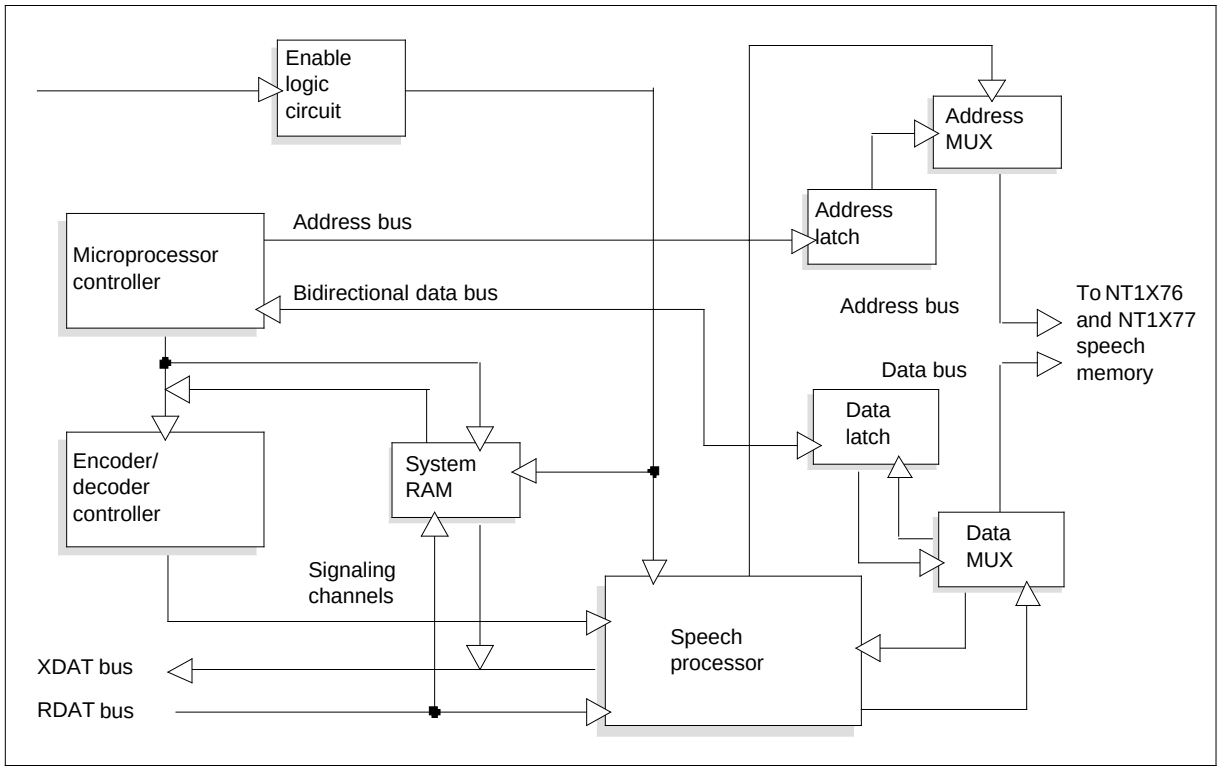
The data MUX uses a bidirectional data bus to receive and send data between the following features:

- microprocessor controller
- speech controller
- NT1X76 and NT1X77 speech memory

The MUX determines when the microprocessor controller can access the speech memory. The MUX has an internal switch. This switch determines if the system uses the NT1X75AA as an 8-circuit, 16-circuit, 24-circuit, or 30-circuit interface.

The relationship between the functional blocks appears in the following figure.

NT1X75AA functional blocks



Technical data

The NT1X75AA has a 4 Hz to 4000 Hz signal requirement with a 0 dB or -6 dB record level. The card has silence termination that corresponds to a zero PCM code. The card also has a phrase termination of 2000 Hz since that code is not present.

NT1X75AA (end)

Dimensions

The dimensions for the NT1X75AA are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 28 mm (1.1 in.)

Power requirements

The NT1X75AA requires a voltage of +5 V and current of 4 A.

Total 48 V power usage is 23 W.

NT1X76AA

Product description

Digital recorded announcement (DRA) hardware consists of a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76AA EEPROM card.

The NT1X76AA is a single density card (128 kbytes). This card represents one virtual card. This card has all 128 kbytes. Seven standard announcements, digits 0 to 9, test tone, prompt tone, and 32 special information tones (SIT) fill the 128 kbytes. The English card represents 32 s of recorded speech. Use key subphrases again to expand this recording to approximately 76 s. The card can be switch selected for any virtual card number from 0 to 7.

Functional description

The NT1X76AA multiplexes addresses because 8-bits are available on the backplane and 20-bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The low address is on the bus by default.

To enable the card, the card select compares A18, A10, and A20 with an attached DIP switch. The A0 is gated to provide for the different addressing mode of the DRA. The DRA requires 4 bits at a given time and the DRA is best to store 8 bits. The controller hardware requires 8 bits and stores the alternate 4 bits for the next cycle. The card-select circuits give access if A0 is 0. The data is gated to the output bus back to the microprocessor during the DS data strobe.

Addresses A12 to A17 (A13 to A 18 for the QM2732D1 version) are decoded for the EPROM chip enables. Each EPROM has two enables that must be pulled low to allow the data on the outputs. Arrange eight row enables and eight column enables to simplify the addressing of the memory array. One of 64 chips receives row and column enables at the same time. One chip supplies data at any time.

NT1X76AA (continued)

Speech memory contents

The phrase IDs and content (silences, phrases, and tones) associated with the NT1X76AA appear in the following table.

NT1X76AA Speech memory contents (Sheet 1 of 2)

Phrase ID Hexadecimal	Phrase ID Decimal	Time (seconds)	Name	Announcement
0	0	1.024	-	1 s of silence
1	1	0.160	-	test tone 760 Hz at -13 dbm
2	2	0.992	-	prompt tone
3 to 7	3 to 7	-	-	reserved phrase
8 to 27	8 to 39	-	SIT1 to SIT32	SIT collection 1 (see note) to SIT collection 32 (see the Special information tone (SIT) table)
28	40	9.248	N-NCA, SOA	We're sorry, all circuits are busy now. Will you please try your call again later? This is a recording. (pause) (location code)
29	41	8.960	P-ROA	We're sorry, your call did not go through. Will you please hang up and try your call again? This is a recording. (pause) (location code)
2A	42	12.032	L-VCA, UCA	We're sorry, your call cannot be completed as dialed. Please check the number and dial again or call your operator to help you. This is a recording. (pause) (location code)
2B	43	12.544	ROH	Please hang up and try your call again. If you need assistance, dial your operator. Please hang up now. This is a recording.
2C	44	6.208	VDN	The number you have reached is not in service. This is a recording.

Note: Phrase names are guidelines. You can change the phrase name as required.

NT1X76AA Speech memory contents (Sheet 2 of 2)

Phrase ID Hexadecimal	Phrase ID Decimal	Time (seconds)	Name	Announcement
2D	45	10.592	M-MCA	The number you have dialed is not a long distance call. Do not dial the digit 1 before the number you are calling. This is a recording.
2E	46	10.016	MCL	You have dialed a number to which long distance charges apply. Please dial the digit 1 before the number you are calling. This is a recording.
2F	47	0.608	digit 0	zero
30	48	0.519	digit 1	one
31	49	0.544	digit 2	two
32	50	0.544	digit 3	three
33	51	0.640	digit 4	four
34	52	0.768	digit 5	five
35	53	0.640	digit 6	six
36	54	0.672	digit 7	seven
37	55	0.544	digit 8	eight
38	56	0.672	digit 9	nine

Note: Phrase names are guidelines. You can change the phrase name as required.

NT1X76AA (continued)

The special information tones, timing and frequencies appear in the following table.

Special Information Tone (SIT) descriptions (Sheet 1 of 2)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
8	8	SIT1	1 short	1 short	1 short
9	9	SIT2	1 short	1 short	1 long
A	10	SIT3	1 short	1 long	1 short
B	11	SIT4	1 short	1 long	1 long
C	12	SIT5	1 short	1 short	1 short
D	13	SIT6	1 short	1 short	1 long
E	14	SIT7	1 short	1 long	1 short
F	15	SIT8	1 short	1 long	1 long
10	16	SIT9	1 long	1 short	1 short
11	17	SIT10	1 long	1 short	1 long
12	18	SIT11	1 long	1 long	1 short
13	19	SIT12	1 long	1 long	1 long
14	20	SIT13	1 long	1 short	1 short
15	21	SIT14	1 long	1 short	1 long
16	22	SIT15	1 long	1 long	1 short
17	23	SIT16	1 long	1 long	1 long
18	24	SIT17	1 short	1 short	1 short
19	25	SIT18	1 short	1 short	1 long

Note: Special information tone components

```
                    First tone Second tone Third tone
Frequencies (Hz)  low   913.8     1370.6      1776.7
                  high  985.2     1428.5      NA
Duration (ms)     short 288
                   long  384
```

Special Information Tone (SIT) descriptions (Sheet 2 of 2)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
1A	26	SIT19	1 short	1 long	1 short
1B	27	SIT20	1 short	1 long	1 long
1C	28	SIT21	1 short	1 short	1 short
1D	29	SIT22	1 short	1 short	1 long
1E	30	SIT23	1 short	1 long	1 short
1F	31	SIT24	1 short	1 long	1 long
20	32	SIT25	1 long	1 short	1 short
21	33	SIT26	1 long	1 short	1 long
22	34	SIT27	1 long	1 long	1 short
23	35	SIT28	1 long	1 long	1 long
24	36	SIT29	1 long	1 short	1 short
25	37	SIT30	1 long	1 short	1 long
26	38	SIT31	1 long	1 long	1 short
27	39	SIT32	1 long	1 long	1 long

Note: Special information tone components

		First tone	Second tone	Third tone
Frequencies (Hz)	low	913.8	1370.6	1776.7
	high	985.2	1428.5	NA
Duration (ms)	short	288		
	long	384		

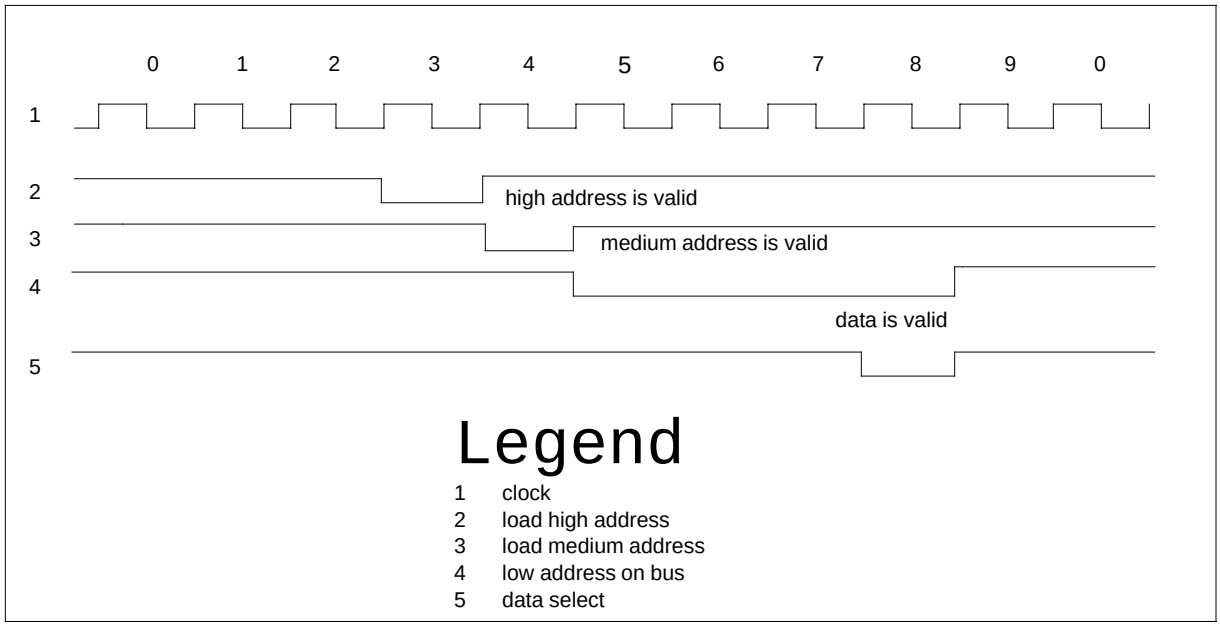
Signaling

Timing

The timing of the NT1X76AA appears in the following figure.

NT1X76AA (end)

NT1X76AA timing



Technical data

Electrical requirements

The voltage required is +5 V. The current required is 2.2 A.

Environmental conditions

The ambient conditions for the NT1X76AA appear in the following table.

NT1X76AA ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30°C	5 to 49°C
Relative humidity	20% to 55%	20% to 80%

NT1X76AB

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76AB EPROM card.

The NT1X76AB is a double density card and has 256 kbytes like two virtual cards. This card occupies one slot in the maintenance trunk module (MTM). This card has a three-position, single-pole, double-throw, dual inline package (DIP) switch. This switch must be set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AB multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The low address is on the bus by default.

To enable the card, the card select compares A18, A10, and A20 with an attached DIP switch. The A0 is gated to provide for the different addressing mode of the DRA. The DRA requires 4 bits at a time, and the DRA is best to store 8 bits. The controller hardware requires 8 bits and stores the alternate 4 bits for the next cycle. The card-select circuits gives access if A0 is 0. The data is gated to the output bus back to the microprocessor during the DS data strobe.

Addresses A12 to A17, or A13 to A 18 for the QM2732D1 version, are decoded for the EPROM chip enables. Each EPROM has two enables. These enables must be pulled low to allow the data on the outputs. Arrange 8 row enables and 8 column enables to simplify the addressing of the memory array. One of 64 chips receives both row and column enables at the same time. One chip supplies data at any one time.

NT1X76AB (continued)

Speech memory contents

The phrase IDs and content associated with the card appear in the following two tables. The content can be silences, phrases and tones. Two virtual cards in the are virtual card 0 and virtual card 1. Refer to the following table.

NT1X76AB Speech memory contents (virtual card 0 and 1) (Sheet 1 of 3)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time[2]	Name[3]	Announcement
0	0	1.024	-	1 s of silence
1	1	0.160	-	test tone 760 Hz at -13 dbm
2	2	0.992	-	prompt tone
3	3	0.512	-	0.5 s of silence
4 to 7	4 to 7	-	-	reserved phrase
8 to 27	8 to 39	-	SIT1 to SIT32	SIT reserved phrase to SIT collection 32 (see the table on page 3)
28	40	7.968 7.872	VCA (virtual card 0) PND (virtual card 1)	(vacant code) We're sorry, your call cannot be completed as dialed. Please check the number and dial again or call your operator to help you. (Prefix not dialed) We're sorry, you must first dial a one or zero when calling this number. Will you please hang up and try your call again?
29	41	7.328	ROH (virtual card 0)	(receiver off hook) If you'd like to make a call, please hang up and try again. If you need help, hang up and then dial your operator.
2A	42	8.608	CCSP (virtual card 0)	(coinless coin sent-paid) We're sorry, your call cannot be completed as dialed from the phone you are using. Please read the instruction card or call your operator to help you.

Note 1: Phrase ID can be in hexadecimal or decimal.

Note 2: Phrase time is in seconds.

Note 3: Phrase names are guidelines. You can change these names as required.

NT1X76AB Speech memory contents (virtual card 0 and 1) (Sheet 2 of 3)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time[2]	Name[3]	Announcement
2B	43	5.760	PDR (virtual card 0)	(partial digits received) We're sorry, your call did not go through. Will you please try your call again?
2C	44	5.984	ATB (virtual card 0)	(all trunks busy) We're sorry, all circuits are busy now. Will you please try your call again later?
2D	45	7.296	P1ND (virtual card 0)	(prefix 1 not dialed) We're sorry, you must first dial a one when calling this number. Will you please hang up and try your call again?
2E	46	8.416	VDCF (virtual card 0)	(voice or data channel failure) We're sorry, due to telephone company facility trouble, your call cannot be completed at this time. Will you try your call again later?
2F	47	0.608	digit 0 (virtual card 1)	zero
30	48	7.776 0.608	P1D (virtual card 0) digit 1 (virtual card 1)	(prefix 1 dialed) We're sorry, it is not necessary to dial a one when calling this number. Will you please hang up and try your call again? one
31	49	0.544	digit 2 (virtual card 1)	two
32	50	0.544	digit 3 (virtual card 1)	three
33	51	0.640	digit 4 (virtual card 1)	four
34	52	0.768	digit 5 (virtual card 1)	five

Note 1: Phrase ID can be in hexadecimal or decimal.

Note 2: Phrase time is in seconds.

Note 3: Phrase names are guidelines. You can change these names as required.

NT1X76AB (continued)

NT1X76AB Speech memory contents (virtual card 0 and 1) (Sheet 3 of 3)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time[2]	Name[3]	Announcement
35	53	0.640	digit 6 (virtual card 1)	six
36	54	0.672	digit 7 (virtual card 1)	seven
37	55	0.544	digit 8 (virtual card 1)	eight
38	56	0.672	digit 9 (virtual card 1)	nine

Note 1: Phrase ID can be in hexadecimal or decimal.

Note 2: Phrase time is in seconds.

Note 3: Phrase names are guidelines. You can change these names as required.

The following table defines the special information tones, timing and frequencies.

Special Information Tone (SIT) definitions (Sheet 1 of 3)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
8	8	SIT1	1 short	1 short	1 short
9	9	SIT2	1 short	1 short	1 long
A	10	SIT3	1 short	1 long	1 short
B	11	SIT4	1 short	1 long	1 long
C	12	SIT5	1 short	1 short	1 short
D	13	SIT6	1 short	1 short	1 long

Note: Special information tone components

```
                     First tone Second tone Third tone
Frequencies (Hz) low   913.8     1370.6      1776.7
                 high  985.2     1428.5      NA
Duration (ms)    short 288
                  long  384
```

Special Information Tone (SIT) definitions (Sheet 2 of 3)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
E	14	SIT7	1 short	1 long	1 short
F	15	SIT8	1 short	1 long	1 long
10	16	SIT9	1 long	1 short	1 short
11	17	SIT10	1 long	1 short	1 long
12	18	SIT11	1 long	1 long	1 short
13	19	SIT12	1 long	1 long	1 long
14	20	SIT13	1 long	1 short	1 short
15	21	SIT14	1 long	1 short	1 long
16	22	SIT15	1 long	1 long	1 short
17	23	SIT16	1 long	1 long	1 long
18	24	SIT17	1 short	1 short	1 short
19	25	SIT18	1 short	1 short	1 long
1A	26	SIT19	1 short	1 long	1 short
1B	27	SIT20	1 short	1 long	1 long
1C	28	SIT21	1 short	1 short	1 short
1D	29	SIT22	1 short	1 short	1 long
1E	30	SIT23	1 short	1 long	1 short
1F	31	SIT24	1 short	1 long	1 long
20	32	SIT25	1 long	1 short	1 short

Note: Special information tone components

```
                    First tone Second tone Third tone
Frequencies (Hz) low   913.8     1370.6      1776.7
                 high  985.2     1428.5      NA
Duration (ms)    short 288
                  long  384
```

NT1X76AB (continued)

Special Information Tone (SIT) definitions (Sheet 3 of 3)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
21	33	SIT26	1 long	1 short	1 long
22	34	SIT27	1 long	1 long	1 short
23	35	SIT28	1 long	1 long	1 long
24	36	SIT29	1 long	1 short	1 short
25	37	SIT30	1 long	1 short	1 long
26	38	SIT31	1 long	1 long	1 short
27	39	SIT32	1 long	1 long	1 long

Note: Special information tone components

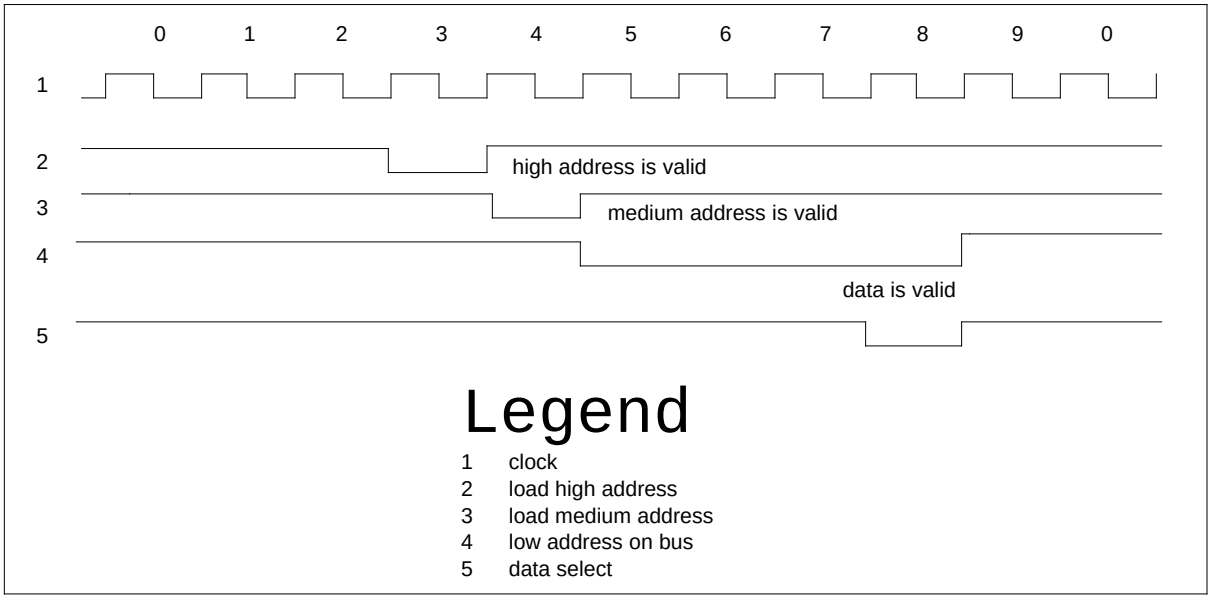
```
                    First tone Second tone Third tone
Frequencies (Hz) low   913.8     1370.6      1776.7
                 high  985.2     1428.5      NA
Duration (ms)    short 288
                  long  384
```

Signaling

Timing

The timing of the NT1X76AB appears in the following figure.

NT1X76AB timing



Technical data

Electrical requirements

The voltage required is +5 V. The current required is 2.2 A.

Environmental conditions

The ambient conditions for the NT1X76AB appear in the following figure.

NT1X76AB ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AE

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76AE EPROM card.

The NT1X76AE is a double density card that has 256 kbytes like two virtual cards. This card occupies one slot in the maintenance trunk module (MTM). This card has a three-position single-pole double-throw dual inline package (DIP) switch. This switch must be set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AE multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The low address is on the bus by default.

To enable the card, the card select compares A18, A10, and A20 with an onboard DIP switch. The A0 is gated to provide for the different addressing mode of the DRA. The DRA requires 4 bits at a time, but the DRA is best to store 8 bits. The controller hardware requires 8 bits and stores the alternate 4 bits for the next cycle. The card-select circuits give access if A0 is 0. The data is gated to the output bus back to the microprocessor during the DS data strobe.

Addresses A12 to A17, or A13 to A 18 for the QM2732D1 version, are decoded for the EPROM chip enables. Each EPROM has two enables that must be pulled low to allow the data on the outputs. Arrange 8 row enables and 8 column enables to simplify the addressing of the memory array. One of 64 chips receives row and column enables at the same time. One chip supplies data at any one time.

Speech memory contents

The phrase IDs and content associated with NT1X76AE the card are presented in the following two tables. The contents can be silences, phrases and tones.

The NT1X76AE has two virtual cards. These cards are referred to as virtual card 0 and virtual card 1.

NT1X76AE Speech memory contents (virtual card 0) (Sheet 1 of 3)

Phase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
0	0	1.024	-	1 s of silence
1	1	0.160	-	test tone 760 Hz at -13dbm
2	2	0.992	-	prompt tone
3	3	0.512	-	0.5 s of silence
4	4	0.256	-	0.25 s of silence
5	5	0.512		ACTS alert tone
6	6	-	-	reserved
7	7	-	-	reserved
8	8	0.576	plsbos	Please (beginning of sentence)
9	9	0.416	min	minute
A	10	0.640	mins	minutes
B	11	0.704	plseos	Please (end of sentence)
C	12	1.184	plsdep	Please deposit
D	13	5.792	dep	Deposit. Please hang up momentarily, listen for dial tone, deposit
E	14	1.024	osos	one s of silence
F	15	1.024	osos	one s of silence
10	16	0.512	10	ten
11	17	0.672	11	eleven
12	18	0.640	12	twelve
13	19	0.864	13	thirteen

Note 1: Phrase ID can be in hexadecimal or decimal.

Note 2: Phrase names are guidelines. You can change the phrase name as required.

NT1X76AE (continued)

NT1X76AE Speech memory contents (virtual card 0) (Sheet 2 of 3)

Phase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
14	20	0.928	14	fourteen
15	21	0.736	15	fifteen
16	22	0.768	16	sixteen
17	23	0.960	17	seventeen
18	24	0.800	18	eighteen
19	25	0.928	19	nineteen
1A to 1F	26 to 31	1.024	osos	1 s of silence
20	32	0.512	20	twenty
21	33	0.608	30	thirty
22	34	0.640	40	forty
23	35	0.480	50	fifty
24	36	0.640	60	sixty
25	37	0.512	70	seventy
26	38	0.416	80	eighty
27	39	0.576	90	ninety
28	40	0.608	100	hundred
29	41	0.704	1000	thousand
2A	42	0.544	dol	dollar
2B	43	0.672	dols	dollars
2C	44	0.480	cent	cent
2D	45	0.640	cents	cents
2E	46	0.448	and	and

Note 1: Phrase ID can be in hexadecimal or decimal.

Note 2: Phrase names are guidelines. You can change the phrase name as required.

NT1X76AE Speech memory contents (virtual card 0) (Sheet 3 of 3)

Phase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
2F	47	0.512	more	more
30	48	0.640	digit 0	zero
31	49	0.512	digit 1	one
32	50	0.480	digit 2	two
33	51	0.672	digit 3	three
34	52	0.672	digit 4	four
35	53	0.672	digit 5	five
36	54	0.608	digit 6	six
37	55	0.672	digit 7	seven
38	56	0.544	digit 8	eight
39	57	0.576	digit 9	nine
3A	58	0.256	qsos	0.25 s of silence
3B	59	0.512	hsos	0.5 s of silence
3C	60	0.992	prompt	prompt tone (includes 0.5 s of silence)
3D	61	0.160	tst	test tone
3E	62	1.024	osos	1 s of silence
3F	63	0.512	alton	ACTS alerting tone

Note 1: Phrase ID can be in hexadecimal or decimal.

Note 2: Phrase names are guidelines. You can change the phrase name as required.

NT1X76AE (continued)

NT1X76AE Speech memory contents (virtual card 1) (Sheet 1 of 2)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
0	0	1.024	-	1 s of silence
1	1	0.160	-	test tone 760 Hz at -13dbm
2	2	0.992	-	prompt tone
3	3	0.512	-	0.5 s of silence
4	4	0.256	-	0.25 s of silence
5 to 7	5 to 7	-		reserved
8	8	0.576	pls	Please
9	9	0.280	plsdep	Please deposit
A	10	0.672	ftf	for the first
B	11	1.568	tnkuuh	Thank you. You have
C	12	2.144	crtoov	credit toward overtime
D	13	0.736	tnku	Thank you
E	14	3.072	plsig	has ended. Please signal when through
F	15	0.896	ftp	for the past
10	16	1.120	chgsr	the charges are
11	17	1.824	plustx	plus tax for
12	18	0.832	end	has ended.
13	19	2.784	ctstdn	Coin test. Please deposit nickel
14	20	2.816	ctstdn	Coin test. Please deposit dime
15	21	2.848	ctstdd	Coin test. Please deposit quarter
16	22	0.544	nkl	nickel
17	23	0.576	dime	dime

Note 1: Phrase ID can be in hexadecimal or decimal.

Note 2: Phrase name are guidelines. You can change the phrase name as required.

NT1X76AE Speech memory contents (virtual card 1) (Sheet 2 of 2)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
18	24	0.608	qrtr	quarter
19	25	1.408	tstend	test has ended
1A	26	0.864	ftn	for the next
1B	27	2.496	cldisc	or your call will be disconnected
1C	28	3.072	clreq	the call you made requires a
1D	29	1.024	osos	1 s of silence
1E	30	3.968	dlagn	and dial your call again. This is a recording.
1F	31	0.768	sec	second
20	32	0.800	secs	seconds
21	33	0.800	plseos	please (end of sentence)
22	34	0.704	dep	deposit (noun)
23	35	0.832	uhave	you have
24	36	0.512	cr	credit
25 to 39	37 to 57	1.024	osos	1 s of silence
3A	58	0.256	qsos	0.25 s of silence
3B	59	0.512	hsos	0.5 s of silence
3C	60	0.992	prompt	prompt tone
3D	61	0.160	tstton	test tone
3E	62	1.024	osos	1 s of silence
3F	63	1.024	osos	1 s of silence

Note 1: Phrase ID can be in hexadecimal or decimal.

Note 2: Phrase name are guidelines. You can change the phrase name as required.

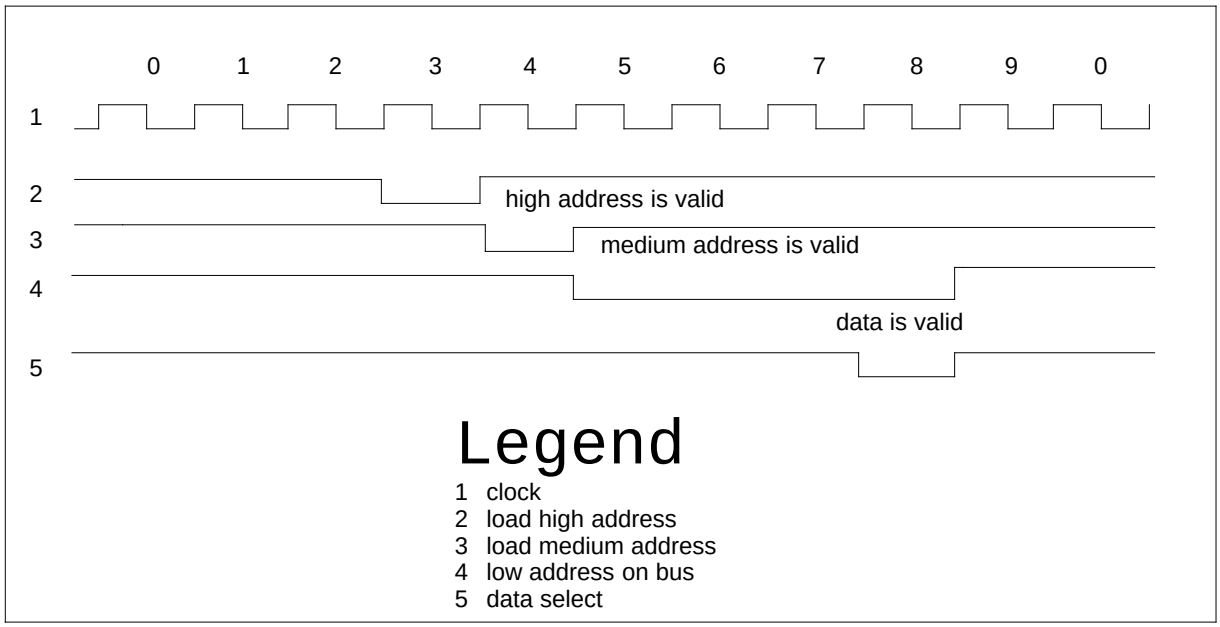
NT1X76AE (end)

Signaling

Timing

The following figure indicates the timing of the NT1X76AE.

NT1X76AE timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 2.2A.

Environmental conditions

The ambient conditions for the NT1X76AE appear in the following table.

NT1X76AE ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30°C	5 to 49°C
Relative humidity	20% to 55%	20% to 80%

NT1X76AF

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the digital recorded announcement PROM auxiliary operator service system card 1.

The NT1X76AF is a double density card (256 Kbytes-two virtual cards). The NT1X76AF occupies one slot in the maintenance trunk module (MTM). The NT1X76AF has a three-position, single-pole, double-throw, dual-inline package (DIP) switch. This switch must be set to the number assigned on the card. This number is the BLOCKLIST value you enter in field CARDINFO of Table DRAMS in the digital switching system.

Functional description

The NT1X76AF multiplexes addresses because 8 bits are available on the backplane and requires 20 bits to address the DRA. The system latches the high address in the high address latch. The system latches the medium address in the medium address latch. The low address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. The EPROM supplies a card enable signal. The signal enables the data buffer and the row decoder. This event occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. The column addresses enable the outputs of the memory devices. The row addresses are chip enables. The data strobe that the processor sends enables the data.

Speech memory contents

The following two tables present the phrase IDs and content (silences, phrases, and tones). The phrase IDs and content associate with the NT1X76AF digital recorded announcement PROM auxiliary operator service system, voice

NT1X76AF (continued)

response card 1. The two virtual cards in the NT1X76AF are virtual card 0 and virtual card 1.

NT1X76AF Speech memory contents for virtual card 0 (Sheet 1 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s silence
1	1	0.160		test tone 750 Hz at -13 dbm
2	2	0.992		prompt tone
3	3	0.512		0.5 s of silence
4	4	1.536	AVRE02	Has been changed to
5	5	4.960	AVRE03	Has been changed to a nonpublished number. It is not listed in our records.
6	6	5.696	AVRE04	Has been changed. You can call toll free: one, eight-hundred,
7	7	1.184	AVRE05	Has been disconnected.
8	8	3.712	AVRE06	Has been disconnected. The customer can be reached at
9	9	5.888	AVRE07	Has been disconnected. You can call toll free: one, eight-hundred,
A	10	3.072	AVRE10	Has moved. Service has been disconnected.
B	11	5.152	AVRE17	At the customer's request, service has been temporarily disconnected.
C	12	7.776	AVRE18	At the customer's request, service has been temporarily disconnected. The customer can be reached at
D	13	6.240	AVRE19	At the customer's request, the number is nonpublished. It is not listed in our records.

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly as the names appear.

NT1X76AF Speech memory contents for virtual card 0 (Sheet 2 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
E	14	3.168	AVRE20	At the customer's request, the service at
F	15	3.584	AVRE23	Due to fire, service has been disconnected.
10	16	6.208	AVRE24	Due to fire, service has been disconnected. The customer can be reached at
11	17	2.496	AVRE25	Due to fire, the service at
12	18	2.784	AVRE26	I repeat.
13	19	3.744	AVRE27	I repeat, the number is:
14	20	4.480	AVRE28	I repeat, the number is: one,
15	21	6.016	AVRE29	I repeat, the toll-free number is: one, eight-hundred
16	22	2.144	AVRE36	Service has been disconnected.
17	23	4.896	AVRE37	Service has been disconnected. The customer can be reached at
18	24	6.944	AVRE38	Service is disconnected. You can now call toll free: one, eight-hundred
19	25	4.224	AVRE42	The customer moved. Service has been disconnected.
1A	26	6.848	AVRE50	The number has changed. You can now call toll free: one, eight-hundred,
1B	27	1.536	AVRE51	The number is:
1C	28	2.400	AVRE52	The number is: one,

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly as the names appear.

NT1X76AF (continued)

NT1X76AF Speech memory contents for virtual card 0 (Sheet 3 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
1D	29	3.936	AVRE55	The toll-free number is: one, eight-hundred,
1E	30	0.864	AVRE59	One
1F	31	1.152	AVRE60	Eight-hundred
20	32	2.016	AVRE61	One, eight-hundred

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly as the names appear.

NT1X76AF Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s silence
1	1	0.160		test tone 750 Hz at -13 dbm
2	2	0.992		prompt tone
3	3	0.512		0.5 s silence
4	4	1.824	AVRE08	Has been temporarily disconnected.
5	5	4.320	AVRE09	Has been temporarily disconnected. The customer can be reached at
6	6	3.872	AVRE12	Is being checked for trouble. Please try your call again later.
7	7	3.456	AVRE13	Is moving. The new service is not yet connected.
8	8	1.760	AVRE15	Is temporarily out of order.

Note 1: Phrase ID can be in hexadecimal or decimal when use of the ASSIGN command in DRAMREC occurs. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly at the names appear.

NT1X76AF Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
9	9	4.288	AVRE16	Is temporarily out of order. Calls are being taken at
A	10	5.920	AVRE31	If you need assistance, please stay on the line. An operator will return.
B	11	5.952	AVRE32	If you need assistance, please stay on the line. An operator will return.
C	12	2.368	AVRE34	It is no longer a free call.
D	13	4.224	AVRE35	It is no longer a free call. You may call collect.
E	14	1.216	AVRE41	The customer at
F	15	4.800	AVRE43	The customer is moving. The new service in not yet connected.
10	16	4.864	AVRE45	The line is being checked for trouble. Please try your call again later.
11	17	2.784	AVRE46	The line is temporarily out of order.
12	18	5.312	AVRE47	The line is temporarily out of order. Calls are being taken at
13	19	3.712	AVRE62	Should be in service. Please try your call again

Note 1: Phrase ID can be in hexadecimal or decimal when use of the ASSIGN command in DRAMREC occurs. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly at the names appear.

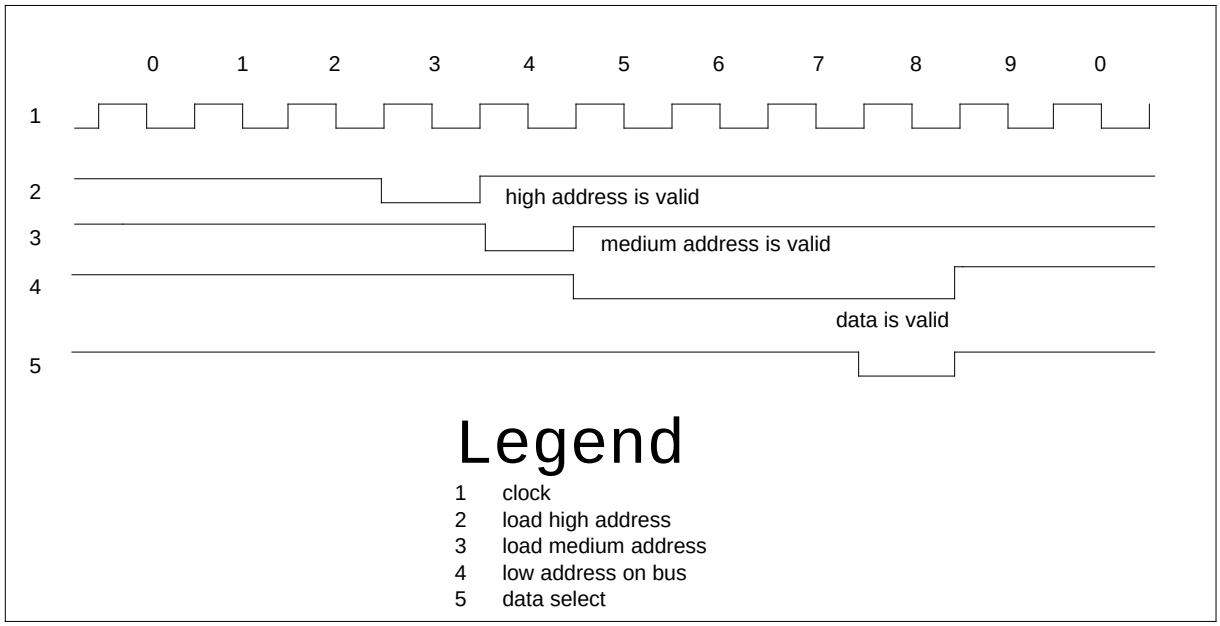
Signaling

Timing

The timing of the NT1X76AF appears in the following figure.

NT1X76AF (end)

NT1X76AF timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76AF appear in the following table.

NT1X76AF ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AG

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76AG auxiliary operator service system, voice response English card 2.

The NT1X76AG is a double density card (256 Kbytes-two virtual cards). The NT1X76AG occupies one slot in the maintenance trunk module (MTM). The NT1X76 has a three-position, single-pole, double-throw, dual inline package (DIP) switch. This switch must be set to the number assigned on the card. This number is the BLOCKLIST value you enter in field CARDINFO of Table DRAMS in the digital switching system.

Functional description

The NT1X76AG multiplexes addresses because 8 bits are available on the backplane and requires 20 bits to address the DRA. The system latches the high address in the high address latch. The system latches the medium address in the medium address latch. The low address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables and write enables. The EPROM supplies a card enable signal. The signal enables the data buffer and the row decoder. This event occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. The column addresses enable the outputs of the memory devices. The row addresses act as chip enables. The processor sends a data strobe. The data strobe also enables the data.

NT1X76AG (continued)

Speech memory contents

The phrase IDs and content (silences, phrases, and tones) that associate with the NT1X76AG card appear in the following two tables. The NT1X76AG contains virtual card 0 and virtual card 1.

NT1X76AG Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
1	1	0.160		test tone 760 Hz at -13 dbm
2	2	0.992		prompt tone
3	3	0.512		0.5 s of silence
4	4	2.272	AVRE01	are being temporarily taken at
5	5	2.592	AVRE11	is equipped for outgoing service only
6	6	1.440	AVRE14	is not yet connected
7	7	3.232	AVRE21	calls are being temporarily taken at
8	8	1.440	AVRE22	calls for
9	9	1.280	AVRE30	I'm sorry
A	10	5.184	AVRE33	It has been changed to a nonpublished number and is not listed in our records.
B	11	3.072	AVRE39	Service has been temporarily disconnected.
C	12	3.328	AVRE40	That line is equipped for outgoing service only.
D	13	1.216	AVRE44	the line at
E	14	0.928	AVRE48	the number
F	15	2.592	AVRE49	the number has been changed to
10	16	1.312	AVRE53	the service at

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly as they appear.

NT1X76AG Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
11	17	2.688	AVRE54	The service is not yet connected.
12	18	1.792	AVRE56	there is no service at
13	19	2.624	AVRE57	There is no service at this number.
14	20	1.312	AVRE58	you have reached

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly as they appear.

NT1X76AG Speech memory contents for virtual card 1 (Sheet 1 of 4)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s of silence
1	1	0.160		test tone 760 Hz at -13 dbm
2	2	0.992		prompt tone
3	3	0.512		0.5 s of silence
4	4	1	EHIRI0	zero (high rising intonation)
5	5	1	EHIRI1	one
6	6	1	EHIRI2	two
7	7	1	EHIRI3	three
8	8	1	EHIRI4	four
9	9	1	EHIRI5	five
A	10	1	EHIRI6	six

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly as they appear.

NT1X76AG (continued)

NT1X76AG Speech memory contents for virtual card 1 (Sheet 2 of 4)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
B	11	1	EHIRI7	seven
C	12	1	EHIRI8	eight
D	13	1	EHIRI9	nine
E	14	1	ELORI0	zero (low rising intonation)
F	15	1	ELORI1	one
10	16	1	ELORI2	two
11	17	1	ELORI3	three
12	18	1	ELORI4	four
13	19	1	ELORI5	five
14	20	1	ELORI6	six
15	21	1	ELORI7	seven
16	22	1	ELORI8	eight
17	23	1	ELORI9	nine
18	24	1	EWAVE0	zero (falling, rising intonation)
19	25	1	EWAVE1	one
1A	26	1	EWAVE2	two
1B	27	1	EWAVE3	three
1C	28	1	EWAVE4	four
1D	29	1	EWAVE5	five
1E	30	1	EWAVE6	six
1F	31	1	EWAVE7	seven

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly as they appear.

NT1X76AG Speech memory contents for virtual card 1 (Sheet 3 of 4)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
20	32	1	EWAVE8	eight
21	33	1	EWAVE9	nine
22	34	1	EFALL0	zero (falling intonation)
23	35	1	EFALL1	one
24	36	1	EFALL2	two
25	37	1	EFALL3	three
26	38	1	EFALL4	four
27	39	1	EFALL5	five
28	40	1	EFALL6	six
29	41	1	EFALL7	seven
2A	42	1	EFALL8	eight
2B	43	1	EFALL9	nine
2C	44	1	EFLTA0	zero (flat A intonation)
2D	45	1	EFLTA1	one
2E	46	1	EFLTA2	two
2F	47	1	EFLTA3	three
30	48	1	EFLTA4	four
31	49	1	EFLTA5	five
32	50	1	EFLTA6	six
33	51	1	EFLTA7	seven
34	52	1	EFLTA8	eight

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names exactly as they appear.

NT1X76AG (continued)

NT1X76AG Speech memory contents for virtual card 1 (Sheet 4 of 4)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
35	53	1	EFLTA9	nine
36	54	1	EFLTB0	zero (flat B intonation)
37	55	1	EFLTB1	one
38	56	1	EFLTB2	two
39	57	1	EFLTB3	three
3A	58	1	EFLTB4	four
3B	59	1	EFLTB5	five
3C	60	1	EFLTB6	six
3D	61	1	EFLTB7	seven
3E	62	1	EFLTB8	eight
3F	63	1	EFLTB9	nine

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

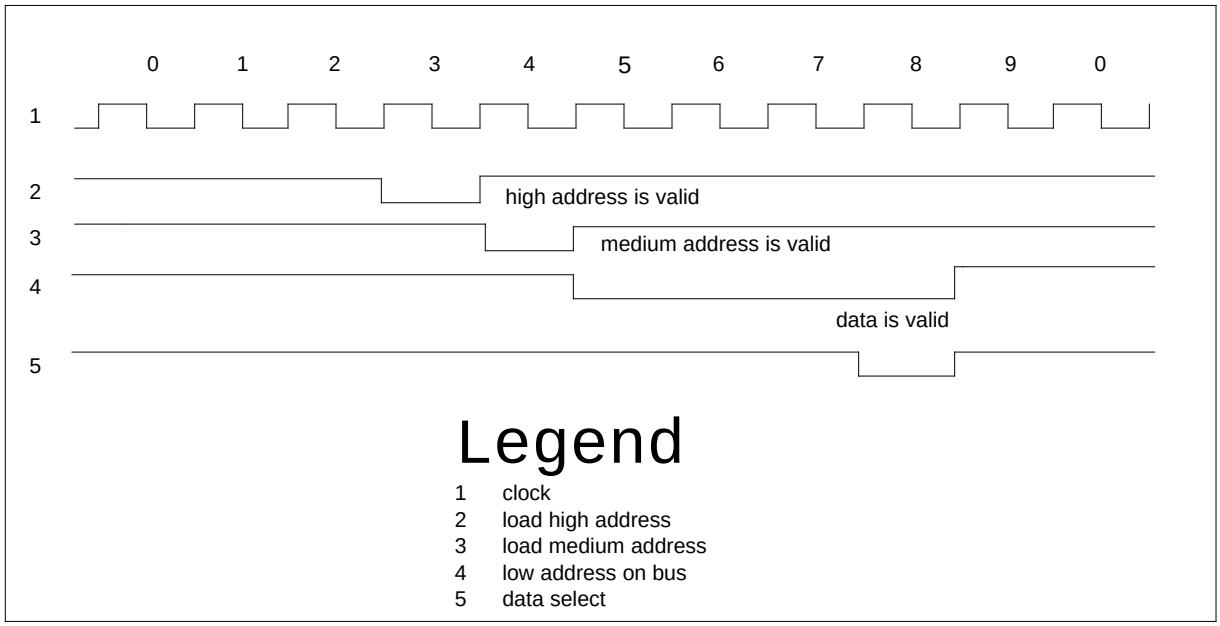
Note 3: Phrase names exactly as they appear.

Signaling

Timing

The following figure shows the timing of the NT1X76AG.

NT1X76AG timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76AG appear in the following tables.

NT1X76AG ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AH

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76AH digital recorded announcement PROM automatic calling card service card.

The NT1X76AH is a double density card (256 Kbytes-two virtual cards). This card occupies one slot in the maintenance trunk module (MTM). The NT1X76AH has a three-position, single-pole, double-throw, dual inline package (DIP) switch. This switch must be set to the number assigned on the card. This number is the BLOCKLIST value you enter in field CARDINFO of Table DRAMS in the digital switching system.

Functional description

The NT1X76AH multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch and the medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal, that the EPROM supplies, enables the data buffer and the row decoder. This signal enables these components when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. Data strobe that the processor sends also enables the data.

Speech memory contents

The following two tables present phrase IDs and content (silences, phrases, and tones) that associate with NT1X76AH the card. The NT1X76AH contains virtual card 0 and virtual card 1.

NT1X76AH Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Content
0	0	1.024		1 s of silence
1	1	0.160		test tone 750 Hz
2	2	0.992		prompt tone
3	3	0.256		0.25 s of silence
4	4	1.216	ACCSTONE	
5	5	5.568	ACCSENG2	The card number is not valid. Please enter your card number again.
6	6	6.464	ACCSENG1	Please enter your calling card number or dial zero to reach an operator. This is a recording.
7	7	3.808	ACCSENG9	Please hang up, then dial zero and the number you are calling.
8	8	7.072	ACCSENG4	The card number is not valid. Please hang up, then dial zero and the number you are calling.
9	9	6.432	ACCSENG8	An incorrect number was dialed. Please hang up, then dial zero and the number you are calling.
A	10	5.024	ACCSENG6	An incorrect number was dialed. Please redial the number you are calling.
B	11	0.608	ACCSENG16	Thank you.

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names are suggestions that can be changed.

NT1X76AH (continued)

NT1X76AH Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Content
C	12	1.504	ACCSENG13	Invalid number.
D	13	6.720	ACCSENG15	We are sorry, your call did not go through. Please try your call again. This is a recording.

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names are suggestions that can be changed.

NT1X76AH Speech memory contents for virtual card 1 (Sheet 1 of 3)

Phrase ID[1] Hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Content
0	0	1.024		1 s of silence
1	1	0.160		test tone 750 Hz
2	2	0.992		prompt tone
3	3	0.256	ACCSPAUSE	0.25 s of silence
4	4	1.216	ACCSTONE	
5	5	1.920	ACCSENG3	Please enter your card number.
6	6	2.176	ACCSENG7	Please dial the number you are calling.
7	7	1.952	ACCSENG5	You may place another call now.
8	8	4.608	ACCSENG12	Valid number, unrestricted PIN, RAO unavailable.
9	9	4.064	ACCSENG10	Valid number, unrestricted PIN, RAO ...

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names are suggestions that can be changed.

NT1X76AH Speech memory contents for virtual card 1 (Sheet 2 of 3)

Phrase ID[1] Hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Content
A	10	3.968	ACCSENG11	Valid number, restricted PIN, RAO ...
B	11	0.704	CENR0	zero (rising inflection)
C	12	0.608	CENR1	one
D	13	0.640	CENR2	two
E	14	0.608	CENR3	three
F	15	0.608	CENR4	four
10	16	0.672	CENR5	five
11	17	0.640	CENR6	six
12	18	0.640	CENR7	seven
13	19	0.608	CENR8	eight
14	20	0.672	CENR9	nine
15	21	0.736	ENG0	zero (flat A intonation)
16	22	0.672	ENG1	one
17	23	0.704	ENG2	two
18	24	0.704	ENG3	three
19	25	0.704	ENG4	four
1A	26	0.704	ENG5	five
1B	27	0.704	ENG6	six
1C	28	0.704	ENG7	seven
1D	29	0.736	ENG8	eight
1E	30	0.672	ENG9	nine

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: Phrase names are suggestions that can be changed.

NT1X76AH (continued)

NT1X76AH Speech memory contents for virtual card 1 (Sheet 3 of 3)

Phrase ID[1] Hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Content
1F	31	0.640	CENF0	zero (falling intonation)
20	32	0.576	CENF1	one
21	33	0.576	CENF2	two
22	34	0.576	CENF3	three
23	35	0.576	CENF4	four
24	36	0.608	CENF5	five
25	37	0.640	CENF6	six
26	38	0.608	CENF7	seven
27	38	0.608	CENF8	eight
28	40	0.640	CENF9	nine

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. All hexadecimal entries must follow the # character (for example, #1F).

Note 2: Phrase time is in seconds.

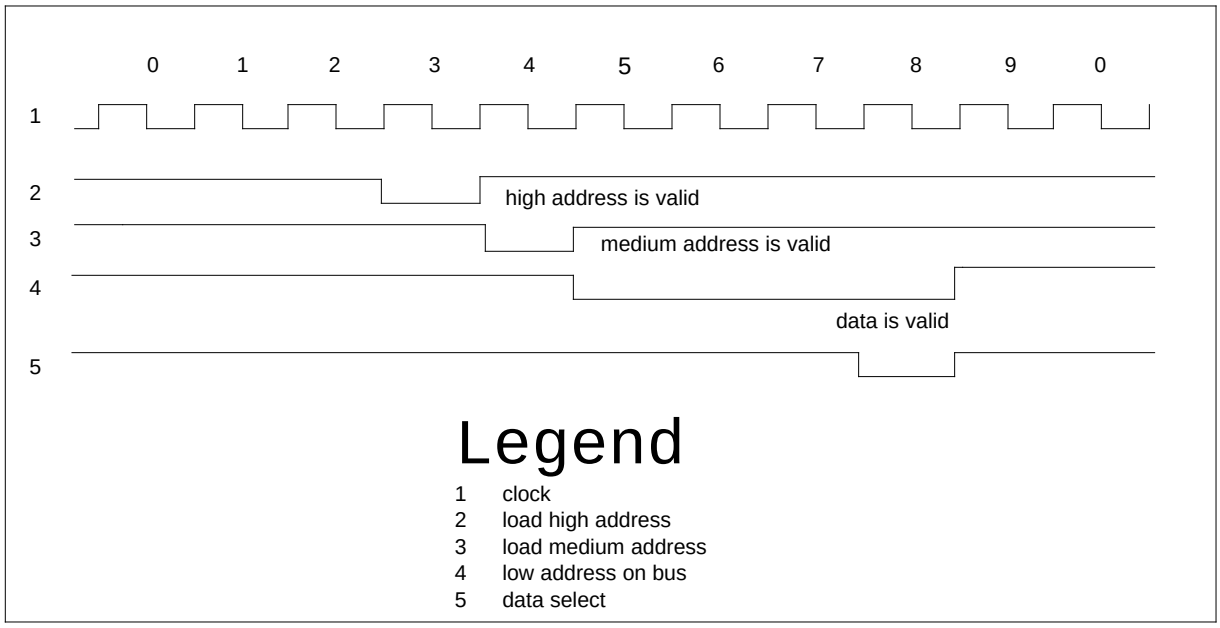
Note 3: Phrase names are suggestions that can be changed.

Signaling

Timing

The following figure describes the timing of the NT1X76AH.

NT1X76AH timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The folowing table provides the ambient conditions for the NT1X76.

NT1X76AH ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AJ

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the EPROM card.

The NT1X76AJ is a double density card (256 Kbytes-two virtual cards). This card occupies one slot in the maintenance trunk module (MTM). The NT1X76AJ has a three-position, single-pole, double-throw, dual inline package (DIP) switch. You must set this switch to the number assigned on the card. This number is the BLOCKLIST value you enter in field CARDINFO of Table DRAMS in the digital switching system.

Functional description

The NT1X76AJ multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch and the medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal, that the EPROM supplies, enables the data buffer and the row decoder. The signal enables these components when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe the processor sends enables the data.

Speech memory contents

The phrase IDs and content (silences, phrases, and tones) associate with the NT1X76AJ CMS/CLASS phase I and II speech ROM card. The NT1X76AJ are virtual card 0 and virtual card 1.

NT1X76AJ Speech memory contents for wvirtual card 0 (Sheet 1 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AJ Speech memory contents for wvirtual card 0 (Sheet 2 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004		0.032	one block of silence
005	3.072		The line was free, but it has just become busy again. You will be notified by special ringing when the line is free. Please hang up now.
	3.264	9.376	
	1.120		
006	2.048		The last number that you called is busy. You will be notified by special ringing when the line is free.
	3.264	8.352	
	1.120		Please hang up now.
007	3.296		You have canceled all of your requests to call someone back. Please hang up now.
	1.120	4.960	
008	3.072		The line was free, but it has just become busy again. You will be notified by special ringing when the line is free. Please hang up now.
	3.264	9.376	
	1.120		
009	1.152		The line is busy.
	3.264	7.456	You will be notified by special ringing when the line is free. Please hang up now.
	1.120		
00A	3.316		You have canceled all of your requests to return calls. Please hang up now.
	1.120	4.800	

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AJ (continued)

NT1X76AJ Speech memory contents for wvirtual card 0 (Sheet 3 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
00B	3.733		We're sorry, the last number that called your line is not known. Please hang up now.
	1.120	5.408	
00C	3.168		We're sorry, the number cannot be reached by this method. Please hang up now.
	1.120	4.832	
00D	6.880		The last call to your telephone has been traced. If you want to take action, contact your police department. Please hang up now.
	1.120	8.544	
00E	0.512	1.024	
			one busy signal beep (including a 0.5 s pause)

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AJ Speech memory contents for wvirtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AJ Speech memory contents for wvirtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
004	6.208	6.272	We're sorry, the number cannot be reached now by this method. Please hang up and try again later.
005	7.680	7.744	The last number that called your line cannot be given out. If you want to call this number, enter 1. In other events, hang up now.
006	7.488	7.552	We're sorry, the last number that you called cannot be reached by this method. Please hang up now and call the number directly.
007	2.848 4.960 1.120	9.952	The last call to your telephone cannot be traced. Please consult the introductory pages of your telephone directory for further instructions. Please hang up now.

Note: Duration includes silence blocks added at the beginning or end.

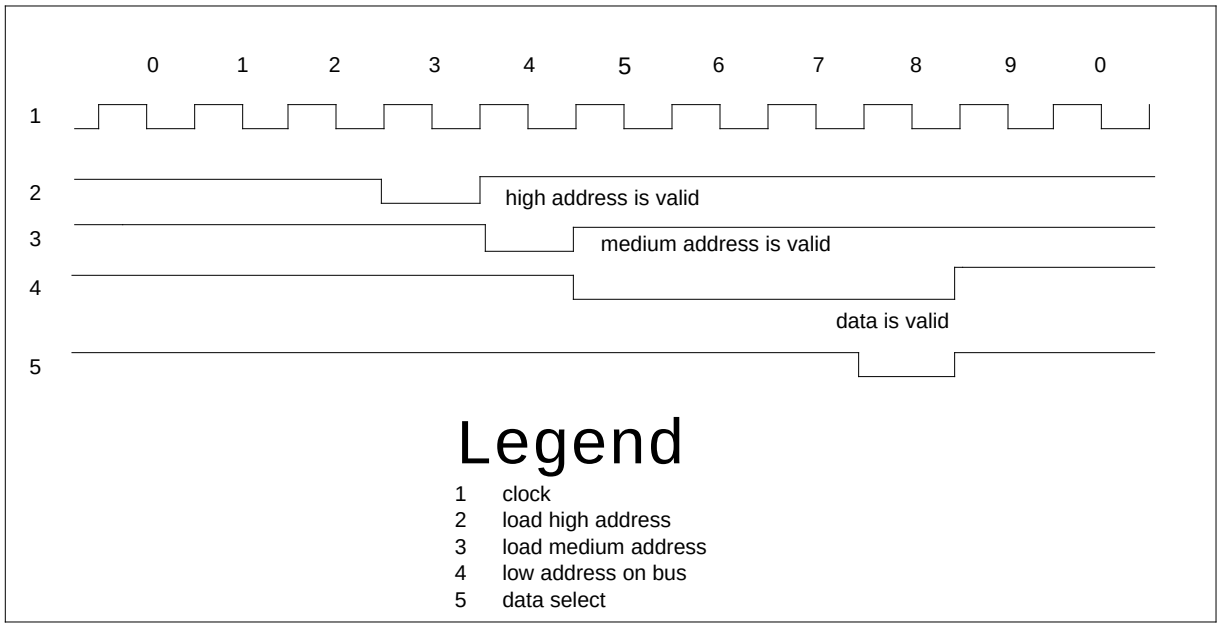
Signaling

Timing

The following figure describes the timing of the NT1X76AJ.

NT1X76AJ (end)

NT1X76AJ timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The following table provides the ambient conditions for the NT1X76.

NT1X76AJ Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AK

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the EPROM card.

The NT1X76AK is a double density card (256 Kbytes-two virtual cards). This card occupies one slot in the maintenance trunk module (MTM). The NT1X76AK has a three-position, single-pole, double-throw, dual inline package (DIP) switch. This switch must be set to the number assigned on the card. This number is the BLOCKLIST value you enter in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AK multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal, that the EPROM supplies, enables the data buffer and the row decoder. The signal enables these components when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. Data strobe that the processor sends enables the data.

Speech memory contents

The phrase IDs and content associate with the NT1X76AK CMS/CLASS phase I and II speech ROM card. The NT1X76AK content includes silences, phrases, and tones. The NT1X76AK are virtual card 0 and virtual card 1.

NT1X76AK Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AK (continued)

NT1X76AK Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	4.672		We're sorry, the last number that you called cannot be reached now by this method. Please hang up and try again later or call the number directly.
	3.904	9.120	
005	2.272	2.656	The last number that called your line was
006	4.096	4.576	To call this number, enter 1; otherwise hang up now.

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AK Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AK Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s second silence
004 - 00D			Digits 0 to 9 with high (rising) intonation
00E - 017			Digits 0 to 9 with low (rising) intonation
018 - 021			Digits 0 to 9 with wave (fallrise) intonation
022 - 02B			Digits 0 to 9 with falling intonation
02C - 035			Digits 0 to 9 with flat intonation
036 - 03F			Digits 0 to 9 with flat intonation

Note: Duration includes silence blocks added at the beginning or end.

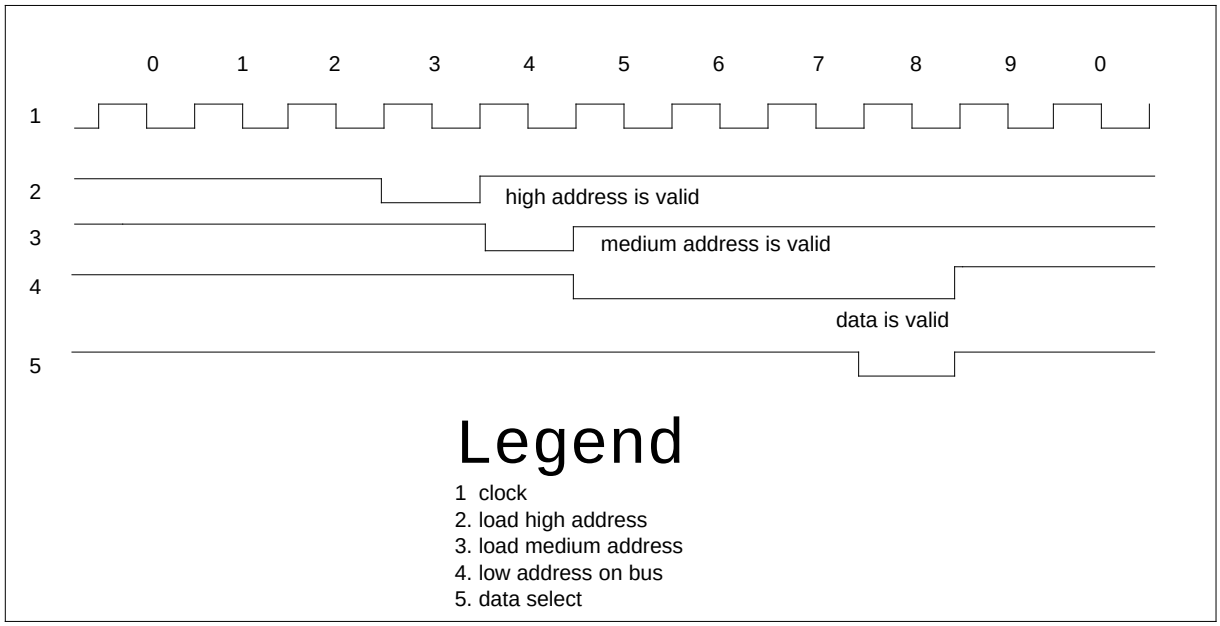
Signaling

Timing

The following figure describes the timing of the NT1X76AK.

NT1X76AK (end)

NT1X76AK timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The following table provides the ambient conditions for the NT1X76AK.

NT1X76AK Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AM

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76AM is a double density card (256 Kbytes-two virtual cards). This card occupies one slot in the maintenance trunk module (MTM). The NT1X76AM has a three-position, single-pole, double-throw, dual inline package (DIP) switch. This switch must be set to the number assigned on the card. This number is the BLOCKLIST value you enter in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AM multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch and the medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal, that the EPROM supplies, enables the data buffer and the row decoder. The signal enables these components when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. Data strobe, that the processor sends, also enables the data.

Speech memory contents

The phrase IDs and content associate with the NT1X76 call forwarding remote access (CFRA) English speech ROM card. The content includes silences, phrases, and tones. The NT1X76AM are virtual card 0 and virtual card 1.

NT1X76AM Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AM (continued)

NT1X76AM Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz ton
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	2.816	3.552	Calls to your telephone will be forwarded to...
005	5.536		To confirm this, press "one"; to forward to a different number, press "two"; to cancel this, please hang up now.
	2,272	8.768	
006	2.080	2.848	Your calls cannot be forwarded to ...
007	1.856	2.368	Please enter another number now.
008	4.288	4.832	Please enter the telephone number to forward, followed by your PIN number.
009	2.816		Calls to your telephone will be forwarded to another number. Please enter this number now.
	1.632	5.856	
00A	3.296	3.840	Please enter a code to remotely access a feature.

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AM Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	4.352	4.896	Please enter a code to activate or to deactivate call forwarding.
005	0.896	1.408	Please enter...
006	0.928	1.088	... the ten-digit
007	3.232	3.424	... telephone number to forward followed by your PIN number.
008	0.928	1.088	... the one-digit
009	0.928	1.056	... the two-digit
00A	0.928	1.088	... the three-digit
00B	0.864	1.024	... the four-digit
00C	0.992	1.152	... the five-digit
00D	0.896	1.056	... the six-digit
00E	0.960	1.120	... the seven-digit

Note: Duration includes silence blocks added at the beginning or end.

NT1X76AM (end)

NT1X76AM Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
00F	0.928	1.088	... the eight-digit
010	0.960	1.120	... the nine-digit
011	0.480	0.992	one

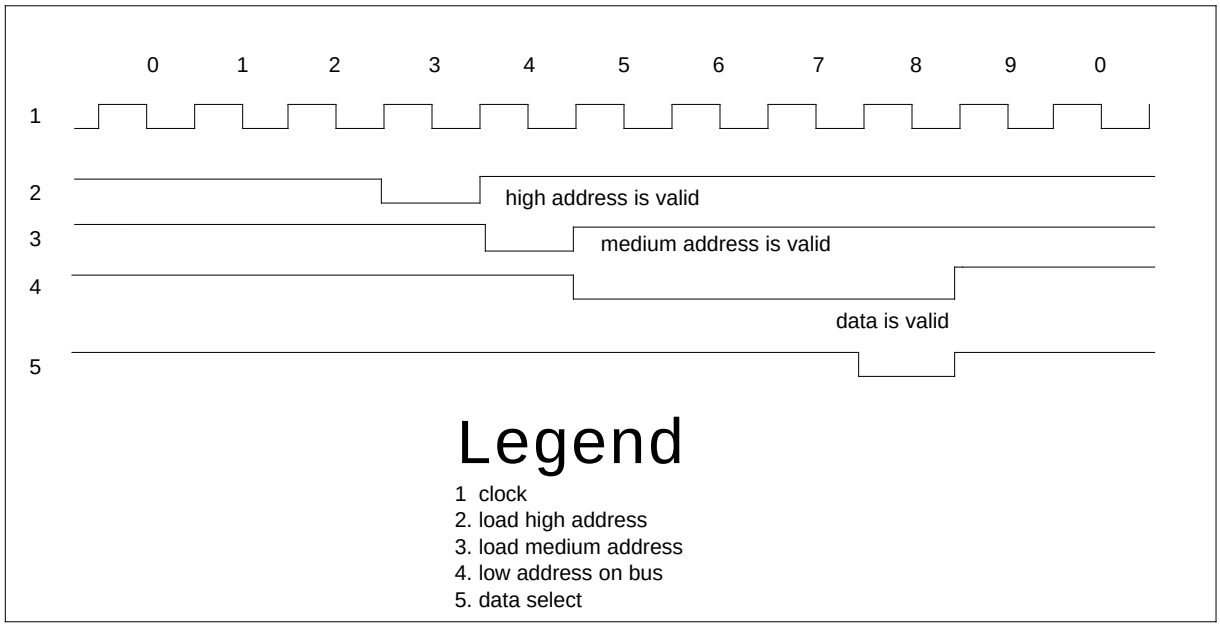
Note: Duration includes silence blocks added at the beginning or end.

Signaling

Timing

The following figure describes the timing of the NT1X76AM.

NT1X76AM timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76AP

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76AP EPROM card.

The NT1X76AP is a double density card (256 kbytes-two virtual cards) and occupies one slot in the maintenance trunk module (MTM). The NT1X76AP has a three-position single-pole double-throw dual inline package (DIP) switch. You must set this switch to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AP multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. When you complete this action, latch the medium address in the medium address latch. The default location of the lower address is the bus.

A decoder EPROM QM27128 provides address decoding, chip enables and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This action occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses activate the outputs of the memory devices, the row addresses function as chip enables. A data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content are silences, phrases and tones. This information, associated with the NT1X76AP CMS/CLASS phase I and II speech ROM

NT1X76AP (continued)

card, appears in the following tables. The two virtual cards in the NT1X76AP are virtual card 0 and virtual card 1.

NT1X76AP Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	4.032	4.704	We are sorry. The digits dialed are not a valid command.
005	6.688	7.232	We are sorry. You must dial a telephone number after dialing the number sign key or the star key.
006	8.128	8.736	We are sorry. You must dial a telephone number after dialing 1, 2, or 1, 1.

Note: Total duration includes silence blocks the system adds at the start or end.

NT1X76AP Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	2.688		To turn this service on, dial 3.
	3.072	21.248	To add an entry, press the number sign key.
	3.776		To remove one or more entries, press the star key.
	3.520		To hear the entries on your list, dial 1.
	3.360		To hear these instructions repeated, dial 0.
	1.280		Please dial now.
005	2.752		To turn this service off, dial 3.
	3.072	21.312	To add an entry, press the number sign key.
	3.776		To remove one or more entries, press the star key.
	3.520		To hear the entries on your list, dial 1.
	3.360		To hear these instructions repeated, dial 0.
	1.280		Please dial now.

Note: Total duration includes silence blocks the system adds at the start or end.

NT1X76AP (continued)

NT1X76AP Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
006	2.688		To turn this service on, dial 3.
	3.328	22.336	To add an entry, dial 1, 2.
	4.608		To remove one or more entries, dial 1, 1.
	3.520		To hear these entries on your list, dial 1.
	3.360		To hear these instructions repeated, dial 0.
	1.280		Please dial now.
007	2.752		To turn this service off, dial 3.
	3.328	22.400	To add an entry, dial 1, 2.
	4.608		To remove one or more entries, dial 1, 1.
	3.520		To hear the entries on your list, dial 1.
	3.360		To hear these instructions repeated, dial 0.
	1.280		Please dial now.

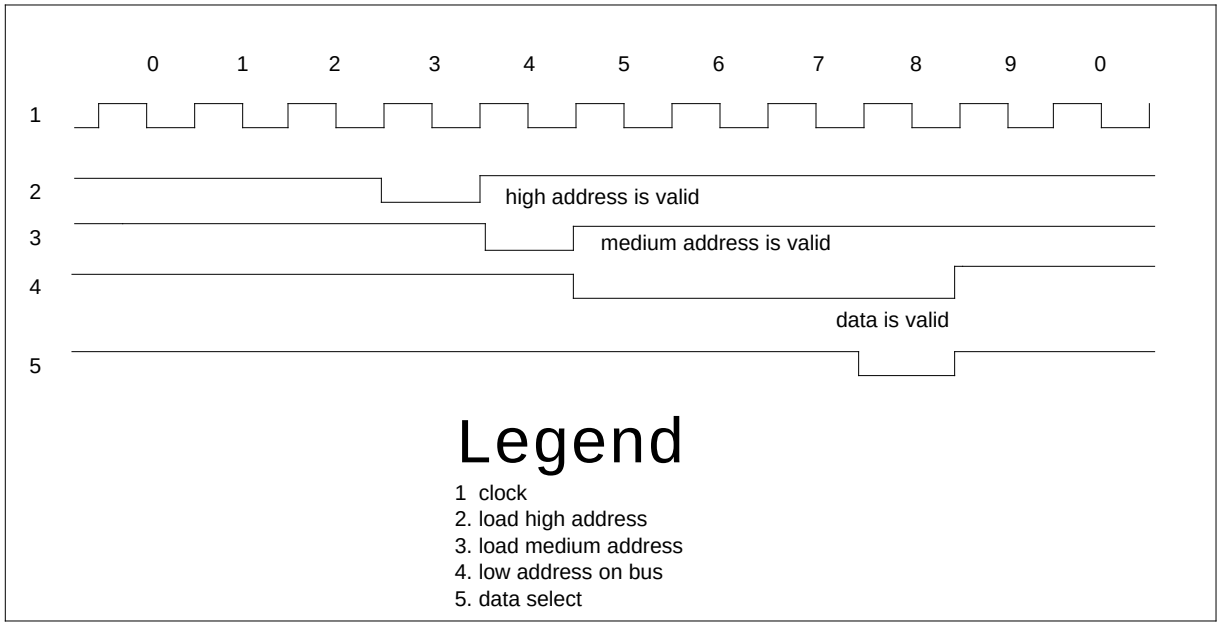
Note: Total duration includes silence blocks the system adds at the start or end.

Signaling

Timing

The timing of the NT1X76AP appears in the following figure.

NT1X76AP timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the appear in the NT1X6AP following table.

NT1X76AP Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AQ

Product description

Digital recorded announcement (DRA) hardware consists of a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76AQ EPROM card.

The NT1X76AQ is a double density card (256 kbytes-two virtual cards) and occupies one slot in the maintenance trunk module (MTM). The NT1X76AQ has a three-position single-pole double-throw dual inline package (DIP) switch. You must set this switch to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AQ multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. After you perform this action, latch the medium address in the medium address latch. The default location of the lower address is the bus.

A decoder EPROM provides address decoding, chip enables and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This action occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses activate the outputs of the memory devices, the row addresses function as chip enables. A data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content are silences, phrases and tones. This information, associated with the NT1X76AQ CMS/CLASS phase I and II speech ROM

card, appears in the following tables. The two virtual cards in the NT1X76AQ are virtual card 0 and virtual card 1.

NT1X76AQ Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	4.672	5.344	Please continue. Dial 0 for instructions or hang up.
005	4.736	5.408	Please start again. Dial 0 for instructions or hang up.
006	3.392	3.936	The number is already on your list as a private entry.
007	2.848	3.392	The number you have removed is a private entry.
008	2.752	3.360	The number to be removed is not on your list.
009	2.336	2.944	There are no more entries on your list.
00A	2.848	3.456	There are no more private entries on your list.
00B	2.816	3.360	The number you have added is a private entry.

Note: Total duration includes silence blocks the system adds at the start or end.

NT1X76AQ (continued)

NT1X76AQ Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	3.584	4.256	Please start again, or dial 0 for instructions.
005	4.640	5.184	We are sorry. The number you have dialed is not available with this service.
006	3.744	4.288	We are sorry. The number you have dialed is incorrect.
007	4.352	4.896	We are sorry. The number of the last calling party is not available.
008	3.264	3.808	We are sorry. You have dialed too few digits.
009	3.136	3.680	We are sorry. You have dialed too many digits.
00A	2.080	2.624	You have cleared the digits dialed.
00B		0.512	.5 s silence
00C		1.024	1 s silence
00D		2.048	2 s silence

Note: Total duration includes silence blocks the system adds at the start or end.

NT1X76AQ Speech memory contents for virtual card 1 (Sheet 2 of 2)

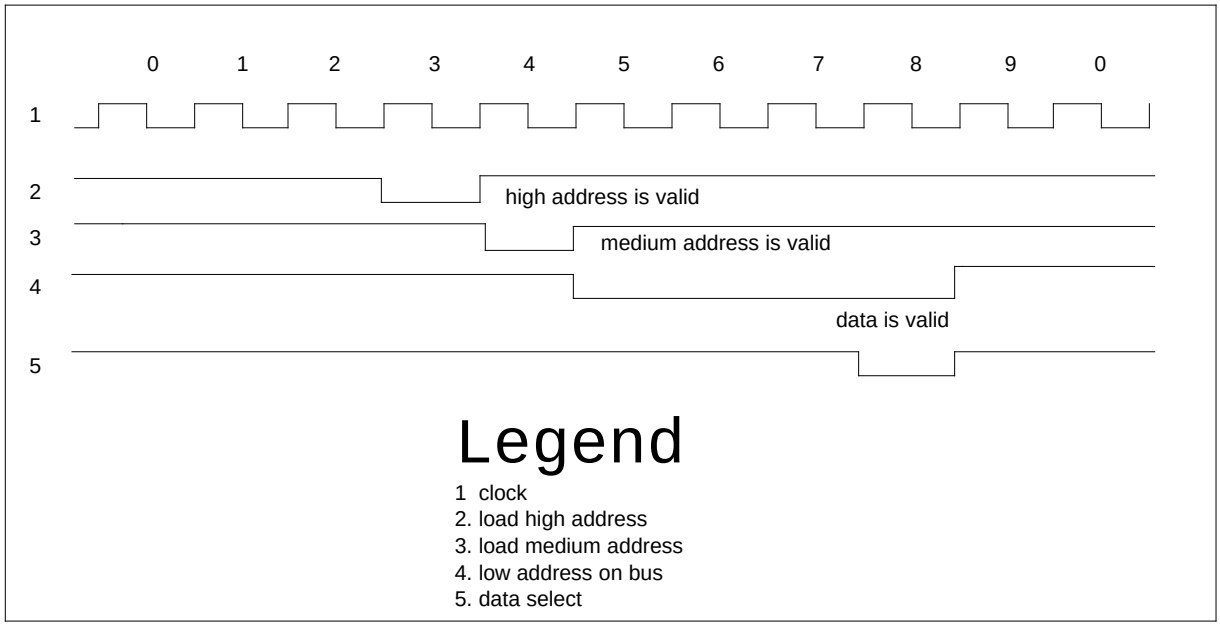
Phrase ID	Duration seconds	Total duration seconds	Content
00E		3.072	3 s silence
00F		4.096	4 s silence
Note: Total duration includes silence blocks the system adds at the start or end.			

Signaling

Timing

The timing of the NT1X76AQ appears in the following figure.

NT1X76AQ timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76AQ (end)

Environmental conditions

The ambient conditions for the NT1X76AQ appear in the following table.

NT1X76AQ Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AR

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76AR EPROM card.

The NT1X76AR is a double-density card (256 kbytes-two virtual cards) and occupies one slot in the maintenance trunk module (MTM). The NT1X76AR has a three-position single-pole double-throw dual inline package (DIP) switch. You must set this switch to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AR multiplexes addresses because 8 bits are available on the backplane and 20 bits are necessary to address the DRA. Latch the high address in the high address latch. After you complete this action, latch the medium address in the medium address latch. The default location of the lower address is the bus.

A decoder EPROM QM27128 provides address decoding, chip enables and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This action occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses activate the outputs of the memory devices, the row addresses function as chip enables. A data strobe from the processor also activates the data.

Speech memory contents

Phrase IDs and silences, phrases and tones associate with the NT1X76AR CMS/CLASS phase I and II speech ROM card. These phrase IDs and silences,

NT1X76AR (continued)

phrases and tones appear in the following tables. The two virtual cards in the NT1X76AR are virtual card 0 and virtual card 1.

NT1X76AR Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration (seconds)	Total duration (seconds)	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.784	3.392	To add an entry, dial 1, 2.
005	3.296	3.904	To add an entry, please press the number sign key.
006	1.984		To reject the last calling party,
	4.576	7.808	dial 1, 2, and then dial 0, 1.
007	1.984		To reject the last calling party,
	7.328	10.560	press the number sign key, dial 0, 1, and then press the number sign key again.

Note: Total duration implies that the phrases have silence blocks added at the start, end or between.

NT1X76AR Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration (seconds)	Total duration (seconds)	Content
008	3.904	4.448	To turn on this service, you must add an entry to your list.
009	6.976	7.648	We are sorry. This service is being interrupted. Please hang up and try again in a few minutes.
Note: Total duration implies that the phrases have silence blocks added at the start, end or between.			

NT1X76AR Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration (seconds)	Total duration (seconds)	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	3.712	4.384	Please continue, or dial 0 for instructions.
005	4.192	4.864	Please try other options, or dial 0 for instructions.
006	4.576	5.184	We are sorry. Please try adding the number again in a few minutes.
Note: Total duration implies that the phrases have silence blocks added at the start, end, or between.			

NT1X76AR (continued)

NT1X76AR Speech memory contents for virtual card 1 (Sheet 2 of 2)

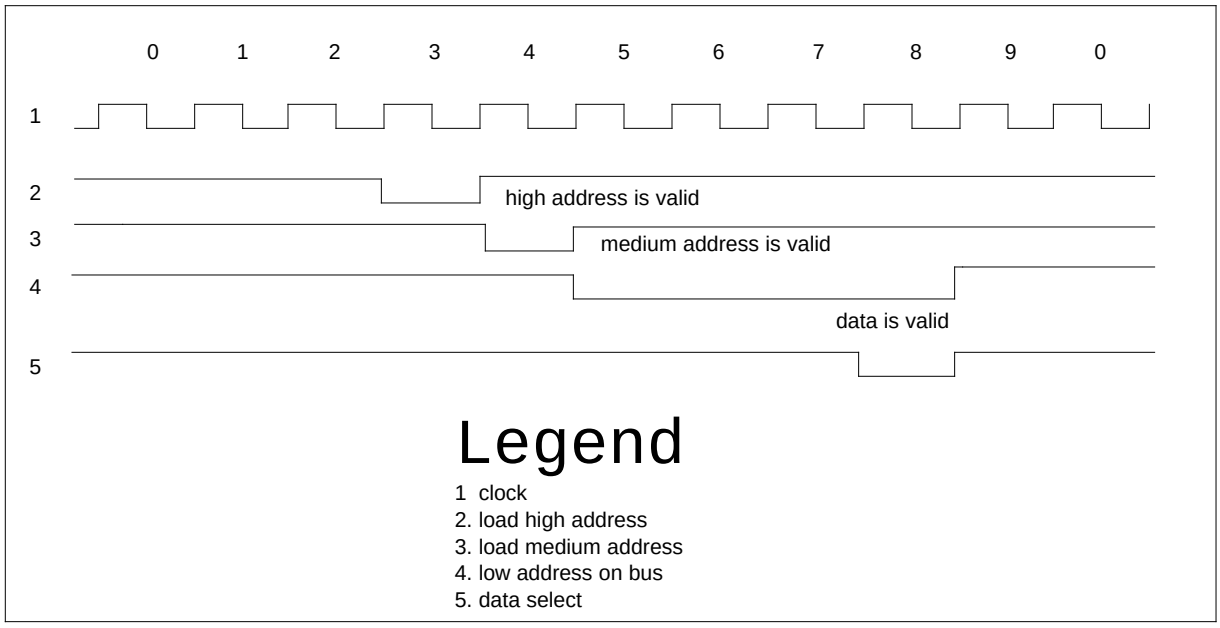
Phrase ID	Duration (seconds)	Total duration (seconds)	Content
007	3.456	4.064	We are sorry. There are no entries on you list.
008	5.592	6.560	We are sorry. Your list is full. You must remove an entry before adding another.
Note: Total duration implies that the phrases have silence blocks added at the start, end, or between.			

Signaling

Timing

The timing of the appears in the following figure.

NT1X76AR timing



Technical data

Electrical requirements

The required voltage is +5V. The required current is 1A.

Environmental conditions

The ambient conditions for the NT1X76AR appear in the following table.

NT1X76AR ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AS

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76AS EPROM card.

The NT1X76AS is a double density card (256 kbytes-two virtual cards) and occupies one slot in the maintenance trunk module (MTM). The NT1X76AS has a three-position single-pole double-throw dual inline package (DIP) switch. You must set this switch to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AS multiplexes addresses because 8 bits are available on the backplane and 20 bits are necessary to address the DRA. Latch the high address in the high address latch. When you complete this action, latch the medium address in the medium address latch. The default location of the lower address is the bus.

A decoder EPROM QM27128 provides address decoding, chip enables and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This action occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses activate the outputs of the memory devices, the row addresses function as chip enables. A data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content are silences, phrases, and tones. This information, associated with the NT1X76AS CMS/CLASS phase I and II speech ROM

card, appears in the following tables. The two virtual cards in the NT1X76AS are virtual card 0 and virtual card 1.

NT1X76AS Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	4.256		Dial the number to be removed, then press the star key again.
	5.664		To remove all entries, dial 0, 8, then press the star key again.
	6.272		To remove just the private entries, dial 0, 9, then press the star key again.
	3.360		To hear these instructions repeated, dial 0.
	1.280	23.808	Please dial now.
005	1.984		Dial the number to be removed.
	3.616		To remove all entries, dial 0, 8.
	4.256		To remove just the private entries, dial 0, 9.

Note: Total duration includes silence blocks the system adds at the start or end.

NT1X76AS (continued)

NT1X76AS Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
	3.360		To hear these instructions repeated, dial 0.
	1.280	17.472	Please dial now.
Note: Total duration includes silence blocks the system adds at the start or end.			

NT1X76AS Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	4.352		Dial the number to be added, then press the number sign key again.
	6.144		To add the last calling party, dial 0, 1, then press the number sign key again.
	1.280	13.664	Please dial now.
005	1.792		Dial the number to be added.
Note: Total duration includes silence blocks the system adds at the start or end.			

NT1X76AS Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
	3.872		To add the last calling party, dial 0, 1.
	1.280	8.832	Please dial now.
006	5.760		Please dial now.
	1.280	8.288	Please dial the number to which you want your calls forwarded, then press the number sign key.
007	3.520		Please dial the number to which you want your calls forwarded.
	1.280	6.048	Please dial now.

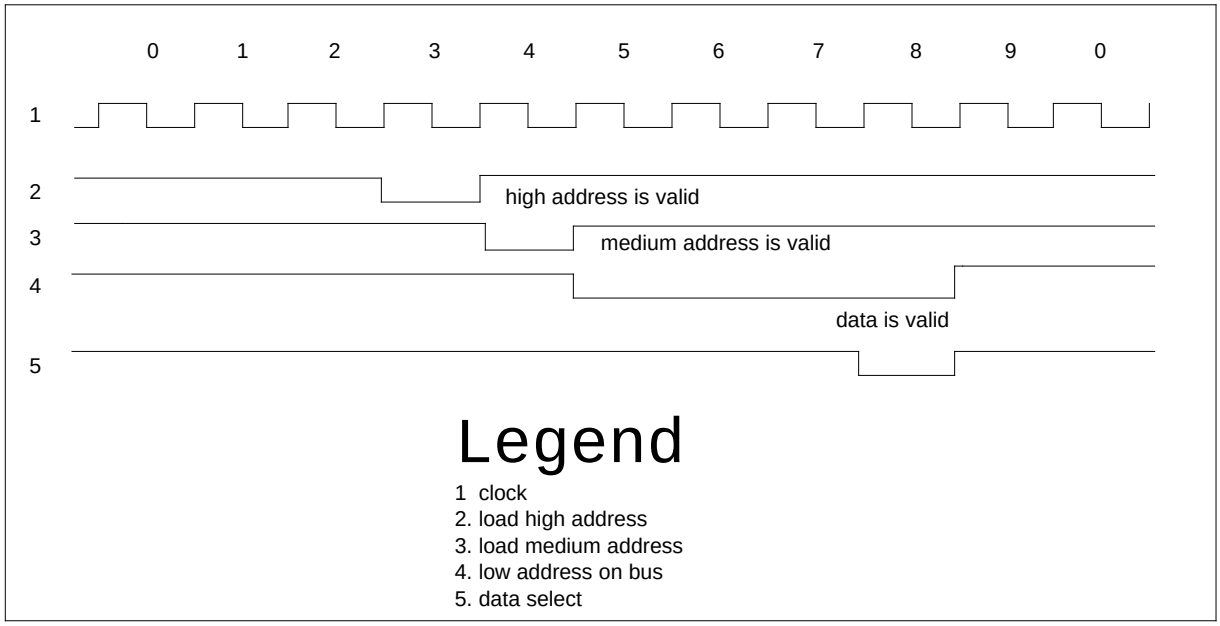
Note: Total duration includes silence blocks the system adds at the start or end.

Signaling

Timing

The timing of the NT1X76AS appears in the following figure.

NT1X76AS timing



NT1X76AS (end)

Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76AS appear in the following table.

NT1X76AS Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AT

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76AT EPROM card.

The NT1X76AT is a double density card (256 kbytes-two virtual cards) and occupies one slot in the maintenance trunk module (MTM). The NT1X76AT has a three-position single-pole double-throw dual inline package (DIP) switch. You must set the switch to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AT multiplexes addresses because 8 bits are available on the backplane and 20 bits are necessary to address the DRA. Latch the high address in the high address latch. When this action is complete, latch the medium address in the medium address latch. The default location of the lower address is the bus.

A decoder EPROM QM27128 provides address decoding, chip enables and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This action occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses activate the outputs of the memory devices, the row addresses function as chip enables. A data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content are silences, phrases and tones. This information, associated with the NT1X76AT CMS/CLASS phase I and II speech ROM

NT1X76AT (continued)

card, appears in the following tables. The two virtual cards in the NT1X76AT are virtual card 0 and virtual card 1.

NT1X76AT Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	0.576	1.600	Next,
005	1.760	2.784	Next, extension
006	0.832	1.856	Repeating,
007	1.984	3.008	Repeating, extension
008	1.536	1.888	The number you have dialed,
009	1.312	1.952	is not permitted.
00A	1.920	2.336	The number you have added is
00B	2.400	2.816	The number you have added is extension
00C	1.824	2.304	The number you have removed is

Note: Total duration includes silence blocks the system adds at the start or end.

NT1X76AT Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
00D	2.400	2.816	The number you have removed is extension
00E	2.112	2.592	The first entry on your list is
00F	2.848	3.328	The first entry on your list is extension
010	2.304	2.912	This number is already on your list.
011	3.744	4.224	This number is already on your list. Extension
012	2.272	2.688	Your calls will be forwarded to
Note: Total duration includes silence blocks the system adds at the start or end.			

NT1X76AT Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004 - 00D			Digits 0 - 9 with high (rising) intonation.
Note: Total duration includes silence blocks the system adds at the start or end.			

NT1X76AT (continued)

NT1X76AT Speech memory contents for virtual card 1 (Sheet 2 of 2)

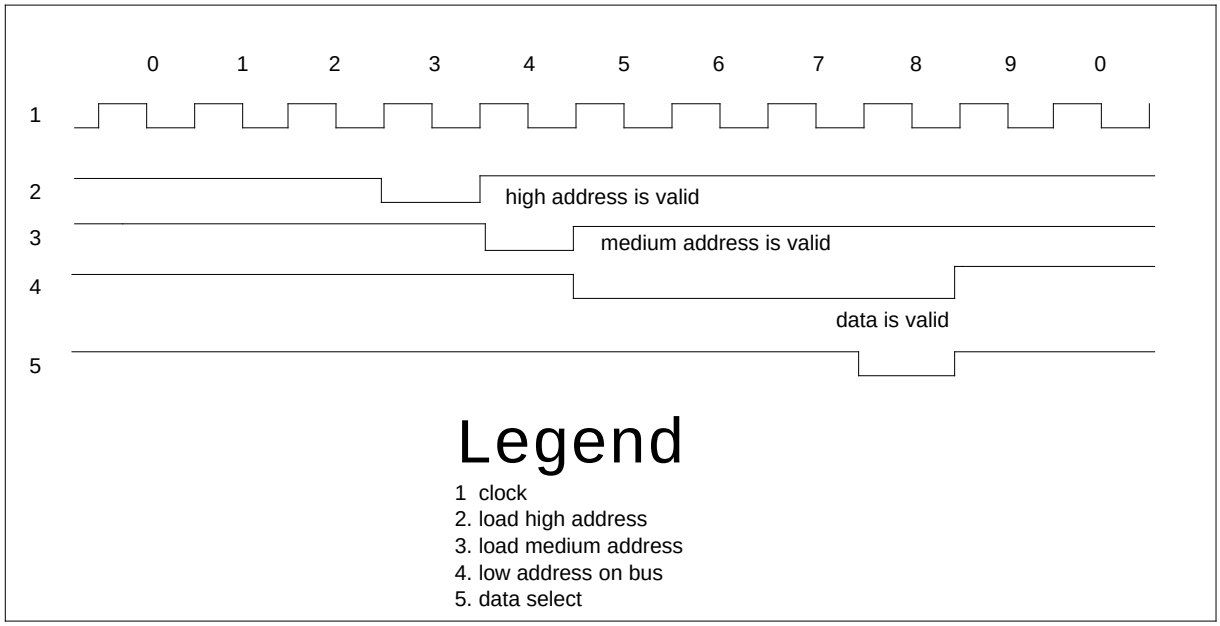
Phrase ID	Duration seconds	Total duration seconds	Content
00E - 017			Digits 0 - 9 with low (rising) intonation.
018 - 021			Digits 0 - 9 with wave (fallrise) intonation.
022 - 02B			Digits 0 - 9 with falling intonation.
02C - 035			Digits 0 - 9 with flat intonation.
036 - 03F			Digits 0 - 9 with flat intonation.
Note: Total duration includes silence blocks the system adds at the start or end.			

Signaling

Timing

The timing of the NT1X76AT appears in the following figure.

NT1X76AT timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76AT appear in the following table.

NT1X76AT Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AU

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76AU EPROM card contains permanent memory.

The NT1X76AU, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76AU has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76AU multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The busy contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses function as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76AU CMS/CLASS phase I and II speech read only memory (ROM) card appear in the following

two tables. The content can be silences, phrases, and tones. The two virtual cards in the NT1X76AU are virtual card 0 and virtual card 1.

NT1X76AU Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration (seconds)	Total duration (seconds)	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	0.25 s silence
004	2.560	3.168	There is one private entry on your list.
005	2.624	3.232	There are two private entries on your list.
006	2.336	2.944	There are three private entries on your list.
007	2.496	3.104	There are four private entries on your list.
008	2.624	3.232	There are five private entries on your list.
009	2.432	3.040	There are six private entries on your list.
00A	2.464	3.072	There are seven private entries on your list.
00B	2.464	3.072	There are eight private entries on your list.
00C	2.560	3.168	There are nine private entries on your list.
00D	2.400	3.008	There are ten private entries on your list.

Note: Total duration implies that the phrases have silence blocks added at the start, end, or between.

NT1X76AU (continued)

NT1X76AU Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration (seconds)	Total duration (seconds)	Content
00E	2.496	3.104	There are 11 private entries on your list.
00F	2.560	3.168	There are 12 private entries on your list.
Note: Total duration implies that the phrases have silence blocks added at the start, end, or between.			

NT1X76AU Speech memory content for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration (seconds)	Total duration (seconds)	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone002
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	1.792	2.464	including one private entry.
005	1.952	2.624	including two private entries.
006	1.824	2.496	including three private entries.
007	2.048	2.720	including four private entries.
008	2.016	2.688	including five private entries.
Note: Total duration implies that the phrases may have silence blocks added at the start, end, or between.			

NT1X76AU Speech memory content for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration (seconds)	Total duration (seconds)	Content
009	1.856	2.528	including six private entries.
00A	2.080	2.752	including seven private entries.
00B	1.920	2.592	including eight private entries.
00C	1.856	2.528	including nine private entries.
00D	2.080	2.752	including ten private entries.
00E	2.048	2.720	including 11 private entries.
00F	1.984	2.656	including 12 private entries.
010	1.792	3.008	This is the end of your list.
011	4.000	5.216	This is the end of your list. Your list is now empty.
Note: Total duration implies that the phrases may have silence blocks added at the start, end, or between.			

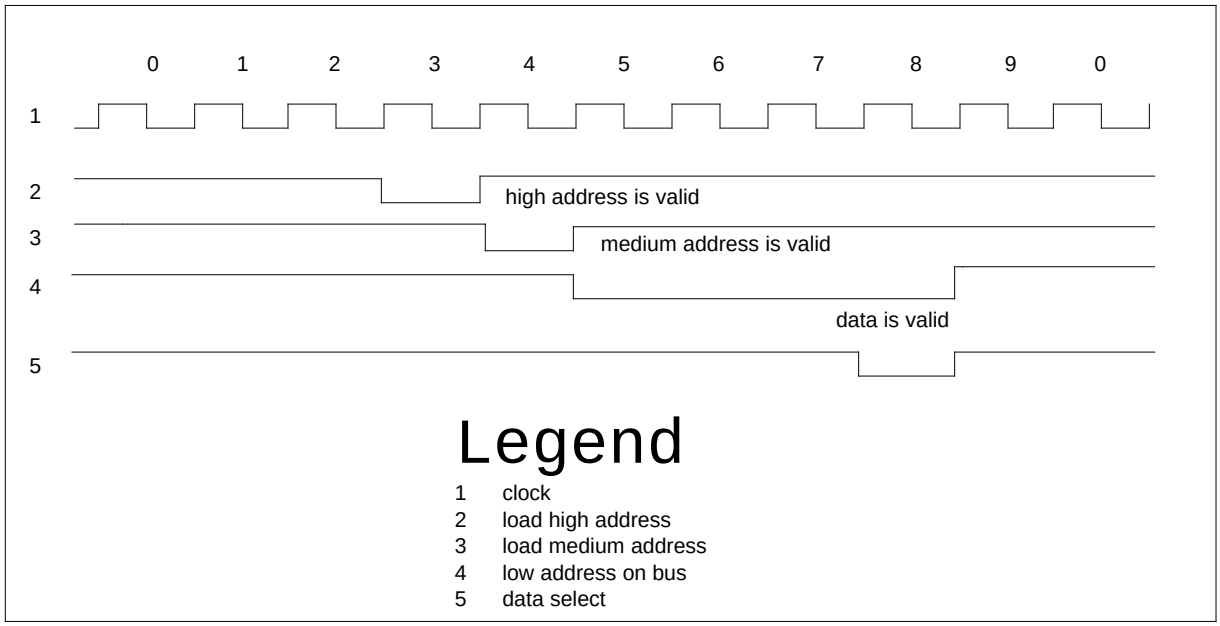
Signaling

Timing

The timing of the NT1X76AU appears in the following figure.

NT1X76AU (end)

NT1X76AU timing



Technical data

Electrical requirements

The required voltage is +5V. The required current is 1A.

Environmental conditions

The following table provides the ambient conditions for the NT1X76AU.

NT1X76AU ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76AV

Product description

Digital recorded announcement (DRA) hardware includes a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76AV EPROM card.

The NT1X76AV is a double density card. The NT1X76AV has 256 Kbytes-two virtual cards. The card occupies one slot in the maintenance trunk module (MTM). The card has a single-pole double-throw dual inline package (DIP) switch. The DIP switch has three positions. You must set the switch to the number assigned on the card. This number is the BLOCKLIST value that appears in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76AV multiplexes addresses because only eight bits are available on the backplane. You require 20 bits to address the DRA. The high address latches in the high address latch. The medium address latches in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal enables the data buffer and the row decoder. The signal enables the buffer and decoder when the decoded address is in the address range of the memory devices. The EPROM supplies the card enable signal.

The row and column address decoders inform the memory devices when column and row addresses are present. While the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. A data strobe enables the data. The processor sends the data strobe.

Speech memory contents

The phrase IDs and content appear in the following two tables. The phrase IDs and content are associated with the NT1X76AV CMS/CLASS phase I and II

NT1X76AV (continued)

speech ROM card. The phrase content includes silences, phrases and tones. The two virtual cards in the NT1X76AV are virtual card 0 and virtual card 1.

NT1X76AV Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s second silence
004	4.608	5.280	Please continue, dial 0 for instructions, or hang up.
005	4.608	5.824	Please continue, dial 0 for instructions, or hang up.
006	1.824	2.176	The list contains one entry.
007	1.760	2.112	The list contains two entries.
008	1.952	2.304	The list contains three entries.
009	2.048	2.400	The list contains four entries.
00A	2.080	2.432	The list contains five entries.
00B	1.984	2.336	The list contains six entries.
00C	2.080	2.432	The list contains seven entries.
00D	2.016	2.368	The list contains eight entries.

Note: Total duration includes silence block added to the beginning or end

NT1X76AV Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
00E	2.080	2.432	The list contains nine entries.
00F	1.856	2.208	The list contains ten entries.
010	2.144	2.496	The list contains 11 entries.
011	2.080	2.432	The list contains 12 entries.
Note: Total duration includes silence block added to the beginning or end			

NT1X76AV Speech memory contents for visual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
		0.992	
003		0.256	.25 s second silence
004	4.064	4.736	Please try other options, or dial 0 for instructions.
005	2.016	2.624	There is one entry on your list
006	1.984	2.592	There are two entries on your list.
Note: Total duration includes silence blocks at the beginning or end			

NT1X76AV (continued)

NT1X76AV Speech memory contents for visual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
007	2.016	2.624	There are three entries on your list.
008	2.112	2.720	There are four entries on your list.
009	2.208	2.816	There are five entries on your list.
00A	1.984	2.592	There are six entries on your list.
00B	2.304	2.912	There are seven entries on your list.
00C	1.952	2.560	There are eight entries on your list.
00D	2.016	2.624	There are nine entries on your list.
00E	2.048	2.656	There are ten entries on your list.
00F	2.112	2.720	There are 11 entries on your list.
010	2.144	2.752	There are 12 entries on your list.
011	2.016	2.624	There are no entries on your list.

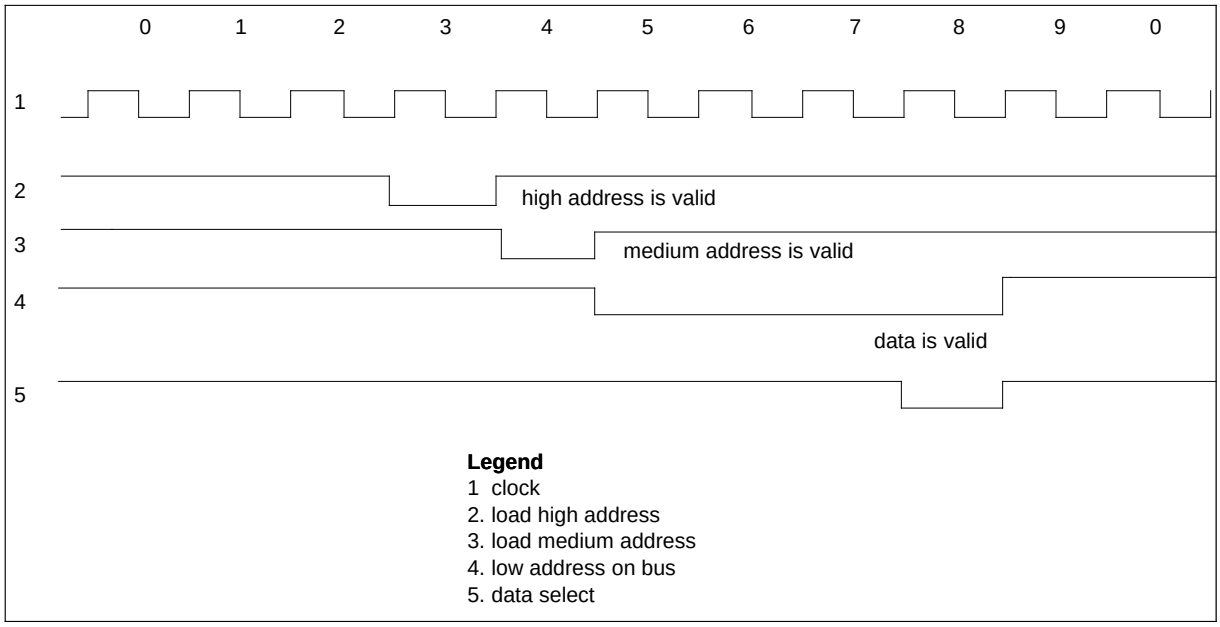
Note: Total duration includes silence blocks at the beginning or end

Signaling

Timing

The timing of the NT1X76AV appears in the following figure.

NT1X76AV timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76AV appear in the following table.

NT1X76AV Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30°C	5 to 49°C
Relative humidity	20% to 55%	20% to 80%

NT1X76AW

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76AW EPROM card contains permanent memory.

The NT1X76AW, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76AW has a three-position, single-pole, double-throw, dual inline package (DIP) switch. You must set the DIP switch to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76AW multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The busy contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses function as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76AW CMS/CLASS phase I and II speech read only memory (ROM) card appear in the following

two tables. The content can be silences, phrases and tones. The two virtual cards in the NT1X76AW are virtual card 0 and virtual card 1.

NT1X76AW Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration Seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
		0.992	
003		0.256	.25 s silence
004	2.464	3.072	Your call block service is now on.
005	2.208	2.816	Your call block service is now off.
006	2.624	3.232	Your call screen service is now on.
007	2.368	2.976	Your call screen service is now off.
008	3.456	4.064	Your selective call forwarding service is now on.
009	3.264	3.872	Your selective call forwarding service is now off.
00A	3.584	4.192	Your distinctive ringing call waiting service is now on.
00B	3.712	4.320	Your distinctive ringing call waiting service is now off.

Note: Total duration includes silence blocks are added at the start or end

NT1X76AW (continued)

NT1X76AW Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration Seconds	Total duration seconds	Content
00C	2.464	3.072	Your avoid-a-call service is now on.
00D	2.464	3.072	Your avoid-a-call service is now off.
00E	0.352	1.024	Prompt tone
Note: Total duration includes silence blocks are added at the start or end			

NT1X76AW Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration Seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
		0.992	
003		0.256	.25 s silence
004	6.944	8.224	If this number is correct, dial 1. If this number is not correct, dial 0.
005	1.280	1.952	Please dial now.
006	6.048	6.720	We are sorry. Please hang up now, consult your written instructions, and try again later.
Note: Total duration includes silence blocks are added at the start or end			

NT1X76AW Speech memory contents for virtual card 1 (Sheet 2 of 2)

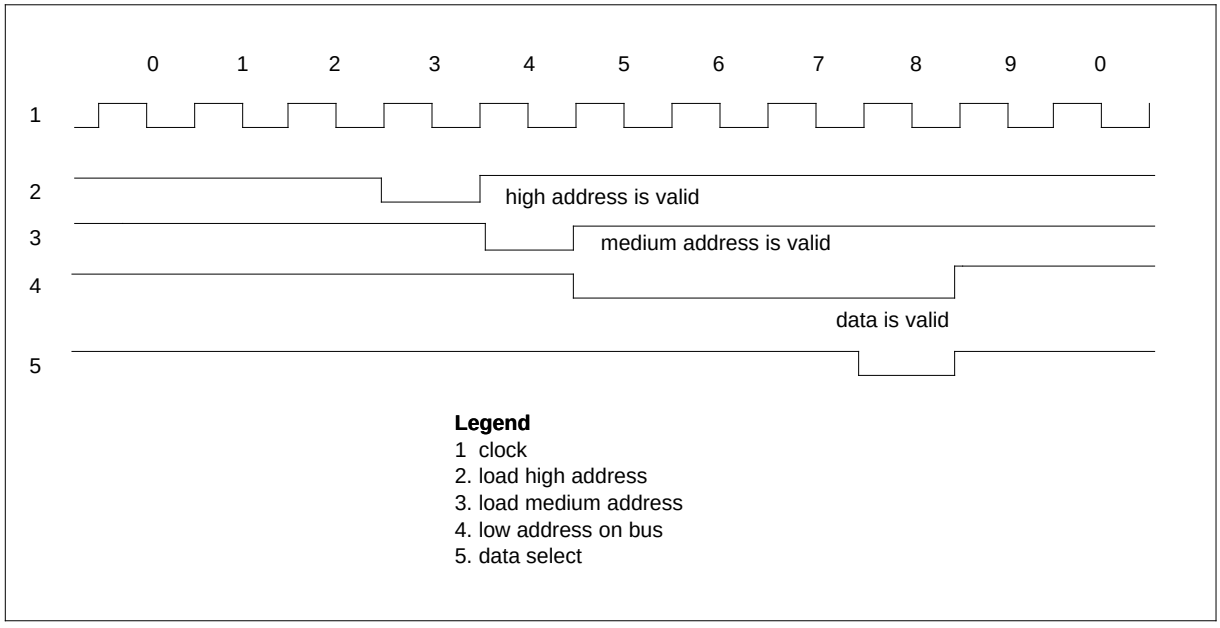
Phrase ID	Duration Seconds	Total duration seconds	Content
007	6.048	7.264	We are sorry. Please hang up now, consult your written instructions, and try again later.
008	5.600	6.272	You may dial during announcements for faster service. When you have finished, hang up.
009	7.104	7.776	After hearing an entry, you may dial 0, 7 to delete it and continue reviewing your list.
Note: Total duration includes silence blocks are added at the start or end			

Signaling

Timing

The timing of the NT1X76AW appears in the following figure.

NTX76AW timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76AW (end)

Environmental conditions

The ambient conditions for the NTX76AW appear in the following table.

NT1X76AW Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76BA

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76BA EPROM card contains permanent memory.

The NT1X76BA, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BA has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BA multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The busy contains the lower address latch by default.

To activate the card, the card select compares A18, A10, and A20 with an attached DIP switch. The A0 is gated to provide for the addressing mode of the DRA. The DRA requires 4 bits at a time. The DRA is best to store 8 bits. The controller hardware requires 8 bits and stores the alternate 4 bits for the next cycle. The card-select circuits provide access if A0 is 0. The data is gated to the output bus and back to the microprocessor during the DS data strobe.

Addresses A12 to A17 (A13 to A18 for the QM2732D1 version) are decoded for the EPROM chip enables. Each EPROM has two enables that you must pull low to allow the data on the outputs. Arrange 8 row enables and 8 column enables to simplify the addressing of the memory array. Only 1 chip of the 64 chips receives row and column enables at the same time. Only 1 chip supplies data at any one time for this reason.

NT1X76BA (continued)

Speech memory contents

The phrase IDs and content associated with the NT1X76BA appear in the following table. The content can be silences, phrases and tones.

NT1X76BA Speech memory contents (Sheet 1 of 2)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
0	0	1.024	-	1 s of silence
1	1	0.160	-	test tone 760 Hz at -13 dbm
2	2	0.992	-	prompt tone
3 to 7	3 to 7	-	-	reserved phrase
8 to 27	8 to 39	-	SIT1 to SIT32	SIT combination 1 (refer to note) to SIT combination 32 (refer to the table on page 4)
28	40	9.248	N-NCA, SOA	Tous les circuits sont occupes pour l'instant. Veuillez rappeler un peu plus tard. Ce message est enregistre. (pause) (code d'identification)
29	41	8.960	P-ROA	Des difficultes techniques nous d'acheminer votre appel. Veuillez raccocher et composer de nouveau. Ce message est enregistre. (pause) (code d'identification)
2A	42	12.032	L-VCA, UCA	Nous avons de la difficulte a vous avez demandee. Veuillez verifier le numero et composer de nouveau, ou demander l'aide du telephoniste. Ce message est enregistre. (pause) (code d'identification)
2B	43	12.544	ROH	Veuillez raccrocher et composer de nouveau. Si l'aide de la telephoniste est necessaire, raccrochez et composez son numero. S'il vous plait, veuillez raccrocher. Ce message est enregistre.

Note 1: Phrase ID can be in hexadecimal or decimal

Note 2: This is a suggested phrase name. You can change the phrase name, if necessary

NT1X76BA Speech memory contents (Sheet 2 of 2)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
2C	44	6.208	VDN	Il n'y a pas de service au numero que vous avez rejoint. Ce message est enregistre.
2D	45	10.592	M-MCA	Le numero compose est un appel local. Ne composez pas le 1 precedent le numero appelle. Ce message est enregistre.
2E	46	10.016	MCL	Le numero compose est un apel interurbain. Veuillez composer le 1 precedent le numero appele. Ce message est enregistre.
2F	47	0.608	digit 0	zero
30	48	0.519	digit 1	un
31	49	0.544	digit 2	deux
32	50	0.544	digit 3	trois
33	51	0.640	digit 4	quatre
34	52	0.768	digit 5	cinq
35	53	0.640	digit 6	six
36	54	0.672	digit 7	sept
37	55	0.544	digit 8	huit
38	56	0.672	digit 9	neuf

Note 1: Phrase ID can be in hexadecimal or decimal

Note 2: This is a suggested phrase name. You can change the phrase name, if necessary

NT1X76BA (continued)

The special information tones, timing and frequencies appear in the following table.

Special Information Tone (SIT) descriptions (Sheet 1 of 2)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
8	8	SIT1	1 short	1 short	1 short
9	9	SIT2	1 short	1 short	1 long
A	10	SIT3	1 short	1 long	1 short
B	11	SIT4	1 short	1 long	1 long
C	12	SIT5	1 short	1 short	1 short
D	13	SIT6	1 short	1 short	1 long
E	14	SIT7	1 short	1 long	1 short
F	15	SIT8	1 short	1 long	1 long
10	16	SIT9	1 long	1 short	1 short
11	17	SIT10	1 long	1 short	1 long
12	18	SIT11	1 long	1 long	1 short
13	19	SIT12	1 long	1 long	1 long
14	20	SIT13	1 long	1 short	1 short
15	21	SIT14	1 long	1 short	1 long
16	22	SIT15	1 long	1 long	1 short
17	23	SIT16	1 long	1 long	1 long
Note: SIT components					
Frequencies(Hz)			First Tone	Second Tone	Third Tone
		low	913.8	1370.6	1776.7
		high	985.2	1468.5	NA
Duration (ms)		short	288		
		long	384		

Special Information Tone (SIT) descriptions (Sheet 2 of 2)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
18	24	SIT17	1 short	1 short	1 short
19	25	SIT18	1 short	1 short	1 long
1A	26	SIT19	1 short	1 long	1 short
1B	27	SIT20	1 short	1 long	1 long
1C	28	SIT21	1 short	1 short	1 short
1D	29	SIT22	1 short	1 short	1 long
1E	30	SIT23	1 short	1 long	1 short
1F	31	SIT24	1 short	1 long	1 long
20	32	SIT25	1 long	1 short	1 short
21	33	SIT26	1 long	1 short	1 long
22	34	SIT27	1 long	1 long	1 short
23	35	SIT28	1 long	1 long	1 long
24	36	SIT29	1 long	1 short	1 short
25	37	SIT30	1 long	1 short	1 long
26	38	SIT31	1 long	1 long	1 short
27	39	SIT32	1 long	1 long	1 long
Note: SIT components					
Frequencies(Hz)			First Tone	Second Tone	Third Tone
		low	913.8	1370.6	1776.7
		high	985.2	1468.5	NA
Duration (ms)		short	288		
		long	384		

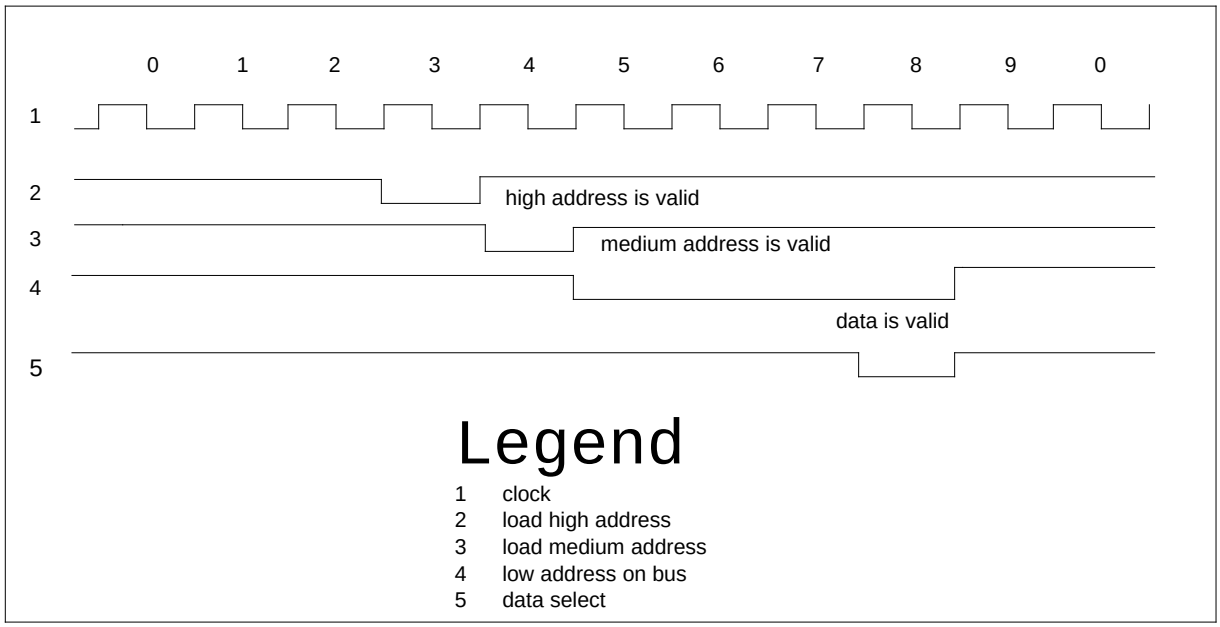
NT1X76BA (end)

Signaling

Timing

The timing of the NT1X76AB appears in the following figure.

NT1X76AB timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 2.2A.

Environmental conditions

The ambient conditions for the NT1X76BA appear in the following table.

NT1X76AB ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30°C	5 to 49°C
Relative humidity	20% to 55%	20% to 80%

NT1X76BF

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76BF digital recorded announcement PROM auxiliary operator service system, voice response French card 1.

The NT1X76BF, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BF has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BF multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The bus contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses function as chip enables. The data strobe from the processor also activates the data.

NT1X76BF (continued)

Speech memory contents

The phrase IDs and content associated with the NT1X76BF card appear in the following two tables. The content can be silences, phrases and tones. The two virtual cards in the NT1X76BF are virtual card 0 and virtual card 1.

NT1X76BF Speech memory contents for virtual card 0 (Sheet 1 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s of silence
1	1	0.160		test tone 760 Hz at -13dbm
2	2	0.992		prompt tone
3	3	0.512		0.5 s of silence
4	4	5.856	AVRF03	a ete remplace. Vous pouvez maintenant appeler sans frais le: un, huit-cent
5	5	1.216	AVRF06	est en derangement
6	6	3.936	AVRF07	est en derangement. Mais, vous pouvez joindre l'abonne au
7	7	1.088	AVRF08	est suspendu
8	8	2.300	AVRF09	est suspendu. Mais, vous pouvez joindre l'abonne au
9	9	1.472	AVRF12	n'est plus en service
A	10	4.320	AVRF13	n'est plus en service. Mais, vous pouvez joindre l'abonne au
B	11	2.560	AVRF14	vous devez maintenant appeler le
C	12	4.608	AVRF15	vous pouvez maintenant appeler sans frais le: un, huit-cent
D	13	4.608	AVRF18	Ce numero a ete remplace. Vous pouvez maintenant appeler sans frais le: un, huit-cent
E	14	2.272	AVRF20	Ce numero n'est plus en service.

Note 1: Phrase ID is in hexadecimal or decimal form when you use the ASSIGN command in the DRAMREC. The # character must precede allhexadecimal entries. For example, #1F

Note 2: Phrase time is in seconds

Note 3: Use phrase names exactly as the names appear

NT1X76BF Speech memory contents for virtual card 0 (Sheet 2 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
F	15	5.248	AVRF21	Il n'y a plus d'abonne a ce numero. Vous devez maintenant appeler le
10	16	7.232	AVRF22	Il n'y a plus d'abonne a ce numero. Vous pouvez maintenant appeler sans frais le: un, huit-cent
11	17	4.096	AVRF23	En raison d'un incendie, ce numero n'est plus en service.
12	18	6.560	AVRF24	En raison d'un incendie, ce numero n'est plus en service. Mais, vous pouvez joindre l'abonne au
13	19	2.240	AVRF25	en raison d'un incendie, le
14	20	2.592	AVRF26	je repete
15	21	3.552	AVRF27	Je repete. Le numero est
16	22	4.320	AVRF28	Je repete. Le numero est: un
17	23	5.216	AVRF29	Je repete. Le numero est: un, huit-cent
18	24	4.608	AVRF32	L'abonne a change d'adress. Il n'y a plus d'abonne a ce numero.
19	25	2.304	AVRF36	La ligne est en derangement.
1A	26	5.056	AVRF37	La ligne est en derangement. Mais, vous pouvez joindre l'abonne au
1B	27	1.472	AVRF40	le numero est
1C	28	2.304	AVRF41	le numero est: un
1D	29	6.144	AVRF53	Vous pouvez obtenir le numero sans frais. Le numero est: un, huit-cent
1E	30	3.360	AVRF58	est en service. Veuillez refaire votre appel.

Note 1: Phrase ID is in hexadecimal or decimal form when you use the ASSIGN command in the DRAMREC. The # character must precede allhexadecimal entries. For example, #1F

Note 2: Phrase time is in seconds

Note 3: Use phrase names exactly as the names appear

NT1X76BF (continued)

NT1X76BF Speech memory contents for virtual card 0 (Sheet 3 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
1F	31	2.592	AVRF62	Il n'y a plus d'abonne a ce numero.
20	32	2.112	AVRF63	mais vous pouvez joindre l'abonne au
31	49		AVRF64	huit-cent
34	52		AVRF65	un

Note 1: Phrase ID is in hexadecimal or decimal form when you use the ASSIGN command in the DRAMREC. The # character must precede allhexadecimal entries. For example, #1F

Note 2: Phrase time is in seconds

Note 3: Use phrase names exactly as the names appear

NT1X76BF Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID[1]hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s of silence
1	1	0.160		test tone 760 Hz at -13 dbm
2	2	0.992		prompt tone
3	3	0.512		0.5 s of silence
4	4	5.344	AVRF02	a ete remplace par un numero confidentiel. Il ne figure pas dans nos listes.
5	5	3.800	AVRF04	a change d'adresse. Mais, la ligne n'est pas encore en service.
6	6	6.304	AVRF17	Ce numero a ete remplace par un numero confidentiel. Il ne figure pas dans nos listes.
7	7	4.192	AVRF31	L'abonne a change d'adresse. Il n'y a plus d'abonne au

Note 1: Phrase ID is in hexadecimal or decimal form when you use the ASSIGN command in the DRAMREC. The # character must precede all hexadecimal entries. For example, #1F

Note 2: Phrase time is in seconds

Note 3: Use phrase names exactly as the names appear

NT1X76BF Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
8	8	4.640	AVRF33	L'abonne a change d'adresse. Mais la ligne n'est pas encore en service.
9	9	1.184	AVRF39	le numero
A	10	2.432	AVRF44	les appels n'y sont plus gratuits
B	11	4.672>	AVRF45	Les appels n'y sont plus gratuits. Mais, vous pouvez appeler a frais vires.
C	12	4.896	AVRF47	Nous procedons a des essais sur la ligne. Veuillez rappeler plus tard.
D	13	2.144	AVRF50	Veuillez rappeler plus tard.
E	14	5.952	AVRF54	A la demande de l'abonne, le numero est confidentiel. Il ne figure pas dans nos listes.
F	15	3.136	AVRF55	a la demande de l'abonne, le service au
10	16	5.152	AVRF56	a la demande de l'abonne, le service est suspendu a ce numero
11	17	2.048	AVRF59	il n'y a plus d'abonne au
12	18	1.856	AVRF61	il n'y a pas d'abonne au

Note 1: Phrase ID is in hexadecimal or decimal form when you use the ASSIGN command in the DRAMREC. The # character must precede all hexadecimal entries. For example, #1F

Note 2: Phrase time is in seconds

Note 3: Use phrase names exactly as the names appear

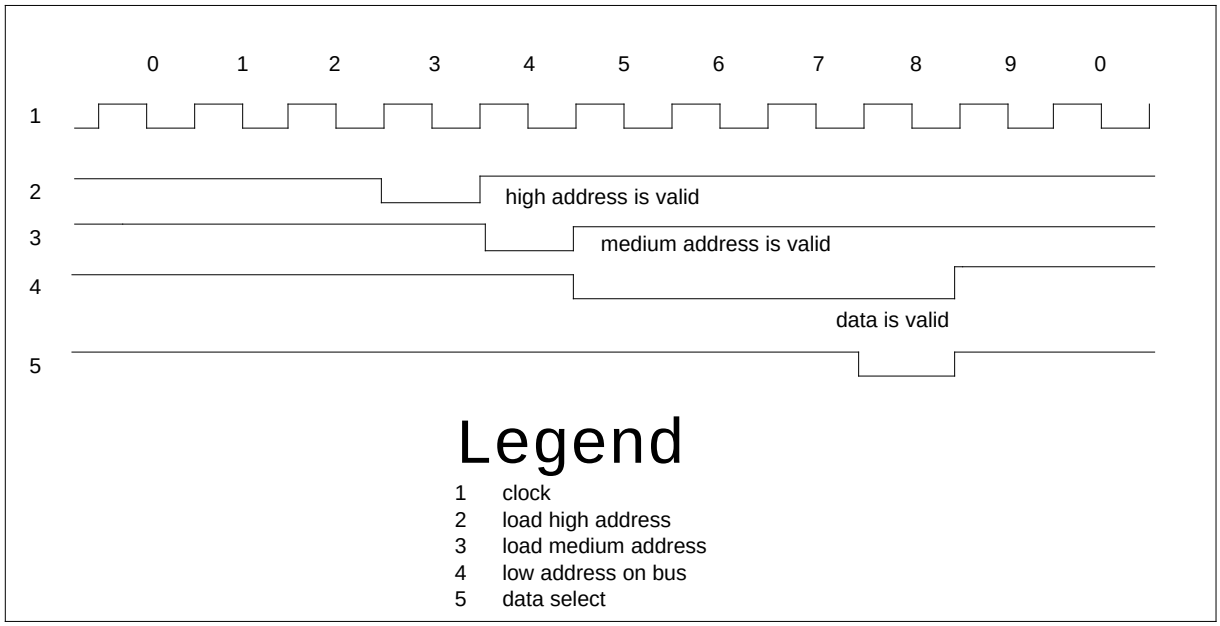
Signaling

Timing

The timing of the NT1X76BF appears in the following figure.

NT1X76BF (end)

NT1X76BF timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76BF appear in the following table.

NT1X76BF ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30°C	5 to 49°C
Relative humidity	20% to 55%	20% to 80%

NT1X76BG

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76BG digital recorded announcement PROM auxiliary operator service system voice response French card 2.

The NT1X76BG, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BG has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BG multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The bus contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address is within the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses function as chip enables. The data strobe from the processor also activates the data.

NT1X76BG (continued)

Speech memory contents

The phrase IDs and content associated with the NT1X76BG card appear in the following two tables. The content can be silences, phrases and tones. The two virtual cards in the NT1X76BG are virtual card 0 and virtual card 1.

NT1X76BG Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s of silence
1	1	0.160		test tone 760 Hz at -13dbm
2	2	0.992		prompt tone
3	3	0.512		0.5 s of silence
4	4	1.920	AVRF01	a ete remplace par le
5	5	1.344	AVRF05	au lieu du
6	6	1.504	AVRF10	n'est pas en service
7	7	1.856	AVRF11	n'est pas encore en service
8	8	3.200	AVRF16	ce numero a ete remplace par le
9	9	2.400	AVRF19	ce numero n'est pas en service
A	10	1.856	AVRF30	je regrette
B	11	1.184	AVRF34	l'abonne du
C	12	0.896	AVRF35	la ligne
D	13	2.496	AVRF38	la ligne n'est pas encore en service
E	14	1.216	AVRF42	le service au
F	15	2.560	AVRF43	le service est suspendu a ce numero
10	16	2.656	AVRF46	nous procedons a des essais sur la ligne
11	17	2.208	AVRF48	on ne peut recevoir d'appels au

Note 1: Phrase ID is in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must precede all hexadecimal entries. For example, #1F.

Note 2: Phrase time is in seconds.

Note 3: Use hrase names exactly as the names appear.

NT1X76BG Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
12	18	5.888	AVRF49	si vous desirez de l'aide, ne quittez pas. Un telephoniste vous repondra.
13	19	1.728	AVRF51	vous avez obtenu le
14	20	2.720	AVRF52	vous devez temporairement appeler le
15	21	3.328	AVRF57	a ce numero, on ne peut recevoir d'appels

Note 1: Phrase ID is in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must precede all hexadecimal entries. For example, #1F.

Note 2: Phrase time is in seconds.

Note 3: Use hrase names exactly as the names appear.

NT1X76BG Speech memory contents for virtual card 1 (Sheet 1 of 4)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s of silence
1	1	0.160		test tone 760 Hz at -13dbm
2	2	0.992		prompt tone
3	3	0.512		0.5 s of silence
4	4	1	FHIRI0	zero (high rising intonation)
5	5	1	FHIRI1	un
6	6	1	FHIRI2	deux
7	7	1	FHIRI3	trois
8	8	1	FHIRI4	quatre
9	9	1	FHIRI5	cinq

Note 1: Phrase ID is in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must precede all hexadecimal entries. For example, #1F.

Note 2: Phrase time is in seconds.

Note 3: Use phrase names exactly as the names appear.

NT1X76BG (continued)

NT1X76BG Speech memory contents for virtual card 1 (Sheet 2 of 4)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
A	10	1	FHIRI6	six
B	11	1	FHIRI7	sept
C	12	1	FHIRI8	huit
D	13	1	FHIRI9	neuf
E	14	1	FLORI0	zero (low rising intonation)
F	15	1	FLORI1	un
10	16	1	FLORI2	deux
11	17	1	FLORI3	trois
12	18	1	FLORI4	quatre
13	19	1	FLORI5	cinq
14	20	1	FLORI6	six
15	21	1	FLORI7	sept
16	22	1	FLORI8	huit
17	23	1	FLORI9	neuf
18	24	1	FWAVE0	zero (falling, rising intonation)
19	25	1	FWAVE1	un
1A	26	1	FWAVE2	deux
1B	27	1	FWAVE3	trois
1C	28	1	FWAVE4	quatre
1D	29	1	FWAVE5	cinq
1E	30	1	FWAVE6	six

Note 1: Phrase ID is in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must precede all hexadecimal entries. For example, #1F.

Note 2: Phrase time is in seconds.

Note 3: Use phrase names exactly as the names appear.

NT1X76BG Speech memory contents for virtual card 1 (Sheet 3 of 4)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
1F	31	1	FWAVE7	sept
20	32	1	FWAVE8	huit
21	33	1	FWAVE9	neuf
22	34	1	FFALL0	zero (falling intonation)
23	35	1	FFALL1	un
24	36	1	FFALL2	deux
25	37	1	FFALL3	trois
26	38	1	FFALL4	quatre
27	39	1	FFALL5	cinq
28	40	1	FFALL6	six
29	41	1	FFALL7	sept
2A	42	1	FFALL8	huit
2B	43	1	FFALL9	neuf
2C	44	1	FFLTB0	zero (flat B intonation)
2D	45	1	FFLTB1	un
2E	46	1	FFLTB2	deux
2F	47	1	FFLTB3	trois
30	48	1	FFLTB4	quatre
31	49	1	FFLTB5	cinq
32	50	1	FFLTB6	six
33	51	1	FFLTB7	sept

Note 1: Phrase ID is in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must precede all hexadecimal entries. For example, #1F.

Note 2: Phrase time is in seconds.

Note 3: Use phrase names exactly as the names appear.

NT1X76BG (continued)

NT1X76BG Speech memory contents for virtual card 1 (Sheet 4 of 4)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
34	52	1	FFLTB8	huit
35	53	1	FFLTB9	neuf
36	54	2.464	AVRF60	Il n'ya pas d'abonne a ce numero

Note 1: Phrase ID is in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must precede all hexadecimal entries. For example, #1F.

Note 2: Phrase time is in seconds.

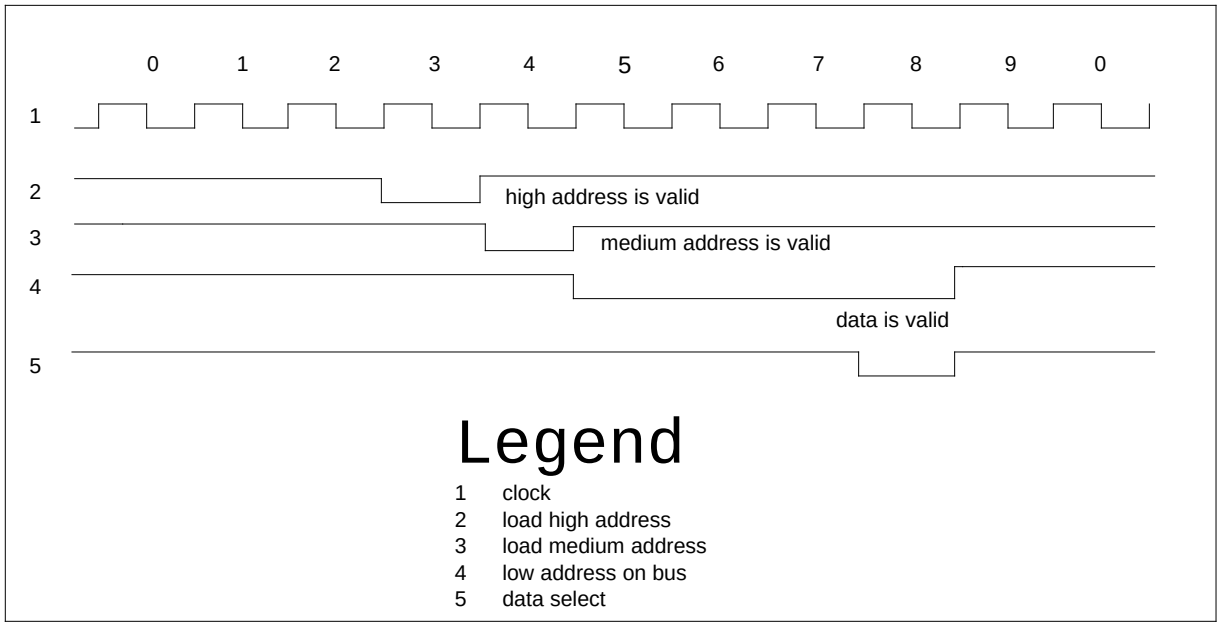
Note 3: Use phrase names exactly as the names appear.

Signaling

Timing

The timing of the NT1X76BG appears in the following figure.

NT1X76BG timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76BG appear in the following table.

NT1X76BG ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76BH

Product description

Digital recorded announcement (DRA) hardware consists of a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76BH digital recorded announcement PROM automatic calling card service French card.

The NT1X76BH is a double density card that has 256 Kbytes like two virtual cards. This card occupies one slot in the maintenance trunk module (MTM). The NT1X76BH has a three-position single-pole double-throw dual inline package (DIP) switch that you set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76BH multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The low address is on the bus by default.

A decoder EPROM QM27128 allows address decoding, chip enables and write enables. The EPROM provides a card enable signal that enables the data buffer and the row decoder. The enable occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. The column addresses enable the outputs of the memory devices and the row addresses operate like chip enables. The processor sends the data strobe that can enable the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76BH card appear in the following two tables. The content can be silences, phrases and tones. The two virtual cards contained in the NT1X76BH are virtual card 0 and virtual card 1.

NT1X76BH Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s of silence
1	1	0.160		test tone 750 Hz
2	2	0.992		prompt tone
3	3	0.256	ACCSPAUSE	0.25 s of silence
4	4	1.216	ACCSTONE	
5	5	5.504	ACCSFRE2	Le numero de carte d'appel recu n'est pas valide. Veuillez entrer a nouveau votre numero de carte.
6	6	7.168	ACCSFRE1	Veuillez entrer votre numero de carte d'appel ou faire le zero pour joindre le telephoniste. C'etait un message enregistre.
7	7	4.928	ACCSFRE9	Veuillez raccrocher, puis faire le zero et composer le numero que vous voulez joindre.
8	8	7.808	ACCSFRE4	Le numero de carte d'appel recu n'est pas valide. Veuillez raccrocher, puis faire le zero et composer le numero que vous voulez joindre.
9	9	8.000	ACCSFRE8	Le numero que vous avez compose est inexact. Veuillez raccrocher, puis faire le zero et composer le numero que vous voulez joindre.

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must come before all hexadecimal entries (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: You must use the phrase names for flat B intonations like FRE0 exactly as the words appear. You can change other phrase names.

NT1X76BH (continued)

NT1X76BH Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
A	10	6.240	ACCSFRE6	Le numero que vous avez compose est inexact. Veuillez composer a nouveau le numero que vous voulez joindre.
B	11	8.256	ACCSFRE15	Des difficultes techniques nous empechent pour l'instant d'acheminer votre appel. Veuillez composer de nouveau. C'etait un message enregistre.

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must come before all hexadecimal entries (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: You must use the phrase names for flat B intonations like FRE0 exactly as the words appear. You can change other phrase names.

NT1X76BH Speech memory contents for virtual card 1 (Sheet 1 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
0	0	1.024		1 s of silence
1	1	0.160		test tone 750 Hz
2	2	0.992		prompt tone
3	3	0.256	ACCSPAUSE	0.25 s of silence
4	4	1.216	ACCSTONE	
5	5	2.496	ACCSFRE3	Veuillez entrer votre numero de carte d'appel.
6	6	2.752	ACCSFRE7	Veuillez composer le numero que vous voulez joindre.
7	7	0.544	ACCSFRE16	merci

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must come before all hexadecimal entries (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: You must use the phrase names for flat B intonations like FRE0 exactly as the words appear. You can change other phrase names.

NT1X76BH Speech memory contents for virtual card 1 (Sheet 2 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
8	8	1.440	ACCSFRE13	numero non valide
9	9	2.112	ACCSFRE5	Vous pouvez maintenant faire un autre appel.
A	10	4.992	ACCSFRE12	numero valide, NIP autorise, BRC non disponible
B	11	4.160	ACCSFRE10	numero valide, NIP autorise, BRC: xxx.
C	12	4.416	ACCSFRE12	numero valide, NIP autorise, BRC non disponible
D	13	0.640	CFRR0>	zero (rising inflection)
E	14	0.544	CFRR1	un
F	15	0.608	CFRR2	deux
10	16	0.608	CFRR3	trois
11	17	0.640	CFRR4	quatre
12	18	0.704	CFRR5	cinq
13	19	0.640	CFRR6	six
14	20	0.672	CFRR7	sept
15	21	0.640	CFRR8	huit
16	22	0.640	CFRR9	neuf
17	23	0.608	FRE0	zero (flat B intonation)
18	24	0.736	FRE1	un
19	25	0.704	FRE2	deux
1A	26	0.704	FRE3	trois

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must come before all hexadecimal entries (for example, #1F).

Note 2: Phrase time is in seconds.

Note 3: You must use the phrase names for flat B intonations like FRE0 exactly as the words appear. You can change other phrase names.

NT1X76BH (continued)

NT1X76BH Speech memory contents for virtual card 1 (Sheet 3 of 3)

Phrase ID[1] hexadecimal	Phrase ID decimal	Time[2]	Name[3]	Announcement
1B	27	0.768	FRE4	quatre
1C	28	0.704	FRE5	cinq
1D	29	0.704	FRE6	six
1E	30	0.736	FRE7	sept
1F	31	0.736	FRE8	huit
20	32	0.704	FRE9	neuf
21	33	0.640	CFRF0	zero (falling intonation)
22	34	0.576	CFRF1	un
23	35	0.608	CFRF2	deux
24	36	0.640	CFRF3	trois
25	37	0.704	CFRF4	quatre
26	38	0.768	CFRF5	cinq
27	39	0.704	CFRF6	six
28	40	0.672	CFRF7	sept
29	41	0.672	CFRF8	huit
2A	42	0.672	CFRF9	neuf

Note 1: Phrase ID can be in hexadecimal or decimal when you use the ASSIGN command in DRAMREC. The # character must come before all hexadecimal entries (for example, #1F).

Note 2: Phrase time is in seconds.

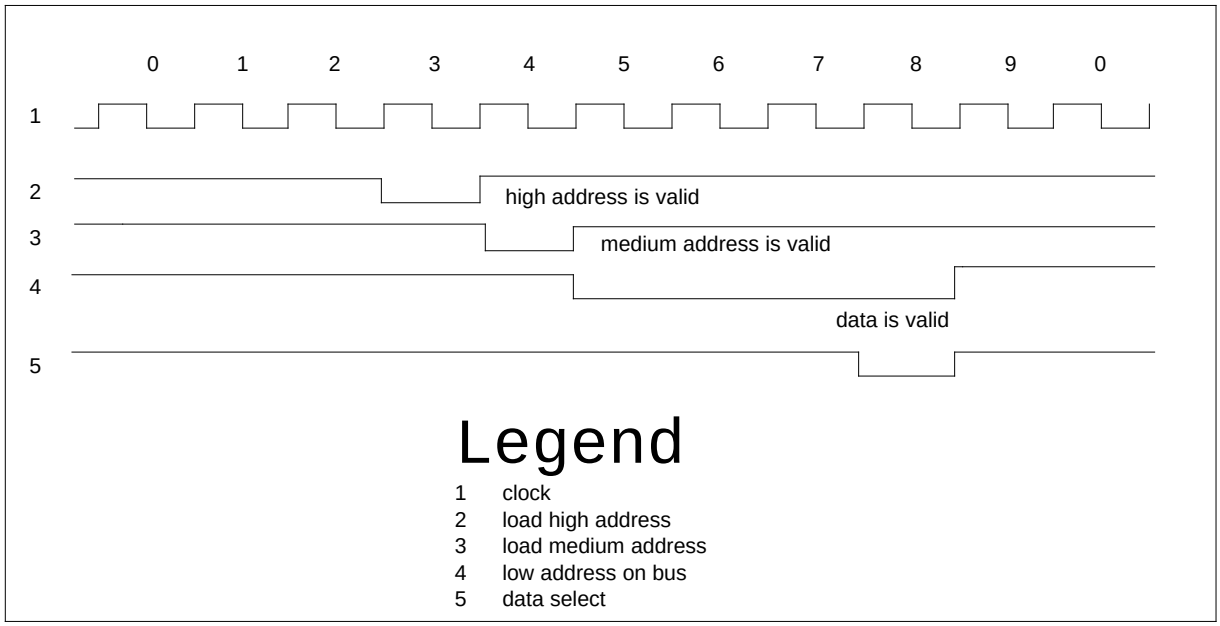
Note 3: You must use the phrase names for flat B intonations like FRE0 exactly as the words appear. You can change other phrase names.

Signaling

Timing

The timing of the NT1X76BH appears in the following figure.

NT1X76BH timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76BH appear in the following table.

NT1X76BH ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 °C	5 to 49 °C
Relative humidity	20% to 55%	20% to 80%

NT1X76BJ

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76BJ is a double density card that has 256 Kbytes like two virtual cards that occupies one slot in the maintenance trunk module (MTM). The NT1X76BJ has a three-position single-pole double-throw dual inline package (DIP) switch, which must be set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76BJ multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 allows address decoding, chip enables and write enables. The EPROM provides a card enable signal that enables the data buffer and the row decoder. The enable occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. The column addresses enable the outputs of the memory devices and the row addresses operate like chip enables. The processor sends the data strobe that can enable the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76BJ CMS/CLASS phase I and II French announcements speech ROM card appear in the following two tables. The content can be silences, phrases and tones. The two

virtual cards contained in the NT1X76BJ are referred to as virtual card 0 and virtual card 1.

NT1X76BJ Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	one second silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	1/4 second silence
004	1.152	1.824	Veuillez raccrocher.
005	3.616	4.160	Il est impossible d'obtenir le numédu dernier demandeur.
006	3.744	4.288	Vous ne pouvez pas composer ce numéau moyen de cette fonction.
007	2.688	3.232	Vous avez annulétoutes vos demandes de rappel.
008	3.168		Le dernier appel que vous avez reçu a été retracé.
	4.160	8.448	Si vous désirez faire d'autres démarches, communiquez avec la police.

Note: Total duration includes silence blocks added at the beginning or end.

NT1X76BJ (continued)

NT1X76BJ Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
009	3.680		Le dernier appel que vous avez reçu ne peut pas être retracé.
	4.320	9.120	Pour obtenir d'autres instructions, consultez les pages liminaires de l'annuaire.
Note: Total duration includes silence blocks added at the beginning or end.			

NT1X76BJ Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	one second silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	1/4 second silence
004	5.536	6.208	Une sonnerie spéciale vous avertira dès qu'elle sera libre. Veuillez raccrocher.
005	4.544	5.152	Vous ne pouvez pas composer actuellement ce numéro au moyen de cette fonction.
006	0.544	1.088	(Busy Tone)
Note: Total duration includes silence blocks added at the beginning or end.			

NT1X76BJ Speech memory contents for virtual card 1 (Sheet 2 of 2)

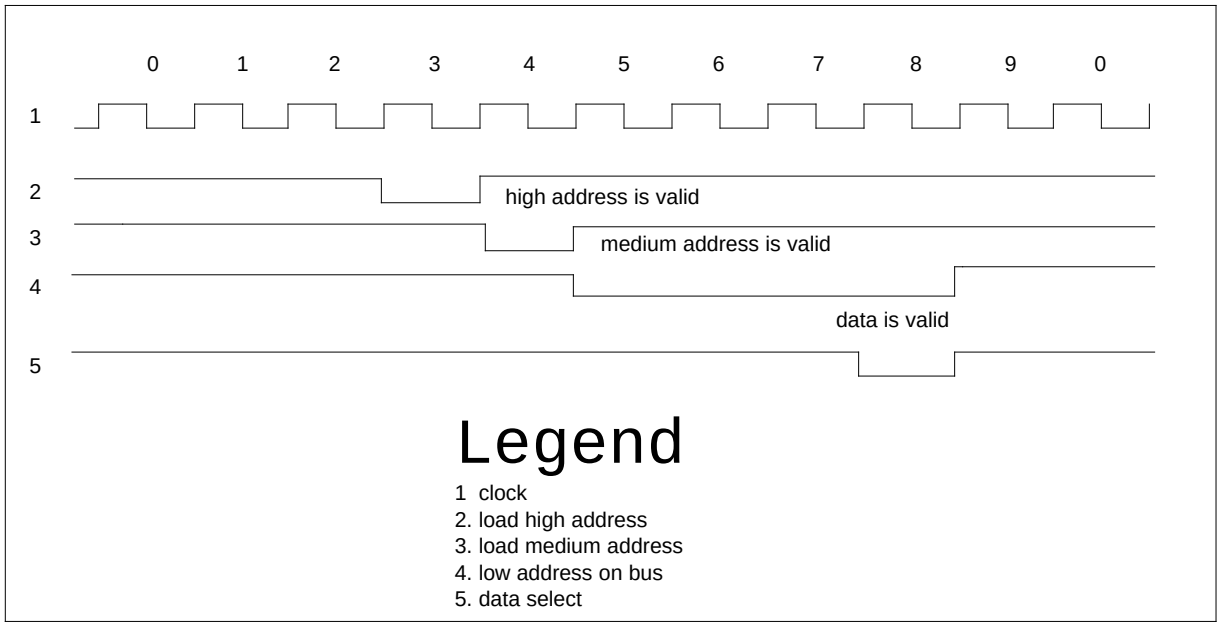
Phrase ID	Duration seconds	Total duration seconds	Content
007	2.688	3.360	Raccrochez et essayez de nouveau plus tard.
008	1.312	1.984	La ligne est occupée.
009	1.824	2.432	La ligne est de nouveau occupée.
00A	4.928	5.600	Raccrochez et essayez de nouveau plus tard, ou composez le numéro vous-même.
Note: Total duration includes silence blocks added at the beginning or end.			

Signaling

Timing

The timing of the NT1X76BJ appears in the following figure.

NT1X76BJ timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BK

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76BK is a double density card that has 256 Kbytes like two virtual cards and occupies one slot in the maintenance trunk module (MTM). The NT1X76BK has a three-position single-pole double-throw dual inline package (DIP) switch, that you must set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76BK multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 allows address decoding, chip enables and write enables. The EPROM provides a card enable signal that enables the data buffer and the row decoder. The enable occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. While the column addresses enable the outputs of the memory devices, the row addresses operate like chip enables. The processer sends a data strobe that can enable the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76BK CMS/CLASS phase I and II French announcements speech ROM card appear in the following two tables. The content can be silences, phrases and tones. The two virtual cards contained in the NT1X76BK are virtual card 0 and virtual card 1.

NT1X76BK Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	one second silence
001			Test tone
Note: Total duration includes silence blocks added at the beginning or end.			

NT1X76BK Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	1/4 second silence
004	3.648	4.928	Pour le composer, faites le "un"; sinon raccrochez.
005	2.688	3.360	Raccrochez et composez le numéro vous-même.
006	2.688	3.168	Le numéro de dernier demandeur est le ...
007	3.296	3.360	Le numéro de dernier demandeur est confidentiel.
008	3.616	4.160	Vous ne pouvez pas composer ce numéro au moyen de cette fonction.

Note: Total duration includes silence blocks added at the beginning or end.

NT1X76BK Speech memory contents for virtual card 1 (Sheet 1 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	one second silence
001			Test tone

Note: Total duration includes silence blocks added at the beginning or end.

NT1X76BK (continued)

NT1X76BK Speech memory contents for virtual card 1 (Sheet 2 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	1/4 second silence
004			0 (High rise intonation)
005			1
006			2
007			3
008			4
009			5
00A			6
00B			7
00C			8
00D			9
00E			0 (Low rise intonation)
00F			1
010			2

Note: Total duration includes silence blocks added at the beginning or end.

NT1X76BK Speech memory contents for virtual card 1 (Sheet 3 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
011			3
012			4
013			5
014			6
015			7
016			8
017			9
018			0 (Fall rise intonation)
019			1
01A			2
01B			3
01C			4
01D			5
01E			6
01F			7
020			8
021			9
022			0 (Falling intonation)
023			1
024			2
025			3
026			4
027			5

Note: Total duration includes silence blocks added at the beginning or end.

NT1X76BK (continued)

NT1X76BK Speech memory contents for virtual card 1 (Sheet 4 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
028			6
029			7
02A			8
02B			9
02C			0 (Level or flat intonation)
02D			1
02E			2
02F			3
030			4
031			5
032			6
033			7
034			8
035			9

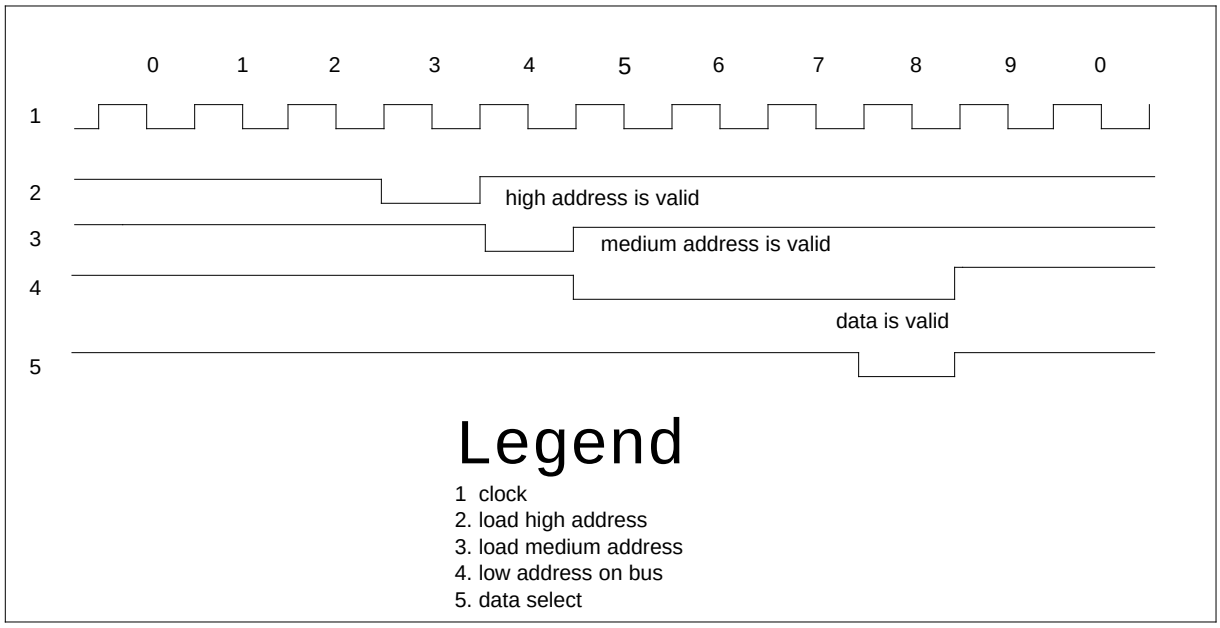
Note: Total duration includes silence blocks added at the beginning or end.

Signaling

Timing

The timing of the NT1X76BK appears in the following figure.

NT1X76BK timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BP

Product description

Digital recorded announcement (DRA) hardware consists of a speech processor, a microprocessor controller and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76BP is a double density card that has 256 Kbytes like two virtual cards). This card occupies one slot in the maintenance trunk module (MTM). The NT1X76BP has a three-position single-pole double-throw dual inline package (DIP) switch, which you must set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76BP multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch and the medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 allows address decoding, chip enables and write enables. The EPROM provides a card enable signal that enables the data buffer and the row decoder. The enable occurs when the decoded address is within the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. While the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The processor sends the data strobe that can enable the data.

Speech memory contents

The phrase IDs and content appear in the following two tables. This IDs and content associate with the NT1X76BP CMS/CLASS phase I and II French announcements speech ROM card. The content can be silences, phrases and

tones. The two virtual cards contained in the NT1X76BP are referred to as virtual card 0 and virtual card 1.

NT1X76BP Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	one second silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	1/4 second silence
004	4.448		Composez le numéro â supprimer et appuyez de nouveau sur l'étoile.
	6.560		Pour supprimer tous les numéros, faites 0, 8 et appuyez de nouveau sur l'étoile.
	7.328		Pour supprimer les numéros confidentiels seulement, faites 0, 9 et appuyez de nouveau sur l'étoile.
	3.456		Pour écouter de nouveau les instructions, faites le 0.
	1.344	26.112	Veuillez faire votre choix.

Note: Total duration includes silence blocks added at the beginning or end.

NT1X76BP (continued)

NT1X76BP Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	one second silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	1/4 second silence
004	1.888		Composez le numéro à supprimer. Pour supprimer tous les numéros, faites 0, 8. Pour supprimer les numéros confidentiels seulement, faites 0, 9. Pour écouter de nouveau les instructions, faites le 0. Veuillez faire votre choix.

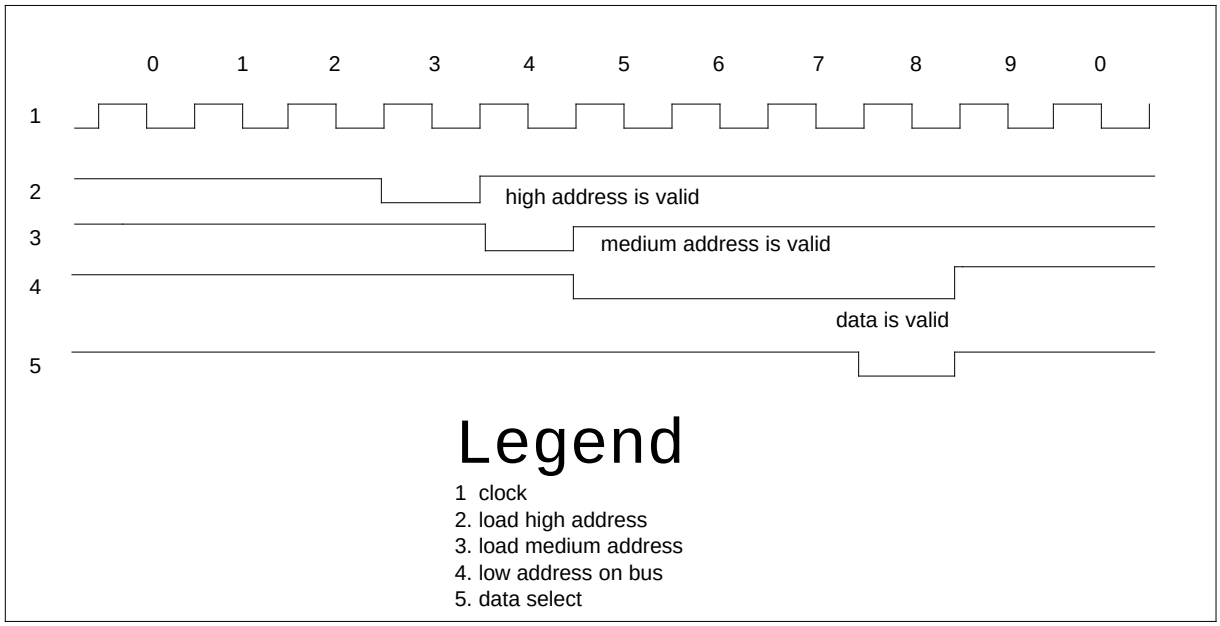
Note: Total duration includes silence blocks added at the beginning or end.

Signaling

Timing

The timing of the NT1X76BP.

NT1X76BP timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BQ

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent memory.

The NT1X76BQ, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BQ has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BQ multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The busy contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses function as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76BQ CMS/CLASS phase I and II French announcements speech ROM card appear in the

following two tables. The content can be silences, phrases, and tones. The two virtual cards in the NT1X76BQ are virtual card 0 and virtual card 1.

NT1X76BQ Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	4.832	5.504	Recommencez, faites le 0 pour obtenir des instructions ou raccrochez.
005	2.720	3.264	Le numéro que vous avez composé est incorrect.
006	1.728	2.400	Cette commande est incorrecte.
007	3.136	3.712	Le numéro à supprimer ne figure pas dans votre liste.

Note: Total duration includes silence blocks added at the beginning or end.

NT1X76BQ (continued)

NT1X76BQ Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	3.840	4.416	Pour activer cette fonction, ajoutez un numéro à votre liste.
005	2.592		Pour refuser les appels du dernier demandeur, appuyez sur le carré, faites 0, 1 et appuyez de nouveau sur le carré.
	5.536	9.248	
006	2.592		Pour refuser les appels du dernier demandeur, faites 1, 2 puis 0, 1.
	4.032	7.808	
007	2.464	3.136	Pour l'ajouter, appuyez sur le carré.
008	2.336	3.008	Pour l'ajouter, faites 1, 2.

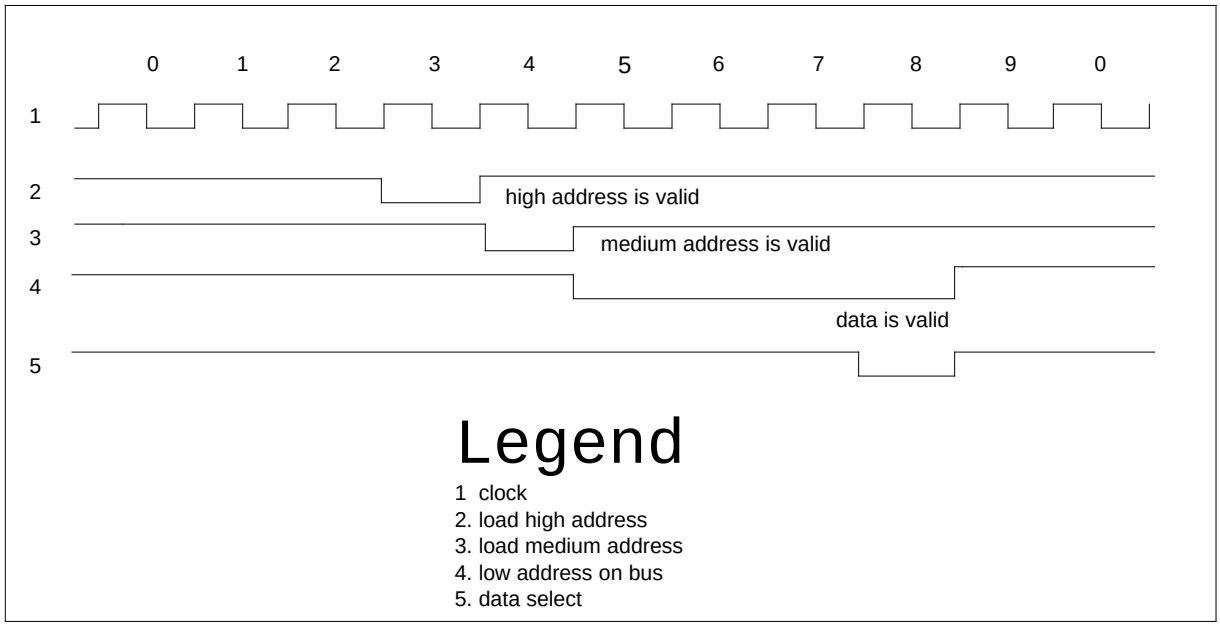
Note: Total duration includes silence blocks added at the beginning or end.

Signaling

Timing

The following diagram displays the timing of the NT1X766BQ.

NT1X76BQ timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BR

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent memory.

The NT1X76BR, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BR has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BR multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The busy contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses function as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76BR CMS/CLASS phase I and II French announcements speech ROM card appear in the

following two tables. The content can be silences, phrases, and tones. The two virtual cards in the are virtual card 0 and virtual card 1.

NT1X76BR Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	4.096		Composez le numéro à ajouter et appuyez de nouveau sur pour ajouter le numéro du dernier demandeur, faites 0, 1 et appuyez de nouveau sur le carré veuillez faire votre choix.
	7.008	14.722	
	1.344		

Note: Total duration includes silence blocks added at the beginning or end.

NT1X76BR Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone

Note: Total duration includes silence blocks added at the start or end.

NT1X76BR (continued)

NT1X76BR Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	2.016		Composez le numéro à ajouter.
	4.384	9.568	Pour ajouter le numéro du dernier demandeur, faiter 0, 1 veuillez faire votre choix.
	1.344		

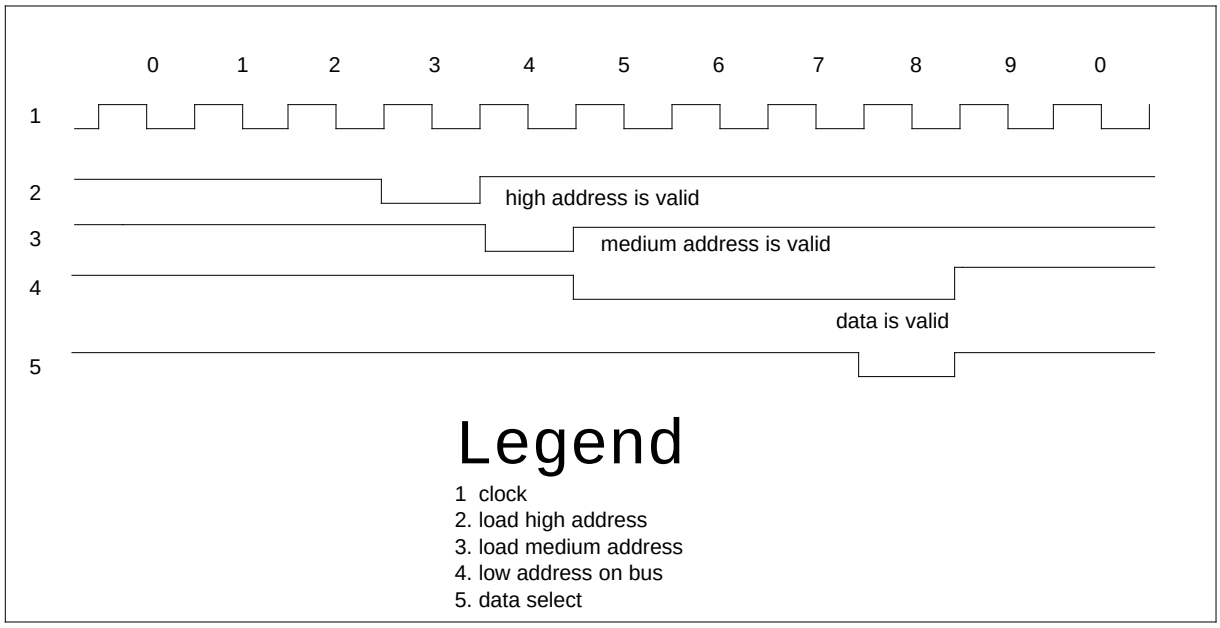
Note: Total duration includes silence blocks added at the start or end.

Signaling

Timing

The timing of the NT1X76BR appears in the following figure.

NT1X76BR timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BS

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent memory.

The NT1X76BS, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BS has a three-position, single-pole, double-throw, dual inline package (DIP) switch. You must set the DIP switch to the number assigned on the card. This number is the BLOCKLIST value in field CARDINFO of Table DRAMS in the digital switching system.

Functional description

The NT1X76BS multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The bus contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies activates the data buffer and the row decoder. This event occurs when decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content appear in the following two tables. The IDs and content associate with the NT1X76BS CMS/CLASS phase I and II French announcements speech ROM card The two virtual cards in the NT1X76BS are virtual card 0 and virtual card 1.

NT1X76BS Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
Note: Total duration includes silence blocks added at the start or end.			

NT1X76BS Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	3.584	4.320	Recommencez ou faites le 0 pour obtenir des instructions.
005	2.976	3.520	Vous avez composé un nombre insuffisant de chiffres.
006	2.880	3.456	Vous avez composé un trop grand nombre de chiffres.
007	3.136	3.744	Le numéro du dernier demandeur n'est pas accessible.
008	3.744	4.352	Le systeme ne peut pas accepter le numéro que vous avez composé.
009	5.088	5.696	Après avoir appuyé sur le carré ou l'étoile, composez un numéro de téléphone.
00A	5.504	6.048	Après avoir faite 1, 2 ou 1, 1, composez un numéro de téléphone.
00B	3.072	3.680	Vous venez de supprimer les chiffres que vous avez composés.
00C	0.352	0.352	(Prompt tone)

Note: Total duration includes silence blocks added at the start or end.

NT1X76BS (continued)

NT1X76BS Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	2.560		Pour activer cette fonction, faites le 3.
	2.880		Pour ajouter un numéro, appuyez sur le carré.
	4.064		Pour supprimer un ou plusieurs numéros, appuyez sur l'étoile.
	3.968		Pour écouter les numéros qui figurent dans votre liste, faites le 1.
	3.456		Pour écouter de nouveau les instructions, faites le 0.
	1.344	21.888	Veuillez faire votre choix.
005	3.040		Pour désactiver cette fonction, faites le 3.
	2.880		Pour ajouter un numéro appuyez sur le carré.
	4.064		Pour supprimer un ou plusieurs numéros, appuyez sur l'étoile.

Note: Total duration includes silence blocks added at the start or end.

NT1X76BS Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
	3.968		Pour &0xe9couter;les num&0xe9ros;qui figurent dans votre liste, faites le 1.
	3.456		Veuillez faire votre choix.
	1.344	22.368	Pour écouter de nouveau les instructions, faites le 0.
006	2.560		Pour activer cette fonction, faites le 3.
	2.784		Pour ajouter un numéro faites 1, 2.
	4.128		Pour supprimer un ou plusieurs numéros faites 1, 1.
	3.968		Pour écouter les numéros qui figurent dans votre liste, faites le 1.
	3.456		Pour écouter de nouveau les instructions, faites le 0.
	1.344	21.856	Veuillez faire votre choix.
007	3.040		Pour désactiver cette fonction, faites le 3.
	2.784		Pour ajouter un numéro faites 1, 2.
	4.128		Pour supprimer un ou plusieurs numéros, faites 1, 1.
	3.968		Pour écouter les numéros qui figurent dans votre liste, faites le 1.
	3.456		Pour écouter de nouveau les instructions, faites le 0.
	1.344	22.336	Veuillez faire votre choix.

Note: Total duration includes silence blocks added at the start or end.

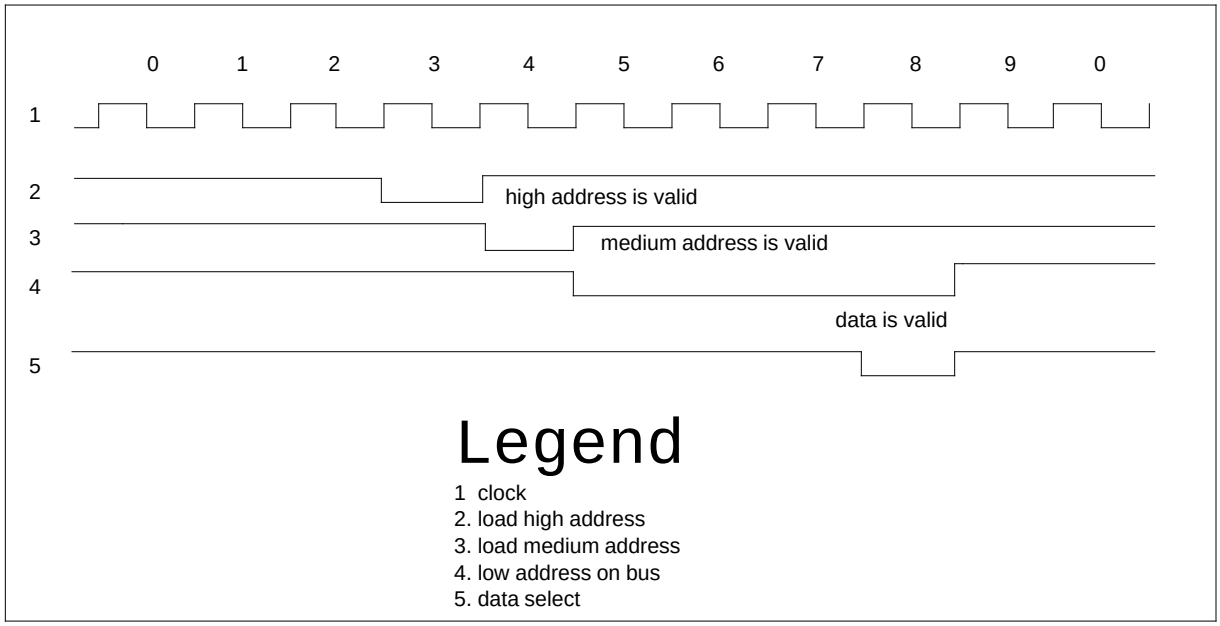
Signaling

Timing

The timing of the NT1X76BS appears in the following figure.

NT1X76BS (end)

NT1X76BS timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BT

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent memory.

The NT1X76BT, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BT has a three-position, single-pole, double-throw, dual inline package (DIP) switch. You must set the DIP switch to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BT multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The bus contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appear in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content appear in the following two tables. The IDs and content associate with the NT1X76BT CMS/CLASS phase I and II French announcements speech ROM card. The content can be silences, phrases, and

NT1X76BT (continued)

tones. The two virtual cards in the NT1X76BT are virtual card 0 and virtual card 1.

NT1X76BT Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		<750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	1.664	2.080	Vous avez ajouté le ...
005	2.816	3.424	Attendez quelques minutes avant d'ajouter le numéro.
006	1.472	1.888	Vous avez supprimé le ...
007	2.528	3.136	Votre liste ne comporte plus aucun numéro.
008	3.488	4.096	Votre liste ne comporte plus aucun numéro confidentiel.
009	1.600	2.272	La liste est terminée.
00A	1.760	2.240	Le premier numéro est le ...
00B	1.824	2.240	Le numéro suivant est le ...

Note: Total duration includes silence blocks added at the start or end.

NT1X76BT Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
00C	4.096	4.704	Ce numéro figure déjà dans votre liste comme numéro confidentiel.
00D	0.832	1.376	Le numéro...
00E	1.728	2.400	Figure déjà dans votre liste.
00F	1.984	2.592	Je répète, le numéro...
Note: Total duration includes silence blocks added at the start or end.			

NT1X76BT Speech memory contents for virtual card 1 (Sheet 1 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004			0 (High rise intonation)
005			1
006			2
Note: Total duration includes silence blocks added at the start or end.			

NT1X76BT (continued)

NT1X76BT Speech memory contents for virtual card 1 (Sheet 2 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
007			3
008			4
009			5
00A			6
00B			7
00C			8
00D			9
00E			0 (Low rise intonation)
00F			1
010			2
011			3
012			4
013			5
014			6
015			7
016			8
017			9
018			0 (Fall rise intonation)
019			1
01A			2
01B			3
01C			4
01D			5

Note: Total duration includes silence blocks added at the start or end.

NT1X76BT Speech memory contents for virtual card 1 (Sheet 3 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
01E			6
01F			7
020			8
021			9
022			0 (Falling intonation)
023			1
024			2
025			3
026			4
027			5
028			6
029			7
02A			8
02B			9
02C			0 (Level or flat intonation)
02D			1
02E			2
02F			3
030			4
031			5
032			6
033			7

Note: Total duration includes silence blocks added at the start or end.

NT1X76BT (end)

NT1X76BT Speech memory contents for virtual card 1 (Sheet 4 of 4)

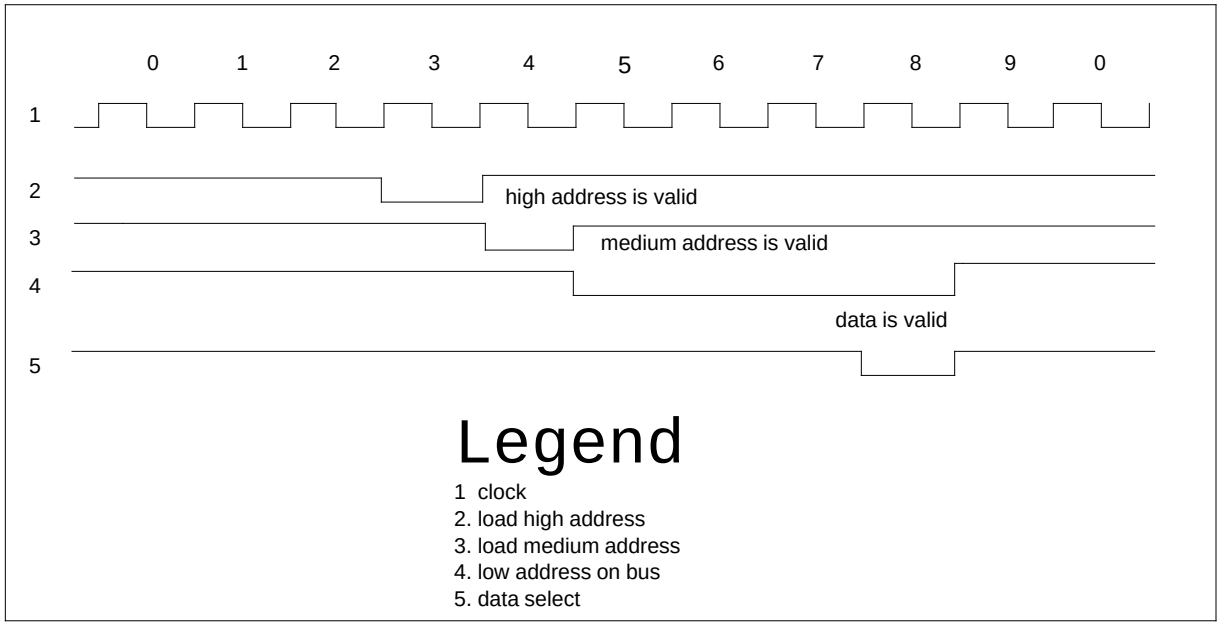
Phrase ID	Duration seconds	Total duration seconds	Content
034			8
035			9
Note: Total duration includes silence blocks added at the start or end.			

Signaling

Timing

The timing of the NT1X76BT appears in the following figure.

NT1X76BT timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BU

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent memory.

The NT1X76BU, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BU has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BU multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The bus contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appear in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76BU CMS/CLASS phase I and II French announcements speech ROM card appear in the

NT1X76BU (continued)

following two tables. The content can be silences, phrases, and tones. The two virtual cards in the NT1X76BU are virtual card 0 and virtual card 1.

NT1X76BU Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	3.168	3.776	Votre liste comporte cinq numéros confidentiels.
005	2.976	3.584	Votre liste comporte deux numéros confidentiels.
006	3.104	3.712	Votre liste comporte huit numéros confidentiels.
007	3.040	3.680	Votre liste comporte neuf numéros confidentiels.
008	3.072	3.680	Votre liste comporte quatre numéros confidentiels.
009	3.104	3.712	Votre liste comporte sept numéros confidentiels.
00A	3.040	3.648	Votre liste comporte six numéros confidentiels.
00B	3.072	3.680	Votre liste comporte trois numéros confidentiels.
00C	3.040	3.648	Votre liste comporte un numéro confidentiel.
00D	4.384	5.056	Activez une autre fonction ou faites le 0 pour obtenir des instructions.

Note: Total duratrion includes silence blocks added at the start or end.

NT1X76BU Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	2.208	2.816	Dont cinq numéros confidentiels.
005	2.080	2.688	Dont deux numéros confidentiels.
006	2.080	2.688	Dont dix numéros confidentiels.
007	2.112	2.720	Dont huit numéros confidentiels.
008	2.080	2.688	Dont neuf numéros confidentiels.
009	2.144	2.752	Dont onze numéros confidentiels.
00A	2.144	2.752	Dont quatre numéros confidentiels.
00B	2.144	2.752	Dont sept numéros confidentiels.
00C	2.176	2.784	Dont six numéros confidentiels.
00D	1.920	2.528	Dont trois numéros confidentiels..
00E	2.016	2.624	Dont un numéro confidentiel.
00F	7.072	7.744	Après chaque numéro, faites 0, 7 si vous désirez le suprimer, et continuez de reviser votre liste.

Note: Total duration includes silence blocks added at the start or end.

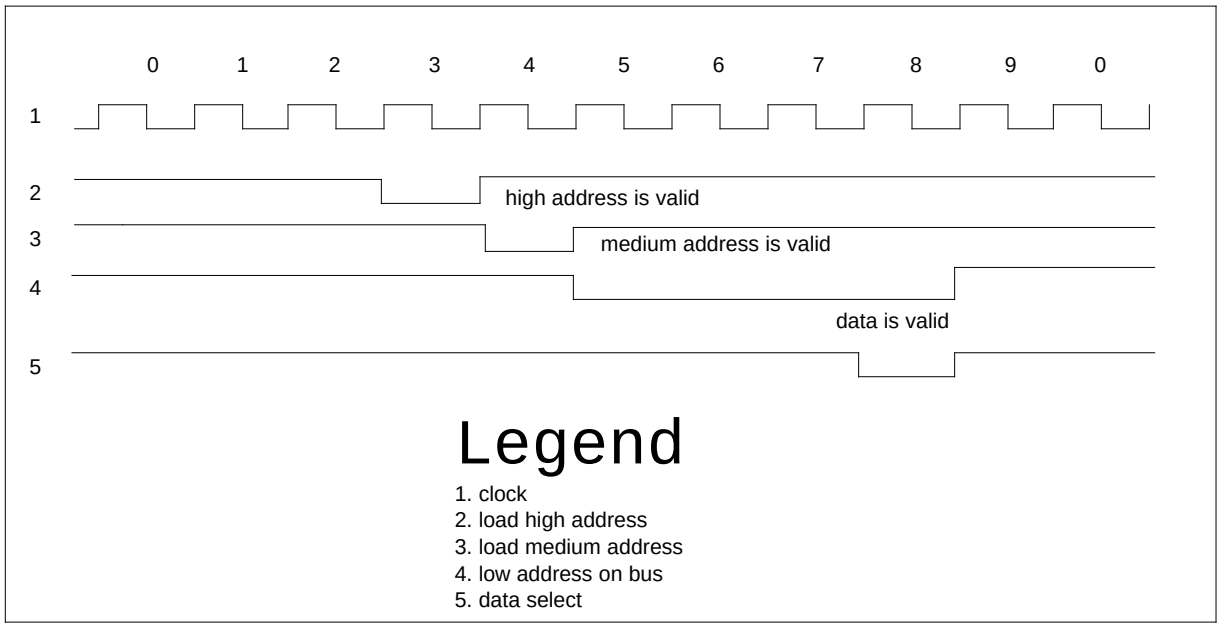
NT1X76BU (end)

Signaling

Timing

The timing of the NT1X76BU appears in the following figure.

NT1X76BU timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BV

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent memory.

The NT1X76BV, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BV has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BV multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The bus contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appear in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76BV CMS/CLASS phase I and II French announcements speech ROM card appear in the

NT1X76BV (continued)

following two tables. The content can be silences, phrases, and tones. The two virtual cards in the NT1X76BV are virtual card 0 and virtual card 1.

NT1X76BV Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
		0.992	
003		0.256	.25 s silence
004	3.168	3.776	Votre liste comporte cinq numéros.
005	2.976	3.584	Votre liste comporte deux numéros.
006	3.104	3.712	Votre liste comporte dix numéros.
007	3.040	3.680	Votre liste comporte douze numéros.
008	3.072	3.680	Votre liste comporte huit numéros.
009	3.104	3.712	Votre liste comporte neuf numéros.
00A	3.040	3.648	Votre liste comporte onze numéros.
00B	3.072	3.680	Votre liste comporte quatre numéros.
00C	3.040	3.648	Votre liste comporte sept numéros.
00D	2.144	2.560	Votre liste comporte six numéros.

Note: Total duration includes silence blocks added at the start or end.

NT1X76BV Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
00E	2.176	2.592	Votre liste comporte trois numéros.
00F	2.176	2.592	Votre liste comporte un numéro.
00D	4.384	5.056	Poursuivez, faites le 0 pour obtenir des instructions ou raccrochez. (Version 2; to be used following a DN)
Note: Total duration includes silence blocks added at the start or end.			

NT1X76BV Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	2.304	2.912	Votre liste comporte cinq numéros.
005	2.112	2.720	Votre liste comporte deux numéros.
006	2.208	2.816	Votre liste comporte dix numéros.
007	2.208	2.816	Votre liste comporte douze numéros.
Note: Total duration includes silence blocks added at the start or end.			

NT1X76BV (continued)

NT1X76BV Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
008	2.208	2.880	Votre liste comporte huit numéros.
009	2.208	2.816	Votre liste comporte neuf numéros.
00A	2.272	2.880	Votre liste comporte onze numéros.
00B	2.208	2.816	Votre liste comporte quatre numéros.
00C	2.336	2.944	Votre liste comporte sept numéros.
00D	2.144	2.752	Votre liste comporte six numéros.
00E	2.272	2.880	Votre liste comporte trois numéros.
00F	2.176	2.784	Votre liste comporte un numéro.

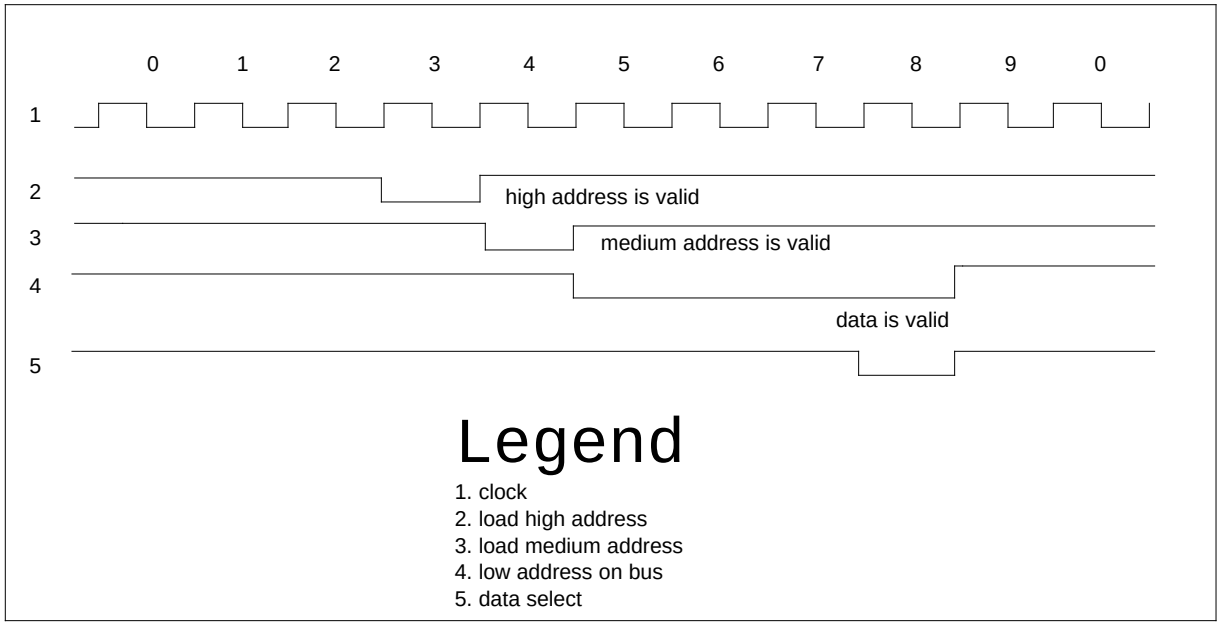
Note: Total duration includes silence blocks added at the start or end.

Signaling

Timing

The timing of the NT1X76BV appears in the following figure.

NT1X76BV timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76BW

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent memory.

The NT1X76BW, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76BW has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76BW multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. Latch the high address in the high address latch. Latch the medium address in the medium address latch. The bus contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal from the EPROM activates the data buffer and the row decoder. This event occurs when the decoded address appear in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe from the processor also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76BW CMS/CLASS phase I and II French announcements speech ROM card appear in the

following two tables. The content can be silences, phrases, and tones. The two virtual cards in the NT1X76BW are virtual card 0 and virtual card 1.

NT1X76BW Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	1.984	2.592	Le sélectif est maintenant activé.
005	2.112	2.720	Le sélectif est maintenant désactivé.
006	4.640	5.312	Poursuivez, faites le 0 pour obtenir des instructions ou raccrochez. (Version 1)
007	5.856	6.528	Pour gagner du temps, vous pouvez composer pendant l'annonce raccrochez dès que vous aurez terminé.
008	2.976	3.584	Le numéro que vous avez ajouté est confidentiel.
009	4.352	4.960	Votre liste est completé. Pour ajouter un numéro supprimez-en un.
00A	2.848	3.392	Vous avez supprimé un numéro confidentiel.
00B	4.800	5.472	Raccrochez, consultez le guide de l'usager et essayez de nouveau plus tard.

Note: Total duration iincludes silence blocks added at the start or end.

NT1X76BW (continued)

NT1X76BW Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	.25 s silence
004	3.232	3.840	Votre liste comporte dix numéros confidentiels.
005	2.112	2.720	Dont douze numéros confidentiels.
006	3.104	3.712	Votre liste comporte douze numéros confidentiels.
007	3.136	3.744	Votre liste comporte onze numéros confidentiels.
008	0.352	0.352	(Prompt tone)
009	3.104	3.776	Raccrochez et essayez de nouveau dans quelques minutes.
00A	2.368	2.976	Votre liste ne comporte aucun numéro.
00B	3.008	3.616	Vous ne pouvez pas accéder à cette fonction actuellement.
00C	2.528	3.200	Votre liste ne comporte plus aucun numéro.

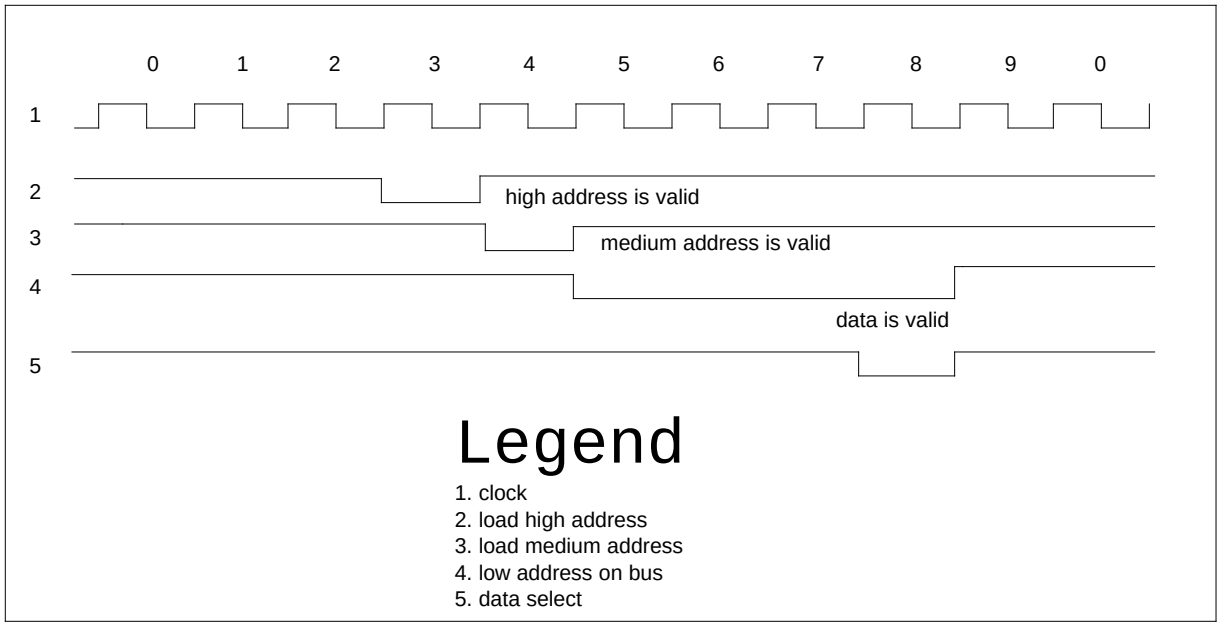
Note: Total duration iincludes silence blocks added at the start or end.

Signaling

Timing

The timing of the NT1X76BW appears in the following figure.

NT1X76BW timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76CA

Product description

Digital recorded announcement (DRA) hardware includes a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76CA EPROM card.

The NT1X76CA is a double density card (256 kbyte-two virtual cards) and occupies one slot in the maintenance trunk module (MTM). The NT1X76CA has a three-position single-pole double-throw dual inline package (DIP) switch. You must set the DIP to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76CA multiplexes addresses because only 8 bits are available on the backplane and the DRA requires 20 bits. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The low address is on the bus by default.

To enable the card, the card select compares A18, A10, and A20 with an onboard dip switch. The A0 is gated to provide for the different addressing mode of the DRA. The DRA requires only 4 bits at a time, but it is more efficient to store 8 bits. The controller hardware requires 8 bits and stores the alternate 4 bits for the next cycle. The card-select circuits only give access if A0 is 0. The data gates the output bus back to the microprocessor during the DS data strobe.

The system decodes addresses A12 to A17 (A13 to A18 for the QM2732D1 version) for the EPROM chip enables. Each EPROM has two enables that you must pull low to allow the data on the outputs. The addressing of the memory array simplifies through the arrangement of eight row enables and eight column enables. Only one of the 64 chips receives both row and column enables at the same time. Only one chip supplies data at any one time.

Speech memory contents

The following two tables present the phrase IDs and content (silences, phrases, and tones) associated with the NT1X76CA card. Virtual card 0 and virtual card 1 refer to the two virtual cards in the NT1X76CA.

NT1X76CA Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
0	0	1.024	-	1 s of silence
1	1	0.160	-	test tone 760 Hz at -13dbm
2	2	0.992	-	prompt tone
3	3	0.512	-	0.5 s of silence
4 to 7	4 to 7	-	-	reserved phrase
8 to 27	8 to 39	-	SIT1 to SIT32	SIT combination 1 (refer to note) to SIT combination 32 (refer to the table on page 4)
28	40	4.320	MCC1	Please dial your card number or zero for an operator now.
29	41	6.016	MCC2	Please dial your card number again now. The card number you have dialed is not valid.
2A	42	2.112	MCC3	Please dial your card number.
2B	43	6.976	MCC4	Please hang up and dial zero plus the number you are calling. The card number you have dialed is not valid.
2C	44	2.176	MCC5	You may dial another call now.
2D	45	5.952	MCC6	Please dial the number you are calling again now. The number you have dialed is not correct.
2E	46	2.336	MCC7	Please dial the number you are calling.

Note 1: Phrase ID can be either hexadecimal or decimal.

Note 2: This name is a suggested phrase name that can change as required.

NT1X76CA (continued)

NT1X76CA Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
2F	47	6.816	MCC8	Please hang up and dial zero plus the number you are calling. The number you have dialed is not correct.
30	48	4.032	MCC9	Please hang up and dial zero plus the number you are calling.
31	49	5.184	MCC10	Valid number unrestricted PIN RAO XXX.
32	50	5.088	MCC11	Valid number restricted PIN, RAO XXX.
33	51	6.176	MCC12	Valid number unrestricted PIN, RAO unavailable.
34	52	3.328	MCC13	Invalid number, please dial again now.
35	53	2.432	MCC14	Invalid number, please hang up.
36	54	5.888	MCC15	Please hang up and dial direct. This number cannot be dialed as a sequence call.
37	55	1.216	ABC tone	Beep and decaying dial tone.

Note 1: Phrase ID can be either hexadecimal or decimal.

Note 2: This name is a suggested phrase name that can change as required.

The following table defines the special information tones, timing and frequencies.

Special Information Tone (SIT) definitions (Sheet 1 of 2)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
8	8	SIT1	1 short	1 short	1 short
9	9	SIT2	1 short	1 short	1 long
A	10	SIT3	1 short	1 long	1 short
B	11	SIT4	1 short	1 long	1 long
C	12	SIT5	1 short	1 short	1 short
D	13	SIT6	1 short	1 short	1 long
E	14	SIT7	1 short	1 long	1 short
F	15	SIT8	1 short	1 long	1 long
10	16	SIT9	1 long	1 short	1 short
11	17	SIT10	1 long	1 short	1 long
12	18	SIT11	1 long	1 long	1 short
13	19	SIT12	1 long	1 long	1 long
14	20	SIT13	1 long	1 short	1 short
15	21	SIT14	1 long	1 short	1 long
16	22	SIT15	1 long	1 long	1 short
17	23	SIT16	1 long	1 long	1 long
Note: SIT components					
Frequencies (Hz)		First tone	Second tone	Third tone	
	low	913.8	1370.6	1776.7	
	high	985.2	1428.5	NA	
Duration (ms)	short	288			
	long	384			

NT1X76CA (continued)

Special Information Tone (SIT) definitions (Sheet 2 of 2)

Phrase number hexadecimal	Phrase number decimal	Name	First tone	Second tone	Third tone
18	24	SIT17	1 short	1 short	1 short
19	25	SIT18	1 short	1 short	1 long
1A	26	SIT19	1 short	1 long	1 short
1B	27	SIT20	1 short	1 long	1 long
1C	28	SIT21	1 short	1 short	1 short
1D	29	SIT22	1 short	1 short	1 long
1E	30	SIT23	1 short	1 long	1 short
1F	31	SIT24	1 short	1 long	1 long
20	32	SIT25	1 long	1 short	1 short
21	33	SIT26	1 long	1 short	1 long
22	34	SIT27	1 long	1 long	1 short
23	35	SIT28	1 long	1 long	1 long
24	36	SIT29	1 long	1 short	1 short
25	37	SIT30	1 long	1 short	1 long
26	38	SIT31	1 long	1 long	1 short
27	39	SIT32	1 long	1 long	1 long

Note: SIT components

Frequencies (Hz)		First tone	Second tone	Third tone
	low	913.8	1370.6	1776.7
	high	985.2	1428.5	NA
Duration (ms)	short	288		
	long	384		

NT1X76CA Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
0	0	1.024	-	1 s of silence
1	1	0.160	-	test tone 760 Hz at -13 dbm
2	2	0.992	-	prompt tone
3	3	0.512	-	0.5 s of silence
4 to 7	4 to 7	-	-	reserved phrase
8 to 27	8 to 39	-	SIT1 to SIT32	SIT combination 1 (refer to note) to SIT combination 32
28	40	0.864	letter C	C
29	41	0.864	letter L	L
2A	42	0.864	letter N	N
2B	43	0.864	letter P	P
2C	44	0.864	letter X	X
2D	45	0.928	MCC16	Thank you
2F	47	0.608	digit 0	zero
30	48	0.519	digit 1	one
31	49	0.544	digit 2	two
32	50	0.544	digit 3	three
33	51	0.640	digit 4	four
34	52	0.768	digit 5	five
35	53	0.640	digit 6	six
36	54	0.672	digit 7	seven

Note 1: Phrase ID can be either hexadecimal or decimal.

Note 2: The phrase name is a suggested phrase name that can change as required.

NT1X76CA (continued)

NT1X76CA Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID[1] Hexadecimal	Phrase ID Decimal	Time (seconds)	Name[2]	Announcement
37	55	0.544	digit 8	eight
38	56	0.672	digit 9	nine

Note 1: Phrase ID can be either hexadecimal or decimal.

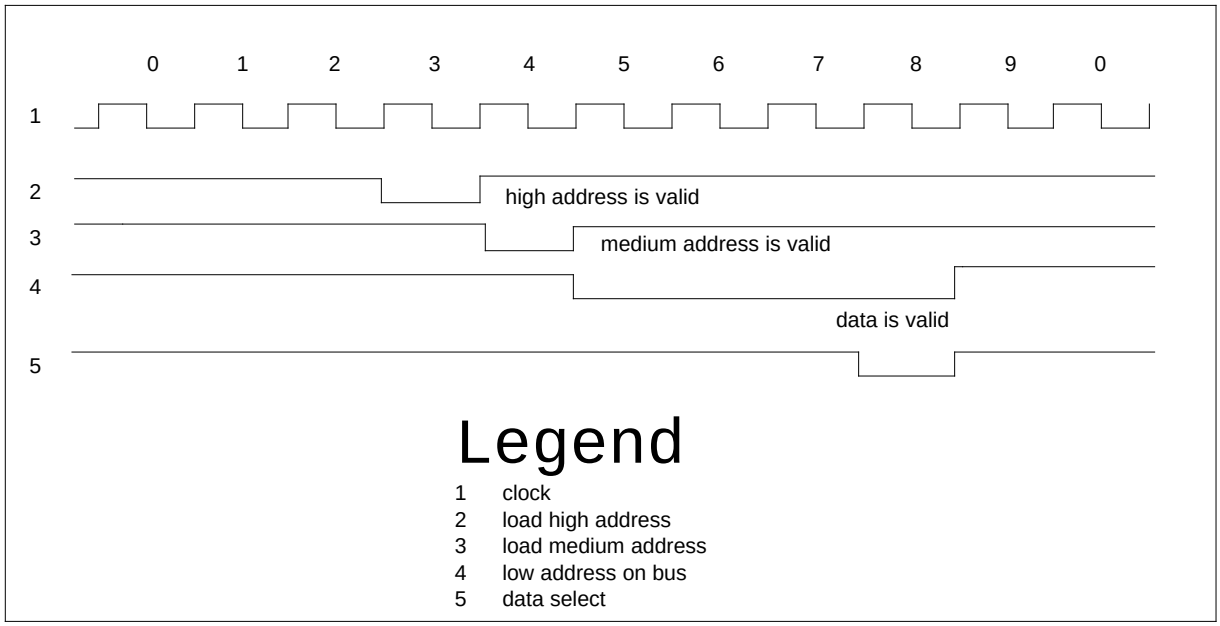
Note 2: The phrase name is a suggested phrase name that can change as required.

Signaling

Timing

The timing of the NT1X76CA appears in the following figure.

NT1X76CA timing



Technical data

Electrical requirements

The voltage required is + 5V. The current required is 2.2A.

Environmental conditions

The following table provides the ambient conditions for the NT1X76CA.

NT1X76CA ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30 ° C	5 to 49 ° C
Relative humidity	20 % to 55 %	20 % to 80 %

NT1X76GA

Product description

Digital recorded announcement (DRA) hardware includes a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76GA is a double density card (256 kbyte-two virtual cards) and occupies one slot in the maintenance trunk module (MTM). It has a three-position single-pole double-throw dual inline package (DIP) switch, which you must set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76GA multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address latches in the high address latch. The medium address latches in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies enables the data buffer. A card enable signal enables the row decoder when the decoded address is within the address range of the memory devices.

The row and column address decoders inform the memory devices of column and row addresses. While the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. A data strobe sent by the processor also enables the data.

Speech memory contents

The following tables present phrase IDs and content associated with the NT1X76GA CMS/CLASS phase I and II speech ROM card. Phrase IDs and

content include silences, phrases, and tones. Virtual card 0 and virtual card 1 refer to the two virtual cards in the NT1X76GA.

NT1X76GA Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.208	2.752	including 11 private entries.
005	1.888	2.432	that includes 12 private entries.
006	2.176	2.720	that includes 13 private entries.
007	2.080	2.624	that includes 14 private entries.
008	1.984	2.528	that includes 15 private entries.
009	2.112	2.656	that includes 16 private entries.
00A	2.240	2.784	that includes 17 private entries.
00B	1.664	2.208	that includes one private entry.
00C	1.760	2.304	that includes two private entries.
00D	1.952	2.496	that includes three private entries.
00E	1.760	2.304	that includes four private entries.

Note: Total duration includes silence blocks at the beginning or end.

NT1X76GA (continued)

NT1X76GA Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
00F	1.984	2.528	that includes five private entries.
010	2.080	2.624	that includes six private entries.
011	1.888	2.432	that includes seven private entries.
012	1.824	2.368	that includes eight private entries.
013	2.016	2.560	that includes nine private entries.
Note: Total duration includes silence blocks at the beginning or end.			

NT1X76GA Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	1.952	2.496	that includes 10 private entries.
005	2.272	2.816	that includes 18 private entries.
006	2.080	2.624	that includes 19 private entries.
007	1.920	2.464	that includes 20 private entries.
Note: Total duration includes silence blocks at the beginning or end.			

NT1X76GA Speech memory contents for virtual card 1 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
008	2.208	2.752	that includes 21 private entries.
009	2.080	2.624	that includes 22 private entries.
00A	2.272	2.816	that includes 23 private entries.
00B	2.208	2.752	that includes 24 private entry.
00C	2.208	2.752	that includes 25 private entries.
00D	2.144	2.688	that includes 26 private entries.
00E	2.208	2.752	that includes 27 private entries.
00F	2.176	2.720	that includes 28 private entries.
010	2.304	2.848	that includes 29 private entries.
011	1.888	2.432	that includes 30 private entries.
012	2.208	2.752	that includes 31 private entries.

Note: Total duration includes silence blocks at the beginning or end.

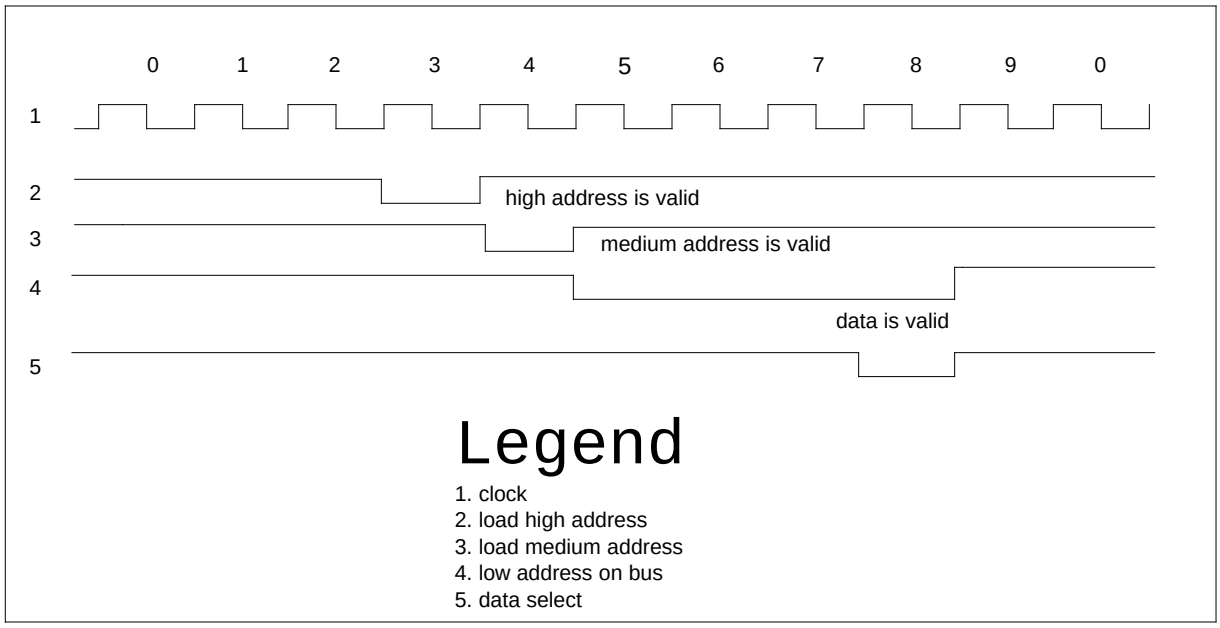
Signaling

Timing

The timing of the NT1X76GA appears in the following figure.

NT1X76GA (end)

NT1X76GA timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GB

Product description

Digital recorded announcement (DRA) hardware includes a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76GB is a double density card (256 kbyte-two virtual cards) and is in one slot in the maintenance trunk module (MTM). The NT1X76GB has a three-position single-pole double-throw dual inline package (DIP) switch, that you must set to the number assigned on the card. This number is the BLOCKLIST value in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76GB multiplexes addresses because only 8 bits are available on the backplane and requires 20 bits to address the DRA. The high address latches in the high address latch. The medium address is latches in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies enables the data buffer. The signal enables the row decoder when the decoded address is within the address range of the memory devices.

The row and column address decoders inform memory devices when there are column and row addresses. While the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. Data strobe sent by the processor also enables the data.

Speech memory contents

The following tables present phrase IDs and content associated with the NT1X76GB CMS/CLASS phase I and II speech ROM card. Phrase IDs and

NT1X76GB (continued)

content include silences, phrase, and tones. Virtual card 0 and virtual card 1 refer to the two virtual cards in the NT1X76GB.

NT1X76GB Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.848	3.392	There are 13 private entries on your list.
005	2.880	3.424	There are 14 private entries on your list.
006	2.720	3.254	There are 15 private entries on your list.
007	2.752	3.296	There are 16 private entries on your list.
008	3.072	3.616	There are 17 private entries on your list.
009	3.008	3.552	There are 18 private entries on your list.
00A	2.848	3.392	There are 19 private entries on your list.
00B	2.720	3.264	There are 20 private entries on your list.
00C	2.816	3.360	There are 21 private entries on your list.
00D	2.784	3.328	There are 22 private entries on your list.
00E	2.816	3.360	There are 23 private entries on your list.

Note: Total duration includes silence blocks at the beginning or end.

NT1X76GB Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.784	3.328	There are 24 private entries on your list.
005	2.880	3.424	There are 25 private entries on your list.
006	2.848	3.392	There are 26 private entries on your list.
007	3.008	3.552	There are 27 private entries on your list.
008	2.368	2.912	There are 28 private entries on your list.
009	2.912	3.456	There are 29 private entries on your list.
00A	2.176	2.720	There are 30 private entries on your list.
00B	2.656	3.200	There are 31 private entries on your list.
00C	3.552	4.224	Please try other options, or dial 0 for instructions.

Note: Total duration includes silence blocks at the beginning or end.

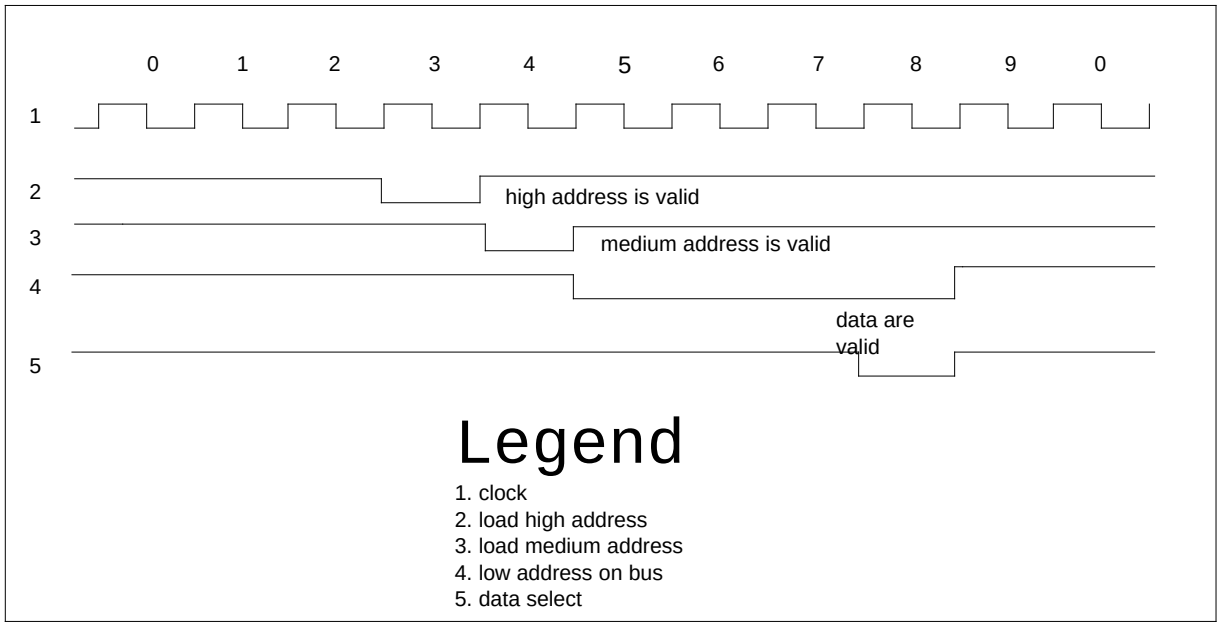
Signaling

Timing

The timing of the NT1X76G Bappears in the following figure.

NT1X76GB (end)

NT1X76GB timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GC

Product description

Digital recorded announcement (DRA) hardware includes a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76GC is a double density card (256 kbyte-two virtual cards). The NT1X76GC is in one slot in the maintenance trunk module (MTM). The NT1X76GC has a three-position single-pole double-throw dual inline package (DIP) switch, which must be set to the number on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76GC multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address latches in the high address latch. The medium address latches in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies enables the data buffer. The signal enables the row decoder when the decoded address is within the address range of the memory devices.

The row and column address decoders inform the memory devices when there are column and row addresses. The column addresses enable the outputs of the memory devices. The row addresses act as chip enables. Data strobe sent by the processor also enables the data.

Speech memory contents

The following tables present phrase IDs and content associated with NT1X76GC CMS/CLASS phase I and II speech ROM card. Phrase IDs and

NT1X76GC (continued)

content include silences, phrases and tones. Virtual card 0 and virtual card 1 refer to the two virtual cards contained in NT1X76GC.

NT1X76GC Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.144	2.688	There are 13 entries on your list.
005	2.336	2.880	There are 14 entries on your list.
006	2.208	2.752	There are 15 entries on your list.
007	2.336	2.880	There are 16 entries on your list.
008	2.336	2.880	There are 17 entries on your list.
009	2.144	2.688	There are 18 entries on your list.
00A	2.368	2.912	There are 19 entries on your list.
00B	2.112	2.656	There are 20 entries on your list.
00C	2.464	3.008	There are 21 entries on your list.
00D	2.368	2.912	There are 22 entries on your list.
00E	2.528	3.072	There are 23 entries on your list.

Note: Total duration includes silence blocks at the beginning or end.

NT1X76GC Speech memory contents for virtual card 0 (Sheet 2 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
00F	2.400	2.944	There are 24 entries on your list.
010	2.400	2.944	There are 25 entries on your list.
Note: Total duration includes silence blocks at the beginning or end.			

NT1X76GC Speech memory contents for virtual card 1 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.272	2.816	There are 26 entries on your list.
005	2.464	3.008	There are 27 entries on your list.
006	2.336	2.880	There are 28 entries on your list.
007	2.336	2.880	There are 29 entries on your list.
008	2.208	2.752	There are 30 entries on your list.
009	2.432	2.976	There are 31 entries on your list.
Note: Total duration includes silence blocks at the beginning or end.			

NT1X76GC (end)

NT1X76GC Speech memory contents for virtual card 1 (Sheet 2 of 2)

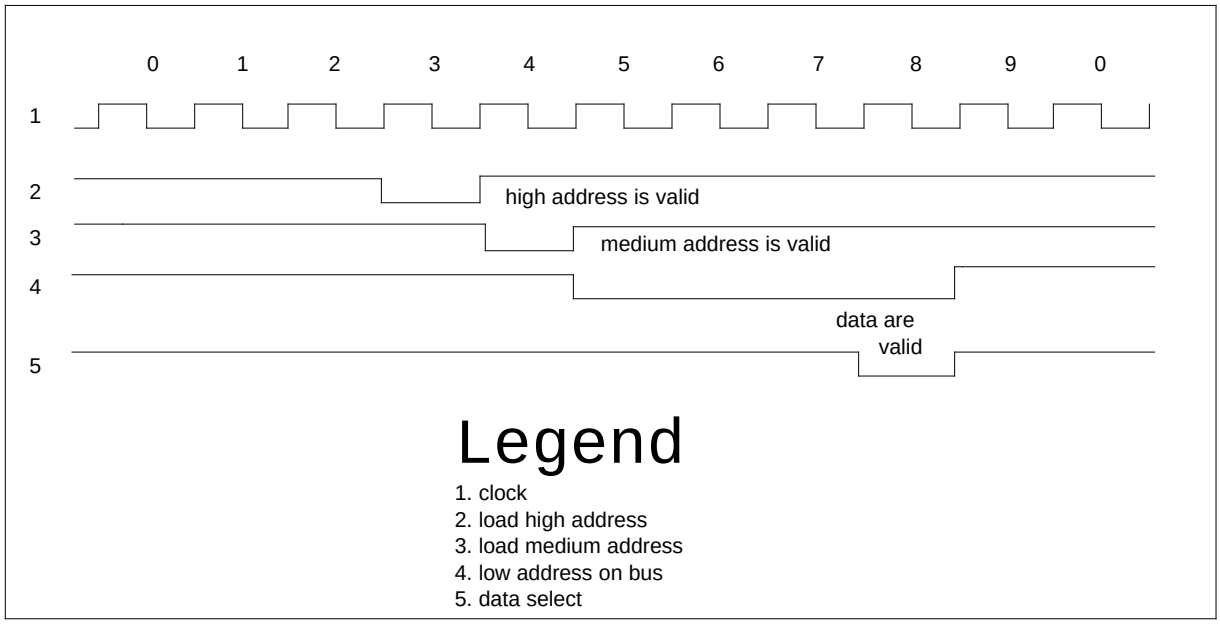
Phrase ID	Duration seconds	Total duration seconds	Content
00A		0.032	
00B		0.640	
Note: Total duration includes silence blocks at the beginning or end.			

Signaling

Timing

The timing of the NT1X76GC appears in the following figure.

NT1X76GC timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GE

Product description

Digital recorded announcement (DRA) hardware includes a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76GE is a double density card (256 kbyte-two virtual cards). The NT1X76GE is in one slot in the maintenance trunk module (MTM). The NT1X76GE has a three-position single-pole double-throw dual inline package (DIP) switch, which must be set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76GE multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address latches in the high address latch. The medium address latches in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies enables the data buffer. The signal enables the row decoder when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when there are column and row addresses. The column addresses enable the outputs of the memory devices. The row addresses act as chip enables. A strobe sent by the processor also enables the data.

Speech memory contents

The following tables present phrase IDs and content associated with the NT1X76GE CMS/CLASS phase I and II speech ROM card. Phrase IDs and

NT1X76GE (continued)

content include silences, phrases and tones. Virtual card 0 and virtual card 1 refer to the two virtual cards in the NT1X76GE.

NT1X76GE Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.464	3.072	Your call block service is now on.
005	2.560	3.168	Your call block service is now off.
006	2.752	3.360	Your call selector service in now on.
007	2.848	3.456	Your call selector service in now off.
008	3.488	4.096	Your preferred call forwarding service is now on.
009	3.392	4.000	Your preferred call forwarding service is now off.
00A	3.392	4.000	Your selective call acceptance service is now on.
00B	3.456	4.064	Your selective call acceptance service is now off.
00C	0.352	1.024	Class prompt tone
00D		0.032	Pause

Note: Total duration includes silence blocks at the beginning or end.

NT1X76GE Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	6.944	8.244	If this number is correct, dial 1. If this number is not correct, dial 0.
005	1.280	1.952	Please dial now.
006	6.048	6.720	We are sorry. Please hang up now, consult your written instructions, and try again later.
007	6.048	7.264	We are sorry. Please hang up now, consult your written instructions, and try again later.
008	5.600	6.272	You may dial during the announcements for faster service. When you finish, hang up.
009	7.104	7.776	After hearing an entry, you may dial 0, 7 to delete the entry and continue reviewing your list.

Note: Total duration includes silence blocks at the beginning or end.

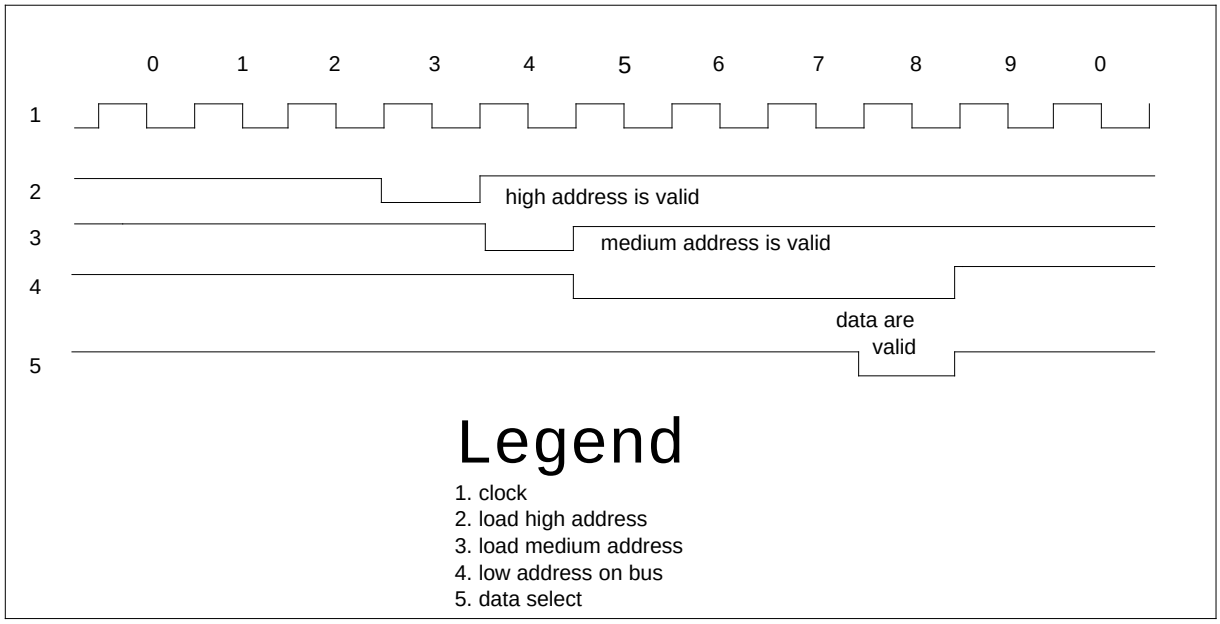
Signaling

Timing

The timing of the NT1X76GE appears in the following figure.

NT1X76GE (end)

NT1X76GE timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GF

Product description

Digital recorded announcement (DRA) hardware includes a speech processor, a microprocessor controller, and speech memory. Permanent speech memory is on the NT1X76 EPROM card.

The NT1X76GF is a double density card (256 kbyte-two virtual cards) and occupies one slot in the maintenance trunk module (MTM). The NT1X76GF has a three-position single-pole double-throw dual inline package (DIP) switch. The switch must be set to the number assigned on the card. This number is the BLOCKLIST value entered in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76GF multiplexes addresses because only 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address latches in the high address latch. The medium address latches in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies enables the data buffer. The signal enables the row decoder when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when there are column and row addresses. The column addresses enable the outputs of the memory devices. The row addresses act as chip enables. Data strobe sent by the processor also enables the data.

Speech memory contents

The following tables present phrase IDs and content associated with the NT1X76GF CMS/CLASS phase I and II speech ROM card. Phrase IDs and

NT1X76GF (continued)

content include silences, phrases and tones. Virtual card 0 and virtual card 1 refer to the two virtual cards contained in NT1X76GF.

NT1X76GF Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.464	3.072	Your call block service is now on.
005	2.560	3.168	Your call block service is now off.
006	2.848	3.456	Your priority call service in now on.
007	2.848	3.456	Your priority call service in now off.
008	2.944	3.552	Your select call forward service is now on.
009	2.994	3.552	Your select call forward service is now off.
00A	3.392	4.000	Your selective call acceptance service is now on.
00B	3.456	4.064	Your selective call acceptance service is now off.
00C	0.352	1.024	Class prompt tone
00D		0.032	Pause

Note: Total duration includes silence blocks at the beginning or end.

NT1X76GF Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	6.944	8.224	If this number is correct, dial 1. If this number is not correct, dial 0.
005	1.280	1.952	Please dial now.
006	6.048	6.720	We are sorry. Please hang up now, consult your written instructions, and try again later.
007	6.048	7.264	We are sorry. Please hang up now, consult your written instructions, and try again later.
008	5.600	6.272	You may dial during the announcements for faster service. When you have finished, hang up.
009	7.104	7.776	After hearing an entry, you may dial 0, 7 to delete it and continue reviewing your list.

Note: Total duration includes silence blocks at the beginning or end.

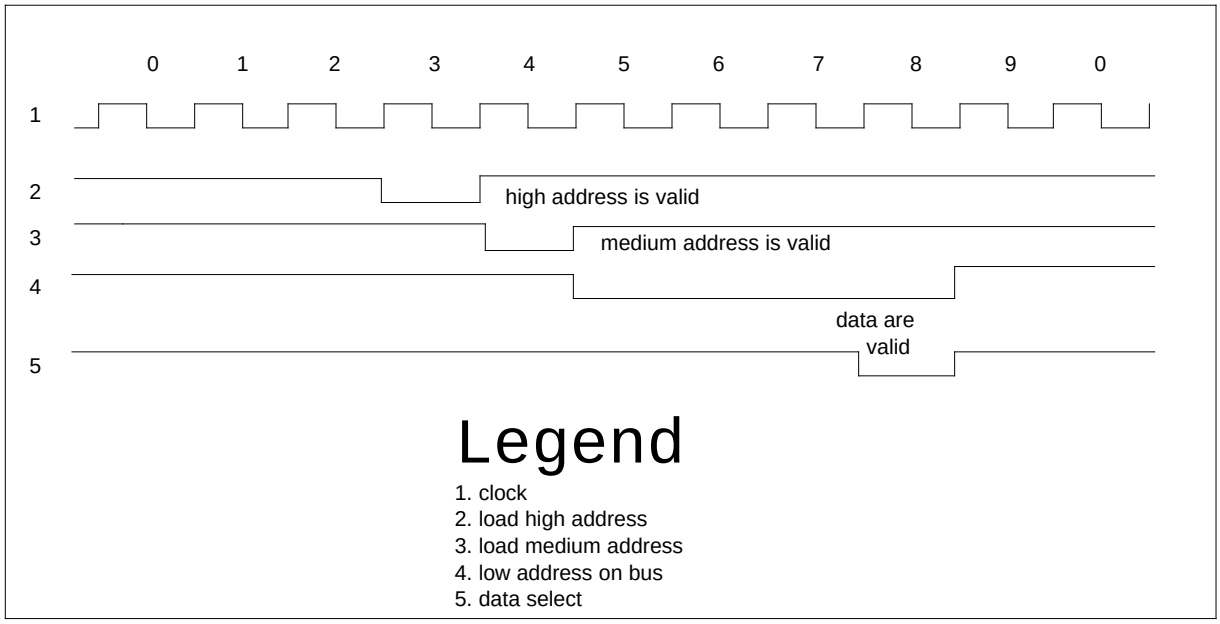
Signaling

Timing

The timing of the NT1X76GF appears in the following figure.

NT1X76GF (end)

NT1X76GF timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GG

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent memory.

The NT1X76GG, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76GG has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76GG multiplexes addresses because the backplane provides 8 bits and requires 20 bits to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The bus contains the lower address latch by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies activates the data buffer and the row decoder. The card enable signal activates the data buffer and row decoder. This event occurs when decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe that the processor sends also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76GG CMS/CLASS phase I and II speech ROM card appear in the following two tables. The

NT1X76GG (continued)

content can be silences, phrases, and tones. The two virtual cards in the NT1X76GG are virtual card 0 and virtual card 1.

NT1X76GG Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	3.136	3.744	Your selective call block service is on.
005	2.976	3.584	Your selective call block service is off.
006	3.072	3.680	Your selective ringing service in on.
007	2.784	3.392	Your selective ringing service in off.
008	3.456	4.064	Your selective call forwarding service is on.
009	3.392	4.000	Your selective call forwarding service is off.
00A	3.392	4.000	Your selective call acceptance service is on.
00B	3.456	4.064	Your selective call acceptance service is off.
00C	0.352	1.024	Class prompt tone
00D		0.032	Pause

Note: Total duration includes silence blocks added at the start or end.

NT1X76GG Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	6.944	8.244	If this number is correct, dial 1. If this number is not correct, dial 0.
005	1.280	1.952	Please dial now.
006	6.048	6.720	We are sorry. Please hang up now, consult your instructions, and try again later.
007	6.048	7.264	We are sorry. Please hang up now, consult your instructions, and try again later.
008	5.600	6.272	You can dial during the announcements for quicker service. When you complete dialing hang up.
009	7.104	7.776	After you hear an entry, you can dial 0, 7 to delete the entry and continue to review your list.

Note: Total duration includes silence blocks added at the start or end.

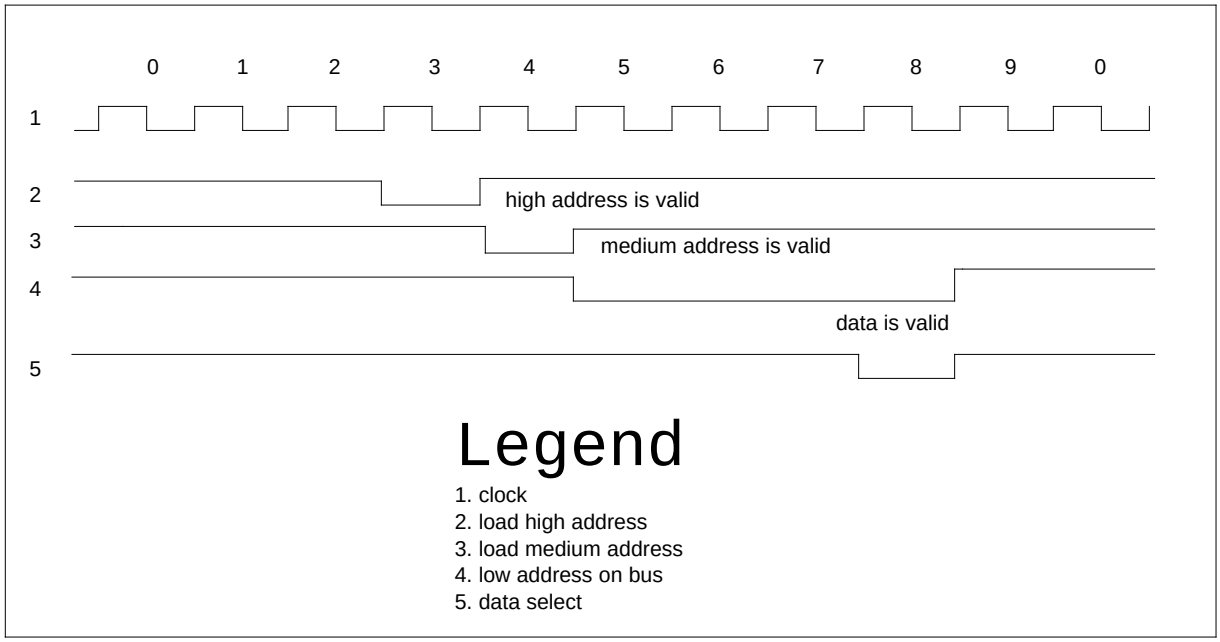
Signaling

Timing

The timing of the NT1X76GG appears in the following figure.

NT1X76GG (end)

NT1X76GG timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GH

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent speech memory.

The NT1X76GH, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76GH has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76GH multiplexes addresses because the backplane provides 8 bits and requires 20 bits to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The bus contains the lower address by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal, that the EPROM supplies activates the data buffer and the row decoder. This signal activates the data buffer and the row decoder. This signal activates when the decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe that the processor sends also activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76GH CMS/CLASS phase I and II speech ROM card appear in the following two tables. The content can be silences, phrases, and tones. The two virtual cards in the are virtual card 0 and virtual card 1.

NT1X76GH Speech memory contents for virtual card 0 (Sheet 1 of 2)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence

Note: Total duration includes silence blocks added at the start or end.

NT1X76GH (continued)

NT1X76GH Speech memory contents for virtual card 0 (Sheet 2 of 2)

001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	2.464	3.072	Your call block service is on.
005	2.560	3.168	Your call block service is off.
006	3.328	3.936	Your VIP alert service is on.
007	3.168	3.776	Your VIP alert service is off.
008	3.296	3.904	Your special call forwarding service is on.
009	3.520	4.128	Your special call forwarding service is off.
00A	3.328	3.936	Your special call acceptance service is on.
00B	3.040	3.648	Your special call acceptance service is off.
00C	0.352	1.024	Class prompt tone
00D		0.032	Pause

Note: Total duration includes silence blocks added at the start or end.

NT1X76GH Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	6.944	8.224	If this number is correct, dial 1. If this number is not correct, dial o.
005	1.280	1.952	Please dial now.
006	6.048	6.720	We are sorry. Please hang up now, consult your instructions, and try again later.
007	6.048	7.264	We are sorry. Please hang up now, consult your instructions, and try again later.
008	5.600	6.272	You can dial during the announcements for faster service. When you finish dialing, hang up.
009	7.104	7.776	After you hear an entry, you can dial 0, 7 to delete the entry. Continue to review your list.

Note: Total duration includes silence blocks added at the start or end.

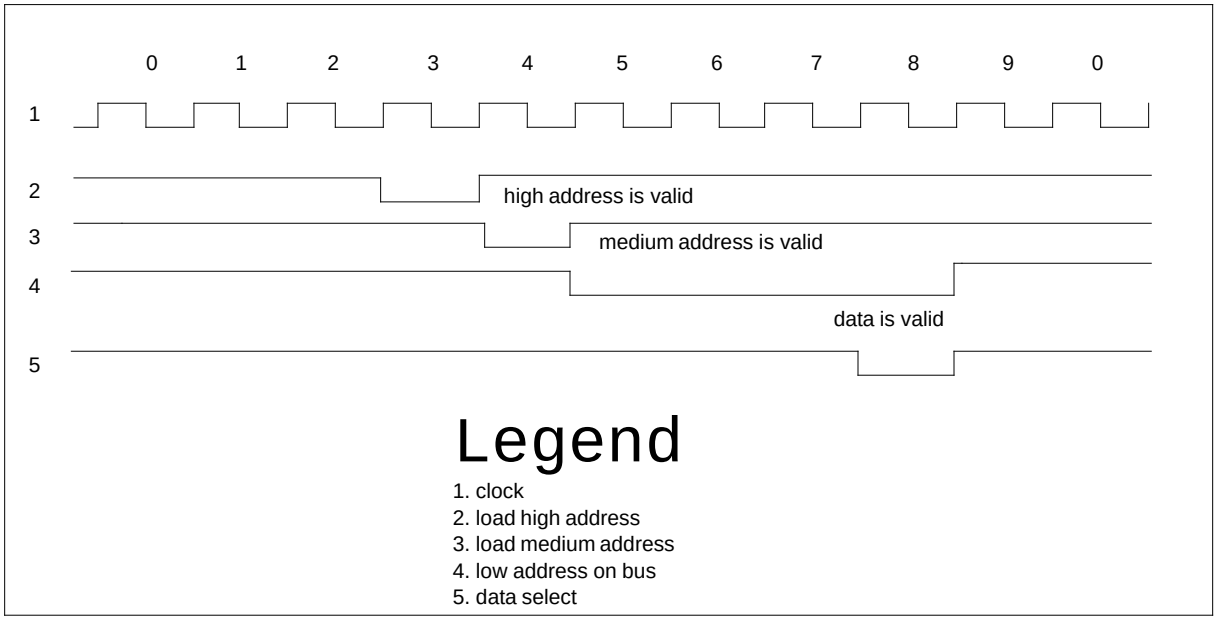
NT1X76GH (end)

Signaling

Timing

The timing of the NT1X76GH appears in the following figure.

NT1X76GH timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GJ

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent speech memory.

The NT1X76GJ, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76GJ has a three-position, single-pole, double-throw, dual inline package (DIP) switch. You must set the switch to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76GJ multiplexes addresses because the backplane provides 8 bits and requires 20 bits to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The bus contains the lower address by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies, activates the data buffer and the row decoder. This signal activates the data buffer and the row decoder when the decoded address is present in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe that the processor sends also activates the data.

Speech memory contents

The phrase IDs and content appear in the following two tables. The IDs and content associate with the NT1X76GJ CMS/CLASS phase I and II speech

NT1X76GJ (continued)

ROM card. The content can be silences, phrases and tones. The two virtual cards in the NT1X76GJ are virtual card 0 and virtual card 1.

NT1X76GJ Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	2.464	3.072	Your call block service is on.
005	2.560	3.168	Your call block service is off.
006	2.912	3.520	Your priority ringing service is on.
007	3.040	3.648	Your priority ringing service is off.
008	3.456	4.064	Your selective call forwarding service is on.
009	3.392	4.000	Your selective call forwarding service is off.
00A	3.392	4.000	Your selective call acceptance service is on.
00B	3.456	4.064	Your selective call acceptance service is off.
00C	0.352	1.024	Class prompt tone
00D		0.032	Pause

Note: Total duration includes silence blocks added at the start or end.

NT1X76GJ Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	6.944	8.224	If this number is correct, dial 1. If this number is not correct, dial 0.
005	1.280	1.952	Please dial now.
006	6.048	7.264	We are sorry. Please hang up now, consult your instructions, and try again later.
007	6.048	7.264	We are sorry. Please hang up now, consult your instructions, and try again later.
008	5.600	6.272	You can dial during the announcements for faster service. When you finish dialing, hang up.
009	7.104	7.776	After you hear and entry, you can dial 0, 7 to delete the entry. Continue to review your list.

Note: Total duration includes silence blocks added at the start or end.

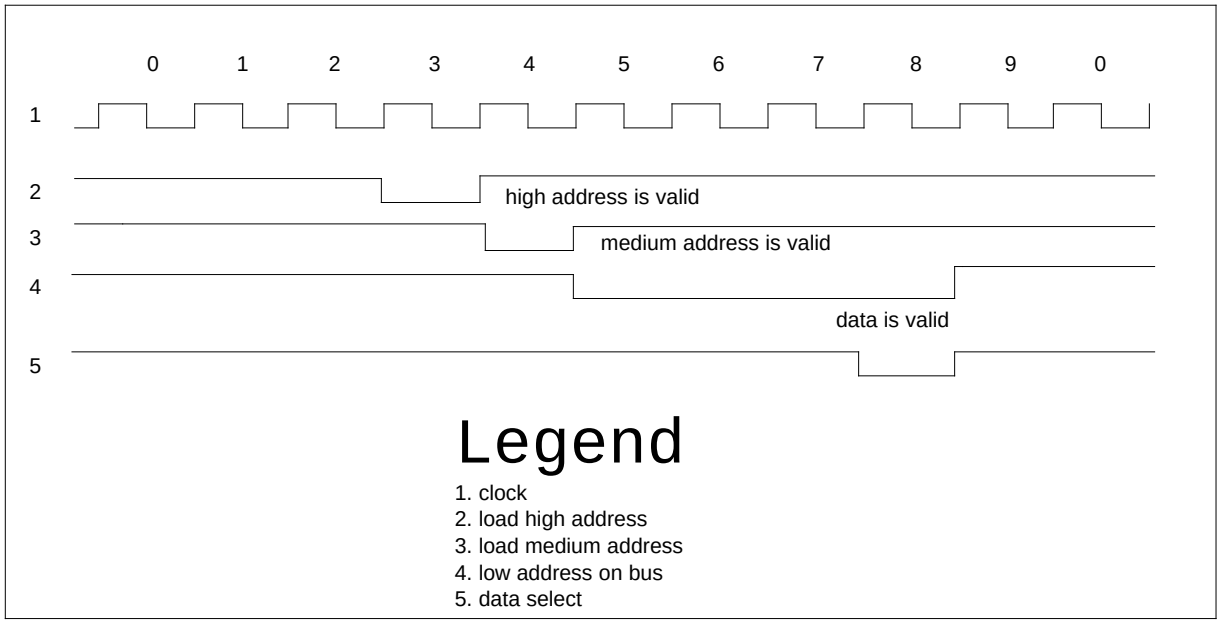
Signaling

Timing

The timing of the NT1X76GJ appears in the following figure.

NT1X76GJ (end)

NT1X76GJ timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GK

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent specch memory.

The NT1X76GK, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76GK has a three-position, single-pole, double-throw, dual inline package (DIP) switch. The DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76GK multiplexes addresses because the backplane provides 8 bits and requires 20 bits to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The bus contains the lower address by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies activates the data buffer and the row decoder. The card enable signal activates the data buffer and the row decoder. This event occurs when decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe that the processor sends activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76GK CMS/CLASS phase I and II speech ROM card appear in the following two tables. The

NT1X76GK (continued)

content can be silences, phrases, and tones. The two virtual cards in the NT1X76GK are virtual card 0 and virtual card 1.

NT1X76GK Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	2.720	3.328	Your call screening service is on.
005	2.784	3.392	Your call screening service is off.
006	3.040	3.648	Your specified ringing service is on.
007	2.944	3.552	Your specified ringing service is off.
008	3.488	4.096	Your preferred call forwarding service is on.
009	3.392	4.000	Your preferred call forwarding service is off.
00A	3.392	4.000	Your selective call acceptance service is on.
00B	3.456	4.064	Your selective call acceptance service is off.
00C	0.352	1.024	Class prompt tone
00D		0.032	Pause

Note: Total duration includes silence blocks added at the start or end.

NT1X76GK Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	6.944	8.224	If this number is correct, dial 1. If this number is not correct, dial 0.
005	1.280	1.952	Please dial now.
006	6.048	6.720	We are sorry. Please hang up now, consult your instructions. Try again later.
007	6.048	7.264	We are sorry. Please hang up now, consult your instructions, and try again later.
008	5.600	6.272	You can dial during the announcements for faster service. When you finish dialing, hang up.
009	7.104	7.776	After you hear an entry, you can dial 0, 7 to delete the entry. Continue to review your list.

Note: Total duration includes silence blocks added at the start or end.

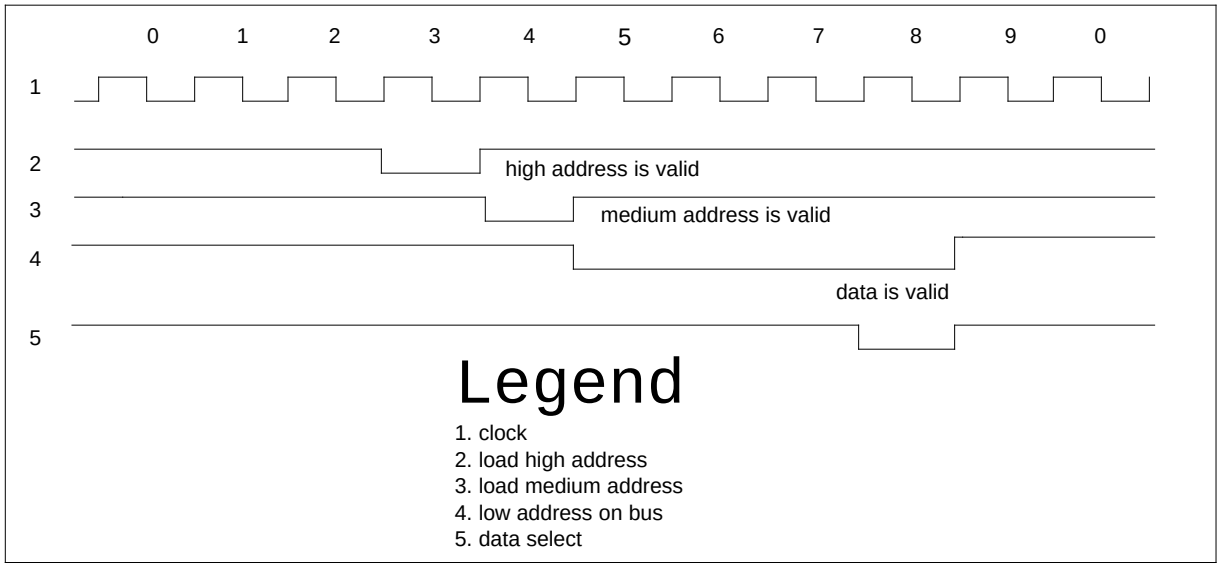
Signaling

Timing

The timing of the NT1X76GK appears in the following figure.

NT1X76GK (end)

NT1X76GK timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GL

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76 EPROM card contains permanent speech memory.

The NT1X76GL, a double density card (256 Kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76GL has a three-position, single-pole, double-throw, dual inline package (DIP) switch. This DIP switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76GL multiplexes addresses because the backplane provides 8 bits and requires 20 bits to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The bus contains the lower address by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies, enables the data buffer and the row decoder. The card enable signal enables the data buffer and the row decoder. This event occurs when decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe that the processor sends also activate the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76GL CMS/CLASS phase I and II speech ROM card appear in the following two tables. The

NT1X76GL (continued)

content can be silences, phrases, and tones. The two virtual cards in the NT1X76GL are virtual card 0 and virtual card 1.

NT1X76GL Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	2.720	3.328	Your call blocker service is on.
005	2.784	3.392	Your call blocker service is off.
006	3.040	3.648	Your priority call service is on.
007	2.944	3.552	Your priority ringing service is off.
008	3.488	4.096	Your preferred call forwarding service is on.
009	3.392	4.000	Your preferred call forwarding service is off.
00A	3.392	4.000	Your selective call acceptance service is on.
00B	3.456	4.064	Your selective call acceptance service is off.
00C	0.352	1.024	Class prompt tone
00D		0.032	Pause

Note: Total duration includes silence blocks added at the start or end.

NT1X76GL Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	6.944	8.224	If this number is correct, dial 1. If this number is not correct, dial 0.
005	1.280	1.952	Please dial now.
006	6.048	6.720	We are sorry. Please hang up now, consult your instructions, and try again later.
007	6.048	7.264	We are sorry. Please hang up now, consult your instructions, and try again later.
008	5.600	6.272	You can dial during the announcements for faster service. When you finish dialing, hang up.
009	7.104	7.776	After you hear an entry, you can dial 0, 7 to delete the entry. Continue to review your list.

Note: Total duration includes silence blocks added at the start or end.

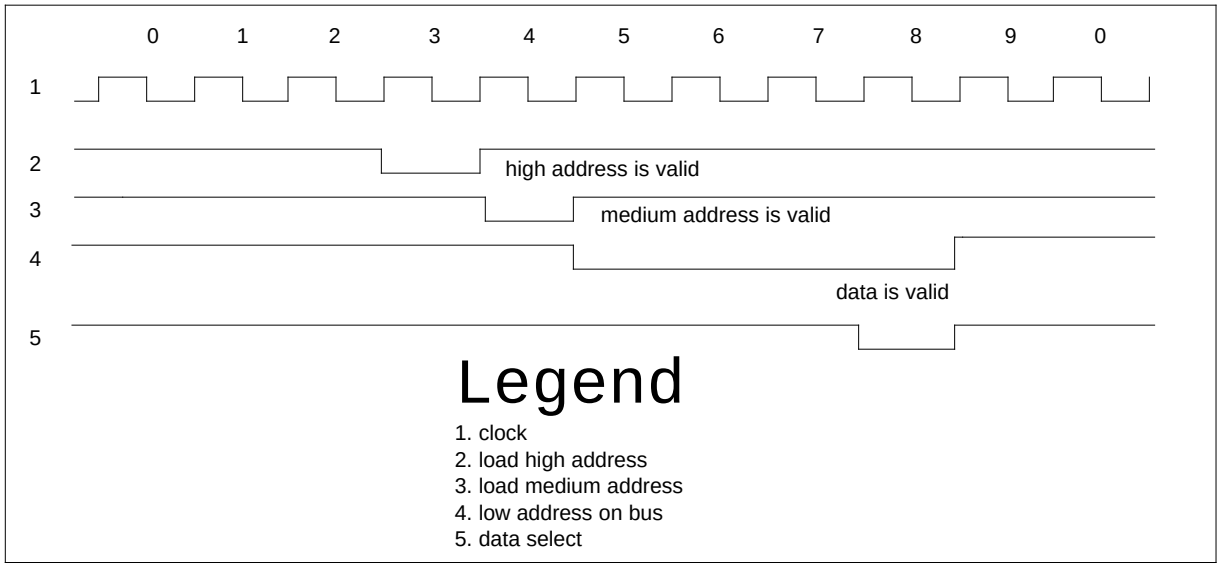
Signaling

Timing

The timing of the NT1X76GL appears in the following figure.

NT1X76GL (end)

NT1X76GL timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

NT1X76GM

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76GM EPROM card contains permanent speech memory.

The NT1X76GM, a double density card (256 kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76GM has a three-position, single-pole, double-throw, dual inline package (DIP) switch. This switch must be set to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76GM multiplexes addresses because the backplane provides 8 bits and requires 20 bits to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The bus contains the low address by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies enables the data buffer and the row decoder. The card enable signal activates the data buffer and row decoder. This event occurs when decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe that the processor sends activates the data.

Speech memory contents

The phrase IDs and content associated with the NT1X76GM CMS/CLASS phase I and II speech ROM card appear in the following two tables. The

NT1X76GM (continued)

content can be silences, phrases, and tones. The two virtual cards in the NT1X76GM are virtual card 0 and virtual card 1.

NT1X76GM Speech memory contents for virtual card 0

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			test tone
		0.160	750 Hz tone
002			prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.816	2.816	Your Call Rejection service is on.
005	2.656	2.656	Your Call Rejection service is off.
006	3.264	3.264	Your Selective Call Acceptance service is on.
007	3.232	3.232	Your Selective Call Acceptance service is off.
008	3.456	3.456	Your Selective Call Forwarding service is on.
009	3.200	3.200	Your Selective Call Forwarding service is off.
00A	2.944	2.944	Your Priority Call service is on.
00B	2.720	2.720	Your Priority Call service is off.
00C	2.752	2.752	Your Avoid-a-call service is on.
00D	2.752	2.752	Your Avoid-a-call service is now off.
00E	0.352	0.352	prompt tone

Note: Total duration includes silence blocks added at the start or end.

NT1X76GM Speech memory contents for virtual card 1

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			Test tone
		0.160	750 Hz tone
002			Prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	.25 s silence
004	6.304	6.304	If this number is correct, dial 1. If this number is not correct, dial 0.
005	1.376	1.376	Please dial now.
006	6.080	6.080	We are sorry. Please hang up now, consult your instructions, and try again later.
007	6.080	6.080	We are sorry. Please hang up now, consult your instructions, and try again later.
008	5.280	5.280	You can dial during the announcements for faster service. When you finish dialing, hang up.
009	5.952	5.952	After hearing an entry, you can dial 0, 7 to delete the entry. Continue to review your list.

Note: Total duration includes silence blocks added at the start or end.

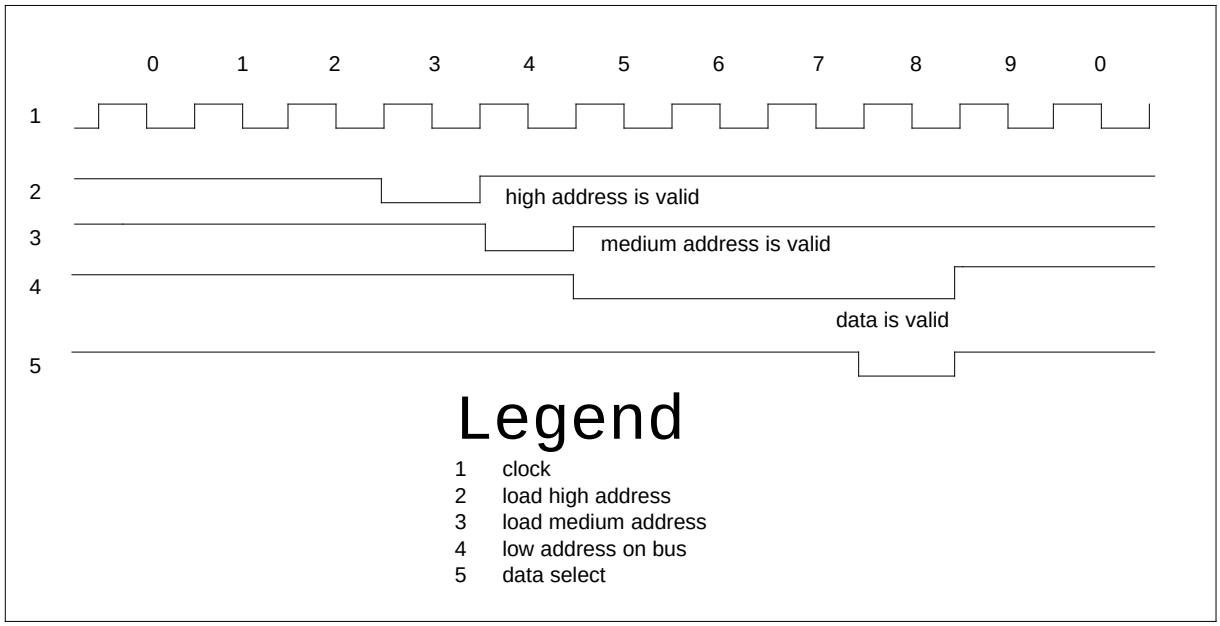
Signaling

Timing

An example of the timing of the NT1X76GM appears in the following figure.

NT1X76GM (end)

NT1X76GM timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76GM appear in the following table.

Condition	Operating range	Short-term range
Temperature	10 to 30°C	5 to 49°C
Relative humidity	20% to 55%	20% to 80%

NT1X76HC

Product description

Digital recorded announcement (DRA) hardware contains a speech processor, a microprocessor controller, and speech memory. The NT1X76HC EPROM card contains permanent memory.

The NT1X76HC, a double density card (256 kbytes-two virtual cards), occupies one slot in the maintenance trunk module (MTM). The NT1X76HC has a three-position, single-pole, double-throw, dual inline package (DIP) switch. You must set the DIP switch to the number assigned on the card. This number is the BLOCKLIST value that field CARDINFO of Table DRAMS in the digital switching system contains.

Functional description

The NT1X76HC multiplexes addresses because the backplane provides 8 bits and requires 20 bits to address the DRA. The high address is latched in the high address latch. The medium address is latched in the medium address latch. The low address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables, and write enables. A card enable signal that the EPROM supplies enables the data buffer and the row decoder. The card enable signal activates the data buffer and row decoder. This event occurs when decoded address appears in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. While the column addresses enable the outputs of the memory devices, the row addresses act as chip enables. The data strobe the processor sends also activates the data.

Speech memory contents

The phrase IDs and content appear in the following two tables. The IDs and content associate with the NT1X76HC CMS/CLASS phase I and II speech

NT1X76HC (continued)

ROM card. The content can be silences, phrases, and tones. The two virtual cards in the NT1X76HC are virtual card 0 and virtual card 1.

NT1X76HC Speech memory contents for virtual card 0 (Sheet 1 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
05	2.816		The card number received is not valid.
	2.240	5.568	Please enter your card number again.
06	2.240		Please enter your calling card number
	2.304		or dial zero to reach an operator.
	1.344	6.464	This is a recording.
07	1.024		Please hang up,
	2.624	3.808	then dial zero and the number you are calling.
08	2.816		The card number received is not valid.
	1.024		Please hang up,
	2.624	7.072	then dial zero and the number you are calling.
09	2.176		An incorrect number was dialed.
	1.024		Please hang up,
	2.624	6.432	then dial zero and the number you are dialing.
0A	2.176		An incorrect number was dialed.
	2.432	5.024	Please redial the number you are calling.
0B	0.608	0.608	Thank you.
0C	1.504	1.504	Invalid number.
0D	0.928		We are sorry,
	1.664		your call did not go through.
	1.728		Please try your call again.
	1.344	6.720	This is a recording.
0E	1.216		(CCC prompt tone)
	2.816		The card number received is not valid.
	2.240	6.784	Please enter your card number again.

Note: Total duration includes silence blocks added at the start or end.

NT1X76HC Speech memory contents for virtual card 0 (Sheet 2 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
0F	1.216		(CCC prompt tone)
	2.240		Please enter your calling card number
	2.304		or dial zero to reach an operator.
	1.344	7.680	This is a recording.
10	1.216		(CCC prompt tone)
	1.024		Please hang up,
	2.624	5.024	then dial zero and the number you are calling.
11	1.216		(CCC prompt tone)
	2.816		The card number received is not valid.
	1.024		Please hang up,
	2.624	8.288	then dial zero and the number you are calling.
12	1.216		(CCC prompt tone)
	2.176		An incorrect number was dialed.
	1.024		Please hang up,
	2.624	5.024	then dial zero and the number you are calling.
13	1.216		(CCC prompt tone)
	2.176		An incorrect number was dialed.
	2.432	6.240	Please redial the number you are calling.
14	1.216		(CCC prompt tone)
	0.608	1.824	Thank you.
15	1.216		(CCC prompt tone)
	1.504	2.720	invalid number

Note: Total duration includes silence blocks added at the start or end.

NT1X76HC (continued)

NT1X76HC Speech memory contents for virtual card 0 (Sheet 3 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
16	1.216		(CCC prompt tone)
	0.928		We are sorry,
	1.664		your call did not go through.
	1.728		Please try your call again.
	1.344	7.936	This is a recording.
17	0.032	0.032	(32 ms silence)
18	0.160	0.160	(160 ms silence)
19	0.320	0.320	(320 ms silence)
1A	0.480	0.480	(480 ms silence)
1B	0.640	0.640	(640 ms silence)
1C	0.800	0.800	(800 ms silence)
1D	0.960	0.960	(960 ms silence)

Note: Total duration includes silence blocks added at the start or end.

NT1X76HC Speech memory contents for virtual card 1 (Sheet 1 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
05	1.920	1.920	Please enter your card number.
06	2.176	2.176	Please dial the number you are calling.
07	1.952	1.952	You may place another call now.
08	0.992		Valid number,
	1.216		unrestricted PIN,
	1.824	4.608	RAO unavailable.
09	0.992		Valid number,
	1.216		unrestricted PIN,
	0.960	4.064	RAO ...

Note: Total duration includes silence blocks added at the start or end.

NT1X76HC Speech memory contents for virtual card 1 (Sheet 2 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
0A	0.992		Valid number,
	1.120		restricted PIN,
	0.960	3.968	RAO...
0B	0.640	0.704	0 (English digit-intonation 1)
0C	0.480	0.608	1 (English digit-intonation 1)
0D	0.448	0.640	2 (English digit-intonation 1)
0E	0.480	0.608	3 (English digit-intonation 1)
0F	0.480	0.608	4 (English digit-intonation 1)
10	0.608	0.672	5 (English digit-intonation 1)
11	0.512	0.640	6 (English digit-intonation 1)
12	0.544	0.640	7 (English digit-intonation 1)
13	0.352	0.608	8 (English digit-intonation 1)
14	0.608	0.672	9 (English digit-intonation 1)
15	0.672	0.736	0 (English digit-intonation 2)
16	0.544	0.672	1 (English digit-intonation 2)
17	0.416	0.704	2 (English digit-intonation 2)
18	0.448	0.704	3 (English digit-intonation 2)
19	0.384	0.704	4 (English digit-intonation 2)
1A	0.512	0.704	5 (English digit-intonation 2)
1B	0.576	0.704	6 (English digit-intonation 2)
1C	0.512	0.704	7 (English digit-intonation 2)
1D	0.352	0.736	8 (English digit-intonation 2)
1E	0.544	0.672	9 (English digit-intonation 2)

Note: Total duration includes silence blocks added at the start or end.

NT1X76HC (continued)

NT1X76HC Speech memory contents for virtual card 1 (Sheet 3 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
1F	0.512	0.640	0 (English digit-intonation 3)
20	0.416	0.576	1 (English digit-intonation 3)
21	0.320	0.576	2 (English digit-intonation 3)
22	0.384	0.576	3 (English digit-intonation 3)
23	0.384	0.576	4 (English digit-intonation 3)
24	0.448	0.608	5 (English digit-intonation 3)
25	0.512	0.640	6 (English digit-intonation 3)
26	0.480	0.608	7 (English digit-intonation 3)
27	0.384	0.608	8 (English digit-intonation 3)
28	0.544	0.640	9 (English digit-intonation 3)
29	1.216		(CCC prompt tone)
	1.920	3.136	Please enter your card number.
2A	1.216		(CCC prompt tone)
	2.176	3.392	Please dial the number you are calling.
2B	1.216		(CCC prompt tone)
	1.952	3.168	You may place another call now.
2C	1.216		(CCC prompt tone)
	0.992		Valid number,
	1.216		unrestricted PIN,
	1.824	5.824	RAO unavailable.
2D	1.216		(CCC prompt tone)
	0.992		Valid number,
	1.216		unrestricted PIN,
	0.960	4.960	RAO ...

Note: Total duration includes silence blocks added at the start or end.

NT1X76HC Speech memory contents for virtual card 1 (Sheet 4 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
2E	1.216		(CCC prompt tone)
	0.992		Valid number,
	1.120		restricted PIN,
	0.960	4.684	RAO ...
2F	0.032	0.032	(32 ms silence)
30	0.160	0.160	(160 ms silence)
31	0.320	0.320	(320 ms silence)
32	0.480	0.480	(480 ms silence)
33	0.640	0.640	(640 ms silence)
34	0.800	0.800	(800 ms silence)
35	0.960	0.960	(960 ms silence)

Note: Total duration includes silence blocks added at the start or end.

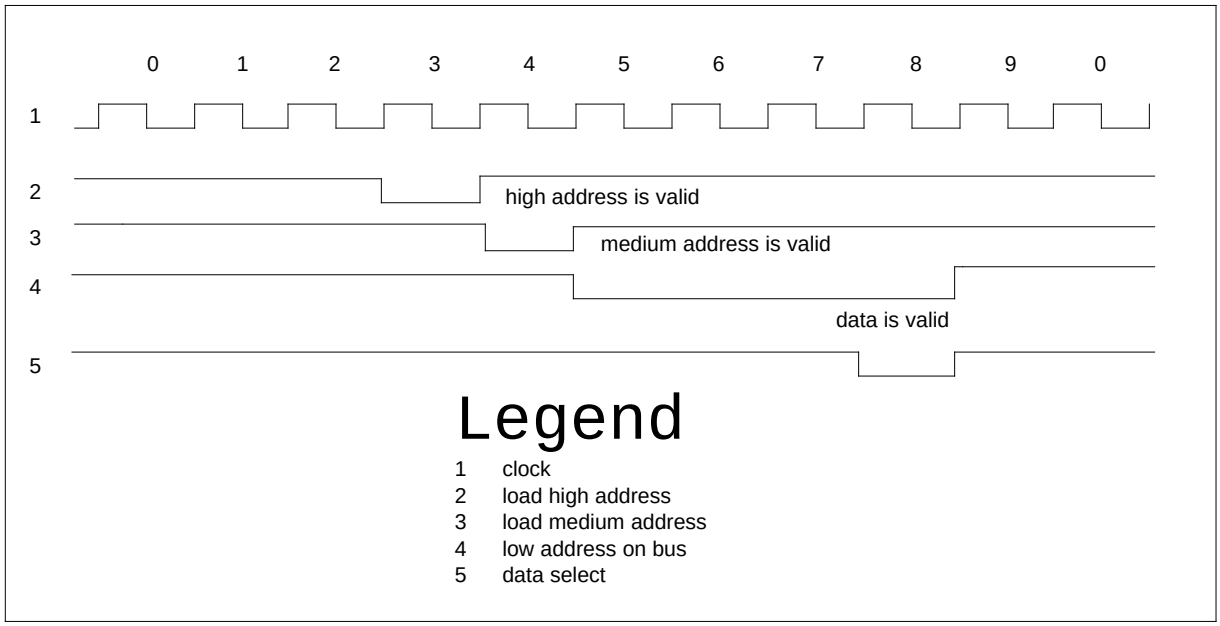
Signaling

Timing

The timing of the NT1X76HC appears in the following figures.

NT1X76HC (end)

NT1X76HC timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The ambient conditions for the NT1X76HC appear in the following table.

NT1X76HC ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30°C	5 to 49°C
Relative humidity	20% to 55%	20% to 80%

NT1X76HD

Product description

Digital recorded announcement (DRA) hardware contains the following:

- a speech processor
- a microprocessor controller
- speech memory

Permanent speech memory is on the NT1X76HD EPROM card.

The NT1X76HD is a double density card (256 kbytes—two virtual cards) that occupies one slot in the maintenance trunk module (MTM). The card has a three-position single-pole double-throw dual inline package (DIP) switch. The switch must be set to the number assigned on the card. This number is the BLOCKLIST value in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76HD multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRA. The high address is latched in the high address latch and the medium address is latched in the medium address latch. The low address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables and write enables. The EPROM QM27128 provides a card enable signal that enables the data buffer and the row decoder. This condition occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders inform the memory devices when column and row addresses are present. When the column addresses make the outputs of the memory devices able, the row addresses act as chip enables. The processor sends data strobe which enables the data.

Speech memory contents

The tables that follow present phrase IDs and content associated with the NT1X76HD CMS/CLASS phase I and II speech ROM card. Content includes

NT1X76HD (continued)

silences, phrases and tones. The two virtual cards contained in the NT1X76HD are virtual card 0 and virtual card 1.

NT1X76HD Speech memory contents for virtual card 0 (Sheet 1 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
00		1.024	one second silence
01			test tone
		0.160	705 Hz tone
02			(prompt tone)
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
03		0.256	0.25 s silence
04			(CCC prompt tone)
	0.992		941 Hz + 1477 Hz tones
	0.224	1.216	350 Hz + 440 Hz tones exponentially decreased with a time constant of 1600
05	2.816		The card number received is not valid.
	2.240	5.568	Please enter your card number again.
06	2.240		Please enter your calling card number
	2.304		or dial zero to reach an operator.
	1.344	6.464	This is a recording.
07	1.024		Please hang up,
	2.624	3.808	then dial zero and the number you are calling.

Note: Total duration includes silence blocks added at the start or end.

NT1X76HD Speech memory contents for virtual card 0 (Sheet 2 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
08	2.816		The card number received is not valid.
	1.024		Please hang up,
	2.624	7.072	then dial zero and the number you are calling.
09	2.176		An incorrect number was dialed.
	1.024		Please hang up,
	2.624	6.432	then dial zero and the number you are calling.
0A	2.176		An incorrect number was dialed.
	2.432	5.024	Please redial the number you are calling.
0B	0.608	0.608	Thank you.
0C	1.504	1.504	invalid number
0D	0.928		We are sorry,
	1.664		your call did not go through.
	1.728		Please try your call again.
	1.344	6.720	This is a recording.
0E	1.216		(CCC prompt tone)
	2.816		The card number received is not valid.
	2.240	6.784	Please enter your card number again.
0F	1.216		(CCC prompt tone)
	2.240		Please enter your calling card number
	2.304		or dial zero to reach an operator.
	1.344	7.680	This is a recording.
10	1.216		(CCC prompt tone)
	1.024		Please hang up,
	2.624	5.024	then dial zero and the number you are calling.

Note: Total duration includes silence blocks added at the start or end.

NT1X76HD (continued)

NT1X76HD Speech memory contents for virtual card 0 (Sheet 3 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
11	1.216		(CCC prompt tone)
	2.816		The card number received is not valid.
	1.024		Please hang up,
	2.624	8.288	then dial zero and the number you are calling.
12	1.216		(CCC prompt tone)
	2.176		An incorrect number was dialed.
	1.024		Please hang up,
	2.432	7.648	then dial zero and the number you are calling.
13	1.216		(CCC prompt tone)
	2.176		An incorrect number was dialed.
	2.432	6.240	Please redial the number you are calling.
14	1.216		(CCC prompt tone)
	0.608	1.824	Thank you.
15	1.216		(CCC prompt tone)
	1.504	2.720	Invalid number.
16	1.216		(CCC prompt tone)
	0.928		We are sorry,
	1.664		your call did not go through.
	1.728		Please try your call again.
	1.344	7.936	This is a recording.
17	0.320	0.320	(32 ms silence)
18	0.160	0.160	(160 ms silence)
19	0.320	0.320	(320 ms silence)
1A	0.480	0.480	(480 ms silence)
1B	0.640	0.640	(640 ms silence)

Note: Total duration includes silence blocks added at the start or end.

NT1X76HD Speech memory contents for virtual card 0 (Sheet 4 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
1C	0.800	0.800	(800 ms silence)
1D	0.960	0.960	(960 ms silence)
Note: Total duration includes silence blocks added at the start or end.			

NT1X76HD Speech memory contents for virtual card 1 (Sheet 1 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
00		1.024	one second silence
01			test tone
		0.160	705 Hz tone
02			(prompt tone)
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
03		0.256	0.25 s silence
04			(CCC prompt tone)
	0.992		941 Hz + 1477 Hz tones
	0.224	1.216	350 Hz + 440 Hz tones exponentially decreased with a time constant of 1600
05	1.920	1.920	Please enter your card number.
06	2.176	2.176	Please dial the number you are calling.
07	1.952	1.952	You may place another call now.
Note: Total duration includes silence blocks added at the start or end.			

NT1X76HD (continued)

NT1X76HD Speech memory contents for virtual card 1 (Sheet 2 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
08	0.992		Valid number,
	1.216		unrestricted PIN,
	1.824	4.608	RAO unavailable.
09	0.992		Valid number,
	1.216		unrestricted PIN,
	0.960	4.064	RAO ...
0A	0.992		Valid number,
	1.120		restricted PIN,
	0.960	3.968	RAO...
0B	0.640	0.704	0 (English digit-intonation 1)
0C	0.480	0.608	1 (English digit-intonation 1)
0D	0.448	0.640	2 (English digit-intonation 1)
0E	0.480	0.608	3 (English digit-intonation 1)
0F	0.480	0.608	4 (English digit-intonation 1)
10	0.608	0.672	5 (English digit-intonation 1)
11	0.512	0.640	6 (English digit-intonation 1)
12	0.544	0.640	7 (English digit-intonation 1)
13	0.352	0.608	8 (English digit-intonation 1)
14	0.608	0.672	9 (English digit-intonation 1)
15	0.672	0.736	0 (English digit-intonation 2)
16	0.544	0.672	1 (English digit-intonation 2)
17	0.416	0.704	2 (English digit-intonation 2)
18	0.448	0.704	3 (English digit-intonation 2)
19	0.384	0.704	4 (English digit-intonation 2)

Note: Total duration includes silence blocks added at the start or end.

NT1X76HD Speech memory contents for virtual card 1 (Sheet 3 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
1A	0.512	0.704	5 (English digit-intonation 2)
1B	0.576	0.704	6 (English digit-intonation 2)
1C	0.512	0.704	7 (English digit-intonation 2)
1D	0.352	0.736	8 (English digit-intonation 2)
1E	0.544	0.672	9 (English digit-intonation 2)
1F	0.512	0.640	0 (English digit-intonation 3)
20	0.416	0.576	1 (English digit-intonation 3)
21	0.320	0.576	2 (English digit-intonation 3)
22	0.384	0.576	3 (English digit-intonation 3)
23	0.384	0.576	4 (English digit-intonation 3)
24	0.448	0.608	5 (English digit-intonation 3)
25	0.512	0.640	6 (English digit-intonation 3)
26	0.480	0.608	7 (English digit-intonation 3)
27	0.384	0.608	8 (English digit-intonation 3)
28	0.544	0.640	9 (English digit-intonation 3)
29	1.216		(CCC prompt tone)
	1.920	3.136	Please enter your card number.
2A	1.216		(CCC prompt tone)
	2.176	3.392	Please dial the number you are calling.
2B	1.216		(CCC prompt tone)
	1.952	3.168	You may place another call now.

Note: Total duration includes silence blocks added at the start or end.

NT1X76HD (continued)

NT1X76HD Speech memory contents for virtual card 1 (Sheet 4 of 4)

Phrase ID	Duration seconds	Total duration seconds	Content
2C	1.216		(CCC prompt tone)
	0.992		Valid number,
	1.216		unrestricted PIN,
	1.824	5.824	RAO unavailable.
2D	1.216		(CCC prompt tone)
	0.992		Valid number,
	1.216		unrestricted PIN,
	0.960	4.960	RAO ...
2E	1.216		(CCC prompt tone)
	0.992		Valid number,
	1.120		restricted PIN,
	0.960	4.684	RAO ...
2F	0.032	0.032	(32 ms silence)
30	0.160	0.160	(160 ms silence)
31	0.320	0.320	(320 ms silence)
32	0.480	0.480	(480 ms silence)
33	0.640	0.640	(640 ms silence)
34	0.800	0.800	(800 ms silence)
35	0.960	0.960	(960 ms silence)

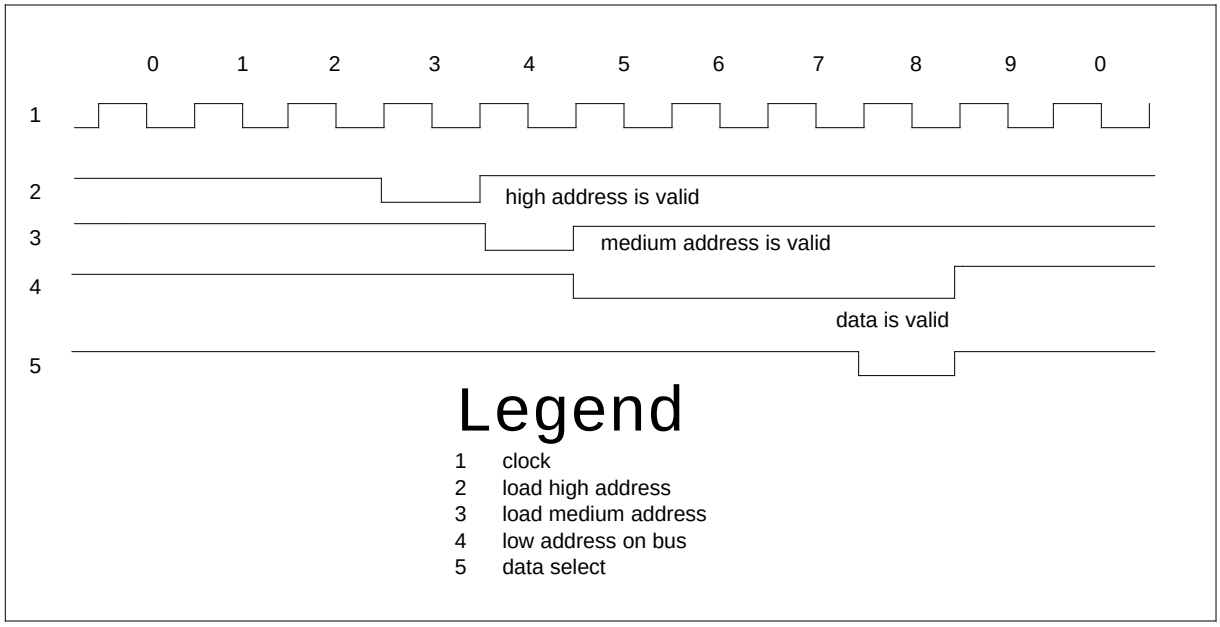
Note: Total duration includes silence blocks added at the start or end.

Signaling

Timing

The NT1X76HD timing appears in the following figure.

NT1X76HD timing



Technical data

Electrical requirements

The voltage required is +5V. The current required is 1A.

Environmental conditions

The table that follows provides the ambient conditions for the NT1X76HD.

NT1X76HD ambient conditions

Condition	Operating range	Short-term range
Temperature	10 to 30°C	5 to 49°C
Relative humidity	20% to 55%	20% to 80%

NT1X76JA

Product description

Digital recorded announcement machine (DRAM) hardware contains the following:

- a speech processor
- a microprocessor controller
- speech memory

Permanent speech memory is on the NT1X76JA EPROM card. The CMS call management services (CMS) and custom local area signaling services (CLASS) circuit cards support residential services.

The NT1X76JA is associated with the NT1X76JB card and is a double-density card (256 Kbytes—two virtual cards).

The Automatic Recall Date and Time (ARDT) feature provides messages for the automatic delivery of date and time announcements. Use of the ARDT feature must occur with the CLASS Automatic Recall feature.

Location

The NT1X76JA occupies one slot in the maintenance trunk module (MTM). The card has a three-position single-pole double-throw dual inline package (DIP) switch. The switch must be set to the number assigned on the card. This number is the BLOCKLIST value in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76JA multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRAM. The high address is latched in the high address latch and the medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables and write enables. A card enable signal enables the data buffer and the row decoder. This condition occurs when the decoded address is in address range of the memory devices. The EPROM supplies the signal.

The row and column address decoders signal the memory devices when column and row addresses are present. The column addresses enable the outputs of the memory devices and the row addresses operate as chip enables. The data strobe the processor sends also enables the data.

Speech memory contents

Tables 1 and 2 show phrase IDs and content associated with the NT1X76JA CMS/CLASS phase I and II speech ROM card. Phrase ID content includes silences, phrases and tones. The NTX1X76JA contains virtual card 0 and virtual card 1.

NT1X76JA Speech memory contents for virtual card 0 (Sheet 1 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001		0.160	test tone 760 Hz at -13 dBm
002		0.992	prompt tone
003		0.512	0.5 s of silence
004		1.0	zero (high rising intonation)
005		1.0	one
006		1.0	two
007		1.0	three
008		1.0	four
009		1.0	five
00A		1.0	six
00B		1.0	seven
00C		1.0	eight
00D		1.0	nine
00E		1.0	zero (low rising intonation)
00F		1.0	one
010		1.0	two
011		1.0	three
012		1.0	four

Note: Total duration includes silence blocks added at the start or end.

NT1X76JA (continued)

NT1X76JA Speech memory contents for virtual card 0 (Sheet 2 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
013		1.0	five
014		1.0	six
015		1.0	seven
016		1.0	eight
017		1.0	nine
018		1.0	zero (falling/rising intonation)
019		1.0	one
01A		1.0	two
01B		1.0	three
01C		1.0	four
01D		1.0	five
01E		1.0	six
01F		1.0	seven
020		1.0	eight
021		1.0	nine
022		1.0	zero (falling intonation)
023		1.0	one
024		1.0	two
025		1.0	three
026		1.0	four
027		1.0	five
028		1.0	six
029		1.0	seven

Note: Total duration includes silence blocks added at the start or end.

NT1X76JA Speech memory contents for virtual card 0 (Sheet 3 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
02A		1.0	eight
02B		1.0	nine
02C		1.0	zero (flat A intonation)
02D		1.0	one
02E		1.0	two
02F		1.0	three
030		1.0	four
031		1.0	five
032		1.0	six
033		1.0	seven
034		1.0	eight
035		1.0	nine
036		1.0	zero (flat B intonation)
037		1.0	one
038		1.0	two
039		1.0	three
Note: Total duration includes silence blocks added at the start or end.			

NT1X76JA Speech memory contents for virtual card 1 (Sheet 1 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001			test tone
		0.160	750 Hz tone
Note: Total duration includes silence blocks added at the start or end.			

NT1X76JA (continued)

NT1X76JA Speech memory contents for virtual card 1 (Sheet 2 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
002			prompt tone
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	2.176	2.368	The last number that called your line was:
005	1.888	2.208	This call was received on:
006	2.848		The last number that called your line cannot be given out.
	1.888	5.088	This call was received on:
007	3.712		We're sorry, the last number that called your line is not known.
	1.888	5.952	This call was received on:
008	1.056		To call this number,
	3.136	4.544	enter "one"; otherwise, hang up now.
009	1.248	1.440	Please hang up now.
00A	1.952	1.984	Calls that are not accepted will be
00B	1.248	1.472	forwarded to
00C	0.736	0.832	forwarded.

Note: Total duration includes silence blocks added at the start or end.

NT1X76JA Speech memory contents for virtual card 1 (Sheet 3 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
00D	0.672	0.736	denied.
00E	2.912	3.104	To change the treatment of calls that are not accepted,
00F	1.184	1.248	dial 4.
010	1.536		To confirm this treatment,
	1.216	3.104	dial 1.
011	1.536	1.600	To change this treatment,
012	0.032		
013	0.160		
014	1.280		dial 0.
	1.312	2.944	Please dial now.

Note: Total duration includes silence blocks added at the start or end.

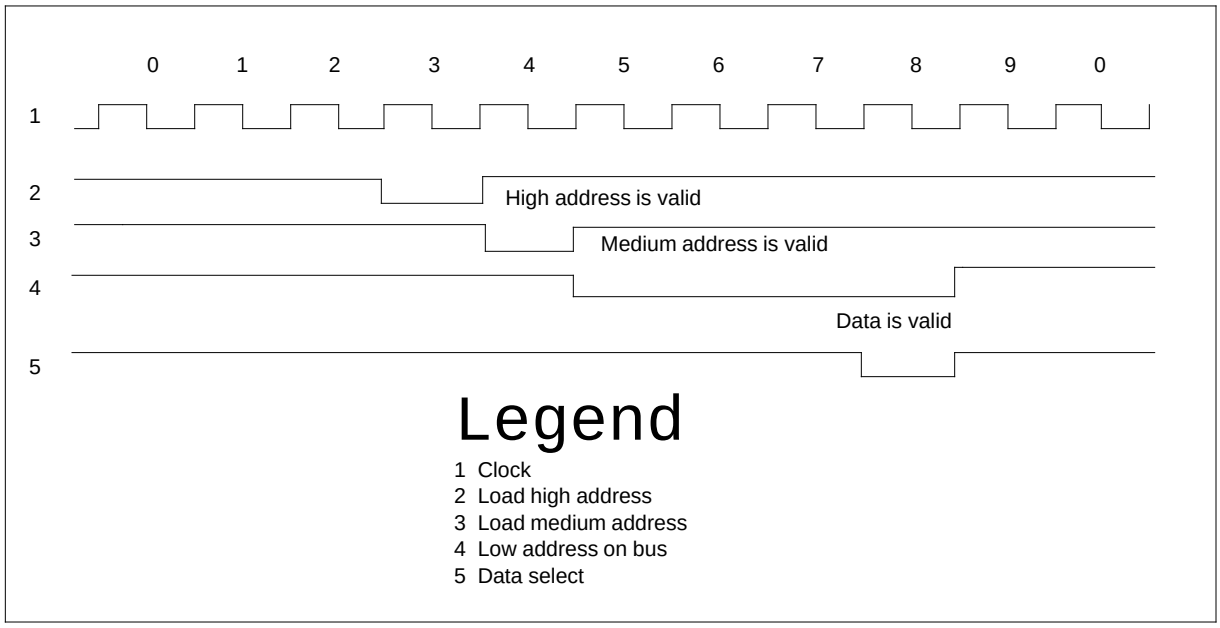
Signaling

Timing

The NT1X76JA timing appears in the following figure.

NT1X76JA (end)

NT1X76JA timing



Technical data

Power requirements

The voltage required is +5V. The current required is 1A.

NT1X76JB

Product description

Digital recorded announcement machine (DRAM) hardware contains the following:

- a speech processor
- a microprocessor controller
- speech memory

Permanent speech memory is on the NT1X76 erasable programmable read-only memory (EPROM) card. The call management services (CMS) and custom local area signaling services (CLASS) circuit cards support residential services.

The NT1X76JB associates with the NT1X76JA card and is a double-density card (256 Kbytes—two virtual cards).

The Automatic Recall Date and Time (ARDT) feature provides messages for the automatic delivery of date and time announcements. Use the ARDT feature with the CLASS Automatic Recall feature.

Location

The NT1X76JB occupies one slot in the maintenance trunk module (MTM). The card has a three-position single-pole double-throw dual inline package (DIP) switch. You must set the switch to the number assigned on the card. This number is the BLOCKLIST value in field CARDINFO of table DRAMS in the digital switching system.

Functional description

The NT1X76JB multiplexes addresses because 8 bits are available on the backplane and 20 bits are required to address the DRAM. The high address is latched in the high address latch and the medium address is latched in the medium address latch. The lower address is on the bus by default.

A decoder EPROM QM27128 provides address decoding, chip enables and write enables. A card enable signal (supplied by the EPROM) activates the data buffer and the row decoder. This condition occurs when the decoded address is in the address range of the memory devices.

The row and column address decoders signal the memory devices when column and row addresses are present. The column addresses activate the outputs of the memory devices and the row addresses act as chip enables. The data strobe the processor sends enables the data.

NT1X76JB (continued)

Speech memory contents

The phrase IDs and content appear in the following tables. The IDs and content associate with the CMS/CLASS phase I and II speech ROM card. Content includes related silences, phrases and tones. The NT1X76JB contains virtual card 0 and virtual card 1.

NT1X76JB Speech memory contents for virtual card 0 (Sheet 1 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	1 s silence
001		0.160	test tone
			750 Hz tone
002			prompt tone
	0.512	0.992	silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128		silence
003		0.256	0.25 s silence
004	0.864	0.928	January,
005	0.864	0.928	February,
006	0.800	0.864	March,
007	0.512	0.576	April,
008	0.480	0.544	May,
009	0.512	0.576	June,
00A	0.672	0.736	July,
00B	0.576	0.640	August,
00C	0.736	0.800	September,

Note: Total duration includes silence blocks added at the start or end.

NT1X76JB Speech memory contents for virtual card 0 (Sheet 2 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
00D	0.704	0.768	October,
00E	0.704	0.768	November,
00F	0.704	0.768	December,
010	0.736	0.800	AM.
011	0.800	0.864	PM.
012	0.384	0.448	at,
013	0.672	0.736	oh one,
014	0.640	0.704	oh two,
015	0.800	0.864	oh three,
016	0.704	0.768	oh four,
017	0.864	0.928	oh five,
018	0.704	0.768	oh six,
019	0.864	0.928	oh seven,
01A	0.672	0.736	oh eight,
01B	0.768	0.832	oh nine,
01C	0.480	0.544	one,
01D	0.480	0.544	two,
01E	0.544	0.608	three,
01F	0.544	0.608	four,
020	0.640	0.704	five,
021	0.576	0.640	six,
022	0.576	0.640	seven,
023	0.448	0.512	eight,

Note: Total duration includes silence blocks added at the start or end.

NT1X76JB (continued)

NT1X76JB Speech memory contents for virtual card 0 (Sheet 3 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
024	0.608	0.672	nine,
025	0.480	0.544	ten,
026	0.608	0.672	eleven,
027	0.576	0.640	twelve,
028	0.672	0.736	thirteen,
029	0.832	0.896	fourteen,
02A	0.768	0.832	fifteen,
02B	0.864	0.928	sixteen,
02C	0.960	1.024	seventeen,
02D	0.736	0.800	eighteen,
02E	0.832	0.896	nineteen,
02F	0.576	0.640	twenty,
030	0.768	0.832	twenty-one,
031	0.800	0.864	twenty-two,
032	0.800	0.864	twenty-three,

Note: Total duration includes silence blocks added at the start or end.

NT1X76JB Speech memory contents for virtual card 1 (Sheet 1 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
000		1.024	one s silence
001			test tone
		0.160	750 Hz tone
002			prompt tone

Note: Total duration includes silence blocks added at the start or end.

NT1X76JB Speech memory contents for virtual card 1 (Sheet 2 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
	0.512		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.032		silence
	0.096		750 Hz tone
	0.128	0.992	silence
003		0.256	0.25 s silence
004	0.896	0.960	twenty-four,
005	0.896	0.960	twenty-five,
006	0.928	0.992	twenty-six,
007	0.896	0.960	twenty-seven,
008	0.704	0.768	twenty-eight,
009	0.864	0.928	twenty-nine,
00A	0.544	0.608	thirty,
00B	0.768	0.832	thirty-one,
00C	0.800	0.864	thirty-two,
00D	0.896	0.960	thirty-three,
00E	0.896	0.960	thirty-four,
00F	0.896	0.960	thirty-five,
010	0.928	0.992	thirty-six,
011	0.800	0.864	thirty-seven,
012	0.672	0.736	thirty-eight,

Note: Total duration includes silence blocks added at the start or end.

NT1X76JB (continued)

NT1X76JB Speech memory contents for virtual card 1 (Sheet 3 of 3)

Phrase ID	Duration seconds	Total duration seconds	Content
013	0.864	0.928	thirty-nine,
014	0.608	0.672	forty,
015	0.832	0.896	forty-one,
016	0.864	0.928	forty-two,
017	0.896	0.960	forty-three,
018	0.864	0.928	forty-four,
019	0.992	1.056	forty-five,
01A	0.992	1.056	forty-six,
01B	0.832	0.896	forty-seven,
01C	0.800	0.864	forty-eight,
01D	0.864	0.928	forty-nine,
01E	0.608	0.672	fifty,
01F	0.832	0.896	fifty-one,
020	0.768	0.832	fifty-two,
021	0.864	0.928	fifty-three,
022	0.896	0.960	fifty-four,
023	0.896	0.960	fifty-five,
024	0.896	0.960	fifty-six,
025	0.832	0.896	fifty-seven,
026	0.832	0.896	fifty-eight,
027	0.960	1.024	fifty-nine,

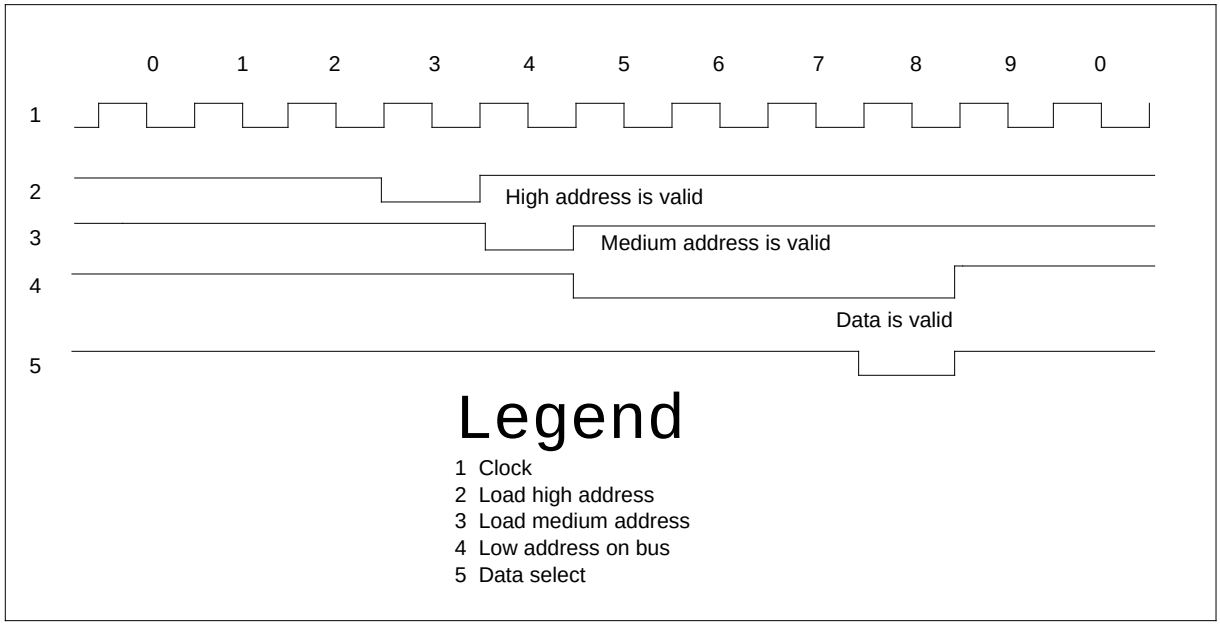
Note: Total duration includes silence blocks added at the start or end.

Signaling

Timing

The NT1X76JB timing appears in the following figure.

NT1X76JB timing



Technical data

Power requirements

The required voltage is +5V. The required current is 1A.

NT1X77AA

Product description

The NT1X77AA digital recorded announcement RAM card is part of the digital recorded announcement (DRA) hardware. The card contains the following:

- a speech processor
- a microprocessor controller
- volatile recordable speech memory

An RAM on the NT1X77AA card provides the speech memory. The RAM stores a maximum of 32 s of speech or tones.

Location

The card occupies one card position in a maintenance trunk module (MTM). The card can use MTM card positions 6 through 14.

Functional description

The NT1X77AA provides 128 kbytes of recordable memory. A menu, silence, test tones, prompt tones and special information tones use 4 kbytes of memory. Speech samples use the memory that remains. The speech is recorded in 31 segments of 1.024 s each. Each recording can last several seconds and recordings can be linked together for long announcements. Each shelf can hold a maximum of eight cards that provide a total 253.9 s of speech available to the DRA equipment.

Functional blocks

The recordable memory contains the functional blocks that follow:

- speech block
- subphrase
- phrase
- announcement
- submenu
- menu
- virtual card

Speech block

A speech block is a single unit of recorded speech, 32 ms long. Each recording contains several blocks linked together.

Subphrase

A subphrase is the smallest unit of speech that the DRA equipment can play. Subphrases can contain 1 to 255 speech blocks and are recordings like we're sorry or the number you have dialed. Each speech block is 32 ms in length.

Phrase

A phrase is a digital recording that consists of a combination of subphrases. Phrases are not complete messages to play back, but are building blocks that create these messages. Each complete phrase must be present on a single card.

Announcement

An announcement is a complete recording that contains phrases the system plays to a customer. The central control (CC) identifies the announcement that plays and sends the list of phrases for the announcement to the DRA. The phrases that an announcement contains can be on different cards.

Submenu

The submenu contains entries for each subphrase that identify the subphrase address. The entries also identify the number of times the subphrase must be repeated.

Menu

The menu contains entries that identify the subphrases in each phrase. Each menu entry contains a list of submenu entries that play to create the selected phrase.

Virtual card

A virtual card is an NT1X77AA card as identified by the DRA equipment. Each card contains a miniature switch that must be set to the virtual card ID. The virtual card ID allows the DRA to identify the card. The switch must be set to the blocklist number assigned in the BLKLIST parameter in the CARDINFO field in Table DRAMS. The following table lists the blocklist switch settings.

Blocklist switch settings

Switch position	Blocklist number							
	0	1	2	3	4	5	6	7
1	down	down	down	down	up	up	up	up
2	down	down	up	up	down	down	up	up
3	down	up	down	up	down	up	down	up

NT1X77AA (end)

Technical data

The NT1X77AA provides signal levels of 0.8V low, 2.0V high. The read/write cycle is 3.9µs.

Dimensions

The dimensions for the NT1X77AA card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 28 mm (1.1 in.)

Power requirements

The power requirements for the NT1X77AA appear in the following table.

Power requirements

	Voltage	Current
Static RAM	+5 V	1.0 A
Dynamic RAM	+5 V	1.0 A
Miscellaneous	+12 V	0.5 A
Miscellaneous	-15 V	10.0 mA

The total 48V power consumption is 11W for the dynamic RAM and 5W for the static RAM.

NT1X78AA

Product description

The NT1X78AA power converter (+5V, -5V, -12V, +24V) card provides regulated and protected power supplies for the disk drive unit (DDU) in DMS-100 equipment.

The card provides +5V, -5V, -12V and +24V power supplies and operates with the NT0X28AL input/output equipment frame supervisory panel (FSP). The input/output controller (IOC) shelf controls the DDU and the FSP.

Location

The card is in the IOC shelf.

Functional description

The NY1X78AA receives a nominal -48V power supply from the office battery. The card provides output voltages of +5V, -5V, -12V and +24V for the DDU. The card regulates the voltages and sends an alarm signal to the FSP when detection of an overvoltage or undervoltage condition occurs.

Functional blocks

The NT1X78AA has the functional blocks that follow:

- input filter
- control circuit supply
- oscillator
- +24 V power switch
- +24 V driver
- +24 V current limiter
- +24 V voltage control
- +24 V output filter
- +5/-12/-5 V power switch
- +5/-12/-5 V driver
- +5/-12/-5 V current limiter
- +5/-12/-5 V voltage control
- +5/-12/-5 V filter circuits
- -12 V regulator
- -5 V regulator

NT1X78AA (continued)

- overvoltage/undervoltage (OV/UV) detector
- relay

Input filter

The input filter performs the following:

- receives the nominal -48V power supply from the office battery
- sends the power to the +24V power switch and the +5/-12/-5V power switch

Control circuit supply

This circuit provides low-voltage power to the circuits that control the two power switches and to the monitor circuits.

Oscillator

The oscillator produces a 32 kHz signal. The voltage control circuits modify the signal. The drive circuits amplify the signal to turn power switches ON and OFF. The converter DRIVE signal from the frame supervisory panel (FSP) activates or deactivates the oscillator.

+24V power switch

The +24V power switch chops the input dc voltage to a rectangular waveform. The waveform is applied across the primary windings of a transformer. The voltage is stepped down. This process causes a lower-voltage rectangular wave across the secondary windings. The secondary voltage is rectified and fed into the +24V output filter.

+24V driver

The +24V driver circuit amplifies the signals from the oscillator and the +24V control circuit. This process makes sure the power switch turns ON and OFF efficiently.

+24V current limiter

The current limit circuit receives a voltage signal proportional to the current in the +24V power switch. If the current is often or always above a specified threshold, the control circuit modifies the input to the driver. This process reduces the duty cycle of the power switch and reduces the power delivered to the +24V output. This circuit ignores instant transient overcurrent conditions.

+24 V voltage control

The following procedure controls the +24 V voltage:

- a sample of the voltage is compared to an internal reference
- the duty cycle of the signal to the +24 V driver that maintains the output voltage at the required level is adjusted

+24 V output filter

The rectified output of the +24 V power switch feeds to a low-pass filter. This process removes the ac ripple and the noise the switching action generates. A sample of this output feeds back to the +24V control circuit to provide regulation. This output also connects to a test jack on the front panel of the power converter through a protective resistor.

+5/-12/-5 V power switch

The +5/-12/-5 V power switch chops the input dc voltage to a rectangular waveform applied across the primary windings of a transformer. The voltage is stepped down. This process produces a lower-voltage rectangular wave across the secondary windings. The system rectifies these secondary voltages and feeds the voltages to the output filters and rectifiers.

+5/-12/-5V driver

The driver circuit amplifies the signals from the oscillator and the +5/-12/-5 V control circuit. This process makes sure the power switch is turned ON and OFF efficiently.

+5/-12/-5 V current limiter

The current limit circuit receives a voltage signal proportional to the current in the +5/-12/-5 V power switch. If the current is often or always above a specified threshold, the control circuit modifies the input to the driver. This modification reduces the duty cycle of the power switch and reduces power delivered to the outputs. This circuit ignores instant transient overcurrent conditions.

+5/-12/-5 V voltage control

The following procedure controls the +5 V output:

- a sample of the voltage is compared to an internal reference
- the duty cycle of the signal to the +5/-12/-5 V driver which maintains output voltage at the required level is adjusted

+5/-12/-5 V filter circuits

The rectified outputs of the +5/-12/-5 V power switch feed to low-pass filters. This process removes the ac ripple and the noise the switching action

NT1X78AA (continued)

generates. A sample of the +5V output feeds back to the +5/-12/-5V control circuit to provide regulation. This output also connects to a test jack on the front panel of the power converter through a protective resistor.

-12 V regulator

The -12 V unregulated output of the +5/-12/-5 V filter feeds to a post-regulator circuit. The circuit reduces the variation on this output to the required tolerance and filters the -12V output. This -12V regulator provides current limiting of this output. This output connects to a test jack on the front panel of the power converter through a protective resistor.

-5 V regulator

The -5 V unregulated output of the +5/-12/-5 V filter feeds to a post-regulator circuit. The circuit reduces the variation on this output to the required tolerance and filters the -5V output. The -5V regulator also provides current limiting of this output. This output connects to a test jack on the front panel of the power converter through a protective resistor.

OV/UV detector

The OV/UV detector circuit detects overvoltage and undervoltage currents. After an appropriate delay that makes sure the detection is real, the circuit deactivates relay K1. This process allows the circuit to send an alarm to the FSP. The signal shuts down the operation of the power converter and lights the light-emitting diode (LED) on the faceplate.

Relay

The card contains one relay to send alarm information to the FSP. The following table lists the alarm and the operated and released functions.

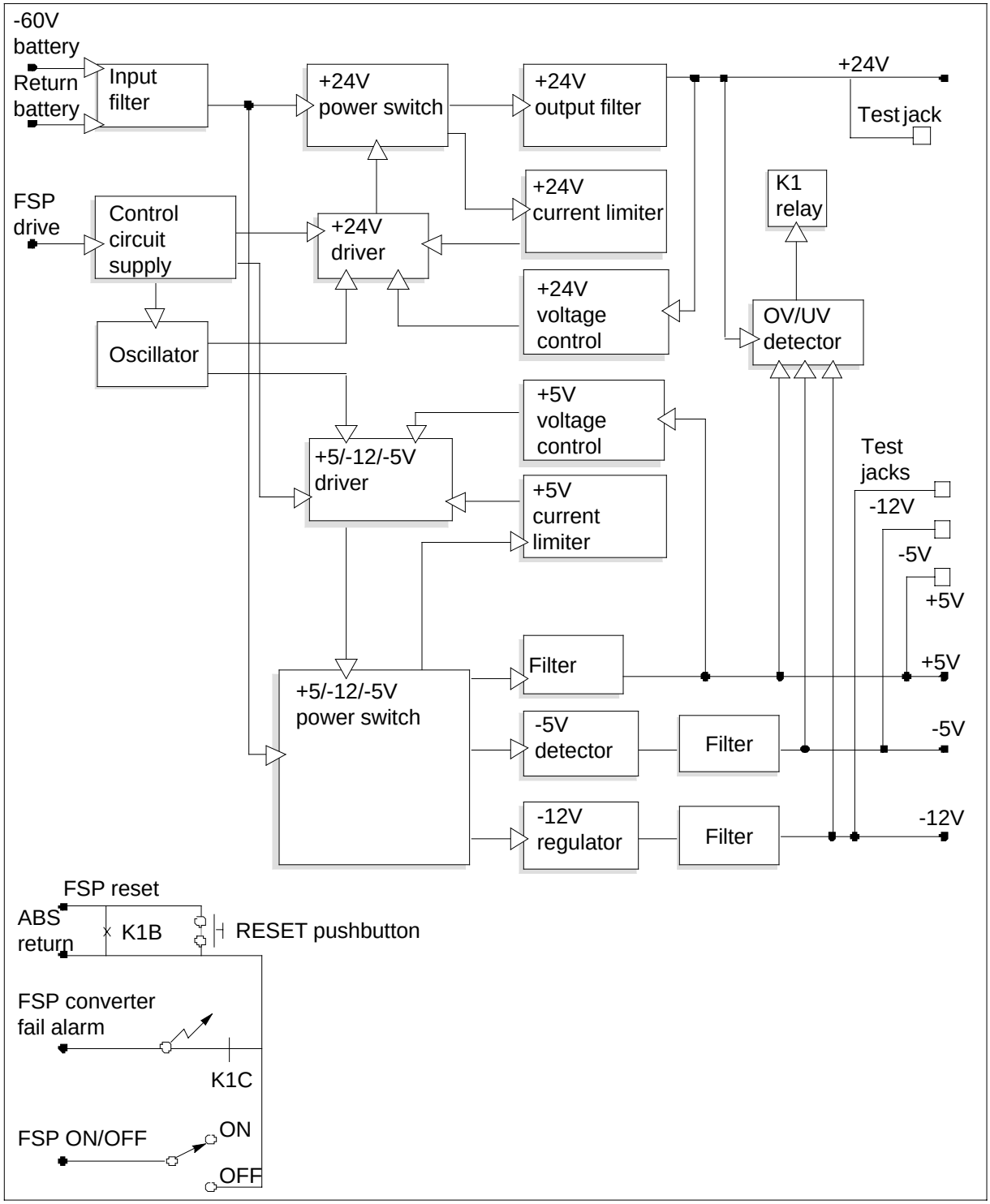
Relay operation

Relay	Operated	Released
K1	Normal operation with contact K1C open and contact K1B closed.	Contact K1C closes, contact K1B opens. The alarm battery supply (ABS) is placed on the FSP converter fail output and the fail LED of the converter is on. The FSP reset to ABS return breaks. This process causes the FSP to shut down the converter.

The relationship between the functional blocks appears in the following figure.

NT1X78AA (continued)

NT1X78AA functional blocks



NT1X78AA (continued)

Technical data

The card has a total power output of 140 W for continuous power and 200W for 1 min at 6.5 A. The following table lists the output specifications for the +24 V output.

Output specifications +24 V

Characteristic	Value
Nominal voltage	+23.6 V
Regulation	-4%
Overvoltage shutdown	+26.0 V ±5%
Undervoltage alarm indication	+19.2 V
Ripple	100m V peak to peak 35m V rms
Current	5.0 A maximum 7.0 A maximum for 1 min 1.0 A minimum
Overcurrent limiting	10.0 A maximum 7.0 A minimum

The output specifications for the +5 V output appear in the following table.

Output specifications +5V (Sheet 1 of 2)

Characteristic	Value
Nominal voltage	+5.0 V
Regulation	±3%
Overvoltage shutdown	+6.0 V ±8%
Undervoltage alarm indication	+4.1 V
Ripple	50 mV peak to peak 20 mV rms

Output specifications +5V (Sheet 2 of 2)

Characteristic	Value
Current	6.0 A maximum 1.0 A minimum
Overcurrent limiting	10.0 A maximum 7.0 A minimum

The output specifications for the -5 V output appear in the following table.

Output specifications -5 V

Characteristic	Value
Nominal voltage	-5.0 V
Regulation	±5%
Overvoltage shutdown	-6.5 V ±8%
Undervoltage alarm indication	-3.2 V
Ripple	50 mV peak to peak 15 mV rms
Current	2.0 A maximum 0.0 A minimum
Overcurrent limiting	5.0 A maximum 3.0 A minimum

The output specifications for the -12 V output appear in the following table.

Output specifications -12 V (Sheet 1 of 2)

Characteristic	Value
Nominal voltage	-12.0 V
Regulation	±5%
Overvoltage shutdown	+15.5 V ±8%
Undervoltage alarm indication	+7.7 V

NT1X78AA (end)

Output specifications -12 V (Sheet 2 of 2)

Characteristic	Value
Ripple	25 mV peak to peak
	15 mV rms
Current	0.9 A maximum
	0.0 A minimum
Overcurrent limiting	2.0 A maximum
	1.0 A minimum

Dimensions

The dimensions for the NT1X78AA are as follows:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.2 in.)
- width: 66 mm (2.6 in.)

Power requirements

The input voltage range is -42V to -56 V. The power requirements for the NT1X78AAappear in the following table.

Power requirements

Voltage	Current
-48 V nominal	3.2 A

The maximum heat dissipation is 70W.

NT1X78KA

Product description

The NT1X78KA power converter card (+5V, -5V, -12V, +24V) provides regulated and protected power supplies for the disk drive unit in DMS-100 equipment. This card is the -60V input version of the NT1X78AA.

The card provides +5V, -5V, -12V and +24V power supplies. The card operates with the NT0X28AL input/output equipment frame supervisory panel (FSP). The input/output controller (IOC) shelf controls the DDU and the FSP.

Location

The card is in the IOC shelf.

Functional description

The NT1X78KA performs the following functions:

- receives a nominal -60V power supply from the office battery
- provides output voltages of +5V, -5V, -12V and +24V for the DDU
- regulates the voltage
- sends an alarm signal to the FSP on detection of an overvoltage or undervoltage condition

Functional blocks

The NT1X78KA has the functional blocks that follow:

- input filter
- control circuit supply
- oscillator
- +24V power switch
- +24V driver
- +24V current limiter
- +24V voltage control
- +24V output filter
- +5/-12/-5V power switch
- +5/-12/-5V driver
- +5/-12/-5V current limiter
- +5/-12/-5V voltage control
- +5/-12/-5V filter circuits

NT1X78KA (continued)

- -12V regulator
- -5V regulator
- overvoltage/undervoltage (OV/UV) detector
- relay

Input filter

The input filter receives the nominal -60V power supply from the office battery. The filter also sends the power to the +24V power switch and the +5/-12/-5V power switch.

Control circuit supply

This circuit provides the low-voltage power to the circuits that control the two power switches and to the monitor circuits.

Oscillator

The oscillator produces a 32 kHz signal. Voltage control circuits modify the signal and drive circuits amplify the signal to turn the power switches ON and OFF. The converter DRIVE signal from the frame supervisory signal (FSP) activates or deactivates the oscillator.

+24V power switch

The +24V power switch chops the input dc voltage to a rectangular waveform applied across the primary windings of a transformer. The voltage is stepped down. This process produces a lower-voltage rectangular waveform applied across the secondary windings. This secondary voltage is rectified and fed into the +24V output filter.

+24V driver

The +24V driver circuit amplifies the signals from the oscillator and the +24V control circuit to make sure the power switch turns ON and OFF efficiently.

+24V current limiter

The current limit circuit receives a voltage signal related to the current in the +24V power switch. If the current is repetitively or continuously above a predetermined threshold, the control circuit modifies the input to the driver. This process reduces the duty cycle of the power switch and lowers the power delivered to the +24V output. This current ignores instant transient overcurrent conditions.

+24V voltage control

The following procedure controls the +24V output:

- a sample of the voltage is compared to an internal reference
- the duty cycle of the signal to the +24V driver that maintains the output voltage at the required level is adjusted

+24V output filter

The rectified output of the +24V power switch feeds to a low-pass filter. This process removes the ac ripple and the noise that the switch action generates. A sample of this output feeds back to the +24V control circuit to provide regulation. This output connects to a test jack on the front panel of the power converter through a protective resistor.

+5/-12/-5V power switch

The +5/-12/-5V power switch chops the input dc voltage to a rectangular waveform. The waveform is applied across the primary windings of a transformer. The voltage is stepped down, which produces a lower-voltage rectangular waveform applied across the secondary windings. These secondary voltages are rectified and fed into the various output filters and rectifiers.

+5/-12/-5V driver

The driver circuit amplifies the signals from the oscillator and the +5/-12/-5V control circuit to make sure the power switch turns ON and OFF efficiently.

+5/-12/-5V current limiter

The current limit circuit receives a voltage signal proportional to the current in the +5/-12/-5V power switch. If the current is often or always above a specified threshold, the control circuit modifies the input to the driver. This process reduces the duty cycle of the power switch and lowers the power delivered to the outputs. This circuit ignores instant transient overcurrent conditions.

+5/-12/-5V voltage control

The following process controls the +5V output:

- a sample of the voltage is compared to an internal reference
- the duty cycle of the signal to the +5/-12/-5V driver is adjusted

This procedure maintains the output voltage at the required level.

+5/-12/-5V filter circuits

The rectified outputs of the +5/-12/-5V power switch feed to low-pass filters. This process removes the ac ripple and the noise that the switch action

NT1X78KA (continued)

generates. A sample of the +5V output is fed back to the +5/-12/-5V control circuit to provide regulation. This output connects to a test jack on the front panel of the power converter through a protective resistor.

-12V regulator

The -12V unregulated output of the +5/-12/-5V filter feeds to a post-regulator circuit. This process reduces the variation on this output to the required tolerance and filters the -12V output. This -12V regulator also provides current limiting of this output. This output connects to a test jack on the front panel of the power converter through a protective resistor.

-5 V regulator

The -5V unregulated output of the +5/-12/-5V filter feeds to a post-regulator circuit. This process reduces the variation on this output to the required tolerance and filters the -5V output. This -5V regulator also provides current limiting of this output. This output connects to a test jack on the front panel of the power converter through a protective resistor.

OV/UV detector

The OV/UV circuit detects overvoltage and undervoltage currents. The circuit deactivates relay K1 to send an alarm signal to the FSP. To make sure the alarm detection is real, the circuit only sends the alarm signal after an appropriate delay. This signal shuts down the operation of the power converter and lights the light-emitting diode (LED) on the faceplate.

Relay

The card contains one relay to send alarm information to the FSP. The operated and released functions of relay K1 appear in the following table.

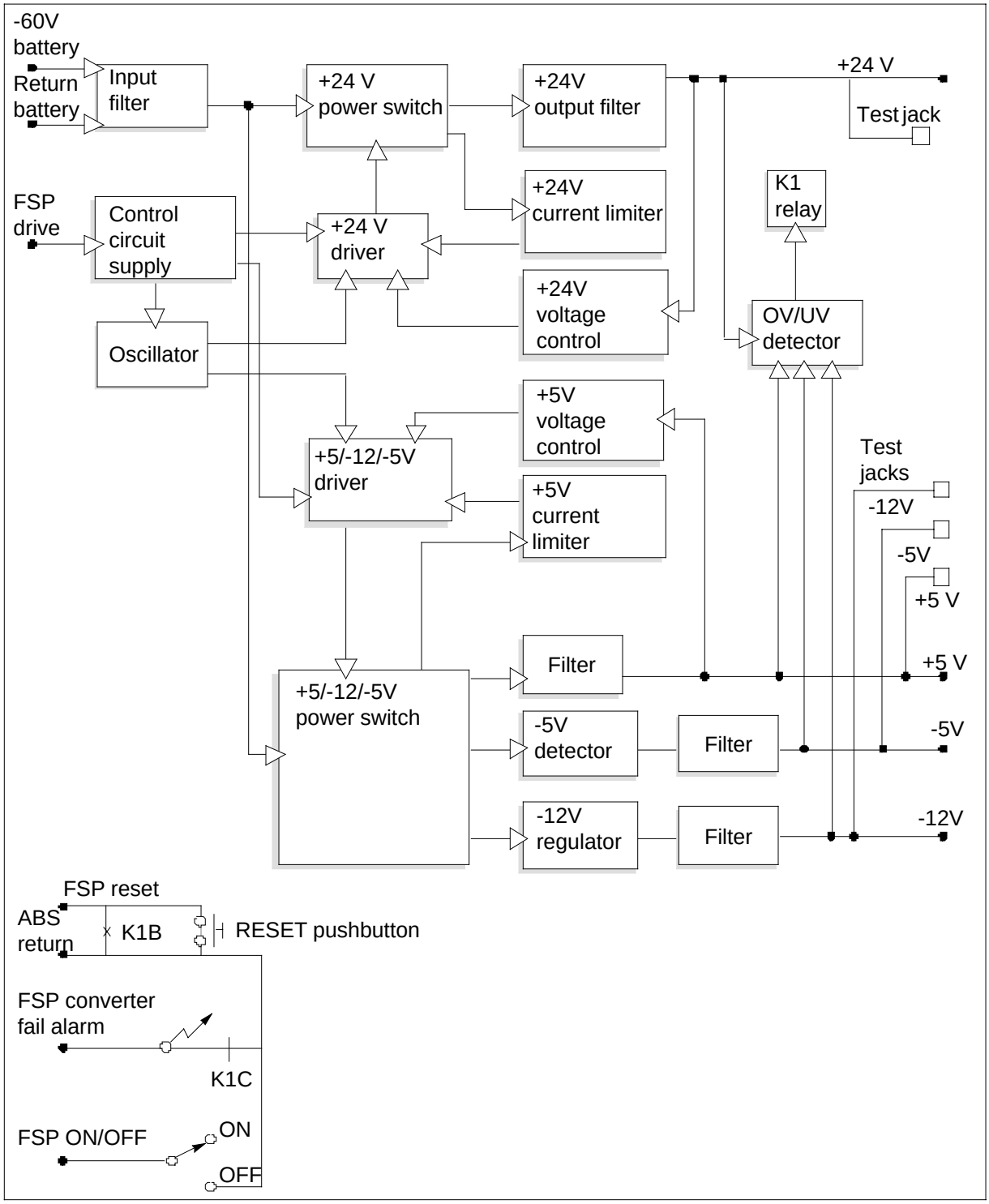
Relay operation

Relay	Operated	Released
K1	Normal operation with contact K1C open and contact K1B closed.	Contact K1C closes, contact K1B opens. The alarm battery supply (ABS) is placed on the FSP converter fail output and the fail LED of the converter is on. The FSP reset to ABS return breaks. The break causes the FSP to shut down the converter.

The relationship between the functional blocks appears in the following figure.

NT1X78KA (continued)

NT1X78KA functional blocks



NT1X78KA (continued)

Technical data

The card has a total power output of 140W for continuous power and 200W for 1 min at 6.5A. The output specifications for the +24V output appear in the following table.

Output specifications +24 V

Characteristic	Value
Nominal voltage	+23.6V
Regulation	-4%
Overvoltage shutdown	+26.0 V ±5%
Undervoltage alarm indication	+19.2V
Ripple	100mV peak to peak 35mV rms
Current	5.0A maximum 7.0A maximum for 1 min 1.0A minimum
Overcurrent limiting	10.0A maximum 7.0A minimum

The output specifications for the +5V output appear in the following table.

Output specifications +5 V (Sheet 1 of 2)

Characteristic	Value
Nominal voltage	+5.0 V
Regulation	±3%
Overvoltage shutdown	+6.0 V ±8%
Undervoltage alarm indication	+4.1V
Ripple	50mV peak to peak 20mV rms

Output specifications +5 V (Sheet 2 of 2)

Characteristic	Value
Current	6.0A maximum 1.0A minimum
Overcurrent limiting	10.0A maximum 6.0A minimum

The output specifications for the -5V output appear in the following table.

Output specifications -5 V

Characteristic	Value
Nominal voltage	-5.0V
Regulation	±5%
Overvoltage shutdown	-6.5V ±8%
Undervoltage alarm indication	-3.2V
Ripple	50mV peak to peak 15mV rms
Current	2.0A maximum 0.0A minimum
Overcurrent limiting	5.0A maximum 3.0A minimum

The output specifications for the -12V output appear in the following table.

Output specifications -12 V (Sheet 1 of 2)

Characteristic	Value
Nominal voltage	-12.0V
Regulation	±5%
Overvoltage shutdown	+15.5 V ±8%
Undervoltage alarm indication	+7.7 V

NT1X78KA (end)

Output specifications -12 V (Sheet 2 of 2)

Characteristic	Value
Ripple	25mV peak to peak
	15mV rms
Current	0.9A maximum
	0.0A minimum
Overcurrent limiting	2.0A maximum
	1.0A minimum

Dimensions

The dimensions for the NT1X78KA are as follows:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.2 in.)
- width: 66 mm (2.6 in.)

Power requirements

The input voltage range is -52V to -72V. The power requirements for the NT1X78KA appear in the following table.

Power requirements

Voltage	Current
-60 V nominal	3.2 A

The maximum heat distribution is 70W.

NT1X79AA

Product description

The NT1X79AA digital recorded announcement electrically erase PROM (EEPROM) card is part of the digital recorded announcement (DRA) hardware. The hardware includes the following components:

- speech processor
- microprocessor controller
- permanent speech memory
- volatile recordable speech memory
- nonvolatile recordable speech memory

The NT1X79AA card provides the nonvolatile recordable speech memory with an EEPROM. The EEPROM stores a maximum of 32 s of speech or tones.

Location

The card is in one card position in a maintenance trunk module (MTM). The card can use MTM card positions 6 through 14.

Functional description

The NT1X79AA provides 128 kbytes of recordable memory. A menu, silence, test tones, prompt tones, and special information tones use 4 kbytes of the memory. Recording speech samples use the memory that remains. The speech is recorded in 31 segments of 1.024 s each. Each recording can be several seconds long. Very long announcements contains recordings strung together. Each shelf can hold a maximum of eight cards. A total of 253.9 s of speech is available to the DRA equipment.

Operating blocks

The NT1X79AA has the following operating blocks:

- speech block
- subphrase
- phrase
- announcement
- submenu
- menu
- virtual card

NT1X79AA (continued)

Speech block

A speech block is a single unit of recorded speech that is 32 ms long. Each recording consists of several blocks strung together.

Subphrase

A subphrase is the smallest unit of speech that the DRA equipment plays. Subphrases consist of from one through 255 speech blocks. Subphrases are normally recordings like we are sorry or the number you have dialed.

Phrase

A phrase is a digital recording that consists of a group of subphrases. Phrases are not complete messages. Phrases are building blocks used to create the messages. A single card must contain each phrase.

Announcement

An announcement consists of phrases that form a complete recording that plays to a customer. The central control (CC) identifies the announcement that plays and sends the list of phrases for the announcement to the DRA. The phrases an announcement contains can be on different cards.

Submenu

The submenu contains entries for each subphrase that identify the address of the subphrase. The entries also identify the number of times the subphrase repeats.

Menu

The menu contains entries that identify the subphrases in each phrase. Each menu entry contains a list of submenu entries that must play to create the selected phrase.

Virtual card

A virtual card is an NT1X79AA card that the DRA equipment identifies. You must set each card that contains a small switch to the virtual card ID. This condition allows the DRA to identify the card. You must set the switch to the

blocklist number in the BLKLIST parameter in the CARDINFO field in Table DRAMS. The following table lists the blocklist switch settings.

Blocklist switch settings

Switch position	Blocklist number							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
1	down	down	down	down	up	up	up	up
2	down	down	up	up	down	down	up	up
3	down	up	down	up	down	up	down	up

Technical data

The NT1X79AA provides signal levels of 0.8V low and 2.0V high. The read/write cycle is 3.9 µs.

Physical dimensions

The dimensions for the NT1X79AA circuit card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)

Power requirements

The power requirements for the NT1X79AA are a voltage of +5V and current of 1.0A.

NT1X80AA

Product description

The improved digital recorded announcement machine card (EDRAM) provides voice messages to the user. The NT1X80AA provides 4.3 min of announcement time and 30 announcement channels.

Location

The NT1X80AA is positioned as a peripheral module (PM) to the DMS. The card is in a provisional trunk slot of the maintenance trunk module (MTM). The card has a DS30 link and connects to the network with a direct cable.

Functional description

Functional blocks

The NT1X80AA has the following functional blocks:

- processor block
- address select decoding
- static RAM (SRAM) and EPROM
- dynamic RAM (DRAM)
- dual port registers
- dual port buffers
- central control (CC) interface

Processor block

The processor block contains a Motorola 68000 16-bit microprocessor that runs on a 12.5 MHz clock. This clock generates from a 25 MHz local oscillator. This block contains bus interface circuits that handle bus direction control. This block also contains circuits that handle bus buffering and decoding of bus signals.

The processor block includes interrupt controller circuits that provide seven levels of prioritized interrupts to the microprocessor. This block also includes power-up reset circuits that generate a pulse to reset the microprocessor.

Address select decoding

The following are the main functions of the address select decoding block:

- generates the DTACK signal
- provides address select decoding
- provides timing multiplex synchronization with dual port memory

SRAM and EPROM

This block contains 32 kwords of SRAM and 64 kwords of EPROM. The SRAM provides storage for the program, data, memory pool and stacks. The EPROM holds the bootstrap loader, OS kernel, monitor, and other debugging utilities.

DRAM

The DRAM block contains dynamic memory that stores the announcement data. The system downloads announcement data from the CC through the DS30 link or the data generates on site. This block includes memory refresh circuits that provide a hidden refresh cycle when the DRAM is not accessed.

Dual port registers

The dual port registers provide an interface between the processor and the MTM hardware. The processor and the QMV88AV trunk module (TM) controller chip provide access to this block.

The registers contains the following four pages that have 256 elements:

- trunk message
- network message
- integrity message
- connection page

Dual port buffers

The processor and the QMV88AV chip provide access to the dual port buffers. The processor can access and process the speech channel pulse code modulation (PCM) data only with the PCM buffer.

CC interface

The CC interface block handles all control and interface with the DS30 link. This block contains the DS30 interface and the trunk module controller chip.

The DS30 interface block includes an NT5L67AA hybrid that provides the physical layer interface with the DS30 link. The N03 DS30 link ASIC drives the DS30 interface block. The N03 DS30 performs functions like DS30 clock recovery, frame pulse detection, and elastic buffering.

The TM controller block contains the QMV88AV TM controller chip. This chip receives and decodes the central processor-side (C-side) DS30 data from the DS30 interface. The chip also extracts the network message data, and stores the data in the MTM dual port registers. The chip sends PCM data to the dual port buffer with the serial bus. For peripheral module-side (P-side) data,

NT1X80AA (continued)

the chip reads the PCM data in the dual port registers. The chip also reads the PCM data in the dual port buffers. The chip converts the data to the correct format and sends the data to the CC with the DS30 interface.

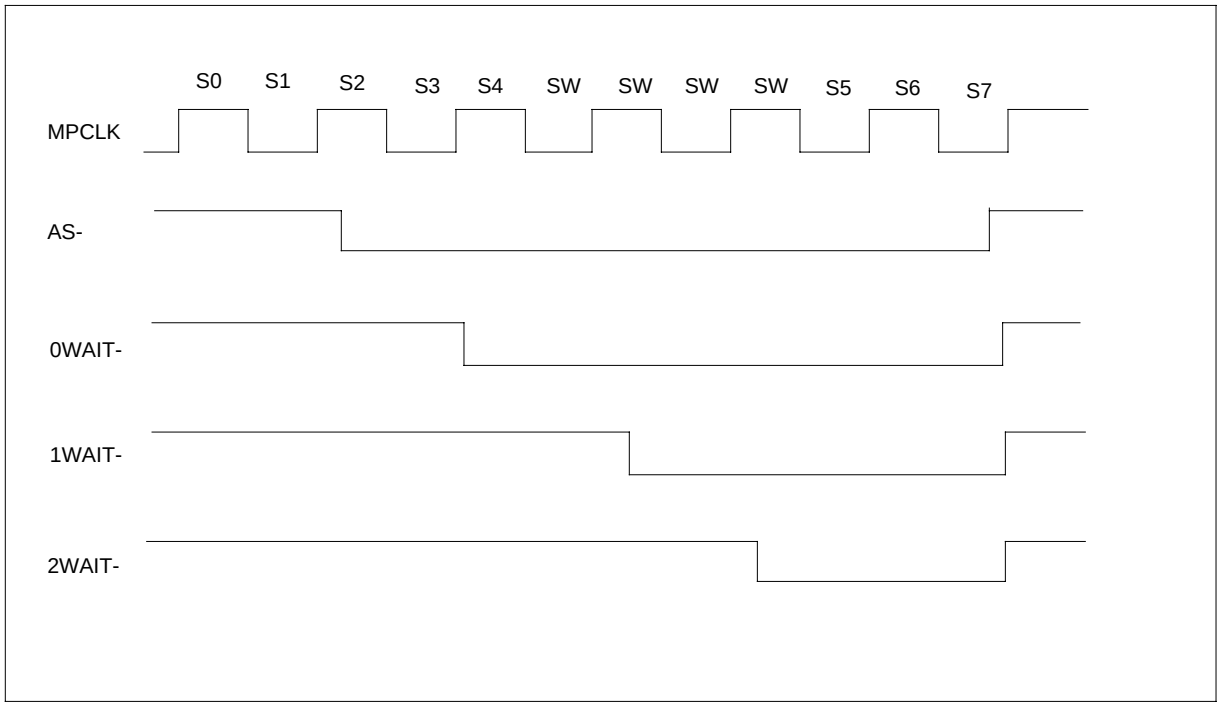
The QMV88AV chip also generates accuracy interrupts if accuracy mismatch or trunk interrupts occur. Trunk interrupts occur if any trunk timer expires.

Signaling

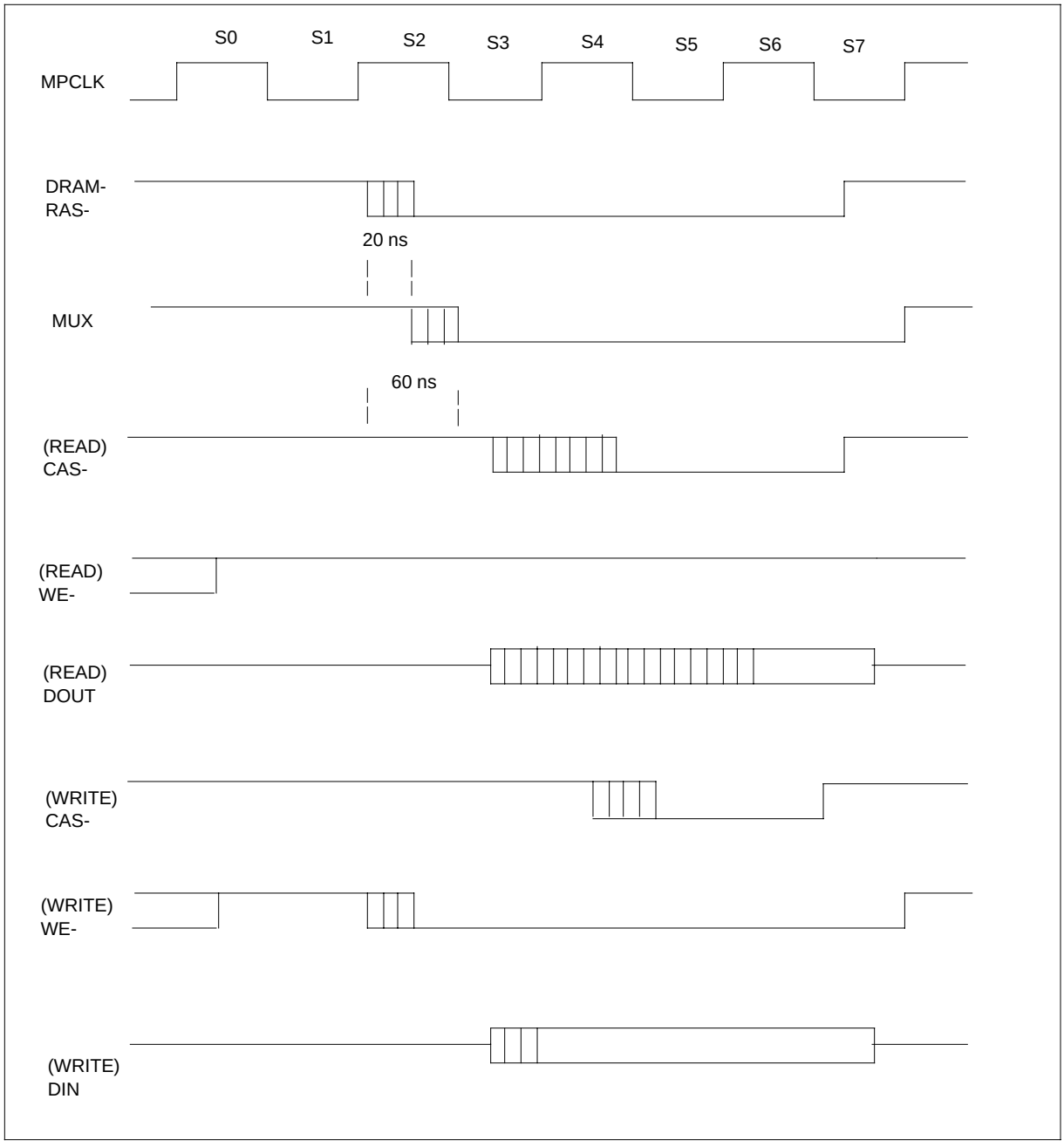
Timing

The following figures show the timing for the NT1X80AA.

NT1X80AA WAIT clock timing

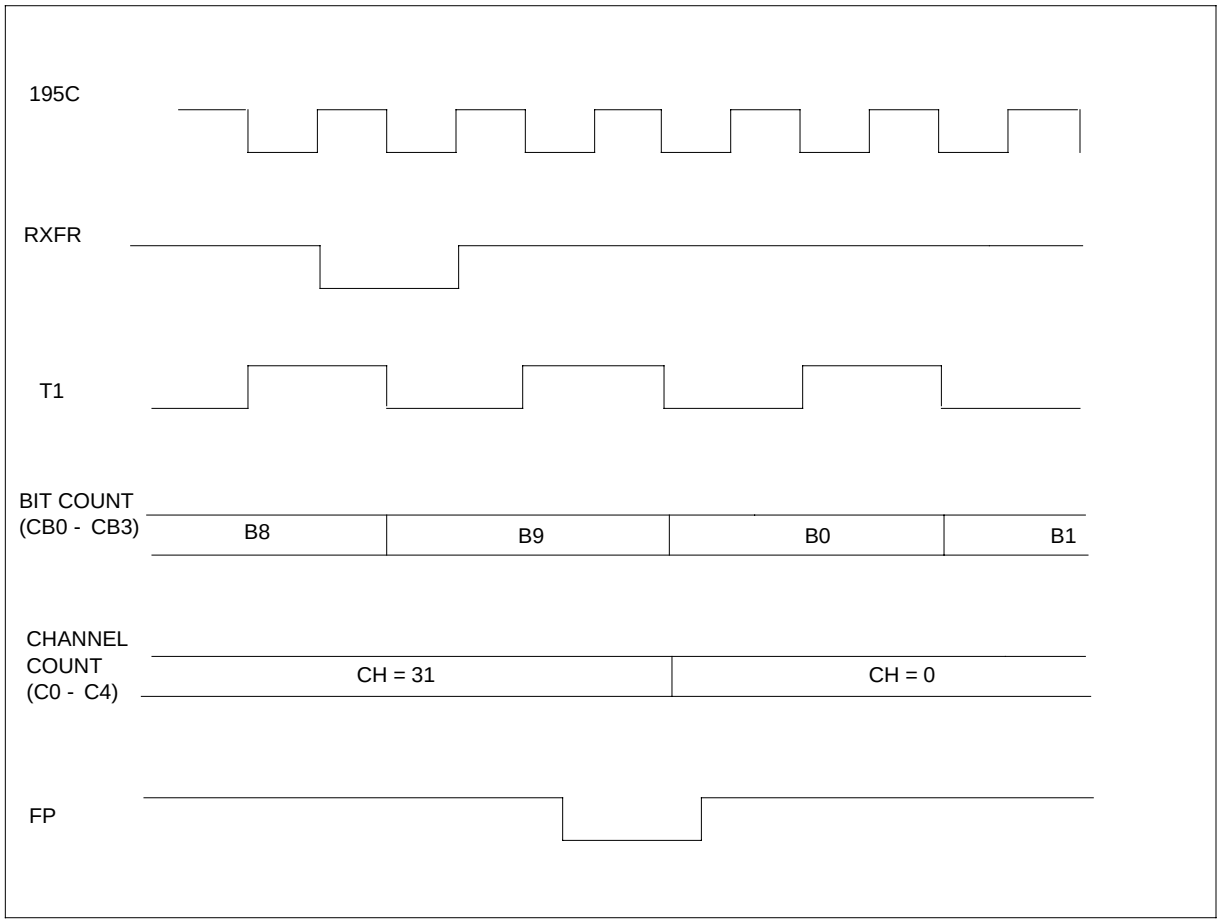


NT1X80AA DRAM access control timing

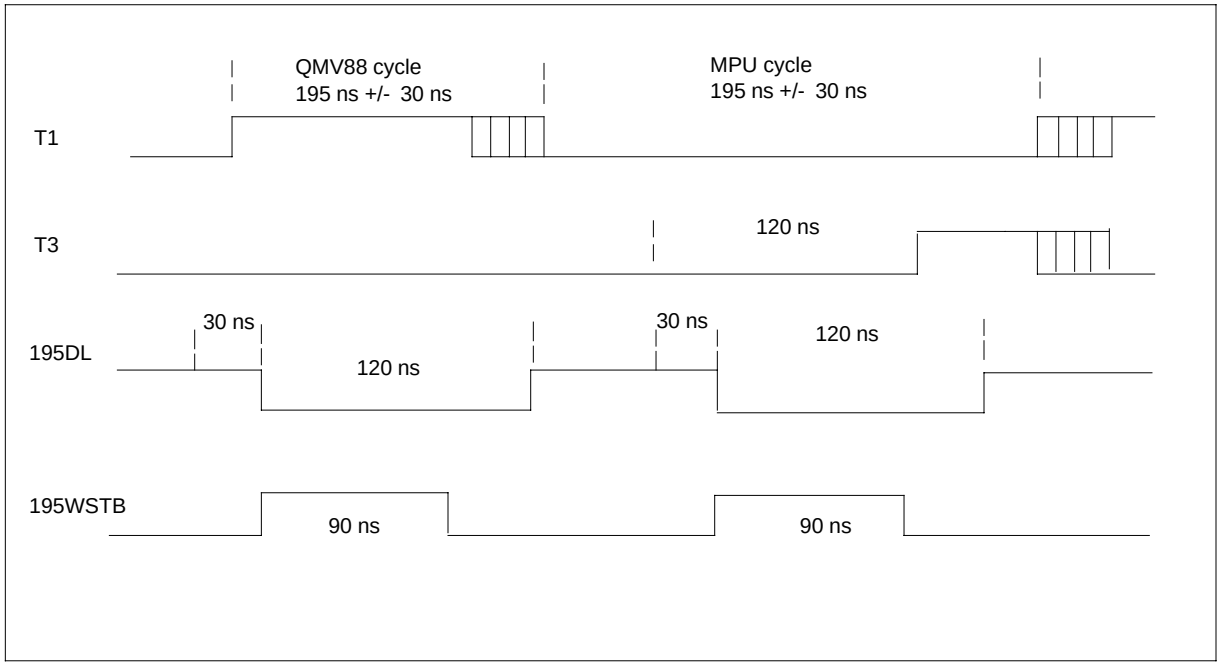


NT1X80AA (continued)

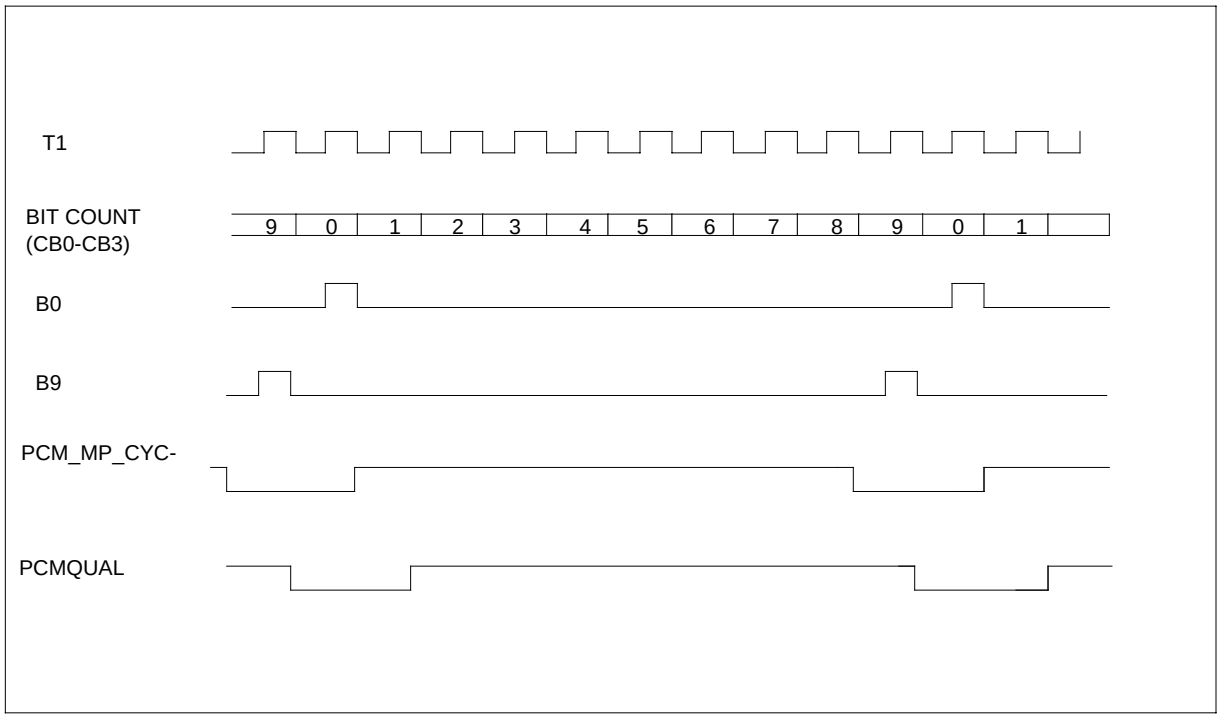
NT1X80AA DS30 link frame pulse timing



NT1X80AA MTM_REG_DPORT access control timing

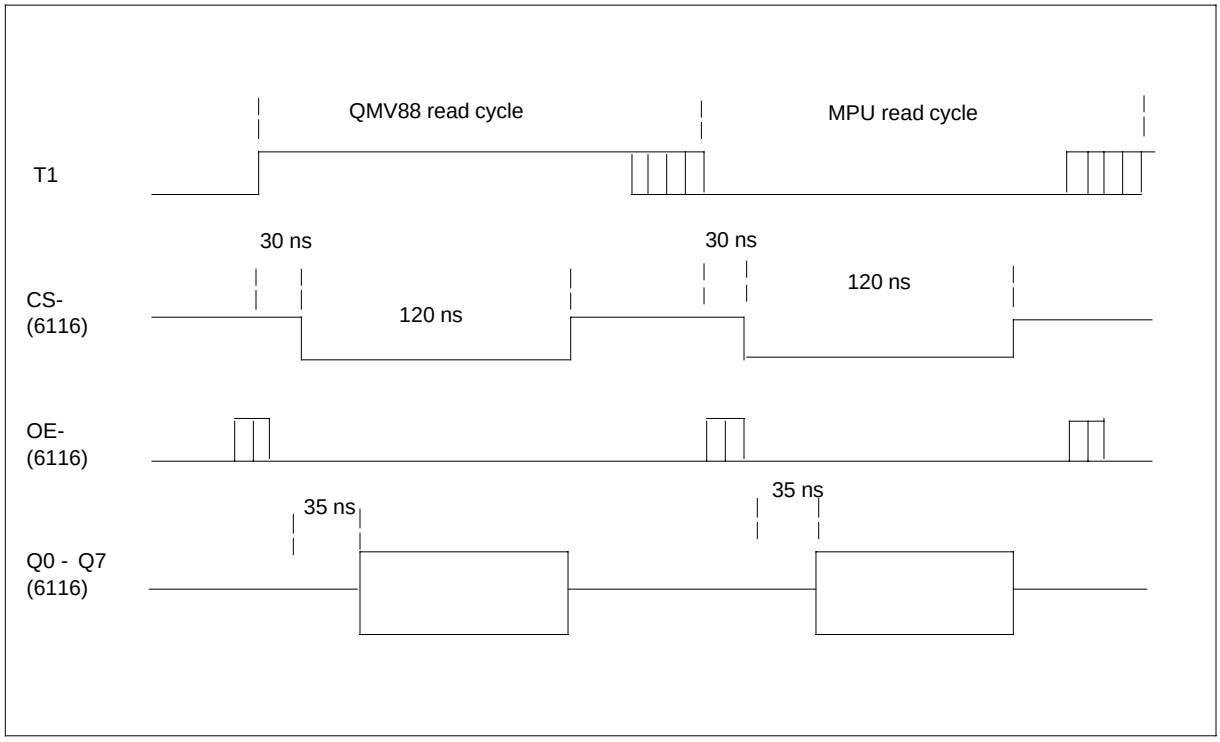


NT1X80AA PCM_BUFFER_DPORT access control timing

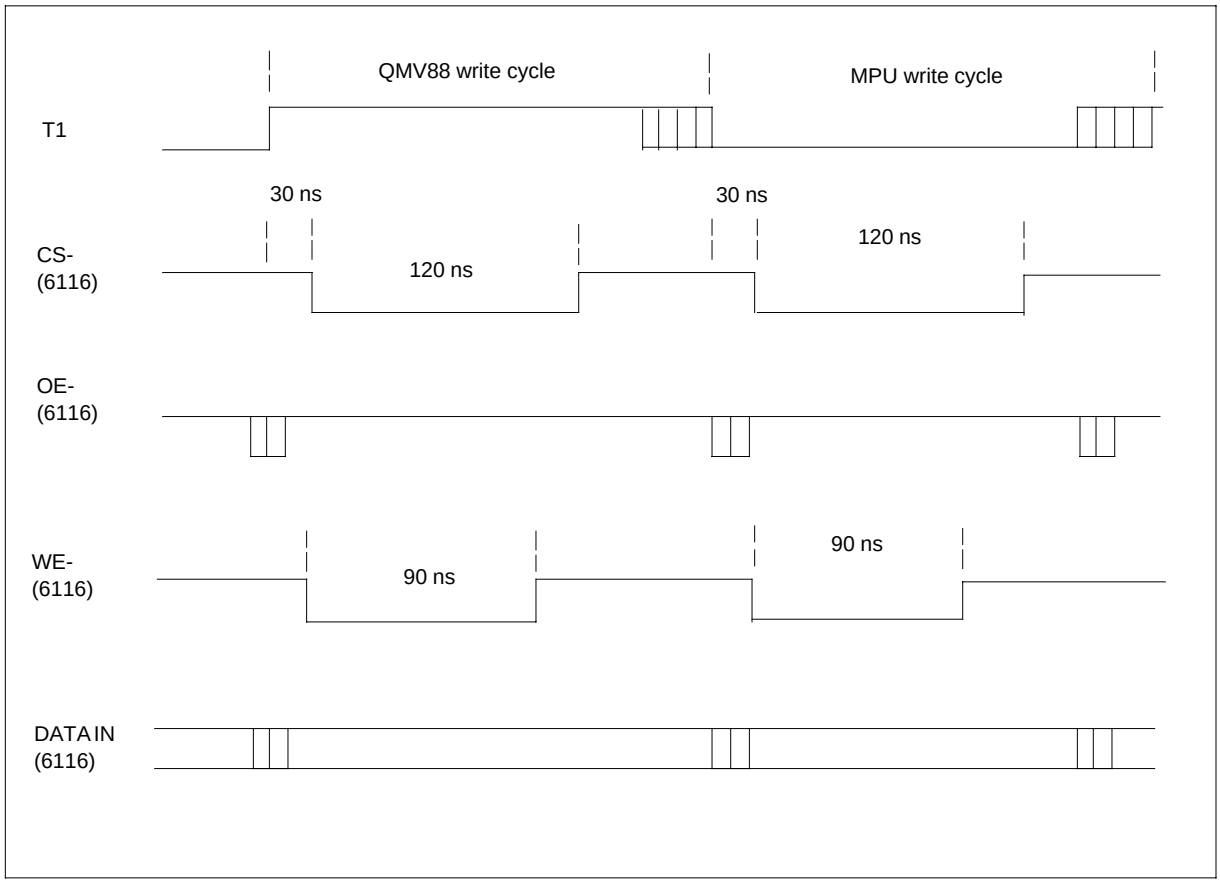


NT1X80AA (continued)

NT1X80AA MTM_REG_DPORT read timing



NT1X80AA MTM_REG_DPORT write timing



Technical data

Power requirements

The minimum supply voltage for the NT1X80AA is 4.5V. The nominal supply voltage is 5V. The maximum supply voltage is 2V. The maximum supply current is 2A.

NT1X80BA

Product description

The improved digital recorded announcement machine card (EDRAM) provides voice messages/instructions to the subscriber. This card reduces the need for operator help. The NTIX80BA provides 16 L.S min of announcement time and 29 announcement channels.

Location

The NTIX80BA is positioned as a peripheral module (PM) to the DMS. The card is in 1 of the 12 trunk slots in a standard MTM/STM/MTM (ISM) shelf. The DS30 cable for EDRAM plugs into the slot pins on the back plane of this shelf.

Functional description

Functional blocks

The NTIX80BA has the following functional blocks:

- processor block
- address select decoding
- static RAM (SRAM) and EPROM
- dynamic RAM (DRAM)
- dual port registers
- dual port buffers
- central control (CC) interface

Processor block

The processor block contains a Motorola 68000 16-bit microprocessor that runs on a 12.5 MHz clock. This clock generates from a 25 MHz local oscillator. This block contains bus interface circuits that handle bus direction control. The bus also controls bus buffering and decoding of bus signals.

The processor block includes interrupt controller circuitry that provides seven levels of prioritized interrupts to the microprocessor. The processor block provides power-up reset circuits that generates a pulse to reset the microprocessor.

Address select decoding

The following are the main functions of the address select decoding block:

- generates the DTACK signal
- provides address select decoding
- provides timing multiplex synchronization with the dual port memory

SRAM and EPROM

This block contains 32K words of SRAM and 64K words of EPROM. The SRAM provides storage for the program, data, memory pool and stacks. The EPROM holds the bootstrap loader, OS kernel, monitor, and other debugging utilities.

DRAM

The DRAM block contains dynamic memory that stores the announcement data. The system downloads the announcement data from the CC through the DS30 link, or the data generates on site. This block also includes memory refresh circuits. This circuits provides a hidden refresh cycle when access to the DRAM does not occur.

Dual port registers

The dual port registers provide an interface between the processor and the MTM hardware. The processor and the FPGA (ACTEL1280) controller chip access this block.

The registers consist of the following four pages and have 256 elements:

- trunk message
- network message
- integrity message
- connection page

Dual port buffers

The processor and the QMV88AV chip access the dual port buffers. The processor can only access and process the speech channel pulse code modulation (PCM) data with the PCM buffer.

CC interface

The CC interface block handles all control and interface with the DS30 link. This block contains the DS30 interface and the trunk module controller chip.

NT1X80BA (continued)

The DS30 interface block includes an NT5L67AA hybrid that provides the physical layer interface with the DS30 link. The N03 DS30 link ASIC drives the DS30 interface block. The N03 DS30 performs functions like DS30 clock recovery, frame pulse detection, and elastic buffering.

The TM controller block contains the QMV88AV TM controller chip. This chip receives and decodes the central processor-side (C-side) DS30 data from the DS30 interface. This chip extracts the network message data and stores the data in the MTM dual port registers. The chip sends the PCM data to the dual port buffer with the serial bus. For peripheral module-side (P-side) data, the chip reads the PCM data in the dual port registers. The chip also reads the PCM data in the dual port buffers. The chip converts the data to the correct format, and sends the data to the CC with the DS30 interface.

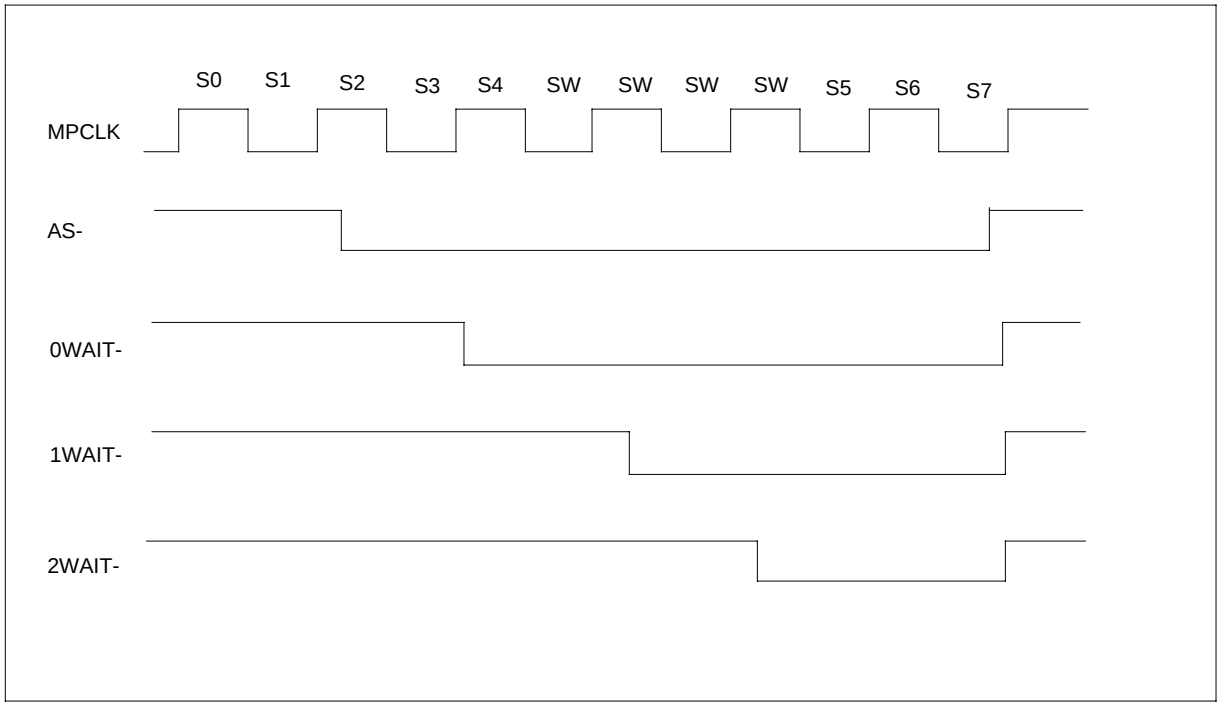
The QMV88AV chip also generates accuracy interrupts if accuracy mismatch, or trunk interrupts occur. Trunk interrupts occur if any trunk timer expires.

Signaling

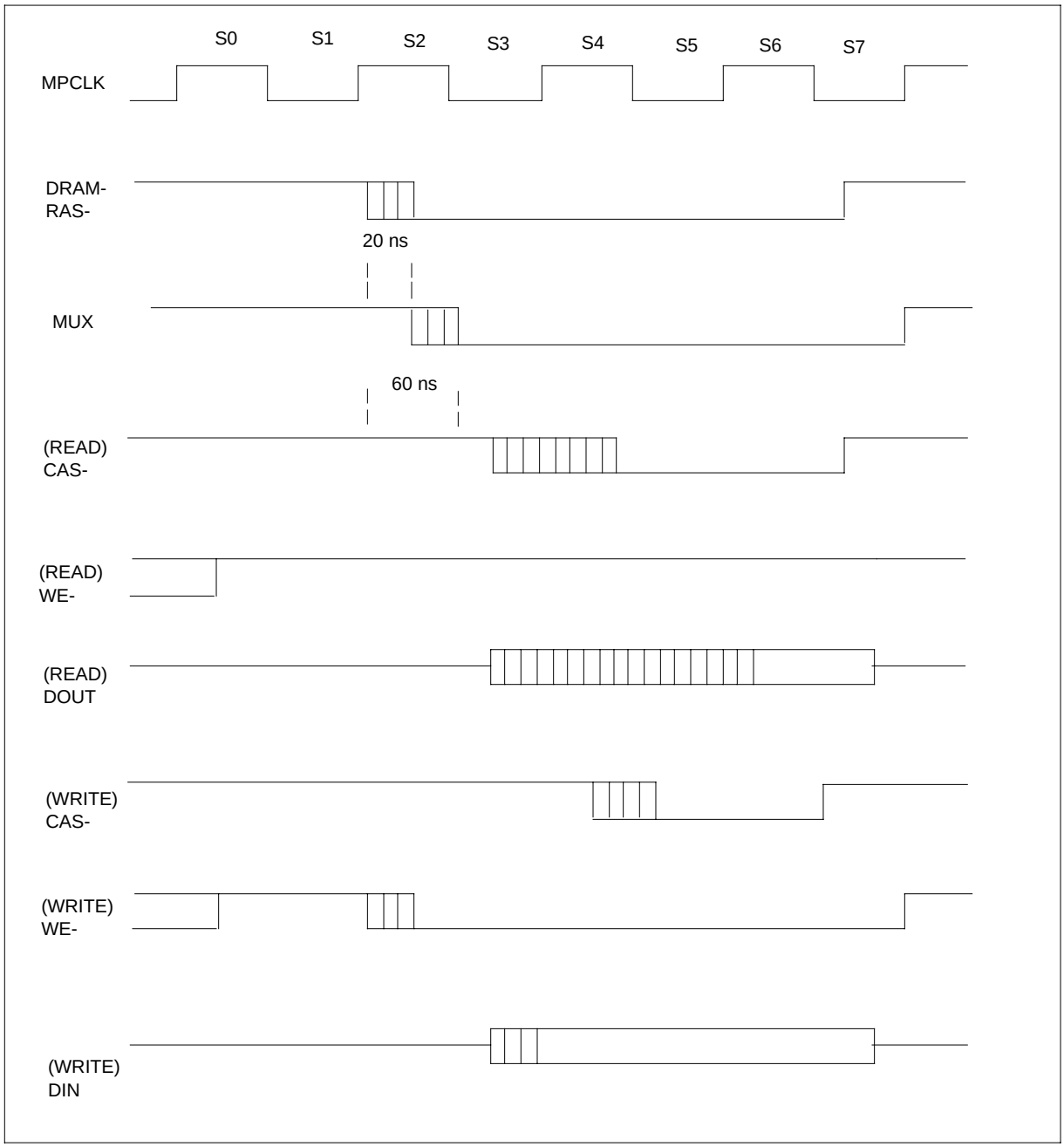
Timing

The following figures show the timing for NTIX80BA

NTIX80BA WAIT clock timing

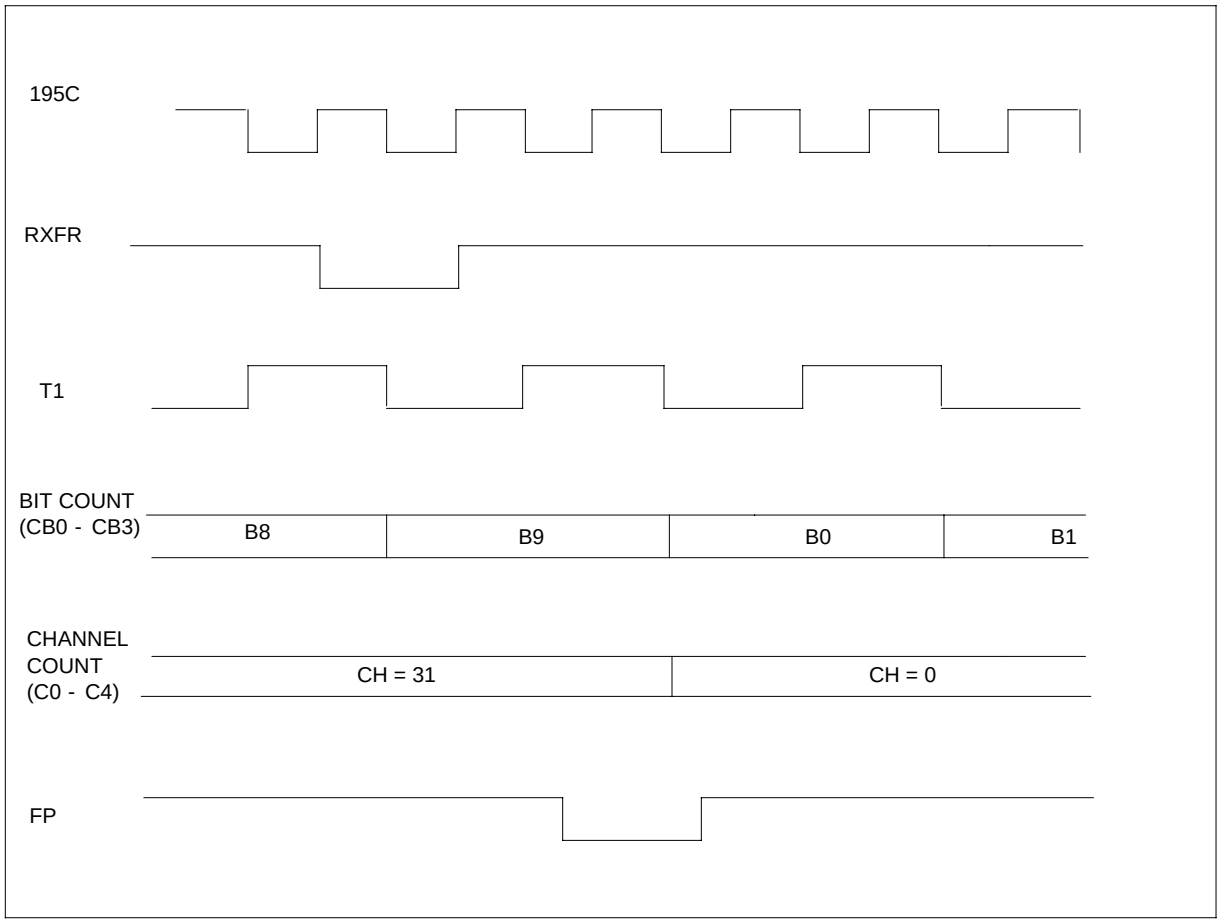


NTIX80BA DRAM access control timing

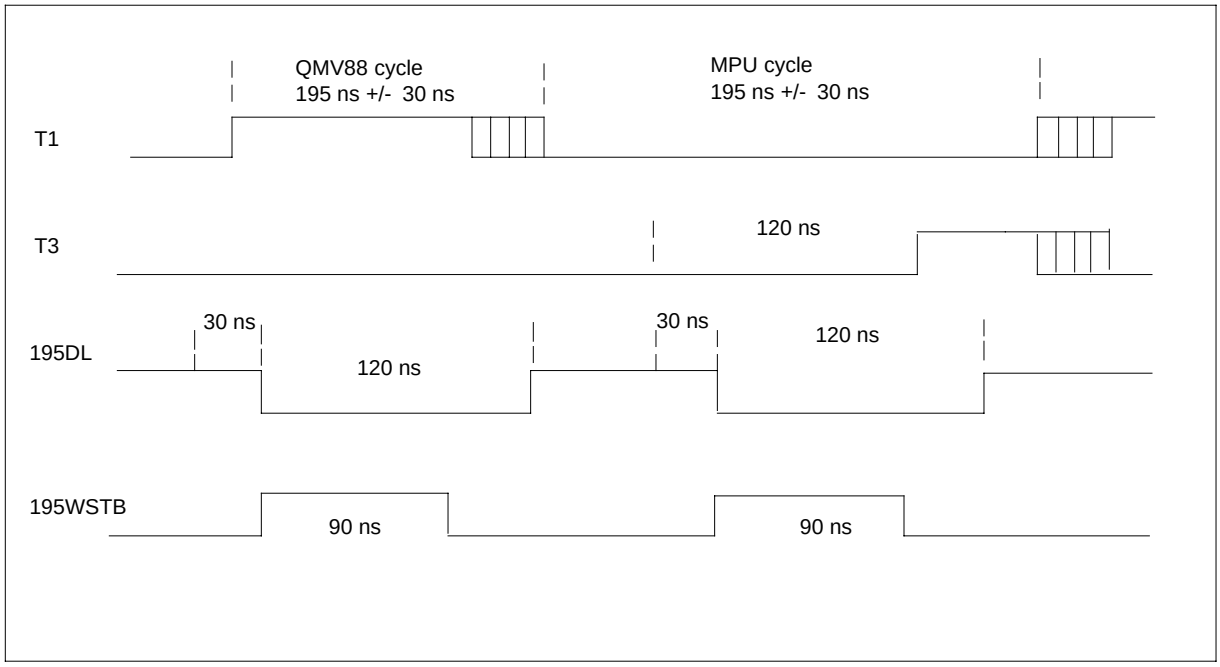


NT1X80BA (continued)

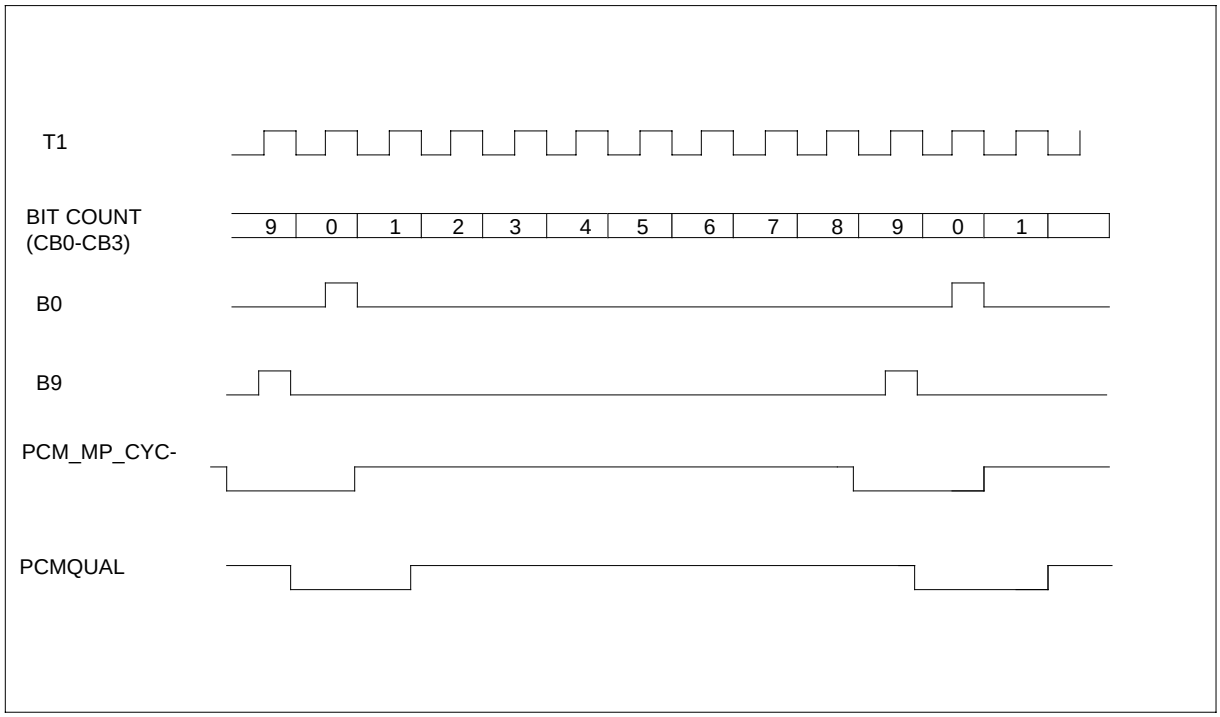
NTIX80BA DS30 link frame pulse timing



NTIX80BA MTM_REG_DPORT access control timing

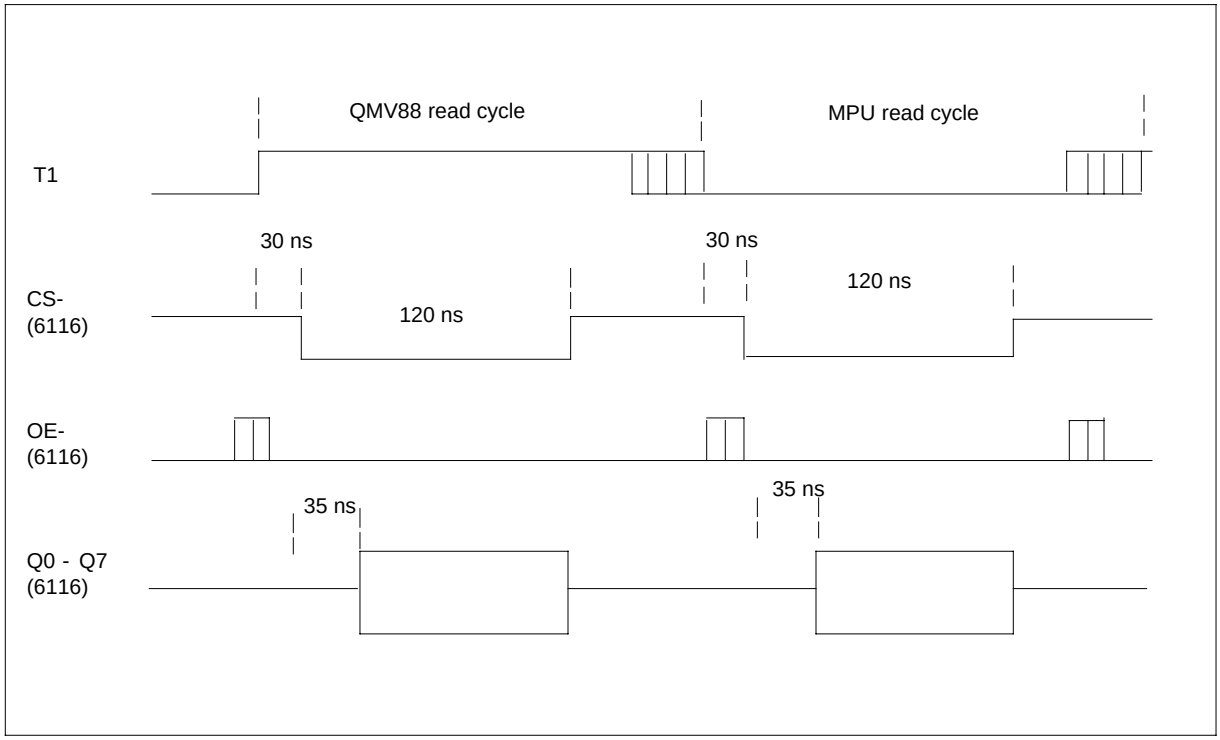


NTIX80BA PCM_BUFFER_DPORT access control timing

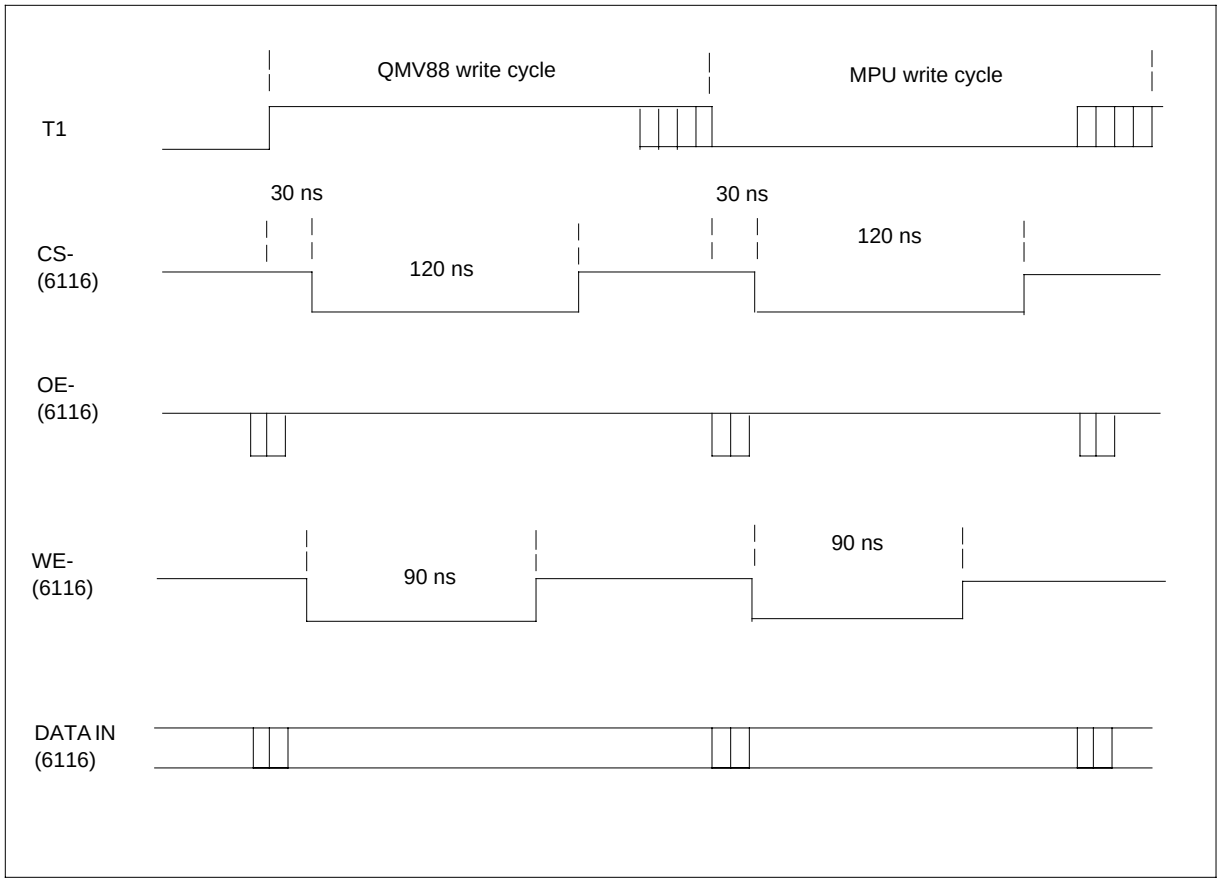


NT1X80BA (continued)

NTIX80BA MTM_REG_DPORT read timing



NTIX80BA MTM_REG_DPORT write timing



Technical data

Power requirements

The minimum supply voltage for the is 4.5V. The nominal supply voltage is 5V and the maximum supply voltage is 2V. The maximum supply current is 2A.

NT1X81AA

Product description

The NT1X81AA conference trunk module (CTM) is a stand alone peripheral module (PM). The NT1X81AA implements five separate, six-port voice conference bridges. The system supports a total of thirty voice channels for conferencing functions.

The NT1X81AA can be provisioned on:

- an STM, with provisional restriction, that an NT2X70 converter pack powers
- an MTM, with a maximum of 12 CTMs for each shelf, powered from an on-board power supply
- an ISM, with a maximum of 17 CTMs for each shelf, powered from an on-board power supply

Location

The CTM plugs into 1 or 12 of the provisionable maintenance trunk slots the current MTM provides. The CTM can be installed in an MTM shelf, where -48V (-60V) poser feed is available on backplane. When this condition occurs, the CTM automatically senses and draws the power form. This power form feeds through the on-board dc/dc 36-72V/5V power converter on the shelf. A single failure of the on-board power converter only affects the one specified CTM with a maximum of 30 conference channels.

Note: Limits on the number of CTM circuit packs installed on a current STM shelf apply. A -48V (-60V) feed is not present on the STM backplane on provisional slots. A maximum of two CTM circuit packs can be installed on any single STM shelf because of this limit. Two CTM circuit packs equals 60 conference ports.

The DS30 cables for the CTM plug into the backplane pins at the back of the shelf. The pins correspond to the slot of the CTM. The same DS30 cable specified for the EDRAM also applies for the CTM.

Functional description

The CTM provides the equivalent functions and capabilities of a current MTM with five NT3X67 six port conference cards. The same conference algorithm, features and maintenance capabilities of the NT3X67 apply to the NT1X81AA. The NT1X81AA emulates the operation of the current MTM controller and conference circuits. The configuration of the CTM can be as five 6 party or ten 3 party conferences.

Functional blocks

The CTM functionally divides into five blocks.

The NT1X81AA has the following functional blocks:

- microprocessor
- MTM controller
- conference circuit
- power converter
- DS30 interface

The microprocessor block is an 8085 NMOS microprocessor. The microprocessor block contains the following:

- 4 Kbytes of EPROM that contains the MTM controller bootstrap loader
- 32 Kbytes of static microprocessor RAM that contains the MTM PM load.
- 32 Kbytes of EPROM that contains all MTM generated tones and logic circuits that consist of buffers and latches

MTM controller

This ASIC implements most of the circuitry associated with the MTM controller function.

Conference circuit

This single device serves all five conference circuits. The device multiplexes the hardware for one conference circuit with the five groups of six voice channels.

Power converter

An on-board power converter module provides ±5V power for CTM logic. This module provides this power when -48V (-36 to -72V) battery feed is available on specified backplane pins of CTM provisional slots. Relay circuitry senses -48V (-36V to -72V) battery voltage and switch CTM ±5V power. The power switches from external power supply, like NT2X70, to internal on-board power supply module.

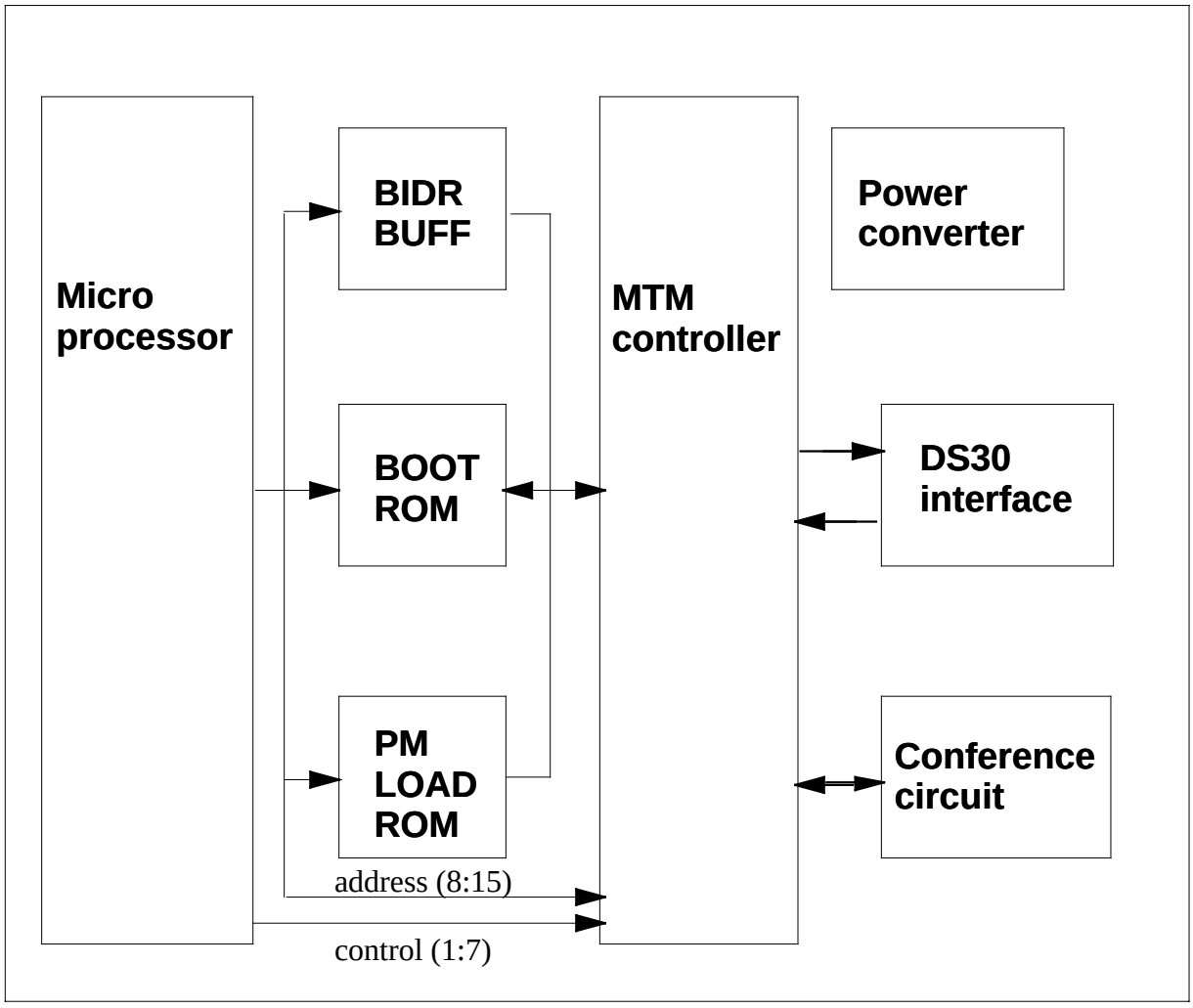
DS30 interface

This block contains a single NT5L67AA hybrid and logic circuitry for one DS30 link interface on both network planes. The DS30 clock and data recovery occur internally to the MTM controller functional block.

The following figure shows the relationship of the functional blocks.

NT1X81AA (end)

NT1X81AA functional blocks



Technical data

Power requirements

The NT1X81AA can be provisioned on the following:

- an STM, with provisional restriction. An NT2X70 converter pack powers an STM
- an MTM, with a maximum of 12 CTMs for each shelf. An on-board power supply powers on MTM.
- an ISM, with a maximum of 17 CTMs for each shelf. An on-board power supply powers an ISM

NT1X81BA

Product description

The NT1X81BA conference trunk module (CTM) for Japan is a stand alone peripheral module (PM). The NT1X81BA implements five separate six-port voice conference bridges. The system supports thirty voice channels for conferencing functions.

Operation in Japan requires modification to the entries. This modification provides for selection of Mu-Law operation and selection of the toneset for Japanese applications.

The NT1X81BA can be provisioned on:

- an STM, with provisional restriction. An NT2X70 converter pack powers an STM.
- an MTM, with a maximum of 12 CTMs for each shelf. An on-board power supply powers an MTM
- an ISM, with a maximum of 17 CTMs per shelf. An on-board power supply powers an ISM.

Location

The CTM can plug into 1 or 12 of the provisionable maintenance trunk slots that the current MTM provides. The CTM can be installed in an MTM shelf where -48V (-60V) poser feed is available on backplane. When this condition occurs, the CTM automatically senses and draws the power form. This form feeds through the on-board dc/dc 36-72V/5V power converter on the shelf. A single failure of the on-board power converter only affects the one CTM with a maximum of 30 conference channels.

Note: Limits on the number of CTM circuit packs installed on a current STM shelf apply. A -48V (-60V) feed on the STM backplane is not present on provisional slots. A maximum of two CTM circuit packs can be installed on any single STM shelf because of this limit. Two circuit packs equal 60 conference ports.

The DS30 cables for the CTM plugs into the backplane pins at the back of the shelf. The pins correspond to the slot of the CTM. The same DS30 cable specified for the EDRAM is specified for the CTM.

Functional description

The CTM provides the equivalent functions and capabilities of the current MTM with five NT3X67 six port conference cards. The same conference algorithm, features and maintenance capabilities of the NT3X67 apply to the NT1X81BA. The NT1X81BA emulates the operation of the current MTM

NT1X81BA (continued)

controller and conference circuits. The configuration of the CTM can be as five 6 party or ten 3 party conferences.

Functional blocks

The CTM functionally divides into five blocks.

The NT1X81BA has the following functional blocks:

- microprocessor
- MTM controller
- conference circuit
- power converter
- DS30 interface

Microprocessor

The microprocessor block is an 8085 NMOS microprocessor. The microprocessor block has the following:

- 4 Kbytes of EPROM that contains the MTM controller bootstrap loader
- 32 Kbytes of static microprocessor RAM that contains the MTM PM load
- 32 Kbytes of EPROM that contains all MTM generated tones and logic circuits that contains buffers and latches

MTM controller

This ASIC implements most of the circuits associated with the MTM controller function.

Conference circuit

This single device serves all five conference circuits. This device multiplexes the hardware for one conference circuit with the five groups of six voice channels.

Power converter

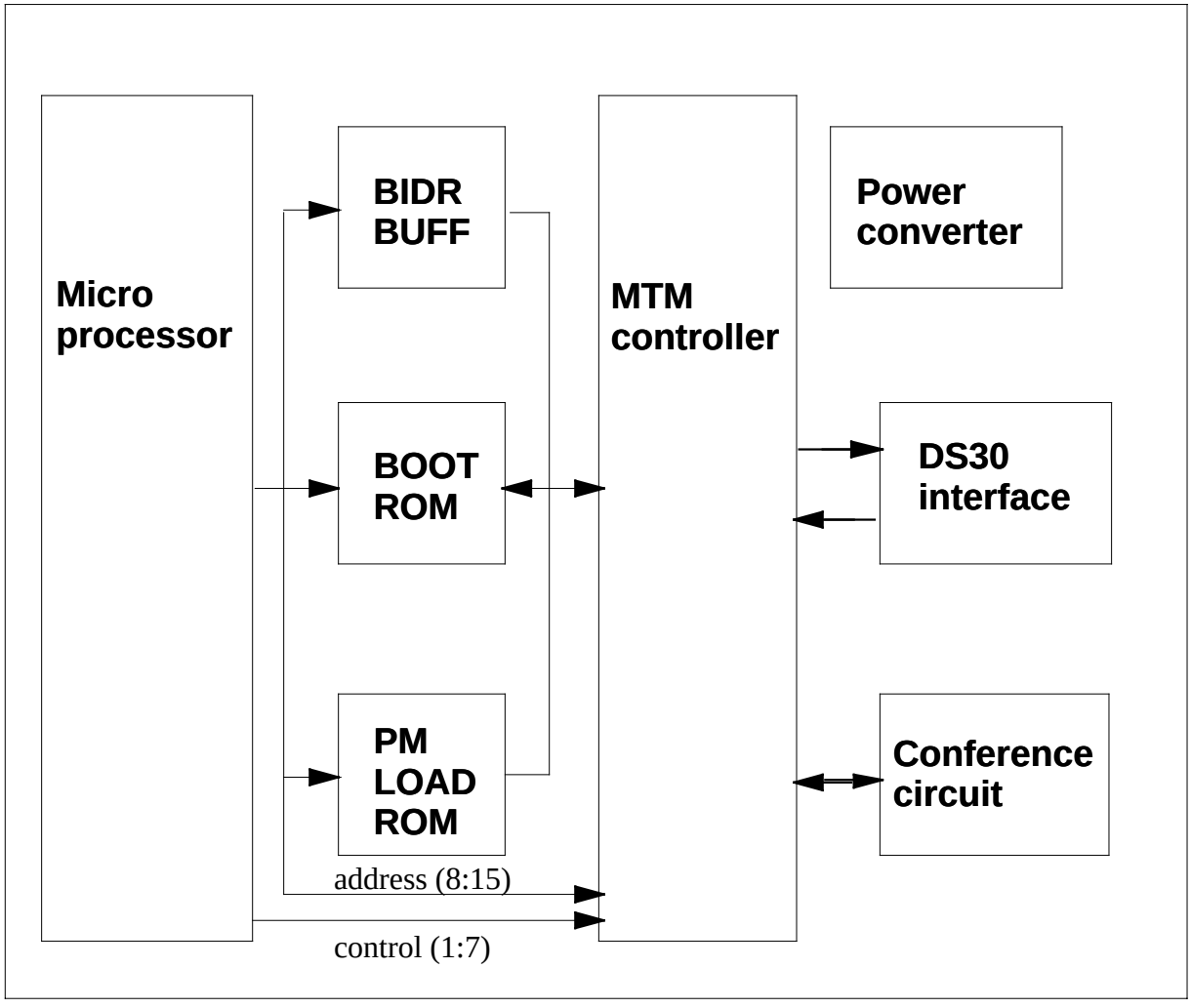
An on-board power converter module provides ±5V power for CTM logic when -48V (-36 to -72V) battery feed is available. The feed is available on specified backplane pins of CTM provisional slots. Relay circuitry senses -48V (-36V to -72V) battery voltage. The circuitry switches to CTM ±5V power from external power supply, like NT2X70, to internal on-board power supply module.

DS30 interface

This block contains a single NT5L67AA hybrid and logic circuitry for one DS30 link interface on both network planes. The DS30 clock and data recovery occurs internally to the MTM controller functional block.

The following figure shows the relationship between the functional blocks.

NT1X81BA functional blocks



NT1X81BA (end)

Technical data

Power requirements

The NT1X81BA can be provisioned on:

- an STM, with provisional restriction, that an NT2X70 converter pack powers
- an MTM, with a maximum of 12 CTMs for each shelf, powered from an on-board power supply
- an ISM, with a maximum of 17 CTMs for each shelf, powered from an on-board power supply

NT1X89AA

Product description

The NT1X89AA multiprotocol controller card is a microprocessor-based device controller. This controller is an interface between the DMS-100 central control (CC) and a maximum of two external data processing systems. Modems that communicate over telephone links connect the external systems to the card.

The CC downloads the operating system and the application software that runs the card when the modem starts the card. This feature allows the modem to reconfigure the card for different applications.

Location

The NT1X89AA occupies one card position on an input/output controller (IOC) shelf.

Functional description

When the system starts the NT1X89AA, the stored start-up routine causes the CC to load the operating system. The CC loads the application-specified software into the card. Based on software instructions, the card controls and operates the communication interfaces.

Functional blocks

The NT1X89AA contains the following functional blocks:

- IOC interface and RAM
- CPU
- EPROM
- dynamic RAM
- multiprotocol data communications interface
- automatic dialer and asynchronous port
- direct memory access (DMA) controller
- reset controller

IOC interface and RAM

The IOC interface circuit contains the IOC interface and the IOC interface RAM. This circuit handles communications between the IOC bus and the CPU. The IOC interface RAM serves as a message buffer for communications between the IOC bus and the CPU.

NT1X89AA (continued)

CPU

Software downloaded from the CC directs the CPU, which controls all operations of the card. In the start-up routine of the card, the CPU communicates with the CC. The CC downloads the operating system and application software. When the software is loaded, the CPU initializes the peripheral devices. The CPU takes control of the modems connected to the data communication channels.

EPROM

The EPROM contains the start-up routine for the card. When the card starts, the CPU reads the code in the EPROM. The EPROM instructs the CPU to download the operating software from the CC.

Dynamic RAM

The DRAM stores downloaded operating system and application software. The card provides 0.5 Mbyte of memory. This memory can process three layers of a many layered data communications protocol. This capability meets the requirement of the International Standards Organization (ISO). The CC must process the application layer.

The system holds 128 Kbyte of DRAM as a data communications buffer. The 128 Kbyte of DRAM can send or receive data from the external equipment.

Multiprotocol data communications interface

The multiprotocol data communications interface consists of two full-duplex RS-232C ports. Each port can operate at the same time at speeds of a maximum of 2400 baud. The interface contains registers that control data flow and the read/write control lines.

The interfaces provide the following signals:

- RI (ring indicator)
- DTR (data terminal ready)
- DSR (data set ready)
- TXD (transmit data)
- RXD (receive data)
- DTEC (DTE transmitter signal element timing)
- TXCLK (DCE transmitter signal element timing)
- RXCLK (receive signal element timing)
- RTS (request to send)

- CTS (clear to send)
- DCD (received line signal detector)

Automatic dialer and asynchronous port

The card provides an RS-366 port for connection to an automatic call unit. The card provides an asynchronous RS-232C port for normal terminal use.

The RS-232C port operates at speeds of a maximum of 2400 baud. The RS-232C port provides the following signals:

- TXD (transmit data)
- RXD (receive data)

The RS-366 port provides the following signals:

- CRQ (call request)
- PWI (power indication)
- DLO (data line occupies)
- COS (call origination state)
- ACR (abandon call and retry)
- PND (present next digit)
- DPR (digit present)
- NB1 (digit signal low order bit)
- NB2 (digit signal second order bit)
- NB3 (digit signal third order bit)
- NB4 (digit signal high order bit)

Direct memory access controller

The DMA controller provides a direct link between the data communications buffer and the external systems connected to the multiprotocol interface. The DMA controller reads data from or writes data to the buffer without CPU interference.

Reset controller

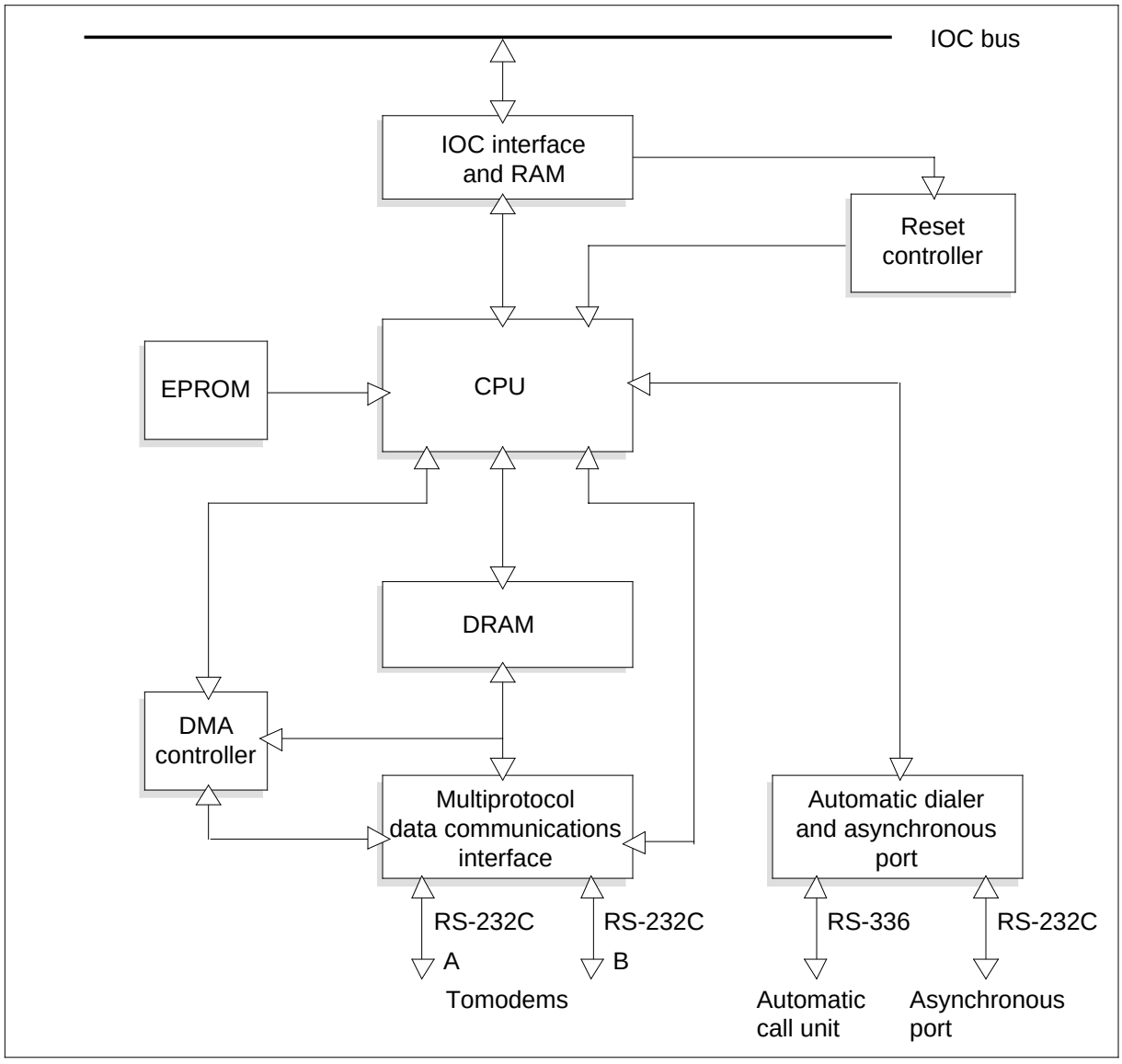
The reset controller makes sure all reset commands are 100 ms in length. The controller recognizes reset commands like power valid, sanity timer, CPU, and IOC reset. The NT1X89AA issues all CPUs. The IOC bus issues all IOC resets. All card-issued reset commands disable the IOC bus. The power valid and sanity timer reset commands reset the complete card. The CPU reset

NT1X89AA (continued)

command resets the complete card except for the CPU. The IOC reset command resets the complete card except for the IOC bus.

The relationship between the functional blocks appear in the following figure.

NT1X89AA functional blocks



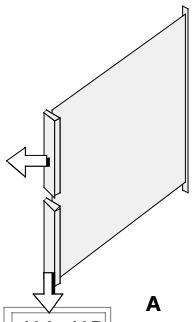
Signaling

Pin outs

The pin outs for the NT1X89AA appear in the following table.

NT1X89AA pin outs

	A	B
1A 1B	GND	GND
2A 2B	+5 V	+5 V
3A 3B	+5 V	+5 V
4A 4B	+5 V	+5 V
5A 5B	GND	GND
6A 6B	--5 V	--5 V
7A 7B	GND	GND
8A 8B	+12 V	+12 V
9A 9B	GND	GND
10A 10B	--12 V	--12 V
11A 11B	GND	GND
12A 12B	AD00--	AD01--
13A 13B	AD02--	AD03--
14A 14B	AD04--	AD05--
15A 15B	AD06--	AD07--
16A 16B	AD08--	AD09--
17A 17B	AD10--	AD11--
18A 18B	AD12--	AD13--
19A 19B	AD14--	AD15--
20A 20B	GND	GND
21A 21B	DUNIT	GND
22A 22B	RS--	GND
23A 23B	WS--	GND
24A 24B	GND	RESET--
25A 25B	GND	GND
26A 26B	DAT0--	DAT1--
27A 27B	DAT2--	DAT3--
28A 28B	DAT4--	DAT5--
29A 29B	DAT6--	DAT7--
30A 30B	GND	GND
31A 31B	MAD12+	MAD13+
32A 32B	MAD14+	MAD15+
33A 33B		
34A 34B		
35A 35B		
36A 36B		
37A 37B		
38A 38B		
39A 39B		
40A 40B		



	A	B
41A 41B	GND	GND
42A 42B	TXDA	RXCA
43A 43B		DSRA
44A 44B	RTSA	TXCA
45A 45B	RXDA	
46A 46B	DCDA	
47A 47B	CTSA	
48A 48B	DTRA	RIA
49A 49B	DTECA	
50A 50B	GND	GND
51A 51B	GND	GND
52A 52B	TXDB	RXCB
53A 53B		DRSB
54A 54B	RTSB	TXCB
55A 55B	RXDB	
56A 56B	DCDB	
57A 57B	CTSB	
58A 58B	DTRB	RIB
59A 59B	DTECB	
60A 60B	GND	GND
61A 61B	GND	GND
62A 62B	CR	DP
63A 63B	NB1	NB2
64A 64B	NB4	NB8
65A 65B		
66A 66B	PI	DLO
67A 67B	COS	ACR
68A 68B	PNO	
69A 69B		
70A 70B	GND	GND
71A 71B	GND	GND
72A 72B	TXM	
73A 73B		
74A 74B		
75A 75B	RXM	
76A 76B		
77A 77B		
78A 78B		
79A 79B		
80A 80B	GND	GND

NT1X89AA (end)

Technical data

Dimensions

The following dimensions are for the NT1X89AA circuit card:

- overall height: 367.5 mm (12.5 in.)
- overall depth: 254.0 mm (10.0 in.)
- overall width: 222 mm (0.875 in.)

Power requirements

The power requirements for the NT1X89AA appear in following table.

Power requirements

Voltage	Current
+12 V	55.00 mA
+5 V	2.22 A
-12 V	75.00 mA

The power requirement is a maximum of 12.66W.

NT1X89BA

Product description

The NT1X89BA enhanced multiprotocol controller (EMPC) is an improvement of the NT1X89AA multiprotocol controller (MPC). The MPC is a general-purpose data communication board on the input/output controller (IOC) shelf. The EMPC supports simultaneous RS-232C operation on two programmable ports (2 and/or 3). The cards allow the system to configure these ports at the maximum rate of 2400 bit/s. The EMPC version has programmable logic (internal Y-connector) that allows a separate V.35 connection on port 1 for speeds of a maximum of 56 and 64 kbit/s. The EMPC allows simultaneous operation of two links. One link can use the V.35 port interface and one link remains RS-232C, or both links use RS-232C links. Protocols like BX.25, Sync, and Async cannot be on one EMPC.

Support for current applications that use MPC and for protocols supported or under development for MPC is available. The NT feature package NTXE98AA requires the use of the EMPC.

Functional description

The NT1X89BA card provides data communications for the DMS-100 Family. Improvements to the card provide the following new features:

- builds on the current MPC ROM firmware base to provide downloading and diagnostic compatibility with the current CC interface
- removes the diagnostics associated with the previous RS-366 port interface because the port is not in the EMPC
- increased processing speed

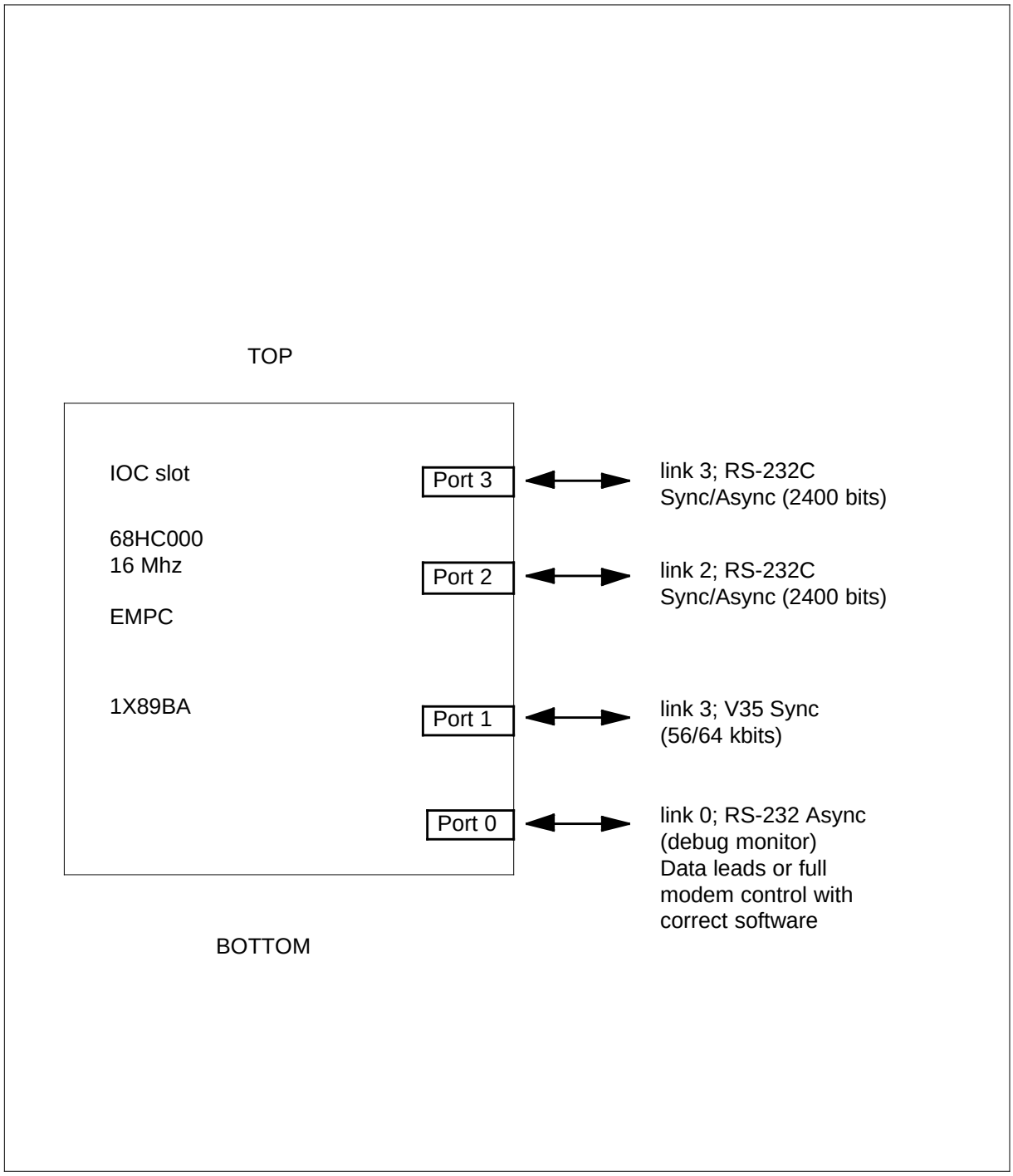
Hardware description

The hardware in the NT1X89BA provides four ports that can input-output to the external world. Different from the MPC, these four ports of the EMPC map to three data links. The same link controls two of the ports (1 and 3). Refer to the following figure.

- Port 0: Async RS-232: for MPC Debug purposes
- Port 1: Sync V.35: entered as Link 3
- Port 2: Sync/Async RS-232
- Port 3: Sync/Async RS-232

NT1X89BA (continued)

NT1X89BA interfaces



Signaling

Interface pin outs

The cables for the V.35 port (Port 1) are:

- IOC bulkhead to 34-pin connector, NT0X96EF
- IOC bulkhead to DB25 connector, NT0X96EG

The cables for the RS-232 ports (Ports 2 and 3) are:

- Asynchronous-IOC to DB25, NT0X96EH
- Synchronous-IOC to DB25, NT0X26LY

The MPC and the EMPC use these RS-232 cables.

The EMPC uses one of two cables for V.35. The EMPC can use a DB25 connector. The DB25 connector can damage equipment. This action can occur if you connect a DB25 connector to the following:

- RS-232C
- other equipment that is not V.35
- V.35 equipment with a DB25 connector that is not compatible with the pin-outs that appear in the following table
- V.35 equipment with a DB25 connector that is not an electrical data communications equipment (DCE)

The EMPC can use the normal V.35 34-pin interface connector.

The pin-outs the EMPC card uses appear in the following table.

NT1X89 pin outs (Sheet 1 of 2)

DB25 male connector pin	Signal at EMPC	34-pin connector
2	TXDA+	P
3	RXDA+	R
4	RTSV	C
5	CTSV	D
6	DSRV	E
7	GROUND	B
8	DCDV	F

NT1X89BA (continued)

NT1X89 pin outs (Sheet 2 of 2)

DB25 male connector pin	Signal at EMPC	34-pin connector
13	TXCA-	AA/a
14	TXDA-	S
15	TXCA+	Y
17	RXCA+	V
19	RXCA-	X

Technical data

Physical characteristics

The dimensions for the NT1X89BA card appear in the following table.

Physical dimensions

Dimension	SI units	Imperial units
Overall height	19.05 mm	0.75 in.
Overall depth	317.5 mm	12.5 in.
Overall width	254 mm	10 in.

Power requirements

The power requirements for the NT1X89BA card appear in the following table.

Power requirements

Power	Rating	Rating	Rating
Voltage required	±5V	±12V	-12V
Current required	2A	0.05A	0.05A
Total power required	11.2W		

Environmental conditions

The environmental conditions required for the NT1X89BA appear in the following table.

Environmental conditions

Condition	Operating range	Short-term range
Ambient temperature	10-30°C	5-49°C
Relative humidity	2-55%	20-80%
Note: At an ambient temperature of 21°C, relative humidity can have a maximum of 80%. At an ambient temperature of 49°C, the relative humidity can be a maximum of 30%.		

NT1X89BB

Product description

The NT1X89BB enhanced multiprotocol controller (EMPC) is an improvement of the NT1X89BA enhanced multiprotocol controller (EMPC). The EMPC is a general-purpose data communication board on the input/output controller (IOC) shelf. The EMPC supports simultaneous operation of two programmable RS-232C port connections. Both cards allow the system to configure these ports at the maximum rate of 19.2 kbit/s. The EMPC version has programmable logic (internal Y-connector) that allows a separate V.35 connector on port 1 for speeds of a maximum of 56 and 64 kbit/s. The EMPC allows simultaneous operation of two links. One link uses the V.35 port interface and one link remains RS-232C, or both links initiate RS-232C links. Protocols (BX.25, X.25, and Async) cannot mix on one EMPC.

Support is available for current applications that use MPC, and for protocols supported or under development for MPC. The NT feature package NTXE98AA requires the use of the EMPC.

Functional description

The NT1X89BB card provides data communications for the DMS-100 Family. Improvements to the card provide the following new features:

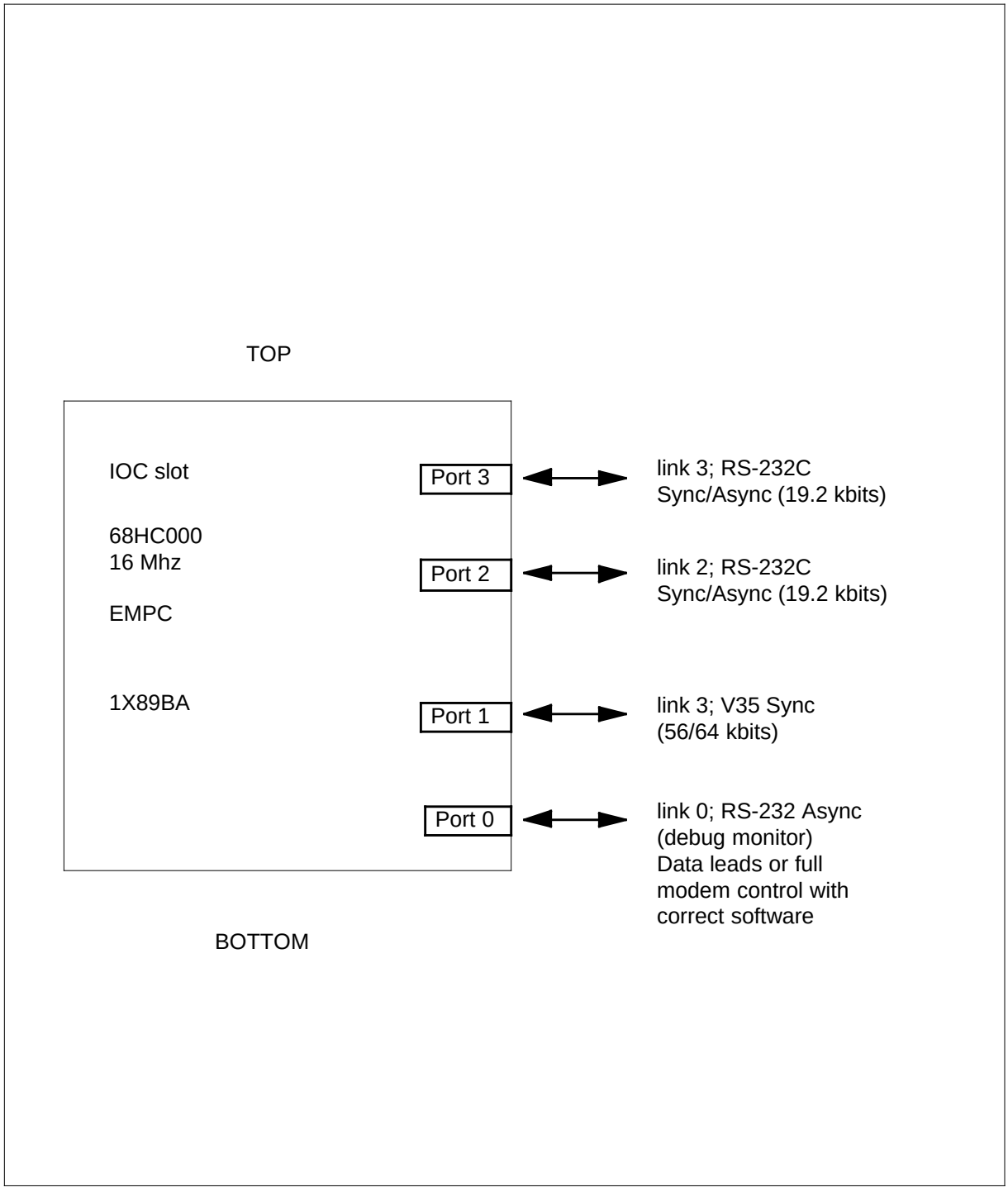
- builds on the current MPC ROM firmware base to provide downloading and diagnostic compatibility with the current CC interface
- removes the diagnostics associated with the previous RS-366 port interface because the port is not in the EMPC

Hardware description

The hardware incorporated in the NT1X89BB provides four ports that can input-output to the external world. These four ports of the EMPC map to three data links. The same data link controls two of the ports (1 and 3). Refer to the following figure.

- Port 0: Async RS-232
- Port 1: Sync V.35
- Port 2: Sync/Async RS-232
- Port 3: Sync/Async RS-232

NT1X89BB interfaces



NT1X89BB (continued)

Signaling

Interface pin-outs

The cables for the V.35 port (Port 1) are:

- IOC bulkhead to 34-pin connector, NT0X96EF
- IOC bulkhead to DB25 connector, NT0X96EG

The cables for the RS-232 ports (Ports 2 and 3) are:

- Asynchronous-IOC to DB25, NT0X96EH
- Synchronous-IOC to DB25, NT0X26LY

The MPC and the EMPC use these RS-232 cables.

The EMPC uses one of two cables for V.35. The EMPC can use a DB25 connector that can damage equipment if you connect the DB25 connector to the following:

- RS-232C
- other equipment that is not V.35
- V.35 equipment with a DB25 connector that does not comply with the pin-outs that appear in the following table.
- V.35 equipment with a DB25 connector that is not an electrical data communications equipment (DCE)

The EMPC can use the normal 34-pin V.35 interface connector (34-pin).

The pin-outs that the EMPC card uses appear in the following table.

NT1X89 pin-outs (Sheet 1 of 2)

DB25 male connector pin	Signal at EMPC	34-pin connector
2	TXDA+	P
3	RXDA+	R
4	RTSV	C
5	CTSV	D
6	DSRV	E
7	GROUND	B
8	DCDV	F

NT1X89 pin-outs (Sheet 2 of 2)

DB25 male connector pin	Signal at EMPC	34-pin connector
13	TXCA-	AA/a
14	TXDA-	S
15	TXCA+	Y
16	RXDA-	T
17	RXCA+	V
19	RXCA-	X

Technical data

Physical characteristics

The dimensions for the NT1X89BB card appear in the following table.

Dimensions

Dimension	SI units	Imperial units
Overall height	19.05 mm	0.75 in.
Overall depth	317.5 mm	12.5 in.
Overall width	254 mm	10 in.

Power requirements

The power requirements for the NT1X89BB card appear in the following table.

Power requirements

Power	Rating	Rating	Rating
Voltage required	+5 V	+12V	-12V
Current required	2.0A	0.05A	0.05A
Total power required	11.2W		

NT1X89BB (end)

Environmental conditions

The environmental conditions required for the NT1X89BB appear in the following table.

Environmental conditions

Condition	Operating range	Short-term range
Ambient temperature	10-30°C	5-49°C
Relative humidity	2-55%	20-80%

NT1X90AA

Product description

The NT1X90AA test signal generator (TSG) 1 card provides programmable dial-up test functions. The TSG 1 card provides internal diagnostic trunk test signals for DMS-100 switching systems.

Location

The card occupies one card position in the maintenance trunk module (MTM) and connects to one trunk. The card is in use with the pulse code modulation (PCM) level meter (PLM). The PLM and the card share a trunk and an enable signal.

Functional description

Control signals from the MTM controller activate the card at the required time. The control signals determine the signal that the TSG produces. The controller determines if the TSG or the PLM is active at a specified time.

Functional blocks

The NT1X90AA has the following functional blocks:

- two trunk logic circuits (TLC)
- tone generator
- quiet termination control
- buffer
- gate
- filter circuits

TLC

The TLCs provide interfaces between the MTM and the TSG card. The MTM sends control data over the receive data (RDAT) bus to TLC-0 and TLC-1. The TLC-0 controls the operation of the card through signals on eight signal distribution (SD) points. The functions the eight SD points provide appear in the following table.

Signal distribution point functions (Sheet 1 of 2)

	Bit number							
Function	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSG card inactive, PLM active								0
TSG card active, PLM inactive								1

NT1X90AA (continued)

Signal distribution point functions (Sheet 2 of 2)

Function	Bit number 7	6	5	4	3	2	1	0
Address filter and quiet termination control					0	0	0	
Address attenuation ROM—least important byte					0	0	1	
Address attenuation ROM—most important byte					0	1	0	
Address frequency selection—least important byte					0	1	1	
Address frequency selection—next important byte					1	0	0	
Address frequency selection—most important byte					1	0	1	
Not used					1	1	0	
Not used					1	1	1	
Control data for select notch filter, select message C filter, select quiet termination, select attenuation coefficient, select frequency coefficient	X	X	X	X				

The TLC-1 controls the tap-off feature of the card. The DMS-100 software activates the TLC at the correct time. The PCM samples for the selected channel are sent to the transmit data (XDAT) bus. The system can use the signals to connect to other test equipment for looping purposes.

Tone generator

The ROM stores the digital tones at a standard transmission level. The TLC-0 sends a signal to the tone generator to produce a specified tone. The digitized tone transfers from the ROM to a multiplier circuit. The multiplier changes the level of the tone to reach the correct level. A compander receives the multiplied tone. The compander converts the digitized tones to PCM samples.

Quiet termination control

The quiet termination control operates when the TLC-0 uses an SD point to request the termination. The quiet termination control sends a termination signal to the output gate.

Buffer

The buffer stores the signal the tone generator circuit produces until the gate releases the signal to the XDAT bus.

Gate

The gate controls the information that the card sends over the XDAT bus. If the gate does not receive the quiet termination control signal, the gate sends the tone over the XDAT bus. If the gate receives a quiet termination signal, the gate does not send the tone over the XDAT bus.

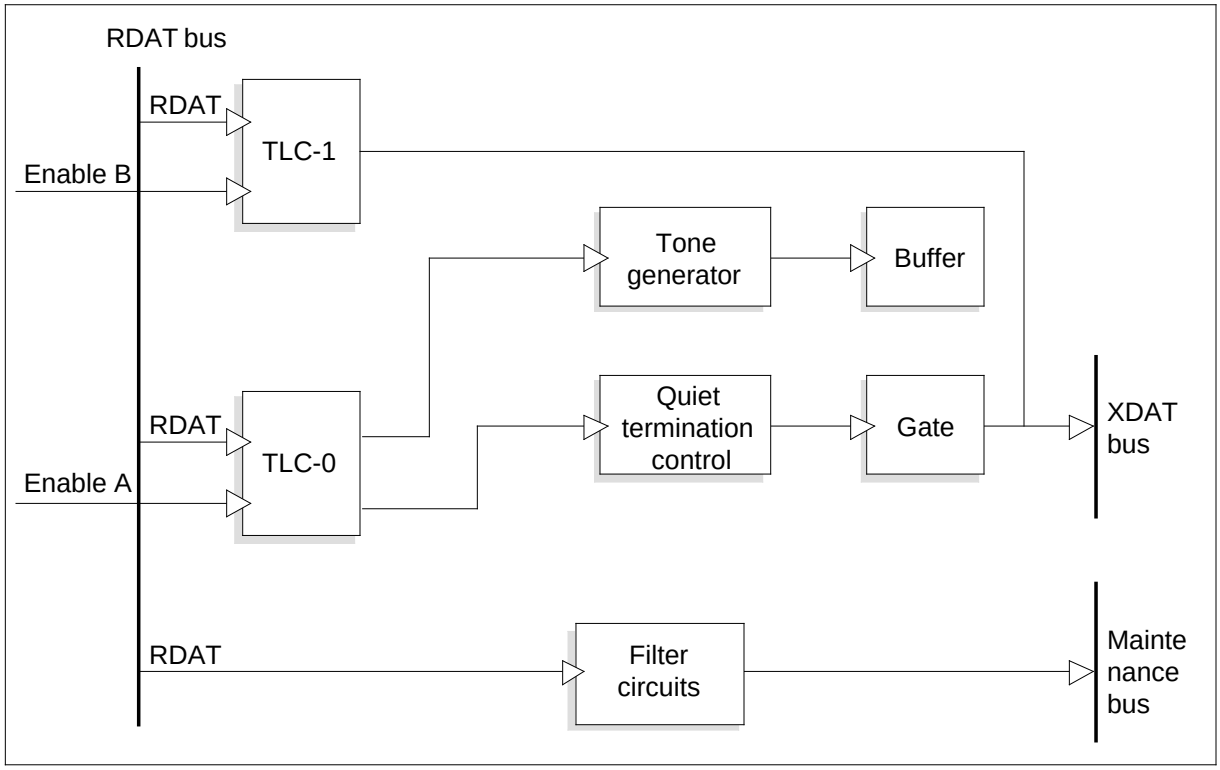
Filter circuits

The filter circuits receive PCM signals from the RDAT bus, decode the signals, and convert the PCM data to voice frequency (VF) signals. The VF signals are applied to two filter circuits. If necessary, specify these two filter circuits. The first filter removes the 1010 Hz test tone. The signals use the first filter during noise measurements. The second filter is C-message weighted. The second filter simulates subscriber conditions. After the VF signals are filtered, the signals return to PCM data. The signals transmit over the Maintenance bus to the level master card.

The relationship between the functional blocks appears in the following figure.

NT1X90AA (continued)

NT1X90AA functional blocks



Technical data

The NT1X90AA tone generator produces tones from 4 Hz through 3996 Hz in 4 Hz steps. The level range is from 0 through -12.5 dBm (±0.1 dB) and ±3 through 60.5 dBm (±0.5 dB).

The 1010 Hz notch filter has the following characteristics:

Upper frequency (Hz)	Lower frequency (Hz)	Loss (dB)
1025	995	-50.0
1182	862	-30.0
1700	400	-0.5

Dimensions

The following dimensions are for the NT1X90AA circuit card:

- overall height: 317.5 mm (12.5 in.)
- overall depth: 254.0 mm (10.0 in.)

Power requirements

The NT1X90AA requires a voltage of +5V. The current required is 1.2A.

NT1X90BA

Product description

The test signal generator a-law TTT (NT1X90BA) circuit card provides programmable dial-up test functions. The NT1X90BA circuit card provides internal diagnostic trunk test signals for the Digital Multiplex System (DMS). International applications uses the NT1X90BA circuit card.

Location

The NT1X90BA circuit card is in one card position in the maintenance trunk module (MTM) and connects to one trunk. The PCM level meter (PLM) uses the NT1X90BA circuit card. The PLM and the NT1X90BA circuit card share an enable signal and a trunk.

Functional description

Signals from the MTM controller activate the NT1X90BA circuit card at the appropriate time. The control signals determine the signal the NT1X90BA circuit card produces. The MTM controller determines if the NT1X90BA circuit card or the PLM is active at a defined time.

Functional blocks

Functional blocks of the NT1X90BA circuit card are:

- two trunk logic circuits (TLC)
- tone generator
- quiet termination control
- buffer
- gate
- filter circuits

Trunk logic circuit

The TLCs provide interfaces between the MTM and the NT1X90BA circuit card. The MTM sends control data over the receive data (RDAT) bus to TLC-0 and TLC-1. TLC-0 controls the operation of the NT1X90BA circuit card through signals on eight signal distribution (SD) points.

The functions provided by the eight SD points appear in the next table.

Signal distribution point functions

Function	Bit number 7	6	5	4	3	2	1	0
TSG card inactive, PLM active								0
TSG card active, PLM inactive								1
Address filter and quiet termination control					0	0	0	
Address attenuation ROM—least important byte					0	0	1	
Address attenuation ROM—most important byte					0	1	0	
Address frequency selection—least important byte					0	1	1	
Address frequency selection—next important byte					1	0	0	
Address frequency selection—most important byte					1	0	1	
Not used					1	1	0	
Not used					1	1	1	
Control data for select notch filter, select message C filter, select quiet termination, select attenuation coefficient, select frequency coefficient	X	X	X	X				

The TLC-1 controls the tap-off feature of the NT1X90BA circuit card. DMS software activates the TLC at the appropriate time. The pulse code modulation (PCM) samples for the selected channel are sent to the transmit data (XDAT) bus. The DMS switch can use the signals to connect to other test equipment for looping purposes.

Tone generator

The read only memory (ROM) stores the digital tones at a standard transmission level. TLC-0 sends a signal to the tone generator to produce a defined tone. The digitized tone transfers from the ROM to a multiplier circuit. The multiplier circuit changes the level of the tone to reach the correct level.

NT1X90BA (continued)

A compander receives the multiplied tone. The compander converts the digitized tones to PCM samples.

Quiet termination control

The quiet termination control operates when TLC-0 uses an SD point to request the termination. The quiet termination control sends a termination signal to the output gate.

Buffer

The buffer stores the signal the tone generator circuit produces until the gate releases the signal to the XDAT bus.

Gate

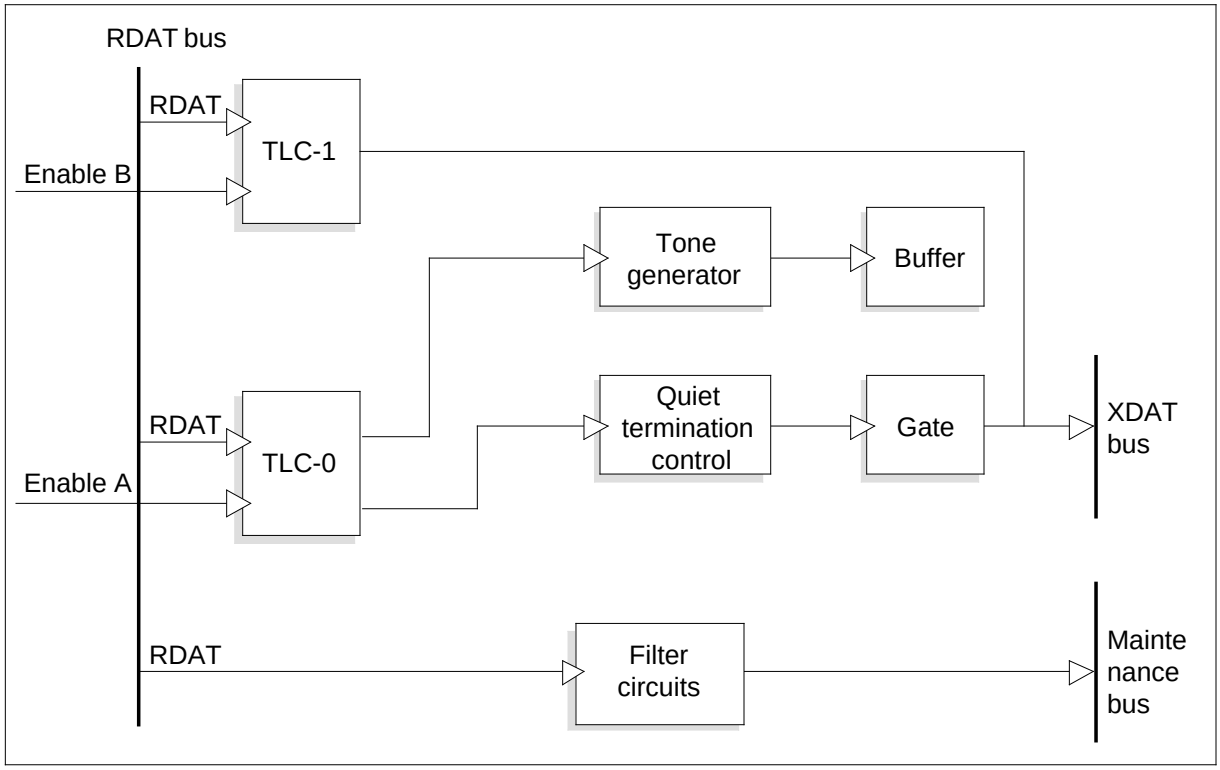
The gate controls the information the NT1X90BA circuit card sends over the XDAT bus. If the gate does not receive the quiet termination control signal, the gate sends the tone over the XDAT bus. If the gate receives a quiet termination signal, the gate does not send the tone over the XDAT bus.

Filter circuits

The filter circuits receive PCM signals from the RDAT bus, decode the signals, and convert the PCM data to voice frequency (VF) signals. The VF signals are applied to two filter circuits. The first filter removes the 1010 Hz test tone. The signals use the first filter during noise measurements. The second filter has a C-message weighting characteristic and is used to apply average subscriber conditions to noise measurements. After the VF signals are filtered, the signals return to PCM data. The signals transmit over the maintenance bus to the level master card.

The relationship between the functional blocks appears in the following figure.

NT1X90BA functional blocks



Technical data

The NT1X90BA circuit card tone generator produces tones from 4 Hz through 3996 Hz in 4 Hz steps. The level range is from 0 through -12.5 dBm (±0.1 dB) and +3 through 60.5 dBm (±0.5 dB).

The 1010 Hz notch filter has the following specifications:

Upper frequency (Hz)	Lower frequency (Hz)	Loss (dB)
1025	995	-50.0
1182	862	-30.0
1700	400	-0.5

NT1X90BA (end)

Dimensions

The following dimensions are for the NT1X90BA circuit card:

- height: 317.5 mm (12.5 in.)
- depth: 254.0 mm (10.0 in.)

Power requirements

The NT1X90BA circuit card requires a voltage of +5V. The current required is 1.2A.

3 NT2Xnnaa

NT2X01AA through NT2X58AT (continued in Vol. 2)

NT2X01AA

Product description

The NT2X01AA data receiver C25 card for automatic identification of outward dialing (AIOD) terminates a data channel. The data channel is between a private branch exchange (PBX) and a central office (CO).

The card performs signaling supervision. The card accepts information required to identify the PBX station number of the station that transmits a call. The card functions as an interface. The interface is between a maintenance trunk module (MTM) in DMS-100 equipment and the circuit that sends data. The circuit that sends data is the far-end or connecting PBX.

The card contains four channels. Each channel operates separately. Each channel operates by the same method.

Location

The card occupies two slots in an MTM. An MTM can contain six cards.

Functional description

The NT2X01AA receives signals from the PBX. The NT2X01AA converts the signals to binary-coded decimal (BCD) signals for transmission to the DMS-100 central control (CC). The circuits that belong to the card indicate simplex or E signals. The cards perform diagnostic tests on the card.

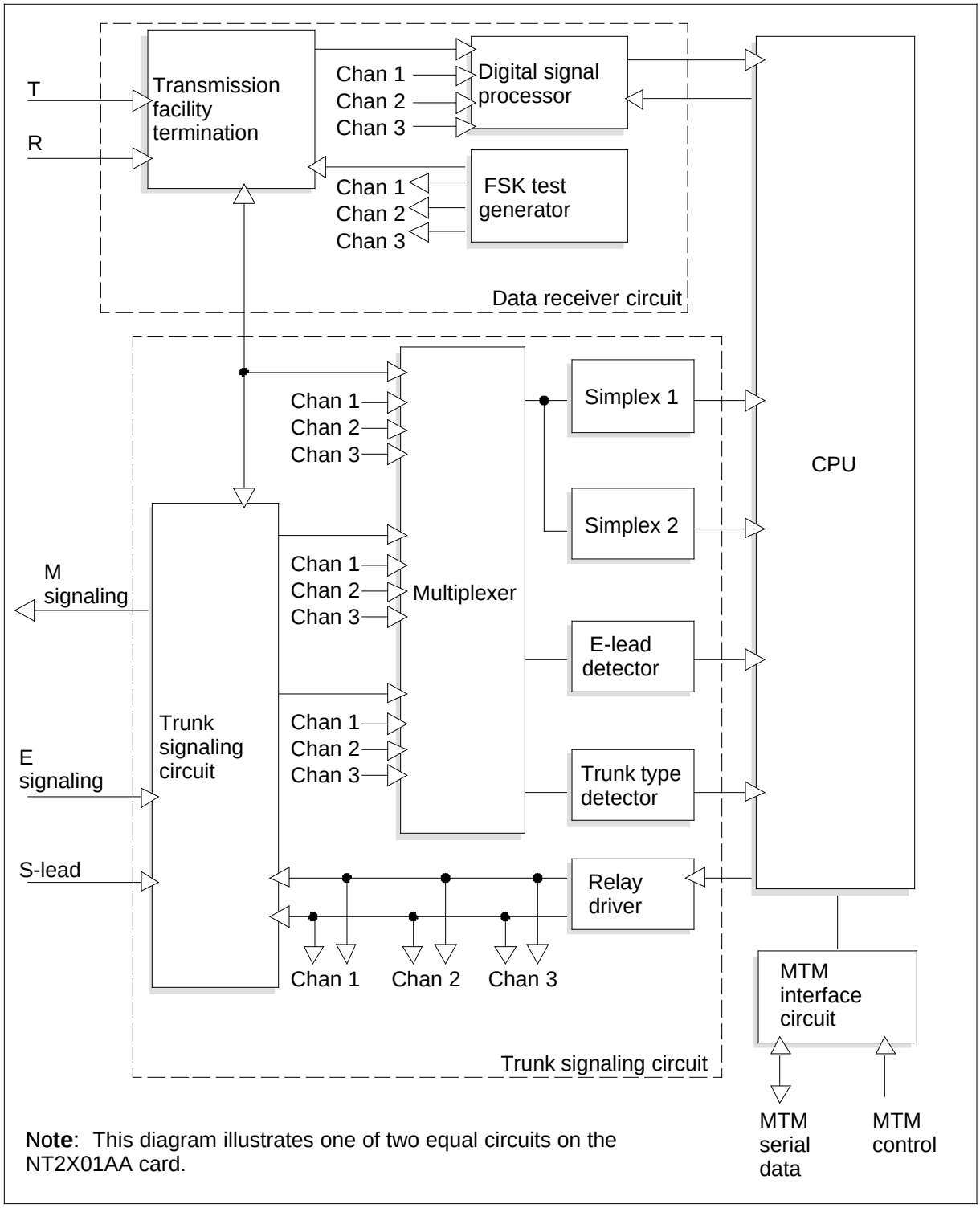
Functional blocks

Each channel in the NT2X01AA contains the following functional blocks:

- transmission facility termination
- digital signal processor
- frequency shift keying (FSK) test generator
- trunk signaling circuit
- multiplexer (MUX)
- two simplex circuits
- E-lead detector
- trunk type detector
- relay driver
- CPU
- MTM interface circuit

The relationship between the operating blocks appears in the following figure.

NT2X01AA functional blocks



Note: This diagram illustrates one of two equal circuits on the NT2X01AA card.

NT2X01AA (continued)

Transmission facility termination

The transmission facility termination receives FSK data from the PBX data link. The transmission facility termination provides termination of the transmission facility on each of the four data link appearances. You can manually select the circuit for 600 or 900Ω.

Digital signal processor

The digital signal processor contains the RAM and ROM required to perform signal processing.

FSK test generator

The FSK test generator filters digital PCM data to remove noise. The generator uses a delayed product technique to demodulate the FSK. To recover data, the generator uses a 1.36 ms clock synchronized to zero paths of the demodulated data.

Trunk-signaling circuit

The CPU controls the trunk-signaling circuit for this function. The trunk-signaling circuit uses E-lead and M-lead modes. The trunk-signaling circuit receives and transmits the E signaling data between the CPU and the PBX.

MUX

The MUX receives data from the trunk signaling circuit. The MUX sends the data to the simplex (SX) circuits, the E-lead detector and the trunk type detector.

Simplex circuits

The two simplex circuits monitor the tip (T) and ring (R) leads. The circuits monitor these leads to indicate idle, seizure, seizure acknowledged and disconnect circuit modes. The circuits operate relays. The circuits send high or low conditions to provide simplex signaling. The relays that the circuits operate and the lead conditions appear in the following table.

Relay operation (Sheet 1 of 2)

	Lead condition		
Relays operated	**SBD**	**RLS**	**EBD**
None	High	Low	Low
K1, K2, K3	High	High	High

Relay operation (Sheet 2 of 2)

Relays operated	Lead condition		
	SBD	**RLS**	**EBD**
K2, K3	Low	Low	High
K1	High	High	Low

The E-lead detector

The E-lead detector receives signals from the multiplexer. The E-lead detector indicates idle, seizure, seizure acknowledged and disconnect circuit modes. The detector operates relays. The detector sends high or low conditions to provide E signals. The relays that the E-lead detector operates and the lead conditions appear in the following table.

Relay operation

Relays operated	Lead condition		
	SBD	**RLS**	**EBD**
None	Low	Low	Low
K1, K2, K3	High	High	High
K2, K3	Low	Low	High
K1	High	High/Low	Low

Note: The K1 RLS may be high or low depending on the external resistance to ground on the M-lead.

Trunk type detector

The trunk type detector receives signals from the MUX. The trunk type detector informs the CPU of the type of trunk.

Relay driver

The relay driver uses signals from the CPU to operate relays that indicate seizure acknowledged and disconnect circuit modes.

CPU

The CPU controls the trunk signaling circuits. The CPU converts 2-out-of-5 code received from the digital signal processor to BCD data. The CPU transmits messages between the NT2X01AA and the DMS-100 CC. The CPU

NT2X01AA (continued)

performs diagnostic tests when the system detects faults. The CPU performs diagnostic tests when the CC requests tests.

MTM interface circuit

The MTM interface circuit provides an interface between the NT2X01AA and the MTM control card. The circuit uses MTM control signals to convert serial MTM data into parallel data. The circuit transmits the data to the CPU. The circuit provides a hardware reset function.

Technical data

You can manually select an input impedance of 900Ω +2.15µ5;F or 600Ω +2.15µ5;F for NT2X01AA. The transmission-receive level range for the card is -6 dBm to -27.5 dBm. The signal-to-noise ratio range is 43 dB to 37.5 dB.

The card has a receive data rate of 735.29 ±5 bps. The card has a bit duration rate of 1.36 ±0.05 ms. The transmission mode is a phase continuous FSK with a logic 1 level of 1850 Hz ±75 Hz and a logic 0 level of 1150 Hz ±50 Hz.

The normal connecting circuit of the card is a 118-A interconnecting unit or an equivalent circuit that uses C25 signaling. The signaling characteristics of the card appear in the following table.

Signaling characteristics

Characteristics	Value
Battery voltage	-42.75 V to -55.50V
Insulation resistance	30 k Ω minimum
Ground potential	±3V maximum
Simplex battery supervision range	0Ω το 1800Ω *(see note)*
Maximum external E-lead resistance	100Ω
Maximum E-lead current	6mA
Maximum M-lead current	100mA
Note: The maximum external resistance of T and R loop is 450 Ω (sx). The maximum external resistance of SX battery that the CO provides to the PBX is 1400 Ω. The internal SX battery resistance of an NT2X01 is 946 ohm nominal.	

Dimensions

The NT2X01AA has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 267 mm (10.5 in.)
- width: 56 mm (2.2 in.)

Power requirements

DANGER

Damage to equipment or loss of service

Only use telephone wiring that a Northern Telecom protector protects. The catalog number for the protector is 303M-12AIKE. Use the wiring with a 26-AWG copper wire with thermoplastic insulation. The maximum fusing wire you can use in series with the protector is 26 AWG.

The card converts voltages of +5V ±0.2V, +12V ±0.3V, -15V ±0.5V, and +22.8V to 27V, with a 24 nominal voltage. The power requirements for the NT2X01AA appear in the following table.

Power requirements

Circuit	Idle/PCP	Busy/PCP
Trunk signaling	2W	14W
Data receiver	5W	5W

NT2X05AA

Product description

The NT2X05AA line module converter +24V card provides a regulated 24V dc power supply. The NT2X05AA line module converter +24V card operates as a ringing generator in line modules (LM). The card operates as a ringing generator in remote line modules (RLM) in DMS-100 equipment.

The NT2X27 ringing generator interface card controls the NT2X05AA card for this function. The card provides a voltage source that you can program. The voltage source supplies ac or dc outputs over a wide range of frequencies and voltages.

Location

The card plugs in a standard DMS-100 equipment shelf.

Functional description

The NT2X05AA converts a nominal -48V current to a regulated +24V current. The card has monitors that shut down the converter if the output exceeds set limits. A bridge circuit works with the NT2X27 to produce ringing patterns.

Functional blocks

The NT2X05AA contains the following functional blocks:

- power switch
- power transformer
- control circuit
- two rectifier/filter circuits
- overvoltage protection and low voltage monitor
- two diodes
- drive circuit
- output bridge
- oscillator
- voltage and current monitor

Power switch

An oscillator controls the power switch for this function. The power switch receives a -48V input from an office battery. The power switch sends the current to the power transformer.

Power transformer

The power transformer steps down the voltage to provide a dc isolation current. The current runs between the -48V input and the floating +24V card output.

Control circuit

To regulate the +24V output, the control circuit controls the on and off times of power transistors in the power switch.

Rectifier/filter circuits

The two rectifier/filter circuits produce +390V and +24.3V outputs. The circuits rectify and filter the currents that the power transformer sends.

Overvoltage protection and low voltage monitor

The overvoltage protection and low voltage monitor shuts down the converter if the output voltage exceeds a threshold level. If you use the converter with a frame supervisory panel (FSP), the shutdown continues. The shutdown stops when you push the RESET button on the converter faceplate.

The monitor detects low voltage currents. The monitor lights a converter fail light-emitting diode (LED) on the converter faceplate if low voltage currents are present.

Diodes

The two diode circuits receive the +24.3V current from the two rectifier/filter circuits. The diode circuits output the regulated +24V card output. One diode circuit outputs the +24V current. This diode sends the signal to the second diode for transmission to a second NT2X05 card.

Drive circuit

The drive circuit receives an input signal from the NT2X27. The drive circuit sends the signal to the output bridge.

Output bridge

The output bridge receives signals from the drive circuit and +390 V from the rectifier/filter circuits. To control the duty cycle, the output bridge changes the output positively or negatively. The change in output generates voltage, frequency and waveform in specified limits.

NT2X05AA (continued)

The NT2X27 card is in the line module controller (LMC) of the LM or RLM. This NT2X27 determines the type of ringing pattern output from the card. Card types and ringing patterns appear in the following table.

Card types and ringing patterns

Card type	Ringing pattern
NT2X27AA	20 Hz bell system
NT2X27AB	Decimonic multifrequency (MF) ringing
NT2X27AC	Harmonic MF ringing
NT2X27AD	Synchromonic 16 Hz ringing
NT2X27AE	Synchromonic MF ringing

Oscillator

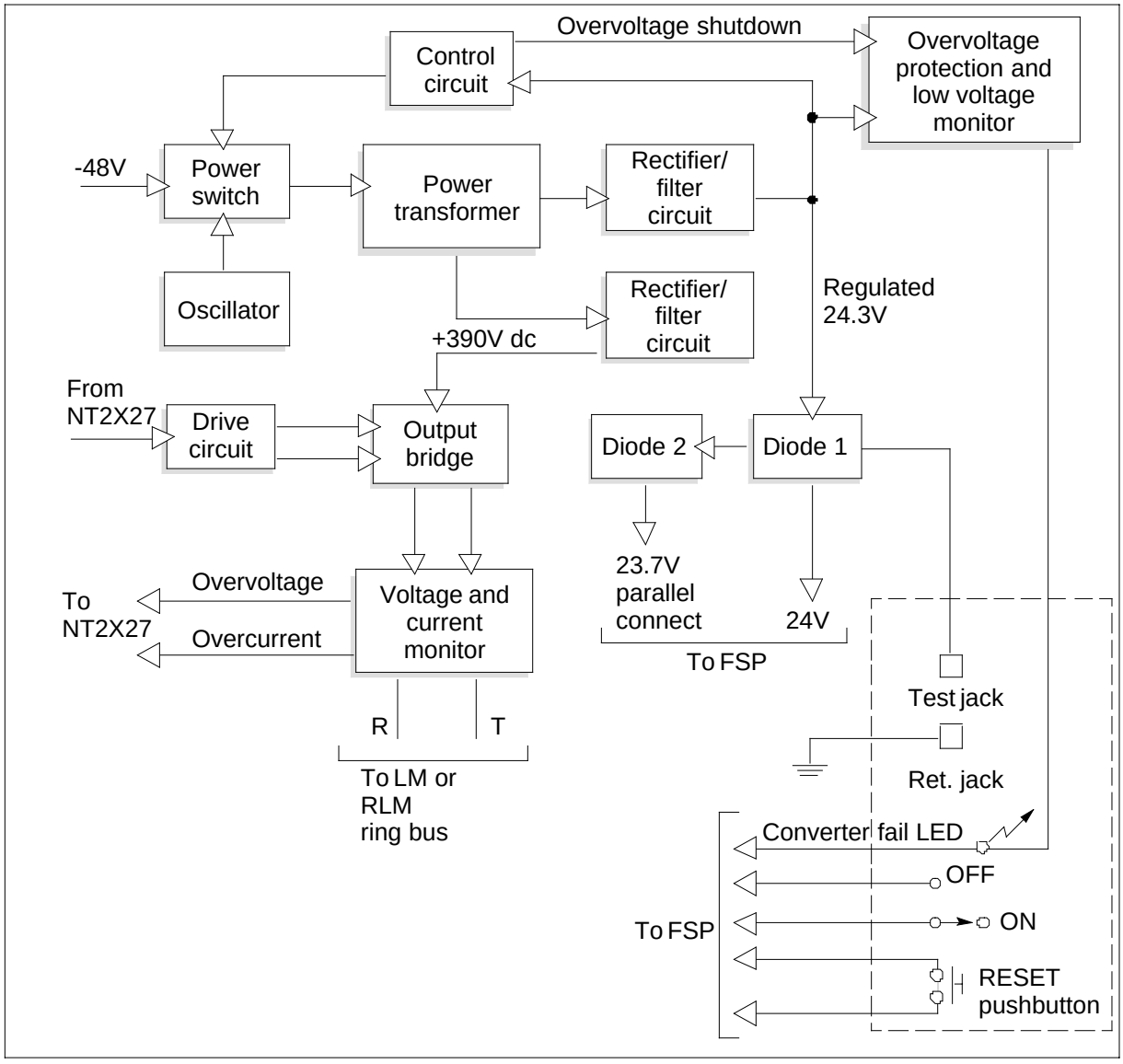
The oscillator uses a 20 kHz frequency to control the power switch.

Voltage and current monitor

The voltage and current monitor does not allow the output of the card to exceed set limits. The monitor transmits an output to the NT2X27 to reduce the input drive to the converter.

The relationship between the operating blocks appears in the following figure.

NT2X05AA functional blocks



NT2X05AA (continued)

Technical data

The converter has a ≥60 percent load range. The output specifications of the NT2X05AA appear in the following table.

Output specifications

Characteristics	Value
Voltage range	23.50V to 24.50V
Factory setting (at 6-A load)	24.00V ±0.05V
Maximum current	12.50A
Minimum current	1.20A
Maximum ripple	200rms
Overvoltage shutdown	29.00V
Overcurrent limiting	14.00A
Low voltage detection	20.00V

The following table lists the ringing output of the card when the NT2X27 controls the card.

Ringing output

Characteristic	Value
Voltage (range that can be programmed) For less than 1 second	-140V to +140V -240V to +240V
Frequency (range that can be programmed)	0 to 67 Hz
Maximum current	350mA
Overvoltage shutback1	>165V for >1.5 s
Voltage detect1	±20V nominal
Current detect[1]	±10mA nominal
Overcurrent shutback1	±350mA nominal
Note: Signal to NT2X27 ringing generator interface.	

dimensions

The NT2X05AA has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 66 mm (2.6 in.)

Power requirements

The maximum input voltage step is ±5 V. The power requirements for the NT2X05AA appear in the following table.

Power requirements

Voltage	Current
-42 V minimum	0.5 A
-48 V nominal	4.0 A
-56 V maximum	9 A

The maximum heat dissipation is 100W.

NT2X05AB

Product description

The NT2X05AB line module converter +24V card provides a regulated 24 V dc power supply. The card operates as a ringing generator in line modules (LM) and remote line modules (RLM) in DMS-100 equipment.

The NT2X27 ringing generator interface card controls the NT2X05AB for this function. The card provides a voltage source that you can program. The voltage source supplies ac or dc outputs over a wide range of frequencies and voltages.

Location

The card plugs into a standard DMS-100 equipment shelf.

Functional description

The NT2X05AB converts a nominal -48V current to a regulated +24V current. The card contains monitors that shut down the converter if the output exceeds set limits. A bridge circuit works with the NT2X27 to produce ringing patterns.

Functional blocks

The NT2X05AB contains the following functional blocks:

- power switch
- power transformer
- control circuit
- two rectifier/filter circuits
- overvoltage protection and low voltage monitor
- two diodes
- drive circuit
- output bridge
- oscillator
- voltage and current monitor

Power switch

The power switch receives a -48V input from an office battery. The power switch sends the current to the power transformer. An oscillator controls the power switch for this function.

Power transformer

The power transformer steps down the voltage to provide a dc isolation current. The current runs between the -48V input and the floating +24V card output.

Control circuit

To regulate the +24V output, the control circuit controls the on and off times of power transistors in the power switch.

Rectifier/filter circuits

The two rectifier/filter circuits produce +390V and +24.3V outputs. The circuits rectify and filter the currents that the power transformer sent.

Overvoltage protection and low voltage monitor

The overvoltage protection and low voltage monitor shuts down the converter if the output voltage exceeds a threshold level. If you use the converter with a frame supervisory panel (FSP), the shutdown continues. When you push the RESET button on the converter faceplate, the shutdown stops.

The monitor detects low voltage currents. The monitor lights a converter fail light-emitting diode (LED) on the converter faceplate if the monitor detects low voltage currents.

Diodes

The two diode circuits receive the +24.3V current from the two rectifier/filter circuits. The circuits output the regulated +24V card output. One diode circuit outputs the +24V current. This diode sends the signal to the second diode for transmission to a second NT2X05 card.

Drive circuit

The drive circuit receives an input signal from the NT2X27. The circuit sends the signal to the output bridge.

Output bridge

The output bridge receives signals from the drive circuit and +390V from the rectifier/filter circuits. To control the duty cycle, the output bridge changes the output positively or negatively. The change in output generates voltage, frequency and waveform in specified limits.

NT2X05AB (continued)

The NT2X27 card in the line module controller (LMC) of the LM or RLM determines the type of ringing pattern output. The card outputs the ringing pattern. Card types and ringing patterns appear in the following table.

Card types and ringing patterns

Card types	Ringing Pattern
NT2X27AA	20 Hz-bell system
NT2X27AB	Decimonic multifrequency (MF) ringing
NT2X27AC	Harmonic MF ringing
NT2X27AD	Synchromonic 16 Hz ringing
NT2X27AE	Synchromonic MF ringing

Oscillator

The oscillator uses a 20 kHz frequency to control the power switch.

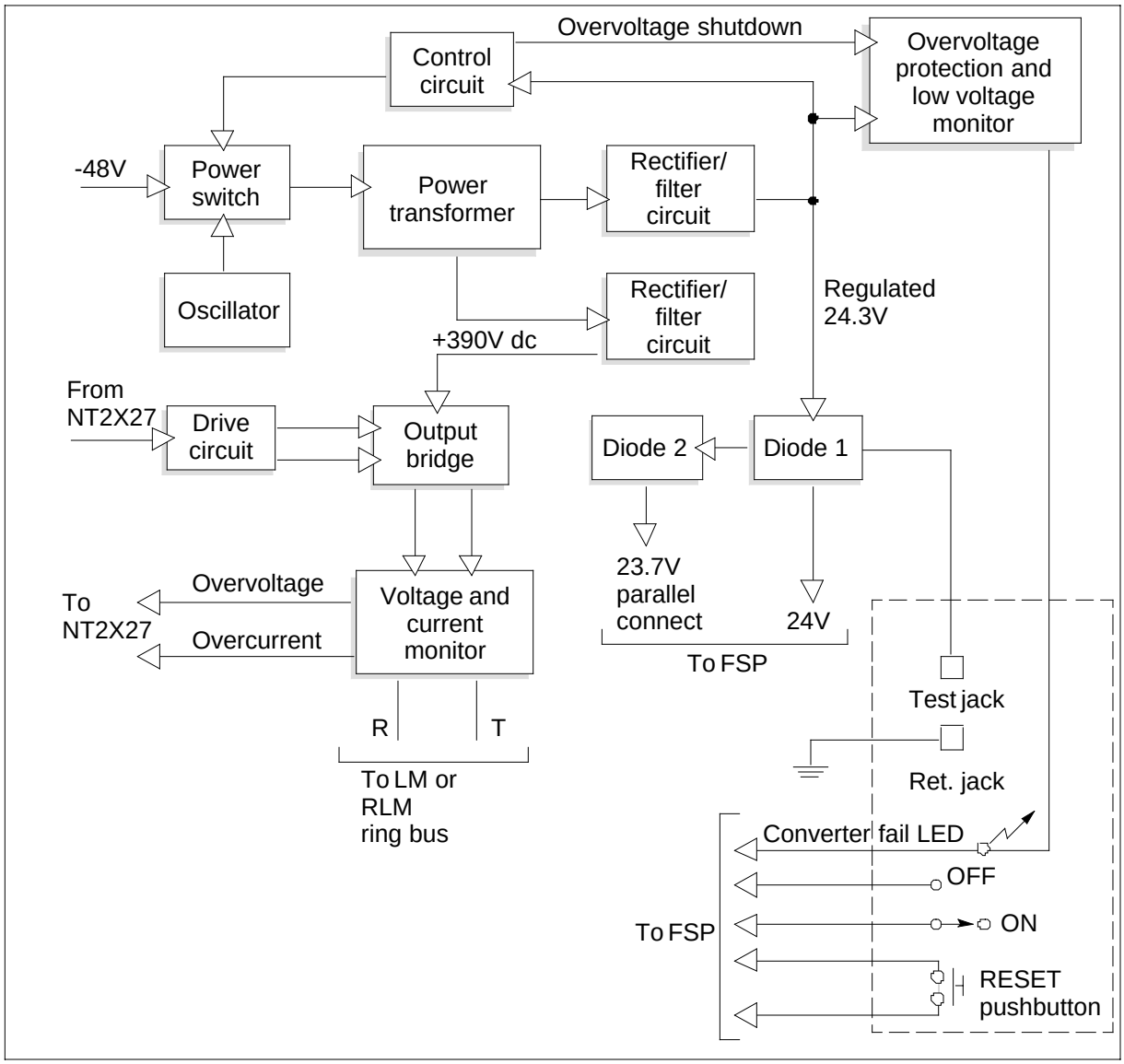
Voltage and current monitor

The voltage and current monitor does not allow the output of the card to exceed set limits. The voltage and current monitor transmits an output to the NT2X27 to reduce the input drive to the converter.

The relationship between the functional blocks appears in the following figure.

NT2X05AB (continued)

NT2X05AB functional blocks



NT2X05AB (continued)

Technical data

The converter has a ≥60 percent load range. The output specifications of the NT2X05AB appear in the following table.

Output specifications

Characteristic	Value
Voltage range	23.50V to 24.50V
Factory setting (at 6-A load)	24.00V ±0.05V
Maximum current	15.50A
Minimum current	0.00A
Maximum ripple	200rms
Overvoltage shutdown	29.00V
Overcurrent limiting	18.25A
Low voltage detection	20.00V

The following table lists the ringing output of the card when the NT2X27 controls the card.

Ringing output

Characteristic	Value
Voltage (range that can be programmed) For less than 1 second	-140V to +140V -240V to +240V
Frequency (range that can be programmed)	0 to 67 Hz
Maximum current	350mA
Overvoltage shutback[1]	>165 V for >1.5 s
Voltage detect[1]	±20V nominal
Current detect[1]	±10 mA nominal
Overcurrent shutback[1]	±350 mA nominal
Note: Signal to NT2X27 ringing generator interface	

Dimensions

The NT2X05AB has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 66 mm (2.6 in.)

Power requirements

The maximum input voltage step is ±5V. The power requirements for the NT2X05AB appear in the following table.

Power requirements

Voltage	Current
-42V minimum	0.5A
-48V nominal	4. A
-56V maximum	9.0A

The maximum heat distribution is 100W.

NT2X05AC

Product description

The NT2X05AC line module (LM) power pack with improved grounding card performs the following functions:

- provides a regulated 24V dc power supply
- operates as a ringing generator in LMs and remote line modules (RLM) in DMS-100 equipment

Under control of the NT2X27 ringing generator interface card, the NT2X05AC card provides a programmable voltage source. The source supplies ac or dc outputs on a range of frequencies and voltages.

The card prevents noise in NT6X21AA or NT6X21AB business set line cards when the following cards combine:

- LM and line concentrating module (LCM)
- RLM and remote line concentrating module (RLCM)

Location

Plug the card in a standard DMS-100 equipment shelf.

Functional description

The NT2X05AC converts a small -48V current to a regulated +2V current. The card monitors shut down the converter if the output exceeds established limits. A bridge circuit works with the NT2X27 to produce ringing patterns.

Functional blocks

The NT2X05AC consists of the following functional blocks:

- power switch
- power transformer
- control circuit
- two rectifier/filter circuits
- overvoltage protection and low voltage monitor
- two diodes
- drive circuit
- output bridge
- oscillator
- voltage and current monitor

Power switch

The power switch, under control of an oscillator, receives a -48V input from an office battery. The switch sends the current to the power transformer.

Power transformer

The power transformer steps down the voltage to provide a dc isolation current between the -48V input and the floating +24V card output.

Control circuit

The control circuit controls the times when power transistors can go on and off in the power switch to regulate the +24V output.

Rectifier/filter circuits

The two rectifier/filter circuits rectify and filter the currents from the power transformer to produce +390V and +24.3V.

Overvoltage protection and low voltage monitor

The overvoltage protection and low voltage monitor shuts down the converter when the output voltage exceeds a threshold level. If you use the converter with a frame supervisory panel (FSP), the shutdown continues until you push the RESET button. The reset button is on the converter faceplate.

The monitor detects low voltage currents. The monitor lights a converter fail light-emitting diode (LED) on the converter faceplate if low voltage currents occur.

Diodes

The two diode circuits receive the +24.3V current from the two rectifier/filter circuits and output the regulated +24V card output. One diode circuit outputs the +24V current. The diode sends the signal to the second diode for transfer to a second NT2X05 card.

Drive circuit

The drive circuit receives an input signal from the NT2X27 and sends the signal to the output bridge.

Output bridge

The output bridge receives signals from the drive circuit and +390V from the rectifier/filter circuits. The bridge changes the positive or negative output to generate limited voltage, frequency and waveform. This action controls the duty cycle.

NT2X05AC (continued)

The NT2X27 card in the line module controller (LMC) of the LM or RLM determines the type of ringing pattern the card outputs. The following table lists the card types and the ringing patterns.

Card types and ringing patterns

Card type	Ringing pattern
NT2X27AA	20 Hz bell system
NT2X27AB	Decimonic multifrequency (MF) ringing
NT2X27AC	Harmonic MF ringing
NT2X27AD	Synchromonic 16 Hz ringing
NT2X27AE	Synchromonic MF ringing

Oscillator

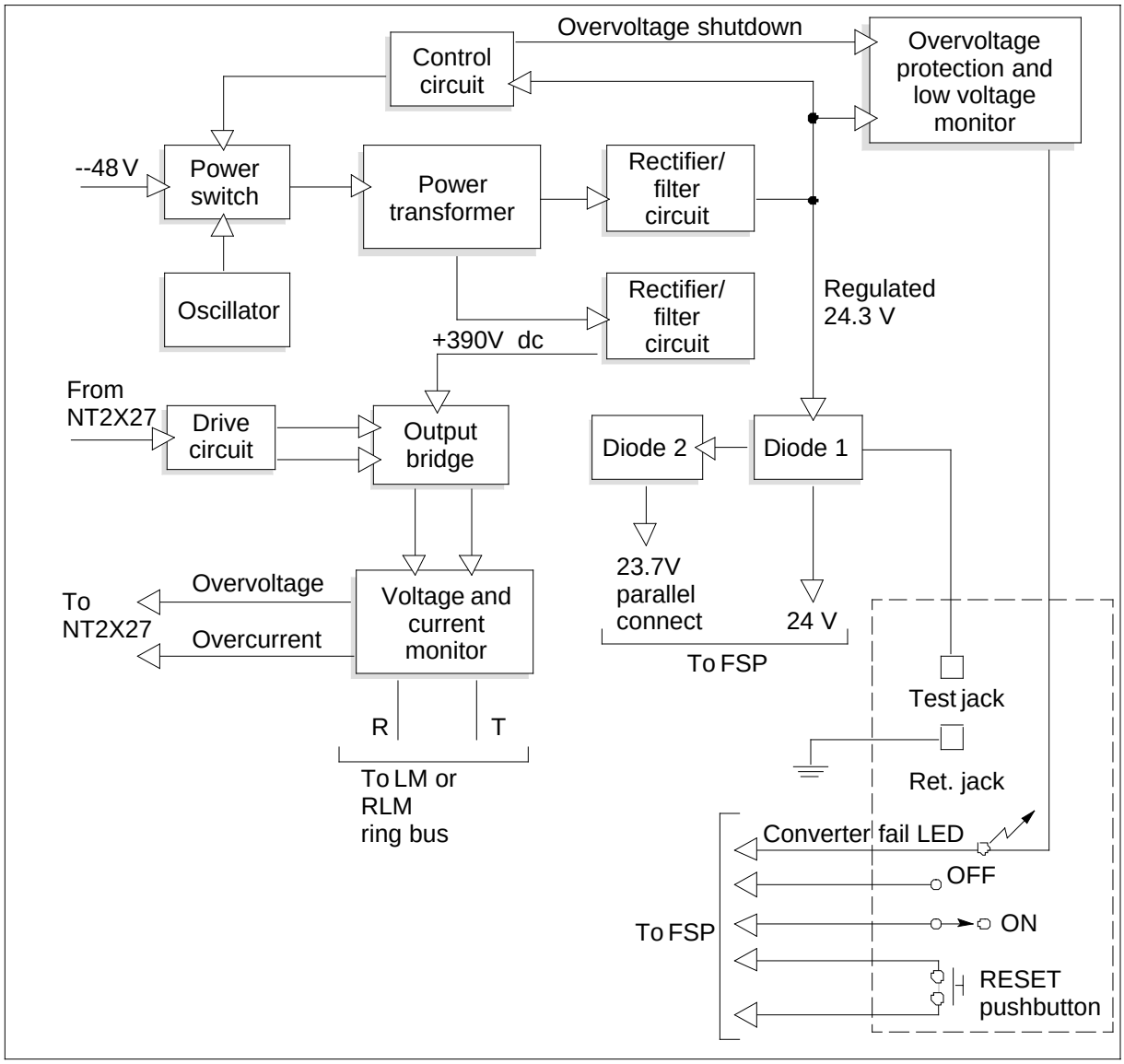
The oscillator uses a 20 kHz frequency to control the power switch.

Voltage and current monitor

The voltage and current monitor transmits an output to the NT2X27 to reduce the input drive to the converter. This action makes sure the card output does not exceed predetermined limits.

The relationship between the functional blocks appears in the following figure.

NT2X05AC functional blocks



NT2X05AC (continued)

Technical data

The converter has a ≥60 percent load range. The following table lists the output requirements of the .

Output specifications

Characteristic	Value
Voltage range	23.50V to 24.50V
Factory setting (at 6-A load)	24.00V ±0.05V
Maximum current	12.50A
Minimum current	1.20A
Maximum ripple	200rms
Overvoltage shutdown	29.00V
Overcurrent limiting	14.00A
Low voltage detection	20.00V

The ringing output of the card when the NT2X27 controls the ringing output appears in the following table.

Ringing output

Characteristic	Value
Voltage (programmable range) For less than 1 s	-140V to +140V -240V to +240V
Frequency (programmable range)	0 to 67 Hz
Maximum current	350mA
Overvoltage shutback[1]	>165V for >1.5 s
Voltage detect[1]	±20V nominal
Current detect[1]	±10mA nominal
Overcurrent shutback[1]	±350mA nominal
Note: Signal to NT2X27 ringing generator interface	

Dimensions

The NT2X05AC has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 66 mm (2.6 in.)

Power requirements

The maximum input voltage step is ±5V. The following table lists the power requirements for the .

Power requirements

Voltage	Current
-42V minimum	0.5A
-48V nominal	4.0A
-56V maximum	9.0A

The maximum heat distribution is 100W.

NT2X06AB

Product description

The NT2X06AB power converter common features card provides a regulated, floating, 5V dc, 40A power supply. The DMS-100 equipment uses the power supply.

Location

Plug the card in a standard DMS-100 equipment shelf.

Functional description

The NT2X06AB receives a small -48V input and converts the input to a regulated 5V output. The card monitors the output and shuts down the converter if the output exceeds a controlled threshold.

Functional blocks

The NT2X06AB consists of following functional blocks:

- power switch
- power transformer
- rectifier/filter circuit
- overcurrent monitor circuit
- overvoltage monitor
- low voltage monitor
- magnetic amplifier
- oscillator

Power switch

The power switch receives a -48V input from an office battery. The switch sends the current to the power transformer. The oscillator controls the power switch.

Power transformer

The power transformer lowers the voltage to provide a dc isolation current between the -48V input and the floating 5V card output.

Rectifier/filter circuit

The rectifier/filter circuit uses a regulated voltage sent through the magnetic amplifier to filter the current and output a regulated 5V current.

Overcurrent monitor circuit

The overcurrent monitor circuit activates if the output from the rectifier/filter circuit exceeds a preset level. If an overload occurs, the circuit reduces the output voltage to limit the output current to a safe value.

Overvoltage monitor

The overvoltage monitor shuts down the converter if the output voltage exceeds a threshold level. If you use the converter with a frame supervisory panel (FSP), the shutdown continues until you push the RESET button. The RESET button is on the converter faceplate.

Low voltage monitor

The low voltage monitor detects low voltage currents. The low voltage monitor lights a converter fail light-emitting diode (LED) on the converter faceplate if low voltage currents occur.

Magnetic amplifier

The magnetic amplifier uses pulse width modulation of the drive signal to regulate the output voltage.

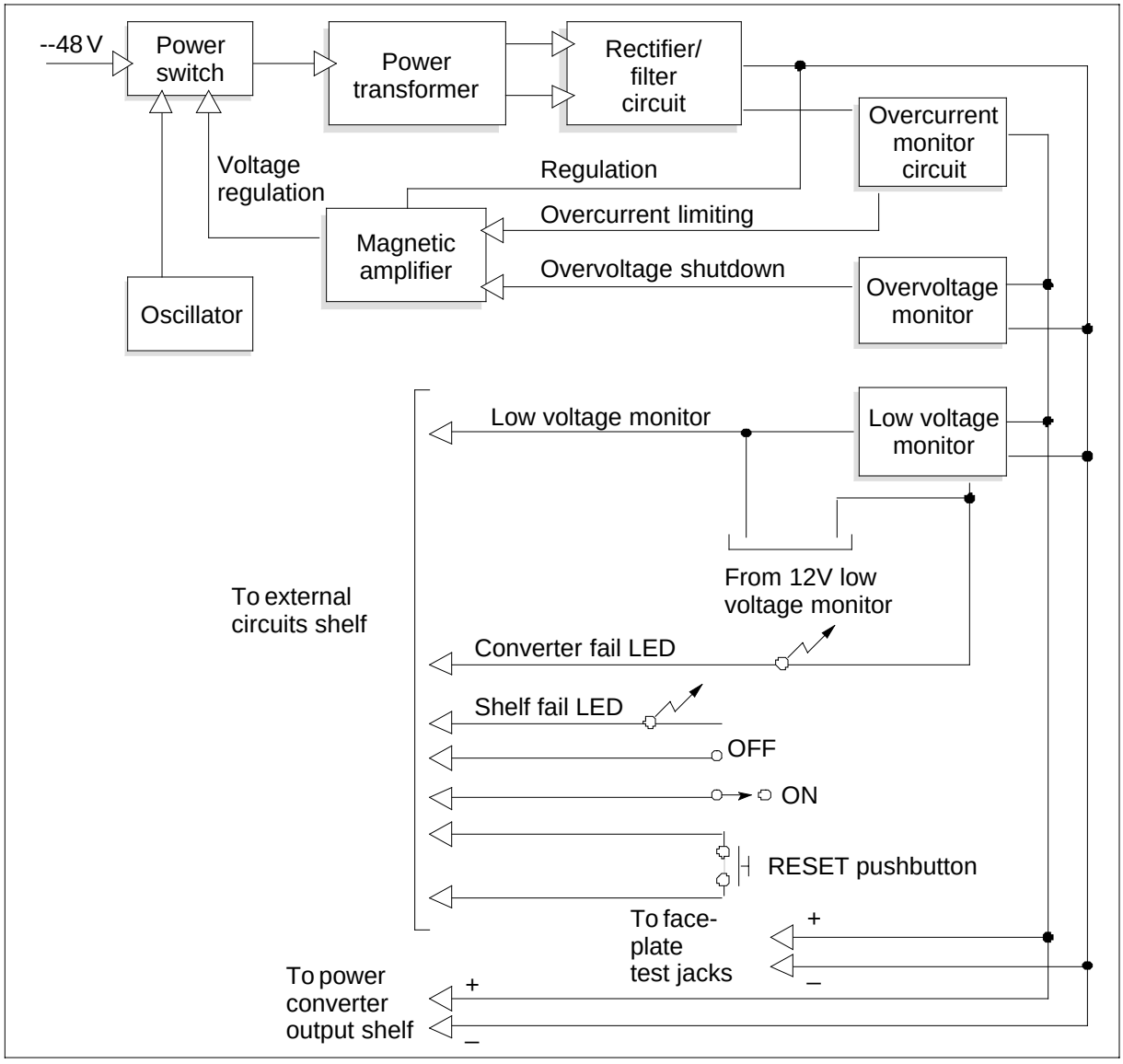
Oscillator

The oscillator uses a 20 kHz frequency to control the power switch.

The relationship between the functional blocks appears in the following figure.

NT2X06AB (continued)

NT2X06AB functional blocks



Technical data

The converter has a >75 percent load range. The following table lists the output specifications of the NT2X06AB.

Output Specifications

Characteristic	Value
Floating voltage	4.9V to 5.2V
Maximum ripple voltage peak to peak	100mV
Maximum current with forced air cooling	40.0A
Maximum current with convection cooling	30.0A
Overvoltage shutdown	6.0V
Overcurrent limiting	45.0A
Low voltage detection	4.0V

Dimensions

The NT2X06AB has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 66 mm (2.6 in.)

Power requirements

The maximum input voltage step is ±5V. The following table lists the power requirements for the NT2X06AB .

Power requirements

Voltage	Current
-42V minimum	0.5A
-48V nominal	4.0A
-56V maximum	6. A

The maximum heat distribution is 67 W.

NT2X06B

Product description

The NT2X06B power converter card provides a regulated, floating, 5V dc, 40A power supply for use in DMS-100 equipment.

Location

Plug the card in a standard DMS-100 equipment shelf.

Functional description

The NT2X06B receives a small -48V input and converts the input to a regulated 5-V output. The card monitors the output and shuts down the converter if the output exceeds a recommended threshold.

Functional blocks

The NT2X06B consists of the following functional blocks:

- power switch
- power transformer
- rectifier/filter circuit
- overcurrent monitor circuit
- overvoltage monitor
- low voltage monitor
- magnetic amplifier
- oscillator

Power switch

The power switch receives a -48V input from an office battery. The power switch sends the current to the power transformer. The power switch is under the control of the oscillator.

Power transformer

The power transformer reduces the voltage to provide a dc isolation current between the -48V input and the floating 5V card output.

Rectifier/filter circuit

The rectifier/filter circuit uses a regulated voltage sent through the magnetic amplifier to filter the current. The rectifier/filter outputs a regulated 5V current.

Overcurrent monitor circuit

The system activates the overcurrent monitor circuit if the output from the rectifier/filter circuit exceeds a preset level. When an overload occurs, the circuit reduces the output voltage to limit the output current to a safe value.

Overvoltage monitor

The overvoltage monitor shuts down the converter if the output voltage exceeds a threshold level. If you use the converted with a frame supervisory panel (FSP), the shutdown continues until you push the RESET button. The RESET button is on the converter faceplate.

Low voltage monitor

The low voltage monitor detects low voltage currents. This monitor lights a converter fail light-emitting diode (LED) on the converter faceplate if low voltage currents occur.

Magnetic amplifier

The magnetic amplifier uses pulse width modulation of the drive signal to regulate the output voltage.

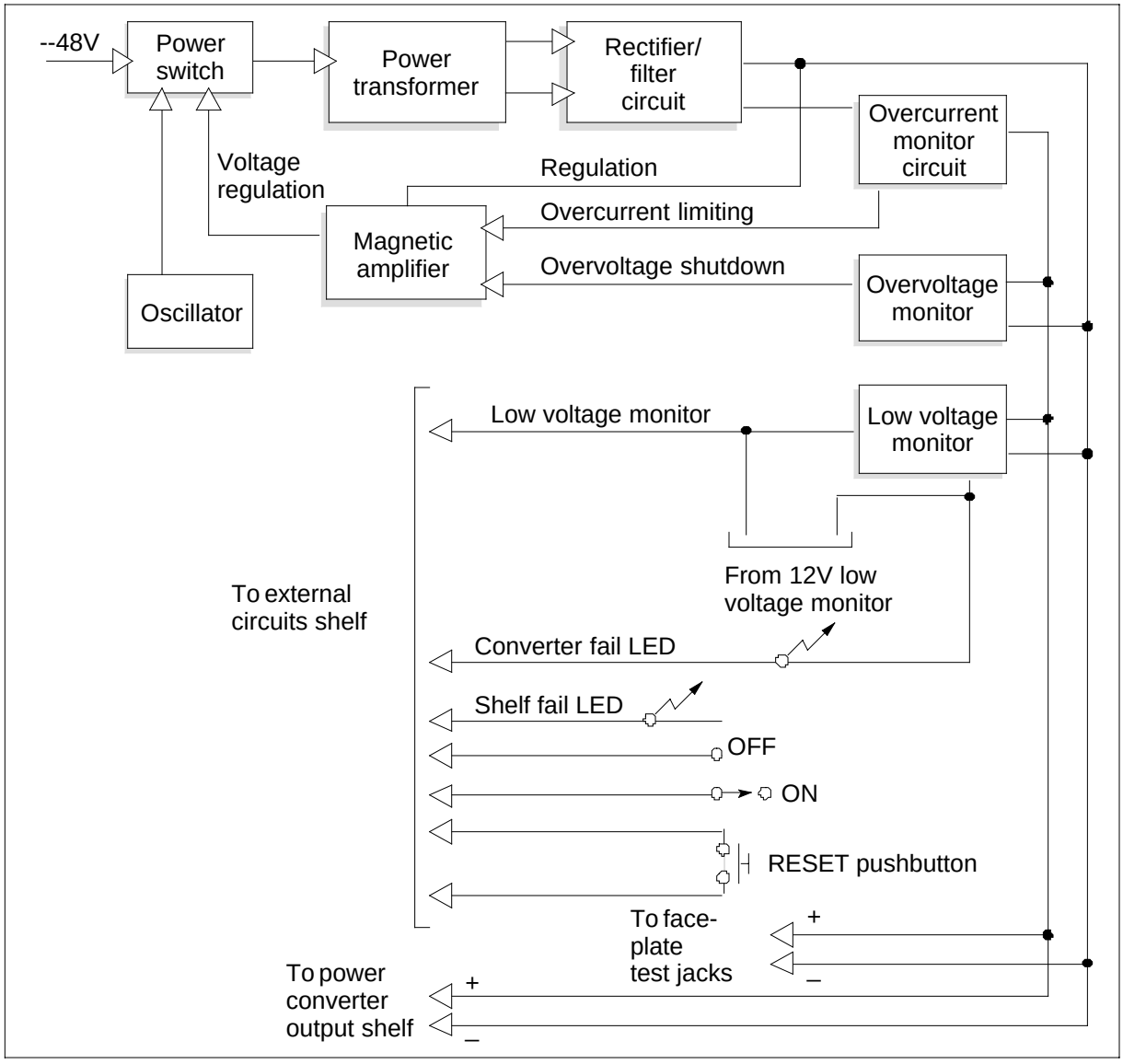
Oscillator

The oscillator uses a 20 kHz frequency to control the power switch.

The relationship between the functional blocks appears in the following figure.

NT2X06B (continued)

NT2X06B functional blocks



Technical data

The converter has a >75 percent load range. The output specifications of the NT2X06B appear in the following table.

Output specifications

Characteristic	Value
Floating voltage	4.9V to 5.2V
Maximum ripple voltage peak to peak	100mV
Maximum current with forced air cooling	40.0A
Maximum current with convection cooling	30 A
Overvoltage shutdown	6.0V
Overcurrent limiting	45.0A
Low voltage detection	4 V

Dimensions

The dimensions for the NT2X06B has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 66 mm (2.6 in.)

Power requirements

The maximum input voltage step is ±5V. The power requirements for the NT2X06B appear in the following table.

Power requirements

Voltage	Current
-42V minimum	0.5A
-48V nominal	4.0A
-56V maximum	6.3A

The maximum heat distribution is 67W.

NT2X07AB

Product description

The NT2X07AB power converter (5V/12V) card provides the following regulated, floating power supplies for use in DMS-100 equipment:

- 5V dc
- 12A
- 12V dc
- 5A

Location

Plug the card in a standard DMS-100 equipment shelf.

Functional description

The NT2X07AB receives a small -48V input and converts the input to regulated 5V and 12V outputs. The card monitors the outputs and shuts down the converter if the outputs exceed recommended thresholds.

Functional blocks

The NT2X07AB consists of the following functional blocks:

- 5V power switch
- 12V power switch
- two power transformers
- two rectifier/filter circuits
- two overcurrent monitor circuits
- two overvoltage monitors
- two low voltage monitors
- two magnetic amplifiers
- two oscillators

5V power switch

The 5V power switch receives a -48V input from an office battery and sends the current to the power transformer in the 5V circuits.

12V power switch

The 12V power switch receives a -48V input from an office battery and sends the current to the power transformer in the 12V circuits.

Power transformers

The power transformers step down the voltage to provide a dc isolation current between the -48V input and the floating 5V and 12V card outputs.

Rectifier/filter circuits

The rectifier/filter circuits use regulated voltages sent through the magnetic amplifiers to filter the current 5V. The circuits output a regulated 5V current from the 5V circuits and a regulated 12V current from the 12V circuits.

Overcurrent monitor circuits

The overcurrent monitor circuits activates when the outputs from the rectifier/filter circuits exceed preset levels. If an overload occurs, the circuits reduce the output voltages to limit the output currents to a safe value.

Overvoltage monitors

The overvoltage monitors shut down the converter if the output voltages exceed preset levels. If you use the converters with a frame supervisory panel (FSP), shutdown continues until you press the RESET button. The RESET button is on the converter faceplate.

Low voltage monitors

Low voltage monitors light a converter fail LED on the converter faceplate when the low voltage monitors detect low voltage currents.

Magnetic amplifiers

The magnetic amplifiers use pulse width modulation of the drive signals to regulate the output voltages.

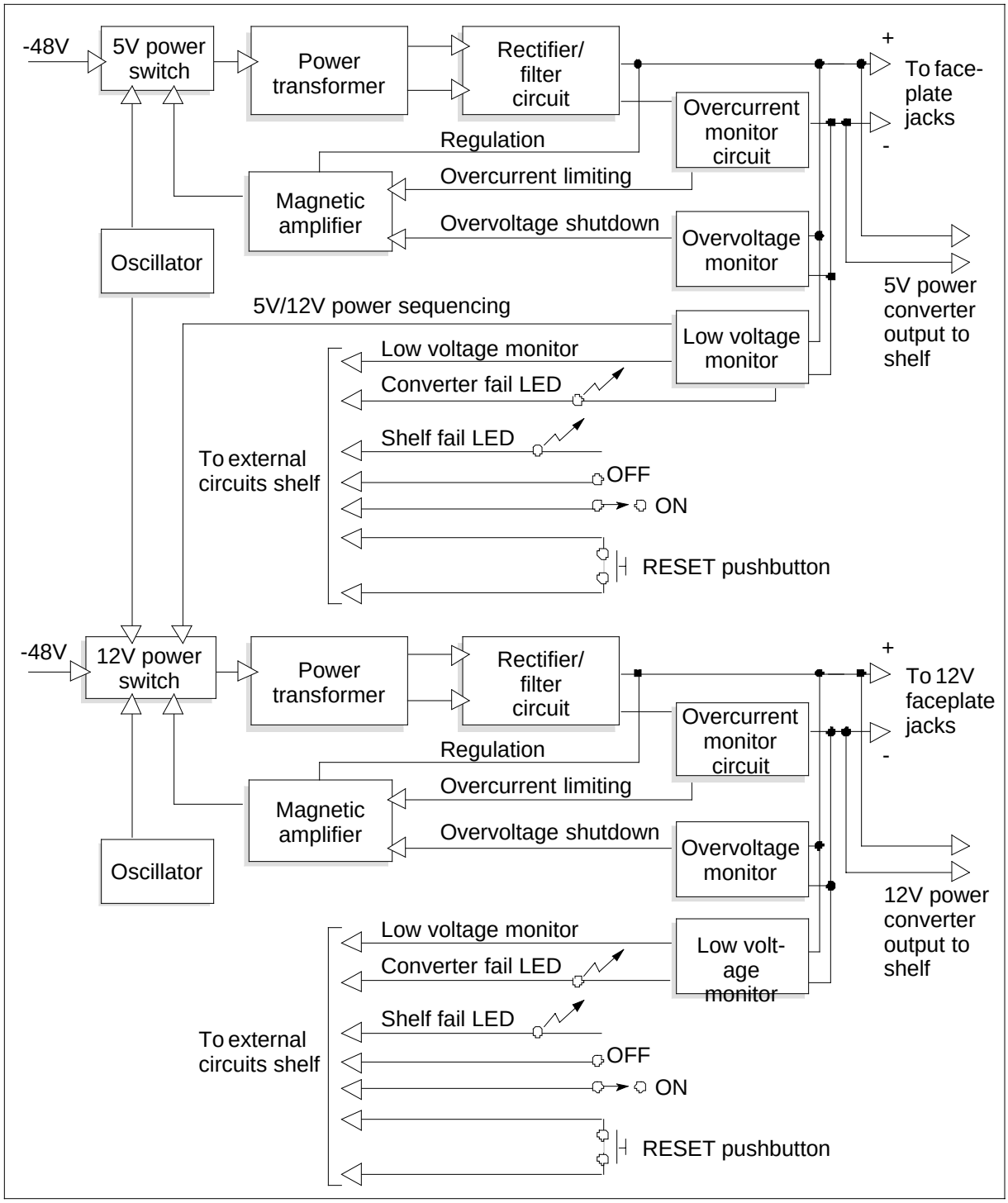
Oscillators

The two oscillators use 20 kHz frequencies to control the power switches.

The relationship between the functional blocks appears in the following figure.

NT2X07AB (continued)

NT2X07AB functional blocks



Technical data

The converter has a >70 percent load range. The following table lists the 12V output specifications of the card.

Output specifications 12V

Characteristic	Value
Floating voltage	11.7V to 12.3V
Maximum ripple voltage peak to peak	240mV
Maximum current	5A
Overvoltage shutdown	14V
Overcurrent limiting	6A
Low voltage detection	10V

The following table lists the 5V output specifications of the card.

Output specifications 5V

Characteristic	Value
Floating voltage	4.9V to 5.2V
Maximum ripple voltage peak to peak	100mV
Maximum current	12A
Overvoltage shutdown	6V
Overcurrent limiting	15A
Low voltage detection	4V

Dimensions

The has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 66 mm (2.6 in.)

NT2X07AB (end)

Power requirements

The maximum input voltage step is ±5V. The power requirements for the NT2X07AB appear in the following table.

Power requirements

Voltage	Current
-42V minimum	0.5 A
-56V maximum	4.0 A

The maximum heat distribution is 51W.

Product description

The NT2X09AA multi-output power converter card provides five regulated common-ground dc power supplies for DMS-100 equipment.

Location

Plug the card in a standard DMS-100 equipment shelf.

Functional description

The NT2X09AA receives a small -48V input and converts the input to regulated +5V, +12V, -5V, -15V, and +24V outputs. The card monitors the outputs and shuts down the converter if the outputs exceed a recommended threshold.

Functional blocks

The NT2X09AA consists of the following functional blocks:

- two power switches
- two power transformers
- two control circuits
- oscillator
- two rectifier/filter circuits
- +12V regulator
- -5V regulator
- overvoltage protection and low voltage monitor

Power switches

The power switches receive the -48V input from the office battery. The switches chop the input in a square-wave voltage under control of the control circuits. Apply the voltage across the primary windings of the power transformer. The duty cycle of this square-wave voltage varies by the control circuits.

Power transformers

The power transformers step down the voltages that the power switches apply across the primary winding. This action produces the required voltages across the secondary windings.

NT2X09AA (continued)

Control circuits

The control circuits change the duty cycle of the power switches to achieve the following:

- voltage regulation for the +5V output for one group of switch, transformer, and control
- voltage regulation for the -15V output for the other group of switch, transformer, and control

To achieve regulation, the circuits sense the appropriate output voltage and compare the appropriate voltage to a reference voltage. The circuits adjust the duty cycle of the switch.

A voltage that represents the output current in each switch provides the current limit function for that switch. This function allows the control circuits to shut down the power switches and remove the output voltage.

Oscillator

In the absence of an external clock signal, the oscillator runs at approximately 30 kHz. Normally, an external clock signal applies 32 kHz to the power converter. The oscillator cannot move from this frequency. This frequency minimizes system interference from noise that the power switches generate.

Rectifier and filter circuits

The secondary output windings of one power transformer produces the outputs. These outputs are rectified and filtered to eliminate noise and ripple and produce the required dc output. Additional regulation is not required for the +5V, -15V, and +24V outputs. A fuse on the faceplate of the NT2X09KA provides overload protection for the +24V output.

+12V regulator

The output of the +12V rectifier and filter is post-regulated to produce the required tolerance on the +12V output. This +12V regulator provides current limiting of this output.

-5V regulator

A part of the -15V output is post-regulated to produce the required tolerance on the -5V output . This -5V regulator provides current limiting of this output.

Overvoltage protection and low voltage monitor

The overvoltage protection circuit detects an overvoltage condition on the +12V, +5V, -15V, and -5V outputs when voltages exceed a preset level. The circuit sends a signal to the control circuits to shut down the power converter. The circuit does not monitor the +24V output for overvoltage.

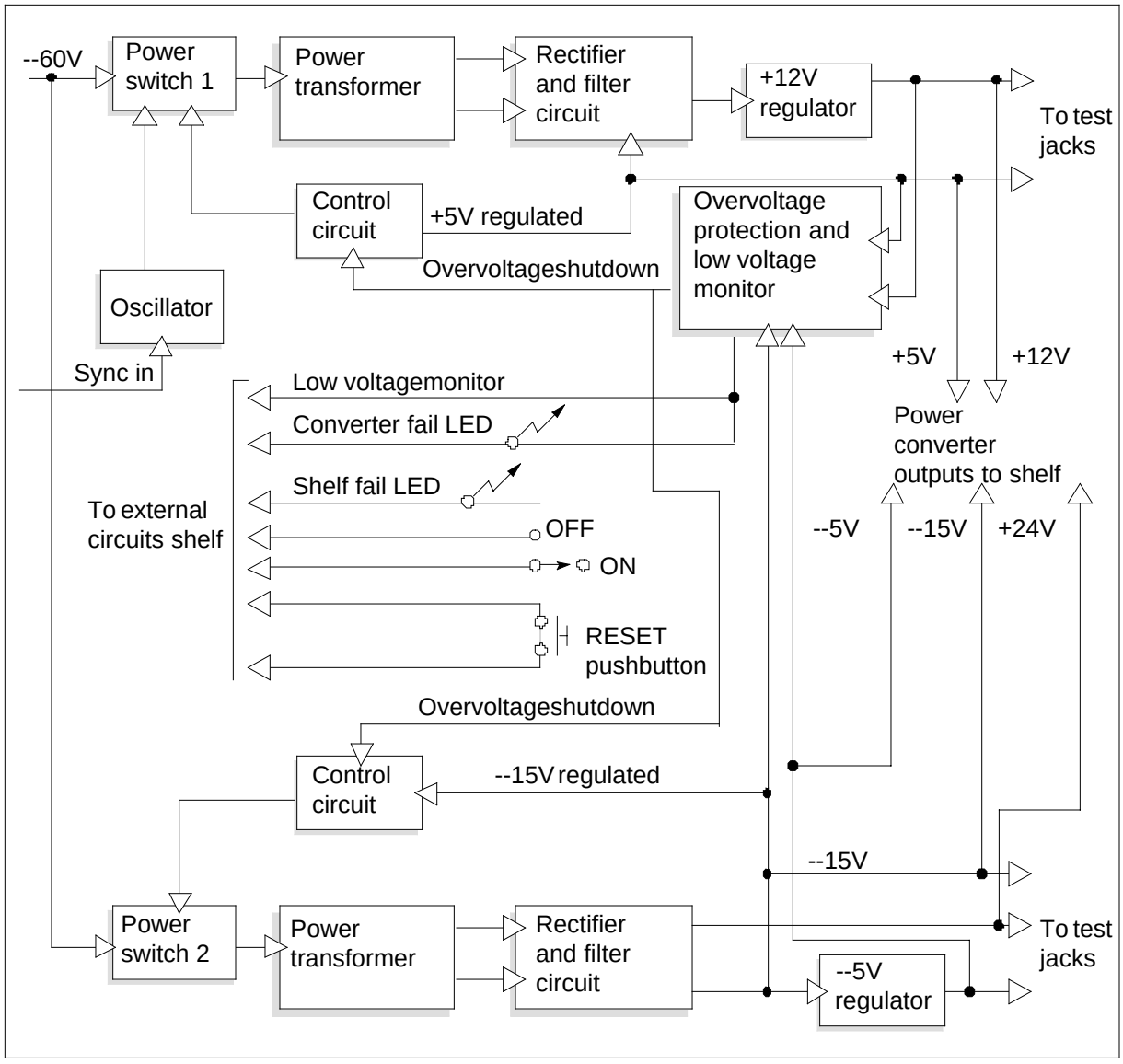
The circuit sends a signal to the frame supervisory panel (FSP). The signal disables input power to the converter and keeps the converter in the shut-down mode until you press the RESET button. The RESET button is on the converter faceplate.

The low-voltage monitor circuit detects low voltage conditions on any output. The monitor also causes a light-emitting diode (LED) on the converter faceplate to light.

The following figure describes the relationship between the functional blocks.

NT2X09AA (continued)

NT2X09AA functional blocks



Technical data

The converter has a 60-percent to 70-percent load range. The following table lists the output specifications for the +24V output.

Output specifications+ 24V

Characteristics	Value
Voltage	+22.5V to +28.0V
Maximum current	1.2A
Current limiting	2A
Low voltage detection	+18V

The following table lists the output specifications for the +12V output.

Output specifications + 12V

Characteristics	Value
Voltage	+11.7V to +12.3 V
Maximum ripple and spikes peak to peak	250mV
Maximum current	2.A
Overvoltage shutdown	+13.2V
Overcurrent limiting	3.0 A
Low voltage detection	+10V

The output specifications for the +5V output appear in the following table.

Output specifications + 5V (Sheet 1 of 2)

Characteristic	Value
Voltage	+4.9 V to +5.1 V
Maximum ripple and spikes peak to peak	100mV
Maximum current	8.5 A
Overvoltage shutdown	+7.1 V

NT2X09AA (continued)

Output specifications + 5V (Sheet 2 of 2)

Characteristic	Value
Overcurrent limiting	10.0 A
Low voltage detection	+4 V

The output specifications for the -15V output appear in the following table.

Output specifications -15V

Characteristic	Value
Voltage	+14.5V to -15.5 V
Maximum ripple and spikes peak to peak	250mV
Maximum current	1.5 A
Overvoltage shutdown	-16.7 V
Overcurrent limiting	2.A
Low voltage detection	-12V

The output specifications for the -5V output appear in the following table.

Output specifications -5V

Characteristic	Value
Voltage	-4.80V to -5.20 V
Maximum ripple and spikes peak to peak	100 mV
Maximum current	0.15 A
Overvoltage shutdown	-5.60 V
Overcurrent limiting	0.25 A
Low voltage detection	-4 V

Dimensions

The NT2X09AA has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 62 mm (2.45 in.)

Power requirements

The maximum input voltage step is ±5V. The power requirements for the NT2X09AA appear in the following table.

Power requirements

Voltage	Current
-42V minimum	0.5A
-56V maximum	5 A

The maximum heat distribution is 70W.

NT2X09BA

Product description

The NT2X09BA multiple output power converter with electromagnetic interference (EMI) shield card provides five regulated common-ground dc power supplies. The DMS-100 equipment uses these power supplies.

The EMI shield connects to the solder side of the card. This connection reduces the EMI that radiates out from the solder side of the paddle board.

Location

The card plugs into a standard DMS-100 equipment shelf.

Functional description

The NT2X09BA receives a nominal -48V input. The NT2X09BA converts the input to regulated +5V, +12V, -5V, -15V and +24V outputs. The card monitors the outputs and shuts down the converter if the outputs exceed a specified threshold.

Functional blocks

The NT2X09BA consists of the following functional blocks:

- two power switches
- two power transformers
- two control circuits
- oscillator
- two rectifier and filter circuits
- +12V regulator
- -5V regulator
- overvoltage protection and low voltage monitor

Power switches

The control circuits control the power switches for this function. The power switches receive the -48V input from the office battery. The power switches divide the input into a square-wave voltage. The power switches apply this voltage across the primary windings of the power transformer. The control circuits vary the duty cycle of this square-wave voltage.

Power transformers

The power transformers step down the voltages that the power switches apply across the primary windings. The power transformers step down the voltages to produce the required voltages across the secondary windings.

Control circuits

The control circuits rotate the duty cycle of the power switches to achieve voltage regulation for specified combinations of switch, transformer and control. Power switches can achieve voltage regulation for the +5V output for one combination. Power switches can achieve voltage regulation for the -15V output for the other combination. To achieve this regulation, the control circuits sense the correct output voltage. The control circuits compare the output voltage to a reference voltage. The control circuits adjust the duty cycle of the switch, if necessary.

A voltage that represents the output current in each switch provides the current limit function for that switch. This function allows the control circuits to shut down the power switches and remove the output voltage.

Oscillator

If an external clock signal is not present, the oscillator runs at 30 kHz. Normally, an external clock signal of 32 kHz is applied to the power converter. The oscillator is locked to this frequency, which minimizes system interference from noise that the power switches generate.

Rectifier and filter circuits

The secondary output windings of a power transformer produce outputs. The output windings rectify and filter outputs to eliminate noise and ripple. The output windings rectify and filter outputs to produce the required dc output. The +5V, -15V and +24V outputs do not require further regulation. A fuse on the faceplate of the NT2X09KA provides overload protection for the +24V.

+12V regulator

The output of the +12V rectifier and filter is post-regulated to produce the required tolerance on the +12V output. This +12V regulator also provides current limits of this output.

-5V regulator

A part of the -15V output is post-regulated to produce the required tolerance on the -5V output. The -5V regulator also provides current limits of this output.

Overvoltage protection and low voltage monitor

When voltages exceed a set level, the overvoltage protection circuit detects an overvoltage condition on the +12V, +5V, -15V and -5V outputs. The control circuits receive a signal to shut down the power converter. The system does not monitor the +24V output for overvoltage.

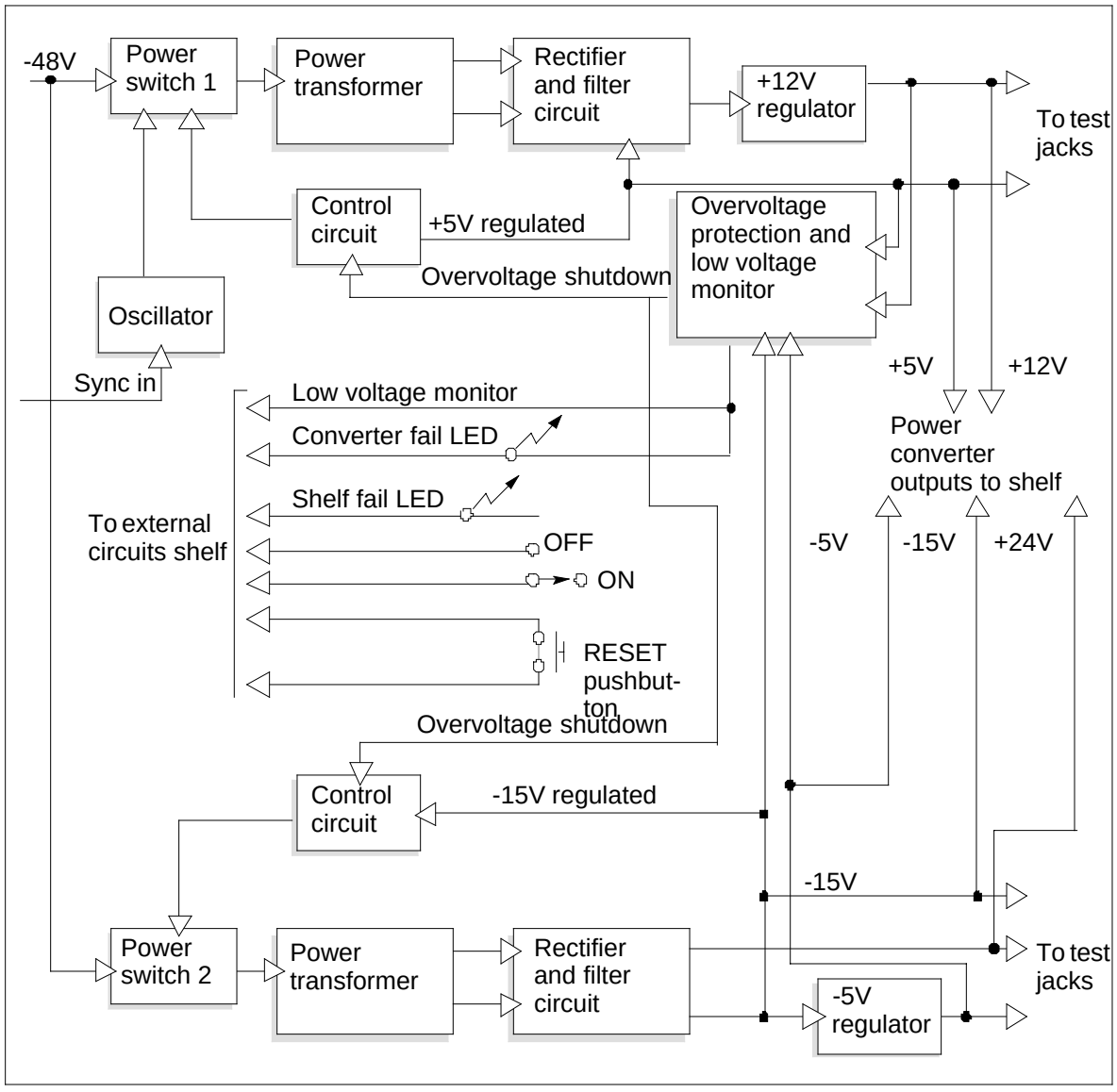
NT2X09BA (continued)

When the frame supervisory panel (FSP) receives a signal, input power to the converter is disabled. The signal keeps the converter in the shut down mode until you press the RESET button on the converter faceplate.

The low-voltage monitor circuit detects low voltage conditions on output. The monitor circuit causes a light-emitting diode (LED) on the converter faceplate to light.

The relationship between the functional blocks appear in the following figure.

NT2X09BA functional blocks



Technical data

The converter has a 60-percent to 70-percent load range. The output requirements for the +24V output appear in the following table.

Output requirements +24V

Characteristic	Value
Voltage	+22.5V to +28.0V
Maximum current	1.2A
Current limits	2.0A
Low voltage detection	+18.0V

The output requirements for the +12V output appear in the following table.

Output requirements +12V

Characteristic	Value
Voltage	+11.7V to +12.3V
Maximum ripple and spikes peak to peak	25 mV
Maximum current	2.0A
Overvoltage shutdown	+13.2V
Overcurrent limits	3.0A
Low voltage detection	+10.0V

The output requirements for the +5V output appear in the following table.

Output requirements +5V (Sheet 1 of 2)

Characteristic	Value
Voltage	+4.9V to +5.1V
Maximum ripple and spikes peak to peak	100mV
Maximum current	8.5A
Overvoltage shutdown	+7.1V

NT2X09BA (continued)

Output requirements +5V (Sheet 2 of 2)

Characteristic	Value
Overcurrent limits	10.0A
Low voltage detection	+4.0V

The output requirements for the -15V output appear in the following table.

Output requirements -15V

Characteristic	Value
Voltage	+14.5V to -15.5V
Maximum ripple and spikes peak to peak	250mV
Maximum current	1.5A
Overvoltage shutdown	-16.5V
Overcurrent limits	2.0 A
Low voltage detection	-12.0V

The output requirements for the -5V output appear in the following table.

Output requirements -5V

Characteristic	Value
Voltage	-4.80V to -5.20V
Maximum ripple and spikes peak to peak	100mV
Maximum current	0.15A
Overvoltage shutdown	-5.60V
Overcurrent limits	0.25A
Low voltage detection	-4.00V

Dimensions

The NT2X09BA has the following dimensions;

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 62 mm (2.45 in.)

Power requirements

The maximum input voltage step is ±5V. The power requirements for the NT2X09BA appear in the following table.

Power requirements

Heading	Heading
-42V minimum	0.5A
-56V maximum	5.0A

The maximum heat dissipation is 70W.

NT2X09KA

Product description

The NT2X09KA multiple output power converter card provides five regulated common-ground dc power supplies for use in DMS-100 equipment. This card is the -60V version of the NT2X09AA.

Location

The card plugs into a standard DMS-100 equipment shelf.

Functional description

The NT2X09KA receives a nominal -60V input. The NT2X09KA converts the input to regulated +5V, +12V, -5V, -15V and +24V outputs. The card monitors the outputs and shuts down the converter if the outputs exceed a specified threshold.

Functional blocks

The NT2X09KA contains the following functional blocks:

- two power switches
- two power transformers
- two control circuits
- oscillator
- two rectifier and filter circuits
- +12V regulator
- -5V regulator
- overvoltage protection and low voltage monitor

Power switches

The control circuits control the power switches for this function. The power switches receive the -60V input from the office battery. The power circuits divide the input into a square waveform. The power switches apply this waveform across the primary windings of the power transformer. The control circuits vary the duty cycle of this square-wave voltage.

Power transformers

The power transformers step down the voltages that the power switches apply across the primary windings. The power transformers step down the voltages to produce the required voltages across the secondary windings.

Control circuits

The control circuits rotate the duty cycle of the power switches to achieve voltage regulation for specified groups of switch, transformer and control. Power switches can achieve voltage regulation for the +5V output for one combination. Power switches can achieve voltage regulation for the -15V output for the other combination. To achieve this regulation, the control circuits sense the correct output voltage. The control circuits compare the output voltage to a reference voltage. The control circuits adjust the duty cycle of the switch, if necessary.

A voltage that represents the output current in each switch provides the current limit function for that switch. This function allows the control circuits to shut down the power switches.

Oscillator

If an external clock signal is not present, the oscillator runs at 30 kHz. Normally, an external clock signal of 32 kHz is applied to the power converter. The oscillator is locked to this frequency which minimizes system interference from noise that the power switches generate.

Rectifier and filter circuits

The secondary output windings of one of the power transformers produce the outputs. The outputs are rectified and filtered to eliminate noise and ripple. The outputs are rectified and filtered to produce the required dc output. The +5V, -15V and +24V outputs do not require additional regulation. A fuse on the faceplate of the provides overload protection for the +24V output.

+12V regulator

The output of the +12V rectifier and filter is post-regulated to produce the required tolerance on the +12V output. This +12V regulator also provides current limits of this output.

-5V regulator

A part of the -15V output is post-regulated to produce the required tolerance on the -5V output . The -5V regulator provides current limits of this output.

Overvoltage protection and low voltage monitor

When voltages exceed a set level, the overvoltage protection circuit detects an overvoltage condition on the +12V, +5V, -15V and -5V outputs. The control circuits receive a signal to shut down the power converter. The overvoltage protection circuit does not monitor the +24V output for overvoltage.

When the frame supervisory panel (FSP) receives a signal, the FSP disables input power to the converter. This action keeps the converter in the shut down

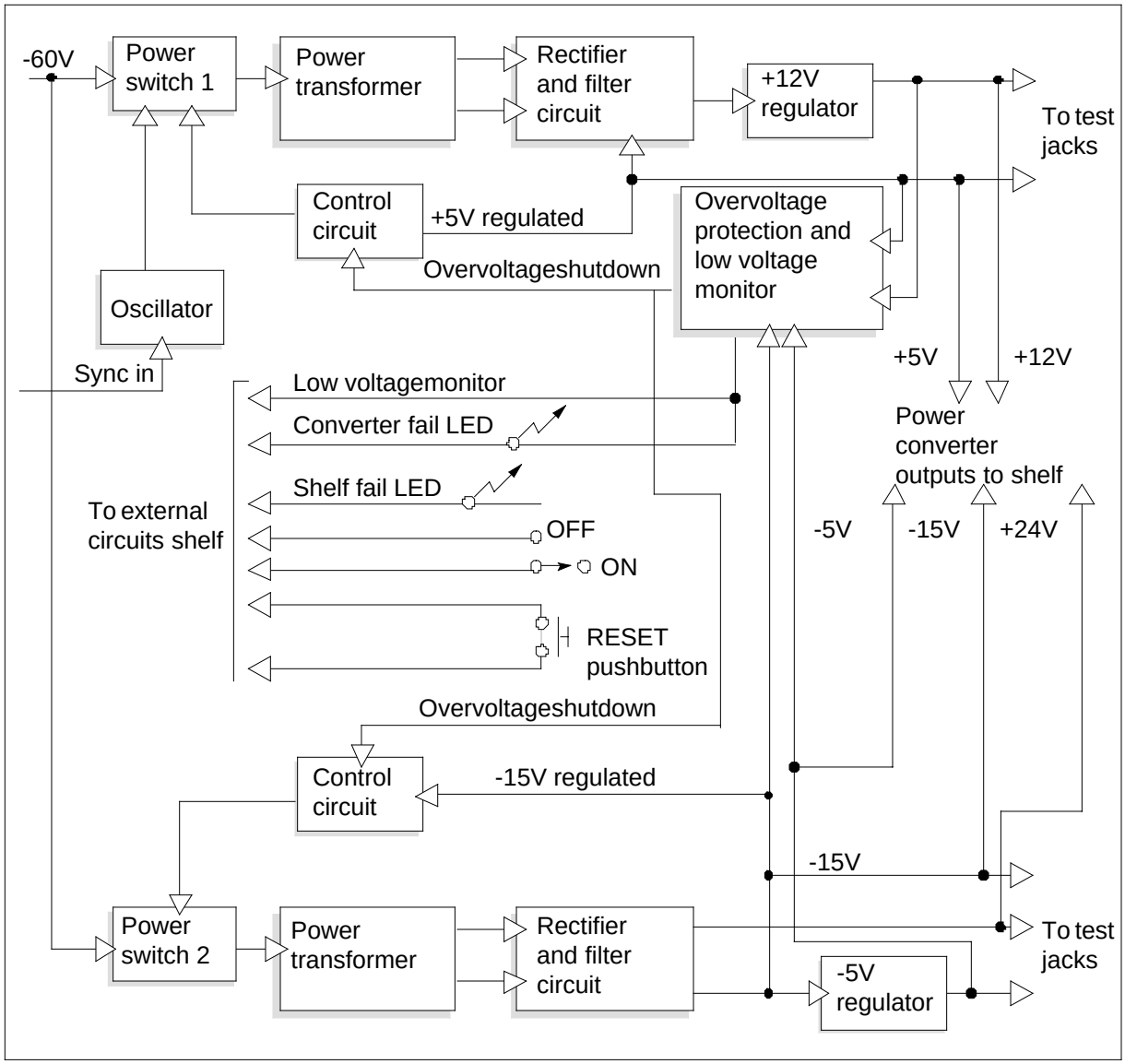
NT2X09KA (continued)

mode. Press the RESET button on the faceplate to return input power to the converter.

The low-voltage monitor circuit detects low voltage conditions on any output. The monitor circuit causes a light-emitting diode (LED) on the converter faceplate to light.

The relationship between the functional blocks appears in the following figure.

NT2X09KA functional blocks



Technical data

The converter has a 60- to 70-percent load range. The output requirements for the +24V output appear in the following table.

Output requirements + 24V

Characteristic	Value
Voltage	+22.5V to +28.0V
Maximum current	1.2 A
Current limits	2.0A
Low voltage detection	+18.0V

The output requirements for the +12 V output appear in the following table.

Output requirements + 12 V

Characteristic	Value
Voltage	+11.7V to +12.3V
Maximum ripple and spikes peak to peak	250mV
Maximum current	2 A
Overvoltage shutdown	+13.2V
Overcurrent limits	3.0A
Low voltage detection	+10.0V

The output requirements for the +5V output appear in the following table.

Output requirements + 5V (Sheet 1 of 2)

Characteristic	Value
Voltage	+4.9V to +5.1V
Maximum ripple and spikes peak to peak	10 mV
Maximum current	8.5A
Overvoltage shutdown	+7.1V

NT2X09KA (continued)

Output requirements + 5V (Sheet 2 of 2)

Characteristic	Value
Overcurrent limits	10.0A
Low voltage detection	+4.0 V

The output requirements for the -15V output appear in the following table.

Output requirements - 15V

Characteristic	Value
Voltage	+14.5V to -15.5V
Maximum ripple and spikes peak to peak	250mV
Maximum current	1.5A
Overvoltage shutdown	-16.7V
Overcurrent limits	2 A
Low voltage detection	-12.0V

The output specifications for the -5V output appear in the following table.

Output specifications -5V

Characteristic	Value
Voltage	-4.80V to-5.20V
Maximum ripple and spikes peak to peak	10mV
Maximum current	0.15A
Overvoltage shutdown	-5.60V
Overcurrent limits	0.25A
Low voltage detection	-4V

Dimensions

The NT2X09KA has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 280 mm (11.0 in.)
- width: 62 mm (2.45 in.)

Power requirements

The maximum input voltage step is ±5V. The power requirements for the NT2X09KA appear in the following table.

Power requirements

Voltage	Current
-52 V minimum	0.5 A
-72 V maximum	5 A

The maximum heat dissipation is 70W.

NT2X10

Product description

The function of the line test unit (LTU) analog card is to perform tests and measurements. These tests and measurements are for subscriber loops or line circuit cards. This card occupies one slot in a maintenance trunk module (MTM) or a remote service module (RSM). This card functions with the LTU digital card. The two cards form the LTU, a part of the line maintenance facility for DMS-100 and DMS-100/200.

The LTU analog card contains circuits that measure alternating current (ac) and direct current (dc) voltages. The card circuits connect resistances and impedance networks to the test leads. The card performs tests to calculate resistance, capacitance, and frequency. The card contains reference voltages and precision resistance for calibration purposes. The card has circuits that perform conversions to allow communication with the LTU digital format.

Location

An odd-numbered slot next to the LTU digital card must contain an LTU analog card. The slot number the LTU analog card occupies must be lower than the slot number that the LTU digital card occupies.

Functional description

The LTU analog card uses the NT2X41 metallic test access (MTA) card to interface with LTU digital cards and with the line circuit. A dedicated microprocessor on the LTU digital cards controls the analog card. The peripheral processor in the MTM does not control the analog card.

All functions of the LTU analog card interface in analog form with the line circuit. The test leads connect to the line circuit. You can refer to this card as an analog card, but the card is not completely analog. Communication with the LTU digital card is in digital form.

This section describes the NT2X10 in relation to the following terms:

- relays
- select section
- calibration
- voltage regulator
- ac and dc voltage
- integrator section
- zero crossing detector
- loop detector

- address decoder
- latches
- buffers
- analog/digital (A/D) convertor

Relays

The relay switching section contains relay drivers that control relays. The relay drivers connects the test leads to the desired section in this card. The latch section controls the relay drivers.

Select section

The select section contains analog solid state switches that the latch section controls. These switches reconfigure a test circuit or direct the output of the desired test circuit. For the switches to reconfigure a test circuit means the selection of dc voltage range. The direction of the output of the desired test circuit is to the A/D converter section.

Calibration

The calibration section provides a reference 10 V dc and a reference 10 V (p to p) ac. This section also provides precision resistances of 271 kohms and 24.9 kohms.

The reference voltages and precision resistances are available to the test circuits for calibration through the relay switching section.

Voltage regulator

The voltage regulator section produces +15V from the +24V available at the input of this card. Several sections of this card require the +15V.

dc voltage

The function of the dc voltage section is to measure dc voltage. The dc voltage measured is on the tip (T) test input lead or ring (R) test input lead, in relation to ground. This circuit provides a high input impedence of approximately 10 Mohms and filter networks to reject ac and noise voltages. Two dc voltage ranges are available when you change the gain of this circuit. The two ranges are under the control of the select section.

ac voltage

The ac voltage section measures the ac voltage on the test leads. A filter network samples, rectifies, and smooths the ac voltage. This action causes dc voltage. The proportion of the dc voltage is based on the root mean square (rms) value of the sampled ac voltages.

NT2X10 (continued)

Integrator

The integrator section measures resistance and capacitance. Two time constants are made available through changes in the amount of capacitance used in this circuit. The two constants are under the control of the select section.

Zero crossing detector

The zero crossing detector measures the voltage frequency (ringing) on the test leads. The positive part of a voltage waveform produces a logic 0 and the negative 1. The logic levels pass to the LTU digital card where the number of 0 to 1 changes are counted. The changes represent zero crossings for the analog waveform. The changes are counted over a timed interval to determine frequency.

Loop detector

The loop detector section detects an off-hook condition in equipment connected to the test leads. Equipment with ground start circuitry or loop seizure circuitry can detect the off-hook condition. The current in the R test lead monitored and, when a greater than a specified value, indicates an off-hook condition.

Address decoder

The address decoder section receives data from the LTU digital card in digital form. The address decoder activates the desired latch or buffer, or the address decoder section triggers the A/D converter. The address decoder triggers the A/D converter to start a conversion cycle.

Latches

The latch section receives data from the LTU digital card in digital form, and activates the desired control lead or leads. The control leads operate relays through relay drivers or switches used to configure the circuitry for a test or measurement.

Buffers

The buffer section is a temporary storage area for data from the A/D converter on this card. The data remains in the buffer until the microprocessor on the LTU digital card accepts the data.

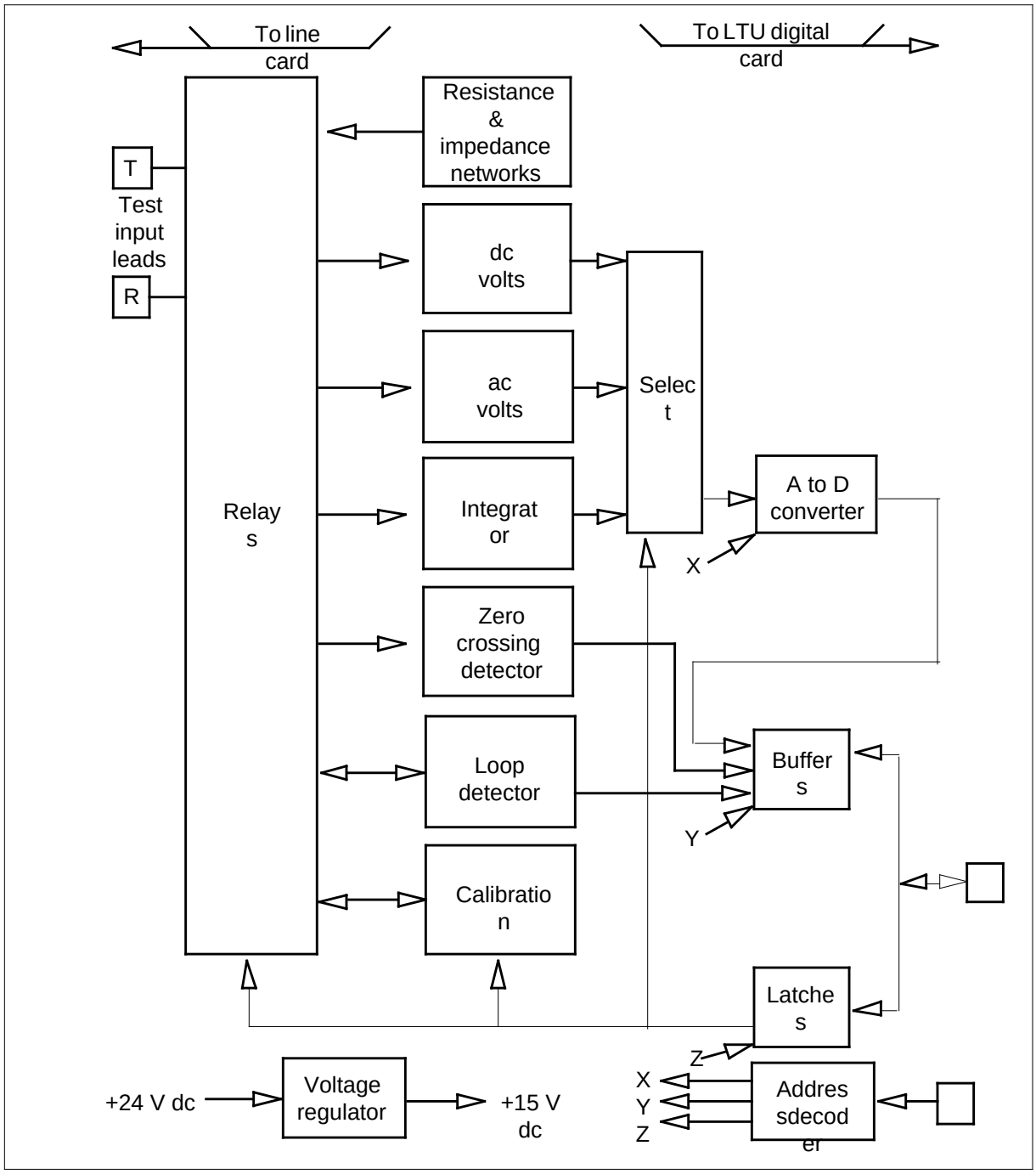
A/D Convertor

The A/D convertor section changes analog information, that is test results from a voltage measurement, into digital information (12-bit parallel data). The digital information can transmit to transmission to the LTU digital card.

Functional blocks

The following figure describes the relationship between the functional blocks.

NT2X10 functional blocks



NT2X10 (continued)

Technical data

This section describes:

- power requirements
- equipment dimensions
- LTU specifications
- environmental conditions.

Power requirements

The NT2X10 input voltages are +24V, +12V, +15V, -15V, and -48V. The power requirements appear in the following table.

Power requirements

Delivery	Maximum	Typical	Idle
+24V Current: +24 Power:	0.250 A 6.0 W	0.150 A 3.6 W	0.040 A 1.0 W
+12V Current: +12 Power:	0.050 A 0.6 W	0.025 A 0.3 A	0.000 A 0.0 W
+ 5V Current: + 5 Power:	0.370 A 1.8W	0.240 A 1.2 W	0.240 A 1.2 W
-15V Current: -15 Power:	0.040 A 0.6 W	0.040 A 0.6 W	0.40 A 0.6 W
-48V Current: -48 Power:	0.050 A 2.4 W	0.020 A 1.0 W	0.000 A 0.0 W

Equipment dimensions

The NT2X10 dimensions are 317.5 mm (12.5 in.) in height, 254 mm (10 in.) in depth, and 29 mm (1.125 in.) in width. The approximate weight is 0.68 kg (1.50 lb).

LTU measurement times

The following table lists the LTU measurement times for the NT2X10.

LTU measurement time

Measurement	Initial test	Continuous test cycle time
dc voltage	1 s	2 s
ac voltage	1 s	2 s
Resistance	5 s	3 s
Capacitance	8 s	4 s
LIT	2.5 s	does not apply

LTU measurement specifications

The following table lists the LTU measurement specifications for the NT2X10. The referenced notes are on the next page.

LTU measurement specifications (Sheet 1 of 3)

Measurement	Range	Steps	Accuracy	Repeatability
dc voltage T/G, R/G (*Refer to* Note 1)	-150 to +150 V	1 V	± 1V or 5%	±1V

Note 1: The measurement error cannot exceed the greater of the two accuracy values given.

Note 2: Measurement of longitudinal current is that that flows from a lead, through a 200ohm resistor, to ground.

Note 3: The accuracies are for the worst case of 50V (ac) or 5 uF, or both present on a lead or leads. Normally, with less than 20V (ac) and less than 2 uF, an accuracy of ±2% is achieved.

Note 4: This measurement occurs when the system requests resistance and voltage on a lead or leads exceeds -9V (dc).

Note 5: This measurement cannot occur if leakage resistance is less than 10kohms. This measurement cannot occur if foreign electromotive force (FEMF) on lead is greater than 75V (rms).

Note 6: Repeatability error increases as FEMF ac voltage increases as expressed in the table below.

Note 7: Signals greater than 50V peak-to-peak are measured.

Note 8: Line insulation testing (LIT) occurs under automatic line testing (ALT) which is designed to test many lines in a short period of time. An LIT performs shorter tests than the LTU can perform and the accuracies of this table are not achieved for LIT.

NT2X10 (continued)

LTU measurement specifications (Sheet 2 of 3)

Measurement	Range	Steps	Accuracy	Repeatability
ac voltage T/G, R/G (*Refer to* Note 1)	0 to +150V (rms)	1 V	±1V or 5%	±1 V
ac current T/G, R/G (*Refer to* Notes 1 and 2)	0 to 150mA (rms)	1 mA	±1mA or 5%	±1 mA
Resistance T/G, R/G, T/R (*Refer to* Note 3)	10 to 99 ohms	1 ohm	±8%	±2 ohms ±1%
	100 to 999 ohms	1 ohm	±4%	±5 ohms ±1%
	1k to 9.99k ohms	10 ohms	±4%	±5 ohms ±1%
	10k to 19.9k ohms	100 ohms	±4%	±5 ohms ±1%
	20k to 99.9k ohms	100 ohms	±4%	±5 ohms ±1%
	100k to 999k ohms	1k ohms	±10%	±5 ohms ±2%

Note 1: The measurement error cannot exceed the greater of the two accuracy values given.

Note 2: Measurement of longitudinal current is that that flows from a lead, through a 200ohm resistor, to ground.

Note 3: The accuracies are for the worst case of 50V (ac) or 5 uF, or both present on a lead or leads. Normally, with less than 20V (ac) and less than 2 uF, an accuracy of ±2% is achieved.

Note 4: This measurement occurs when the system requests resistance and voltage on a lead or leads exceeds -9V (dc).

Note 5: This measurement cannot occur if leakage resistance is less than 10kohms. This measurement cannot occur if foreign electromotive force (FEMF) on lead is greater than 75V (rms).

Note 6: Repeatability error increases as FEMF ac voltage increases as expressed in the table below.

Note 7: Signals greater than 50V peak-to-peak are measured.

Note 8: Line insulation testing (LIT) occurs under automatic line testing (ALT) which is designed to test many lines in a short period of time. An LIT performs shorter tests than the LTU can perform and the accuracies of this table are not achieved for LIT.

LTU measurement specifications (Sheet 3 of 3)

Measurement	Range	Steps	Accuracy	Repeatability
Resistance to Battery T/B, R/B, (*Refer to* Note 4)	10 to 999 ohms	1 ohm	±5%	±5 ohms ±2%
	1k to 9.99k ohms	10 ohms	±5%	±5 ohms ±2%
	10k to 19.9k ohms	100 ohms	±5%	±5 ohms ±2%
	20k to 99.9k ohms	100 ohms	±10%	±5 ohms ±10%
	100k to 999k ohms	1k ohms	±10%	±5 ohms ±10%
Capacitance T/G, R/G, T/R (*Refer to* Notes 5 and 6)	0.01 to 0.99 uF	0.01 uF	±10%	±0.02 uF ±2%
	1.00 to 5.00 uF	0.01 uF	±10%	±0.02 uF ±2%
Frequency T/R (*Refer to* Note 7)	0 to 255Hz	±1Hz	±1Hz	±1 Hz
Capacitance T/G, R/G, T/R (*Refer to* Notes 5 and 6)	0.01 to 0.99 uF	0.01 uF	±10%	±0.02 uF ±2%
	1.00 to 5.00 uF	0.01 uF	±10%	±0.02 uF ±2%
Frequency T/R (*Refer to*Note 7)	0 to 255 Hz	±1 Hz	±1 Hz	±1 Hz

Note 1: The measurement error cannot exceed the greater of the two accuracy values given.

Note 2: Measurement of longitudinal current is that that flows from a lead, through a 200ohm resistor, to ground.

Note 3: The accuracies are for the worst case of 50V (ac) or 5 uF, or both present on a lead or leads. Normally, with less than 20V (ac) and less than 2 uF, an accuracy of ±2% is achieved.

Note 4: This measurement occurs when the system requests resistance and voltage on a lead or leads exceeds -9V (dc).

Note 5: This measurement cannot occur if leakage resistance is less than 10kohms. This measurement cannot occur if foreign electromotive force (FEMF) on lead is greater than 75V (rms).

Note 6: Repeatability error increases as FEMF ac voltage increases as expressed in the table below.

Note 7: Signals greater than 50V peak-to-peak are measured.

Note 8: Line insulation testing (LIT) occurs under automatic line testing (ALT) which is designed to test many lines in a short period of time. An LIT performs shorter tests than the LTU can perform and the accuracies of this table are not achieved for LIT.

NT2X10 (end)

The following table lists the repeatability error margins.

Repeatability error margin

Voltage	Repeatability
10V (rms)	±0.1 u F
20V (rms)	±0.2 u F
30V (rms)	±0.3 u F
40V (rms)	±0.4 u F
50V (rms)	±0.5 u F
60V (rms)	±0.6 u F

Environmental conditions

The NT2X10 performs under limited environmental controls. These controls appear in the following table.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 °C to 30 °C (50 °F to 86 °F)	5 °C to 49 °C (41 °F to 120.2 °F)
Relative humidity	20% to 55%	20% to 80%

Note: A relative humidity of 80% is expected at an ambient temperature of 21° C (69.8°F) maximum. At an ambient temperature of 49°C (120.2°F), the relative humidity must be a maximum of 30%.

NT2X11AA

Product description

The NT2X11AA line test unit (LTU) digital card operates with the LTU analog card. The analog card tests and measures a subscriber loop or a line circuit card. The two cards are a part of the lines maintenance facility for the DMS-100 and DMS-100/200.

The LTU digital card has the following functions:

- performs timing functions
- stores the instructions for the tests that the LTU analog card performs
- interprets the test results

Location

The card occupies one card position in a maintenance trunk module (MTM) or a remote service module (RSM). The card must be in an even-numbered slot next to the LTU analog card. The slot number of the LTU digital card must be higher than the slot of the LTU analog card.

Functional description

The LTU digital card receives requests from the MTM central control (CC). The card sends instructions to the LTU analog card to perform specified tests. The LTU analog card sends back results from the tests. The LTU digital card reads the results and sends the information back to the CC.

Functional blocks

The NT2X11AA consists of the following functional blocks that follow:

- CPU
- programmable interval timer (PIT)
- ROM
- RAM
- buffers

CPU

The central processing unit (CPU) controls the functions of the LTU analog card. The CPU reads the test instructions. The CPU sends signals to the LTU analog card to perform the selected tests. The CPU sends signals to and receives signals from the PIT to measure desired time intervals.

NT2X11AA (continued)

Programmable interval timer

The programmable interval timer (PIT) provides measured time intervals under the direction of the CPU. When the CPU instructs to start a specified time interval, the PIT activates the PIT clock to count down the interval. The PIT clock and the DMS clock operate in sync. When the time interval expires, the PIT sends the CPU a signal over the CPU interrupt lead.

ROM

The read only memory (ROM) stores the program code that performs and reads the LTU tests. The test instructions are sent to the CPU. The CPU performs the instructions to control the LTU analog card when the card performs a test. When tests results return, the CPU uses analysis codes from the ROM to read the results.

RAM

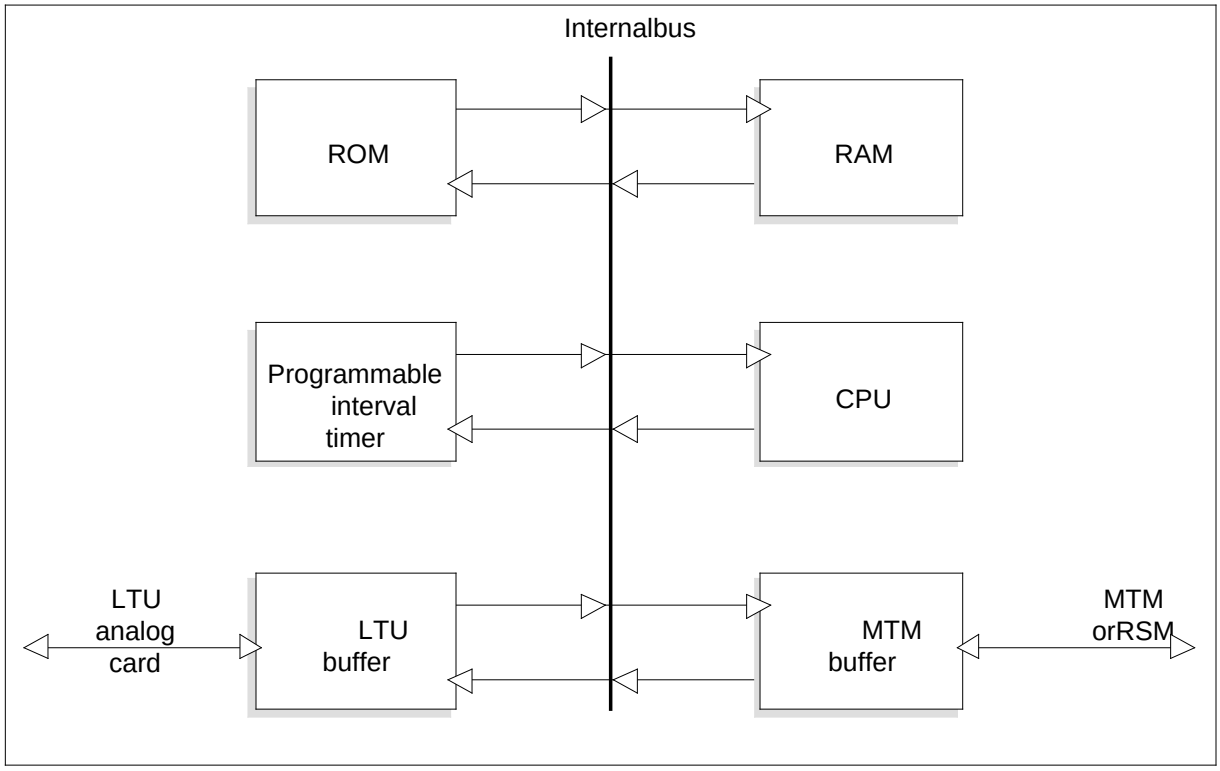
The random access memory (RAM) serves as a temporary storage area to hold data during a test. The RAM capacity is 1 Kbyte.

Buffers

Two buffers are available. One buffer handles communications with the LTU analog card. The second buffer handles communications with the MTM or RSM. The LTU buffer stores data and addresses sent to or received from the LTU parallel bus. The MTM buffer stores data, timing pulses, and card enable signals sent to or received from the CC.

The relationship between the functional blocks appears in the following figure.

NT2X11AA functional blocks



Technical data

Dimensions

The NT2X11AA circuit card has the following dimensions:

- height: 317.5 mm (12.5 in.)
- depth: 254 mm (10.0 in.)

Power requirements

The following table shows the power requirements for the NT2X11AA.

Power requirements

Voltage	Maximum current	Standard current	Idle current
+ 12V	0.05 A	0.03 A	0.03 A
+ 5V	2.10 A	1.50 A	1.20 A
- 15V	0.05 A	0.03 A	0.03 A

NT2X14

Product description

The line module controller (LMC) and remote line controller (RLC) are similar shelves in structure. The LMC is part of the double-bay line module equipment (LME) and the RLC is part of the remote line module (RLM) frames.

LMC

The LMC controls the flow of pulse code modulation (PCM) voice and signaling data between a maximum of four, 4-wire, 32-channel, duplicated digital speech links to the network (NET) or DMS-100 Family of digital switching systems and 20 sets of digital terminal groups to the line drawers (LD).

The LMC contains a master processor (MP) that controls three auxiliary processors that handle control messages and signaling. The MP also controls PCM connections to the line circuits (LC).

The LMC provides a concentration of 640 analog subscriber lines. The analog subscriber lines consist of 20 terminal groups of 32 lines each. The LMC also provides a maximum of 120 PCM digital speech link channels. The PCM digital speech link channels consist of a maximum of 4 links at 30 PCM channels each. The LCM provides a concentration of the analog subscriber lines and PCM digital speech link channels to the office switching NET.

RLC

The RLC controls the flow of PCM voice and signaling data between a maximum of four, 2-way, 24-channel DS-1 carrier links to the remote digital carrier links, to the remote (host) Digital Multiplex System (DMS) family office and 20 sets of digital terminal groups, to the LD or up to 19 LDs, and to a remote service module (RSM).

To reference additional information about the previous components, refer to hardware description NT0X45 for the LME and RLM frames. Refer to NT2X31 for the Digital Carrier Module-Remote (DCM-R). Refer to NT2X19 for the Ld, and NT2X58 for the RSM.

The RLC contains an MP that controls two auxiliary processors. One processor handles high-level data link control (HDLC) messages between the RLC MP and the host office central control (CC). The other processor handles signaling. The MP also controls PCM connections to the LC.

The 640-line configuration of the RLC provides a concentration of 640 analog subscriber lines to a maximum of 4 DS-1 carrier links. The DS-1 carrier link

consists of 24 PCM channels for each link. The 640-line configuration of the RLC provides these analog subscriber lines to the host office.

The 608-line configuration of the RLC provides a concentration of 608 analog subscriber lines. The analog subscriber lines consist of 19 terminal groups of 32 lines for each group. The RLC provides this concentration to a maximum of 4 DS-1 carrier links to the host office. The twentieth group controls the NT2X58 RSM.

The RLC intra-calling (IAC) option enables calls to be completed locally through the RLC when the calls are between subscribers. Subscribers must connect to the same double-bay, RLM frame. When the appropriate software is present, IAC activates.

The RLC emergency stand-alone (ESA) option allows plain ordinary telephone service (POTS) between subscribers connected to the same RLM frame. The RLM frame must be 608-line RLC. The ESA requires an extension memory card and a dedicated RSM. When the appropriate hardware and software is present, ESA activates.

The primary features common to the LMC and the RLC follow:

- provides automatic load-sharing with the mating controller when a controller in the double-bay area fails
- contains two ringing generators (RG) and power converter cards that share the load of the bay
- provides programmable RG functions to produce harmonic, decimonic, or synchronomic types of frequency ringing. Provided automatic number identification (ANI) and coin control voltages
- contains a digital tone generator that conforms to the North American precise audible tone plan
- provides interchangeable LC cards of types that can be selected that provide two combinations of LC functions. The two combinations are Type A LC NT2X17 and Type B LC NT2X18

Location

Each LME or RLM bay contains one LMC or RLC shelf.

Functional description

A functional description of the LMC and the RLM appears in this section.

NT2X14 (continued)

LMC

The PCM data can enter the LMC at any of the four NET ports (0-3). Data that passes from the NET to an LD and LC is on the receive path. Data that originates in an LC and passes to the NET is on the transmit path.

The LMC is described in terms of the receive path, transmit path, control, shelf and cards.

Receive path

The receive path of a 32-channel PCM data stream can enter on both planes of NET port-0. This event appears in the figure on page 4. The data routes through the NET interface (NI) and NET receive bus-0 to the receive multiplexer (MUX). In this event, the system selects one of 20 (0-19) terminal receive busses, like bus-0. The data routes to the primary bus interface-0 in the NT2X19 LD-0. Terminal control bus-0 controls bus interface-0. This event occurs so that the set of 32-channel data distributes to the 32 LC (0-13) with appropriate timing. Each piece of channel data associates with an analog subscriber line. The LC converts the PCM data to analog signals. Each NET port associates with one of the four NET receive busses (such as port-0 to bus-0). Similar action occurs at the same time on the other three NET receive busses 1-3.

Transmit path

On the transmit path, each of the 32 LCs converts the associated subscriber analog signals to PCM data. The system routes the set of 32-channel PCM data through primary bus interface-0 to terminal transmit bus-0. The set of 32-channel PCM data represents the analog inputs from 32 subscriber line. Connection memory controls routing between LDs 0-19 and the 20 terminal transmit busses. Control occurs through 20 terminal control busses (0-19).

The 32-channel data on terminal transmit bus-0 enters the transmit MUX. When this event occurs, the system selects one of four (0-3) NET transmit busses. The NET transmit bus routes the data to planes -0 and -1 or NET port-0. Each NET transmit bus associates with one of the four NET ports bus-0 to port-0. Similar action occurs at the same time on the other three NET transmit busses 1-3.

Control

The connection memory and control circuits provide control over the NI, the receive and transmit MUXs and the bus interfaces. The MP controls connection memory and control circuits.

The terminal transmit, receive and control busses for LD-0 comprise terminal group-0. Similar terminal groups (1-19) provide transmit, receive and control

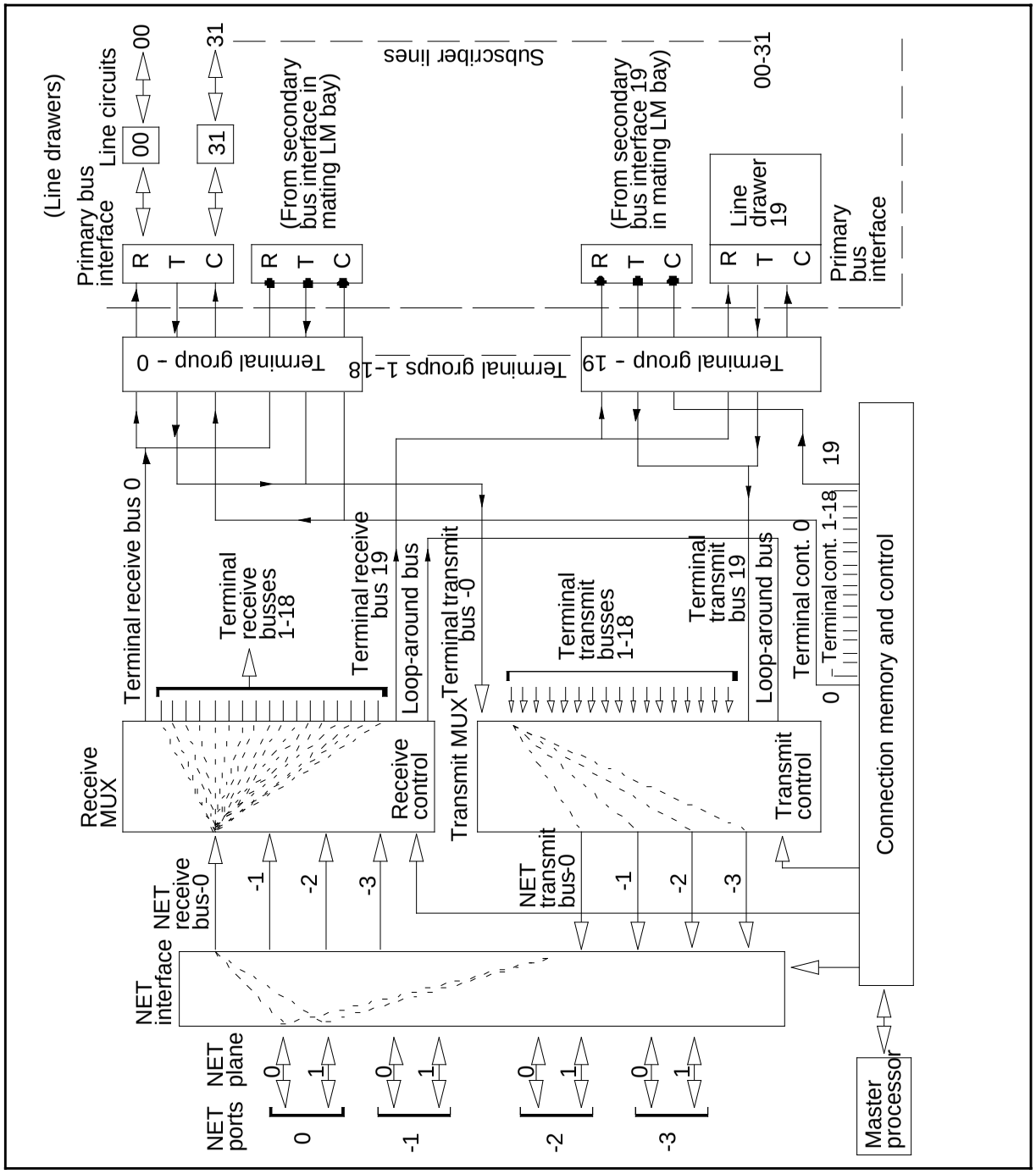
paths to all 20 LDs. The above terminal groups also provide transmit, receive to the 20 sets of subscriber lines (00-31), totalling 640 lines.

The terminal groups also accept the receive, transmit and control busses from the secondary bus interfaces in the LDs of the mating bay. In the event of a fault in the LMS of one bay, the activity monitor signals the condition to the office CC. If the fault is of enough severity, the CC activates the secondary bus interfaces in the LDs of the failed bay. The active controller assumes control of the terminal groups from the activate controllers mate in addition to the active controllers.

The following figure illustrates the LMC signal flow.

NT2X14 (continued)

NT2X14 LMC signal flow



Shelf and cards

The LMC consists of a metal shelf assembly with a printed-circuit backplane. The back plane contains internal common busses, intercard connections, and power feeds.

Receptacles for external cable connections are behind the backplane. Sockets to receive the connectors on the printed-circuit cards are on the front. The cards are plugged into slots in the shelf assembly. The function of each LMC card is in the following table.

LMC card description (Sheet 1 of 2)

Card	Description
Network interface	The network interface card contains eight diphase modulators and demodulators, assigned to four ports in each of two planes. A loop-around (LA) circuit for each channel loops the eight speech bits back toward the NET for maintenance purposes. The network interface also generates parity check bits for signals on the transmit path to the NET.
Receive MUX	The receive MUX card contains the receive MUX circuit which performs the connections between four NET receive busses. A separate bus provides an LA path to the transmit bus.
Connection memory and transmit MUX	This card contains the random access memory (RAM) for the connection memory and the transmit MUX circuit. The transmit MUX circuit forms the connections between 20 terminal transmit busses. A separate bus provides an LA path to the receive MUX.
PP message processor	The PP message processor card provides integrity-checking and channel supervision messages for each PCM channel connection to the LM. The PCM channel connects from the NET under the control of the MP.
CC message processor	The CC message processor card controls the handling and routing of CC (channel 00) messages to and from the CC. The CC is in the DMS-100 digital processor control. The CC message processor card also contains the LM clock pulse generator.
Master processor	The MP card contains a 12-K static RAM and 2-K erasable programmable read-only memory (EPROM). The MP card provides the main computing element in the LM and controls the CC and PP message processors. The MP card also controls signaling processor (SP) and connection memory.

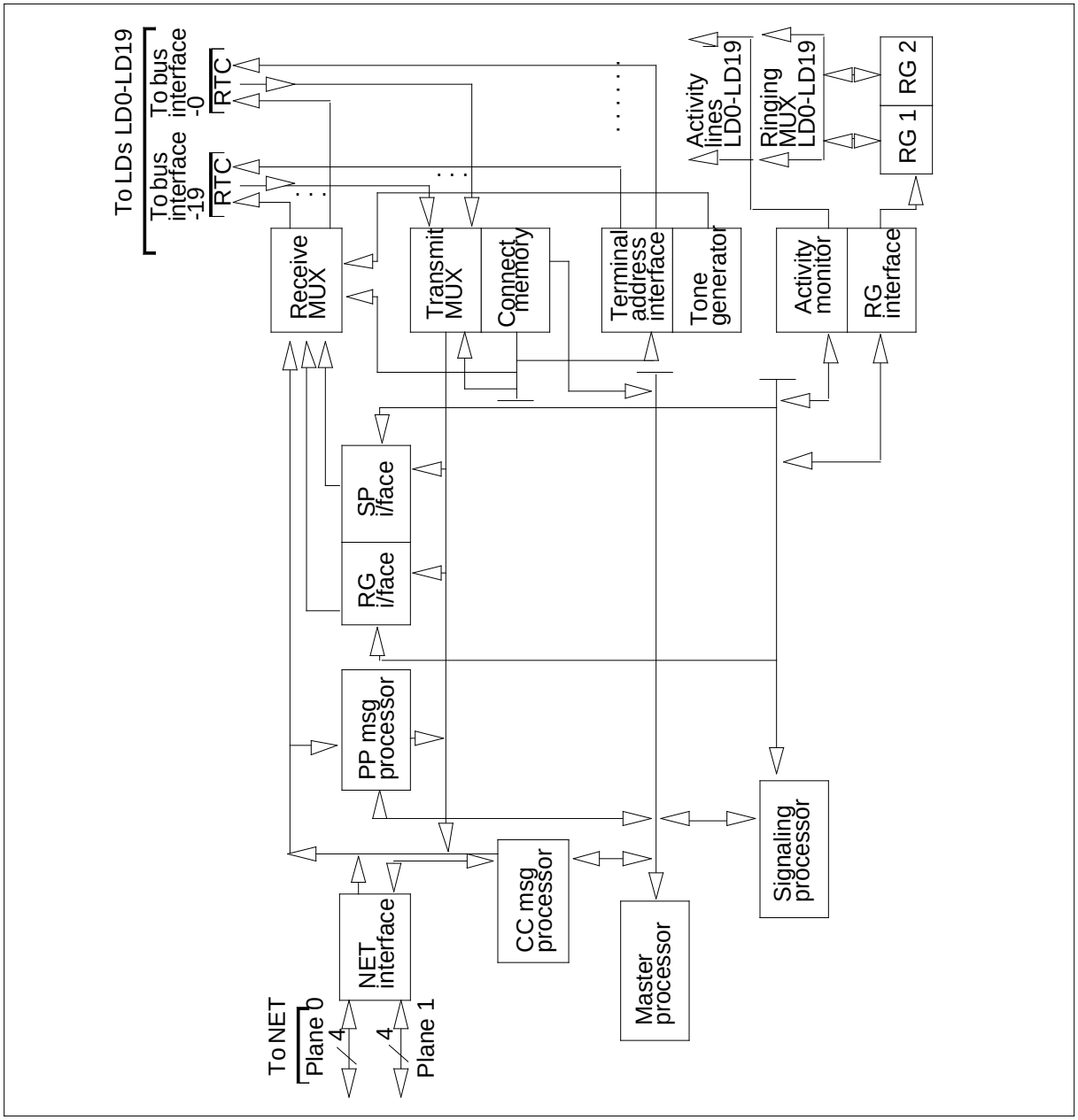
NT2X14 (continued)

LMC card description (Sheet 2 of 2)

Card	Description
Signaling processor interface	The SP interface card contains buffer memory and interface circuits. The memory and interface circuits are between the receive and transmit data streams and control messages for scanning, ringing, and LC control.
Ringing generator card	The RG card generates signals to control the application of the RGs to the ringing MUX in each LD. The application occurs under control of the SP. The RG card also contains the activity monitor which times-out if a controller loses sanity. A loss of sanity enables the mating LM controller to assume control through the secondary bus interfaces in the LD.
Terminal address interface and tone generator	The terminal address interface and tone generator card contains circuits that generate line addresses for line cards in the LDs. The terminal address interface and tone generator also houses a digital tone generator for standard signaling tones.
+24V converter and ringing generator	The RG is a programmable power converter which, in addition to normal ringing requirements, provides coin function and ANI voltages. Control of this card occurs through the SP and RG interface. This card also converts the -48V office battery to +24V feed the LC cards require.
±5V/12V converter	The ±5V/12V converter card converts the -48V office battery feed to lower-voltage, filtered feeds the controller cards require.

The following figure illustrates the relationship between the LMC cards.

NT2X14 LMC card functions



RLC

The signal flow of the RLC is similar to that of the LMC. The functional description with the following figure applies to the RLC, except as follows:

- For the RLC, the DS-1 interfaces replace the NI. The purpose of the DS-1 interface is to convert the 32-channel, 2.56 Mb/s format within the RLC to

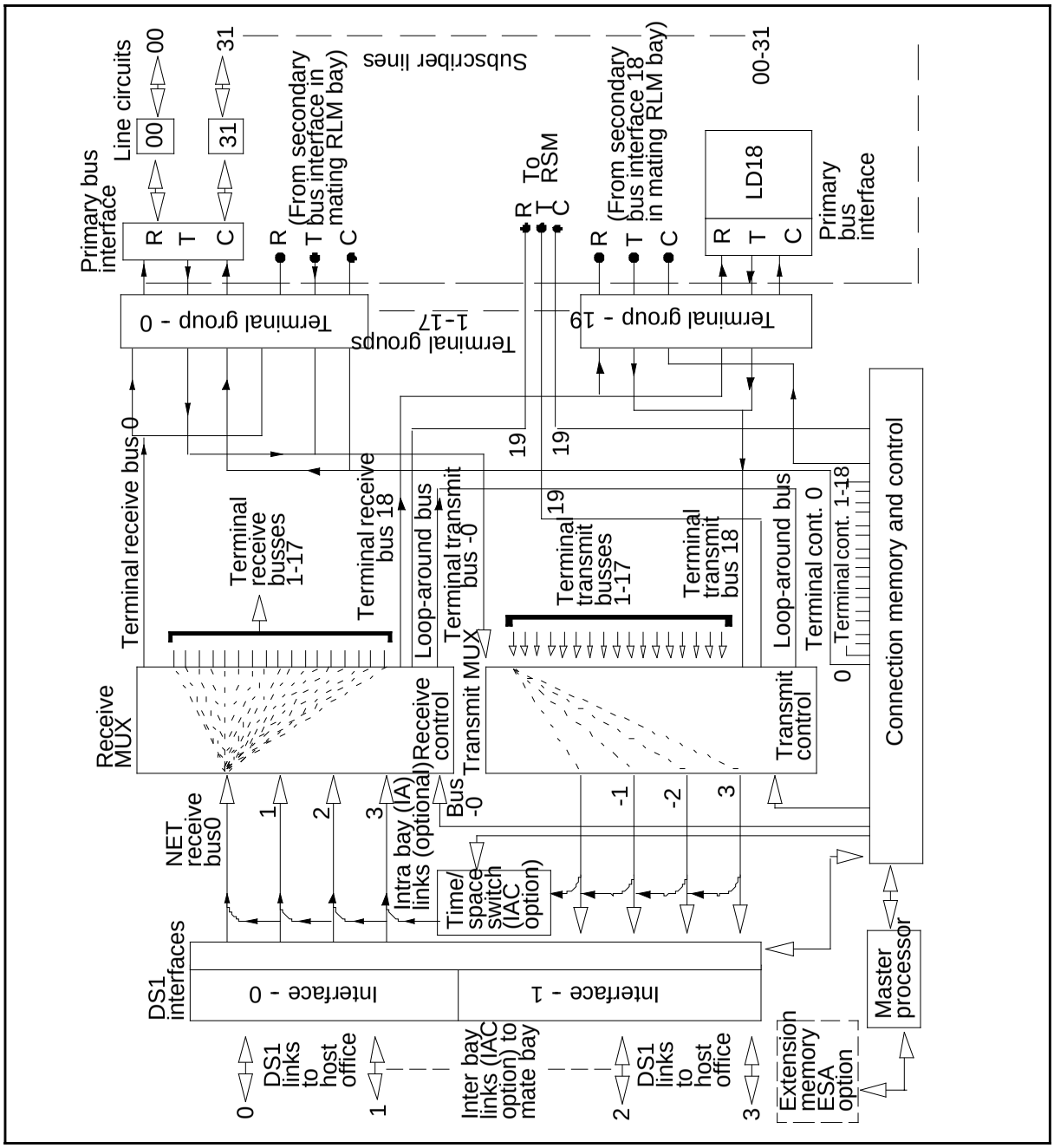
NT2X14 (continued)

the 24-channel. The DS-1 carrier equipment uses the 1.544 Mb/s format and the opposite.

- The RLC can have one or two DS-1 interface cards (2 links for each card). The number of links required by the host office determines the number of cards the RLC can have. Each card (0 or 1) has two ports for DS-1 connections.
- In the 640-line configuration, the assignment of the 20 terminal groups (0-19) is the same as in an LMC.
- In the 608-line configuration, terminal groups 0-18 interface with LD 0-18. Terminal group 19 is assigned to interface with the NT2X58 RSM.
- In the IAC option configuration, the time/space switch function activates to handle intra-bay connection between the four transmit and receive busses. The system provides a maximum of two inter-bay links to handle connections to the mate bay. The possible combinations of DS-1, IR, and IA calls are set up using call-processing facilities of the host office CC. The RLC in each RLM bay makes the connections between subscribers LCs. The RLC makes the connections instead of through the host office switching NET.
- In the ESA configuration, if the DS-1 links to the host office have failed, the RLC performs all the call processing and connections. For this option, the MP has an extension memory card. An exclusively assigned RSM serves the associated RLM bays. The RSM has Digitone receivers to replace those at the host office which are inaccessible when ESA is active.

The following figure illustrates the RLC signal flow.

NT2X14 RLC signal flow



NT2X14 (continued)

The configuration of the RLC shelf is similar to that of the LMC shelf. The following table describes the RLC cards.

RLC card descriptions (Sheet 1 of 2)

Card	Description
DS-1 interfaces	The DS-1 interface cards contain two bipolar converters for each card. The converters interface with the transmit and receive channels of the DS-1 bit streams. The bipolar DS-1 signals convert to transistor-to-transistor logic (TTL) data format and vice versa. Other circuits convert the DS-1 data at 1.5444 Mb/s to the RLC at a rate of 2.56 Mb/s and suppress the A and B bit DS-1 signaling. All signaling between the RLC and the host office is on a common channel, like channel 1 of DS-1 link 0. The DS-1 interface cards correspond to the NI card in the LMC.
Receive MUX	The receive MUX card contains the receive MUX circuit that performs the connections between four NET receive busses. A separate bus provides an LA path to the transmit bus.
Connection memory, transmit MUX, and Time/Space switch card	The connection memory, transmit MUX, and Time/Space switch card contains the RAM for the connection memory and the transmit MUX circuit. The transmit MUX circuit performs the connections between 20 terminal transmit busses. A separate bus provides an LA path to the receive MUX. When the IAC option is not activated, the Time/Space switch circuit does not operate. When the IAC option is required, the system loads the appropriate software package and the Time/Space switch is activated. The Time/Space switch function is capable of switching PCM data from any channel of any of the four transmit busses. The connection memory directs the Time/Space switch.
Extension memory card	The extension memory card contains the RAM circuits which are accessible to the MP card. The extension memory card also provides an additional 64-K memory capability for use by the MP when ESA is activated.
HDLC message processor	The HDLC message processor card contains a microprocessor and a controller section as well as timing and control circuits provide synchronization between the RLC circuits (2.56 MHz) and the clock signal extracted from the DS-1 links (1.544 MHz). The HDLC card controls the flow of messages between the RLC and the host office CC. (The card replaces the PP message processor and CC message processor cards used in the LCM.)

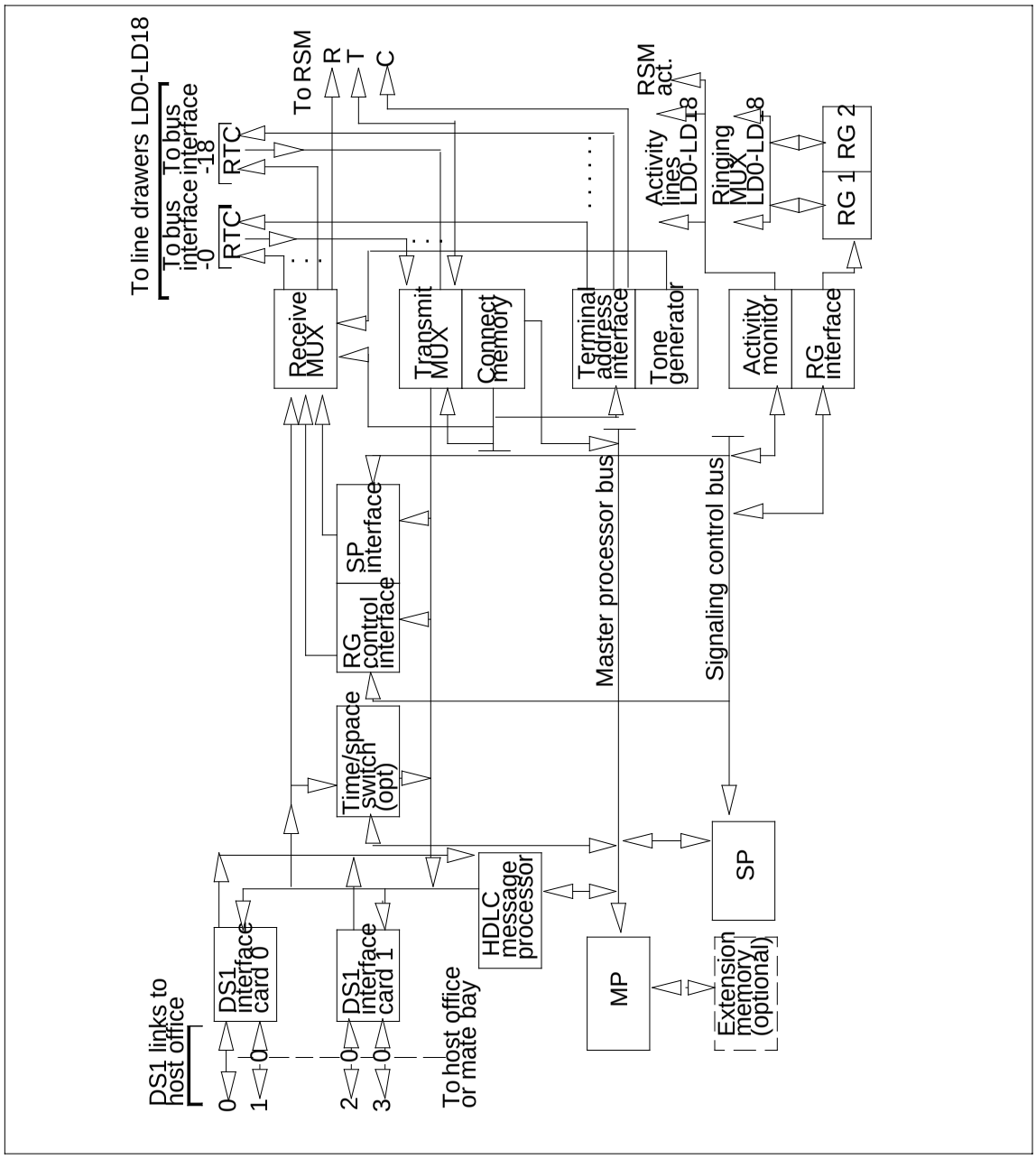
RLC card descriptions (Sheet 2 of 2)

Card	Description
Master processor	The MP provides the main computing element in the LM and contains a 12-K static RAM. The MP also contains an 80-K storage capability for dynamic RAM, and 2 k EPROM. In addition, the MP controls the HDLC message processor and the SP and connection memory.
Signaling processor interface	The SP interface card contains buffer memory and interface circuits between the receive and transmit data streams and control messages. Control messages concern scanning, ringing, and LC control.
Ringing generator card	The RG card generates signals to control application for the RGs to the ringing MUX in each LD. The application is under control of the SP. The RG card also contains the activity monitor which times-out if a controller loses sanity. A loss of sanity enables the mating LM controller to assume control through the secondary bus interfaces in the LD.
Terminal address interface and tone generator	The terminal address interface and tone generator card contains circuits that generate the line addresses for the LCs in the LDs. The terminal address interface and tone generator also houses a digital tone generator for standard signaling tones.
+24V convertor and ringing generator	The RG converter is a programmable power converter which, in addition to normal ringing requirements, provides coin functions and ANI voltages. Control of the card occurs through the SP and RG interface. The RG converter card also converts -48V office battery to +24V feed required by the LC cards.
±5V/12V convertor	The ±5V/12V converter card converts the -48V office battery feed to lower-voltage, filtered feeds required by the controller cards require.

The following figure illustrates the relationship between the RLC cards.

NT2X14 (continued)

NT2X14 RLC card functions



Technical data

The technical data section provides specifications for the following:

- NT power requirements
- equipment dimensions

- environmental conditions
- input/output characteristics
- connection memory
- overall delay
- ringing generators
- tone generator
- MP extension memory
- the signaling processor

Note: Data applies to the LMC and the RLC unless indicated.

Power requirements

The NT2X14 power requirements appear in the following table.

Power requirements

Battery voltage	-42.75V to -55.8V
Power consumption	Refer to the NT0X45 LME or RLM frame power consumption formula.

Equipment dimensions

The NT2X14 dimensions are 356 mm (14 inches) in height, 610 mm (24 inches) in width, and 305 mm (12 inches) in depth. The approximate weight of the NT2X14 is 29.5 kg (65 lb).

Environmental conditions

The NT2X14 performs under limited environmental constraints as illustrated in the following table.

Ambient conditions

Condition	Operating range	Short term range
Temperature	10 °C to 30 °C (50 °F to 86 °F)	5 °C to 49 °C (41 °F to 120.2 °F)
Relative humidity	20% to 55%	20% to 80%

Note: A relative humidity of 80% is expected at an ambient temperature of 21°C (69.8°F) maximum. At an ambient temperature of 49°C (120.2°F), the relative humidity is expected to be 30% maximum.

NT2X14 (continued)

Input/output characteristics

The input/output characteristics for the NT2X14 appear in the following table.

Input/output characteristics (Sheet 1 of 2)

LMC		**RLC**	
NET interface		DS-1 interface	
Rate	2.56 Mb/s	Rate	1.544 Mb/s
Channels per frame	32	Channels per frame	24
Bits per channel	10	Bits per channel	8
Channels numbered	0-31	Channels numbered	1-24
Bits numbered	0-9	Bits numbered	1-8
Channel sent first	0	Channel sent first	1
Bits sent first	9	Bits sent first	1
Frame bit	Ch-0, bit-0	Frame bit	193
Code		Code	
DCM diphase with frame pulse violation once for each frame		PCM bipolar, 192 speech bits followed by the193rd bit once for each frame	
Message channel	0	Primary message channel DS-1 port -0, channel-1	
NET port	0	Standby message channel DS-1 port-1, channel-1	

Input/output characteristics (Sheet 2 of 2)

LMC	RLC		
	DS-1 link combinations to DCM-R		
	DS-1	IA	IR
	4	1	0
	3	1	1
	2	2	1
	4	0	0
	2	1	2
	3	0	0
	2	0	0

Connection memory

The specifications for the connection memory appear in the following table.

Connection memory

Total capacity	512 bytes (8-bit bytes) (32 groups of 16 bytes)
Response time	390ns (minimum) 1.95us (maximum)

Overall delay

The overall delay specification from the receive bus to the transmit bus is 40 bits.

Ringing generators

The specifications for RGs (2 RGs for each shelf) coin control is ±130 V (dc). The ANI specification is ±48V (dc) common tip/ring (T/R) output with current sensing. Ringing power conforms with REA specification PE-40 with a ringing power of 15 V using North American ringing schemes.

Tone generator

The specification for the tone generator is 2-K read-only memory (ROM) which stores ringback, busy, and dial tones. Tones conform with the North American Precise Audible Tone Plan.

NT2X14 (end)

Master processor

The specification for the RLC MP is 80-K RAM. The specification for the LMC MP and for both controllers is 48-K RAM. The EPROM specification is 2 K.

Extension memory

The specifications for the extension memory are 64-K RAM for the RLM with the ESA option only.

Signaling processor

The specifications for the SP are 12-K ROM and 2-K EPROM.

Product description

The line circuit card type A provides a single-party, two-party, or four-party voice and signaling interface. The interface is between a two-wire, analog subscriber line and one channel. This channel is of the four-wire, 32-channel, 2.56 Mb/s bit stream of the DMS-100 Family of switching systems.

The NT2X17 provides subscriber line interface features, card features, and test features.

The primary subscriber line interface usability features of the NT2X17 are as follows:

- single-party bridged ringing
- two-party divided ringing
- four-party fully-selective ringing
- dial-pulse or Digitone operation
- frequency-selective ringing
- compatible with loopextenders, repeaters, and analog concentrators
- protected against lightning surges, short circuits, and power line induction

The primary card features of the NT2X17 are as follows:

- programmable receive loss control in digital/analog (d/a) direction
- selection of balance networks that can be programmed
- power down mode minimizes power consumption in the idle state
- software-controlled cutoff
- synchronous ring rely operation to minimize transient generation
- senses line current for signaling and supervision purposes

The primary test features of the NT2X17 are as follows:

- metallic test access to the loop of a subscriber
- digital and analog loop-around
- ringing path continuity check
- bridged monitor access to the line circuit of a subscriber

Location

The NT2X17 card occupies one of the 32 plug-in line circuit (LC) positions in the line drawer.

NT2X17 (continued)

Functional description

The functional description of the line circuit card (Type A) is as follows:

- control
- supervision and signaling
- ringing
- ring trip
- receive speech path
- transmit speech path
- test circuits
- test access (TA)
- analog loop-around
- digital loop-around
- cutover control

Control

Communication between the LC card and the line drawer (LD) occurs through the digital receive/transmit sequences on the bidirectional bus. Each sequence consists of 10 bits. Each sequence can contain pulse code modulated (PCM) speech samples or signaling and control data.

In the receive digital-to-analog (d/a) direction, the access chip in the LC receives an initialization bit. A mode bit follows the initialization bit. The mode bit indicates if the other bits in the sequence represent PCM data or control data. After the system receives 10 bits, the bus direction reverses. The LC card transmits 10 bits of PCM speech or signaling data from the LC card to the LD. The LC card transmits the data through the access chip. The data transfer is complete. The 2.56 MHz transistor-to-transistor logic (TTL) clock signal from the LD times the data transfer sequences.

Supervision and signaling

The on/off-hook supervision and dial pulsing (DP) from the subscriber appears on the tip (T) and ring (R) leads of the analog line of the subscriber. The supervision hybrid detects the on/off supervision and the DP.

The supervision network passes the detected signals to the access chip in digital form. The system transfers digitone signaling to the access chip through the voice frequency (VF) transformer and coder decoder (Codec). The system inserts signaling information on the bidirectional bus. The system transfers

signaling information at the correct channel time during the data transfer sequence.

The flux balance winding of the VF transformer operates in conjunction with circuits in the supervision network. The flux balance winding automatically cancels any flux dc line currents that flow in the supervision circuits produce. The cancellation of flux improves the quality of the VF transformer for speech transmission.

Ringing

The ringing (RG) relay handles ringing signals destined for the equipment of the subscriber. The system addresses control message bits to the associated line card during the data transfer sequence. Control message bits cause the relay driver to operate the RG relay. When the relay driver operates the RG, the supervision voltages disconnect. The ringing bus connects to the supervision circuit. Outgoing ringing signals pass from the ringing bus multiplexer (MUX) card in the line drawer (LD). The ringing signals go through the VF transformer to the T and R leads of the line that belongs to the subsrcriber. The signaling processor in the line module controller (LMC) controls ringing signals. The remote line controller (RLC) in the line module (LM) or remote line module (RLM) controls ringing signals. Refer to NT2X14 for details on the LMC and RLC. Refer to NT0X45 for details of the LM and RLM.

Ring trip

The relay driver operates the RG and the ringing waveform can be present. When this condition occurs, the ring trip (RT) output of the supervision hybrid provides a linear voltage related to the loop current. The system applies the voltage to the Codec chip. The LMC or RLC processes the voltage to find a DC component. The DC component indicates a ring trip condition. The supervision data line provides the ring trip during the silent interval of the ringing waveform.

Receive speech path

Speech signals that route to a subscriber enter the LC card through the bus interface card in the LD. Speech signals enter as a stream of PCM samples of the analog voice signals. The LMC or RLC address the samples to specified line cards. Samples for the equipment of the subscriber appear at the access chip through the bidirectional bus receive path. The access chip passes the received PCM (RPCM) to the Codec and d/a filter circuits in the Codec/Filter chip.

The decoder section of the Codec changes the PCM samples to analog VFD signals. The d/a filter filters the VFD signals to construct the original analog VF signal. The VF passes through the buffer amplifiers in the transmission

NT2X17 (continued)

hybrid and the VF transformer. The VF passes to the tip (T) and ring (R) leads of the analog line that belongs to the subscriber. You can program loss control for the d/a speech path through control data on the bidirectional bus. Loss control is programmable through control data on the loss adjustment control line from the access chip.

Transmit speech path

In the transmit direction of transmission, analog VF signals from the equipment of the subscriber appear. The VF signals appear at the T and R leads of the line belonging to the subscriber. The VF signals pass through the VF transformer to buffer amplifiers and a high-pass filter in the transmission hybrid.

After high-pass filtering, the VF signals enter the transmit analog-to-digital (a/d) filter in the Codec/filter chip. The filter chip limits the bandwidth of the VF signals. The encoder section of the Codec samples VF signals at an 8-kHz rate. The VF signals convert to PCM samples. The transmit PCM (XPCM) routes through the access chip to the bus interface in the line drawer. In the line drawer, the PCM is multiplexed to a stream of similar samples from 31 other LC cards.

To achieve singing margin on all subscriber loops, the transmission hybrid includes two balancing networks. One network is for nonloaded loops. The other network is for loaded loops. Refer to the Technical data section in this chapter for exact network characteristics. Control data on the bidirectional bus programs the selection of the balance network. The balance network control line from the access chip programs the selection of the balance network.

A 2.56 MHz complimentary metal oxide semiconductor (CMOS) clock signal from the LMC or RLC (NT2X14) provides timing for the Codec.

Capacitor 1 (C1) provides a path for VF signals. The C1 does not allow the signals to enter the supervision circuits.

Test circuits

Coded control signals on the bidirectional bus activate the test circuits in the LC card. The code that the access chip receives determines the route of the signals. The access chip can send signals to relay drivers. The relay drivers operate the test access (TA) relay or the cut-off (CO) relay. The access chip can also use signals to activate test circuits in the access chip.

Test access

The test access (TA) provides metal contact with the analog line of the subscriber and the VF transformer. When relay drivers operate the TA and CO

relays, contacts of TA are closed. The contacts of CO are open. When This condition isolates the subscriber loop from the LC card. The system can apply subscriber loop tests through the TA to the T and R leads. When only the relay drivers operate the TA, the TA provides bridged monitor access. The TA provides access to the T and R leads of the subscriber and the VF transformer.

Analog loop-around

When only the relay drivers operate the CO, the T and R leads are isolated. The VF transformer is unbalanced. The VF transformer operates with almost zero loss. The analog loop-around contains a digital VF signal. The analog loop-around sends the VF signal to the access chip through the bidirectional bus from a test signal generator. After conversion to analog, the test signal crosses to the transmit path. The signal converts back to digital. The signal returns to the test equipment through the access chip and bidirectional bus. The system can test the condition of the transmit and receive signal circuits. The system compares the circuits to the input and output signals to test the condition of the circuits.

Digital loop-around

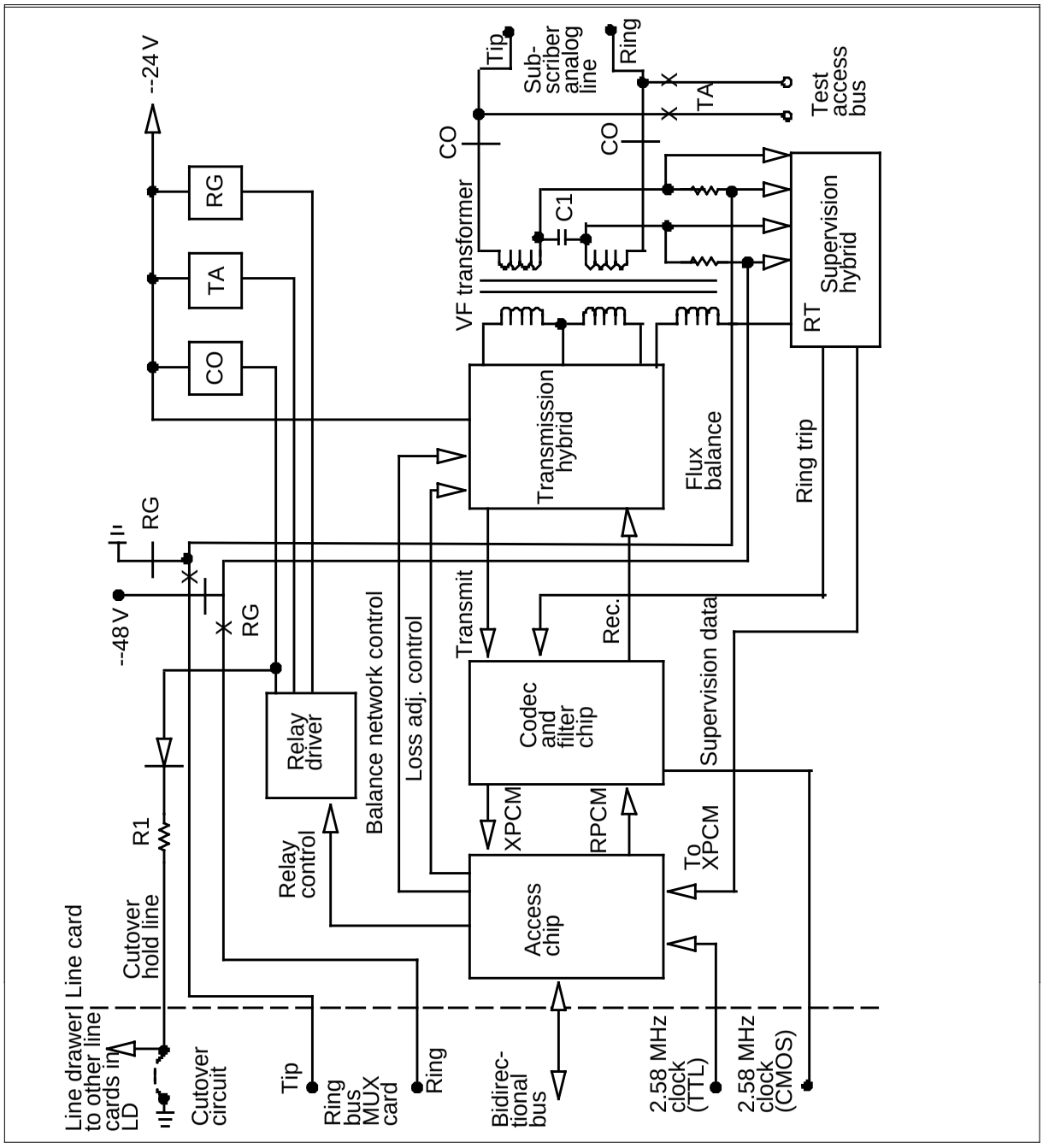
The correct control code appears on the bidirectional bus. The system loops the RPCM stream in the access chip to the XPCM stream. The system receives a special 8-bit test pattern and transmits the test pattern again. This test determines the accuracy of the digital PCM channel and the receive and transmit circuits of the access chip.

Cutover control

The CO relay also provides a facility for software-controlled cutover. For cutover, a cutover hold line ground occurs through a common cutover circuit in the LD. Current flows through the CO relay with R1 and the cutover line. The CO relays in all LC cards in the LD are opened but not operated. This condition causes the CO contacts to be open. This condition isolates the T and R leads of the addressed line circuit. The isolation occurs from the connections sequence on the bidirectional bus to the main distribution frame (MDF). When the data exchange sequence on the bidirectional bus completes, the system removes the cut-off control code. The current through the cutover hold line holds the CO relay in the operated state. At cutover time, removal of the ground on the cutover hold line occurs. This action opens the hold current path for all CO relays in the line drawer. The system releases any CO relay that was set to the cut-off state earlier. The tip and ring leads of LC cards connect to the associated MDF connections.

NT2X17 (continued)

NT2X17 functional blocks



Technical data

The technical data section provides the following specifications for the NT2X17:

- signaling characteristics
- power requirements
- equipment dimensions
- environmental conditions
- transmission specifications

Signaling characteristics

The specifications for signaling characteristics appear in the following table.

Signaling characteristics

Signaling	Characteristics
Talk battery	-42.5V to -55.8V
Normal range (float charge)	-49V to -53.5V
Maximum discharge (no charge)	-42.75V
Maximum charge (equalizing)	-55.8V
Ground resistance	50ohms maximum
Lightning surge protection	1kV (10 X 1000 usec) tip/ring, tip/ground, ring/ground
60 Hz ac induction (steady state)	normal service with a maximum of 40 mA for each conductor, longitudinal induction
Short circuit protection (through R2 and R3)	tip/ring, tip/ground, ring/ground
Total loop resistance (including 500 type set for 21 mA)	≤2000 ohms maximum
Conductor leakage resistance	≥10 kohms minimum

NT2X17 (continued)

Power requirements

The NT2X17 power requirements appear in the following table.

Power requirements	
Power consumption	250mW
Converted voltages	+15V ±1% +24V ±0.5 V

Equipment dimensions

The NT2X17 dimensions are 101.6 mm (4 in.) in height and 101.6 mm (4 in.) in width. The approximate weight is 170 g (6 ounces).

Environmental conditions

The NT2X17performs under limited environmental constraints that appear in the following table.

Ambient conditions

Condition	**Operating range**	**Short-term range**
Temperature	10 °C to 30 °C (50 °F to 86 °F)	5 °C to 49 °C (41 °F to 120.2 °F)
Relative humidity	20% to 55%	20% to 80%

Note: A relative humidity of 80% is expected at an ambient temperature of 21°C (69.8°F) maximum. At an ambient temperature of 49°C (120.2°F), the relative humidity is expected to be 30% maximum.

Transmission specifications

Specifications for transmission specifications appear in the following table.

Transmission specifications (Sheet 1 of 2)

Heading	**Heading**
Transmission level point (TLP) at MDF	0 dBm
Overload level	+3 dBm

Transmission specifications (Sheet 2 of 2)

Heading	Heading
Frequency response	Relative loss
200-250 Hz	4.0 dB
250-300 Hz	2.0 dB
350-2400 Hz	0.75 dB
2400-3000 Hz	2.0 dB
3000-3400 Hz	4.0 dB
Return loss (900 ohm #2.16 uF)	
echo return loss (ERL)	20 dB
structural return loss (SRL)	14 dB
Programmable d/a loss range	0 through 7 dB (in 1 dB increments)
Programmable balancing networks	
nonloaded cable	927 ohm #0.039 uF
loaded cable (#. connected in parallel)	1650 ohm #0.005 uF

NT2X18

Product description

The line circuit (LC) card (type B) provides voice and signaling interfaces between:

- two-wire analog subscriber lines
- the four-wire, 32-channel, 2.56 Mbit/sec digital bit stream of the DMS-100 Family switching systems

Each card provides a single, two or multi-party interface with one channel of the DMS system.

The LC cards (type B) have two configurations. Northern Telecom identifies the configurations with product engineering codes (PEC) NT2X18AC and NT2X18AD. Both cards interface with the following:

- subscriber lines
- coin ringing circuits
- private automatic branch exchange (PABX) ringing circuits
- coded ringing circuits

The NT2X18AD card has more complete coin features than NT2X18AC.

Features

The NT2X18 provides primary usability features for the following:

- subscriber line interface
- coin features
- PABX features
- business features
- card features
- test features

The subscriber line features include the following:

- provides dial pulse (DP) or DIGITONE (DGT) operation
- provides compatibility with loop extenders, repeaters, and analog concentrators
- protects against lightning surges, short circuits, and power line induction
- provides single-party bridged ringing
- provides two-party AC/DC superimposed ringing

- provides four-party fully selective ringing
- provides frequency-selective ringing
- provides multi-party AC/DC, superimposed or frequency-selective ringing (bridged or divided)

The coin features include the following:

- provides dial tone first (NT2X18AC only)
- provides dial tone first, with or without +48V on tip, loop start (NT2X18AD only)
- provides semi post-pay
- allows compatibility with single-slot or multi-slot coin stations
- provides coin-first operation, with or without +48V on tip, ground start (NT2X18AD only)

The PABX features include the following:

- provides ground start or loop start option
- provides toll diversion
- provides hotel or motel service
- provides WATS and TWX

The business features include the following:

- allows compatibility with key telephone systems (1A2 or equivalent), foreign exchange (FX) lines, bridge lifters, and telephone answering service and recordings

The card features include the following:

- provides programmable receive loss control in the digital-to-analog (D/A) direction
- provides programmable selection of balance networks
- provides power-down mode to minimize power consumption in the idle state
- provides software-controlled cutover
- provides synchronous ring relay operation to minimize transient generation
- senses line current for signaling and supervision purposes

NT2X18 (continued)

The test features include the following:

- provides metallic test access (MTA) to the loop of the subscriber
- provides digital and analog loop-around
- provides bridged monitor access to the lc of the subscriber
- provides diagnostics, signaling self-test during cutover (NT2X18AD only)

Location

The NT2X18AD or the NT2X18AD occupies one of 32 plug-in LC positions in the line drawer (LD).

Functional description

Communication between the LC card and the LD occurs through digital receive and transmit sequences on the two way bus. The sequences contain 10 bits. The sequences can contain pulse code modulation (PCM) speech samples or control data.

In the receive (D/A) direction, the access chip in the LC card receives an initialization bit. A mode bit follows the initialization bit. The mode bit indicates if the other bits in the sequence represent PCM or control data. After the LC receives 10 bits, the bus direction reverses. At this point the system transmits 10 bits of PCM or control data from the LC card and through the access chip. The system transmits the bits to the LD, to complete the data transfer. The 2.56 MHz transistor-transistor logic (TTL) clock signal from the LD times the data transfer sequence.

The system transfers the DGT signaling to the access chip through the voice frequency (VF) transformer and Codec. The system inserts signaling information on the two way bus. The system transfers the information at the correct channel time during the data transfer sequence.

The flux balance winding of the VF transformer operates in conjunction with circuits in the supervision network. These components cancel any flux that line currents flowing in the supervision circuits produce. This condition improves the quality of the VF transformer for speech transmission.

Supervision and signaling

On-hook supervision, off-hook supervision, and DP from the subscriber appear on the tip and ring (T/R) leads of the analog line of the subscriber. Supervision and signaling functionality varies and depends on if the system uses the NT2X18AC or the NT2X18AD.

NT2X18AC

For the NT2X18AC, the supervision network loop detector or the tip detector accomplishes detection. The data selector selects the loop detector or tip detector outputs. The selection occurs in response to a control message from the access chip. Loop or coin mode supervision passes through the data selector to the transmit PCM (XPCM) path in the access chip.

NT2X18AD

For the NT2X18AD, detection occurs across resistors R2 and R3. The loop signaling mode uses both resistors. The coin mode uses R2. The loop/coin mode selector line selects the loop or coin outputs in response to a control message from the access chip. Loop or coin mode supervision passes through the supervision line to the XPCM path in the access chip.

Ringing

The ringing relay handles ringing signals the system routes to the equipment of the subscriber. Control message bits, addressed to associated LC during the data transfer sequence, cause the relay driver to operate the ringing relay. When the ringing relay is operated, the supervision voltages are disconnected and the ringing bus connects to the supervision circuit. Outgoing ringing signals pass from the ringing bus multiplexer (MUX) card in the LD through the VF transformer. The ringing signals at this point pass to the T/R leads of the line of the subscriber. The signaling processor (SP) in the line module controller (LMC) controls ringing signals. The remote line module (RLM) in the line module (LM) or the remote line controller (RLC) can also control ringing signals.

Note: Refer to hardware description NT2X14 for the LMC and RLC. Refer to hardware description NT0X45 for the LM and RLM.

Ring tip

Ringing relay can operate when the ringing waveform is present. When this condition occurs, the system provides a linear voltage proportional to loop current at the RT output or the supervision network. This voltage applies to the Codec chip. The LMC or RLC processes the voltage to determine the presence of a dc component and indicates a ring trip condition. The system provides ring trip during the silent interval of the ringing waveform through the supervision data line.

Receive speech path

Speech signals the system routes to a subscriber enter the LC card through the bus interface card (BIC) in the LD. These signals enter as a stream of PCM samples of the analog voice signals. Samples for equipment of the subscriber appear at the access chip through the two way bus receive path. The LMC or

NT2X18 (continued)

RLC addresses these samples to an exact LC card. The access chip passes the receive PCM (RPCM) to the Codec and D/A filter circuits in the Codec/filter chip.

The decoder section of the Codec changes the PCM samples into analog VF signals. The D/A filter filters these analog VF signals to reconstruct the original analog VF signal. The VF passes through the buffer amplifiers in the transmission hybrid. The VF also passes through the VF transformer to the T/R leads of the analog line of the subscriber. Loss of control for the D/A speech path is programmable through control data. This path is programmable on the two way bus and the loss adjustment control line from the access chip.

Transmit speech path

In the transmit direction of transmission, analog VF signals enter the transmit analog/digital (A/D) filter in the Codec/filter chip. The filter chip limits the bandwidth of the VF signals. The VF signals from the equipment of the subscriber appear at the T/R leads of the line that belongs to the subscriber. The VF signals pass through the VF transformer to buffer amplifiers and a 60Hz filter in the transmission hybrid.

After high-pass filtering, the encoder section of the Codec samples the VF signals. The Codec samples the VF signals at an 8 kHz rate. The Codec converts the VF signals to XPCM samples. The system routes the PCM through the access chip to the bus interface in the LD. The PCM is multiplexed to a stream of similar samples from 31 other LC cards in the LD.

To achieve the singing margin on all subscriber loops, two balancing networks are included in the transmission hybrid. One network is for loops that are not loaded. The other network is for loaded loops. Selection of the balance network is programmable through the control data on the two way bus. Selection of the balance network is also programmable through the balance network control line from the access chip.

The 2.56 MHz (CMOS) clock signal from the LMC or RLC provides timing from the Codec. The C1 provides a path for VF signals. The C1 does not allow the signals to enter the supervision circuits.

Test circuits

Coded control messages on the two way bus activate the test circuits in the LC card. The route of the signal depends on the code the access chip receives. The access chip can send the signals to the relay driver. The relay driver operates the test access (TA) relay or the cutoff (CO) relay. The access chip can also use the signals to activate test circuits in the access chip.

Test access (TA) relay

The TA relay provides metal contact with the analog line of the subscriber and the VF transformer. With TA and CO relays operated, the contacts of TA are closed. The contacts of the CO are operated. This operation isolates the loop of the subscriber from the LC card. This action allows the system to apply subscriber loop tests through the TA to the T/R leads. Only the TA relay is operated. The TA provides bridged monitor access to the T/R leads of the subscriber and VF transformer.

Digital loop-around

The correct control code can appear on the two way bus. When this condition occurs, the system loops the RPCM stream in the access chip to the XPCM stream. The system receives a special 8-bit test pattern. The system transmits the test pattern again. The test determines the integrity of the digital PCM channel. The test also checks the integrity of receive and transmits circuits of the access chip.

Analog loop-around

With only the CO relay operated, the T/R leads are isolated and the VF transformer is unbalanced. This condition allows the VF signals on the receive path to appear on the transmit path with approximately zero loss. The analog loop-around contains a VF signal in digital form. The analog-loop around sends the VF signal to the access chip. The analog sends the signal through the two way bus from a test signal generator. After conversion to analog, the test signal crosses the transmit path. The test signal converts back to digital and returns to the test equipment through the access chip and the two way bus. By comparison of the input and output signals, the condition of the transmit and receive circuits can be tested.

Cutover control

The CO relay also provides a facility for software-controlled cutover. For cutover, the cutover hold line is grounded through a common cutover circuit in the LD. Enough current flows through the CO relay through R1 and the cutover hold line. This condition causes the CO relays in all LC cards in the LD to be energized, and not operated. When addressed to a specific LC through the two way bus, the CO control code operates in the addressed LC. This condition opens the CO contacts. This condition also isolates the T/R leads of the addressed LC from the connections to the main distribution frame (MDF).

After the data exchange sequence on the two way bus completes, removal of the CO control code occurs. The current through the cutover hold line holds the CO relay in the operated state. At cutover time, removal of the ground on the cutover hold line occurs. This condition opens the hold current path for all CO relays in the LD. Any CO relay previously set to the cutoff state is released.

NT2X18 (continued)

This condition simultaneously connects the T/R leads of any selected number of LC cards to the associated MDF connections.

Self-test network

Register-diode network R4/CR1 contains a signaling self-test network. The self-test network connects across the T/R leads to the line circuit when the CO relay is operated. The self-test network can determine the functioning of relays RG, TP, RV1, and RV2 and switch S1. The network monitors the supervision data and the presence or absence of loop current. The network can apply diagnostic tests through the two way bus to determine all relay states. During the analog loop-around test, the self-test network does not operate. The network does not operate because the -48V on the ring leads reverse biases the diode.

Coin mode control

The coin mode control descriptions vary and depend on if the system uses the NT2X18AC or the NT2X18AD.

NT2X18AC

For the NT2X18AC in coin mode, the data selector receives a control code through the access chip. The control code selects the tip detector as a source of supervision. Coin mode control uses the reversal relay RV. When a control message from the access chip operates a RV, the RV reverses the polarity of the signaling voltage on the T/R leads. Relay RV operates on operator assisted connections. Relay RV disables the DGT termination pad in the telephone set and prevents the generation of false coin signaling tones. Relay RV is under software control through the access chip and relay driver.

NT2X18AD

For the NT2X18AD in coin mode, the supervision network receives a control code from the loop and coin selector line from the access chip. The control code selects the input from tip resistor R2 as a source of supervision. Coin mode control activates when relay RV1 operates.

Relay RV1 operates on operator-assisted connections. Relay RV1 reverses the and reverses the T/R leads of the subscriber. This action disables the DGT termination pad in the telephone set and prevents the generation of false coin signaling tones.

When relay RV2 operates with relay RV1, the two relays reverse the polarity of the signaling voltage. The polarity of the signaling voltage is normally ground on tip and -48V on ring. Relay RV2 and RV1 reverse the polarity to ground on tip and +48V on ring. Operation in this mode requires the use of a +48V power converter (NT2X03AA) in the LD. When the system uses relay

RV2, coin mode supervision is not required. The system selects loop mode supervision. Relays RV1 and RV2 are under software control through the access chip and relay driver.

Ground start option

The ground start option functionality varies and depends on if the system uses NT2X18AC or the NT2X18AD.

NT2X18AC (PABX service)

For the NT2X18AC, switch S1 on the card is set to the GD position. This condition occurs in conjunction with the normally operated contacts of the tip relay TP. This condition manually programs the card to interface with a ground start PABX. A ground start seizure consists of a ground on the ring lead. A seizure passes the ground through the supervision network and access chip to the two way bus and to the switching system. When the system recognizes a valid seizure, the system responds with a control message which operates relay TP. When TP contacts close, the tip lead circuit is closed and normal supervision is in effect. At the same time, a disabled ac filter in the supervision network allows the detection of dial pulsing (DP).

NT2X18AD (PABX service or coin-first service)

For the NT2X18AC, switch S1 is set to the GD position. This setting can occur in conjunction with the normally operated contacts of the tip relay TP. When this condition occurs, this setting manually programs the card to interface with a ground start PABX or coin-first pay telephone. In the GD position, the following procedure occurs:

- the tip circuit of the subscriber is opened
- the supervision threshold is altered for single-lead supervision (through TP closed contacts
- a 60Hz filter line to the supervision network is enabled
- the ring lead of the subscriber connects to a current-limited battery through resistors R3 and R5.

A ground start seizure includes a ground on the ring lead. The ground is detected across resistor R3 and passes through the supervision network to the switching system. When the system recognizes a valid seizure, the system responds with a control message which operates relay TP. When TP contacts close, the tip lead circuit closes. If this event occurs, the supervision threshold alters for loop supervision, and the ac filter in the supervision network is disabled. This occurrence allows for the detection of dial pulsing (DP). Normal supervision is in effect.

NT2X18 (continued)

Loop start option

The loop start option functionality varies and depends if the NT2X18AC or the NT2X18AD is in use.

NT2X18AC (PABX service)

Set the S1 switch to the LP position to program the NT2X18AC card. The LP position by-passes the TP contacts in the tip lead circuit. A loop start seizure includes a loop closure across the T/R leads. The system detects the seizure and passes the seizure through the supervision network to the switching system. When the system recognizes a valid seizure, the system responds with a control message that operates relay TP. The contacts of the TP close and disable an ac filter in the supervision network. This procedure allows for the detection of DP.

NT2X18AD (PABX service or coin-first service)

The S1 switch is set to the LP position to program the NT2X18AC. In the LP position, the normally opened contacts of the tip relay TP are bypassed. This occurrence closes the tip circuit of the subscriber and short-circuits resistor R5. In the LP position, the supervision threshold line and ac filter line are open which disables these two circuits. A loop start seizure includes a loop across the T/R leads that passes through the supervision network to the switching system. Resistor R2 and R3 detect a loop across the T/R leads. Loop starts do not require the TP relay operation because the ac filter is already in the disable position. This procedure allows for the detection of DP.

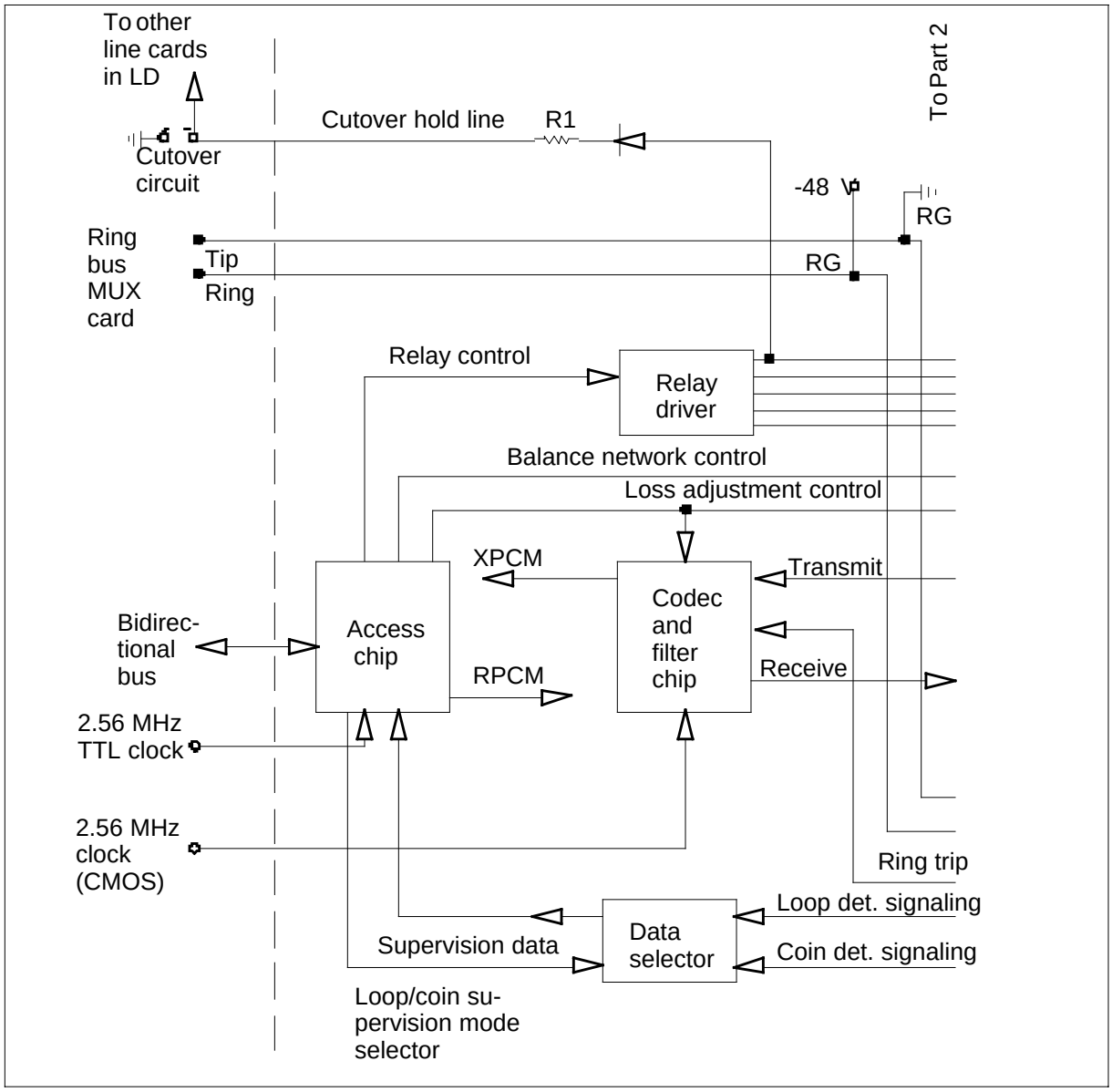
The following figures illustrate the NT2X18:

- Line card, Type B (Part 1 of 2)
- Line card, Type B (Part 2 of 2)

- Line card, Type B with +48V (Part 1 of 2)
- Line card, Type B with +48V (Part 2 of 2)

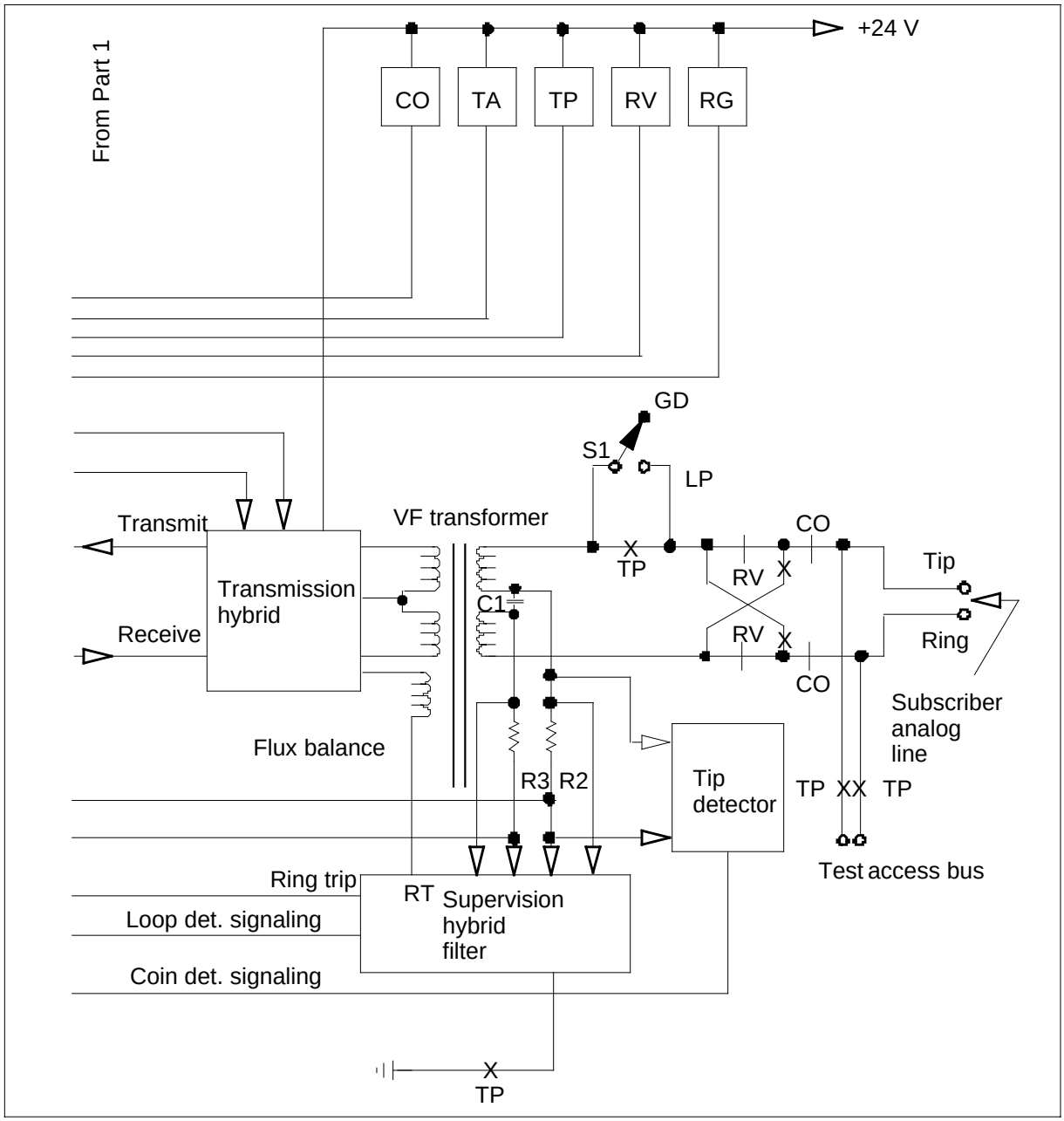
Note: These figures appear in split frames to improve the readability of the complex diagrams.

NT2X18 Line card, Type B (Part 1 of 2)

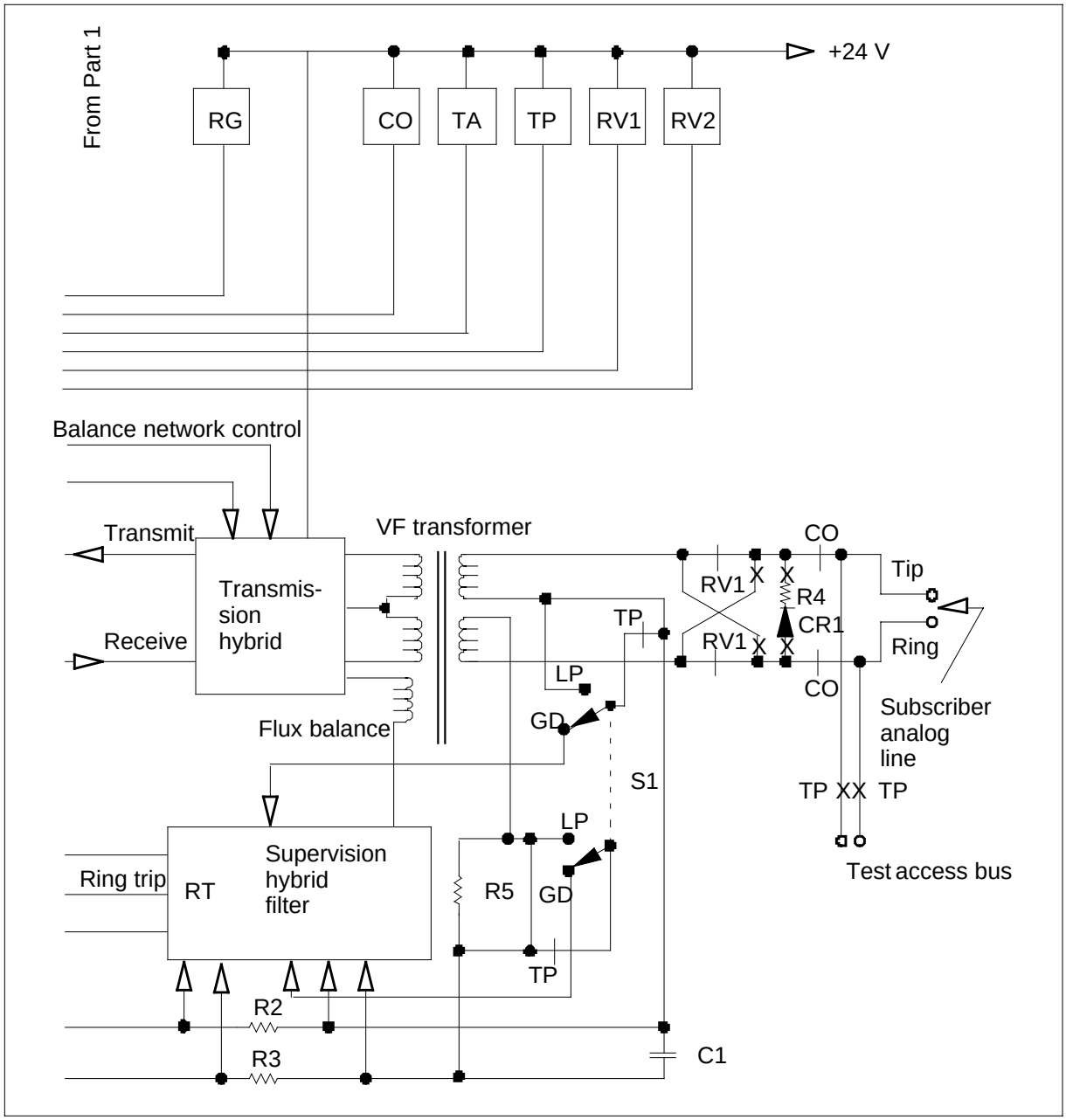


NT2X18 (continued)

NT2X18 Line card, Type B (Part 2 of 2)

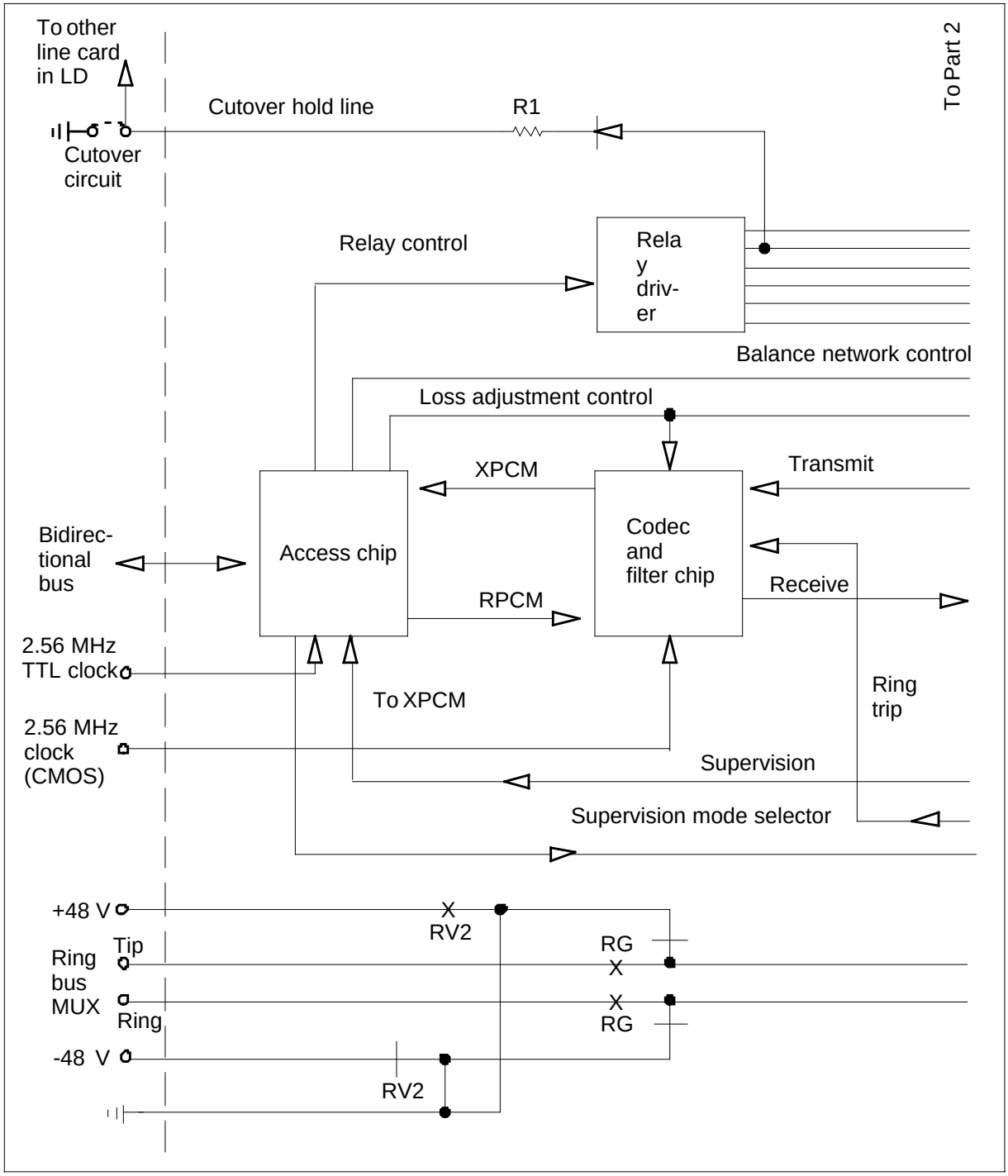


NT2X18 Line card, Type B with +48 V (Part 1 of 2)



NT2X18 (continued)

NT2X18 Line card, Type B with +48 V (Part 2 of 2)



Technical data

The technical data section for the NT2X18 provides specifications for the following:

- the power requirements
- transmission specifications
- equipment dimensions
- environmental conditions
- signaling characteristics

Power requirements

The NT2X18 power requirements appear in the following table.

Power requirements

Power consumption	NT2X18AC: 420 mW (idle) NT2X18AD: 220 mW (idle)
Converted voltages	+24V ±0.5V +15 V ±1%

Transmission specifications

The NT2X18 transmission specifications appear in the following table.

Transmission specifications (Sheet 1 of 2)

Transmission level point (TLP) at MDF	0 dBm
Overload level	+3 dBm
Frequency response	Relative loss
200-250 Hz	4.0 dB
250-300 Hz	2.0 dB
300-1400 Hz	0.75 dB
2400-3000 Hz	2.0 dB
3000-3400 Hz	4.0 dB
Return loss (900 ohm #2.16 uF)	
Echo return loss (ERL)	20 dB
Structural return loss (SRL)	14 dB

NT2X18 (continued)

Transmission specifications (Sheet 2 of 2)

Programmable D/A loss range	0 through 7 dB (in 1 dB steps)
Programmable balancing networks	
Nonloaded cable	927 ohm #00.039 uF
Loaded cable (# . connected in parallel)	1650 ohm #0.005 uF

Equipment dimensions

The NT2X18 dimensions are 101.6 mm (4 in.) in height and 101.6 mm (4in.) in width. The approximate weight of the NT2X18 is 170 g (6 oz).

Environmental conditions

The NT2X18 performs under limited environmental constraints. These constraints appear in the following table.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	10°C to 30°C (50°F to 86°F)	5°C to 49°C (41°F to 120.2°F)
Relative humidity	20% to 55%	20% to 80%

Note: A relative humidity of 80% is expected at an ambient temperature of 21°C (69.8°F) maximum. At an ambient temperature of 49°C (120.2°F), the relative humidity is expected to be 30% maximum.

Signaling characteristics

The NT2X18 signaling characteristics appear in the following table.

Signaling characteristics (Sheet 1 of 2)

Talk battery	-42.75 V to -55.8 V
Normal range (float charge)	-49.0 V to -53.5 V
Maximum discharge (no charge)	-42.75 V
Maximum charge (equalizing)	-55.8 V
Ground potential	±3 V
Ground resistance	50 ohm maximum

Signaling characteristics (Sheet 2 of 2)

Lightening surge protection	1 kV (10x100 us) tip/ring, tip/ground, ring/ground
60 Hz induction (steady state)	Normal service with maximum 40 mA for each conductor, longitudinal induction.
Short circuit protection (through R2 and R3)	Tip/ring, tip/ground, ring/ground
Total loop resistance (including 500 type set for 21 mA) Residential Coin	≤2000 ohm maximum ≤1600 ohm maximum
Ground start (NT2X18AD only) Ring lead resistance	1040 ohm maximum
Conductor leakage resistance	
Residential	≤10 kohm minimum
Coin	≤30 kohm minimum

NT2X31AJ

Product description

The NT2X31AJ digital carrier module (DCM) functions as the interface between the following units of the DMS digital network:

- a maximum of five 24-channel, 1.544 Mbps DS-1 carrier systems
- a four 32-channel, 2.56 Mbps DS30 duplicated links (ports)

The module performs all the basic functions to convert signals between the DS-1 and DS30 formats. The module also functions as an interface for the DS-1 A/B bits signaling method and the DS30 signal distribution (SD)/scan method.

The following three DCM configurations are available:

- the basic or DCM-B version (NT2X31AJ) provides the basic interface functions
- the DCM-S version (NT2X31AE) provides the basic functions. The DCM-S version contains additional circuits for clock synchronization
- the DCM-R version functions as an interface for
  - — a maximum of four DS-1 carrier systems and a remote line module (RLM) link
  - — a maximum of five RLM links
  - — any collection of five DS-1 carrier systems and RLM links

The DCM-R version can also have clock synchronization circuits.

In the DCM-B (NT2X31AJ), an algorithm assigns the speech channels on five DS-1 links to an equal number of DS30 channels. The DS30 channels are on four DS30 links. The algorithm distributes the channels evenly over the four DS30 links.

The control section controls operation of the DCM-B. The control card includes the following circuit cards:

- control (NT2X33AA)
- supervision (NT2X34AA)
- tone (NT2X37AA)
- signaling (NT2X38AA)

The processor circuit card (NT2X32AA) controls the control section.

The module also includes the following:

- power converters (NT2X06AA and NT2X07AA)
- a network interface (NI) circuit card (NT2X36AA)
- a maximum of five DCM interface (DS-1 line) circuit cards (NT2X35AA)

A bidirectional, 2.56 Mbps speech bus connects the DCM interface circuit cards and the NI circuit card. The speech bus has four paths in each direction. Each two-way path is associated with one of the four duplicated speech links. A processor bus (P-bus) links the circuit cards in the control section.

The module includes a maintenance bus that links the DCM interface circuit cards. The DCM signaling circuit card provides a separate path to monitor the DS-1 channels. The path detects the following:

- slips
- reframing
- sustained synchronization losses
- bipolar variations
- remote alarms

The path also provides a card-present signal for each DCM interface circuit card.

The DCM-B features looparound functions for the network and DCM interface circuit cards.

Parts

The DCM contains the following components:

- NT2X32AA—DCM processor card
- NT2X33AB—Control circuit card
- NT2X34AA—Supervision circuit card
- NT2X35AB—DCM interface (DS-1 line) circuit cards
- NT2X36AA—NI card
- NT2X36AB—NI card
- NT2X37AB—Tone circuit card

NT2X31AJ (continued)

- NT2X38AB—Signaling circuit card
- NT2X70AA—Power converter
  - — NT2X06AA—Power converter feature
  - — NT2X07AA—Power converter feature

Design

The NT2X31AJ design appears in the following table and figure.

NT2X31AJ components (Sheet 1 of 4)

Card PEC	Slot	Description
NT0X50AC	11F, 15F, 16F	*Filler face plate* The filler face plate or panel fills empty card slots in the unit. Each unit has a maximum of five spare card slots. Slots 15, 16, and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. Slots 13 and 19 do not have access.
NT0X50AE	1F, 17F, 18F	*Filler face plate* The filler face plate or panel fills empty card slots in the unit. Each unit has a maximum of five spare card slots. Slots 15, 16, and 17 have access to the SP address bus and the parallel speech bus. Slots 13 and 19 do not have access.
NT2X70AA	19F, 20F	*Power converter* The power converter converts the -48V dc battery voltage into the regulated dc voltages that the DCM circuits require. The NT2X06AA power converter feature produces a heavy-duty, +5V, 40-A output. The NT2X07AA power converter feature produces dual -5V and +12V outputs. The battery voltage is applied to the power converters through the frame supervisory panel (FSP).

NT2X31AJ components (Sheet 2 of 4)

Card PEC	Slot	Description
NT2X32AA	14F	*Digital carrier module processor card* The DCM processor circuit card contains a microprocessor, a maximum of 3K of RAM, and a 2K PROM. The circuit card performs the following to control operation of the circuit cards in the DCM-B shelf: • reads commands received from the DMS control module (CM) • acts on the commands • responds to line changes that the supervision and signaling circuit cards detect The processor communicates with the other circuit cards in the control section over the processor bus. The processor includes interrupt capabilities. The processor features single-line enable signals for each card. Parity over data detects memory faults.
NT2X33AB	13F	*Control circuit card* The control circuit card contains circuits that work with the CM. A ROM controls these circuits. These circuits handle messages. The card contains: • a message buffer • detection-code firmware to detect a reset message • a sanity timer that is responsible for DCM sanity The card includes a phase-locked loop (PLL) that extracts the 10.24-MHz clock signal from the network speech data.
NT2X34AA	12F	*Supervision circuit card* The supervision circuit card includes a hard-wired sequencer. The sequencer exchanges channel supervisory messages with the network and parity-detection circuits that check incoming speech signals. All 120 speech channels share the circuits. The circuit card includes a processor bus interface with interrupt capabilities.

NT2X31AJ (continued)

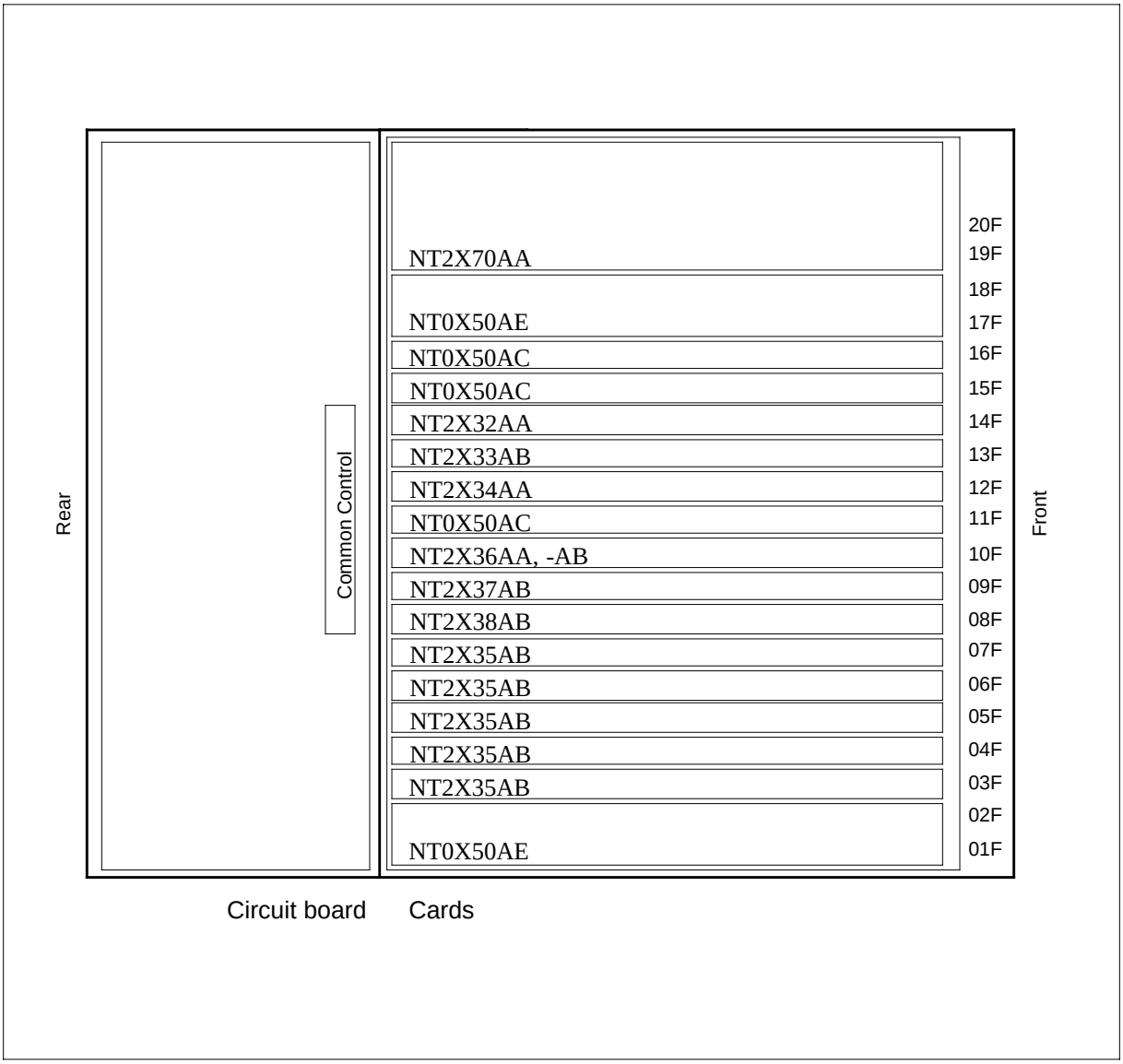
NT2X31AJ components (Sheet 3 of 4)

Card PEC	Slot	Description
NT2X35AB	3F-7F	*Digital carrier module interface circuit card* The DCM interface (DS-1 line) circuit card contains the DS-1 transmit and receive interface circuits. The receive circuits include the following: • bipolar decoder • slip-and-retiming buffer • A/B frame detection The transmit circuits include zero-suppression logic, a two-channel-long elastic buffer for retiming, and bipolar modulation circuits. The circuit card sends alarm, error, and administration data to the signaling circuit card over the maintenance bus. The DCM interface circuit card includes maintenance features like the following: • local alarm input • remote alarm • slips • bipolar violation outputs • monitoring outputs for slip buffer phase. These outputs are for office synchronization • card-present output • looparound for the DS-1 circuits The DCM interface does not include the bipolar encoder and decoder.
NT2X36AA	10F	*Network interface card* The NI card contains eight biphase modulators, one for each plane of the four DS30 ports. The circuit card includes parity generation for signals sent to the network. The circuit card includes maintenance looparound circuits for the eight speech bits.

NT2X31AJ components (Sheet 4 of 4)

Card PEC	Slot	Description
NT2X36AB	10F	*Network interface card* The NI card contains eight biphase modulators, one for both planes of the four DS30 ports. The circuit card includes parity generation for signals sent to the network. The circuit card includes maintenance looparound circuits for the eight speech bits.
NT2X37AB	9F	*Tone circuit card* The tone circuit card controls tone insertion and looparound. The tone circuit card contains a digital tone generator and a channel memory. The tone circuit card generates the following: • dial tone • alternative dial tone • audible ring • multifrequency (MF) signaling signals
NT2X38AB	8F	*Signaling circuit card* The signaling circuit card contains circuits that extract the A/B signaling bits from the DS-1 data streams. The circuits receive the data streams from the DCM interface (DS-1 line) circuit cards. A filter eliminates the effects of contact bounce and carrier hits. A scanner that a ROM controls monitors the buffers. The scanner reports changes in the received A/B bits. Buffers and timers produce output pulses, and insert A/B bits onto the speech bus. Maintenance circuits and circuits that monitor lines for all DCM interface (DS-1 line) circuit cards are also provided.

NT2X31AJ components



NT2X31AT

Product description

Enhanced Network (ENET) applications use the NT2X31AT digital carrier module (DCM) shelf. This shelf mounts in an NT0X46AB frame. This shelf provides an interface between the DMS-100 Family switching network and digital trunk facilities. The DCM presents a standard interface to the primary digital carrier signal. The primary digital carrier signals is DS-1. This DS-1 signal contains 24 VF channels time multiplexed onto a 1.544 Mbit/s stream. The DS-1 line signaling format defines the time multiplier for the VF channels. The DCM provides an interface for a maximum of five DS-1 links. The DS-1 links have four 32-channel speech links to each of the duplicate networks. The module provides all the basic functions to convert signals between the DS-1 and DS30 formats. The module also functions as an interface for the DS-1 A/B bits signaling method and the DS30 signal distribution (SD)/scan method.

In the DCM, an algorithm assigns the speech channels on five DS-1 links to an equal number of DS30 channels. These channels are on four DS30 links. The algorithm distributes the channels evenly over the four DS30 links. The control section operates the DCM.

The control section includes the following cards:

- control (NT2X33AE)
- supervision (NT2X34AA)
- tone (NT2X37AB)
- signaling (NT2X38AC) circuit

The processor circuit card (NT2X32AA) runs the control section. The module includes:

- a power converter (NT2X70AE)
- a network interface (NI) circuit card (NT2X36AA)
- a maximum of five DCM interface (DS-1 line) circuit cards (NT2X35AB).

A bidirectional, 2.56 Mbit/s speech bus connects the DCM interface circuit cards and the NI circuit card. The speech bus has four paths in each direction. Each two-way path is associated with one of the four duplicated speech links. A processor bus (P-bus) links the circuit cards in the control section.

The module also includes a maintenance bus that links the DCM interface circuit cards. The DCM signaling circuit card provides a separate path that can

NT2X31AT (continued)

use to monitor the DS-1 channels. The path provides a card-present signal for each DCM interface circuit card. The path detects the following:

- slips
- reframing
- sustained synchronization losses
- bipolar variations

The DCM features looparound functions for the network and DCM interface circuit cards.

Parts

The NT2X31AT contains the components that follow:

- NT2X32AA-DCM processor card
- NT2X33AE-control circuit card
- NT2X34AA-supervision circuit card
- NT2X35AB-DCM interface (DS-1 line) line circuit cards
- NT2X36AA-NI card
- NT2X37AB-tone circuit card
- NT2X38AC-signaling circuit card
- NT2X70AE-power converter

Design

A description of the components appears in the following table. The design of the NT2X31AT appears in the following figure.

NT2X31AT parts (Sheet 1 of 3)

PEC	Slot	Description
NT2X32AA	14F	*Digital carrier module processor card* The DCM processor circuit card contains a microprocessor, a maximum of 3K of RAM, and a 2K PROM. The card interprets and acts on commands that the DMS control module (CM) sends. The card responds to line changes the supervision and signaling circuit cards detect. These processes allow the card to control the operation of the circuit cards in the DCM shelf. The processor communicates with the other circuit cards in the control section over the processor bus. The processor includes interrupt abilities. The processor features single-line, enable signals for each card. Parity over data detects memory faults.
NT2X33AE	13F	*Control circuit card* The control card has a 50 ms message timer limit that allows the DCM to work in ENET applications. The card provides reset signals, frame pulses, and clock pulses to other circuit cards. The card exchanges maintenance information with the NT2X32AA processor card. The card processes message bytes. The card checks interoffice synchronization.
NT2X34AA	12F	*Supervision circuit card* The supervision circuit card includes a hard-wired sequencer that exchanges channel supervisory messages with the network. The card contains circuits that detect parity. The circuits check incoming speech signals. All 120 speech channels share the circuits. The circuit card also includes a processor bus interface with interrupt capabilities.

NT2X31AT (continued)

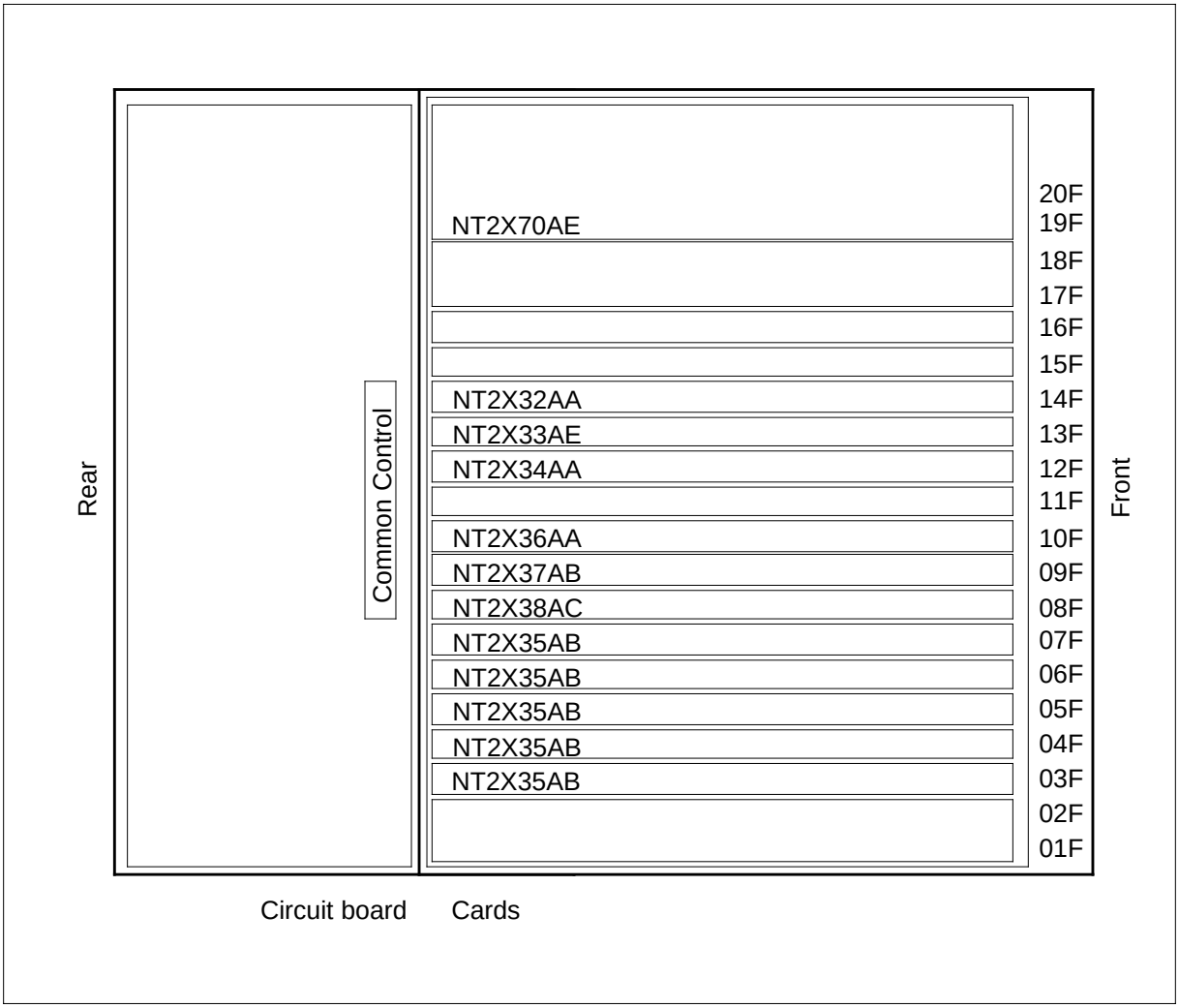
NT2X31AT parts (Sheet 2 of 3)

PEC	Slot	Description
NT2X35AB	3-7F	*Digital carrier module interface circuit card* The DCM interface (DS-1 line) circuit card contains the DS-1 transmit and receive interface circuits. The receive circuits include a bipolar decoder, a slip-and-retiming buffer, and A/B frame detection. The transmit circuits include zero-suppression logic, a two-channel-long elastic buffer for retiming, and bipolar modulation circuits. The circuit card sends alarm, error, and administration data to the signaling circuit card over the maintenance bus. The DCM interface circuit card includes maintenance features like the following: • local alarm input • remote alarm • slips • bipolar violation outputs • slip buffer phase monitoring outputs for office synchronization • card-present output The DCM interface incorporates looparound for the DS-1 circuits. The DCM interface does not include the bipolar encoder and decoder.
NT2X36AA	10F	*Network interface card* The NI card contains eight biphase modulators, one for each plane of the four DS30 ports. The circuit card includes parity generation for signals sent to the network. The circuit card includes maintenance looparound circuits for the eight speech bits.
NT2X37AB	9F	*Tone circuit card* The tone circuit card contains a digital tone generator and a channel memory. The tone circuit card controls tone insertion and looparound. The tone circuit card generates dial tone, alternative dial tone, audible ring, and multifrequency (MF) signaling.

NT2X31AT parts (Sheet 3 of 3)

PEC	Slot	Description
NT2X38AC	8F	*Signaling circuit card* The signaling circuit card contains circuits that extract the A/B signaling bits from a maximum of five DS-1 data streams. The signaling circuit card receives the signalling bits from the DCM interface (DS-1 line) circuit cards. A filter eliminates the effects of contact bounce and carrier hits. A scanner that a ROM controls monitors the buffers. The scanner reports changes in the received A/B bits. Buffers and timers produce output pulses. Buffers and timers insert A/B bits onto the speech bus. Maintenance circuits and circuits that monitor lines for all DCM interface (DS-1 line) circuit cards are provided.
NT2X70AE	19F, 20F	*Power converter* The NT2X70AE is a dc-to-dc regulated power converter. The NT2X70AE works with a dc voltage of -48V input. The NT2X70AE supplies dc voltages +5, -5, +12, and -12V, with a common ground.

NT2X31AT components



NT2X33AE

Product description

For Series 1 peripherals to function with enhanced network (ENET), an increased message timer limit is necessary. The NT2X33AE introduces a 50-ms message timer limit through a firmware change.

The ENET applications use the NT2X33AE. The NT2X33AE is backward compatible with the NT2X33AB. Older J-Net applications use the NT2X33AB. Except for the timer limit, the NT2X33AE is identical to the NT2X33AB.

Functional description

The NT2X33AE performs the following functions:

- receives CH0 message bytes from both planes of port 0
- transmits CH0 message bytes to both planes of port 0
- supplies clock and frame pulse to the other cards
- provides a reset to the other cards
- receives maintenance information from NT2X32 processor card
- transmits maintenance information to the NT2X32 processor card
- processes message bytes
- checks inter-office synchronization

Functional blocks

NT2X33AE contains the functional blocks that follow:

- clock switch circuit
- 2.56 MHz phase lock loop (PLL)
- clock and frame pulse drivers
- bit and channel counters plus miscellaneous timing
- CH0 messages shifted in
- CH0 messages shifted out
- 8085A microprocessor
- PROM
- RAM
- address decoder
- interrupt register

NT2X33AE (continued)

- peripheral processor (PP) address buffer
- PP bidirectional data buffer
- read/write control
- maintenance register
- T1 slip register

Clock switch circuit

This block selects one good clock and frame pulse from both planes of port 0 for the PLL. A clock switch occurs when four framing errors have occur. If a clock switch occurs, framing errors are not counted for 100 ms. The PLL has time to lock on to the new clock.

2.56-MHz phase lock loop

The 2.56 MHz PLL produces a clean clock. The clock has a 50% duty cycle that is phase locked to the incoming clock. One of the outputs of the PLL is a clock with a frequency of 10.24 MHz. The other cards use this frequency.

Clock and frame pulse drivers

This block distributes a 10.24 MHz clock and 97 ns frame pulse to the other cards. The digital carrier module (DCM) cards share the four sources of clock and frame. Twisted pair distributes clock and frame along the backplane.

Bit and channel counters plus miscellaneous timing

This circuit counts 10 bits and 32 channels. These channel counters are offset one channel from the internal DCM channel names. Channel 0 of the NT2X33 control card refers to channel 1 of the XPCM bus. The bit and channel counters generate signals. Several signals perform miscellaneous timing functions.

CH0 messages shifted in

This circuit takes serial CH0 data from both planes of port 0. This circuit converts the data to a parallel form that the NT2X33AE control processor can read. The processor must not read these registers during channel 0 time.

CH0 messages shifted out

This circuit contains two parallel-to-serial shift registers that the NT2X33AE control processor can write into. The serial data is sent out in channel 0 of port 0 on both planes. The processor must not write to these registers during channel 4 time.

8085A microprocessor

This microprocessor sends and receives messages. This process includes the following:

- send and receive protocol
- check checksum
- count errors
- buffer messages
- perform related functions

The hardware reset for the control processor occurs during channel 31, bits 2 and 6. When the control processor receives a reset message, the control processor can reset the rest of the DCM.

PROM

The 4 Kbytes of PROM contains the firmware required to send and receive messages. Program store uses two Kbytes. The rest is spare.

RAM

The 2-Kbyte RAM contains the receive and transmit message buffers. The RAM has two separate areas. One area stores received messages and control information. The other area stores transmitted messages. The control processor can read or write all the RAM. The NT2X33AE processor can read all the RAM. The NT2X33AE can write only to that area of RAM dedicated to the storage of transmitted messages.

Address decoder

This block generates the read and write enable for all registers and memory.

Interrupt decoder

The control processor writes this register to a one (1). This process interrupts the NT2X33 processor. To clear the interrupt from the NT2X33 processor card, read a given location.

Peripheral processor address buffer

This block buffers the address bus of the NT2X32 processor card on to the NT2X33 control card.

Peripheral processor bidirectional data buffer

This block buffers processor data that comes on to the control card. This block buffers processor data that leaves the control card.

NT2X33AE (continued)

Read/write control

This circuit controls the reading and writing of the RAM buffer from the NT2X32 processor card. When a read or write is necessary, the circuit puts the control to a hold state. This state allows the hardware access to 8085A buses. A read or write holds the control processor for a maximum of two clock cycles.

Maintenance register

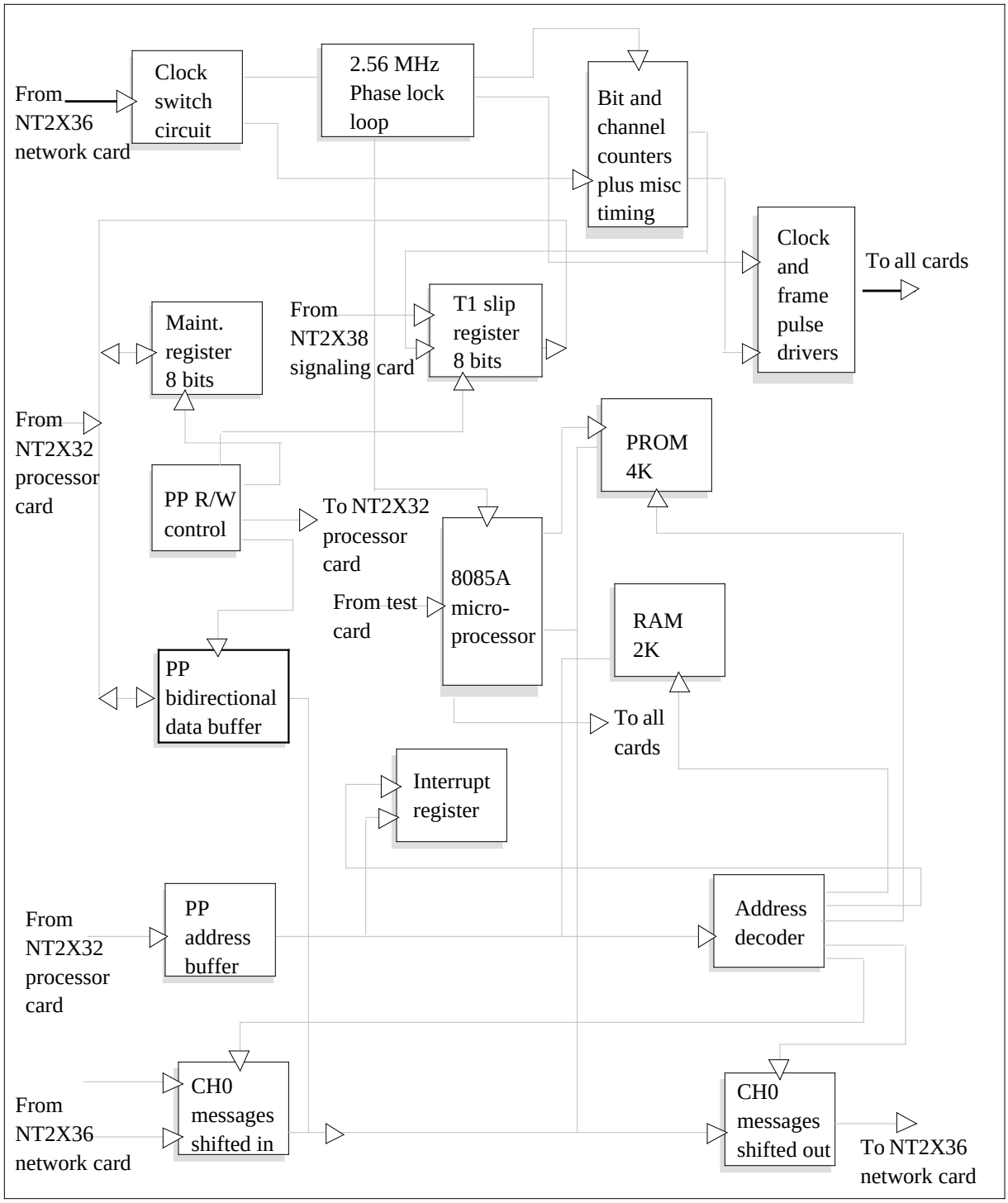
This register is read and written from the NT2X32 processor card. This register sends and receives maintenance information. This circuit contains one receive, and one transmit register. The receive register contains four scan points, two bits for framing errors, and one bit for the plane. The DCM locks to this plane.

T1 slip register

This register allows the software to monitor the inter-office synchronization. This register compares the internal frame pulses of the DCM to the frame pulses derived from a T1 link to a DCM. The DCM connects to another network. The slip between these signals latches into the register.

The relationship between the functional blocks appears in the following figure.

NT2X33AE functional blocks

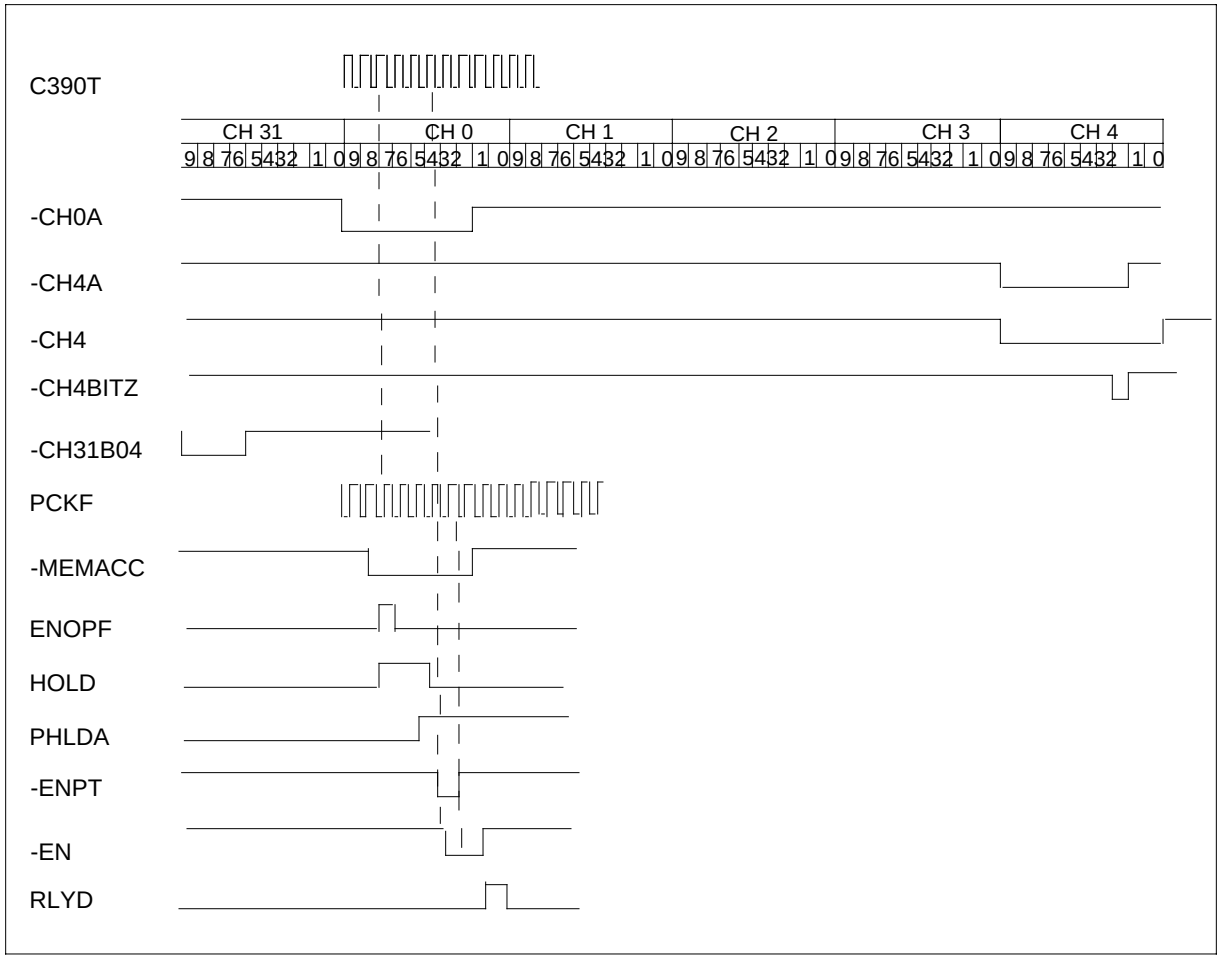


NT2X33AE (continued)

Timing

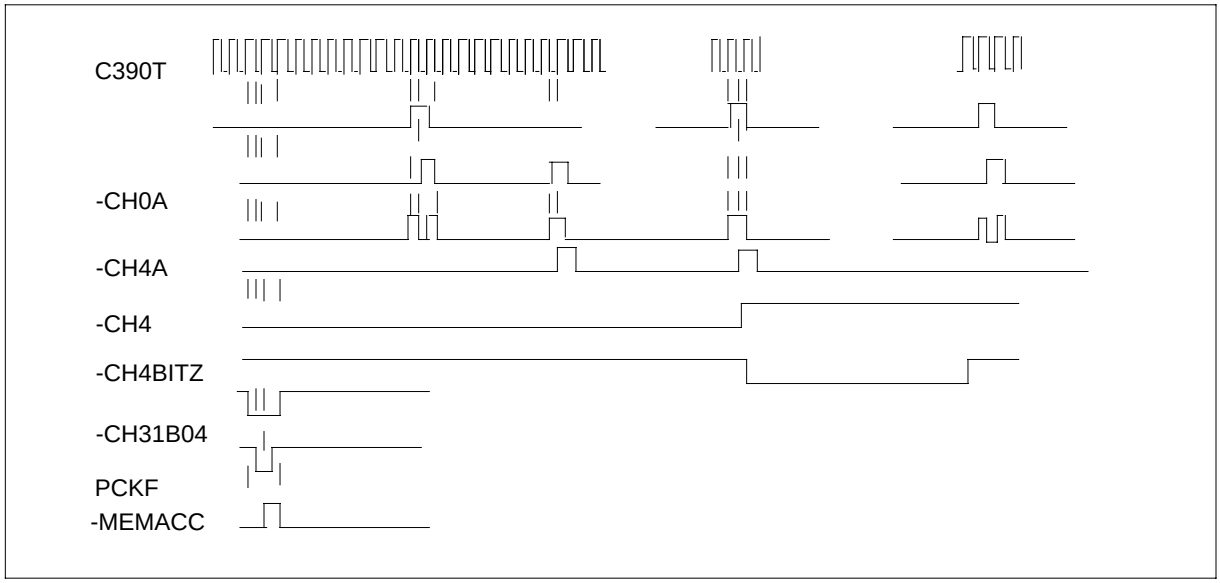
The timing required to send and receive CH0 message bytes appears in the following figure. The timing the NT2X32 processor card requires to read or write memory on the NT2X33 control card appears in the following figure.

NT2X33AE timing



The timing required for the clock switch circuit appears in the following figure.

NT2X33AE clock switch circuit timing



NT2X35AB

Product description

The NT2X35AB digital carrier module (DCM) interface card provides a two-way, digital, voice, and signaling interface between selected channels. The channels are four 32-channel bit streams of the DCM in a DMS-100 and one DS-1, 24-channel, bipolar bit stream.

Location

The card plugs in one of five assigned slots in the DCM shelf.

Functional description

The NT2X35AB uses receive pulse code modulation (RPCM) circuitry in the receive direction. This RPCM converts transistor-transistor logic (TTL) signals to bipolar signals for transmission to the DS-1 equipment. The card receives bipolar signals from the DS-1 equipment in the transmit direction. The card uses transmit PCM (XPCM) circuits. These circuits converts the bipolar signal to TTL signals for transmission to the speech bus of the DCM. Maintenance circuits in the card monitors the performance of the card.

Operating blocks

The RPCM circuit consists of the following functional blocks:

- RPCM select circuit
- insert local alarm circuit
- zero code suppression
- 16-bit elastic store
- multiplexer (MUX)
- looparound multiplexer (LA MUX)
- write counter
- frame pulse retiming circuit
- read counter
- TTL-to-bipolar converter
- attenuator and equalizer
- looparound retiming circuit
- maintenance register
- toggle circuit

RPCM select circuit

The RPCM select circuit selects one of four 8-bit RPCM data streams from the DCM speech bus. Under control of enable signals, the RPCM connects the stream to the 16-bit elastic store. The circuit selects a total of 24-PCM words.

Insert local alarm circuit

The insert local alarm circuit enables the DCM to insert a local alarm if an alarm occurs on a specified channel.

Zero code suppression

The zero code suppression prevents the bipolar signal from assuming a zero value. The code monitors the PCM bit stream for an 8-bit word that contains all logic high values. The code changes the next least significant bit to a logic low.

16-bit elastic store

The 16-bit elastic store receives the 24 selected 8-bit PCM words and holds the data for a period of one-channel time. The store sends the data to the MUX. Store the PCM data according to addresses that the write counter selects.

MUX

The MUX inserts DS-1 framing patterns in the RPCM. The frame pulse retiming circuit controls this action.

LA MUX

There are two LA MUXs. One is in the RPCM circuitry and the other is in the XPCM circuitry. The two LA MUXs allow a test of all components in the RPCM and XPCM transmit paths. The LA MUXs disconnect PCM data from the TTL-to-bipolar converter in the RPCM circuitry. The LA MUXs connect the data to the bipolar-to-TTL converter in the XPCM circuitry.

Write counter

The write counter receives enable signals from the DCM. The counter determines the write address for the PCM data in the 16-bit elastic store.

Frame pulse retiming circuit

The frame pulse retiming circuit controls the DS-1 framing patterns that the MUX inserts. This circuit retimes the circuit to a 1.544 MHz rate. The circuit outputs a clock signal used to control the read counter.

Read counter

The read counter reads the PCM data out of the 16-bit elastic store at a 1.544-MHz rate. The transmit clock in the frame pulse retiming circuit controls the counter.

NT2X35AB (continued)

TTL-to-bipolar converter

The TTL-to-bipolar converter receives the TTL signal from the DCM. The converter converts the signal to a bipolar signal for transmission to the DS-1 equipment.

Attenuator and equalizer

The attenuator and equalizer compensates for the effect of cable lengths on data transmission to the DS-1 equipment. Seven small switches enable adjustment for three ranges of cable lengths.

The following table lists the small switch settings for the different cable lengths.

Equalizer switch settings

	Switch settings						
Distance	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0-46 m (0-150 ft)	ON	OFF	OFF	OFF	OFF	OFF	OFF
47-137 m (151-450 ft)	ON	OFF	ON	ON	ON	OFF	OFF
138-229 m (451-750 ft)	OFF	ON	OFF	OFF	OFF	ON	ON

Looparound retiming circuit

The looparound retiming circuit retimes the loop signal from the DCM maintenance bus to 1.544 MHz.

Maintenance register

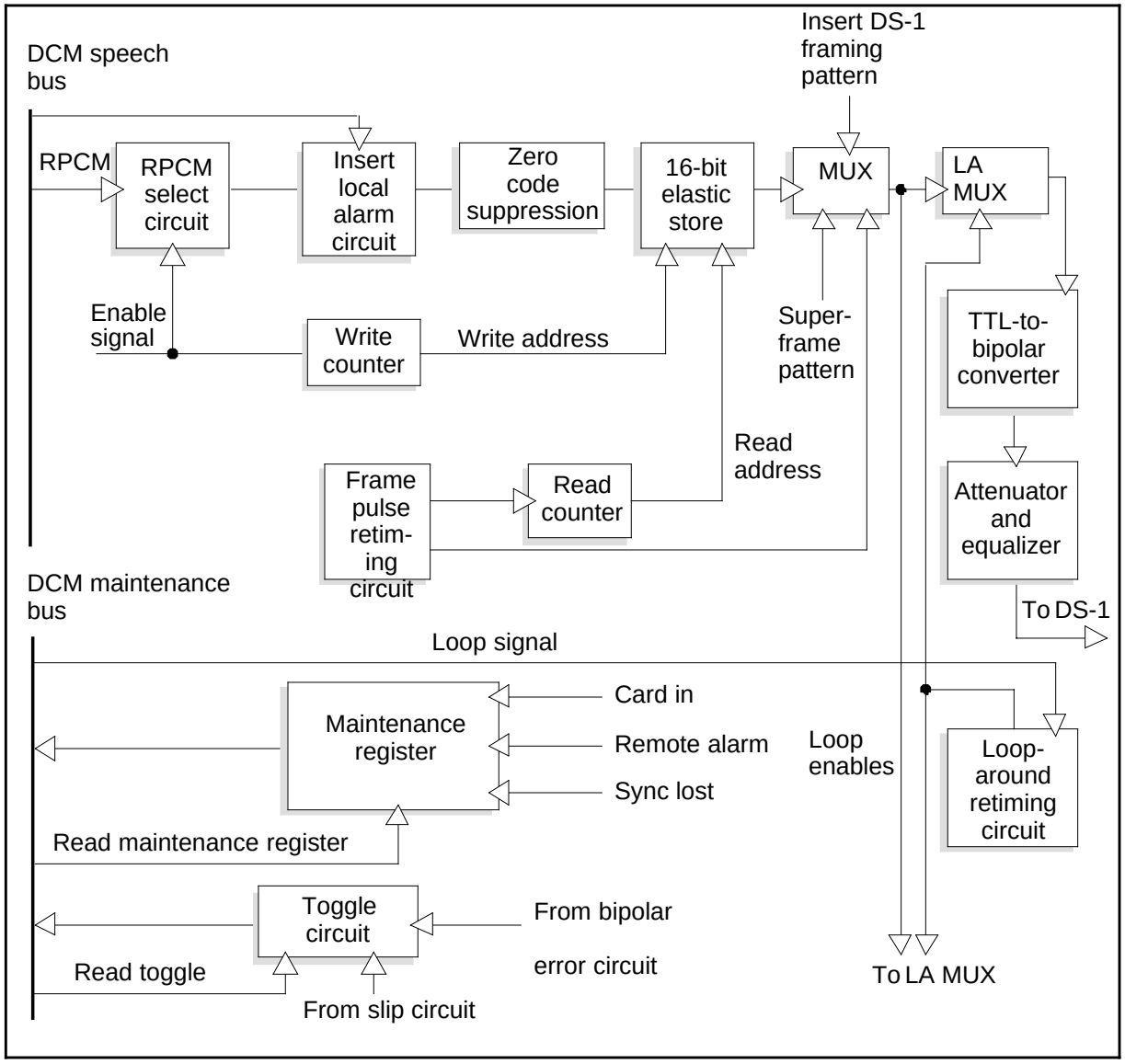
The maintenance register records card-in, remote-alarm, and synchronization-lost signals. The DCM sends a read-maintenance-register signal. The maintenance register responds. The maintenance register informs the DCM if the five assigned slots contain DS-1 line cards.

Toggle circuit

The toggle circuit stores bipolar violation, detector, and slip circuit information. When the DCM sends a read-toggle signal, the toggle circuit informs the DMC if these events have occurred.

The relationship between the functional blocks appears in the following figure.

NT2X35AB RPCM functional blocks



The XPCM circuit contains the following functional blocks:

- remote alarm detector
- bipolar violation detector
- bipolar-to-TTL converter
- two-frame elastic store
- read/write control circuit
- synchronization (sync) circuit

NT2X35AB (continued)

- XPCM latch circuit
- XPCM retiming circuit
- LA MUX
- received clock synchronization circuit
- DS-1 bit/channel two-frame counter
- signaling/frame decoder (sig)
- read/write MUX
- slip circuit
- two-frame counter
- DMS bit/channel counter
- hold DMS channel counter
- XPCM distribution circuit
- buffer

Remote alarm detector

The remote alarm detector monitors the synchronization of the card. If an out-of-synchronization state persists, the detector sends an error signal to the maintenance register.

Bipolar violation detector

The bipolar violation detector monitors the conversion of the bipolar signal to a TTL signal. The detector generates a bipolar error signal if an abnormal bipolar pattern occurs.

Bipolar-to-TTL converter

The bipolar-to-TTL converter receives the bipolar DS-1 signal and converts the signal to a PCM bit stream TTL signal.

Two-frame elastic store

The two-frame elastic store receives and transmits XPCM data between the DS-1 equipment and the DCM speech bus. Data is written into the circuit at a different rate than data is read out of the circuit. The difference in frequency between the DS-1 and DMS clocks determines this action.

Read/write control circuit

The read/write control circuit controls the read and write activity. The circuit uses one half of the clock signal that the synchronization circuit sends. The circuit uses the signal to read XPCM data out of the two-frame elastic store.

The circuit uses one half of the signal to write XPCM data into the two-frame elastic store.

Synchronization circuit

The synchronization circuit sends a clock signal to the read/write control circuit to time the read and write activity. The circuit checks for timing pattern synchronization. The circuit sends an out-of-synchronization signal to the maintenance register if the timing patterns are not synchronized.

XPCM latch circuit

The XPCM latch circuit receives XPCM data from the LA MUX and sends the data to the XPCM retiming circuit.

XPCM retiming circuit

The XPCM retiming circuit is controlled by the received clock synchronization circuit. The circuit retimes the XPCM data for transmission to the two-frame elastic store.

Received clock synchronization circuit

The received clock synchronization circuit samples the DS-1 bit stream to extract a clock signal. This signal synchronizes the data with the DMS clock. The circuit controls the flow of PCM data through the XPCM latch and XPCM retiming circuits.

DS-1 bit/channel two-frame counter

The DS-1 bit/channel two-frame counter assigns the write address of XPCM data read into the two-frame elastic store.

Signaling/frame decoder

The signaling/frame decoder circuit decodes the signaling and framing data. The circuit identifies the XPCM signaling frames based on the modulated frame pulse bit.

Read/write MUX

The read/write MUX receives the address assignment from the DS-1 bit/channel two-frame counter. The MUX selects the DMS counters for PCM data that enters the two-frame elastic store.

Slip circuit

The slip circuit compares the DS-1 counter addresses with the DMS counter addresses. The addresses may be in two channels. The read addresses change to the addresses in the second frame of the two-frame elastic store. The circuit also generates a slip signal that is sent to the toggle circuit.

NT2X35AB (continued)

Two-frame counter

The two-frame counter receives signals from the DMS bit/channel counter. The counter counts the frames for the slip circuit to change the read address of the two-frame elastic store.

DMS bit/channel counter

The DMS bit/channel counter receives signals from the hold DMS channel counter. The DMS bit/channel sends signals to the two-frame counter. The channel also sends signals to the read/write MUX to control the input of data bits into the DMS channels.

Hold DMS channel counter

The hold DMS channel counter uses transmit enable signals to control the DMS channel counters.

XPCM distribution circuit

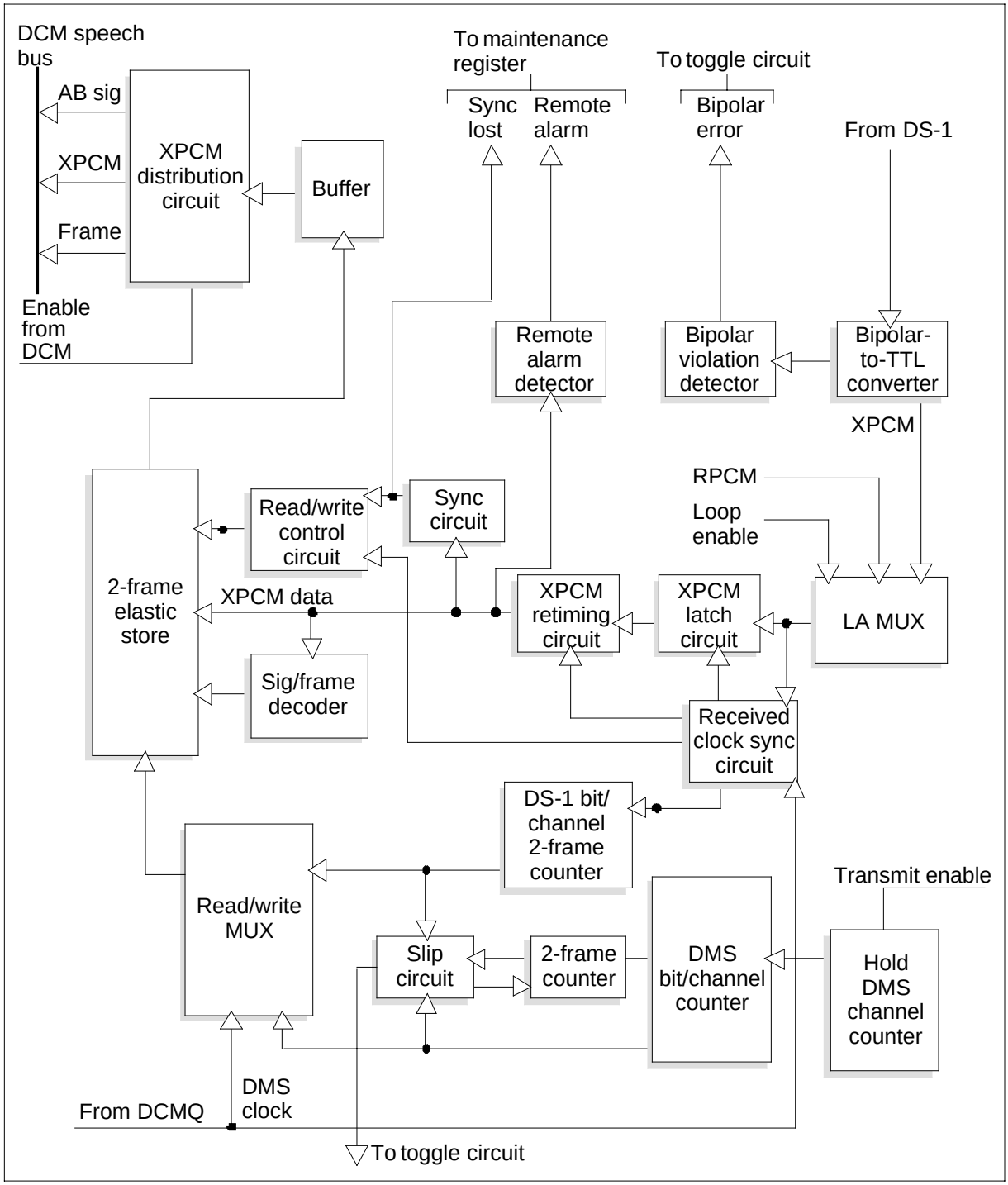
The XPCM distribution circuit receives the XPCM data from the buffer. Under control of enable signals, the circuit sends the data to one of four XPCM data streams on the DMS speech bus.

Buffer

The buffer receives XPCM data from the two-frame elastic store and sends the data to the XPCM distribution circuit.

The relationship between the functional blocks appears in the following figure.

NT2X35AB XPCM operating blocks



NT2X35AB (continued)

Technical data

The DMS-100 network interface characteristics appears the following table.

Network interface characteristics

Characteristic	Value
Rate	2.56 Mbps
Structure	32 10-bit channels per frame
Data format	Bits numbered 9 to 0, bit 9 transmitted first
Channels	Channels numbered 0 to 31, channel 0 transmitted first
Ports	Ports numbered 0 to 3, plane 0 and plane 1
Frame	Frame bit 0, channel 0
Signaling	Message channel—port 0, channel 0, bits 9 to 2, bit 9 is most important, bit 1 is not used
Code	Biphase with frame pulse problem once per frame
Receiver sensitivity	0.25 V peak to peak
Driver output	2.00 V peak to peak
Rise time	50 ns minimum
Line impedance	100 Ω
Transformer interwinding isolation	500 V dc minimum

The DS-1 carrier interface characteristics appear in the following table.

DS-1 carrier interface characteristics (Sheet 1 of 2)

Characteristic	Value
Input rate	1.544 Mbps ±200 bps
Output rate	1.544 Mbps, phase locked to office clock

DS-1 carrier interface characteristics (Sheet 2 of 2)

Characteristic	Value
Structure	24 channels per frame, 8 bits per channel
Data format	Bits numbered 1 to 8, bit 1 transmitted first
Idle code	0 1 1 1 1 1 1 1 (bit 1 = 0)
Channels	Channels numbered 1 to 24, channel 1 transmitted first
Ports	Ports numbered 0, 1, 2, 3, 4
Frame	193 bits per frame
Signaling (DCM-B, DCM-S)	A- and B-bits
Signaling (DCM-R)	Port 0, channel 1; port 1, channel 1
Code	Bipolar
DS-1 receiver input signal	±1.5V to ±3.0V
DS-1 transmitter	±6 ±0.6V output pulse height ±0.3V positive-negative unbalance 324 ±30 ns half-amplitude width ±15 ns unbalance in width of positive-negative pulse 80 ns rise and fall time 20 to 40% overshoot at trailing edge Average minimum density, a minimum of 1 pulse in 8, a maximum of 15 consecutive zeros
Line impedance	100 Ω balanced
Transformer interwinding isolation	500V dc minimum

Physical dimensions

The physical dimensions for the NT2X35AB are as follows:

- height: 353 mm (13.9 in.)
- depth: 279 mm (11.0 in.)
- width: 28 mm (1.125 in.)

NT2X35AB (end)

Power requirements

The power requirements for the NT2X35AB appear in the following table.

Power requirements

Voltage	Current	Dissipation
+5 V	2.0A	10W
+12V	0.1A	1W

NT2X43

Product description

The DMS-Family office uses two office alarm circuit 3 cards. These cards provide control circuits, duplicated ±130V and 20 Hz supplies. The cards provide -48V distribution to audible and visual alarms for the DMS-100 Family alarm system. The cards provide transformers for the local talk line circuit and -48V distribution to data link control cards of the data loop system.

The primary features of the NT2X43 are as follows:

- Each card provides the control relays for the following functions:
  - — office alarm unit alarm
  - — dead system alarm
  - — dead system audible alarm reset
  - — transfer to alternate ±130V and 20-Hz (ac) supplies in case of supply failure
  - — cut-off of -48V distribution if the card is in the wrong card position
- Each card provides the following:
  - — a ±20Hz (ac) ringing generator (RG)
  - — a transformer to the local talk line circuit
  - — -48V distribution to associated hardware
- The alarm system software controls some card functions through signal distribution (SD) cards. The SD cards are in the office alarm unit (OAU) and maintenance trunk module (MTM) shelves.
- The alarm system monitors some card functions software through scan detector cards in the OAU and MTM shelves.

Location

One of the two office alarm circuit 3 cards is in the OAU. The other circuit card is in an associated MTM. Each card occupies two card positions. The office alarm circuit 3 cards appear in the following figures.

Functional description

The system generates an OAU alarm when a fault causes the release of the normally-operated relay AB. The relay AB is in the office alarm circuit 3 card. The office alarm circuit 3 card is in the OAU or MTM. The OAU and MTM monitor the alarm circuits of the respective circuits of the other unit through scan points. The release of relay AB in the OAU causes a make contact to open. The make contact removes ground from scan point ABOAUFL in the MTM. The release of relay AB in the MTM removes ground from scan point

NT2X43 (continued)

ABMTMFL in the OAU. The alarm system software initiates the corresponding audible and visual alarms when these scan points change state.

One of the following conditions causes the system to generate the OAU alarm:

- Loss of -48V office battery supply to the OAU or MTM shelf.
- A blown F1 fuse on the office alarm circuit 3 card. This failure removes battery from relay AB.
- The normally-operated relay 130 releases when the following occurs:
  - — failure of the ±130V converter
  - — a blown F2 fuse or F3 fuse on the office alarm circuit 3 card

This failure opens a make contact in the ground path of relay AB.

- Failure of the 20-Hz (ac) RG on the office alarm circuit 3 card causes normally-operated relay ac to release. This failure opens a make contact in the ground path of relay AB.
- A communication loss between the central control (CC) and the OAU and MTM shelf. This loss of communication releases SD point OAUFAIL in the OAU or MTMFAIL in the MTM. The communication loss removes ground from the corresponding AB relay.

Dead system alarm

The alarm system hardware generates the dead system alarm to indicate a loss of call-processing ability in the DMS office. The system generates this alarm when a double fault causes the release of the normally-operated relay DS. The release of the relay DS occurs in the office alarm circuit 3 card of the OAU and the MTM.

The DS relays in the OAU and the MTM have two ground connections. One connection point is at SD point OAUFAIL and another connection is at SD point MTMFAIL. A loss of communication with the CC in the OAU or MTM can release the OAUFAIL or MTMFAIL SD point. When this event occurs, the alternate SD point continues to ground the DS relays. A loss of sanity in the CC software causes a loss of communication between the CC and the OAU and MTM. The loss of CC software sanity releases both DS relays. Multiple defects in the DMS Family message system cause a loss of communication between the CC and the OAU and MTM.

A ground connection connects to the critical system lamp on the alarm control and display panel (ACD). The critical bell connects to the ground connection through break contacts of both DS relays. The system generates an audible and visual critical system alarm generates when both DS relays are released.

A -48V power failure that occurs in the OAU or MTM causes the system to generate a dead system alarm. The alarm generation occurs while the OAU or MTM is out of communication with the CC. A power failure in the OAU causes the system to generate the visual alarm (critical system lamp). A power failure in the MTM causes the system to generate the audible alarm (critical bell).

Remote dead system indication

When the dead system condition occurs and the office is empty, the system provides a facility. The facility transfers the alarm to a remote monitoring location. The remote alarm transfer must be in effect.

Audible alarm reset

The operation of the audible alarm reset switch on the ACD places a ground on scan points AUDARO and AUDARM. This action occurs when the system functions normally. The scan points are in the OAU and MTM. The alarm system software detects the change of state in these scan points and silences any current audible alarm. A copy of these scan points allows the audible alarm to be silent if the OAU or MTM is out of service (OOS).

When a dead system alarm occurs, the software can not silence the audible alarm. A hardware facility silences the critical alarm bell in this event. The release of relay DS in the OAU and MTM closes break contacts. The break contacts connect the audible alarm reset switch to the winding of relay AR in the OAU and the MTM. The ground that operates relay K1 is available when the card is in the correct card position.

±130V and 20-Hz (ac) supply transfer

In each office alarm circuit 3 card, the ±130V converter provides ±130V and -130V signaling voltages for the remote alarm transfer circuit. This circuit is in the office alarm circuit 2 card (NT2X42).

The 20-Hz (ac) RG provides 20-Hz (ac) superimposed on -48V (dc) to operate the following:

- alarm battery subset
- minor alarm subset
- trunk test center (TTC) chime

The supplies from the office alarm circuit 3 card in the OAU or MTM connect to the alarm system. The supplies connect to the alarm system through make contacts of SD point-controlled PT relays.

NT2X43 (continued)

The supplies in the OAU normally connect with the alarm system. The PT relay in the OAU is operated through SD point OAUPWR. The PT relay in the MTM is released. If the supplies in the OAU fail, the alarm relay AB is released and scan point ABOAUFL in the MTM detects the alarm condition. Before the system generates the OAU alarm, the alarm system software transfers to the alternate supplies in the MTM. The alarm system releases SD point OAUPWR. The alarm system releases the SD point in the OAU and operates SD point MTMPWR in the MTM transfers the supplies. The correction of the fault in the OAU operates relay AB again. The alarm system software transfers back to the OAU supplies. This action releases SD point MTMPWR and operating SD point OAUPWR. If one of the MT supplies fail while the OAU supplies are OOS, the software transfers back to the OAU supplies. The corresponding audible alarms or remote alarms, or both, become OOS. A loss of communication with the CC causes the release of relay AB in the OAU. When this event occurs, the alarm system software cannot release SD point OAUPWR before the transfer of supplies. Both supplies must not connect. Release of relay AB occurs to guarantee the release of relay PT. This action causes a make contact of relay AB in the ground path relay PT opens.

-48V distribution

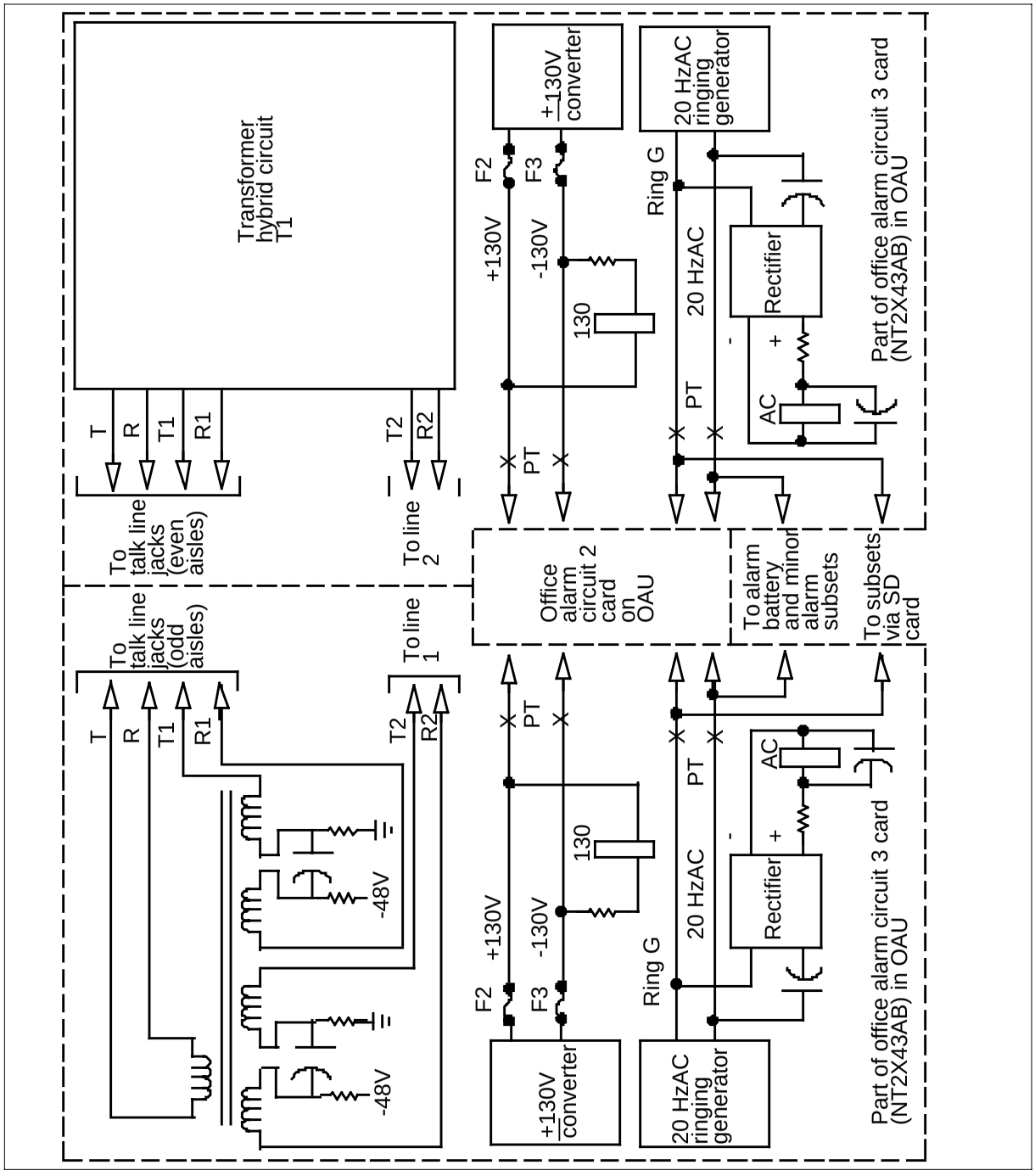
The office alarm circuit 3 card in the OAU distributes -48V through the F1 fuse. The office alarm circuit 3 card also distributes -48V through a make contact of normally-operated relay K1. The circuit card distributes power to the critical bell and main tone bar of the alarm system. The data link control cards (NT0X89) of the data loop system also receive power from the circuit card. The office alarm circuit 3 card in the MTM distributes -48V to lamps on the alarm control. The circuit card also distributes power to display panels and the DMS exit alarm panels. Relay K1 provides a safety device that cuts off -48V distribution on each card. The device cuts distribution of power if the card is in the wrong card position in the OAU and MTM. The ground that operates relay K1 is available when the card is in the correct card position.

Local talk line transformers

The local talk lines are two office telephone lines. The office lines terminate on the Logic telephone set at the MAP terminal in the DMS-100 Family office. Each office alarm circuit 3 card contains a transformer hybrid circuit (T1). The T1 divides one of the two local talk lines into a separate transmit and receive path. The T1 divides the lines before the lines are multiplied to talk line jacks. The talk line jacks are in all even or odd aisles in the office.

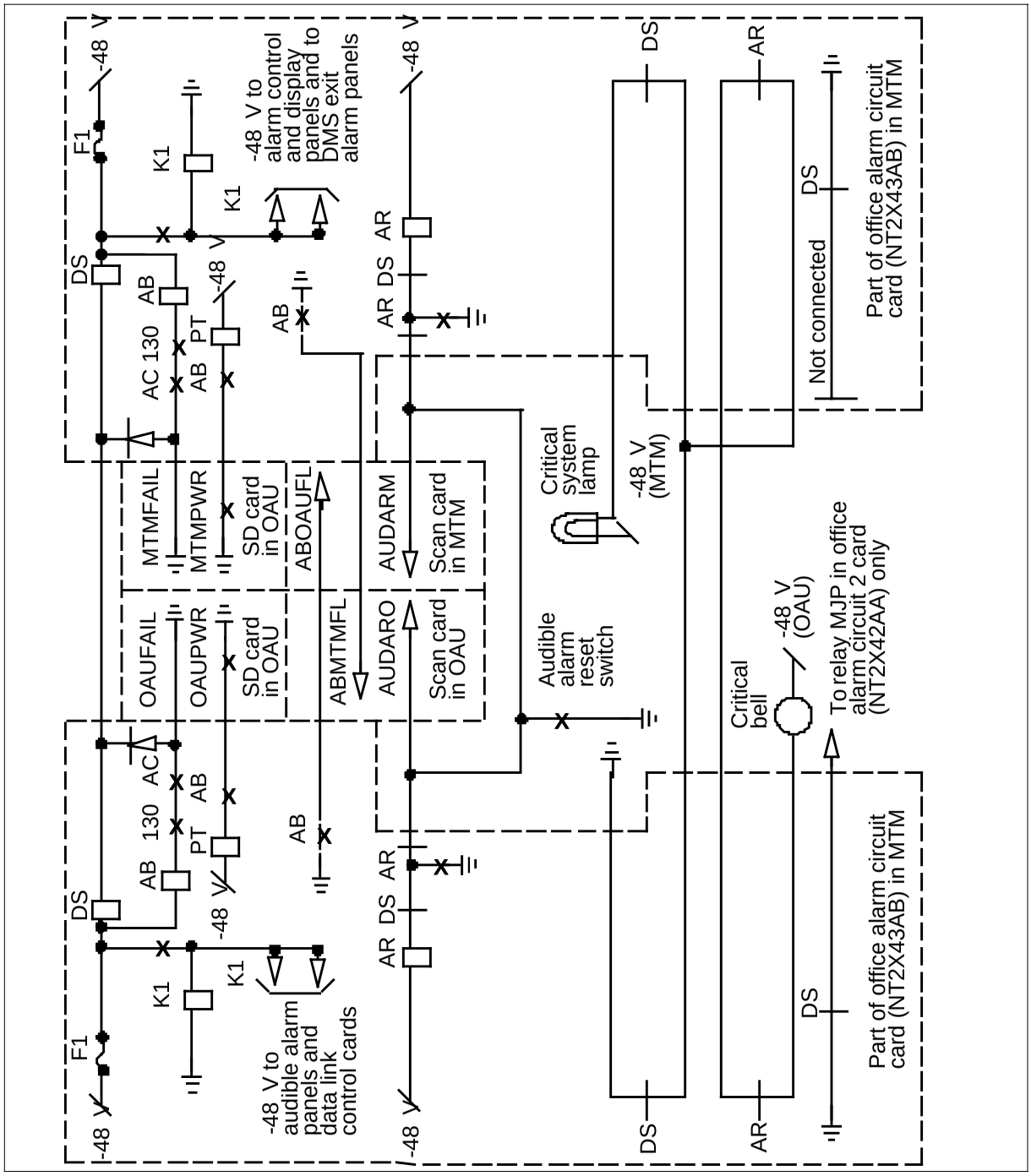
The relationship between the operating blocks for the NT2X43 appears in the following figure.

NT2X43 functional blocks for part of office alarm circuit 3 card (OAU and MTM)



NT2X43 (continued)

NT2X43 functional blocks for part of office alarm circuit 3 card (OAU and MTM)



Technical data

The technical data section provides specifications for the NT5X92 power requirements, equipment dimensions and environmental conditions.

Power requirements

The power requirements appear in the following table.

Power requirements

Nominal voltage	-52 V
Current drain	250 mA

Equipment dimensions

The NT2X43 dimensions are 317.5 mm (12.5 in.) in height and 254 mm (10 in.) in depth.

Environmental conditions

The NT2X43 performs under limited environmental restrictions, as the following table describes.

Ambient conditions

Condition	Operating range	Short-term range
Temperature	10 °C to 30 °C (50 °F to 86 °F)	5 °C to 49 °C (41 °F to 120.2 °F)
Relative humidity	20% to 55%	20% to 80%

Note: Expect a relative humidity of 80%, at a maximum ambient temperature of 21°C (69.8°F). At an ambient temperature of 49°C (120.2°F), expect the maximum relative humidity to be 30%.

NT2X45AB

Product description

The NT2X45AB trunk module interface card conforms to DMS common features. Some functions of the NT2X45AB are implemented on thick-film hybrids.

Functional description

The NT2X45AB handles communication between the analog transmission and signaling trunk facilities and the digital multiplex circuits in the trunk module. The number and type of cards selected must match the type of trunk facilities. Some cards have two trunk interface circuits. Other cards have one trunk interface circuit. Limits determine the number of trunk interface circuits.

Functional blocks

The NT2X45AB consists of the following operating blocks:

- timing and control circuits
- network data receiver
- trunk interface
- coder-decoder (CODEC) interface
- network data transmitter

Timing and control circuits

The timing and control functions are as follows:

- distribution of clock and frame pulse to the related cards
- bit and channel timing
- data bus buffering

Network data receiver

The network data receiver functions are as follows:

- dual ac transmission interface
- biphase decoder
- clock and frame selection
- clock stability created by phase-locked loop
- channel alignment
- network B-message removal

Trunk interface

The trunk interface functions are as follows:

- channel R-data selection between plane 0 or 1
- trunk R-message insertion
- channel R-parity bit check
- channel R-integrity bit removal
- trunk R-data selection
- data selection for the trunk bypass register
- channel X-integrity bit insertion
- trunk parity check

Coder-decoder interface

The CODEC interface functions are as follows:

- generation of control signals for the CODEC card
- digital pad multiplication of analog data bytes

Network transmitter

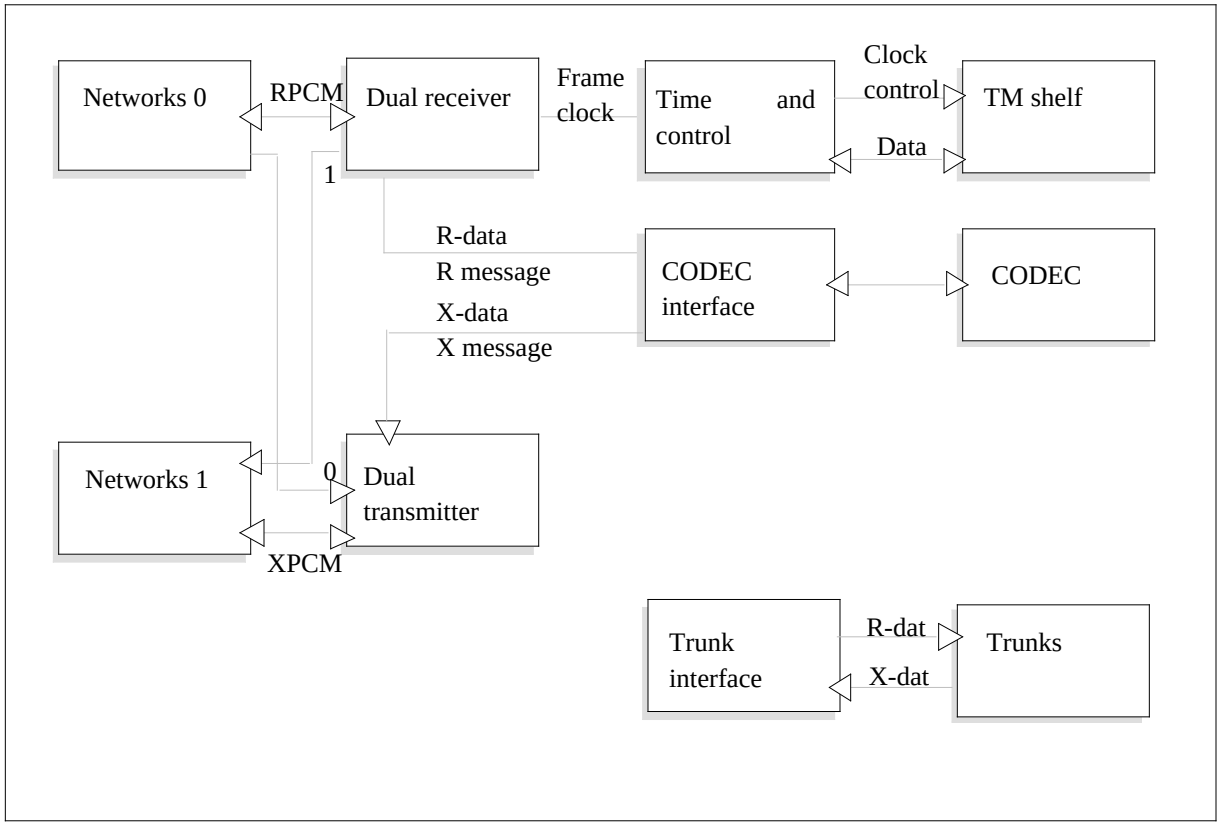
The network transmitter functions are as follows:

- trunk X-message removal
- network X-data selection
- network X-message insertion
- X-parity bit generation and insertion
- frame pulse insertion
- biphase encoding
- dual ac transmission

The basic components and connections of the NT2X45AB appear in the following figure.

NT2X45AB (continued)

NT2X45AB operating blocks



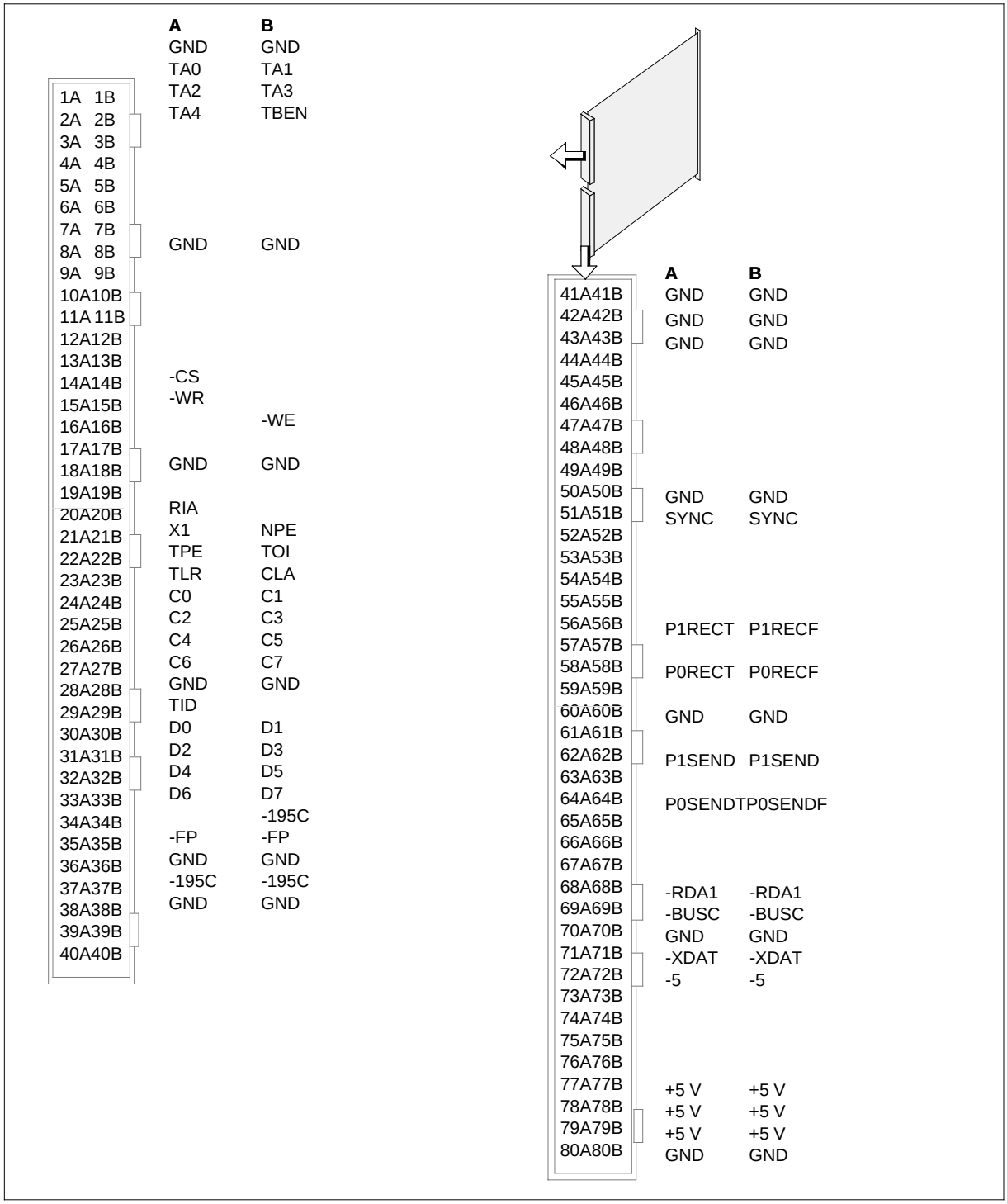
Signaling

Pin-outs

The NT2X45AB pin-outs appear in the following figure.

NT2X45AB (continued)

NT2X45AB pin-outs



NT2X45AB (end)

Technical data

Power requirements

The NT2X45AB converts -48V input to 5V output.

NT2X46

Product description

The metallic test access (MTA) unit is a modified Minibar switch used to provide metal dc connections. The metal dc connections are between test circuits and the line circuits in line modules (LM) or remote line modules (RLM). The MTA unit works with the Minibar driver card (NT2X50) as part of the line maintenance facility for DMS-100 and DMS-100/200.

Location

The NT2X46 is frame-mounted. Normally the NT2X46 is on a miscellaneous (MIS) equipment frame or a remote service equipment (RSE) frame.

Functional description

The arrangement of the MTA allows access for a maximum of ten LM or RLM bays or 16 test circuits. The MTA has a two-wire switched path. The test circuits connect to the MTA appearances at the main distribution frame (MDF). The LM or RLM and the Minibar driver connect to the MTA.

Matrix

The MTA is a Minibar arranged to provide a 16 x 20 two-wire switching matrix. The group of more than one MTA results in a larger matrix.

LM/RLM appearances

The MTA has 20 two-wire appearances on the vertical side of the matrix. Each LM has two test access buses. One MTA can serve a maximum of ten LM or RLM bays.

Test circuit appearances

The MTA has 16 two-wire appearances on the horizontal levels 0 to 7. Each two-wire appearances create two appearances. Levels 8 and 9 control the selection of the required appearances on a set horizontal level. Levels 8 and 9 are steering levels. When more than 16 test appearances are necessary, the number of MTA used increases. The Matrix expansion part of the Functional description section in this hardware description describes this increase.

Matrix operation

The Minibar driver card controls the MTA unit. The Minibar driver card unit supplies the ground potential to operate the desired select and hold magnets.

The operation of two select magnets (SM) and on hold magnet (HM) and the release of the HM establishes a matrix connection. The matrix connection continues until the release of the HM.

NT2X46 (continued)

For example, to establish a connection between test circuit appearance #14 and LR or RLM appearance #00 perform the following in order:

1. operate SM9 and SM7
2. operate HM00
3. release SM9 and SM7

A maximum of 16 matrix connections can be present at the same time. This restriction applies if only one test circuit can connect to one LM or RLM appearance at one time.

MTA path monitor

When a path is made from an LM or RLM to a test circuit, the Minibar driver receives an indication. The indication tells the Minibar that a set of crosspoints has operated. This indication is a pulse of -48V volt potential. The pulse travels from a point on the vertical side of the matrix through a steering magnet crosspoint (8 or 9). The pulse travels through a select magnet crosspoint (0 to 7) and through a set of select off normal (SDN) contacts. This pulse is present during the creation of a path. The pulse is not present when system maintains the path through the matrix.

Matrix expansion

One MTA connects to a maximum of ten LM or RLM bays. When an office or site contains more than ten LMs or five RLMs, more MTA units are necessary. Connectors C11 and C12 multiply test circuit appearances 2 to 15 to all MTAs. The multiplication of the test circuits provides most test circuits access to all LMs. Test circuit appearances zero and one are not multiplied to other MTAs. These test circuit appearances connect to test circuits dedicated to a maximum of 10 LM or RLM bays.

One MTA connects to a maximum of 16 test circuits. When more than 16 test circuits are necessary, the number of MTA increases.

For example, the matrix in a 32 000 line office can consist of the following:

- 5 MTA units if 16 test circuit appearances are sufficient
- 10 MTA units if 17 to 32 test circuit appearances are required
- 15 MTA units if 33 to 48 test circuit appearances are are required

External connections

All connections to the MTA are through 16 34-pin connectors. The uses of connectors C1 to C15 appear in the following table.

External connections

Heading	Purpose
C00	The C00 connector connects one lead from each HM (20 leads). The C00 connector also connects one lead from each SM (10 leads), and a test lead to the Minibar driver.
C01 to C10	The C01 to C10 connectors connect the 20 LM or RLM appearances (00-19) to 20 LM or RLM test access buses. Each connector contains four leads that connect to each LM or RLM bay. These four leads are the tip (T) and ring (R) from two MTA appearances to the two test access buses.
C11	The C11 connector connects 14 test circuit appearances (2-15) to the MDF. These circuit appearances will be jumpered to test circuits or connect the 14 test circuit appearances 2-15 with another MTA.
C12	The C12 connector has each pin multiplied to the pins of connector C11. The C12 connects the 14 test appearances (2-15) of 2 MTAs when required.
C13 to C14	The C13 to C14 connectors connect the LM or RLM appearances to another MTA. The connectors connect the appearances when more than 16 test circuit appearances are necessary in an office. Connector C13 contains the T and R from LM or RLM appearances10-19.
C15	The C15 connector connects 2 MTA test appearances (0 and 1) to the MDF. These 2 test appearances have access only to the LM or RLM connected to one MTA.

Functional blocks

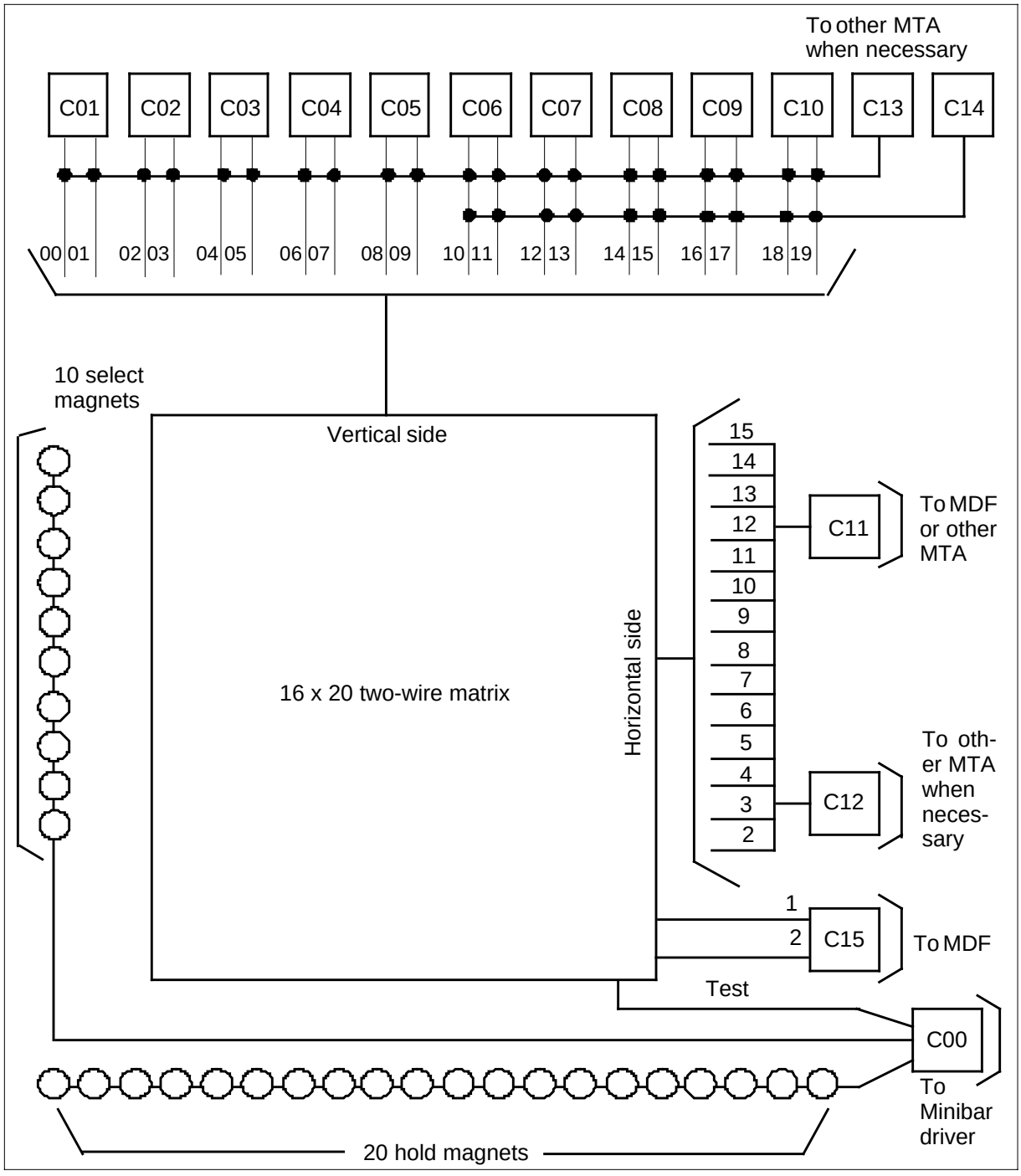
The NT2X46 has the following operating blocks:

- MDF
- LM or RLM
- Minibar driver located in a maintenance trunk module (MTM) or a remote service module (RSM)

The relationship with the functional blocks appears in the following figure.

NT2X46 (continued)

NT2X46 functional blocks



Technical data

This section provides technical specifications for the . The technical specifications include power requirements, environmental conditions and equipment dimensions.

Power requirements

The nominal input voltage is -48V. The minimum input voltage is -42.75V. The maximum input voltage is -55.8V. Other NT2X46 power requirements appear in the following table.

Power requirements

	Maximum	Normal	Idle
Current	0.823A	0.190A	0.0A
Power	39.5W	9.0W	0.0W

Environmental conditions

The NT2X46 performs under limited environmental restrictions, as the following table describes.

Ambient condition

Condition	Operating range	Short-term range
Temperature	10 °C to 30 °C (50 °F to 86 °F)	5 °C to 49 °C (41 °F to 120.2 °F)
Relative humidity	20% to 55%	20% to 80%

Note: Expect a relative humidity of 80% at a maximum ambient temperature of 21°C (69.8°F). At an ambient temperature of 49°C (120.2°F), the relative humidity can be a maximum of 30%.

Equipment dimensions

The NT2X46 dimensions are 152.4 mm (6 in.) in height, 279.4 mm (11 in.) in depth, and 13.69 kg (30 lb) in weight.

Note: If the unit is not mounted below another unit, leave a minimum of 76.2 mm (3 in.) above the unit. This space allows the cable connection panel to pivot.

NT2X47AA

Product description

The transmission test unit (TTU) contains the NT2X47AA transmission test module control signal generator card. The TTU also contains the NT2X56AA digital filter (DF) card. The TTU is a digital signal processor. You can program the TTU to permit transmission measurements and performance of maintenance functions. The card controls the testing procedures and generates tones that the tests require. The combination of the and the NT2X56AA allows the performance of automatic transmission measuring equipment-2 (ATME2). The ATME2 tests for a 104 test line.

Location

The NT2X47AA occupies one card position in the maintenance trunk module (MTM) shelf. The card must be in the slot next to the digital filter card.

Functional description

The NT2X47AA contains two main processors. The processors are the master processor (MP) and the signal processor (SP). The card receives instructions from the central control (CC) to perform a test. When this event occurs, the MP controls the generation, reception, and timing of the tones specified in the test. After the test is complete, the MP transmits the test results to the CC. The SP generates the tones that the TTU tests require. The SP generates the correct tone waveform and supplies the tone at the correct level for the test.

Functional blocks

The NT2X47AA consists of the following operating blocks:

- MP/MTM interface
- MP
- MP memory
- DF interface
- direct memory access (DMA) controller
- master/signal interface
- pulse code modulation (PCM) signal generator
- PCM output interface
- timer
- SP memory

MP/MTM interface

The master processor handles data communication between the card and the MTM through the MP/MTM interface. The interface uses the signaling channels 0 and 16 of the PCM interface. The interface transmits system supervision information.

MP

The main function of the master processor is to control the tones generated and received for the test procedure. The CC informs the MP of the test the MP must perform. The MP reads the test instructions from the MP memory. The MP controls the SP to produce the correct test tones. In addition, the MP controls the interfaces between the MP and the MTM, the SP, and the DF card.

MP memory

The MP memory has 12 kbyte of PROM and 2 kbyte of RAM. The PROM memory is not volatile and stores test instructions. The RAM memory is volatile and stores test results for a short time.

DF interface

The DF interface handles most of the communications between the MP and the DF card. The MP controls communications that use the DF interface. Communications occur when the MP initializes the DF filter of select RAM or reads the DF PROM.

Direct memory access controller

The DMA controller sends results from the DF card directly to the MP RAM. On the reception of a request from the DF, the DMA controller places the MP in hold mode. After this action, the DMA controller transfers the data to the MP RAM. When the data transfer is complete, the DMA controller releases the MP from hold mode.

Master/signal interface

The MP and the SP send messages to each other through the master/signal interface. The interface uses the data buses on the MP and the SP and four control signals and one interrupt line.

PCM signal generator

The PCM signal generator creates PCM waveforms for the tones the MP requests. The signal generator reads information on how to construct specified tones from the SP PROM. After the generator reads the information, the generator constructs the waveforms. The generator stores the waveforms in the SP RAM.

The system uses μ=255 encoding to construct PCM signals.

NT2X47AA (continued)

PCM output interface

The PCM output interface receives the tone waveforms from the SP RAM. The PCM sends the waveforms over the transmit data (XDAT) bus.

Timer

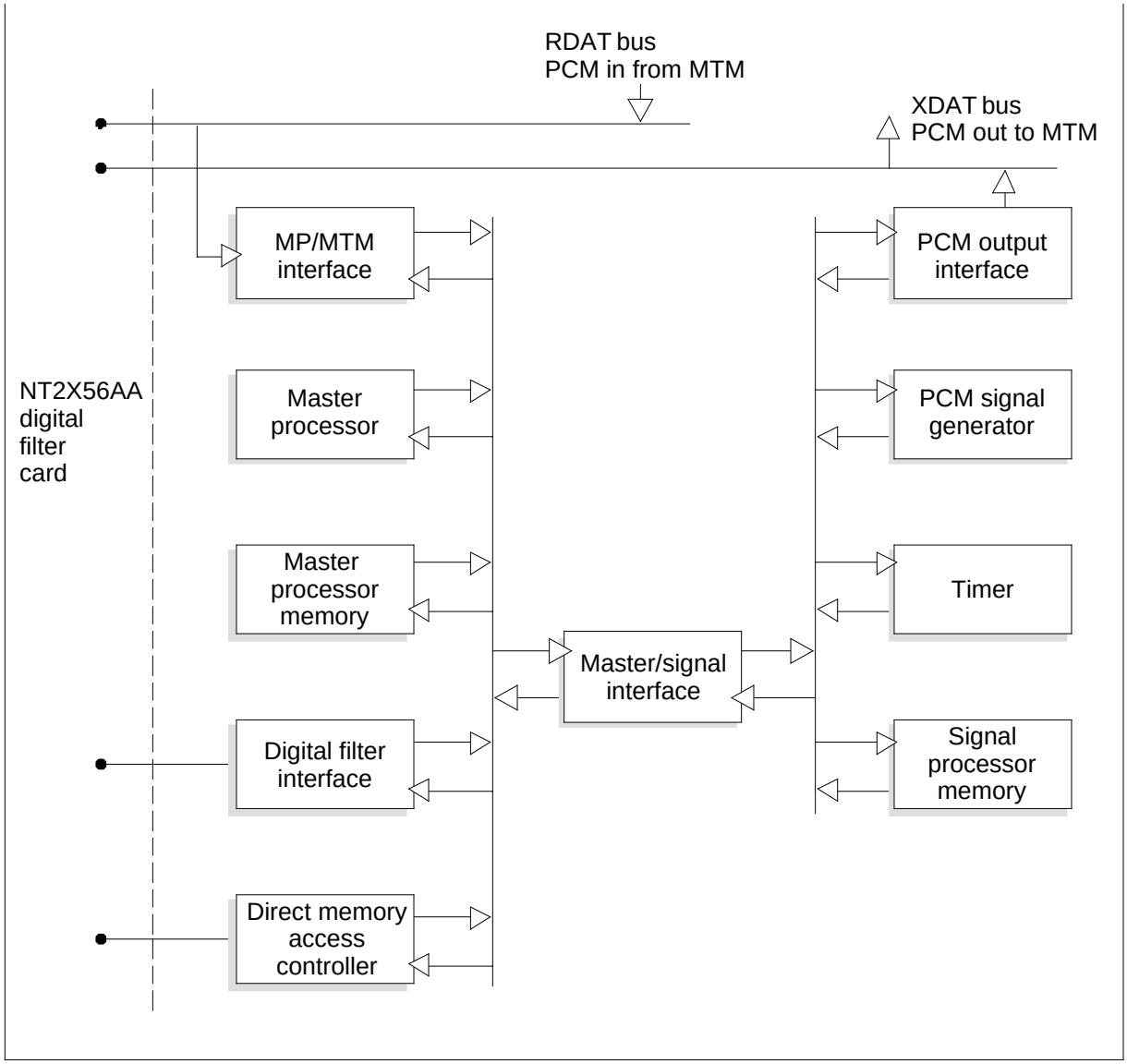
The timer times MP time-outs and count frames. You can program the timer for intervals from microseconds through 56 s. The intervals determine when the MP times out and needs to be reset. The other part of the timer counts frames to control the PCM output interface.

SP memory

The SP memory consists of 8 kbyte of PROM and 2 kbyte of RAM. The PROM memory is not volatile and stores companding tables to construct tone waveforms. The RAM memory is volatile and stores completed tone waveforms before the system sends the waveforms out.

The relationship between the functional blocks appears in the following figure.

NT2X47AA operating blocks



Technical data

The frequency range of the NT2X47AA tone generator is from 4 Hz through 3996 Hz in 4-Hz increments. The level range of the tone generator is from -60 dBm through +3 dBm.

NT2X47AA (end)

Dimensions

The dimensions for the NT2X47AA circuit card are as follows:

- height:

  353 mm (13.9 in.)

- depth:

  277 mm (10.9 in.)

Power requirements

The power requirements for the NT2X47AA appear in the following table.

Power requirements

Voltage	Current
+5 V	1.65A
-12V	7.00mA
-15V	0.05mA

Power distribution is 8.35W.

NT2X47AB

Product description

The transmission test unit (TTU) contains the NT2X47AB transmission test unit controller card and the NT2X56AA digital filter (DF) card. The TTU is a digital signal processor. You can program the TTU to permit transmission measurements and performance of maintenance functions. The NT2X47AB card controls the testing procedures and generates the tones that the tests require. The NT2X47AB can work with the NT2X56AA. This combination allows automatic transmission measuring equipment (ATME) test procedures to occur for a DMS-300 office.

Location

The NT2X47AB occupies one card position in the maintenance trunk module (MTM) shelf. The card must be in the slot next to the digital filter card.

Functional description

The NT2X47AB contains two main processors. The processors are the master processor (MP) and the signal processor (SP). The MP controls the generation, reception, and timing of tones the test specifies. The MP controls these actions when the card receives instructions from the central control (CC) to perform a test. After the test is complete, the MP transmits the test results back to the CC. The SP generates the tones the TTU tests require. The SP generates the correct tone waveform and supplies the tone at the correct level for the test.

Functional blocks

NT2X47AB has the following operating blocks:

- MP/MTM interface
- MP
- MP memory
- DF interface
- direct memory access (DMA) controller
- master/signal interface
- PCM signal generator
- PCM output interface
- timer
- SP memory

NT2X47AB (continued)

MP/MTM interface

The MP controls data communication between the card and the MTM through the MP/MTM interface. The interface uses the signaling channels 0 and 16 of the PCM interface. The interface transmits system supervision information.

MP

The main function of the master processor is to control tones generated and received for the test procedure. The CC informs the MP of the test the MP must perform. The MP reads the test instructions from the MP memory. The MP controls the SP so that the SP produces the correct test tones. In addition, the MP controls the interfaces between the MP and the MTM, the SP and the DF card.

MP memory

The MP memory consists of 12 kbyte of PROM and 2 kbyte of RAM. The PROM memory is not volatile and stores test instructions. The RAM memory is volatile and stores test results on a short period of time.

DF interface

The DF interface handles most communications between the MP and the DF card. The MP controls most communications that use the DF interface. Communications occur when the MP initializes the DF filter of select RAM or reads the DF PROM.

Direct memory access controller

Use the DMA controller to send results from the DF card directly to the MP RAM. When the DMA controller receives a request from the DF, the DMA controller places the MP in hold mode. After this action occurs, the DMA controller transfers the data to the MP RAM. When the data transfer is complete, the DMA controller releases the MP from hold mode.

Master/signal interface

The MP and the SP send messages with the master/signal interface. The interface uses the data buses on the MP and the SP and four control signals and one interrupt line.

PCM signal generator

The PCM signal generator creates PCM waveforms for the tones the MP requests. The signal generator reads information on how to construct specified tones from the SP PROM. The PCM generator constructs the waveforms and stores the waveforms in the SP RAM.

The system uses μ=255 encoding to construct PCM signals.

PCM output interface

The PCM output interface receives the tone waveforms from the SP RAM. After the interface receives the waveforms, the interface sends the waveforms over the transmit data (XDAT) bus.

Timer

The timer times MP time-outs and count frames. You can program the timer for intervals from microseconds through 56 s. The intervals determine when the MP has timed out and must be reset. The other part of the timer counts frames to control the PCM output interface.

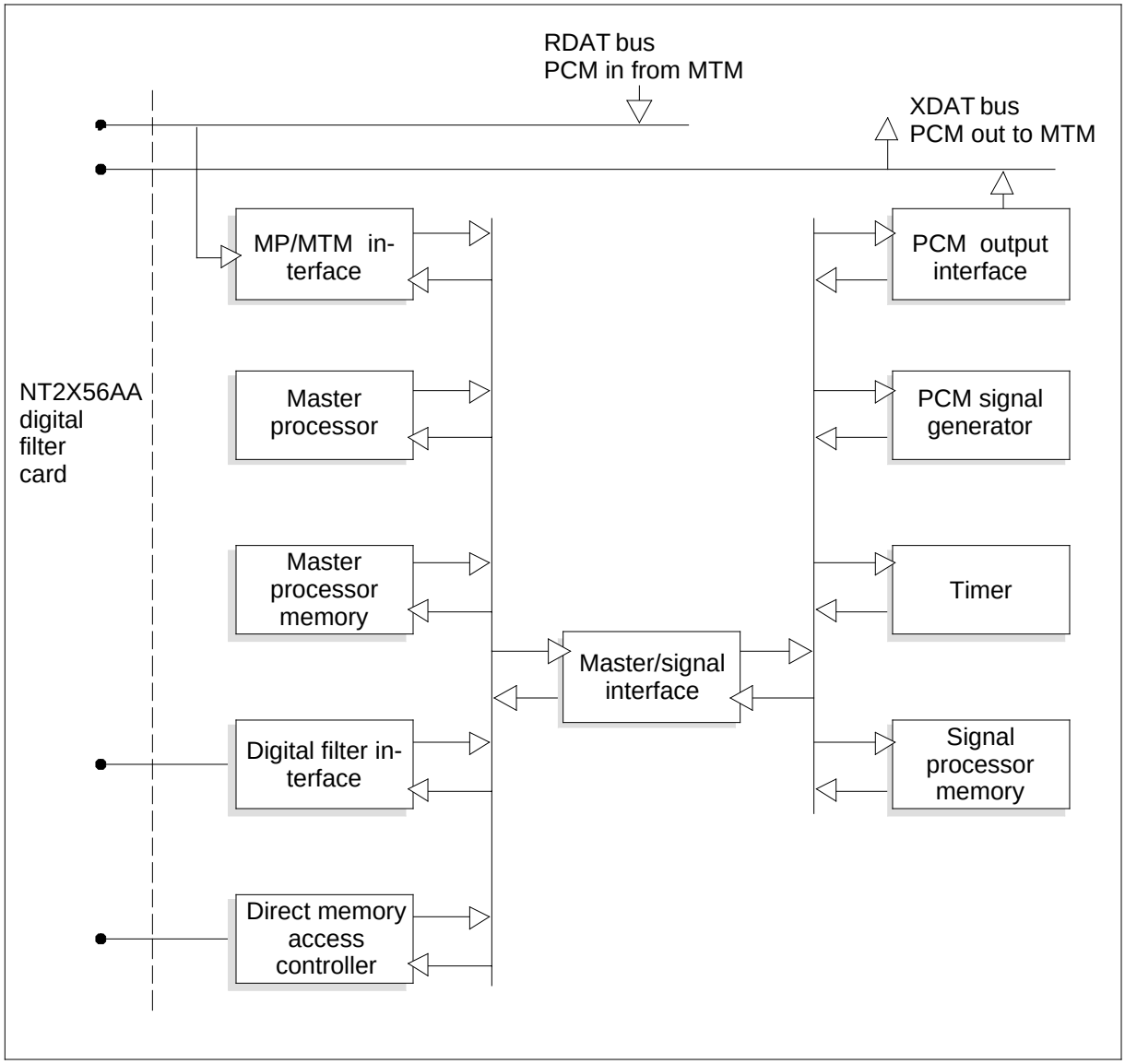
SP memory

The SP memory consists of 8 kbyte of PROM and 2 kbyte of RAM. The PROM memory is not volatile and stores companding tables to construct tone waveforms. The RAM memory is volatile and stores completed tone waveforms before the system sends them out.

The relationship between the functional blocks appears in the following figure.

NT2X47AB (continued)

NT2X47AB functional blocks



Technical data

The frequency range of the NT2X47AB tone generator is from 4 Hz through 3996 Hz in 4 Hz increments. The level of the tone generator range is from -60 dBm through +3 dBm.

Dimensions

The dimensions for the NT2X47AB circuit card are as follows:

- height:

  353 mm (13.9 in.)

- depth:

  277 mm (10.9 in.)

Power requirements

The power requirements for the NT2X47AB appear in the following table.

Power requirements

Voltage	Current
+5 V	1.65A
-12V	7.00mA
-15V	0.05mA

Power distribution is 8.35W.

NT2X47AC

Product description

The test transmission unit (TTU) contains the NT2X47AC transmission test unit controller card and the NT2X56AB digital filter (DF). The TTU is a digital signal processor. You can program the TTU to permit transmission measurements and performance of maintenance functions. The NT2X47AC card controls the test procedures and generates the tones that the tests require. The NT2X47AC and NT2X56AB are combined to perform automatic transmission measuring equipment-2 (ATME2) test procedures and automatic transmission measuring system test procedures (ATMS). The NT2X47AC and NT2X56AB use the ATME2 for a 104 test line and the ATMS for a 105 test line.

Location

The NT2X47AC occupies one card position in the maintenance trunk module (MTM) shelf. Place the card in the slot opposite the digital filter card.

Functional description

The NT2X47AC contains two main processors: the master processor (MP) and the signal processor (SP). The card receives instructions from the central control (CC) to perform a test. The MP controls the generation, reception and timing of the tones specified in the test. After the test is complete, the MP transmits the test results back to the CC. The SP generates the tones required for the TTU tests. The SP generates the correct tone waveform. The SP supplies the tone at the correct level for the test.

Functional blocks

The NT2X47AC has the following functional blocks:

- MP/MTM interface
- MP
- MP memory
- DF interface
- direct memory access (DMA) controller
- master/signal interface
- PCM signal generator
- PCM output interface
- timer
- SP memory

MP/MTM interface

The master processor handles the data communication between the card and the MTM through the MP/MTM interface. The interface uses the signaling channels 0 and 16 of the PCM interface. The interface also transmits system supervision information.

MP

The main function of the master processor is to control the tones that are generated and received for the test procedure. The CC informs the MP of the test to perform. The MP reads the test instructions from the MP memory. The MP controls the SP to produce the correct test tones. The MP also controls the interfaces between the MP and the MTM, the SP and the DF card.

MP memory

The MP memory contains of 12 Kbytes of PROM and 2 Kbytes of RAM. The PROM is nonvolatile memory that stores test instructions. The RAM is volatile memory that stores test results for a limited amount of time.

DF interface

The DF interface handles most of the communications between the MP and the DF card. The MP uses the DF interface to control communications. Communications occur when the MP initializes the DF filter select RAM or the MP reads the DF PROM.

Direct memory access controller

The DMA controller sends results from the DF card directly to the MP RAM. When the DMA controller receives a request from the DF, the DMA controller places the MP in hold mode. The DMA transfers the data to the MP RAM. When the data transfer is complete, the DMA controller releases the MP from hold mode.

Master/signal interface

The MP and the SP send messages with the master/signal interface. The interface uses the data buses on the MP and the SP, four control signals and one interrupt line.

PCM signal generator

The PCM signal generator creates PCM waveforms for the tones that the MP requests. The signal generator reads information on how to construct tones from the SP PROM. The signal generator constructs the waveforms. The signal generator stores the waveforms in the SP RAM.

The PCM signals are constructed with μ=255 encoding.

NT2X47AC (continued)

PCM output interface

The PCM output interface receives tone waveforms from the SP RAM. The PCM output interface sends the waveforms out over the transmit data (XDAT) bus.

Timer

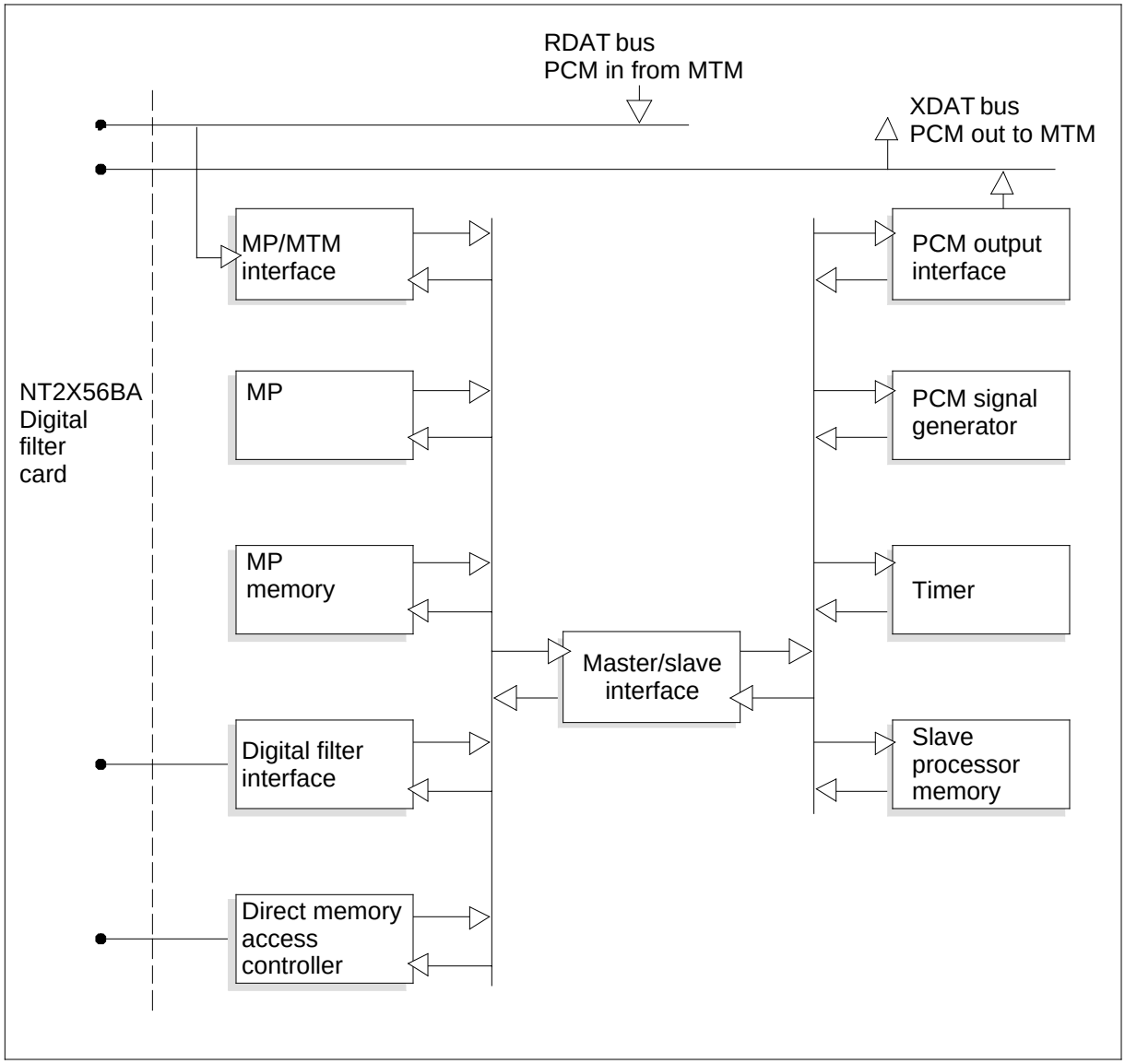
The timer times the MP time-outs and count frames. You can program the timer for intervals from microseconds through 56 s. You can program the timer to determine when the MP has timed out and must be set again. The other part of the timer counts frames to control the PCM output interface.

SP memory

The SP memory contains 8 Kbytes of PROM and 2 Kbytes of RAM. The PROM is nonvolatile memory that stores companding tables for constructing tone waveforms. The RAM is volatile memory that stores completed tone waveforms before the SP sends the waveforms out.

The relationship between the functional blocks appears in the following figure.

NT2X47AC functional blocks



Technical data

The frequency range of the NT2X47AC tone generator is from 4 through 3996 Hz in 4 Hz increments. The level of the tone ranges from -60 dBm through +3 dBm.

NT2X47AC (end)

Dimensions

The dimensions for the NT2X47AC circuit card follow:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)

Power requirements

The power requirements for the NT2X47AC appear in the following table.

Power requirements

Voltage	Current
+5 V	1.65A
-12V	7.00mA
-15V	0.0 mA

The power distribution is 8.35W.

NT2X47BA

Product description

The NT2X47BA control processor (CP) and the NT2X56BA digital filter make up the transmission test unit (TTU). The TTU is a digital signal processor. You can program the TTU to allow transmission measurements and the performance of maintenance functions. The CP card controls test procedures and generates the tones that the tests require. The combination of NT2X47BA and NT2X56BA perform international automatic transmission measuring equipment (ATME) and automatic transmission measuring system (ATMS) tests.

Location

The NT2X47BA occupies one card position in the maintenance trunk module (MTM) shelf. Place the card in the slot next to the digital filter card.

Functional description

The CP card contains two main processors. The processors are the master processor (MP) and the slave processor. The card receives instructions from the central control (CC) to perform a test. The MP controls the generation, reception and timing of the tones that the test specifies. When the test is complete, the MP transmits the test results back to the CC. The slave processor generates the tones for the TTU tests. The slave processor generates the correct tone waveform. The slave processor also supplies the tone at the correct level for the test.

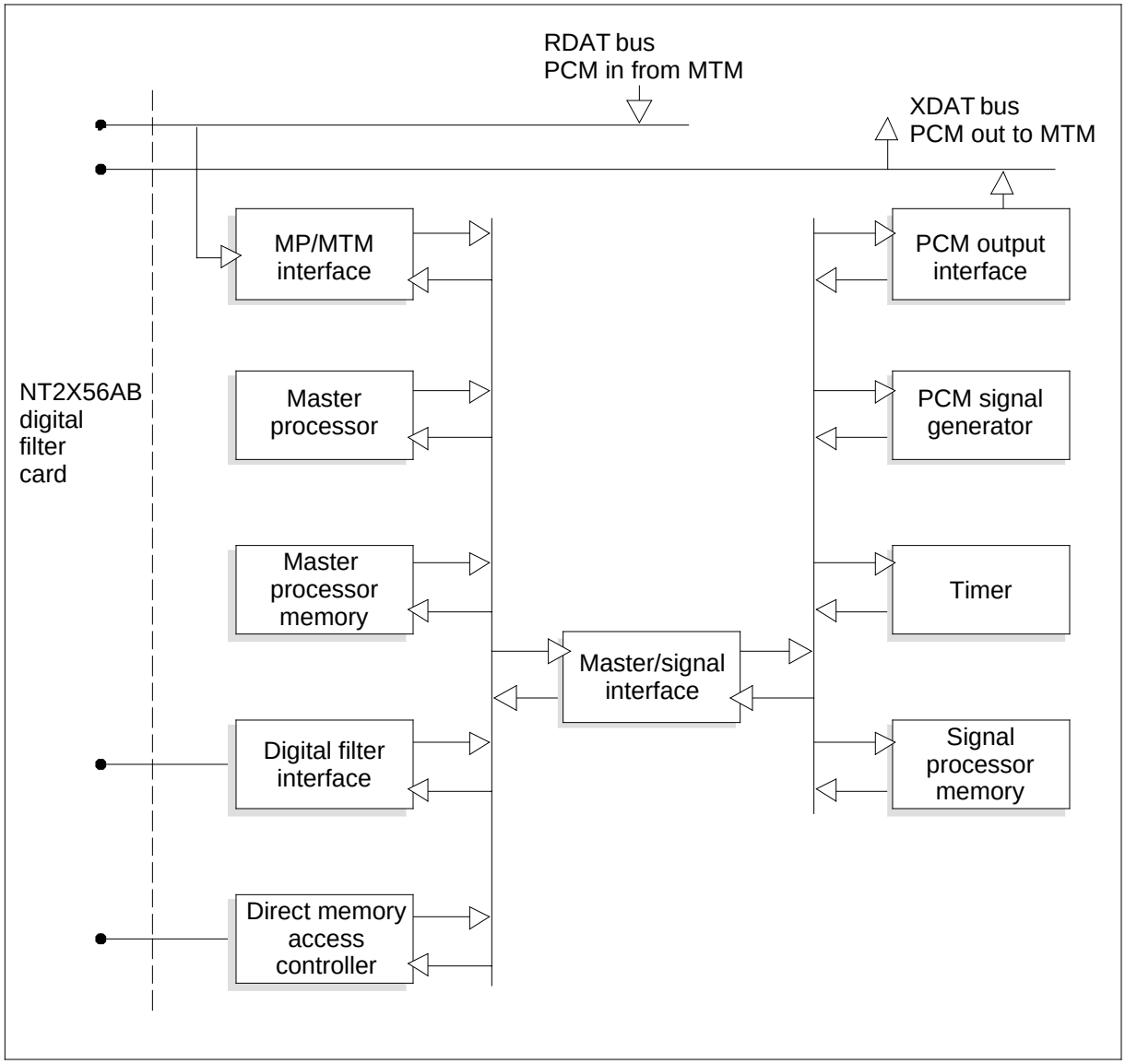
Functional blocks

The NT2X47BA appear in the following figure. The functional blocks are as follows:

- MP/MTM interface
- MP
- MP memory
- digital filter interface
- direct memory access (DMA) controller
- master/slave interface
- pulse code modulation (PCM) signal generator
- PCM output interface
- timer
- slave processor memory

NT2X47BA (continued)

NT2X47BA functional blocks



MP/MTM interface

The MP uses the MP/MTM interface to handle data communication between the card and the MTM. The interface uses signaling channels 0 and 16 of the PCM interface. The interface also transmits system supervision information.

MP

The main function of the MP is to control the tones for the test procedure. The CC informs the MP of the test to perform. The MP reads the test instructions from the MP memory. The MP controls the slave processor to produce the

correct test tones. The MP also controls the interfaces between the MP and the MTM, the slave processor and the DF card.

MP memory

The MP memory has 12 kbytes of PROM and 2 kbytes of RAM. The PROM is non-volatile memory that stores test instructions. The RAM is volatile memory that stores test results for a limited time.

Digital filter interface

The digital filter interface handles most of the communications between the MP and the DF card. The MP controls communications that use the DF interface. Communications occur when the MP initializes the DF filter select RAM or reads the DF PROM.

DMA controller

The DMA controller sends results from the DF card directly to the MP RAM. When the DMA receives a request from the DF, the DMA controller places the MP in hold mode. The DMA controller transfers the data to the MP RAM. When the data transfer is complete, the DMA controller releases the MP from hold mode.

Master/slave interface

The MP and the slave processor send messages to each other with the master/slave interface. The interface uses the data buses on the MP and the slave processor. The interface also uses four control signals and one interrupt line.

PCM signal generator

The PCM signal generator creates the PCM waveforms for the tones that the MP requests. The signal generator reads information on how to construct tones from the slave processor PROM. The signal generator constructs the waveforms. The signal generator stores the waveforms in the slave processor RAM.

The PCM signals are constructed with A-law coding.

PCM output interface

The PCM output interface receives the tone waveforms from the slave processor RAM. The PCM sends the waveforms out over the XDAT bus.

Timer

The slave processor timer times MP timeouts and counts frames. You can program the timer for intervals from microseconds to 56 s. You can program

NT2X47BA (end)

the timer to determine when the MP times out and must be set again. The other part of the timer counts frames to control the PCM output interface.

Slave processor memory

The slave processor memory has of 8 kbytes of PROM and 2 kbytes of RAM. The PROM is non-volatile memory that stores companding tables for constructing tone waveforms. The RAM is volatile memory that stores completed tone waveforms before the PCM sends the waveforms out.

Technical data

The frequency range of NT2X47BA tone generator is from 4 to 3996 Hz in 4-Hz increments. The level range of the tone generator is from -60 dBm to +3 dBm.

Dimensions

The dimensions for NT2X47BA circuit card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)

Power requirements

The power requirements for the NT2X47BA appear in the following table.

Power requirements

Voltage	Current
+ 5V	1.65A
-12V	7mA
-15V	0.05mA

The power distribution is 8.35W.

Product description

The NT2X48AA digital four-channel multifrequency receiver card receives pulse code modulation (PCM) data from a maximum of four channels. The NT2X48AA detects standard multifrequency (MF) tones on the four channels. The card decodes the tones and provides 8-bit binary codes to indicate the tones received.

The card is designed for μ-law applications.

Location

The NT2X48AA occupies two card positions in a maintenance trunk module (MTM) or a trunk module (TM).

Functional description

The digital filter system detects the MF tones in the PCM data received on the receive data (RDAT) bus. The output of the filter is sent to the microprocessor. The microprocessor converts the tone information to binary-code format. The code information returns to the MTM with the transmit data (XDAT) bus.

Functional blocks

The NT2X48AA contains the following functional blocks:

- PCM data input
- digital filter
- control sequencer
- serial accumulator
- microprocessor
- trunk logic circuit (TLC)

PCM data input

The PCM data input circuit receives the PCM information from the RDAT bus. The RDAT bus is under control of the enable lines. The PCM data input circuit holds the data in the input circuit until the RDAT sends the data to the digital filter.

Digital filter

The digital filter converts the data that enters the filter circuit into linear form. The digital filter squares the data to determine the signal strength. The digital filter circuit contains six separate filters, one filter for each MF tone. The digital filter operates under control of the sequencer. The output of the filter circuit is sent to the serial accumulator.

NT2X48AA (continued)

Control sequencer

The control sequencer synchronizes the processing of the tone information with the rate of received PCM information. The sequencer synchronizes with the first received PCM sample. The sequencer synchronizes again with each PCM sample that follows. The sequencer output regulates the operation of the digital filter and the microprocessor.

Serial accumulator

The serial accumulator takes samples of the filter circuit output and adds the values of the samples. The accumulator takes 2 bytes of samples for each of the eight filters. The accumulator adds the values of the samples and sends the results to the microprocessor. The accumulator uses direct memory access (DMA) to place the data directly in the memory of the microprocessor.

Microprocessor

The microprocessor receives the output of the serial accumulator and decodes the meaning of the tone. The MF tones that the microprocessor decodes appear in the following table.

Received MF tones (Sheet 1 of 2)

Digit or explanation	Signaling frequencies (Hz)
1	700 + 900
2	700 + 1100
3	900 + 1100
4	700 + 1300
5	900 + 1300
6	1100 + 1300
7	700 + 1500
8	900 + 1500
9	1100 + 1500
0	1300 + 1500
KP-preparation for digits	1100 + 1700
ST-end of pulsing sequence	1500 + 1700
TSP-traffic service position system	900 + 1700

Received MF tones (Sheet 2 of 2)

Digit or explanation	Signaling frequencies (Hz)
TSP2-traffic service position system	1300 + 1700
TSP3-traffic service position system	700 + 1700
Coin collect-coin control	700 + 1100
Coin return-coin control	1100 + 1700
Ringback-coin control	700 + 1700
Code 11-inward operator	700 + 1700
Code 12-delay operator	900 + 1700
KP1-terminal call	1100 + 1700
KP2-transmit call	1300 + 1700

After the microprocessor decodes the tone, the microprocessor creates an 8-bit code. The 8-bit code identifies the tone. The microprocessor sends the 8-bit code to the trunk logic circuit. The 8-bit code format appears in the following table.

8-bit code format

Explanation	8-bit code
Valid digit-XXXX=received digit in hexadecimal form	1 Y0Y XXXX
Valid pause (no signal)	0 000 0000
Error message-noisy	1 011 001
Error message-large twist	1 011 010
Error message-three frequencies	1 011 100
Error message-indecision or invalid	1 011 111
Error message-no interdigit pause (XXXX=received digit)	1 111 XXXX

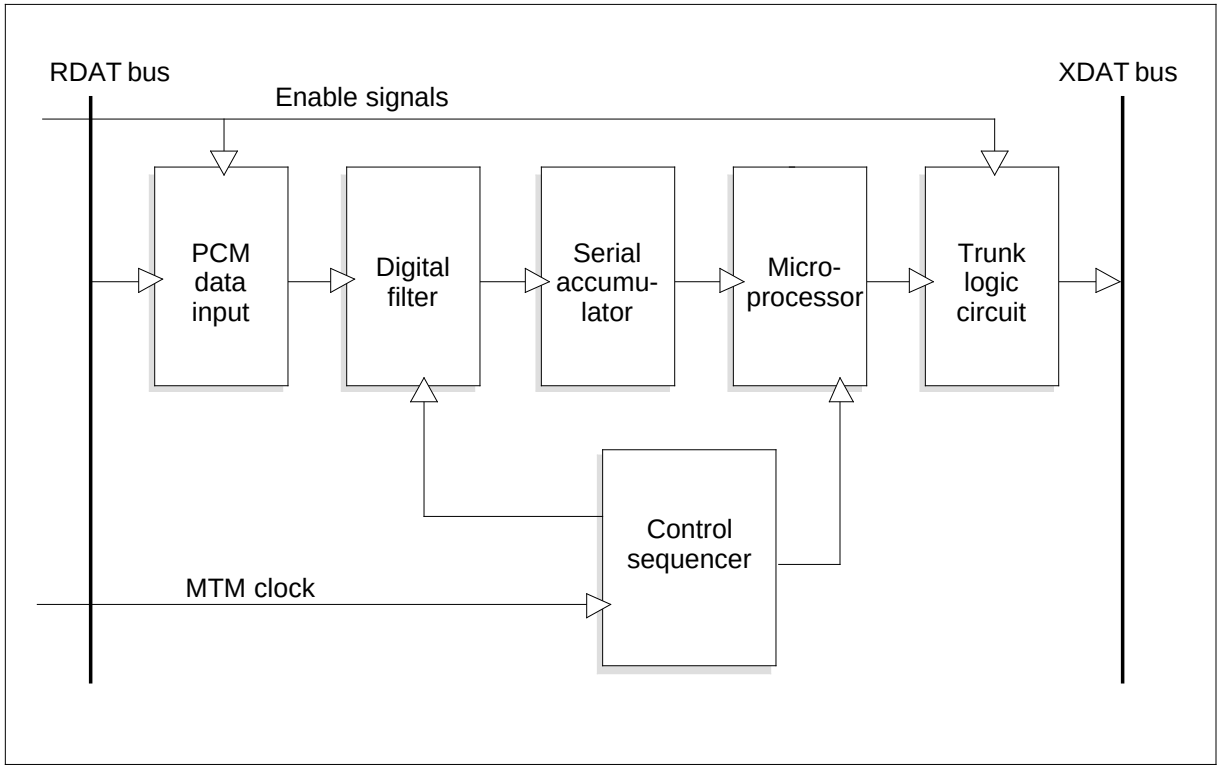
TLC

The TLC sends the 8-bit code to the MTM. The TLC receives the code from the microprocessor. The TLC sends the code over the XDAT bus when the system scans the channel of the card.

NT2X48AA (continued)

The relationship between the functional blocks appears in the following figure.

NT2X48AA functional blocks



Technical data

The NT2X48AA accepts or rejects digits according to the standards that appear in the following table.

Input signal tolerances (Sheet 1 of 2)

Standard	Accept digits	Reject digits
Frequency tolerance	±1.5% + 10 Hz of nominal frequency	±5% of nominal, either frequency
Signal duration	≥20 ms ON	≤10 ms ON
	≥55 ms ON KP	
	≥25 ms OFF	≤10 ms OFF

Input signal tolerances (Sheet 2 of 2)

Standard	Accept digits	Reject digits
Input level	-22 to -2 dBm per frequency	≥-30 dBm per frequency
Twist	≥6 dB between two frequencies	≥16 dB between two frequencies

Dimensions

The dimensions for the NT2X48AA circuit card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 56 mm (2.2 in.)

Power requirements

The power requirements for the NT2X48AA appear in the following table.

Power requirements

Voltage	Current
+12V	0.01A
+5V	2.00A
-15V	0.10A

NT2X48AB

Production description

The NT2X48AB digital four-channel receiver card receives pulse code modulation (PCM) data from a maximum of four channels. The NT2X48AB card detects standard Digitone tones on these channels. The card decodes the received tones and provides 8-bit binary codes. The codes indicate the received tones.

The card is designed for μ-law applications.

Location

The NT2X48AB occupies two card positions in a maintenance trunk module (MTM) or a trunk module (TM).

Functional description

The Digitone tones are detected in the PCM data. A digital filter system receives the tones on the receive data (RDAT) bus. The filter output goes to the microprocessor. The microprocessor converts the received tone information to binary-code format. The transmit data (XDAT) bus returns the code information to the MTM.

Functional blocks

The NT2X48AB contains the following functional blocks:

- PCM data input
- digital filter
- control sequencer
- serial accumulator
- microprocessor
- trunk logic circuit (TLC)

PCM data input

The RDAT bus sends the PCM information to the PCM data input circuit. The enable lines control the PCM information. The input circuit holds the data until the data goes to the digital filter.

Digital filter

Data that enters the filter circuit converts to linear form. The data converts to linear form before the filter circuit squares the data to determine the signal strength. The digital filter circuit contains eight separate filters. One file is present for each Digitone tone. The sequencer controls the digital filter operation. The filter circuit output goes to the serial accumulator.

Control sequencer

The control sequencer synchronizes the tone information processing at the rate of received PCM information. The sequencer synchronizes again with the PCM sample that was received first and synchronizes again with every PCM sample that follows. The sequencer output regulates the operation of the digital filter and the microprocessor.

Serial accumulator

The serial accumulator takes samples of the filter circuit output and adds the values of the samples. The accumulator takes 2 bytes of samples for each of the eight filters. The accumulator adds the values of the samples and sends the figure to the microprocessor. The accumulator uses direct memory access (DMA) to place the data in the memory of the microprocessor.

Microprocessor

The microprocessor receives the output of the serial accumulator and decodes the meaning of the received tone. The Digitone tones that the microprocessor decodes appear in the following table.

Received MF tones (Sheet 1 of 2)

Digit or explanation	Signaling frequencies (Hz)
1	1209 + 697
2	1336 + 697
3	1477 + 697
4	1209 + 770
5	1336 + 770
6	1477 + 770
7	1209 + 852
8	1336 + 852
9	1477 + 852
0	1336 + 941
*	1209 + 941
#	1477 + 941
Spare	1633 + 697

NT2X48AB (continued)

Received MF tones (Sheet 2 of 2)

Digit or explanation	Signaling frequencies (Hz)
Spare	1633 + 770
Spare	1633 + 852
Spare	1633 + 941

After the microprocessor decodes the received tone, the microprocessor creates an 8-bit code. The 8-bit code identifies the tone and sends the code to the trunk logic circuit. The 8-bit code format appears in the following table.

8-bit code format

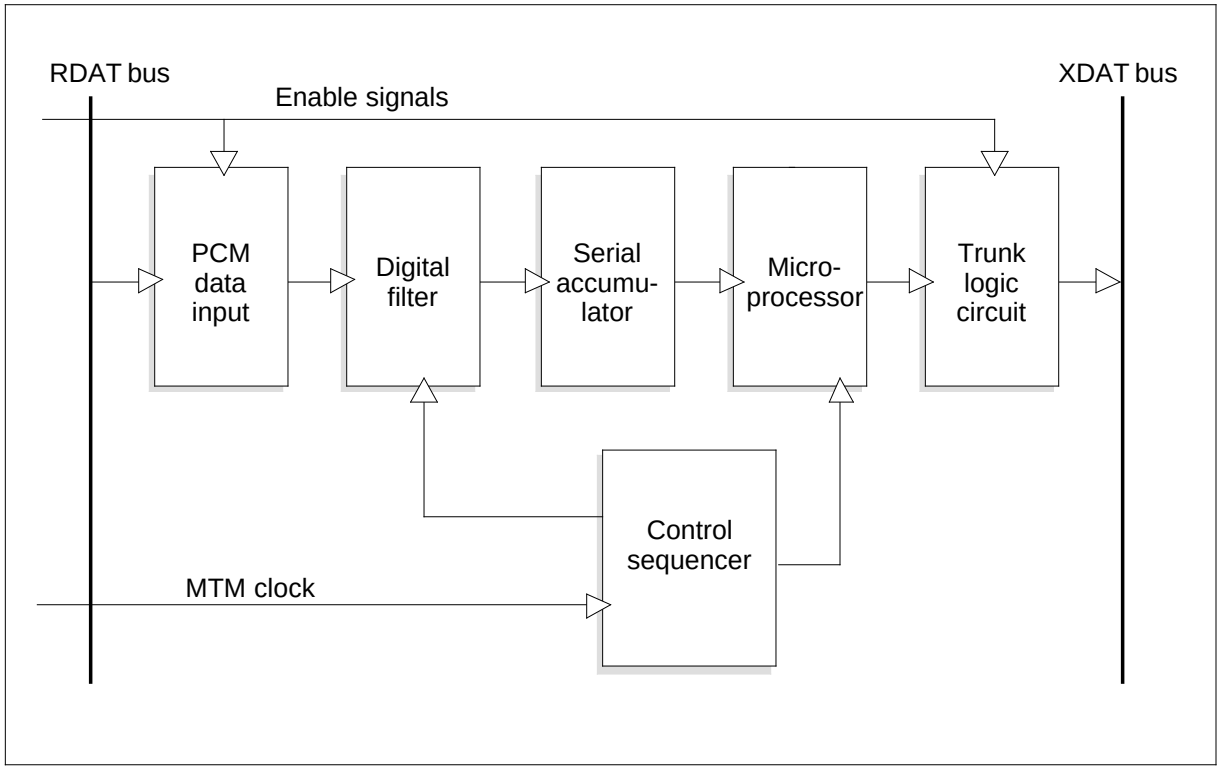
Explanation	8 bit code
Valid digit-XXXX=received digit in hexadecimal form	1 000 XXXX
Valid pause (no signal)	0 000 000

TLC

The TLC sends the 8-bit code to the MTM. The TLC receives the code from the microprocessor and sends the code with the XDAT bus. The TLC sends the code when the channel of the RC is scanned.

The relationship between the functional blocks appears in the following figure.

NT2X48AB functional blocks



Technical data

The information in the following table determines if the NT2X48AB accepts or rejects digits.

Input signal tolerances (Sheet 1 of 2)

Standard	Accept digits	Reject digits
Frequency tolerance	±1.5% + 10 Hz of nominal frequency	±3.5% of nominal, either frequency
Signal duration	≥40 ms ON	≤15 ms ON
	≥20 ms OFF	≤15 ms OFF
	>85 ms ON plus OFF	

NT2X48AB (end)

Input signal tolerances (Sheet 2 of 2)

Standard	Accept digits	Reject digits
Input level	-24 dBm to 0 dBm per frequency	≥-32 dBm per frequency
Twist	-8 dB to 4 dB high frequency to low frequency	≥16 dB high frequency to low frequency

The NT2X48AB detects low-level Digitone tones in gaussian and impulse noise. The NT2X48AB detects the tones with a low error rate. The card detects tones in signal echoes delayed a maximum of 20 ms. The card can detect tones from the original signal that are reduced by a maximum of 10 dB.

Dimensions

The NT2X48AB circuit card has the following dimensions:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 56 mm (2.2 in.)

Power requirements

The power requirements for the NT2X48AB appear in the following table.

Power requirements

Voltage	Current
+12 V	0.01A
+5 V	2.0 A
-15V	0.10A

NT2X48BA

Product description

The NT2X48BA digital four-channel multifrequency receiver card receives pulse code modulation (PCM) data from a maximum of four channels. The receiver card detects standard multifrequency (MF) tones on these four channels. The card decodes the received tones and provides 8-bit binary codes to indicate the tones received.

The card is for μ-law applications.

Location

The NT2X48BA occupies one card position in a maintenance trunk module (MTM) or a trunk module (TM).

Functional description

A digital filter system detects the MF tones in the PCM data received on the receive data (RDAT) bus. The microprocessor receives the output of the filter. The microprocessor converts the received tone information to binary-code format. The microprocessor returns the code information to the MTM on the transmit data (XDAT) bus.

Functional blocks

The NT2X48BA has the following functional blocks:

- PCM data input
- digital filter
- control sequencer
- serial accumulator
- microprocessor
- trunk logic circuit (TLC)

PCM data input

The PCM data input circuit receives the PCM information from the RDAT bus under control of the enable lines. The PCM data input circuit holds the data until the circuit sends the data to the digital filter.

Digital filter

Data that enters the filter circuit converts to linear form. The circuit filter squares the data to determine the signal strength. The digital filter circuit has six separate filters. One filter is present for each MF tone. The digital filter circuit operates under control of the sequencer. The filter circuit sends the output to the serial accumulator.

NT2X48BA (continued)

Control sequencer

The control sequencer synchronizes the processing of the tone information with the rate of received PCM information. The sequencer synchronizes with the first received PCM sample. The sequencer synchronizes with each PCM sample that follows. The sequencer output regulates the operation of the digital filter and the microprocessor.

Serial accumulator

The serial accumulator takes samples of the filter circuit output and adds the values of the samples. The accumulator takes two bytes of samples for each of the eight filters. The accumulator adds the values of the samples and sends the results to the microprocessor. The accumulator uses direct memory access (DMA) to place the data into the memory of the microprocessor.

Microprocessor

The microprocessor receives the output of the serial accumulator and decodes the meaning of the received tone. The MF tones that the microprocessor decodes appear in the following table.

Received MF tones (Sheet 1 of 2)

Digit or explanation	Signaling frequencies (Hz)
1	700 + 900
2	700 + 1100
3	900 + 1100
4	700 + 1300
5	900 + 1300
6	1100 + 1300
7	700 + 1500
8	900 + 1500
9	1100 + 1500
0	1300 + 1500
KP-preparation for digits	1100 + 1700
ST-end of pulsing sequence	1500 + 1700
TSP-traffic service positions system	900 + 1700

Received MF tones (Sheet 2 of 2)

Digit or explanation	Signaling frequencies (Hz)
TSP2-traffic service position system	1300 + 1700
TSP3-traffic service position system	700 + 1700
Coin collect-coin control	700 + 1100
Coin return-coin control	1100 + 1700
Ringback-coin control	700 + 1700
Code 11-inward operator	700 + 1700
Code 12-delay operator	900 + 1700
KP1-terminal call	1100 + 1700
KP2-transmit call	1300 + 1700

After the microprocessor decodes the received tone, the microprocessor creates an 8-bit code to identify the tone. The microprocessor sends the code to the trunk logic circuit. The 8-bit code format appears in the following table.

8-bit code format

Explanation	8-bit code
Valid digit-XXXX=received digit in hexadecimal form	1 Y0Y XXXX
Valid pause (no signal)	0 000 0000
Error message-noisy	1 011 001
Error message-large twist	1 011 010
Error message-three frequencies	1 011 100
Error message-indecision or invalid	1 011 111
Error message-no interdigit pause (XXXX=received digit)	1 111 XXXX

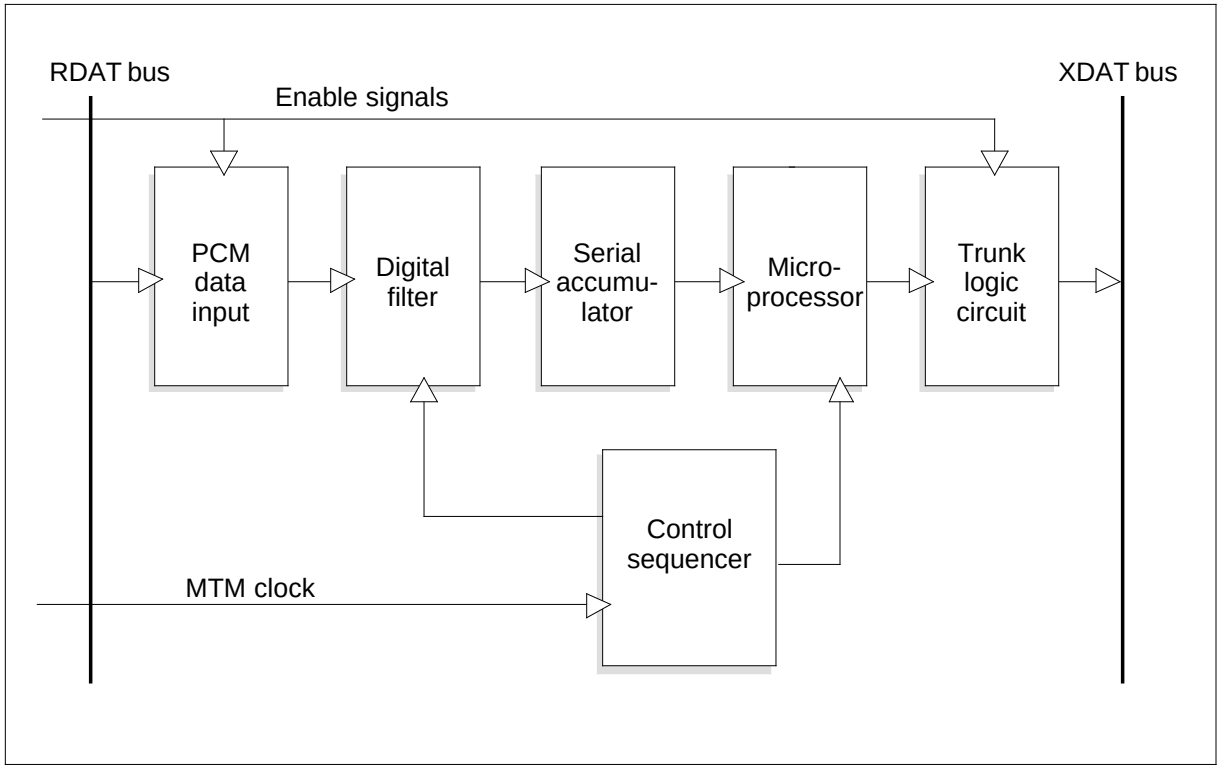
TLC

The TLC sends the 8-bit code to the MTM. The TLC receives the code from the microprocessor. The TLC sends the code over the XDAT bus when the channel of the card is scanned.

NT2X48BA (continued)

The relationship between the functional blocks appears in the following figure.

NT2X48BA functional blocks



Technical data

The information that appears in the following table determines if the NT2X48BA accepts or rejects digits.

Input signal tolerances (Sheet 1 of 2)

Standard	Accept digits	Reject digits
Frequency tolerance	±1.5% + 10 Hz of nominal frequency	±5% of nominal, either frequency
Signal duration	≥20 ms ON	≤10 ms ON
	≥55 ms ON KP	≤10 ms OFF
	≥25 ms OFF	

Input signal tolerances (Sheet 2 of 2)

Standard	Accept digits	Reject digits
Input level	-22 to -2 dBm per frequency	≥-30 dBm per frequency
Twist	≥6 dB between two frequencies	≥16 dB between two frequencies

Dimensions

The dimensions for the NT2X48BA circuit card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 28 mm (1.1 in.)

Power requirements

The power requirements for the NT2X48BA appear in the following table.

Power requirements

Voltage	Current
+12 V	0.01 A
+5 V	2.00 A
-15 V	0.10 A

NT2X48BB

Product description

The NT2X48BB digital four-channel dual-tone multifrequency (DTMF) receiver card receives pulse code modulation (PCM) data from a maximum of four channels. The DTMF receiver card detects standard Digitone tones on these four channels. The card decodes the received tones. The card provides 8-bit binary codes to indicate the tones received.

The card is for μ-law applications.

Location

The NT2X48BB is in one card position in a maintenance trunk module (MTM) or a trunk module (TM).

Functional description

A digital filter system detects the Digitone tones in the PCM data received on receive data (RDAT) bus. The microprocessor receives the output of the filter. The microprocessor converts the received tone information into binary-code format. The microprocessor returns the code information to the MTM on the transmit data (XDAT) bus.

Functional blocks

The NT2X48BB has the following functional blocks:

- PCM data input
- digital filter
- control sequencer
- serial accumulator
- microprocessor
- trunk logic circuit (TLC)

PCM data input

The PCM data input circuit receives the PCM information from the RDAT bus under control of the enable lines. The PCM data input circuit holds the data in the input circuit until the circuit sends the data to the digital filter.

Digital filter

Data that enters the filter circuit converts to linear form. The circuit filter squares the data to determine the signal strength. The digital filter circuit has eight separate filters. One filter is present for each Digitone tone. The digital filter circuit operates under control of the sequencer. The filter circuit sends the output to the serial accumulator.

Control sequencer

The control sequencer synchronizes the processing of the tone information with the rate of received PCM information. The sequencer synchronizes with the first received PCM sample. The sequencer synchronizes with each PCM sample that follows. The sequencer output regulates the operation of the digital filter and the microprocessor.

Serial accumulator

The serial accumulator takes samples of the filter circuit output and adds the values of the samples. The accumulator takes two bytes of samples for each of the eight filters. The accumulator adds the values of the samples and sends the results to the microprocessor. The accumulator uses direct memory access (DMA) to place the data into the memory of the microprocessor.

Microprocessor

The microprocessor receives the output of the serial accumulator. The microprocessor decodes the meaning of the received tone. The Digitone tones that the microprocessor decodes appear in the following table.

Received MF tones (Sheet 1 of 2)

Digit or explanation	Signaling frequencies (Hz)
1	1209 + 697
2	1336 + 697
3	1477 + 697
4	1209 + 770
5	1336 + 770
6	1477 + 770
7	1209 + 852
8	1336 + 852
9	1477 + 852
0	1336 + 941
*	1209 + 941
#	1477 + 941
Spare	1633 + 697

NT2X48BB (continued)

Received MF tones (Sheet 2 of 2)

Digit or explanation	Signaling frequencies (Hz)
Spare	1633 + 770
Spare	1633 + 852
Spare	1633 + 941

After the microprocessor decodes the received tone, the microprocessor creates an 8-bit code to identify the tone. The microprocessor sends the code to the trunk logic circuit. The 8-bit code format appears in the following table.

8-bit code format

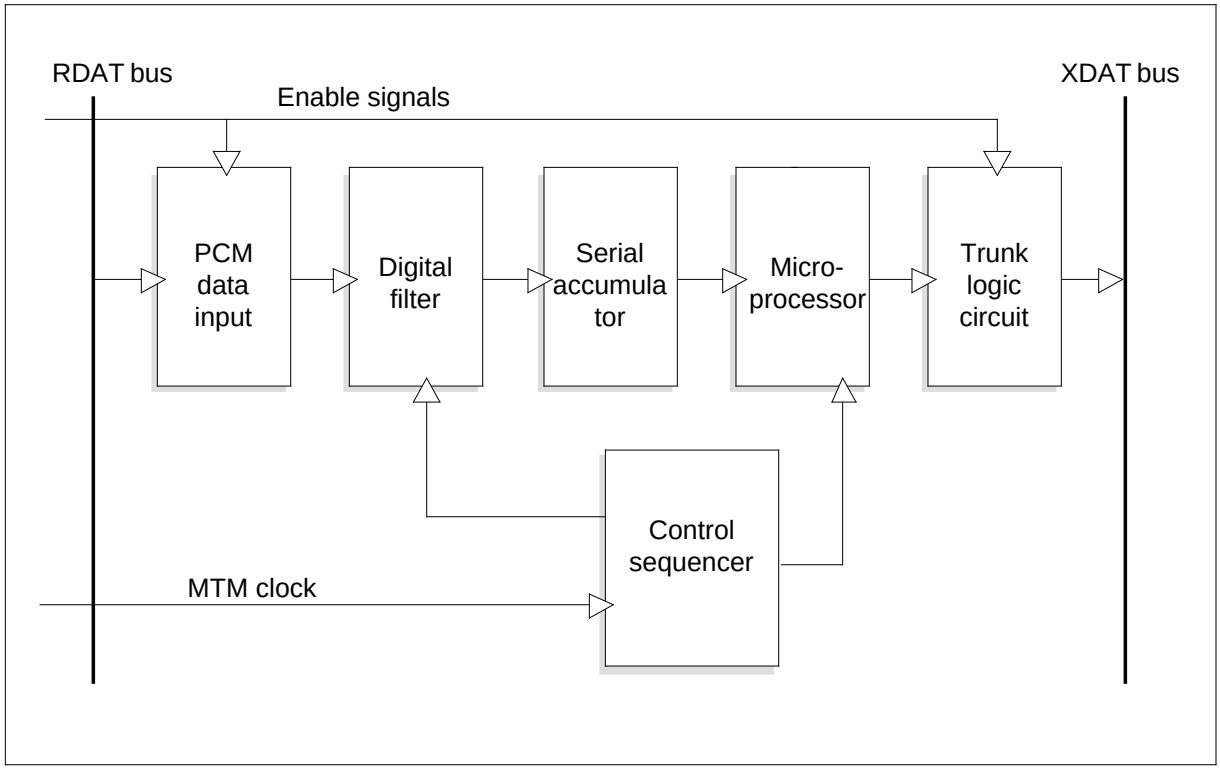
Explanation	8-bit code
Valid digit-XXXX=received digit in hexadecimal form	1 000 XXXX
Valid pause (a signal is not available)	0 000 0000

TLC

The TLC sends the 8-bit code to the MTM. The TLC receives the code from the microprocessor. The TLC sends the code over the XDAT bus when the channel of the card is scanned.

The relationship between the functional blocks appears in the following figure.

NT2X48BB functional blocks



Technical data

The information that appears in the following table determines if the accepts or rejects the digits.

Input signal tolerances (Sheet 1 of 2)

Standard	Accept digits	Reject digits
Frequency tolerance	±1.5% + 10 Hz of nominal frequency	±3.5% of nominal, either frequency
Signal duration	≥40 ms ON	≤15 ms ON
	≥20 ms OFF	≤15 ms OFF
	>85 ms ON plus OFF	

NT2X48BB (end)

Input signal tolerances (Sheet 2 of 2)

Standard	Accept digits	Reject digits
Input level	-24 to 0 dBm for each frequency	≥-32 dBm for each frequency
Twist	-8 dB to 4 dB high frequency to low frequency	≥16 dB high frequency to low frequency

The NT2X48BB detects low-level Digitone tones in the gaussian and impulse noise with a low error rate. The card detects tones in the signal echoes delayed a maximum of 20 ms from the original signal. The card detects tones in the signal echoes reduced in level a minimum of 10 dB from the original signal.

Dimensions

The following are the dimensions for the NT2X48BB circuit card:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 28 mm (1.1 in.)

Power requirements

The power requirements for the NT2X48BB appear in the following table.

Power requirements

Voltage	Current
+12 V	0.01 A
+5 V	2.00 A
-15 V	0.10 A

NT2X48CA

Product description

The NT2X48CA A-law multifrequency receiver (International-Turkey) receives pulse code modulation (PCM) data to a maximum of four channels. The receiver detects standard multifrequency (MF) tones on these channels. The card decodes the received tones and provides 8-bit binary codes to indicate the tones received.

The card is for A-law applications.

Location

The NT2X48CA occupies two card positions in a maintenance trunk module (MTM) or a trunk module (TM).

Functional description

A digital filter system detects the MF tones in the PCM data received on the receive data (RDAT) bus. The filter sends output of the filter to the microprocessor. The microprocessor converts the received tone information into binary-code format. The microprocessor returns the code information to the MTM on the transmit data (XDAT) bus.

Functional blocks

The NT2X48CA has the following functional blocks:

- PCM data input
- digital filter
- control sequencer
- serial accumulator
- microprocessor
- trunk logic circuit (TLC)

PCM data input

The PCM data input circuit receives the PCM information from the RDAT bus under control of the enable lines. The circuit holds the data until the circuit sends the data to the digital filter.

Digital filter

Data that enters the filter circuit converts to linear form. The filter squares the data to determine the signal strength. The digital filter circuit has six separate filters. One filter is present for each MF tone. The digital filter circuit operates under the control of the sequencer. The filter circuit sends the output to the serial accumulator.

NT2X48CA (continued)

Control sequencer

The control sequencer synchronizes the processing of the tone information with the rate of received PCM information. The sequencer synchronizes with the first received PCM sample. The sequencer synchronizes with each PCM sample that follows. The sequencer output regulates the operation of the digital filter and the microprocessor.

Serial accumulator

The serial accumulator takes samples of the filter circuit output and adds the values of the samples. The accumulator takes two bytes of samples for each of the eight filters. The accumulator adds the values of the samples and sends the results to the microprocessor. The accumulator uses direct memory access (DMA) to place the data directly into the memory of the microprocessor.

Microprocessor

The microprocessor receives the output of the serial accumulator. The microprocessor decodes the meaning of the received tone. The MF tones that the microprocessor decodes appear in the following table.

Received MF tones (Sheet 1 of 2)

Digit or explanation	Signaling frequencies (Hz)
1	700 + 900
2	700 + 1100
3	900 + 1100
4	700 + 1300
5	900 + 1300
6	1100 + 1300
7	700 + 1500
8	900 + 1500
9	1100 + 1500
0	1300 + 1500
KP-preparation for digits	1100 + 1700
ST-end of pulsing sequence	1500 + 1700
TSP-traffic service position system	900 + 1700

Received MF tones (Sheet 2 of 2)

Digit or explanation	Signaling frequencies (Hz)
TSP2-traffic service position system	1300 + 1700
TSP3-traffic service position system	700 + 1700
Coin collect-coin control	700 + 1100
Coin return-coin control	1100 + 1700
Ringback-coin control	700 + 1700
Code 11-inward operator	700 + 1700
Code 12-delay operator	900 + 1700
KP2-transmit call	1300 + 1700

After the microprocessor decodes the received tone, the microprocessor creates an 8-bit code to identify the tone. The microprocessor sends the code to the trunk logic circuit. The 8-bit code format appears in the following table.

8-bit code format

Explanation	8-bit code
Valid digit-XXXX=received digit in hexadecimal form	1 Y0Y XXXX
Valid pause (no signal)	0 000 0000
Error message-noisy	1 011 001
Error message-large twist	1 011 010
Error message-three frequencies	1 011 100
Error message-indecision or invalid	1 011 111
Error message-no interdigit pause (XXXX=received digit)	1 111 XXXX

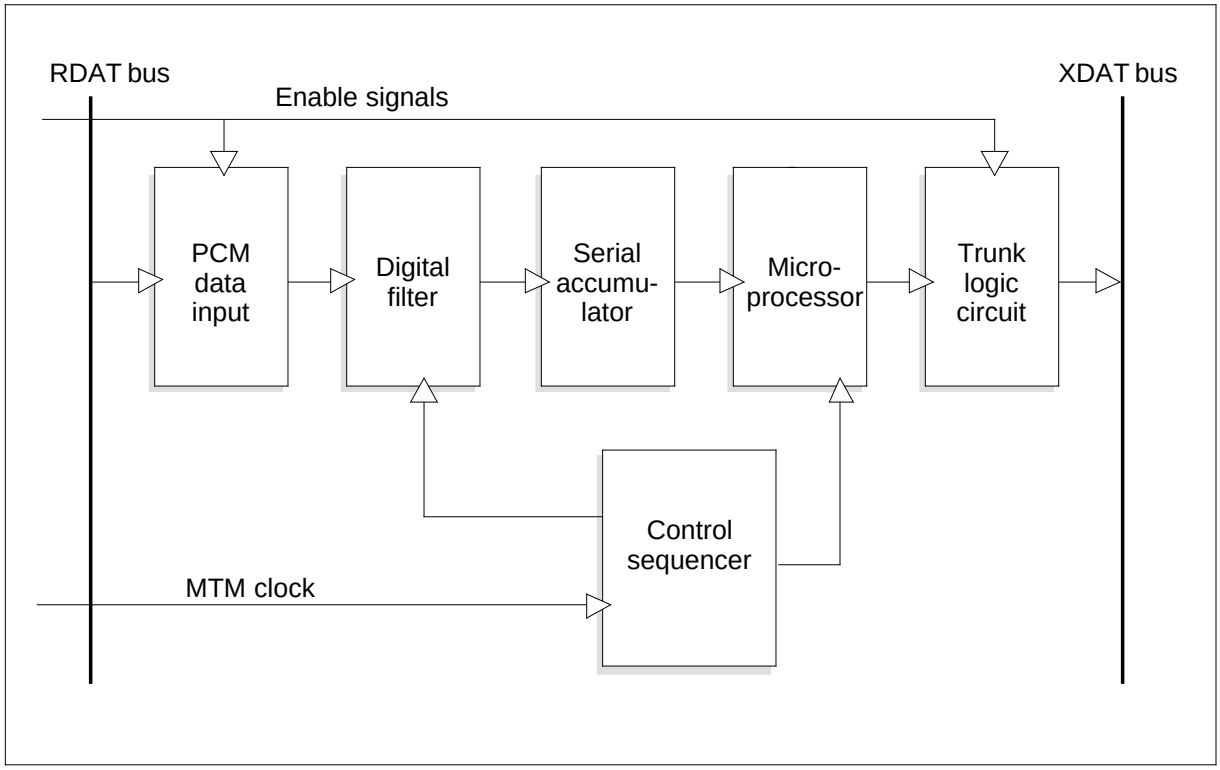
TLC

The TLC sends the 8-bit code to the MTM. The TLC receives the code from the microprocessor. The TLC sends the code over the XDAT bus when the channel of the card is scanned.

The relationship between the functional blocks appears in the following figure.

NT2X48CA (continued)

NT2X48CA functional blocks



Technical data

The information that appears in the following table determines if the NT2X48CA accepts or rejects digits.

Input signal tolerances

Standard	Accept digits	Reject digits
Frequency tolerance	±1.5% + 10 Hz of nominal frequency	±5% of nominal, either frequency
Signal duration	≥20 ms ON	≤10 ms ON
	≥55 ms ON KP	
	≥25 ms OFF	≤10 ms OFF
Input level	-22 to -2 dBm for each frequency	≥-30dBm for each frequency
Twist	≥6 dB between two frequencies	≥16 dB between two frequencies

Dimensions

The dimensions for the NT2X48CA circuit card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 56 mm (2.2 in.)

Power requirements

The power requirements for the NT2X48CA appear in the following table.

Power requirements

Voltage	Current
+12 V	0.01 A
+5 V	2.00 A
-15 V	0.10 A

NT2X48CB

Product description

The NT2X48CB Digitone receiver card receives pulse code modulation (PCM) data from a maximum of four channels. The Digitone receiver card detects standard Digitone tones on these four channels. The card decodes the received tones. The card provides 8-bit binary codes to indicate the tones received.

The card is for μ-law applications in the United Kingdom market.

Location

The NT2X48CB occupies two card positions in a maintenance trunk module (MTM) or a trunk module (TM).

Functional description

A digital filter system detects the Digitone tones in the PCM data received on the receive data (RDAT) bus. The filter sends output of the filter to the microprocessor. The microprocessor converts the received tone information into binary-code format. The microprocessor sends the code information to the MTM on the transmit data (XDAT) bus.

Functional blocks

The NT2X48CB has the following functional blocks:

- PCM data input
- digital filter
- control sequencer
- serial accumulator
- microprocessor
- trunk logic circuit (TLC)

PCM data input

The PCM data input circuit receives the PCM information from the RDAT bus under the control of the enable lines. The PCM data input circuit holds the data in the input circuit until the circuit sends the data to the digital filter.

Digital filter

Data that enters the filter circuit converts to linear form. The circuit filter squares the data to determine the signal strength. The digital filter circuit has eight separate filters. One filter is present for each Digitone tone. The digital filter circuit operates under the control of the sequencer. The filter circuit sends the output to the serial accumulator.

Control sequencer

The control sequencer synchronizes the processing of the tone information with the rate of received PCM information. The sequencer synchronizes with the first received PCM sample. The sequencer synchronizes with each PCM sample that follows. The sequencer output regulates the operation of the digital filter and the microprocessor.

Serial accumulator

The serial accumulator takes samples of the filter circuit output and adds the values of the samples. The accumulator takes two bytes of samples for each of the eight filters. The accumulator adds the values of the samples and sends the results to the microprocessor. The accumulator uses direct memory access (DMA) to place the data directly into the memory of the microprocessor.

Microprocessor

The microprocessor receives the output of the serial accumulator. The microprocessor decodes the meaning of the received tone. The Digitone tones that the microprocessor decodes appear in the following table.

Received MF tones (Sheet 1 of 2)

Digit or explanation	Signaling frequencies (Hz)
1	1209+697
2	1336+697
3	1477+ 697
4	1209+770
5	1336+770
6	1477+770
7	1209+852
8	1336+852
9	1477+852
0	1336+941
×	1209+ 941
#	1477+941
Spare	1633+697

NT2X48CB (continued)

Received MF tones (Sheet 2 of 2)

Digit or explanation	Signaling frequencies (Hz)
Spare	1633+770
Spare	1633+852
Spare	1633+941

After the microprocessor decodes the received tone, the microprocessor creates an 8-bit code to identify the tone. The microprocessor sends the code to the trunk logic circuit. The 8-bit code format appears in the following table.

8-bit code format

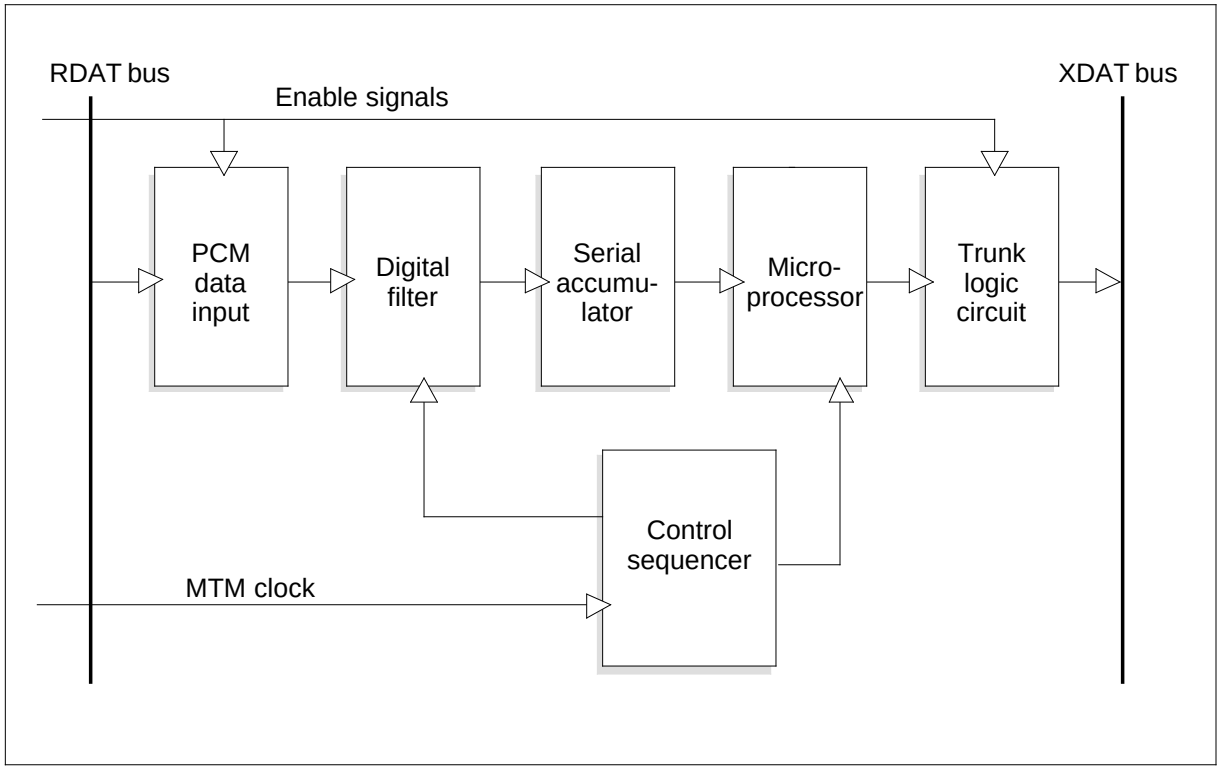
Explanation	8-bit code
Valid digit-XXXX=received digit in hexadecimal form	1 000 XXXX
Valid pause (no signal)	0 000 0000

TLC

The TLC sends the 8-bit code to the MTM. The TLC receives the code from the microprocessor. The TLC sends the code over the XDAT bus when the channel of the card is scanned.

The relationship between the functional blocks appears in the following figure.

NT2X48CB functional blocks



Technical data

The information in the following table determines if the NT2X48CB accepts or rejects digits.

Input signal tolerances (Sheet 1 of 2)

Standard	Accept digits	Reject digits
Frequency tolerance	±1.5% + 10 Hz of nominal frequency	±3.5% of nominal, either frequency
Signal duration	≥40 ms ON	≤15 ms ON
	≥20 ms OFF	≤20 ms OFF
	≥85 ms ON plus OFF	

NT2X48CB (end)

Input signal tolerances (Sheet 2 of 2)

Standard	Accept digits	Reject digits
Input level	-24 to 0 dBm for each frequency	≥-32 dBm for each frequency
Twist	-8 dB to 4 dB high frequency to low frequency	≥16 dB high frequency to low frequency

The NT2X48CB detects with a low error rate. The NT2X48CB detects low-level Digitone tones in gaussian and impulse noise. The card detects tones in signal echoes delayed a maximum of 20 ms. The card detects tones of signal echoes reduced in level a minimum of 10 dB from the original signal.

Dimensions

The dimensions for the NT2X48CB circuit card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 56 mm (2.2 in.)

Power requirements

The power requirements for the NT2X48CB appear in the following table.

Power requirements

Voltage	Current
+12 V	0.01 A
+5 V	2.00 A
-15 V	0.10 A

NT2X48CC

Product description

The NT2X48CA A-law dual-tone multifrequency (DTMF) receiver receives pulse code modulation (PCM) tones from four channels at the same time. The receiver detects standard DTMF tones on these channels. The card decodes the received tones and provides 8-bit binary codes to indicate the tones received.

The card is for A-law applications in the United Kingdom.

Location

The NT2X48CC occupies two card positions in a maintenance trunk module (MTM) or a trunk module (TM).

Functional description

A digital filter system detects the DTMF tones in the PCM data received on the receive data (RDAT) bus. The filter sends output of the filter to the microprocessor. The microprocessor converts the received tone information into binary-code format. The microprocessor sends the code information to the MTM on the transmit data (XDAT) bus.

Functional blocks

The NT2X48CC has the following functional blocks:

- PCM data input
- digital filter
- control sequencer
- serial accumulator
- microprocessor
- trunk logic circuit (TLC)

PCM data input

The PCM data input circuit receives the PCM information from the RDAT bus under the control of the enable lines. The PCM data input circuit holds the data in the input circuit until the circuit sends the data to the digital filter.

Digital filter

Data that enters the filter circuit converts to linear form. The circuit filter squares the data to determine the signal strength. The digital filter circuit has eight separate filters. One filter is present for each DTMF tone. The digital filter circuit operates under the control of the sequencer. The filter circuit sends the output to the serial accumulator.

NT2X48CC (continued)

Control sequencer

The control sequencer synchronizes the processing of the tone information with the rate of received PCM information. The sequencer synchronizes with the first received PCM sample. The sequencer synchronizes with each PCM sample that follows. The sequencer output regulates the operation of the digital filter and the microprocessor.

Serial accumulator

The serial accumulator takes samples of the filter circuit output and adds the values of the samples. The accumulator takes two bytes of each channel for each of the eight filters. The accumulator adds the values of the 64 samples and sends the results to the microprocessor. The accumulator uses direct memory access (DMA) to place the data directly into the memory of the microprocessor.

Microprocessor

The microprocessor receives the output of the serial accumulator. The microprocessor decodes the meaning of the received tone. The DTMF tones that the microprocessor decodes appear in the following table.

Received DTMF tones (Sheet 1 of 2)

Digit or explanation	Signaling frequencies (Hz)
1	1209+697
2	1336+697
3	1477+ 697
4	1209+770
5	1336+770
6	1477+770
7	1209+852
8	1336+852
9	1477+852
0	1336+941
×	1209+ 941
#	1477+941
Spare	1633+697

Received DTMF tones (Sheet 2 of 2)

Digit or explanation	Signaling frequencies (Hz)
Spare	1633+770
Spare	1633+852
Spare	1633+941

After the microprocessor decodes the received tone, the microprocessor creates an 8-bit code to identify the tone. The microprocessor sends the code to the trunk logic circuit. The 8-bit code format appears in the following table.

8-bit code format

Explanation	8-bit code
Valid digit-XXXX=received digit in hexadecimal form	1 000 XXXX
Valid pause (no signal)	0 000 0000

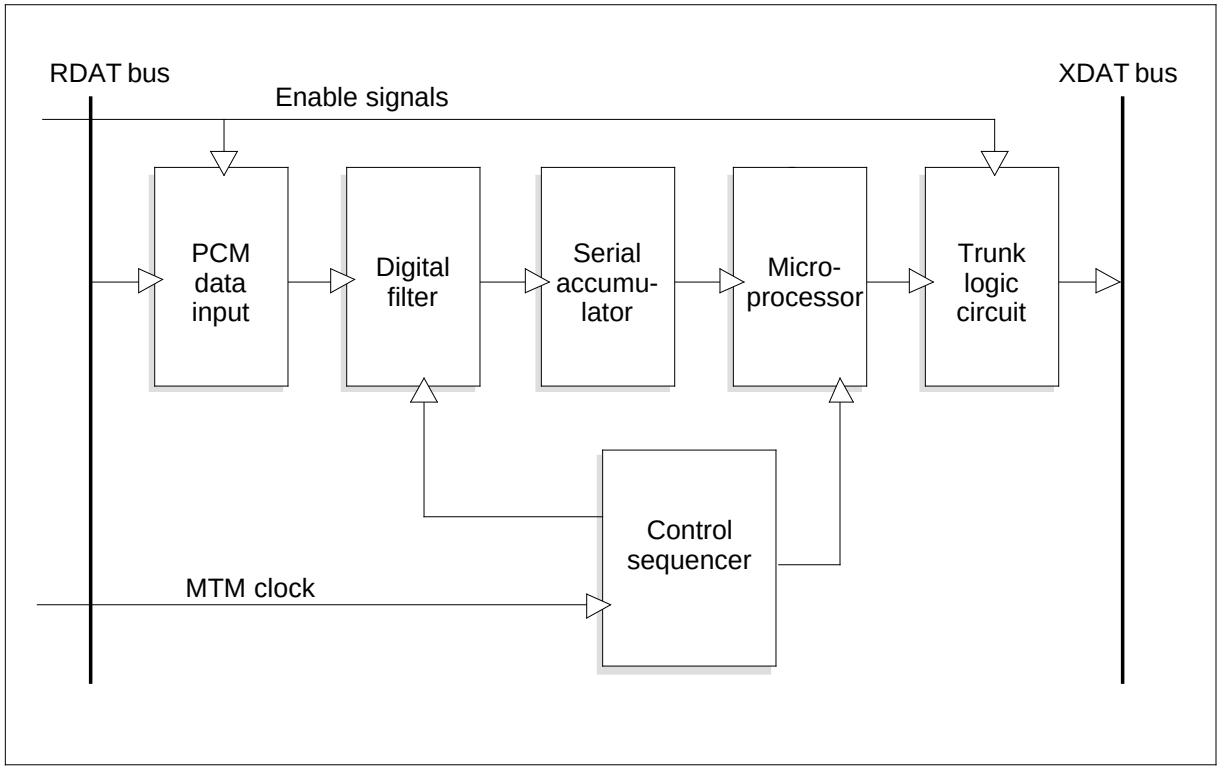
Trunk logic circuit

The TLC sends the 8-bit code to the MTM. The TLC receives the code from the microprocessor. The TLC sends the code over the XDAT bus when the channel of the card is scanned.

The relationship between the functional blocks appears in the next figure.

NT2X48CC (continued)

NT2X48CC functional blocks



Technical data

The information in the following table determines if the NT2X48CC accepts or rejects digits.

Input signal tolerances (Sheet 1 of 2)

Standard	Accept digits	Reject digits
Frequency tolerance	±1.5% + 10 Hz of nominal frequency	±3.5% of nominal frequency
Signal duration	≥40 ms ON	≤15 ms ON
	≥20 ms OFF	≤15 ms OFF
	≥85 ms ON plus OFF	

Input signal tolerances (Sheet 2 of 2)

Standard	Accept digits	Reject digits
Input level	-24 to -3 dBm for each frequency	≤-32 dBm for each frequency
Twist	-8 to 4 dB high frequency to low frequency	≤16 dB high frequency to low frequency

Dimensions

The dimensions for the NT2X48CC circuit card are as follows:

- height: 353 mm (13.9 in.)
- depth: 277 mm (10.9 in.)
- width: 56 mm (2.2 in.)

Power requirements

The power requirements for the NT2X48CC appear in the following table.

Power requirements

Voltage	Current
+12 V	0.01 A
+5 V	2.00 A
-15 V	0.10 A

NT2X50AB

Product description

The NT2X50AB minibar driver card controls the operation of an NT2X46 metallic test access (MTA) card. The NT2X50AB and the MTA card operate as part of the line maintenance facility for the DMS-100 and DMS-100/200 systems.

Location

The card occupies one card position in a maintenance trunk module (MTM) or a remote service module (RSM).

Functional description

The NT2X50AB receives digital instructions from the MTM or RSM. The NT2X50AB decodes the instructions and sends signals to the MTA card. The MTA card uses the signals to operate select and hold magnets.

Functional blocks

The NT2X50AB has of the following functional blocks:

- two trunk logic circuits (TLC)
- hold magnet relay drivers
- hold magnet relay switches
- multiplexer (MUX)
- select magnet relay drivers
- select magnet relay switches
- test detector

TLC

The trunk logic circuit (TLC) is responsible for communications between the card and the MTM or RSM. The MTM sends instructions to operate or release the magnets. The TLC receives the instructions and sends the instructions to the relay drivers. Two TLCs are available. The TLC-A accepts instructions for the hold magnets. The TLC-B accepts instructions for the select magnets. The TLC-A can return a signal to the MTM that indicates the status of the hold magnets. The TLC-B can return a signal that checks that a path completed through the MTA.

Hold magnet relay drivers

The hold magnet relay drivers receive instructions from the TLC-A to operate or release specified hold magnets. The drivers activate the relay switches. When a driver receives an instruction to activate a magnet, the driver activates that magnet. The magnet is active until the driver receives an instruction to

deactivate the magnet. Even if the TLC-A requests the release of the magnet, the magnet remains active until the magnet is deactivated.

Hold magnet relay switches

The relay drivers activate the hold magnet relay switches to operate or release specified magnets in the MTA. The switches connect to 20 leads. The leads connect to the hold magnets.

MUX

The TLC-A receives a request from the MTM to check the status of a hold magnet. The TLC sends a signal to the MUX. The MUX checks the status of the monitor contacts of the relay. The MUX returns the status to the TLC. The MTM reads the results from the TLC to check valid relay operation.

Select magnet relay drivers

The select magnet relay drivers receive instructions from TLC-B to operate or release specified select magnets. The drivers activate the relay switches. When a driver receives instruction to activate a magnet, that magnet stays active. For deactivation, the TLC-B instructs the driver to release the magnet. The TLC-B does not have to deactivate select magnets.

Select magnet relay switches

The relay drivers activate the select magnet relay switches to operate or release specified select magnets in the MTA. The switches connect to 10 leads. The 10 leads connect to the hold magnets.

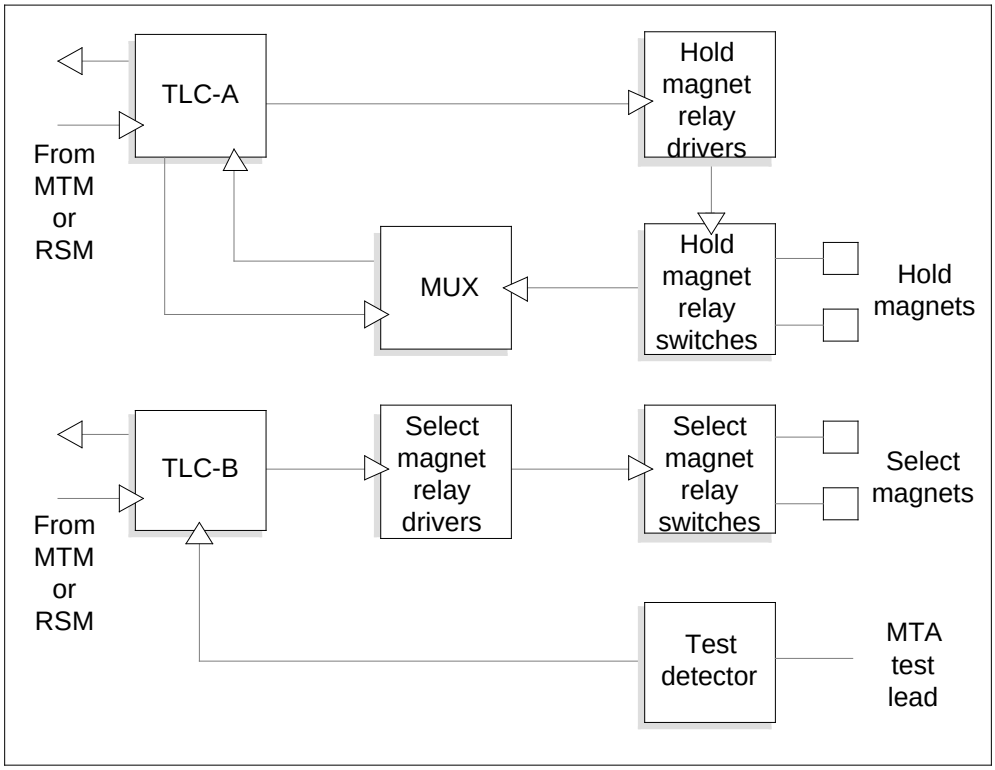
Test detector

The test detector checks that a path completed through the MTA when the hold or select magnets are operated. When a path completes, the MTA produces a -48V pulse. The detector detects the pulse on the MTA test lead and sends a lower voltage pulse to the TLC-B. The MTM reads the pulse to check that the path is complete in the MTA.

The relationship between the functional blocks appears in the following figure.

NT2X50AB (continued)

NT2X50AB functional blocks



Technical data

Dimensions

Dimensions of the NT2X50AB circuit card are as follows.

- height: 317 mm (12.5 in.)
- depth: 254 mm (10.0 in.)

Power requirements

The current and power requirements of the card appear in the following table. Standard conditions are the five MTA magnets in operation.

Current requirements (Sheet 1 of 2)

Voltage	Maximum current	Normal current	Idle current
+24 V	0.50 A	0.17 A	0.00 A
+12 V	0.01 A	0.01 A	0.01 A

Current requirements (Sheet 2 of 2)

Voltage	Maximum current	Normal current	Idle current
+5 V	0.12 A	0.08 A	0.08 A
-15 V	0.01 A	0.01 A	0.01 A

Power requirements

Voltage	Maximum power	Normal power	Idle power
+24 V	12.0 W	4.10 W	0.00 W
+12 V	0.15 W	0.15 W	0.15 W
+5 V	0.60 W	0.40 W	0.40 W
-15 V	0.15 W	0.15 W	0.15 W

NT2X52AD

Description

The NT2X52AD trunk module 8-wire with access shelf goes in an NT0X46AB trunk module equipment frame. The DMS-300 offices use the trunk module. This trunk module has leads to allow connection to a test access network (TAN). These leads allow connection of external test equipment to trunk facilities and circuits with a metallic path through the TAN.

The NT2X52AD is different from the special function NT2X52AG TM8-type module in DMS-100 PBX and common carrier applications. The NT2X52AR replaces this shelf in Canadian applications.

Parts

The TM8 shelf has optional trunk cards and the following components:

- NT0X70AA—trunk module (TM) processor and memory card
- NT2X09AA—power converter card
- NT2X45AB—TM interface card
- NT2X53AA—TM control card
- NT2X59AB—group CODEC DMS-300 (Teleglobe)

Design

The parts appear in the following table.

NT2X52AD parts (Sheet 1 of 2)

PEC	Slot	Description
Varies	5-19F	*Optional trunk cards* You can install a maximum of 15 optional trunk cards to meet traffic requirements. These circuit cards can be conference circuits, CCITT trunk circuits, communication test line circuits, CAMA position signaling circuits. These cards can also be digital 4-channel multifrequency receiver circuits.
NT0X70AA	2F	*Trunk module processor and memory card* The TM processor and memory card controls or performs all the operations in the TM8. The card has a microprocessor, a ROM, and two RAMs. One RAM stores programs and one RAM stores operational information. Operational information is pulse code modulated (PCM) channel-to-trunk connection assignments. This card generates clock signals, checks parity, and synchronizes the activities of the module circuits.

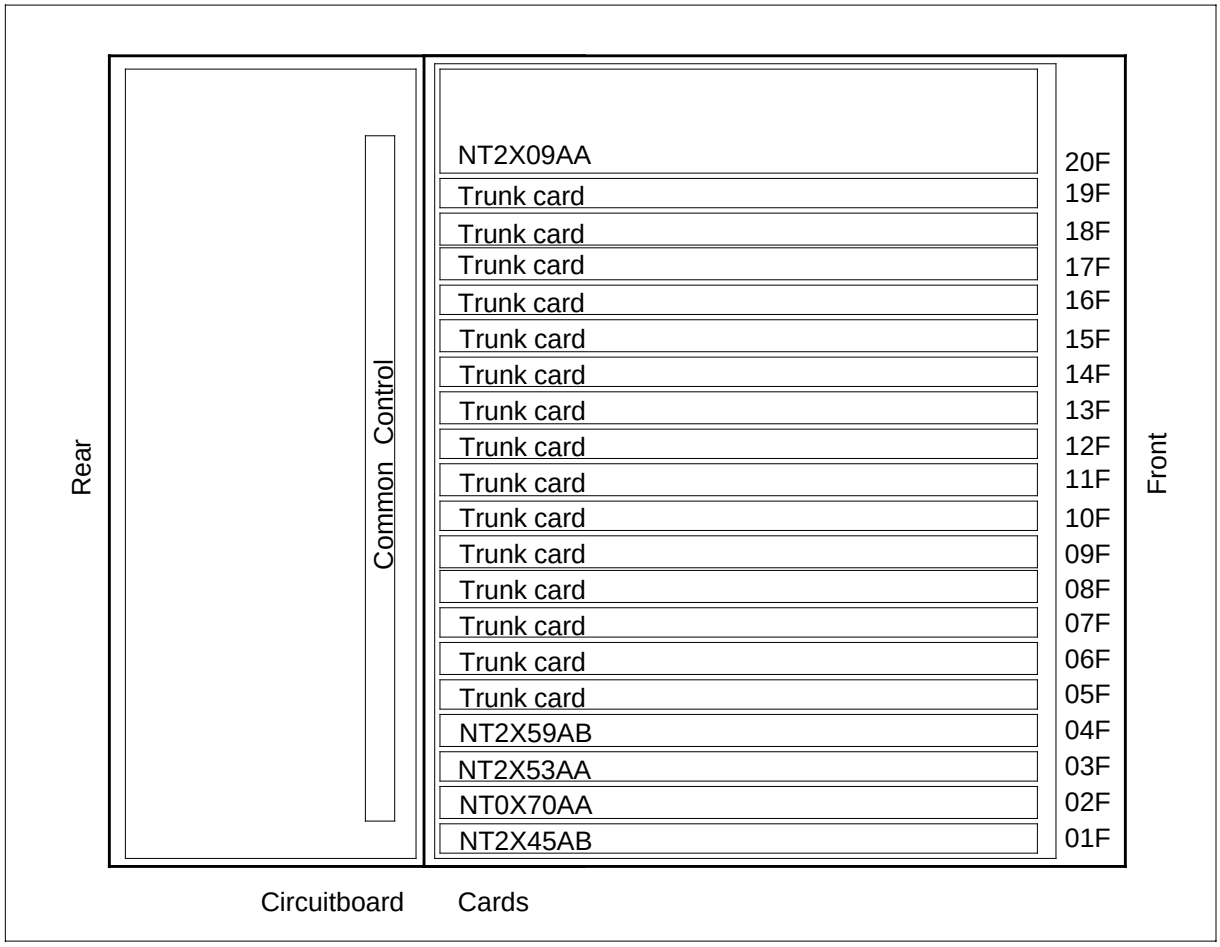
NT2X52AD parts (Sheet 2 of 2)

PEC	Slot	Description
NT2X09AA	20F	*Power converter card* The power converter card converts the dc voltage of -48V to the dc operating voltages (-5, -15, +5, +12, and +24V). These voltages are required in the TM8. The card includes a low-voltage monitor circuit, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X45AB	1F	*Trunk module interface card* The TM interface card provides a pair of 2-way interfaces between the two transmission paths of each network plane and the TM8. The TM interface card includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The TM aligns and reformats PCM samples on the transmit and receive paths. The TM separates control messages from the speech samples and sends the messages to the TM control card.
NT2X53AA	3F	*Trunk module control card* The TM control card provides a pair of 2-way interfaces between the two transmission paths of each network plane and the TM8. The control card includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The control card aligns and reformats PCM samples on the transmit and receive paths. The control card separates control messages from the speech samples and sends the messages to the control circuit. The control circuit organizes the flow of incoming and outgoing messages. The control circuit includes three controllers. The three controllers handle trunk, network, and integrity messages. The control circuit generates enabling signals for the 30 separate trunk interfaces. The control circuit trades data with the trunk interface cards and routes speech samples to the NT2X59AB card. Data and address buses transfer data between the TM control card and the processor and memory card.
NT2X59AB	4F	*Group CODEC DMS-300 (Teleglobe) card* A DMS-300 peripheral module uses this card. The NT2X59AB card changes analog samples into PCM code words. The card converts PCM word streams into analog samples. The card routes speech samples to the correct trunk interface card. The card includes a ROM that stores digital tones for dialing and signaling.

NT2X52AD (end)

The design of the NT2X52AD appears in the following figure.

NT2X52AD parts



NT2X52AE

Description

The NT2X52AE two-wire trunk module (TM2) functions as an interface. The TM2 acts as an interface between a maximum of 30 analog trunk circuits and several components of the digital switching system. These components are 32-channel, time-division, pulse-code-modulated (PCM) speech and control streams. The TM2 converts analog trunk speech and signaling information to and from a 2.56 Mbps stream.

The TM2 is mounted in a single-bay TM equipment (TME) or digital carrier equipment (DCE) frame. The TM2 accommodates many two-wire trunk circuits, like multi-frequency (MF) and dial pulse (DP) receivers. The TM2 consists of a control section, a power converter and interchangeable trunk interfaces. The control section includes the TM interface, TM processor, TM control, and group coder-decoder (CODEC) and tone circuit packs (CP). The control circuit card handles the data processing, control, and group CODEC and tone functions. The control circuit card is the interface between the DS30 speech links and the two planes of the network.

The three types of data exchange between the TM2 and the associated switching network. These data include messages between the control module (CM) and the TM2 control circuits, supervisory messages between connected TMs, and PCM speech samples.

The three types of data transfer in a time frame of 32 channel times. The trunk circuits send messages between the TM2 and the CM over signaling and control channels. Supervisory messages between connected TMs use the channel supervisory bit in the associated speech channel. Each trunk circuit in the TM2 is scanned one time for each 40 frames, at 5 ms intervals. The trunk circuits send or receive data that operate or release signal distribution points.

The TM2 separates control messages from the PCM speech samples. The TM2 aligns and reformats data on the receive channels from the two network module planes. The PCM receive signals change to pulse-amplitude-modulated (PAM) signals. Digital tones are added as necessary. The PAM signals samples are used to reconstruct the original analog signals. The trunk circuits send these signals to the trunk transmission facilities.

On the transmit side, analog speech signals from the trunk facilities change to PAM samples. The PAM samples change to PCM signals. Digital tones are added to the PCM signals, if necessary. The PCM samples and associated data are combined and reformatted for a data stream on the speech link transmit path. Two data buses, XDAT and RDAT, transfer transmit and receive data, in that order.

NT2X52AE (continued)

The TM2 also includes looparound facilities for maintenance and troubleshooting. Digital looparound links the RDAT and XDAT buses. Analog looparound links the XPAM and RPAM buses. Looparound is provided for each trunk interface circuit.

Parts

The TM2 contains trunk interface CPs and the following parts:

- NT0X70AA—TM processor and memory CP
- NT2X09AA—Power converter
- NT2X45AB—TM interface CP
- NT2X53AA—TM control CP
- NT2X59AA—Group CODEC and tone CP

Design

The following table describes the design of the NT2X52AE.

NT2X52AE parts (Sheet 1 of 3)

PEC	Slot	Description
—	5F-19F	*Trunk interface circuit packs* The trunk interface CPs are the interface between analog transmission and signaling trunk facilities and the digital multiplex circuits in the TM. The number and type of CPs in a given module depend on the type of trunk facilities. Some trunk interface CPs have two trunk interface circuits. Others have only one. Each interface contains a sampling gate for speech processing, and signaling circuits. Each interface must contain buffers for signaling data, looparound test circuits, and card-type identification.
NT0X70AA	2F	*Trunk module processor and memory circuit pack* The TM processor and memory CP controls or performs the operations in the TM2. The TM2 contains a microprocessor, a ROM, and two RAM. One RAM stores programs and the other RAM stores operational information (PCM-channel-to-trunk connection assignments). The CP performs the processing functions for the TM2. The CP generates clock signals, checks parity, and synchronizes the activities of the module circuits.

NT2X52AE parts (Sheet 2 of 3)

PEC	Slot	Description
NT2X09AA	20F	*Power converter* The power converter converts the -48V dc to the operating voltages (-5V, -15V, +5V, +12V, and +24V dc) that the circuits in the TM2 require. The power converter includes a low-voltage monitor circuit, and overvoltage and overcurrent protection. The power converter includes faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X45AB	1F	*Trunk module interface circuit pack* The TM trunk interface CP provides a pair of two-way interfaces. These interfaces are between the two transmission paths of each network plane and the TM. The TM trunk interface CP aligns and reformats PCM samples on the transmit and receive paths. The TM trunk interface includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The TM trunk interface separates control messages from the speech samples and sends them to the TM control CP.

NT2X52AE (continued)

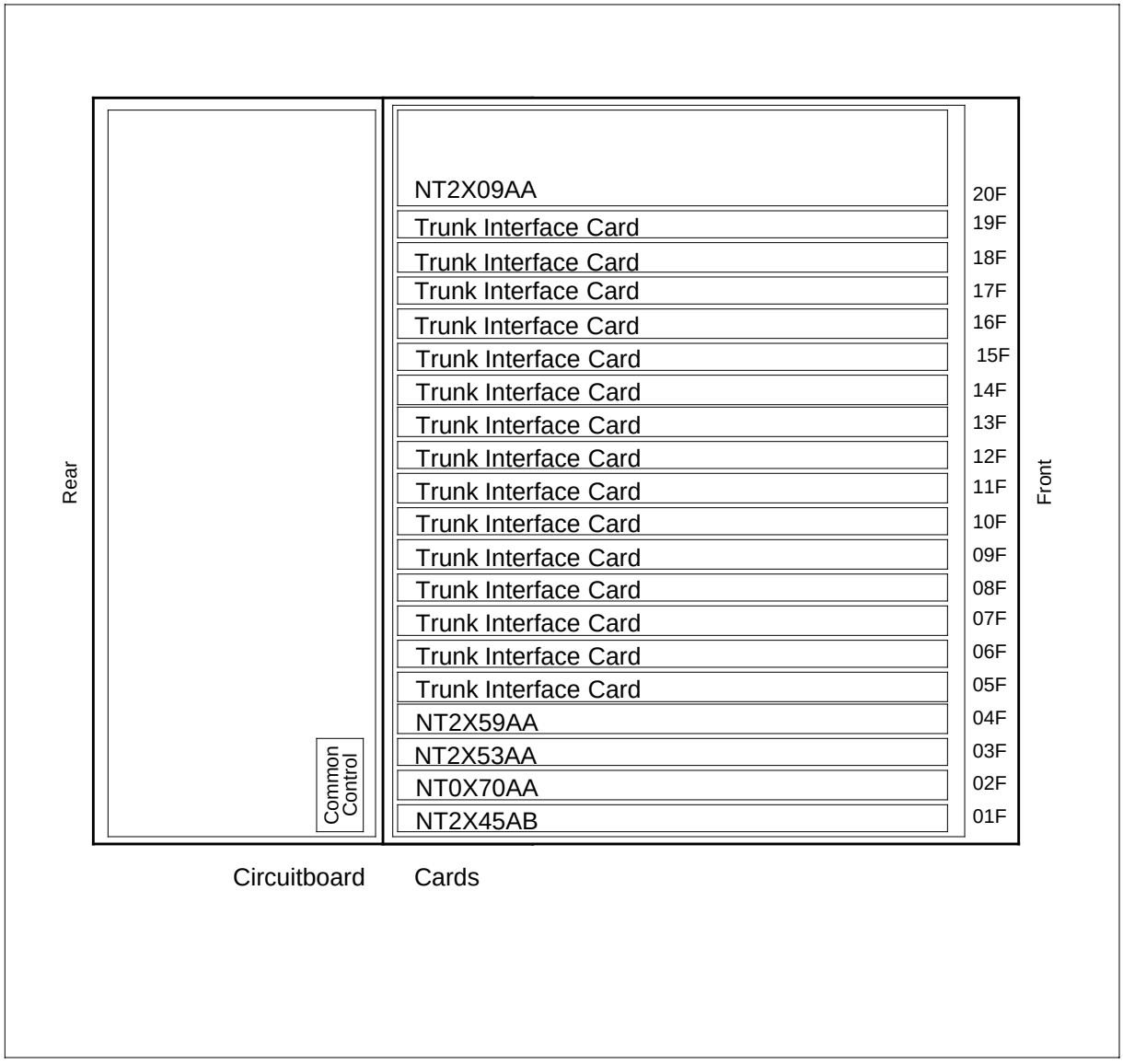
NT2X52AE parts (Sheet 3 of 3)

PEC	Slot	Description
NT2X53AA	3F	*Trunk module control circuit pack* The TM control CP provides a pair of two-way interfaces between the two transmission paths of each network plane and the TM2. This CP aligns and reformats PCM samples on the transmit and receive paths. The CP separates control messages from the speech samples and sends the messages to the control circuit. This CP includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The control circuit organizes the flow of incoming and outgoing messages. This circuit includes three controllers that handle trunk, network, and integrity messages. The circuit generates enabling signals for the 30 trunk interfaces. The circuit also exchanges data with the trunk interface CPs and routes speech samples to the group CODEC and tone CP. Data transfer between the TM control CP and the processor and memory CP through the data and address buses. The processor and memory circuit controls or performs operations in the TM2. The processor contains a microprocessor, a ROM, and two RAMs. One RAM stores programs. The other RAM stores operational information (PCM-channel-to-trunk connection assignments). The circuit performs the processing functions for the TM2. This circuit generates clock signals, checks parity, and synchronizes the activities of the module circuits. The group CODEC and tone CP changes analog samples to PCM code words. The group CODEC converts PCM word streams to analog samples. The group CODEC routes speech samples to the correct trunk interface CP, and includes a ROM. This ROM stores digital tones for dialing and signaling.
NT2X59AA	4F	*Group coder-decoder and tone circuit pack* The group CODEC and tone CP changes analog samples to PCM code words. The group CODEC converts PCM word streams to analog samples. The group routes speech samples to the correct trunk interface CP, and includes a ROM. This ROM stores digital tones for dialing and signaling.

The following figure describes the design of the NT2X52AE.

NT2X52AE (end)

NT2X52AE parts



NT2X52AF

Description

The NT2X52AF four-wire trunk module (TM4) is an interface. The TM4 is an interface between a maximum of 30 analog trunk circuits and several components of the digital switching system. These components are the 32-channel, time-division, pulse-code-modulated (PCM) speech and control streams. The TM4 converts analog trunk speech and signaling information to and from a 2.56-Mbps stream.

The TM4 is mounted in a single-bay trunk module equipment (TME) or digital carrier equipment (DCE) frame. The TM4 accommodates many four-wire trunk circuits, like multifrequency (MF) and dial pulse (DP) receivers. The TM4 consists of a control circuit card, a power converter, and interchangeable trunk interfaces. The control circuit card is the interface between the DS30 speech links and the two planes of the network. The circuit card is responsible for data processing, control, and group coder-decoder (CODEC) functions.

Three types of data exchange between the TM4 and the associated switching network. These data are messages between the control module (CM) and the TM4 control circuits, supervisory messages between connected trunk modules (TM), and PCM speech samples.

The three types of data transfer in a time frame with 32 channel times. The system sends messages between the TM4 and the CM over signaling and control channels. Supervisory messages between TMs that connect use the channel supervisory bit in the associated speech channel. Each trunk circuit in the TM is scanned one time each 40 frames at 5-ms intervals. The circuits send or receive data that operate or release signal distribution points.

The TM4 separates control messages from the PCM speech samples. The TM4 aligns and reformats data on the receive channels from the two network module planes. The PCM receive signals change to pulse-amplitude-modulated (PAM) signals. Digital tones are added as necessary. The PAM signals samples reconstruct the original analog signals. The system sends the signals to the trunk transmission facilities.

On the transmit side, analog speech signals from the trunk facilities change to PAM samples. The PAM samples change to PCM signals. Digital tones are added to the PCM signals. The PCM samples and associated data are combined and reformatted in a data stream on the speech link transmit path. Two data buses, XDAT and RDAT, transfer, transmit and receive data, in that order.

The TM4 includes looparound facilities for maintenance and troubleshooting. Digital looparound links the RDAT and XDAT buses. Analog looparound links

the XPAM and RPAM buses. Looparound is provided for each trunk interface circuit.

Parts

The TM4 contains trunk interface circuit packs (CP), the NT2X09AA power converter, and the TM CP.

Design

The following table describes the design of the NT2X52AF.

NT2X52AF parts (Sheet 1 of 2)

PEC	Slot	Description
—	5F-19F	*Trunk interface circuit packs* The trunk interface CPs are the interface between analog transmission and signaling trunk facilities and the digital multiplex circuits in the TM. The number and type of CPs in a given module depend on the type of trunk facilities. Some trunk interface CPs have two trunk interface circuits. Other CPs have one trunk interface circuit. Each interface contains a sampling gate for speech processing and signaling circuits. Each interface also contains buffers for signaling data, looparound test circuits, and card-type identification.
NT0X70AA	2F	*Trunk module processor and memory circuit pack* The TM processor and memory CP controls or performs operations in the TM2. The processor contains a microprocessor, a ROM, and two RAMs. One RAM stores programs. The other RAM stores operational information (PCM-channel-to-trunk connection assignments). The CP performs the processing functions for the TM2. This CP generates clock signals, checks parity, and synchronizes the activities of the module circuits.
NT2X09AA	20F	*Power converter* The power converter converts the -48V dc to the operating voltages (-5V, -15V, +5V, +12V, and +24V dc) that the circuits in the TM2 require. The power converter includes a low-voltage monitor circuit, and overvoltage and overcurrent protection. The converter also includes faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.

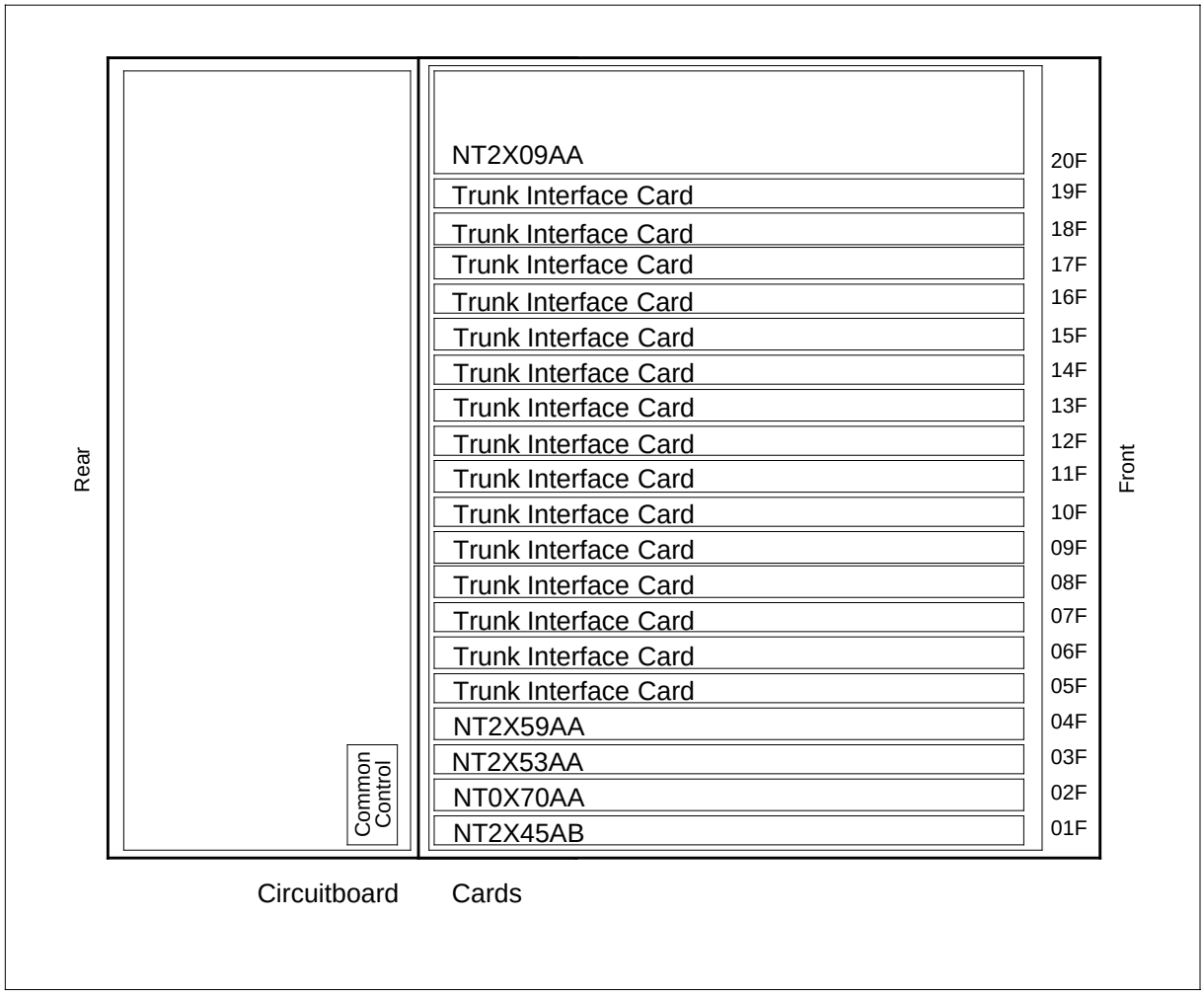
NT2X52AF (continued)

NT2X52AF parts (Sheet 2 of 2)

PEC	Slot	Description
NT2X45AB	1F	*Trunk module interface circuit pack* The TM trunk interface CP provides a pair of two-way interfaces between the two transmission paths of each network plane and the TM. The TM trunk interface CP aligns and reformats PCM samples on the transmit and receive paths. The CP includes message registers as well as bit and channel timing, parity-checking, and data-reformatting circuits. The TM also separates control messages from the speech samples and sends the messages to the TM control CP.
NT2X53AA		*Trunk module control circuit pack* The TM control CP provides a pair of two-way interfaces. The interfaces are between the two transmission paths of each network plane and the TM2. This CP aligns and reformats PCM samples on the transmit and receive paths. The CP also separates control messages from the speech samples, and sends the messages to the control circuit. This CP includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The control circuit organizes the flow of incoming and outgoing messages. This circuit includes three controllers that handle trunk, network, and integrity messages. The circuit generates enabling signals for the 30 trunk interfaces. The circuit exchanges data with the trunk interface CPs and routes speech samples to the group CODEC and tone CP. Data transfers between the TM control CP and the processor and memory CP through the data and address buses. The processor and memory circuit controls or performs operations in the TM2. The processor contains a microprocessor, a ROM, and two RAMs. One RAM stores programs. The other RAM stores operational information (PCM-channel-to-trunk connection assignments). The circuit performs the processing functions for the TM2. This circuit generates clock signals, checks parity, and synchronizes the activities of the module circuits.
NT2X59AA	4F	*Group coder-decoder and tone circuit pack* The group CODEC and tone CP changes analog samples to PCM code words. The group CODEC converts PCM word streams to analog samples. The group CODEC routes speech samples to the appropriate trunk interface CP. The group includes a ROM that stores digital tones for dialing and signaling.

The following figure displays the design of the NT2X52AF.

NT2X52AF parts



NT2X52AM

Description

The two-wire trunk module (TM2) is an interface. The TM2 is an interface between a maximum of 30 analog trunk circuits and components of the digital switching system. These components include the 32-channel, time-division, pulse-code-modulated (PCM) speech and control streams. The TM2 converts analog trunk speech and signaling information to and from a 2.56-Mbps stream.

The TM2 is mounted in a single-bay trunk module equipment (TME) or digital carrier equipment (DCE) frame. The TM2 accommodates many two-wire trunk circuits, like multifrequency (MF) and dial pulse (DP) receivers. The TM2 consists of an NT4X65AB control circuit pack (CP), an NT2X09AA power converter, and interchangeable trunk interfaces. The control CP functions as the interface between the DS30 speech links and the two planes of the network. The TM2 is responsible for data processing, control, and group coder-decoder (CODEC) and tone functions.

Three types of data exchange between the TM2 and the associated switching network. These data are messages between the control module (CM) and the trunk module (TM) control card, supervisory messages between connected TMs, and PCM speech samples.

The three types of data transfer in a time period of 32 channel times. The system sends messages between the TMs and the CM over signaling and control channels. Supervisory messages between connected TMs use the channel supervisory bit in the associated speech channel. Each trunk circuit in the TM2 is scanned one time each 40 frames, at 5-ms intervals. The trunk circuit sends or receives data that operate or release signal distribution points.

The TM2 separates control messages from the PCM speech samples. The TM2 aligns and reformats data on the receive channels from the two network module planes. The PCM receive signals convert to pulse-amplitude-modulated (PAM) signals. Digital tones are added as necessary. The PAM signals samples reconstruct the original analog signals. These signals are sent to the trunk transmission facilities.

On the transmit side, analog speech signals from the trunk facilities change to PAM samples. These signals change to PCM signals. Digital tones are added to the PCM signals. The PCM samples and associated data are combined and reformatted to a data stream on the speech link transmit path. Two data buses, XDAT and RDAT, transfer transmit and receive data, in that order.

The TM2 includes looparound facilities for maintenance and troubleshooting. Digital looparound links the RDAT and XDAT buses. Analog looparound links

the XPAM and RPAM buses. Looparound is provided for each trunk interface circuit.

Parts

The TM2 contains trunk interface CPs, the NT2X09AA power converter, and the NT4X65AB TM control CP.

Design

The following table describes the design of the NT2X52AM.

NT2X52AM parts (Sheet 1 of 2)

PEC	Slot	Description
—	5F-19F	*Trunk interface circuit packs* The trunk interface CPs are the interface between analog transmission and signaling trunk facilities and the digital multiplex circuits in the TM. The number and type of CPs in a given module depend on the type of trunk facilities. Some trunk interface CPs have two trunk interface circuits. Other trunk interface CPs have one trunk interface circuits. Each interface contains a sampling gate for speech processing, and signaling circuits. Each interface also contains buffers for signaling data, looparound test circuits, and card-type identification.
NT0X70AA	2F	*Trunk module processor and memory circuit pack* The TM processor and memory CP controls or performs operations in the TM2. The processor contains a microprocessor, a ROM, and two RAMs. One RAM stores programs. The other RAM stores operational information (PCM-channel-to-trunk connection assignments). The CP performs the processing functions for the TM2. This CP generates clock signals, checks parity, and synchronizes the activities of the module circuits.
NT2X09AA	20F	*Power converter* The power converter converts the -48Vdc to the operating voltages (-5V, -15V, +5V, +12V, and +24V dc) that the circuits in the TM2 require. The converter includes a low-voltage monitor circuit, overvoltage and overcurrent protection. The converter also includes faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.

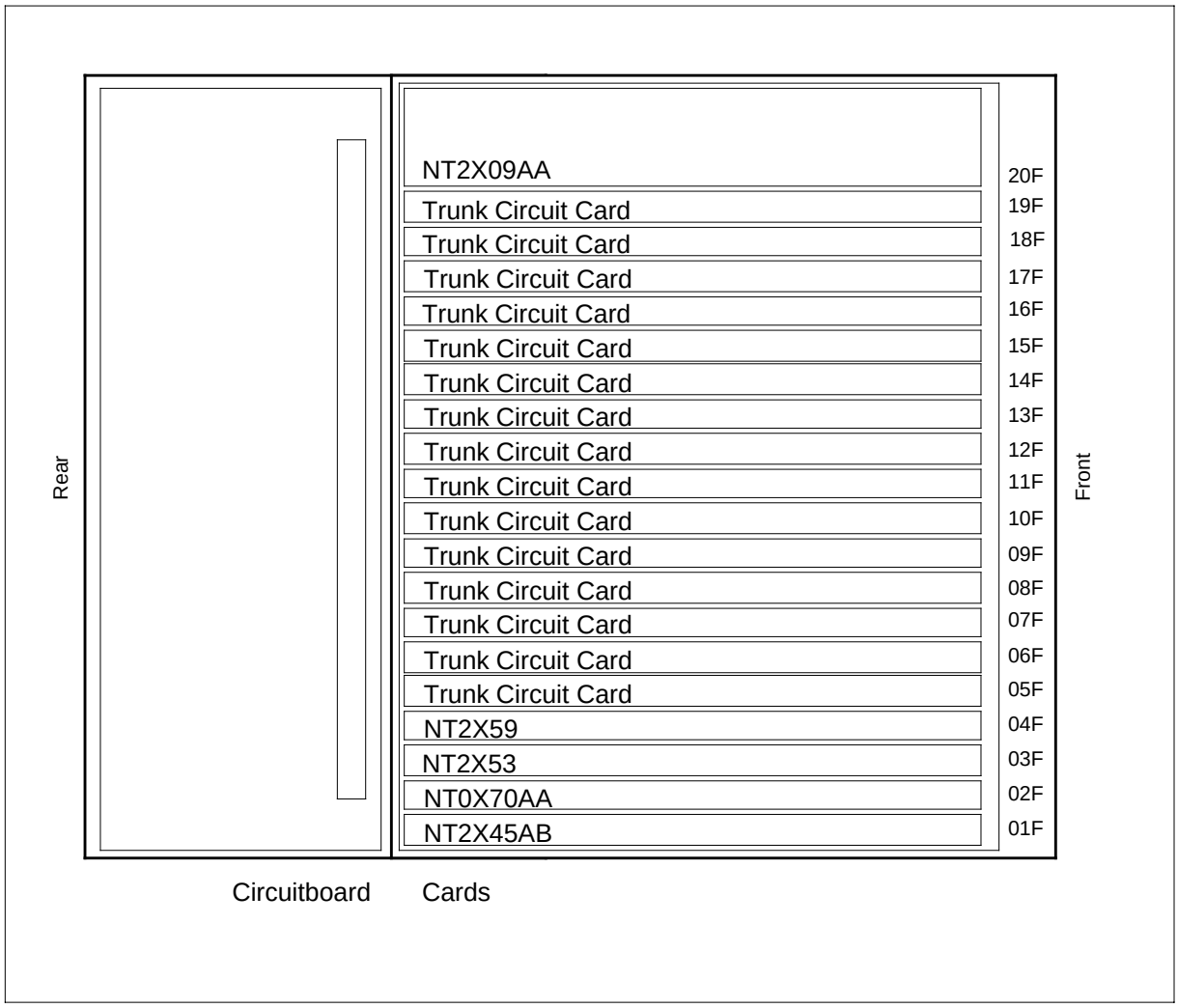
NT2X52AM (continued)

NT2X52AM parts (Sheet 2 of 2)

PEC	Slot	Description
NT2X45AB	1F	*Trunk module interface circuit pack* The TM trunk interface CP provides a pair of two-way interfaces between the two transmission paths of each network plane and the TM. The TM trunk interface CP aligns and reformats PCM samples on the transmit and receive paths. The CP includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The CP also separates control messages from the speech samples. The CP sends the messages to the TM control CP.
NT2X53AA	3F	*Trunk module control circuit pack* The TM control CP provides a pair of two-way interfaces between the two transmission paths of each network plane and the TM2. The CP aligns and reformats PCM samples on the transmit and receive paths. The CP separates control messages from the speech samples, and sends the messages to the control circuit. The CP includes message registers as well as bit and channel timing, parity-checking, and data-reformatting circuits. The control circuit organizes the flow of incoming and outgoing messages. This circuit includes three controllers that handle trunk, network, and integrity messages. The circuit generates enabling signals for the 30 trunk interfaces. The circuit exchanges data with the trunk interface CPs. The circuit routes speech samples to the group CODEC and tone CP. Data transfers between the TM control CP and the processor and memory CP through the data and address buses. The processor and memory circuit controls or performs operations in the TM2. The processor contains a microprocessor, a ROM, and two RAMs. One RAM stores programs. The other RAM stores operational information (PCM-channel-to-trunk connection assignments). The circuit performs the processing functions for the TM2. This circuit generates clock signals, checks parity, and synchronizes the activities of the module circuits. The group CODEC and tone CP changes analog samples to PCM code words. The group CODEC converts PCM word streams to analog samples. The group routes speech samples to the appropriate trunk interface CP. The group CODEC includes a ROM that stores digital tones for dialing and signaling.
NT2X59AA	4F	*Group coder-decoder and tone circuit pack* The group CODEC and tone CP changes analog samples to PCM code words. The group CODEC converts PCM word streams to analog samples. The group CODEC routes speech samples to the appropriate trunk interface CP. The group includes a ROM that stores digital tones for dialing and signaling.

The following figure displays the design of the NT2X52AM.

NT2X52AM parts



NT2X52AN

Description

The NT2X52AN four-wire trunk module (TM4) is for Canadian applications. The TM4 is an interface between a maximum of 30 analog trunk circuits and several components of the digital switching system. These components include the 32-channel, time-division, pulse code modulated (PCM) speech and control streams. The TM4 converts analog trunk speech and signaling information to and from a 2.56-Mbit/s stream.

The TM4 is mounted in an NT0X46AB trunk module equipment (TME) or digital carrier equipment (DCE) frame. The TM4 accommodates many four-wire trunk circuits, like multi-frequency (MF) and dial pulse (DP) receivers. The TM4 consists of a control circuit card, a power converter and interchangeable trunk interfaces. The control circuit card is the interface between the DS30 speech links and the two planes of the network. The control circuit card is also responsible for data processing, control, and group coder-decoder (CODEC) functions.

Three types of data exchange between the TM4 and the associated switching network. These data are messages between the control module (CM) and the TM4 control circuits, supervisory messages between connected trunk modules (TM), and PCM speech samples.

The three types of data transfer in a time frame of 32 channel times. The system sends messages between the TM4 and the CM over signaling and control channels. Supervisory messages between connected TMs use the channel supervisory bit in the associated speech channel. Each trunk circuit in the TM is scanned one time each 40 frames, at 5-ms intervals. Each trunk circuit sends or receives data that operate or release signal distribution points.

The TM4 separates control messages from the PCM speech samples. The TM4 aligns and reformats data on the receive channels from the two network module planes. The PCM receive signals convert to pulse amplitude modulated (PAM) signals. Digital tones are added as necessary. The PAM signals samples reconstruct the original analog signals. These signals are sent to the trunk transmission facilities.

On the transmit side, analog speech signals from the trunk facilities convert to PAM samples. The PAM samples convert to PCM signals. Digital tones are added to the PCM signals. The PCM samples and associated data are combined and reformatted in a data stream on the speech link transmit path. Two data buses, XDAT and RDAT, transfer transmit and receive data, in that order.

The TM4 includes looparound facilities for maintenance and troubleshooting. Digital looparound links the RDAT and XDAT buses. Analog looparound links the XPAM and RPAM buses. Looparound is available for each trunk interface circuit.

The components listed below are part of the NT2X58AZ maintenance trunk module common circuit pack. This common circuit pack is used when the TM4 does not contain the NT3X05AA/AC digital data line card. If the application requires use of the NT3X05AA/AC digital data line card, the common circuit pack NT2X58CP must be used in the TM4.

Parts

The TM4 contains trunk interface CPs and the following parts:

- NT0X70AA—TM processor and memory card
- NT2X09AA—power converter card
- NT2X45AB—TM interface card
- NT2X53AA—TM control card
- NT2X59AA—group CODEC DMS-100/200 card

Design

The following table describes the parts of the NT2X52AN.

NT2X52AN parts (Sheet 1 of 3)

PEC	Slot	Description
Varies	5-19F	*Trunk interface cards* The trunk interface cards are the interface between analog transmission and signaling trunk facilities and the digital multiplex circuits in the TM. The number and type of cards in a given module depend on the type of trunk facilities. Some trunk interface cards have two trunk interface circuits. Other trunk interface cards have one trunk interface circuit. Each interface contains a sampling gate for speech processing, and signaling circuits. Each interface card contains buffers for signaling data, looparound test circuits, and card-type identification.

NT2X52AN (continued)

NT2X52AN parts (Sheet 2 of 3)

PEC	Slot	Description
NT0X70AA	2F	*Trunk module processor and memory card* The TM processor and memory card controls or performs operations in the TM4. The TM4 contains a microprocessor, a ROM, and two RAMs. One RAM stores programs. The other RAM stores operational information (PCM channel-to-trunk connection assignments). This card generates clock signals, and checks parity. This card synchronizes the activities of the module circuits.
NT2X09AA	20F	*Power converter card* The power converter card converts the dc voltage of -48 V into the dc operating voltages (-5, -15, +5, +12, and +24V) that the circuits in the TM4 require. The converter includes a low-voltage monitor circuit, and overvoltage and overcurrent protection. The converter includes faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X45AB	1F	*Trunk module interface card* The TM trunk interface card provides a pair of two-way interfaces. These interfaces are between the two transmission paths of each network plane and the TM. The TM trunk interface card aligns and reformats PCM samples on both the transmit and receive paths. The TM trunk interface card includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The TM separates control messages from the speech samples and sends the messages to the TM control card.

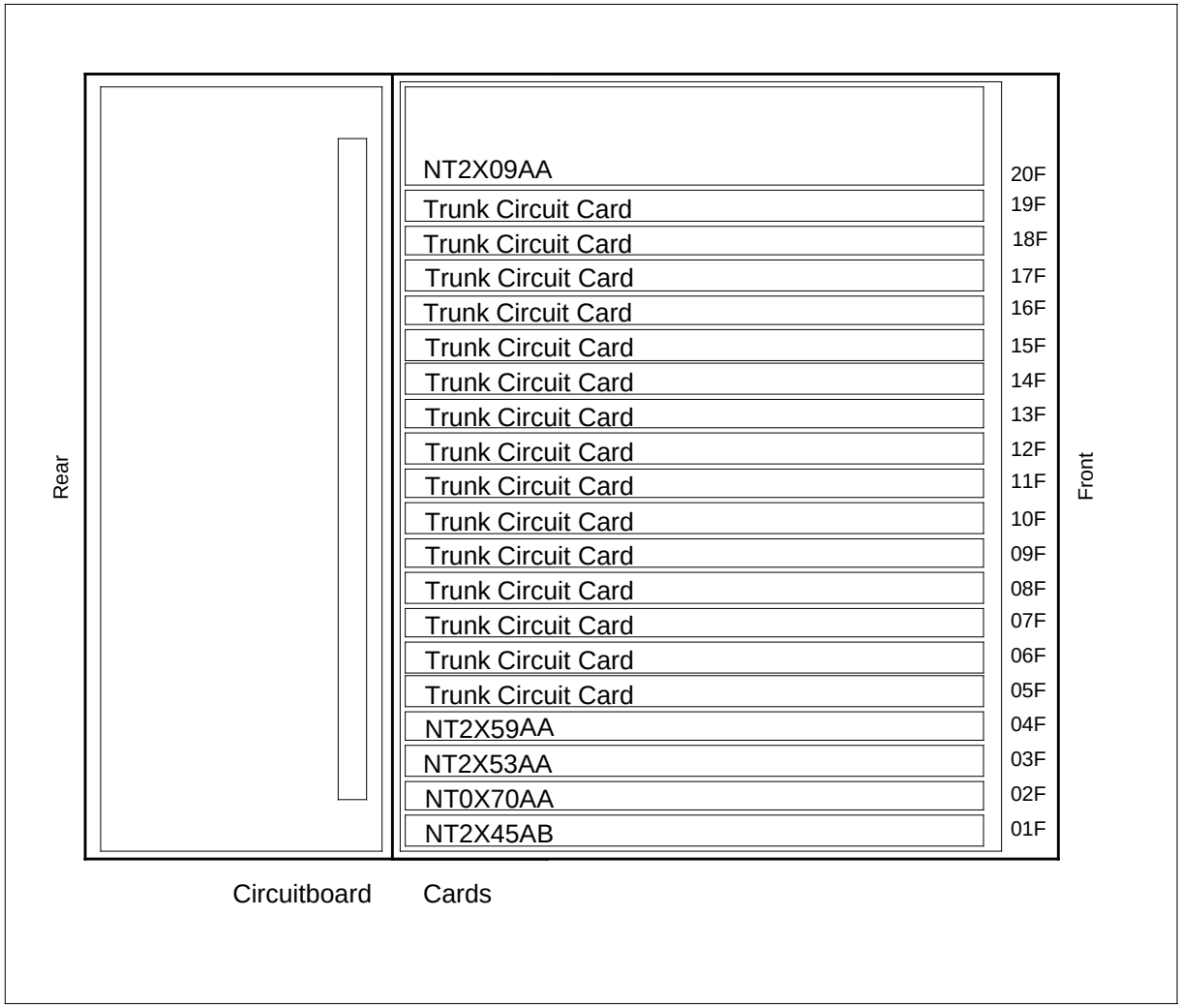
NT2X52AN parts (Sheet 3 of 3)

PEC	Slot	Description
NT2X53AA	3F	*Trunk module control card* The TM control card provides a pair of two-way interfaces between the two transmission paths of each network plane and the TM4. This card aligns and reformats PCM samples on the transmit and receive paths. The card separates control messages from the speech samples, and sends the messages to the control circuit. The TM control card includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The control circuit organizes the flow of incoming and outgoing messages. This circuit includes three controllers that handle trunk, network, and integrity messages. The circuit generates enabling signals for the 30 trunk interfaces. The circuit exchanges data with the trunk interface cards and routes speech samples to the group CODEC and tone card. Data transfers between the TM control card and the processor and memory card through the data and address busses. The processor and memory circuit controls or performs operations in the TM4. The processor contains a microprocessor, a ROM, and two RAMS. One RAM stores programs. The other RAM stores operational information (PCM channel-to-trunk connection assignments). This circuit generates clock signals, checks parity, and synchronizes the activities of the module circuits. The group CODEC DMS-100/200 card changes analog samples to PCM code words and converts PCM word streams into analog samples. The group routes speech samples to the correct trunk interface card, and includes a ROM that stores digital tones for dialing and signaling.
NT2X59AA	4F	*Group CODEC DMS-100/200 card* The group CODEC DMS-100/200 card changes analog samples to PCM code words and converts PCM word streams to analog samples. The group CODEC routes speech samples to the correct trunk interface card. The group includes a ROM that stores digital tones for dialing and signaling.

The following figure describes the design of the NT2X52AN.

NT2X52AN (end)

NT2X52AN parts



NT2X52AP

Description

The NT2X52AP eight-wire trunk module (TM8) is an interface. The TM8 is an interface between a maximum of 30 analog trunk circuits and components of the digital switching system. These components include the 32-channel, time-division, pulse-code-modulated (PCM) speech and control streams. The TM8 converts analog trunk speech and signaling information to and from a 2.56-Mbps stream.

The TM8 is mounted in a single-bay trunk module equipment (TME) or digital carrier equipment (DCE) frame. The TM8 accommodates many international trunk circuits, like multifrequency (MF) and dial pulse (DP) receivers. The TM8 consists of a control circuit card, a power converter, and many interchangeable trunk interfaces. The control circuit pack (CP) functions as the interface between the DS30 speech links and the two planes of the network. The control circuit pack is also responsible for data processing, control, and group coder-decoder (CODEC) functions.

Three types of data exchange between the international trunk module (TM) and the associated switching network. These data are messages between the control module (CM) and the TM control circuits, supervisory messages between connected TMs, and PCM speech samples.

The three types of data transfer in a time frame of 32 channel times. The system sends messages between the TM and the CM over signaling and control channels. Supervisory messages between connected TMs use the channel supervisory bit in the associated speech channel. Each trunk circuit in the TM is scanned one time each 40 frames (at 5-ms intervals). Each trunk circuit sends or receives data that operate or release signal distribution points.

The TM8 separates control messages from the PCM speech samples. The TM8 also aligns and reformats data on the receive channels from the network module planes. The PCM receive signals convert to pulse-amplitude-modulated (PAM) signals. Digital tones are added as necessary. The PAM signals samples are used to reconstruct the original analog signals. These signals are sent to the trunk transmission facilities.

On the transmit side, analog speech signals from the trunk facilities convert to PAM samples. The PAM samples convert to PCM signals. Digital tones are added to the PCM signals. The PCM samples and associated data are combined and reformatted in a data stream on the speech link transmit path. Two data buses, XDAT and RDAT, are used to transfer transmit and receive data, in that order.

NT2X52AP (continued)

The TM8 also includes looparound facilities for maintenance and troubleshooting. Digital looparound links the RDAT and XDAT buses. Analog looparound links the XPAM and RPAM buses. Looparound is provided for each trunk interface circuit.

Parts

The TM8 contains trunk interface CPs, the NT2X09AA power converter, and the NT4X65AB TM control CP.

Design

The following table describes the design of the NT2X52AP.

NT2X52AP parts (Sheet 1 of 3)

PEC	Slot	Description
—	5F-19F	*Trunk interface circuit packs* The trunk interface CPs are the interface between analog transmission and signaling trunk facilities and the digital multiplex circuits in the TM. The number and type of CPs in a given module depend on the type of trunk facilities. Some trunk interface CPs have two trunk interface circuits. Other trunk interface CPs have one trunk interface circuit. Each interface contains a sampling gate for speech processing, and signaling circuits. Each interface contains buffers for signaling data, looparound test circuits, and card-type identification.
NT0X70AA	2F	*Trunk module processor and memory circuit pack* The TM processor and memory CP controls or performs operations in the TM2. The processor contains a microprocessor, a ROM, and two RAMs. One RAM stores programs. The other RAM stores operational information (PCM-channel-to-trunk connection assignments). The CP performs the processing functions for the TM2. This CP generates clock signals, checks parity, and synchronizes the activities of the module circuits.
NT2X09AA	20F	*Power converter* The power converter converts the -48V dc to the operating voltages (-5V, -15V, +5V, +12V, and +24V dc) that the circuits in the TM2. The converter includes a low-voltage monitor circuit, overvoltage and overcurrent protection. The converter includes faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.

NT2X52AP parts (Sheet 2 of 3)

PEC	Slot	Description
NT2X45AB	1F	*Trunk module interface CP* The TM trunk interface CP provides a pair of two-way interfaces between the two transmission paths of each network plane and the TM. The TM trunk interface CP aligns and reformats PCM samples on the transmit and receive paths. The CP includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The CP also separates control messages from the speech samples and sends the messages to the TM control CP.
NT2X59AA	4F	*Group coder-decoder and tone circuit pack* The group CODEC and tone CP changes analog samples to PCM code words. The group CODEC converts PCM word streams to analog samples. The group CODEC is responsible for routing speech samples to the correct trunk interface CP. The group includes a ROM that stores digital tones for dialing and signaling.

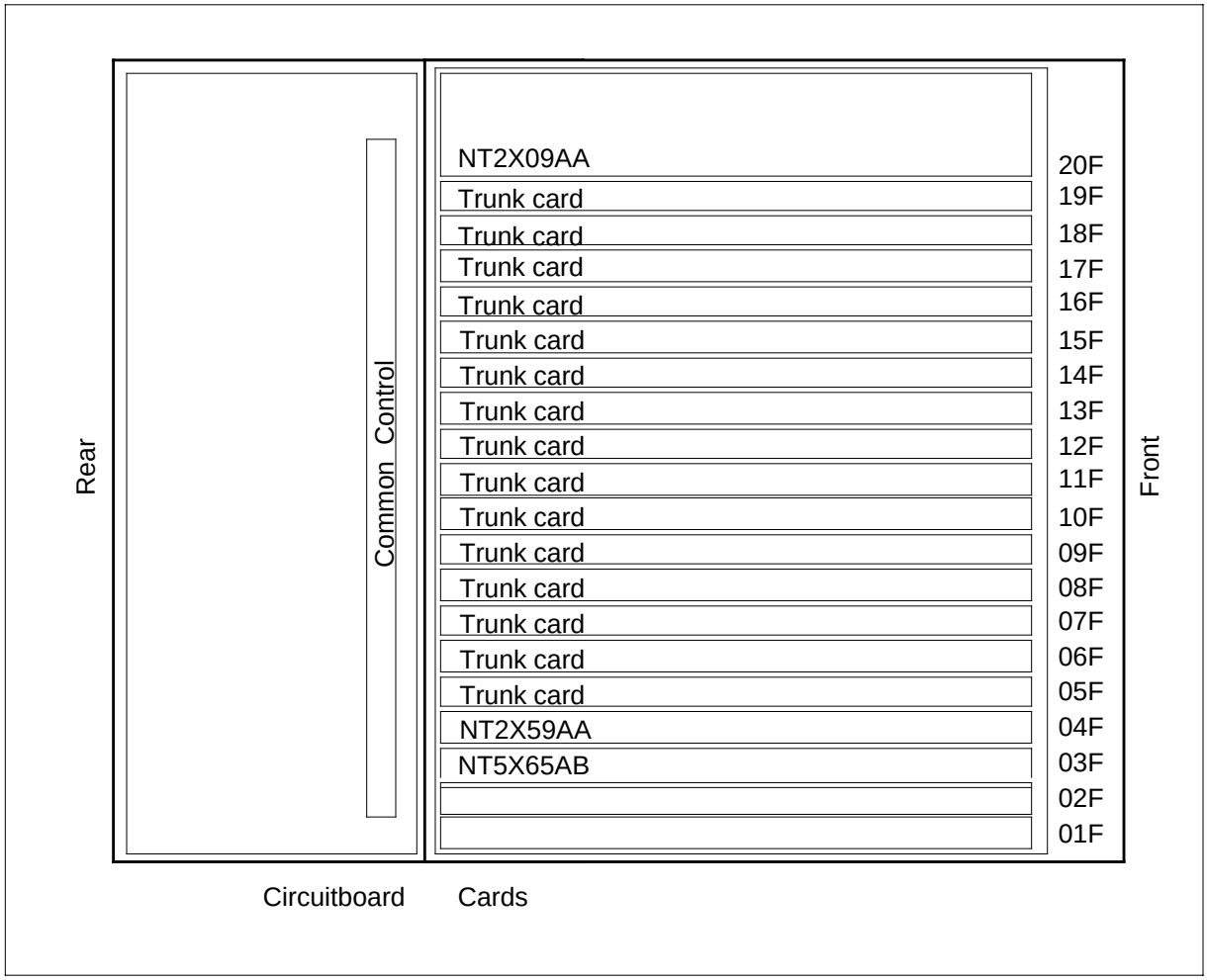
NT2X52AP (continued)

NT2X52AP parts (Sheet 3 of 3)

PEC	Slot	Description
NT4X65AB	3F	*Trunk module control circuit pack* The TM control CP provides a pair of two-way interfaces between the two transmission paths of each network plane and the TM2. This CP aligns and reformats PCM samples on the transmit and receive paths. The CP separates control messages from the speech samples, and sends the messages to the control circuit. The CP includes message registers, bit and channel timing, parity-checking, and data-reformatting circuits. The control circuit organizes the flow of incoming and outgoing messages. This circuit includes three controllers that handle trunk, network, and integrity messages. This circuit generates enabling signals for the 30 trunk interfaces. The circuit exchanges data with the trunk interface CPs and routes speech samples to the group CODEC and tone CP. Data transfer between the TM control CP and the processor and memory CP through the data and address buses. The processor and memory circuit controls or performs operations in the TM2. The processor contains a microprocessor, a ROM memory, and two RAMs. One RAM stores programs. The other RAM one stores operational information (PCM-channel-to-trunk connection assignments). This circuit performs the processing functions for the TM2. This circuit generates clock signals, checks parity, and synchronizes the activities of the module circuits. The group CODEC and tone CP changes analog samples to PCM code words and converts PCM word streams to analog samples. The group routes speech samples to the correct trunk interface CP. This interface includes a ROM that stores digital tones for dialing and signaling.

The following figure describes the design of the NT2X52AP.

NT2X52AP parts



NT2X52AR

Description

The NT2X52AR trunk module 8-wire is only used for Canadian applications in DMS-300 offices. The NT2X52AR has access shelf mounts in an NT0X46AB trunk module equipment frame. The NT2X52AR shelf has leads to allow connection to a test access network (TAN). The feature permits a metallic path through the TAN to connect external test equipment to trunk facilities and circuits.

Each NT2X52AR shelf contains one DMS-300 trunk module common card. This common card is the NT2X52AL. This TM8 shelf is different from the special function TM8-type module, NT2X52AP. The DMS-100 PBX and common carrier applications use the NT2X52 AP.

Parts

The TM8 shelf contains optional trunk cards and the following parts:

- NT2X09AA—power converter card
- NT2X59AB—group CODEC DMS-300 (Teleglobe) card
- NT4X65AB—combination control circuit card

Design

The parts appear in the following table.

NT2X52AR parts (Sheet 1 of 2)

PEC	Slot	Description
Varies	5-19F	*Optional trunk cards* You can install a maximum of 15 optional trunk cards to meet traffic requirements. Selects these circuit cards from five types of circuits. These circuits include conference circuits, CCITT trunk circuits, communication test line circuits, CAMA position signaling circuits, and digital 4-channel multifrequency receiver circuits.
NT2X09AA	20F	*Power converter card* The power converter card converts the dc voltage of -48V into the dc operating voltages (-5, -15, +5, +12, and +24V). The circuits in the TM8 require this operating voltage. The card includes a low-voltage monitor circuit, overvoltage and overcurrent protection, faceplate test jacks, and faceplate light-emitting diode (LED) status indicator.

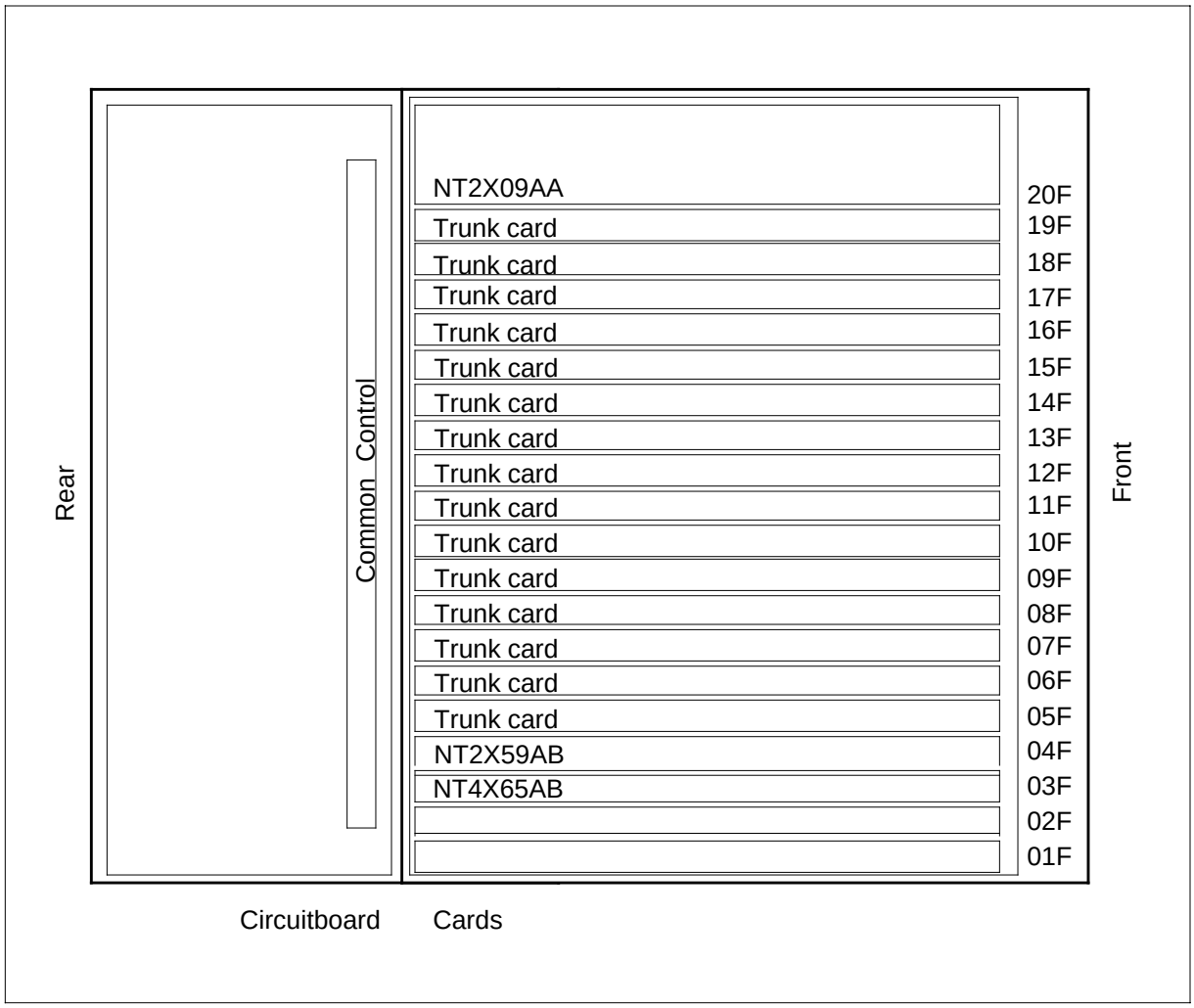
NT2X52AR parts (Sheet 2 of 2)

PEC	Slot	Description
NT2X59AB	4F	*Group CODEC DMS-300 (Teleglobe) card* A DMS-300 peripheral module uses the NT2X59AB. The NT2X59AB card changes analog samples in to pulse code modulated (PCM) code words. The NT2X59AB converts PCM word streams into analog samples. The NT2X59AB routes speech samples to the appropriate trunk interface card. The NT2X59AB includes a ROM that stores digital tones for dialing and signaling.
NT4X65AB	3F	*Combination control circuit card* The combination control circuit card combines the function of the control card, the interface card, and the processor and memory card. The NT4X65AB contains the network interface, processing, and control circuits for each TM8 shelf. The network interface includes two bi-directional interfaces for the two transmission paths from both network planes. The NT4X65AB contains message registers, bit and channel timing circuits, parity-checking circuits, and circuits that format the data again. The processor performs or controls all the operations that the components of the TM8 accomplish. The processor includes a firmware-driven microprocessor and two RAMs. One RAM stores program information and the other RAM stores operational information. This operational information includes connection information for PCM channel-to-trunk assignments. The second RAM includes circuits that generate the clock signal, check parity, and perform synchronization. The control section contains the circuit controllers that handle different messages.

The design of the NT2X52AR shelf appears in the figure.

NT2X52AR (end)

NT2X52AR parts



NT2X52BB

Description

International applications for DMS-100 or DMS 200 offices use the NT2X52BB shelf as an 8-wire trunk module (TM). The NT2X52BB mounts in an NT0X46AB trunk module equipment frame.

Parts

The NT2X52BB shelf contains a maximum of 15 optional trunk cards and the following components:

- NT0X70AA—Trunk module processor and memory card
- NT2X09AA—power converter card
- NT2X45BA—TM interface card
- NT2X53AA—TM control card
- NT2X59CA—A-law TM CODEC with BT tones

Design

A description of the components appear in the following table.

NT2X52BB components (Sheet 1 of 3)

PEC	Slot	Description
Varies	5-19F	*Optional trunk cards* You can install a maximum of 15 optional trunk cards to meet traffic requirements. Select these circuit cards from communication test line circuits, multifrequency receiver circuits, and jack-ended trunk circuits.
NT0X70AA	2F	*Trunk module processor and memory card* The TM processor and memory card controls or performs all the operations in the ITM8 shelf. The TM processor contains a microprocessor, a ROM, and two RAMs. One RAM stores programs and the second RAM stores operational information. The operation information includes pulse code modulated (PCM) channel-to-trunk connection assignments. This card generates clock signals, checks parity, and synchronizes the activities of the circuits in the module.

NT2X52BB (continued)

NT2X52BB components (Sheet 2 of 3)

PEC	Slot	Description
NT2X09AA	20F	*Power converter card* The power converter card converts the dc voltage of -48V into dc operating voltages (-5, -15, +5, +12, and +24V). The circuits in the ITM8 shelf require these voltages. The card includes a low-voltage monitor circuit, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) state indicator.
NT2X45BA	1F	*Trunk module interface card* The TM interface card serves as the network interface for the network planes. The card provides two 2-way interfaces for the two transmission paths from the network planes. The card contains message registers, bit and channel timing circuits, circuits that check parity, and circuits that format data again.
NT2X53AA	3F	*Trunk module control card* The TM control card includes message registers, bit and channel timing, checks parity, and circuits that format data again. The TM control card aligns and formats PCM samples on the transmit and receive paths. The TM control card separates control messages from the speech samples. The TM control card sends messages to the control circuit. The control circuit organizes the flow of incoming and outgoing messages. This circuit includes three controllers that handle trunk, network, and integrity messages. The circuit generates enabling signals for the 30 separate trunk interfaces. The circuit exchanges data with the trunk interface cards. The circuit routes speech samples to the NT2X59CA card. The system transfers data between the TM control card and the processor through the data and address buses. The system transfers data from the memory card through the data and address buses.

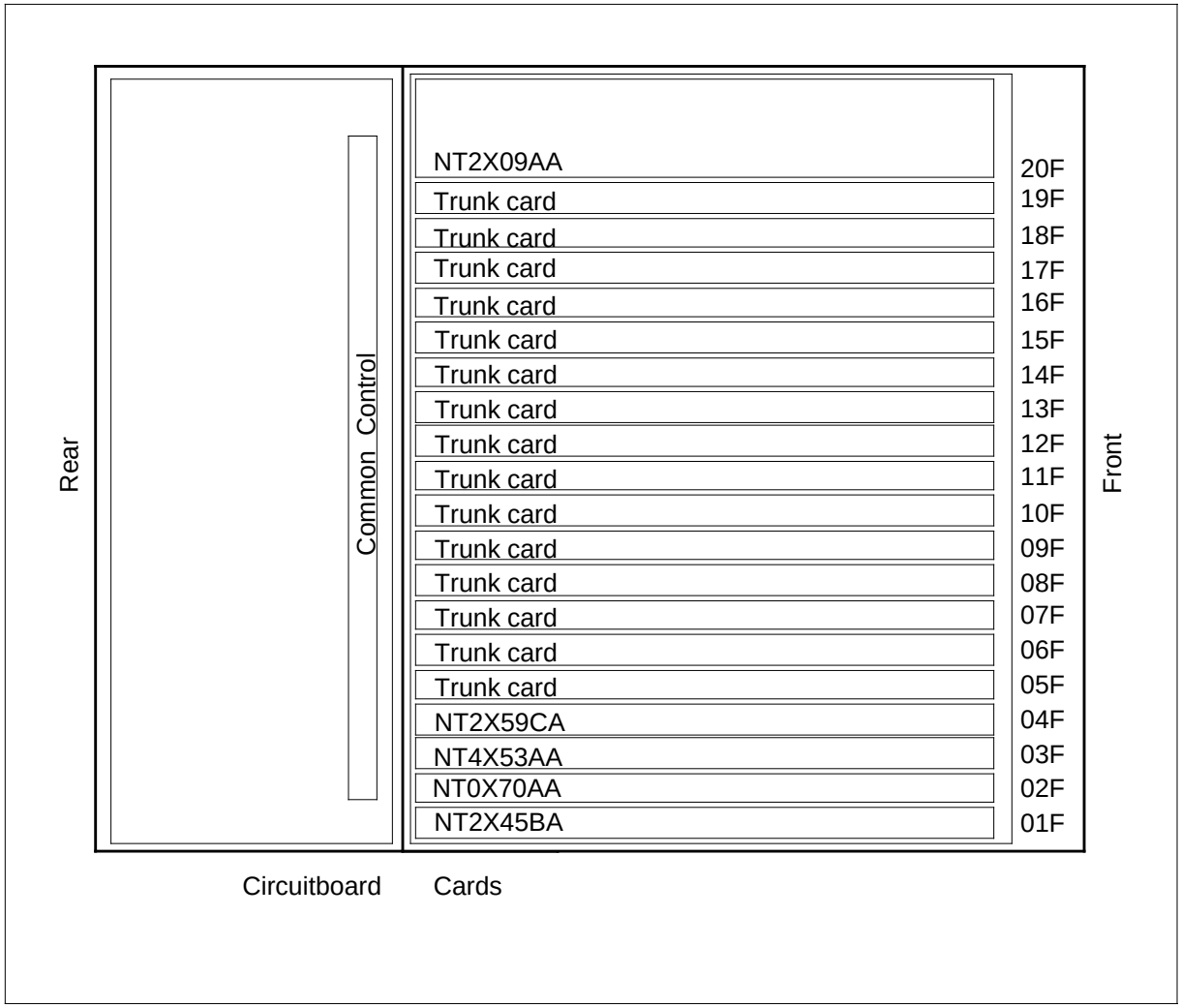
NT2X52BB components (Sheet 3 of 3)

PEC	Slot	Description
NT2X59CA	4F	*A-law TM CODEC with BT tones card* The NT2X59CA card codes pulse amplitude modulation (PAM) signals into PCM and decodes PCM signals into PAM signals. The card produces PCM tones for signaling and supervision purposes. The card receives PCM signals from the C-bus. The card decodes these signals into PAM data. The card sends the data to the trunk circuits over the receive-PAM (RPAM) bus. Trunk circuits send PAM signals over the transmit-PAM (XPAM) bus. The card encodes PAM signals into PCM. The card sends PCM signals over the C-bus. The card generates standard digital tones for supervision or signaling. The card inserts the tones into an output channel. The operation of the card is in synchronization with the system clock signal.

The design of the NT2X52BB shelf appears in the figure.

NT2X52BB (end)

NT2X52BB components



NT2X52CC

Description

Turkey and Memory DMS-300 applications use the NT2X52CC as an 8-wire trunk module. The NT2X52CC shelf mounts in an NT0X46AB trunk module (TM) equipment frame. The NT2X52CC shelf has leads to allow connection to a test access network (TAN). These leads allow a metallic path through the TAN to connect external test equipment to trunk facilities and circuits.

Parts

The NT2X52CC shelf contains a maximum of 15 optional trunk cards and the following components:

- NT0X70AC—TM processor card
- NT2X09AA—power converter card
- NT2X45BA—TM interface card
- NT2X53AA—TM control card
- NT2X59CB—A-law TM CODEC DMS-300 card

Design

A description of the components appears in the following table.

NT2X52CC components (Sheet 1 of 3)

PEC	Slot	Description
Varies	5-19F	*Optional trunk cards* You can install a maximum of 15 optional trunk cards to meet traffic requirements. Select these optional cards from CCITT R1, CCITT 5, and CCITT 6 trunk circuit cards.
NT0X70AC	2F	*Trunk module processor card* This card is a replacement for NT0X70AA. This TM processor card controls or performs all the operations in the NT2X52CC shelf. The card contains a microprocessor, a ROM, and two RAMs. One RAM stores programs and the second RAM stores operational information. Operational information includes pulse code modulated (PCM) channel-to-trunk connection assignments. This card generates clock signals, checks parity, and synchronizes the activities of the module circuits.

NT2X52CC (continued)

NT2X52CC components (Sheet 2 of 3)

PEC	Slot	Description
NT2X09AA	20F	*Power converter card* The power converter card converts the dc voltage of -48 V into dc operating voltages (-5, -15, +5, +12, and +24 V). The circuits in this shelf require these voltages. The card includes a low-voltage monitor circuit, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate light-emitting diode (LED) status indicator.
NT2X45BA	1F	*Trunk module interface card* The TM interface card serves as the network interface for the planes of the network. The card provides two 2-way interfaces for the two transmission paths from both network planes. The card contains message registers, bit and channel timing circuits, circuits that check parity, and circuits that format data again.
NT2X53AA	3F	*Trunk module control card* The TM control card includes message registers, bit and channel timing circuits, circuits that check parity, and circuits that format data again. The card aligns and formats PCM samples again on the the transmit and receive paths. The card separates control messages from the speech samples. The card sends messages to the control circuit. The control circuit organizes the flow of incoming and outgoing messages. This circuit includes three controllers that handle trunk, network, and integrity messages. The circuit generates enabling signals for the 30 separate trunk interfaces. The circuit exchanges data with the trunk interface cards. The NT2X53AA routes speech samples to the NT2X59CB card. The system transfers data between the TM control card and the processor card through the data and address buses.

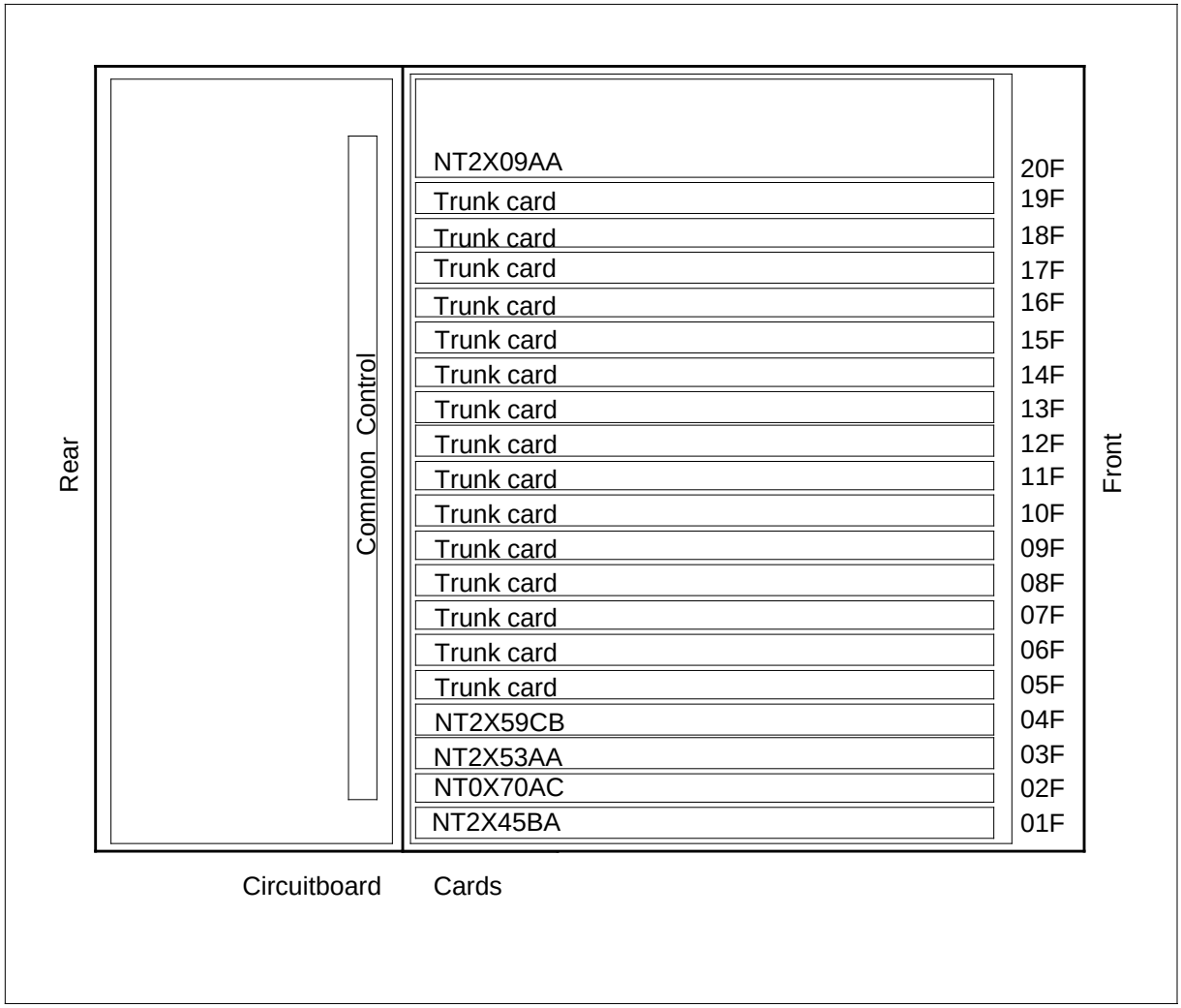
NT2X52CC components (Sheet 3 of 3)

PEC	Slot	Description
NT2X59CB	4F	*A-law TM CODEC DMS-300* The DMS-300 applications use the NT2X59CB card. The card codes pulse amplitude modulation (PAM) signals into PCM. The card decodes PCM signals into PAM signals. The card produces PCM tones for signaling and supervision purposes. The card receives PCM signals from the C-bus. The card decodes the signals into PAM data. The card sends these signals to the trunk circuits over the receive-PAM (RPAM) bus. The card receives PAM signals over the transmit-PAM (XPAM) bus. The card encodes PAM signals into PCM. The card sends the PAM signals over the C-bus. The card generates standard digital tones for supervision or signaling. The card inserts the tones in an output channel. The operation of the card is in synchronization with the system clock signal.

The design of the NT2X52CC shelf appears in the figure.

NT2X52CC (end)

NT2X52CC components



NT2X55AA

Product description

The NT2X55AA signal distribution card (type II) provides interface circuits to connect DMS-100 switching systems to external relay-controlled equipment. The card contains 14 interface circuits. Each circuit has four output options. The DMS central control (CC) operates the NT2X55AA.

Location

The card is in one card position in a maintenance trunk module (MTM).

Functional description

The MTM controls the NT2X55AA operation through signals. The card activates a minimum of one of the relays that connect to the external equipment. The card receives the signals and decodes the signals. The card activates or deactivates the selected relays. Each relay connects to a four-position switch that selects how the relays appear to the external equipment.

Functional blocks

The NT2X55AA contains the following functional blocks:

- trunk logic circuits (TLC)
- relays
- output switches

TLC

The TLCs receive instructions from the MTM. The TLCs decode the instructions and activate the relays. The instructions are sent over the receive data (RDAT) bus. The TLCs act on these instructions when MTM sends the correct enable signal. The received instructions determine if the TLC operates or releases the selected relay.

The TLC-0 controls relays K-0, K-2, K-4, K-6, K-8, K-10, and K-12. The TLC-1 controls relays K-1, K-3, K-5, K-7, K-9, K-11, and K-13.

Relays

The relays contain single-pole, double-throw (SPDT) contacts. The TLCS control these relays. The relay contacts are mercury wetted to allow applications that require high contact ratings.

Output switches

All 14 relays have a four-position switch that connects to a two-position switch. When you manually change the switch positions, the output conditions

NT2X55AA (continued)

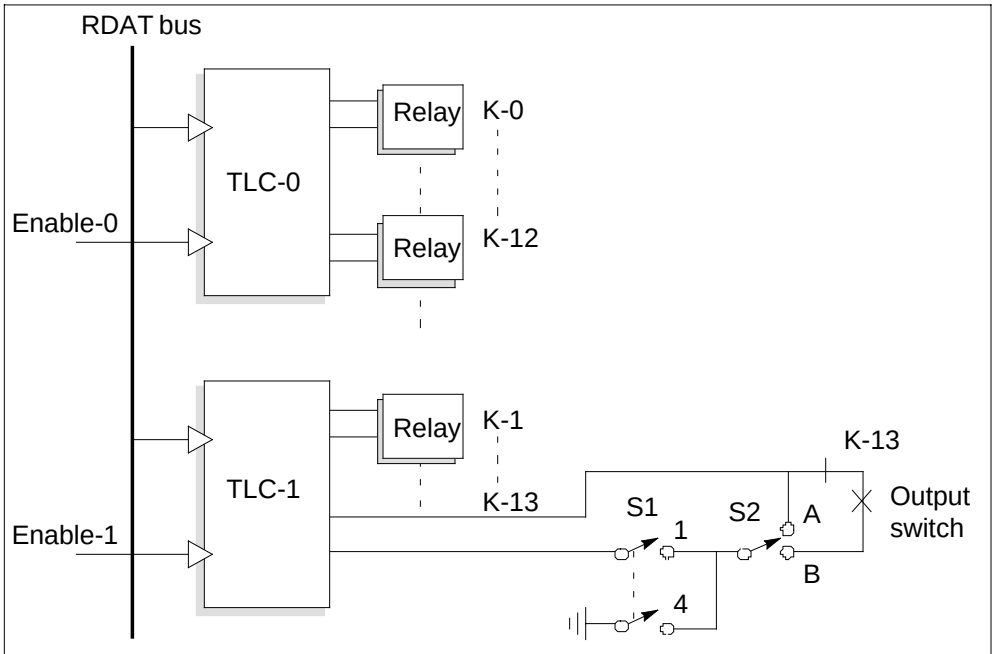
of the relay can change. The switch settings for each relay appear in the following table.

Switch settings

Switch positions S1	S2, position 1	S2, position 4	Relay conditions Relay operated	Relay released	Output lead type
A	OFF	ON	Ground, closed	Ground, open	Single
B	OFF	ON	Ground, open	Ground, closed	Single
A	ON	OFF	Loop, closed	Loop, open	Double
B	ON	OFF	Loop, open	Loop, closed	Double

The relationship between the functional blocks appears in the following figure.

NT2X55AA functional blocks



Note: This detail of relay K-13 describes the operation of all 14 relays.

Technical data

The NT2X55AA output relays use contacts rated at 2A and 500V.

Physical dimensions

The dimensions for the NT2X55AA circuit card are as follows:

- overall height: 353 mm (13.9 in.)
- overall depth: 267 mm (10.5 in.)
- overall width: 29 mm (1.125 in.)

Power requirements

The power requirements for the NT2X55AA are a voltage of +24V and power of 5.1W maximum. These power requirements occur when all relays operate.

NT2X56AA

Product description

The transmission test unit (TTU) contains the following:

- the NT2X56AA transmission test module digital filter (DF) card
- the NT2X47AA or NT2X47AB control processor (CP)

The TTU is a digital signal processor. The user can program the TTU to allow for transmission measurements and perform maintenance functions. The DF card receives pulse code modulation (PCM) tones. The DF card uses filters to determine the power of the tones.

The combination of the NT2X56AA and the NT2X47AA performs automatic transmission measuring equipment-2 (ATME-2) tests for a 104 test line. The NT2X56AA and the NT2X47AB perform ATME-2 tests for a DMS-300 office.

Location

The NT2X56AA is in one card position in the maintenance trunk module (MTM) shelf. The card must be in the slot next to the CP card.

Functional description

The DF card receives PCM data from the receive data (RDAT) bus. The DF card filters the data and samples the filter outputs. The DF card sends the total of the samples to the CP card. The DF card contains 32 filters. A single test can use any of the 10 filters. The filters are stored in memory. The CP card selects the filters.

Functional blocks

The NT2X56AA contains the following functional blocks:

- PCM interface
- linearization PROM
- DF
- filter select RAM
- serial accumulator
- direct memory access (DMA) interface
- feedback register
- buffer

PCM interface

The PCM interface receives the PCM data from the RDAT bus. The PCM interface sends test signals to the CP card over the transmit data (XDAT) bus. The PCM data is received in 8-bit format at 32 channels for each frame. Enable signals from the MTM control PCM data. The PCM interface holds the data in 8-bit serial form until the card is ready to process the data.

Linearization PROM

After the PCM interface receives data from the RDAT bus, the PCM sends the data to the linearization PROM. The PROM converts the 8-bit serial data into 16-bit linear data for further processing. The PROM contains four linearization tables. The CP card can select one linearization table to use in a given test.

DF

The DF contains 32 filter circuits stored in RAM. A test can use any of the ten filters. The master processor (MP) on the CP card reads from, and writes to the filter RAM, to select the filters to use.

Filter select RAM

The CP card selects the filters and linearization tables to use for a given test. The CP card selects the filters and tables to send instructions to the filter select RAM. The MP in the CP card writes the following into the filter select RAM to use for a test:

- addresses of the filters
- linearization table

The RAM passes the instructions to the linearization PROM and the DF.

The MP in the CP card can read the contents of the filter select RAM.

Serial accumulator

The output of the DFs is sampled. The samples are stored in the serial accumulator. After the system accumulator contains 64 samples, the system accumulator sends the data to the DMA interface. The DMA interface transfers the data to the CP card.

The CP card in every sample group receives three 8-bit bytes from each filter.

DMA interface

The DMA interface receives filter samples from the serial accumulator. The DMA interface sends the data to the DMA controller on the CP card. The controller stores the data directly in the MP memory on the CP card to wait for processing.

NT2X56AA (continued)

Feedback register

The feedback register controls communication between the DF and the serial accumulator. This register controls communication while the DMA interface transfers data to the CP card. During the data transfer, the feedback register forces the feedback from the accumulation to 0. This action allows new data to enter the accumulator.

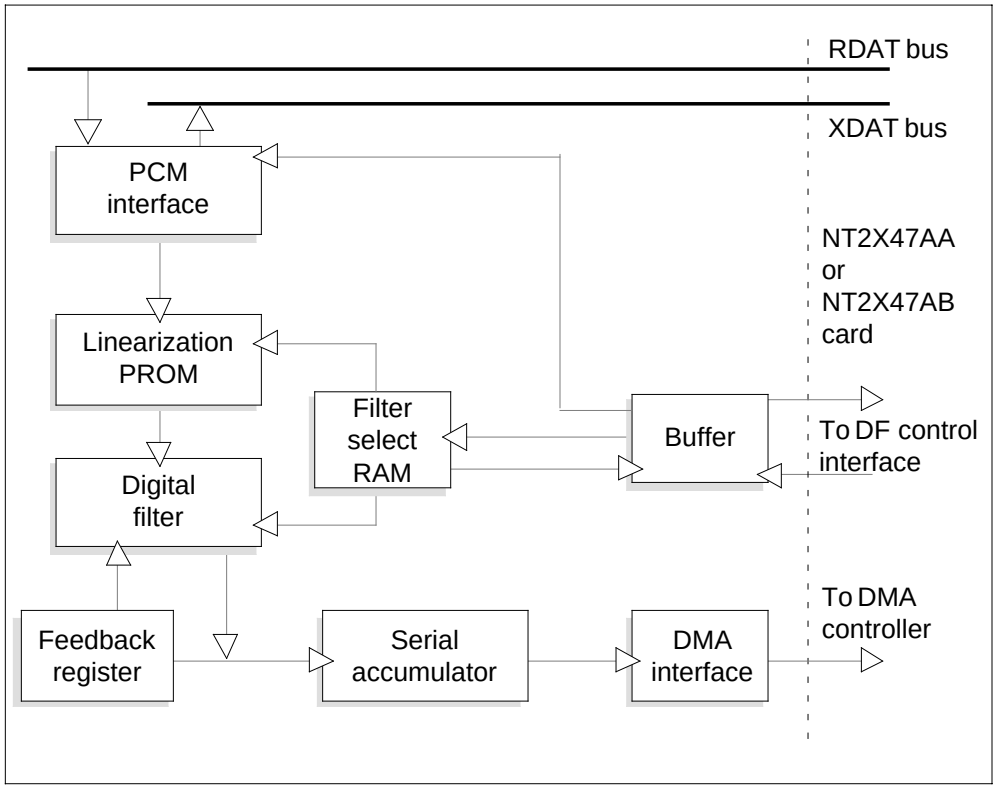
Buffer

The buffer controls communication between the DF card and the CP card. The buffer does not control DMA communications. The buffer receives requests from the CP card to read the filter select RAM. The buffer passes the request to the RAM and receives the requested data from the RAM. The buffer returns the data to the CP card.

The buffer passes test requests to the DF card. The buffer sends the test data to the PCM interface. The RM interface sends the data over the XDAT bus.

The relationship between the functional blocks appears in the following figure.

NT2X56AA functional blocks



Technical data

The NT2X56AA accepts PCM input signals between 4 Hz and 4 kHz at levels from -88.8 dB through +6 dB (±0.1 dB).

Physical dimensions

The dimensions for the NT2X56AA circuit card are as follows:

- overall height: 353 mm (13.9 in.)
- overall depth: 277 mm (10.9 in.)
- overall width: 28 mm (1.1 in.)

Power requirements

The power requirements for the NT2X56AA appear in the following table.

Power dissipation is 12.9W.

Power requirements

Voltage	Current
+5 V	1.45A
-12V	0.47A

NT2X56AB

Product description

The transmission test unit (TTW) contains:

- the NT2X56AB transmission test module digital filter (DF) card
- the NT2X47AC control processor (CP) card

The TTU is a digital signal processor. The user can program the TTU to allow for transmission measurements and perform maintenance functions. The DF card receives pulse code modulation (PCM) tones. The DF card uses filters to determine the power of the tones.

The combination of the NT2X56AB and the NT2X47AC performs automatic transmission measuring equipment-2 (ATME-2) tests for a 104 test line. The NT2X56AB and the NT2X47AC perform automatic transmission measuring system (ATMS) tests for a 105 test line.

Location

The NT2X56AB is in one card position in the maintenance trunk module (MTM) shelf. The card must be in the slot next to the CP card.

Functional description

The DF card receives PCM data from the receive data (RDAT) bus. The DF card filters the data and samples the filter outputs. The DF card sends the total of the samples to the CP card. The DF card contains 32 filters. A single test can use any of the 10 filters. The filters are stored in memory. The CP card selects the filters.

Functional blocks

The NT2X56AB contains the following functional blocks:

- PCM interface
- linearization PROM
- DF
- filter select RAM
- serial accumulator
- direct memory access (DMA) interface
- feedback register
- buffer

PCM interface

The PCM interface receives the PCM data from the RDAT bus. The PCM interface test signals to the CP card over the transmit data (XDAT) bus. The PCM data is received in 8-bit format at 32 channels for each frame. Enable signals from the MTM control the PCM data. The PCM interface holds the data in 8-bit serial form until the card is ready to process the data.

Linearization PROM

After the PCM interface receives the data from the RDAT bus, the interface sends the data to the linearization PROM. The PROM converts the 8-bit serial data into 16-bit linear data for additional processing. The PROM contains four linearization tables. The CP card selects one table for use in a given test.

DF

The DF contains 32 separate filter circuits stored in RAM. A given test can use any of the 10 filters. The master processor (MP) on the CP card can read from and write to the filter RAM. This MP performs this action to select the filters to use.

Filter select RAM

The CP card selects the filters and linearization tables to use for a given test. The CP selects the filters and tables to send instructions to the filter select RAM. The MP in the CP card writes the following into the filter select RAM to use for a test:

- the addresses of the filters
- the linearization table

The RAM passes the instructions to the linearization RAM and the digital filter.

The MP in the CP card can read the contents of the filter select RAM.

Serial accumulator

The output of the DFs is sampled. The samples are stored in the serial accumulator. After the serial accumulator contains the 64 samples, the serial accumulator sends the data to the DMA interface. The DMA interface transfers the data to the CP card.

The CP card in each group of samples receives three 8-bit bytes from each filter.

NT2X56AB (continued)

DMA interface

The DMA interface receives filter samples from the serial accumulator. The DMA interface sends the data to the DMA controller on the CP card. The controller stores the data directly in the MP memory on the CP card to wait for processing.

Feedback register

The feedback register controls communication between the DF and the serial accumulator. This register controls communication while the DMA interface transfers data to the CP card. During the transfer of data, the feedback register forces the feedback from the accumulator to 0. This action allows new data to enter the accumulator.

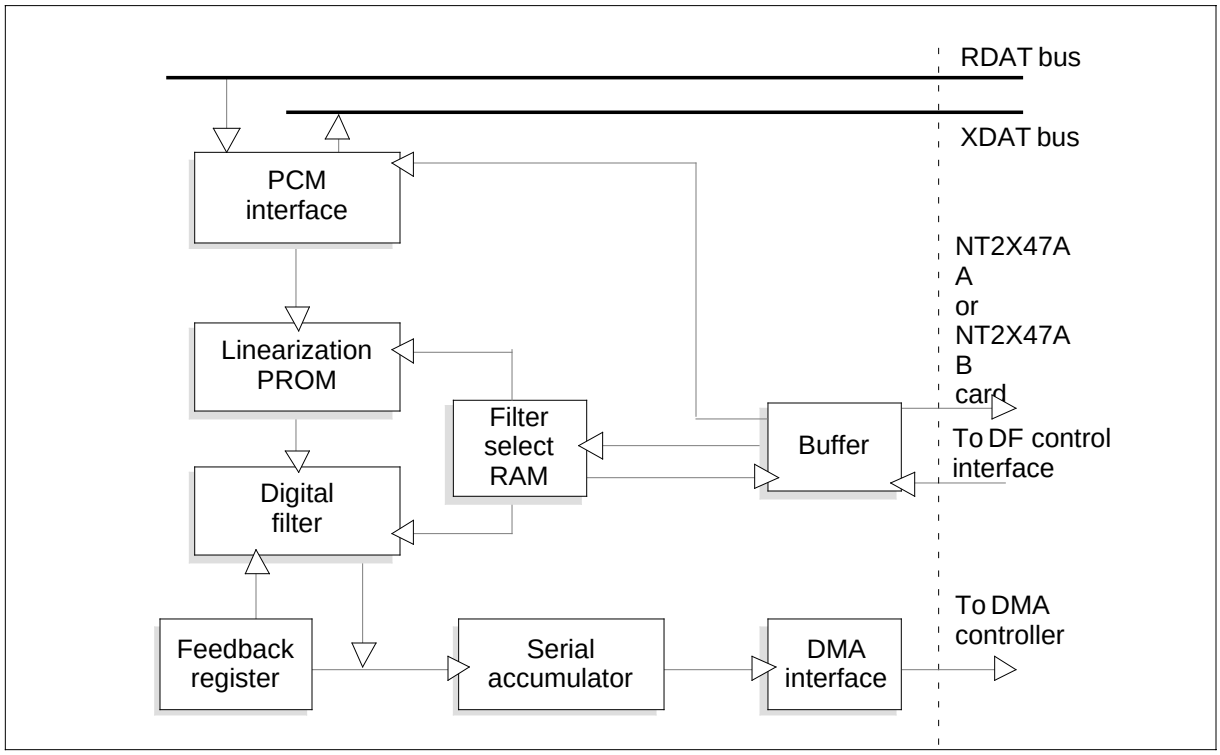
Buffer

The buffer controls communication between the digital filter card and the CP card. The buffer does not control DMA communications. The buffer receives requests from the CP card to read the filter select RAM. The buffer passes the request to the RAM. The buffer receives the requested data from the RAM. The buffer returns the data to the CP card.

The buffer passes test requests to the DF card. The buffer sends the test data to the PCM interface. The buffer sends the data over the XDAT bus.

The relationship between the functional blocks appears in the following figure.

NT2X56AB functional blocks



Technical data

The NT2X56AB accepts PCM input signals between 4 Hz and 4 kHz at levels from -88.8 dB through +6 dB (±0.1 dB).

Dimensions

The dimensions of the NT2X56AB circuit card are as follows:

- overall height: 353 mm (13.9 in.)
- overall depth: 277 mm (10.9 in.)
- overall width: 28 mm (1.1 in.)

NT2X56AB (end)

Power requirements

The power requirements for the NT2X56AB appear in the following table.

Power requirements

Voltage	Current
+5 V	1.45A
-12V	0.47A

Power dissipation is 12.9W.

NT2X56BA

Product description

The transmission test unit (TTU) contains:

- the NT2X56BA digital filter (DF) (A-law TTU card)
- the NT2X47BA control processor (CP) card

The TTU is a digital signal processor. The user can program the TTU to allow for transmission measurements and perform maintenance functions. The DF card receives pulse code modulation (PCM) tones. The DF card uses filters to determine the power of the tones.

The combination of the NT2X56BA and the NT2X47BA performs the following:

- international automatic transmission measuring equipment (ATME)
- automatic transmission measuring system (ATMS) tests

Location

The NT2X56BA is in one card position in the maintenance trunk module (MTM) shelf. The card must be in the slot next to the CP card.

Functional description

The DF card receives PCM data from the receive data (RDAT) bus. The DF card filters the data and samples the filter outputs. The DF card sends the total of the samples to the CP card. The DF card contains 32 filters. A single test can use any of the 10 filters. The filters are stored in memory. The CP card selects the filters.

Functional blocks

The NT2X56BA contains the following functional blocks:

- PCM interface
- linearization PROM
- DF
- filter select RAM
- serial accumulator
- direct memory access (DMA) interface
- feedback register
- buffer

NT2X56BA (continued)

PCM interface

The PCM interface receives the PCM data from the RDAT bus. The PCM interface sends test signals to the CP card over the transmit data (XDAT) bus. The PCM data is received in 8-bit format at 32 channels for each frame. Enable signals from the MTM control the PCM data. The PCM interface holds the data in 8-bit serial form until the card is ready to process the data.

Linearization PROM

After the PCM interface receives the data from the RDAT bus, the interface sends the data to the linearization PROM. The PROM converts the 8-bit serial data into 16-bit linear data for additional processing. The PROM contains four linearization tables. The CP card selects one table for use in a given test.

DF

The DF contains 32 separate filter circuits stored in RAM. A given test can use any of the 10 filters. The master processor (MP) on the CP card can read from and write to the filter RAM. The MP reads from and writes to the filter RAM to select the filters to use.

Filter select RAM

The CP card selects the filters and linearization tables to use for a given test. To select the filters and tables, the card sends instructions to the filter select RAM. The MP in the CP card writes the following into the filter select RAM to use for a test:

- addresses of the filters
- the linearization table

The RAM passes the instructions to the linearization RAM and the digital filter.

The MP in the CP card can read the contents of the filter select RAM.

Serial accumulator

The output of the DFs is sampled. The samples are stored in the serial accumulator. After the accumulator contains 64 samples, the serial accumulator sends the data to the DMA interface. The DMA interface transfers the data to the CP card.

The CP card in each group of samples receives three 8-bit bytes from each filter.

DMA interface

The DMA interface receives filter samples from the serial accumulator. The DMA interface sends the data to the DMA controller on the CP card. The controller stores the data directly in the MP memory on the CP card to wait for processing.

Feedback register

The feedback register controls communication between the DF and the serial accumulator. The register controls communication while the DMA interface transfers data to the CP card. While the the DMA interface transfers the data, the feedback register forces the feedback from the accumulator to 0. This condition allows new data to enter the accumulator.

Buffer

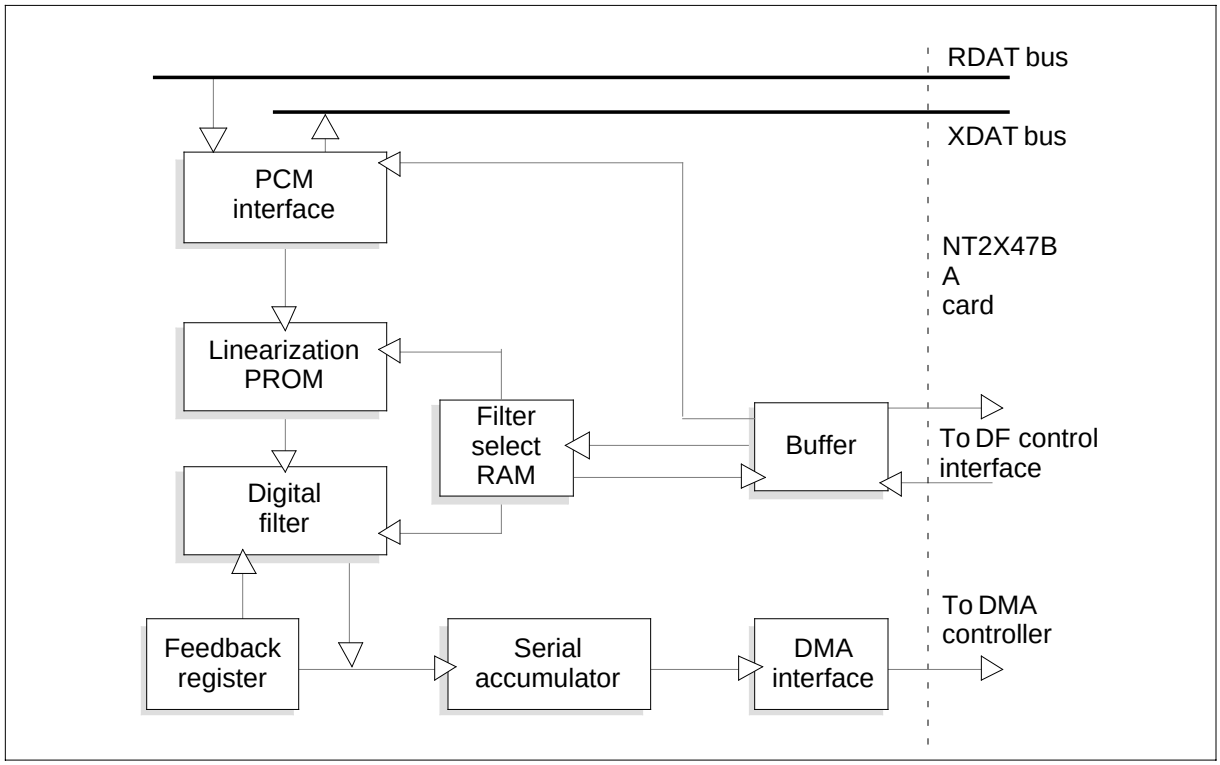
The buffer controls communication between the DF card and the CP card. The buffer does not control DMA communications. The buffer receives requests from the CP card to read the filter select RAM. The buffer passes the request to the RAM. The buffer receives the requested data from the RAM. The buffer returns the data to the CP card.

The buffer passes test requests to the DF card. The buffer sends the test data to the PCM interface. The interface sends the data over the XDAT bus.

The relationship between the functional blocks appears in the following figure.

NT2X56BA (continued)

NT2X56BA functional blocks



Technical data

The accepts PCM input signals between 4 Hz and 4 kHz at levels from -88.8 dB through +6 dB (±0.1 dB).

Dimensions

The dimensions of the NT2X56BA circuit card are as follows:

- overall height: 353 mm (13.9 in.)
- overall depth: 277 mm (10.9 in.)
- overall width: 28 mm (1.1 in.)

Power requirements

The power requirements for the NT2X56BA appear in the following table:

Power requirements

Voltage	Current
+5 V	1.45A
-12V	0.47A

Power dissipation is 12.9W.

NT2X57AA

Product description

The signal distribution (NT2X57AA) circuit card provides an interface between the Digital Multiplex System (DMS) and external relay-controlled equipment. The NT2X57AA circuit card contains 14 interface circuits. Each interface circuit has four output options. The NT2X57AA circuit card is controlled by software from the central control (CC).

Location

The card occupies one card position in a maintenance trunk module (MTM).

Functional description

The NT2X57AA circuit card activates a minimum of one relay connected to external equipment. The NT2X57AA circuit card receives and decodes the signals and activates or deactivates the selected relays. Each relay connects to a four-position switch that selects how the relays appear to the external equipment.

Functional blocks

Functional blocks of the NT2X57AA circuit card are:

- trunk logic circuits (TLC)
- relays
- output switches

Trunk Logic Circuit

The TLCs receive instructions from the MTM. The TLCs decode the instructions and activate the relays. The instructions are sent over the receive data (RDAT) bus. The instructions received determine if the TLC operates or releases the selected relay.

Each TLC controls a group of seven relays through seven signal distribution (SD) points. When a control signal activates an SD point, and the enable signal is applied to the appropriate TLS, the associated relay is operated. TLC-0 controls relays K-0 through K-6. TLC-1 controls relays K-10 through K-16.

Relays

The relays contain single-pole, double-throw (SPDT) contacts that operate under control of the TLCs. The relay contacts are miniature, flat-spring, and mounted on board. These relays allow applications that require low contact ratings and resistive loads.

Output switches

Each of the 14 relays has a four-position switch that connects to a two-position switch. When the switch positions are manually changed, the output conditions of the relay leads can also be changed. The switch settings for each relay appear in the next table.

Switch settings

Switch position S1	Switch position S2 (1)	Switch position S2 (4)	Relay K1 operated	Relay K1 released	Output lead type
A	OFF	ON	ground-closed	ground-open	single
B	OFF	ON	ground-open	ground-closed	single
A	ON	OFF	loop-closed	loop-open	double
B	ON	OFF	loop-open	loop-closed	double

Note 1: S1 positions apply to S1.00 through S1.06 and S1.10 through S1.16.

Note 2: S2 positions apply to S2.00 through S2.06 and S2.10 through S2.16.

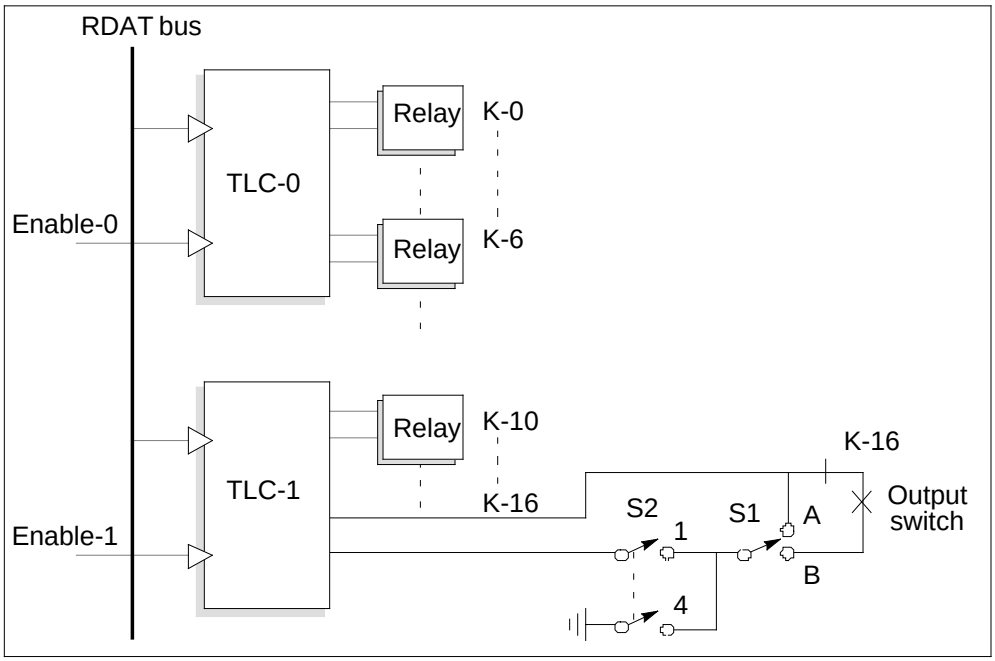
Note 3: S2 positions 2 and 3 are not connected.

Note 4: K1 states apply to K1.00 through K1.06 and K1.10 through K1.16.

The relationship between the functional blocks appears in the next figure. The detail of relay K-16 shows the operation of all 14 relays.

NT2X57AA (end)

NT2X57AA functional blocks



Technical data

The NT2X57AA output relays use contacts rated at 1A and 100V.

Physical dimensions

The dimension of the NT2X57AA circuit card are as follows:

- overall height: 353 mm (13.9 in.)
- overall depth: 267 mm (10.5 in.)
- overall width: 29 mm (1.125 in.)

Power requirements

The power requirements for the NT2X57AA appear in the next table.

Power requirements

Voltage	Current
+12V	8mA (TLC only)
+24V	180mA (all relays operated)

NT2X57AB

Product description

The signal distribution with OAU monitor (NT2X57AB) circuit card provides an interface between the Digital Multiplex System (DMS) and external relay-controlled equipment. The NT2X57AB circuit card contains 14 interface circuits. Each interface circuit has four output options. The NT2X57AB circuit card is controlled by software from the central control (CC).

Location

The NT2X57AB circuit card occupies one card position in a maintenance trunk module (MTM) or an office alarm unit (OAU).

Functional description

The NT2X57AB circuit card activates a minimum of one relay that connects to external equipment. The NT2X57AB circuit card monitors the communication path between the OAU and the CC. The NT2X57AB circuit card receives and decodes the signals and activates or deactivates the selected relays. Each relay connects to a four-position switch that selects how the relays appear to the external equipment.

Functional blocks

Functional blocks of the NT2X57AB circuit are:

- trunk logic circuits (TLC)
- relays
- output switches
- OAU monitor

Trunk Logic Circuit

The TLCs receive instructions from the MTM. The TLCs decode the instructions and activate the relays after receiving instructions over the receive data (RDAT) bus. The instructions received determine if the TLC operates or releases the selected relay.

Each TLC controls a group of seven relays through seven signal distribution (SD) points. When a control signal activates an SD point, and the enable signal is applied to the appropriate TLC, the associated relay is operated. TLC-0 controls relays K-0 through K-6. TLC-1 controls relays K-10 through K-16. TLC-0 does not operate relay K-0 directly. TLC-0 controls the relay K-0 through the OAU monitor.

NT2X57AB (continued)

Relays

The relays contain single-pole, double-throw (SPDT) contacts that operate under control of the TLCs. The relay contacts are small, flat-spring, board-mounted relays. The relay contacts allow for applications that require low contact ratings and resistive loads.

Output switches

Each of the 14 relays has a four-position switch with a connected two-position switch. When the switch positions are manually changed, the output conditions of the relay leads can also be changed. The switch settings for each relay appear in the next table.

Switch settings

Switch position S1	Switch position S2 (1)	Switch position S2 (4)	Relay K1 operated	Relay K1 released	Output lead type
A	OFF	ON	ground-closed	ground-open	single
B	OFF	ON	ground-open	ground-closed	single
A	ON	OFF	loop-closed	loop-open	double
B	ON	OFF	loop-open	loop-closed	double

Note 1: S1 positions apply to S1.00 through S1.06 and S1.10 through S1.16.

Note 2: S2 positions apply to S2.00 through S2.06 and S2.10 through S2.16.

Note 3: S2 positions 2 and 3 are not connected.

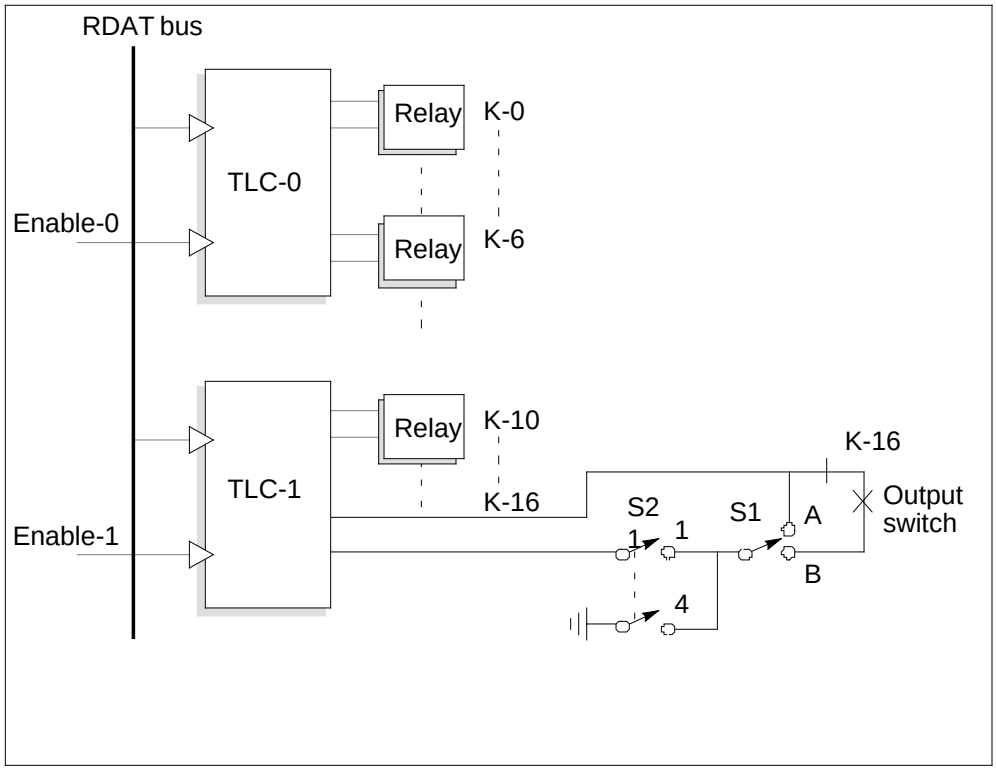
Note 4: K1 states apply to K1.00 through K1.06 and K1.10 through K1.16.

Office alarm unit monitor

The office alarm unit (OAU) monitor consists of a 5 second timer. The OAU monitor connects TLC-0 to K-0. The OAU monitor consists of a 5 second timer. The OAU monitor connects TLC-0 to K-0. The OAU monitor operates relay K-0 as long as the timer is in operation. TLC-0 monitors a signal from the OAU. The signal cycles at a rate of 60 impulses each minute during correct communication between the OAU and the CC. TLC-0 uses the signal to refresh the timer. This action keeps the timer in operation when a signal is present. If communication between the OAU and the CC stops, the signal is not present and the monitor timer stops. When the timer is no longer in operation, the monitor releases relay K-0.

The next figure describes the relationship between functional blocks. The detail of relay K-16 describes the operation of the 14 relays.

Figure NT2X57AB functional blocks



Technical data

The NT2X57AB circuit card output relays use contacts that rate at 1A and 100V.

Dimensions

Dimensions for the NT2X57AB circuit card are:

- height: 353 mm (13.9 in.)
- depth: 267 mm (10.5 in.)
- width: 29 mm (1.125 in.)

NT2X57AB (end)

Power requirements

The next table lists the power requirements for the NT2X57AB.

Power requirements

Voltage	Current
+12V	8mA (TLC only)
+24V	180mA (all relays operated)

NT2X58AC

Description

The NT2X58AC maintenance trunk module (MTM) links channels to other channels. The MTM links channels from the network modules (NM) to channels on test or service circuit cards installed in the MTM. This MTM functions as a switch center for control messages. The control module in the DMS-core and test or service circuit cards exchange control messages. Internally, the MTM provides the necessary low-voltage supplies, and the necessary connections. The exchange data between the test circuit cards and the low-voltage supplies requires these low-voltage supplies and connections.

The MTM contains a control section that includes the NT2X45AB trunk module (TM) interface. The control section of the MTM contains the NT0X70AA TM processor, and the NT2X53AA TM control cards. The TM control cards make and maintain connections. Direct data exchange between the test cards occurs through two buses, maintenance (MAINT) 1 and 2. Data exchange between the test cards does not use XDAT or RDAT buses. The MTM includes two power converter cards and a maximum of 12 test circuit cards. The TM has one power converter card.

The MTM provides digital and analog looparound provisions. In digital looparound, the receive data (RDAT) bus loops back to the transmit data (XDAT) bus. The RDAT/XDAT connections loop back to the trunk logic circuits (TLC) in the test and service cards. In analog looparound the receive pulse amplitude modulation (RPAM) bus loops to the transmit PAM (XPAM) bus. The common control section controls both looparound functions. The common control section sends messages to different service and test cards as necessary.

Looparound circuits are available in each test or service card for channel-specific looparound tests. The common control section controls these circuits. The common control section addresses specified test or service cards through their TLC.

Parts

The MTM contains test and service circuit cards and the following components:

- NT0X50AA-Filler faceplate or panel
- NT0X70AA-TM processor card
- NT2X06AB-Power converter
- NT2X09AA-Power converter
- NT2X45AB-TM interface card

NT2X58AC (continued)

- NT2X53AA-TM control card
- NT2X59AA-Group coder-decoder (CODEC) and tone circuit card

Design

The following table and figure describe the design of the NT2X58AC.

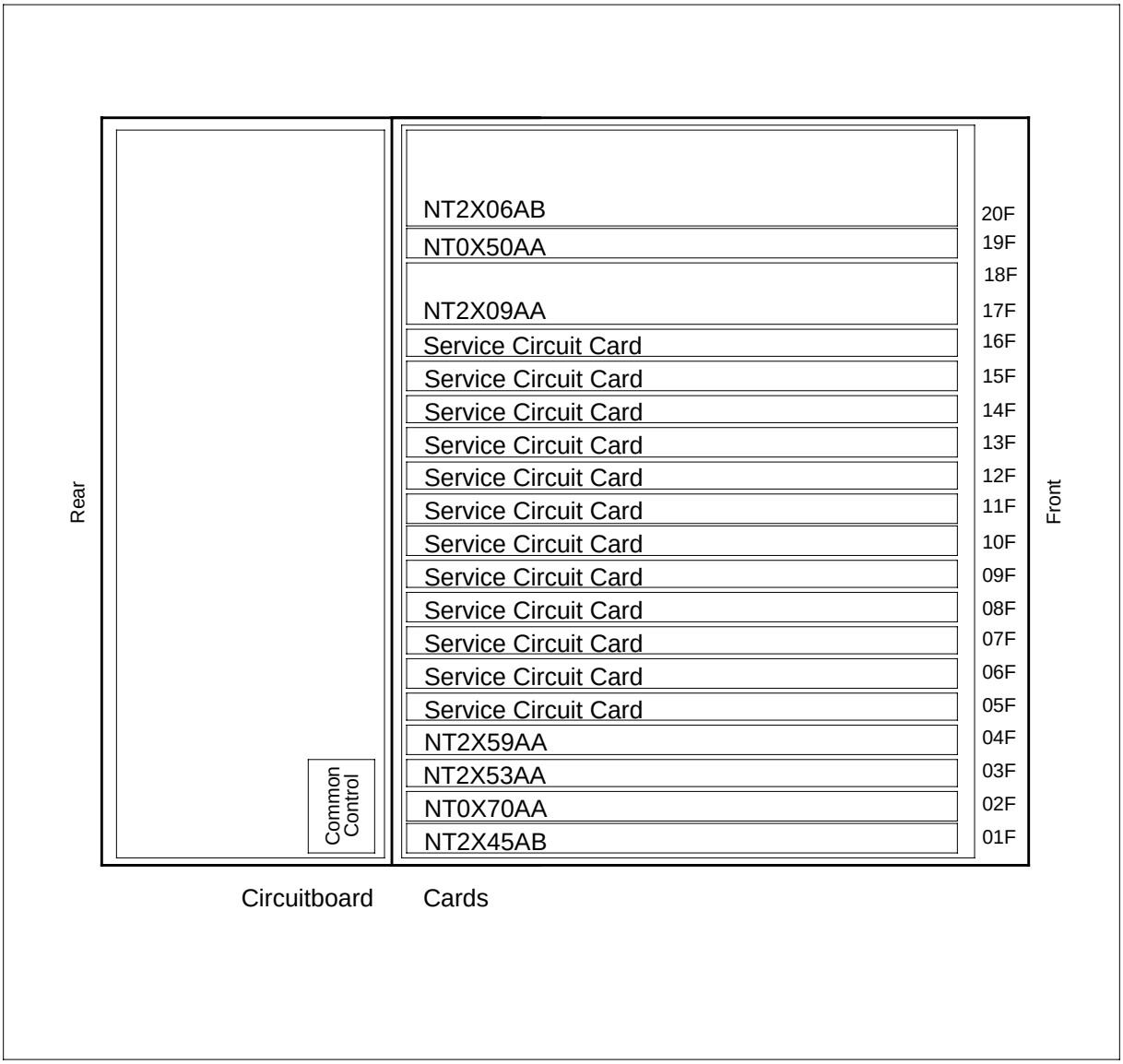
NT2X58AC component (Sheet 1 of 2)

PEC	Slot	Description
	5F-16F	*Test and service circuit card* Maintenance programs control test and service cards that use the RDAT, XDAT and MAINT buses. The maintenance programs reside in the control module of the central switch. The software provides the correct control codes and enabling signals. These codes and signals function with test and service cards installed in the MTM.
NT0X50AA	19F	*Filler faceplate* Use the filler faceplate or panel to fill empty card slots in the module. A maximum of five spare card slots are present in each module. Three of the slots (15, 16, and 17) have access to the signaling processor (SP) address bus and the parallel speech bus. The spare slots that remain (13 and 19) do not have access.
NT0X70AA	2F	*Trunk module processor card* The TM processor performs or controls all operations that the components of the MTM accomplish. The card contains a firmware-driven microprocessor and two RAMs. One RAM stores program information. The other RAM stores operational information. Operational information includes connection information for PCM channel-to-trunk assignments. The card includes circuits that generate the clock signal, check parity, and perform synchronization.
NT2X06AB	20F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards in the module need. The NT2X06AB converter produces a 5V, 40A output. The power converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The power converter includes faceplate test jacks, and a faceplate light-emitting diode (LED) state indicator.

NT2X58AC component (Sheet 2 of 2)

PEC	Slot	Description
NT2X09AA	17F	*Power converter* The power converter converts the -48V dc to the lower voltages needed by the circuit cards in the module. The NT2X09AA converter produces -5V, -15V, +5V, +12V, and +24V dc. The power converter includes a low-voltage monitor circuit, overvoltage and overcurrent protection, faceplate test jacks, and a faceplate LED state indicator.
NT2X45AB	1F	*Trunk module interface card* The TM interface card serves as the network interface for both planes of the network. The TM interface card provides two two-way interfaces for the two transmission paths from both network planes. The TM interface card contains message registers and bit and channel timing circuits. The TM interface card contains circuits to check parity and circuits that format data again.
NT2X53AA	3F	*Trunk module control card* The TM control card contains the circuit controllers that handle different messages. The TM control card communicates information with the processor card over data and address buses. The TM control card produces enable signals for the circuits on the test and service circuit cards.
NT2X59AA	4F	*Group CODEC and tone circuit card* The group coder-decoder (CODEC) and tone circuit card perform the same functions as in the TM. The group CODEC and tone circuit card create pulse-code-modulation (PCM) and words from PAM analog samples. The group CODEC and tone circuit card decodes PCM word streams into analog samples. The group CODEC and tone card include the ROMs that contain the digital tones for dialing and signaling.

NT2X58AC components



NT2X58AE

Description

The NT2X58AE remote service module (RSM) and a NT2X46AA or NT2X46AB metallic test access (MTA) unit provide control and connections for remote metallic test access. The RSM and MTA provide these functions through a host office to subscriber line circuits connected to a group of remote line modules (RLM). The location of the RSM is normally in the NT6X10AA remote service equipment frame. The RSM is a modified version of the maintenance trunk module (MTM). The RSM provides an interface for external alarm circuits at the remote site. If an installed NT2X84AB digitone receiver is present, the RSM provides optional emergency stand-alone (ESA) service circuits. These circuits function if a DS-1 link fails and disconnects an RLM from its host office.

The RSM does not connect directly to the DMS network. The RSM does not have autonomous circuits. The remote line controller (RLC) in the RLM provides control functions. Communication with the host office is not direct. There are two common circuit cards in the module. One of these cards is the NT3X51AA RLM service shelf interface circuit pack (CP). Other cards in the module are the NT2X59AA group coder-decoder (CODEC) and tone circuit cards. These common circuit cards provide internal shelf control and control functions for the MTA. The RLM service shelf interface CP connects to the control buses, terminal transmit, and receive of the RLC. The transmit data (XDAT) and receive data (RDAT) buses carry speech or data. The XDAT and RDAT carry speech or data to and from specified test access or service cards. The control bus carries the address the control section uses to generate enable signals. Enable signals, when required, activate the test access and service cards. The RLC controls the trunk/service circuit-speech channel association. Two maintenance buses, MAINT 1 and 2, can transfer data between the trunk/service circuit cards.

Line tests are performed and the results are transmitted to the DMS control module (CM). Terminal digroup 19 of the RLC and the message channel of the first DS-1 link transmit the results. To test a line, the NT2X50AB minibar driver card in the RSM selects a crosspoint on the MTA unit. The crosspoint associates with the test access (TA) bus. The TA bus connects to the group of line drawers that contain the line circuit to test. The NT2X11AA digital line test unit (LTU) card and the NT2X10AA analog LTU cards in the RSM control test conditions.

The RSM includes a talk monitor circuit that functions in conjunction with the group CODEC and tone card. The RSM includes the test trunk cards to test the speech path of subscriber loop and line circuits. The module functions as an interface between digital circuits in the module and external relay controlled devices. The module functions as an interface between remote-site alarms and

NT2X58AE (continued)

the host office. The signal distribution (SD) and scan cards handle these functions.

The RSM requires lower voltages. The RSM includes power converters, NT2X09AA and NT2X06AB, that convert the -48V dc into lower voltages.

Parts

The RSM consists of the following components:

- NT0X10AA-Scan card
- NT0X50AA-Filler face plate
- NT2X06AA-Power converter
- NT2X09AA-Power converter
- NT2X10AA-Analog LTU card
- NT2X11AA-Digital LTU card
- NT2X48AB-Digitone receiver card (ESA option only)
- NT2X50AB-Minibar driver card
- NT2X57AA-SD card
- NT2X59AA-Group CODEC and tone circuit card
- NT2X90AB-Test trunk card
- NT3X51AA-RLM service shelf interface CP

Design

The following table and figure describe the design of a normal RSM. The type and function of the RSM in specified applications can cause the layout of current modules to be different.

NT2X58AE components (Sheet 1 of 4)

PEC	Slot	Description
NT0X10AA	8F	*Scan card* The scan card detects external alarms like the aisle alarm on a frame supervisory panel (FSP). The scan card relays the information to the host office. The scan card monitors the condition of contacts at the remote site and relays the information to the host office. The scan cards relays the information through the service shelf interface card, the RLC, and the DS-1 message channel.

NT2X58AE components (Sheet 2 of 4)

PEC	Slot	Description
NT0X50AA	19F	*Filler face plate* Use the filler face plate or panel to fill empty card slots in the shelves. A maximum of five spare card slots are present in each module. Slots 15, 16, and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. The spare slots that remain (13 and 19) do not have access.
NT2X06AA	20F	*Power converter* The power converters change the -48V dc office battery voltage to the lower voltages the circuits in the RSM need. The NT2X06AA converter, which occupies two slots, produces a 5V, 40A output.
NT2X09AA	17F, 18F	*Power converter* The power converters change the -48V dc office battery voltage into the lower voltages the circuits in the RSM need. The NT2X09AA power converter, a two-slot card, produces multiple outputs.
NT2X10AA	9F	*Analog line test unit card* The analog and digital LTUs function together and are always in pairs in card slots next to each other. The analog LTU is in an odd-numbered slot, the digital LTU is in an even-numbered slot. The two cards provide test conditions for tests on line circuits. The RLC through the service shelf interface card controls the two cards.
NT2X11AA	10F	*Digital line test unit card* The analog and digital LTUs function together and are always in pairs in card slots next to each other. The analog LTU is in an odd-numbered slot, the digital LTU is in an even-numbered slot. Both cards provide test conditions for tests on line circuits. The RLC through the service shelf interface card controls both cards.

NT2X58AE (continued)

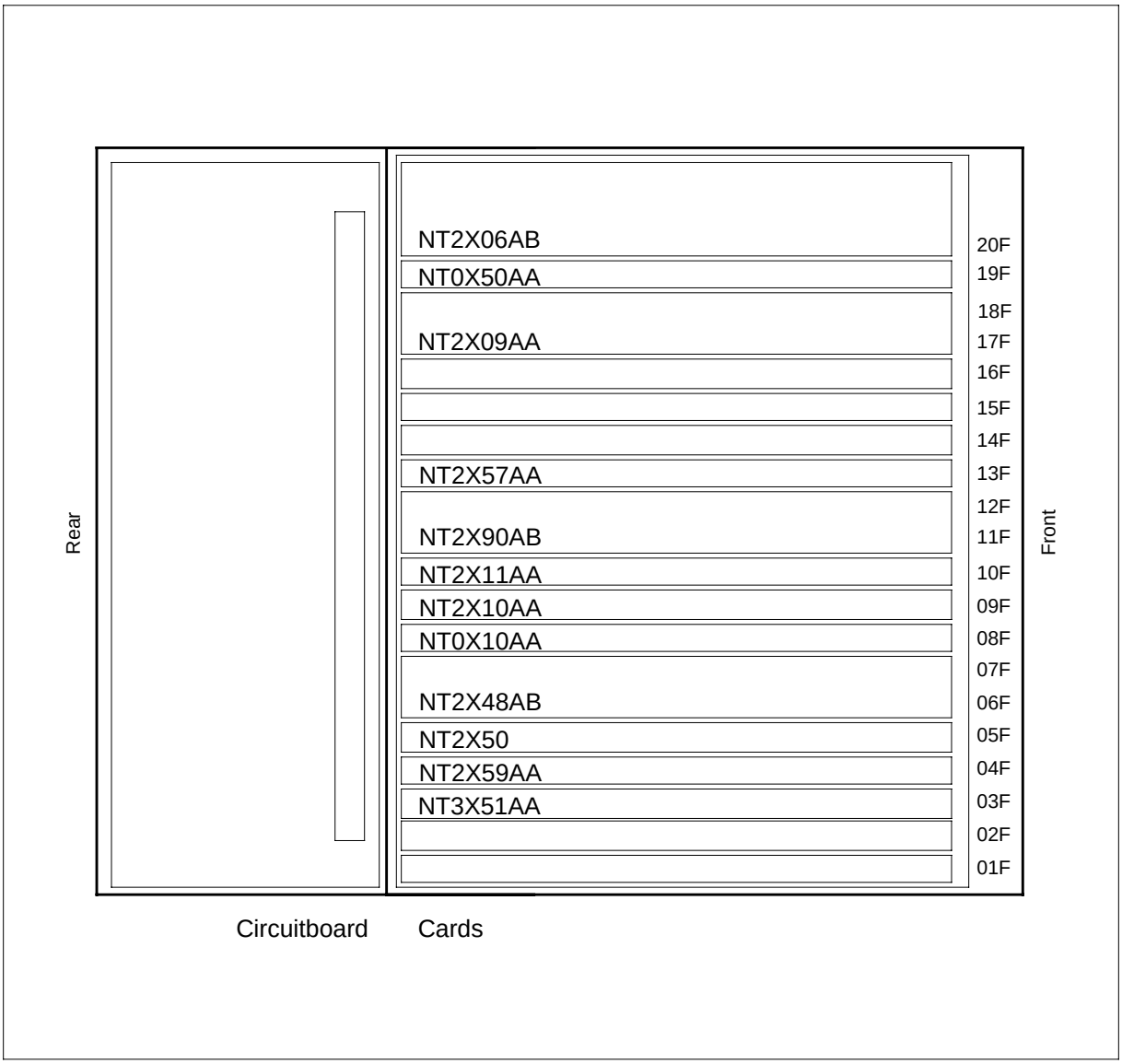
NT2X58AE components (Sheet 3 of 4)

PEC	Slot	Description
NT2X48AB	6F	*Digitone receiver card (ESA option only)* Use the digitone receiver card for an RSM with an incorporated ESA option. The digitone receiver card must be in slots 6 and 7 of the RSM. This card replaces the digitone receiver card in the host office if the DS-1 links fail. Each digitone card provides four receiver functions and occupies two cards slots. When the digitone receiver card includes the ESA option, each RSM is dedicated to a single RLM.
NT2X50AB	5F	*Minibar driver card* The RLC controls the minibar driver card through the service shelf interface card in the RSM. The minibar driver card selects the specified MTA crosspoints required to test a line circuit. The crosspoints associate with the TA bus connected to the group of line drawers. The group of line draws contain the line circuit being tested. The control words address to the circuit through the bus interface card (BIC) selects the specified line circuit tested
NT2X57AA	13F	*Signal distribution card* The SD card functions as an interface. The SD is an interface between digital circuits in the RLM and a maximum of 14 external relay-controlled devices. A remote site maintains the external relay-controlled devices. A message from the computing module (CM) at the host office can activate a relay in the SD card. The activation messages reach the SD card through the DS-1 message channel and digroup 19 of the RLC. The service shelf interface card carries the activation message.
NT2X59AA	4F	*Group CODEC and tone circuit card* The function of the group CODEC and tone card are the same as in the MTM shelf. The group CODEC and tone card creates pulse-code-modulation (PCM) words from pulse amplitude modulated (PAM) analog samples. The group CODEC and tone card decodes PCM word streams into analog samples. The group CODEC and tone card can function with test trunk cards, in the talk monitor circuit. The monitor circuit checks the operation of the speech paths of subscriber loops and line circuits to the host office.

NT2X58AE components (Sheet 4 of 4)

PEC	Slot	Description
NT2X90AB	11F,12F	*Test trunk card* The test trunk card works with the group CODEC and tone card to provide talk monitor functions. The card is usually next to an LTU pair.
NT3X51AA	3F	*Remote line module service shelf interface circuit pack* The RLM service shelf interface CP provides internal control for the circuits in the RSM. The RLM service shelf interface CP provides control for the MTA unit. The CP is responsible for selecting MTA crosspoints and line circuits to test. The CP does not have autonomous control circuits. The RLC in the prime RLM bay (normally bay 0), controls the card. Control automatically switches to the RLC in the other bay (normally bay 1) if the prime RLC fails.

NT2X58AE components



NT2X58AF

Description

The NT2X58AF office alarm unit (OAU) links channels from the network modules (NM) with circuits designed to detect and operate office alarms. The OAU is like the maintenance trunk module (MTM). The OAU contains a control section, that has the NT2X45AB trunk module (TM) interface circuit pack and the NT0X70AA TM processor circuit pack (CP). The OAU also has NT2X53AA control circuit cards. The OAU includes many different alarm circuit cards. There is no coder-decoder (CODEC) and tone card because OAU does not process transmit and receive pulse-amplitude-modulated (PAM) signals. In addition to common data buses, data can transfer between cards over two separate maintenance buses.

The OAU includes the NT2X06AB and NT2X09AA power converters. These power converters produce the low-voltage supplies. These power converters provide connections. The exchange of data between alarm circuit cards and low-voltage supplies requires these low-voltage supplies and these connections. The OAU includes a separately fused -48 V bus and ground return for the alarm circuits.

Each alarm circuit can associate with a maximum of 30 speech or data channels, as the DMS system software directs. Two additional channels are used for signaling and control. The alarm circuit cards used in the OAU include three NT2X57AA signal distribution (SD) cards. The alarm circuit cards used in the OAU include between three and five NT0X10AA scan detector cards. The alarm circuit cards used in the OAU include different office alarm circuits. The alarm circuits provide an interface for visual and audible alarm signals.

The three SD cards act as an interface between the alarm system software and relay-controlled equipment in the unit. The scan detector cards detect external contact states. The cards convert the contact states to trunk logic circuits (TLC) scan states. The cards convert the contact states to different office alarm circuits provide an interface for visual and audible alarm signals.

The OAU holds a total of 11 alarm circuit cards. The current number of scan detector and different alarm cards in the OAU shelf depends on the size of the office. The unit must have a minimum of three installed scan detector cards.

The OAU includes digital and analog looparound provisions. In digital looparound, the receive data (RDAT) bus loops back to the transmit data (XDAT) bus. The RDAT bus loops back to the RDAT/XDAT connections to the TLCs in the test and service cards. The receive PAM (RPAM) bus loops to the transmit PAM (XPAM) bus for analog looparound. The common control section, controls both looparound functions. The common control section sends messages addressed to the different service and test cards as necessary.

NT2X58AF (continued)

Looparound circuits are available in each test or service card for channel-specific looparound tests. The common control section controls this activity. The common control section addresses specified test or service cards through their TLC.

Parts

The OAU contains alarm circuit cards and the following components:

- NT0X10AA—Scan circuit card
- NT0X50AA—Filler face plate
- NT0X50AC—Filler face plate
- NT0X70AA—TM processor card
- NT2X06AB—Power converter
- NT2X09AA—Power converter
- NT2X45AB—TM interface card
- NT2X53AA—TM control card
- NT2X57AA—Alarm circuit card
- NT2X59AA—Alarm circuit card
- NT3X82AA—Alarm circuit card
- NT3X85AA—Alarm circuit card

Design

The following table and figure describe the design of the NT2X58AF.

NT2X58AF parts (Sheet 1 of 6)

PEC	Slot	Description
NT0X10AA	5F, 6F	*Scan circuit card* The scan circuit cards include SD cards (NT2X57AA) and different scan detector cards (NT0X10AA). The scan circuit cards include three types of different office alarm circuit cards. The SD is an interface between alarm system software and relay-controlled components. The relay-controlled components are in the unit. The SD activates audible alarms, visual alarms, or associated circuits like the remote alarm transfer circuit. The scan detector cards monitor the state of the alarm system hardware. The cards monitor the alarm system hardware to detect alarm conditions or the position of manual control switches. The OAU shelf uses three types of different office alarms. The OAU uses office alarm circuit 1, office alarm circuit 2, and office alarm circuit 3. Office alarm circuit 1 contains relays that control the alarm grouping circuit and the power plant exit lamps. Office alarm circuit 2 card contains relays that control the remote alarm transfer circuit and the trunk test center (TTC) chime. Office alarm circuit 2 card contains relays that control the TTC night alarm transfer circuit, and the DMS exit pilot lamps. Office alarm circuit 2 card contains a hardware interrupter circuit for the major chime. Office alarm circuit 3 card, a two-slot card, contains a 130-V power supply and a 20-Hz ringing supply. Office alarm circuit 3 card controls relays for the OAU and dead-system alarms. Office alarm circuit 3 card controls a transformer for the odd-aisle multiple of the local talk line circuit.
NT0X50AA	19F	*Filler face plate* Use the filler face plate or panel to fill empty card slots in the unit. A maximum of five spare card slots are present in each unit. Slots 15, 16, and 17 have access to the SP address bus and the parallel speech bus. The spare slots, 13 and 19, that remain do not have access.
NT0X50AC	10F-12F, 14F	*Filler face plate* Use the filler face plate or panel to fill empty card slots in the unit. A maximum of five spare card slots are available in each unit. Slots 15, 16, and 17 have access to the SP address bus and the parallel speech bus. The spare slots, 13 and 19, that remain do not have access.

NT2X58AF (continued)

NT2X58AF parts (Sheet 2 of 6)

PEC	Slot	Description
NT0X70AA	2F	*Trunk module processor card* The TM processor card performs or controls all of the operations accomplished by the circuits of the OAU. The TM processor card contains a firmware-driven microprocessor. The TM processor contains two RAMs. One RAM stores program information and one RAM stores operational information. The TM processor includes circuits that generate the clock signal, check parity, and perform synchronization.
NT2X06AB	20F	*Power converter* The power converter converts the -48V dc to the lower voltages the circuit cards in the unit need. The NT2X06AB converter produces a 5V, 40A output. The power converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The power converter includes face plate test jacks and a face plate light-emitting diode (LED) status indicator.
NT2X09AA	17F	*Power converter* The power converter converts the -48V dc to the lower voltages the circuit cards in the unit need. The NT2X09AA converter produces -5V, -15V, +5V, +12V, and +24V dc. The power converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The power converter provides face plate test jacks and a face plate LED state indicator.
NT2X45AB	1F	*Trunk module interface card* The TM interface card serves as the network interface for the two planes of the network. The TM interface card provides two two-way interfaces for the two transmission paths from both network planes. The TM interface card contains message registers and bit and channel timing circuits. The TM interface card contains parity-check circuits, and circuits that format data again.
NT2X53AA	3F	*Trunk module control card* The TM control card contains circuit controllers that handle different messages. The TM control card communicates information with the processor circuit card. Communication occurs over data and address buses. The TM control card produces enable signals for the circuits on the service and test cards.

NT2X58AF parts (Sheet 3 of 6)

PEC	Slot	Description
NT2X57AA	7F-9F	*Alarm circuit card* The alarm circuit cards include SD cards (NT2X57AA), and different scan detector cards (NT0X10AA). The scan circuit cards include three types of different office alarm circuit cards. The SD is an interface between alarm system software and relay-controlled components. The relay-controlled components are in the unit. The SD activates audible alarms, visual alarms, or associated circuits like the remote alarm transfer circuit. The scan detector cards monitor the state of the alarm system hardware. The cards monitor the alarm system hardware to detect alarm conditions or the position of manual control switches. The OAU shelf uses three types of different office alarms. The OAU uses office alarm circuit 1, office alarm circuit 2, and office alarm circuit 3. Office alarm circuit 1 contains relays that control the alarm grouping circuit and the power plant exit lamps. Office alarm circuit 2 card contains relays that control the remote alarm transfer circuit and the trunk test center (TTC) chime. Office alarm circuit 2 card contains relays that control the TTC night alarm transfer circuit, and the DMS exit pilot lamps. Office alarm circuit 2 card contains a hardware interrupter circuit for the major chime. Office alarm circuit 3 card, a two-slot card, contains a 130-V power supply and a 20-Hz ringing supply. Office alarm circuit 3 card controls relays for the OAU and dead-system alarms. Office alarm circuit 3 card controls a transformer for the odd-aisle multiple of the local talk line circuit.

NT2X58AF (continued)

NT2X58AF parts (Sheet 4 of 6)

PEC	Slot	Description
NT2X59AA	4F	*Alarm circuit card* The alarm circuit cards include SD cards (NT2X57AA) and different scan detector cards (NT0X10AA). The scan circuit cards include three types of different office alarm circuit cards. The SD is an interface between alarm system software and relay-controlled components. The relay-controlled components are in the unit. The SD activates audible alarms, visual alarms, or associated circuits like the remote alarm transfer circuit. The scan detector cards monitor the state of the alarm system hardware. The cards monitor the alarm system hardware to detect alarm conditions or the position of manual control switches. The OAU shelf uses three types of different office alarms. The OAU uses office alarm circuit 1, office alarm circuit 2, and office alarm circuit 3. Office alarm circuit 1 contains relays that control the alarm grouping circuit and the power plant exit lamps. Office alarm circuit 2 card contains relays that control the remote alarm transfer circuit and the trunk test center (TTC) chime. Office alarm circuit 2 card contains relays that control the TTC night alarm transfer circuit, and the DMS exit pilot lamps. Office alarm circuit 2 card contains a hardware interrupter circuit for the major chime. Office alarm circuit 3 card, a two-slot card, contains a 130-V power supply and a 20-Hz ringing supply. Office alarm circuit 3 card controls relays for the OAU and dead-system alarms. Office alarm circuit 3 card controls a transformer for the odd-aisle multiple of the local talk line circuit.

NT2X58AF parts (Sheet 5 of 6)

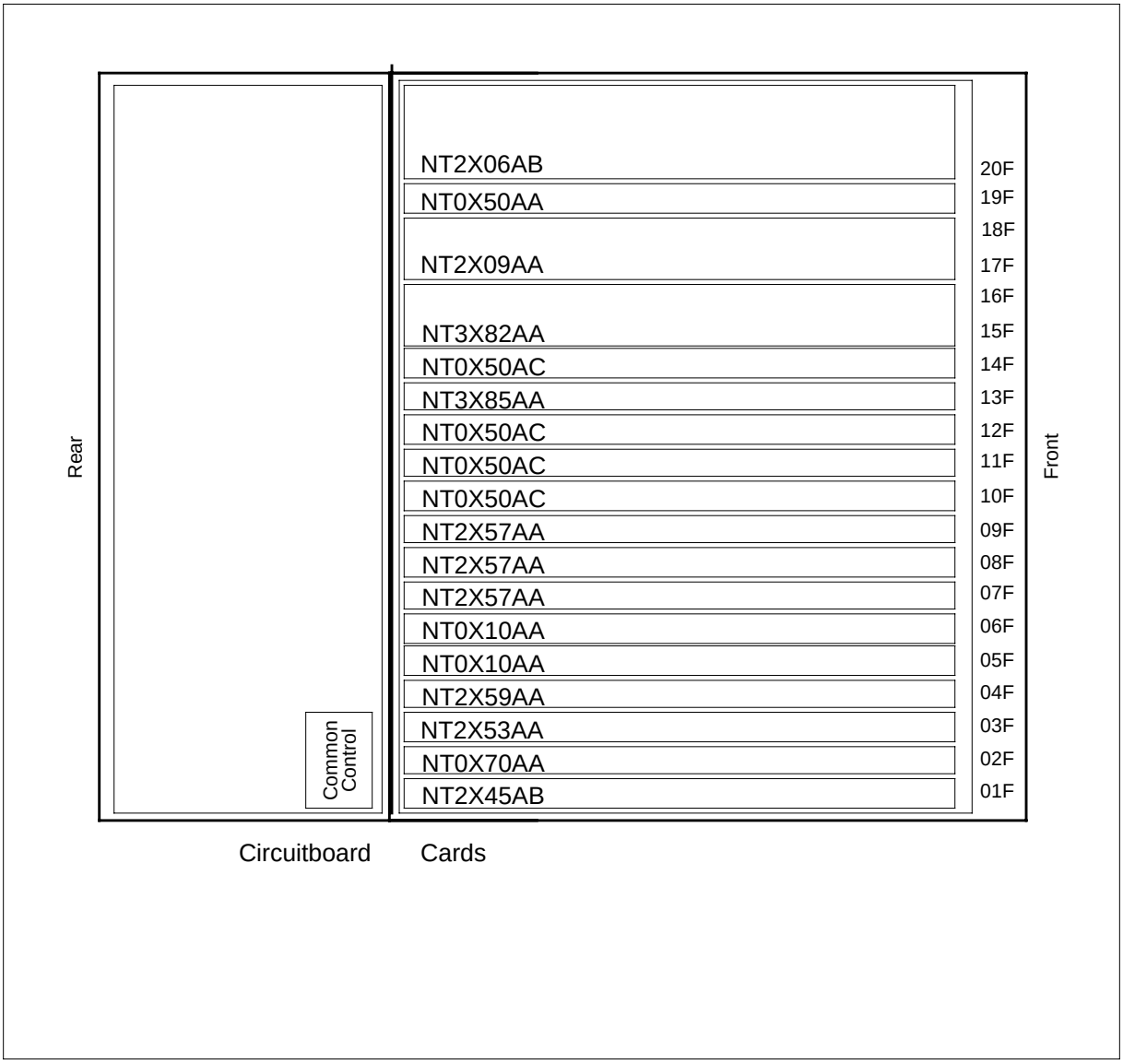
PEC	Slot	Description
NT3X82AA	15F	*Alarm circuit card* The alarm circuit cards include SD cards (NT2X57AA) and different scan detector cards (NT0X10AA). The scan circuit cards include three types of different office alarm circuit cards. The SD is an interface between alarm system software and relay-controlled components. The relay-controlled components are in the unit. The SD activates audible alarms, visual alarms, or associated circuits like the remote alarm transfer circuit. The scan detector cards monitor the state of the alarm system hardware. The cards monitor the alarm system hardware to detect alarm conditions or the position of manual control switches. The OAU shelf uses three types of different office alarm. The OAU uses office alarm circuit 1, office alarm circuit 2, and office alarm circuit 3. Office alarm circuit 1 contains relays that control the alarm grouping circuit and the power plant exit lamps. Office alarm circuit 2 card contains relays that control the remote alarm transfer circuit and the trunk test center (TTC) chime. Office alarm circuit 2 card contains relays that control the TTC night alarm transfer circuit, and the DMS exit pilot lamps. Office alarm circuit 2 card contains a hardware interrupter circuit for the major chime. Office alarm circuit 3 card, a two-slot card, contains a 130-V power supply and a 20-Hz ringing supply. Office alarm circuit 3 card controls relays for the OAU and dead-system alarms. Office alarm circuit 3 card controls a transformer for the odd-aisle multiple of the local talk line circuit.

NT2X58AF (end)

NT2X58AF parts (Sheet 6 of 6)

PEC	Slot	Description
NT3X85AA	13F	*Alarm circuit card* The alarm circuit cards include SD cards (NT2X57AA) and different scan detector cards (NT0X10AA). The scan circuit cards include three types of different office alarm circuit cards. The SD is an interface between alarm system software and relay-controlled components. The relay-controlled components are in the unit. The SD activates audible alarms, visual alarms, or associated circuits like the remote alarm transfer circuit. The scan detector cards monitor the state of the alarm system hardware. The cards monitor the alarm system hardware to detect alarm conditions or the position of manual control switches. The OAU shelf uses three types of different office alarms. The OAU uses office alarm circuit 1, office alarm circuit 2, and office alarm circuit 3. Office alarm circuit 1 contains relays that control the alarm grouping circuit and the power plant exit lamps. Office alarm circuit 2 card contains relays that control the remote alarm transfer circuit and the trunk test center (TTC) chime. Office alarm circuit 2 card contains relays that control the TTC night alarm transfer circuit, and the DMS exit pilot lamps. Office alarm circuit 2 card contains a hardware interrupter circuit for the major chime. Office alarm circuit 3 card, a two-slot card, contains a 130-V power supply and a 20-Hz ringing supply. Office alarm circuit 3 card controls relays for the OAU and dead-system alarms. Office alarm circuit 3 card controls a transformer for the odd-aisle multiple of the local talk line circuit.

NT2X58AF parts



NT2X58AG

Description

The NT2X58AG maintenance trunk module (MTM) for the digital recorded announcement machine (DRAM) contains circuits. These circuits store recorded phrases. The MTM module, in conjunction with the DMS control module (CM), routes circuits the recorded phrases to speech channels.

The module is like the NT2X58AC MTM except that a group of circuit cards replaces the service circuit cards. This group of cards is the DRAM unit. The intercard bus links the first ten module slots. The MTM uses even-odd connections between cards.

The DRAM control section establishes and maintains connections and controls the operation of the module. The DRAM control section is identical to the control section in the MTM. The DRAM control section contains the following cards:

- NT2X45AB trunk module (TM) interface card
- NT2X70AA TM processor card
- NT2X53AA TM control card
- NT2X59AA group coder-decoder (CODEC)
- tone circuit cards.

The DRAM unit contains a speech processor, a microprocessor controller, and speech memory. Circuit cards house the speech processor, microprocessor controller and speech memory. The microprocessor controller and speech processor are on the NT1X75BA enhanced digital recorded announcement (DRA) controller card. The cards that can provide speech memory are as follows:

- NT1X76AA PROM
- NT1X77AA RAM
- NT1X79AA EEPROM

The unit must contain a minimum of one PROM or RAM card. The unit can use a maximum of any eight PROM, EEPROM, and RAM cards.

Parts

The MTM for DRAM contains the following components:

- NT0X50AA—Filler face plate or panel.
- NT0X50AC—Filler face plate or panel.

- NT0X70AA—TM processor card.
- NT1X75BA—DRA controller card.
- NT1X76AA—PROM cards.
- NT1X77AA—RAM cards.
- NT1X79AA—EEPROM cards.
- NT2X06AB—Power converter.
- NT2X09AA—Power converter.
- NT2X45AB—TM interface card.
- NT2X53AA—TM control card.
- NT2X59AA—Group CODEC and tone circuit card.

Design

The following table and figure describe the design of the NT2X58AG.

NT2X58AG components (Sheet 1 of 6)

PEC	Slot	Description
NT0X50AA	19F	*Filler face plate* The filler face plate or panel fills empty card slots in the module. A maximum of five spare card slots can be present in each module. Slots 15, 16, and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. Slots 13 and 19 do not have access to the address bus and the parallel speech bus.
NT0X50AC	14F-16F	*Filler face plate* The filler face plate or panel fills empty card slots in the module. A maximum of five spare card slots can be present in each module. Slots 15, 16, and 17 have access to the SP address bus and the parallel speech bus. Slots 13 and 19 do not have access to the address bus and the parallel speech bus.

NT2X58AG (continued)

NT2X58AG components (Sheet 2 of 6)

PEC	Slot	Description
NT0X70AA	2F	*Trunk module processor card* The TM processor card performs or controls operations that the components of the MTM accomplish. Firmware drives the microprocessor. The TM processor card contains a microprocessor. The TM processor contains two RAMs. One RAM stores program information and one RAM stores operational information. Operational information includes connection information for pulse-code modulation (PCM) channel-to-trunk assignments. The TM processor card includes circuits that generate the clock signal, check parity, and perform synchronization.
NT1X75BA	5F	*Digital recorded announcement controller card* The DRAM unit contains a DRA controller card (NT1X75BA), PROM (NT1X76) cards, EEPROM (NT1X79AA) cards and RAM (NT1X77AA) cards. The unit must contain at least one PROM or RAM card. The unit can use a maximum of any eight PROM, RAM, and EEPROM cards. Manual switches configure the DRA controller for 8-channel, 16-channel, 24-channel, or 30-channel operation. The DRA controller controls the transmission and reception of messages between the DRAM unit and the DMS CM. The DRA controller selects and retrieves recorded phrases from the PROM, EEPROM, and RAM cards. The DRA controller transmits recorded phrases on speech link channels. The DRA controller controls the recording of new announcements and assigns the announcements to an appropriate section of memory. Each PROM, EEPROM and RAM memory card contains storage space for phrases. These phrases can be a maximum of 31 s in length. The CM instructs the DRA controller card to transmit complete announcements and to join incomplete announcements to complete messages. Procedures in the DMS-100 Menu Commands Reference Manual, 297-1001-801 allow manual control from the MAP level during maintenance procedures. These procedures also allow manual control from the MAP level during new message recording. The RAM card (NT1X77AA) stores complete and incomplete announcements that are recorded on site. These announcements are made on a PCM-channel network connection. These announcements are lost if you remove the card from the slot. The EEPROM card (NT1X79AA) stores messages recorded on site. These messages are not lost when you remove the card. To remove the messages you must erase the memory electrically.

NT2X58AG components (Sheet 3 of 6)

PEC	Slot	Description
NT1X76AA	6F-8F	*Programmable read-only memory cards* The DRAM unit contains a DRA controller card (NT1X75BA), PROM (NT1X76) cards, EEPROM (NT1X79AA) cards, and RAM (NT1X77AA) cards. The unit must contain a minimum of one PROM or RAM card. The unit can use a maximum of any eight PROM, RAM, and EEPROM cards. Manual switches configure the DRA controller for 8-channel, 16-channel, 24-channel, or 30-channel operation. The DRA controller controls the transmission and reception of messages between the DRAM unit and the DMS CM. The DRA controller selects and retrieves recorded phrases from the PROM, EEPROM, and RAM cards. The DRA controller transmits recorded phrases on selected speech link channels. The DRA controller controls the recording of new announcements and assigns the announcements to an appropriate section of memory. Each PROM, EEPROM, and RAM memory card contains storage space for phrases. These phrases can be a maximum of 31 s in length. The CM instructs the DRA controller card to transmit complete announcements and to join incomplete announcements to complete messages. Procedures in the DMS-100 Menu Commands Reference Manual, 297-1001-801 allow manual control from the MAP level during maintenance procedures. These procedures also allow manual control from the MAP level during new message recording. The RAM card (NT1X77AA) stores complete and incomplete announcements, that are recorded on site. These announcements are made over a PCM-channel network connection. These announcements are lost if you remove the card from the slot. The EEPROM card (NT1X79AA) stores messages recorded on site, and the messages are not lost when you remove the card. To remove the messages erase the memory electrically.

NT2X58AG (continued)

NT2X58AG components (Sheet 4 of 6)

PEC	Slot	Description
NT1X77AA	9F-11F	*Random-access memory cards* The DRAM unit contains a DRA controller card (NT1X75BA), PROM (NT1X76) cards, EEPROM (NT1X79AA) cards, and RAM (NT1X77AA) cards. The unit must contain a minimum of one PROM or RAM card. The unit can use a maximum of any eight PROM, RAM, and EEPROM cards. Manual switches configure the DRA controller for 8-channel, 16-channel, 24-channel, or 30-channel operation. The DRA controller controls the transmission and reception of messages between the DRAM unit and the DMS CM. The DRA controller selects and retrieves recorded phrases from the PROM, EEPROM, and RAM cards. The DRA controller transmits recorded phrases on selected speech link channels. The DRA controller controls the recording of new announcements and assigns the announcements to an appropriate section of memory. Each PROM, EEPROM, and RAM memory card contains storage space for phrases. These phrases can be a maximum of 31 s in length. The CM instructs the DRA controller card to transmit complete announcements and to join incomplete announcements to complete messages. Procedures in the DMS-100 Menu Commands Reference Manual, 297-1001-801 allow manual control from the MAP level during maintenance procedures. These procedures also allow manual control from the MAP level during new message recording. The RAM card (NT1X77AA) stores complete and incomplete announcements that are recorded on site. These announcements are made over a PCM-channel network connection. These announcements are lost if you remove the card from the slot. The EEPROM card (NT1X79AA) stores messages recorded on site, and the messages are not lost when you remove the card. To remove the messages you must erase the memory electrically.

NT2X58AG components (Sheet 5 of 6)

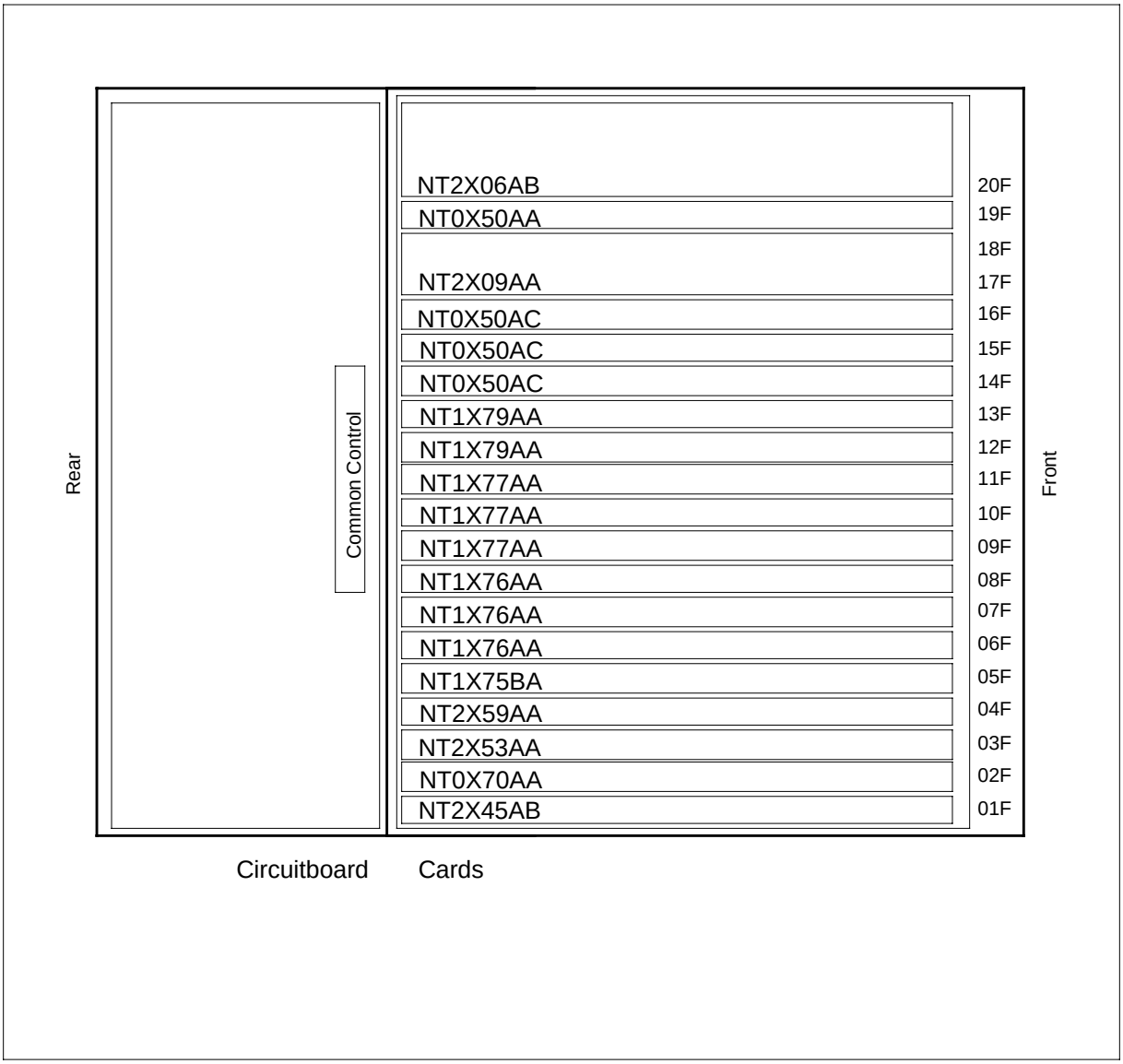
PEC	Slot	Description
NT1X79AA	12F, 13F	*Electronically erasable read-only memory cards* The DRAM unit contains a DRA controller card (NT1X75BA), PROM (NT1X76) cards, EEPROM (NT1X79AA) cards, and RAM (NT1X77AA) cards. The unit must contain a minimum of one PROM or RAM card. The unit can use a maximum of any eight PROM, RAM, and EEPROM cards. Manual switches configure the DRA controller for 8-channel, 16-channel, 24-channel, or 30-channel operation. The DRA controller controls the transmission and reception of messages between the DRAM unit and the DMS CM. The DRA controller selects and retrieves recorded phrases from the PROM, EEPROM, and RAM cards. The DRA controller transmits recorded phrases on selected speech link channels. The DRA controller controls the recording of new announcements and assigns the announcements to an appropriate section of memory. Each PROM, EEPROM, and RAM memory card contains storage space for phrases. These phrases can be a maximum of 31 s in length. The CM instructs the DRA controller card to transmit complete announcements and to join incomplete announcements to complete messages. Procedures in the DMS-100 Menu Commands Reference Manual, 297-1001-801 allow manual control from the MAP level during maintenance procedures. These procedures also allow manual control from the MAP level during new message recording. The RAM card (NT1X77AA) stores complete and incomplete announcements, that are recorded on site. These announcements are made over a PCM-channel network connection. These announcements are lost if you remove the card from the slot. The EEPROM card (NT1X79AA) stores messages recorded on site, and the messages are not lost when you remove the card. To remove the messages erase the memory electrically.
NT2X06AB	20F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards in the module require. The NT2X06AB converter produces a 5V, 40-A output. The converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The converter includes face plate test jacks and a face plate light-emitting diode (LED) state indicator.

NT2X58AG (end)

NT2X58AG components (Sheet 6 of 6)

PEC	Slot	Description
NT2X09AA	17F-18F	*Power converter* The NT2X06AB and NT2X09AA power converters convert the -48V dc to the lower voltages that the circuit cards in the module require. The NT2X06AB converter produces a 5V, 40A output. The NT2X09AA converter produces -5V, -15V, +5V, +12V, and +24V dc outputs. Both converters include a low-voltage monitor circuit, overvoltage and overcurrent protection, face plate test jacks, and a face plate LED state indicator.
NT2X45AB	1F	*Trunk module interface card* The TM interface card serves as the network interface for both planes of the network. The TM interface card provides two-way interfaces for the two transmission paths from both network planes. The TM contains message registers, bit and channel timing circuits, circuits that check parity, and circuits that format data again.
NT2X53AA	3F	*Trunk module control card* The TM control card contains the circuit controllers that handle different messages. The TM control card exchanges information with the processor circuit card. This exchange occurs over data and address buses and produces enabling signals for the circuits in the DRAM unit.
NT2X59AA	4F	*Group CODEC and tone circuit card* The group CODEC and tone circuit card (NT2X59AA) creates pulse-code modulation (PCM) words from pulse amplitude modulated (PAM) analog samples. The group CODEC and tone circuit card decodes PCM word streams into analog samples. These functions are the same functions the group CODEC and tone circuit card performs in the MTM. This circuit card includes the ROMs that contain the digital tones for dialing and signaling.

NT2X58AG components



NT2X58AL

Description

The maintenance trunk module (MTM) shelf provides service interfaces for service, test, and maintenance circuits and scanner and signal distributor cards. The NT2X58AL MTM is available for use in Canada and mounts in the NT0X46AB frame. The NT2X58AL MTM links channels from the network modules to channels on test or service circuit cards in the MTM. The MTM functions as a switching center for control messages. This switching center is for control messages. The control module in the DMS-core and each test or service circuit card exchange these messages. Internally, the MTM provides low-voltage supplies and the connections. These low-voltage supplies and connections allow the exchange of data between the test circuit cards and the low-voltage supplies.

The MTM contains an NT4X65AB trunk module control card that makes and maintains connections. Two buses, maintenance (MAINT) 1 and 2, exchange data between the test circuit cards. The MTM does not use XDAT or RDAT buses. The MTM has two power converter cards and a maximum of 14 service or test circuit cards.

The MTM has digital and analog looparound provisions. In digital looparound, the RDAT bus loops back to the XDAT bus and the RDAT/XDAT connections. The RDAT loops to the trunk logic circuits (TLC) in the test and service cards. The RPAM bus loops to the XPAM bus for analog looparound. The common control section controls the two looparound functions. The common control section sends messages addressed to the different service and test cards.

Looparound circuits are available in each test or service card for channel-specific looparound tests. The common control section also controls these circuits. The common control section addresses specified test or service cards through the TLC.

Parts

The MTM contains test and service circuit cards and the following components:

- NT0X50AA-filler faceplate
- NT2X06AB-power converter card
- NT2X09AA-power converter card
- NT2X59AA-group CODEC DMS-100/200 card
- NT4X65AB-trunk module control card

Design

The following table describes the components. The figure that follows the table illustrates the design of the NT2X58AL.

NT2X58AL components (Sheet 1 of 2)

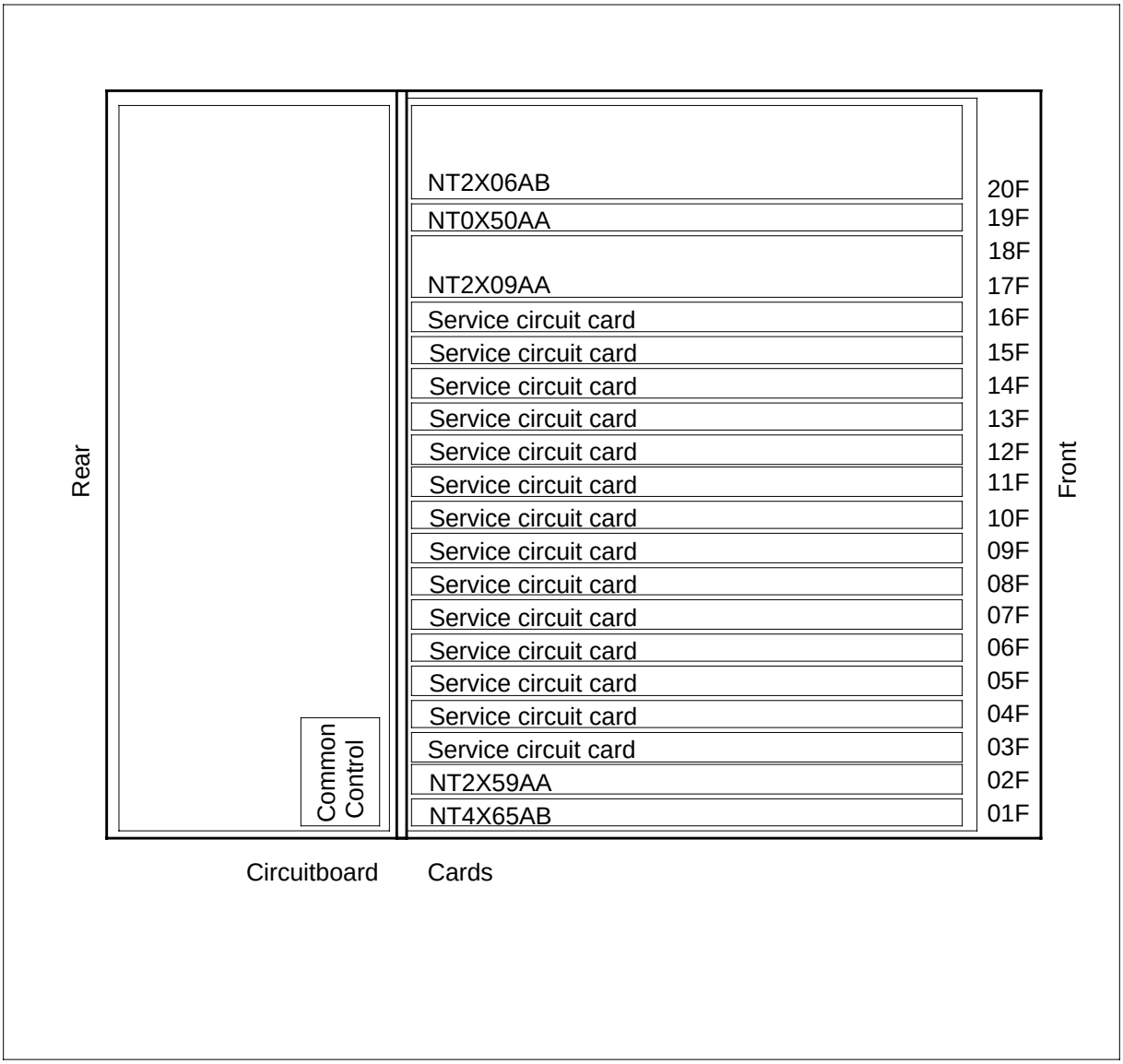
PEC	Slot	Description
-	3-16F	*Test and service cards* Test and service cards vary based on the purpose of the card. Cards provide an interface with analog trunks, signaling, test, service, or alarm circuits. The test and service circuit cards use the RDAT, XDAT, and MAINT buses. Maintenance programs control the test and service circuit cards. Maintenance programs reside in the control module of the central switch. The software provides the correct control codes and enabling signals. These codes and signals operate with the test and service cards in the MTM.
NT0X50AA	19F	*Filler faceplate* The filler faceplate or panel fills empty card slots in the module.
NT2X06AB	20F	*Power converter card* The power converter card converts the dc voltage of -48V to the lower voltages the circuit cards in the module need. The NT2X06AB converter produces a 5-V, 40-A output. The converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The converter includes faceplate test jacks and a faceplate light-emitting diode (LED) status indicator.
NT2X09AA	17F	*Power converter card* The power converter card converts the dc voltage of -48V to the lower voltages that the circuit cards in the module need. The NT2X09AA converter produces dc voltages of -5, -15, +5, +12, and +24V. The converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The converter includes faceplate test jacks and a faceplate LED state indicator.

NT2X58AL (end)

NT2X58AL components (Sheet 2 of 2)

PEC	Slot	Description
NT2X59AA	2F	*Group CODEC DMS-100/200 card* The group CODEC DMS-100/200 card creates pulse code modulation words from pulse amplitude modulated analog samples. The group CODEC DMS-100/200 card decodes pulse code modulation word streams into analog samples. The group CODEC DMS-100/200 card includes the ROMs that contain the digital tones for dialing and signaling.
NT4X65AB	1F	*Trunk module control card* The trunk module control card provides high level control in the maintenance trunk module. The trunk module control card controls signal and supervision functions. The trunk module control card controls network messaging to the host DMS and processing of PCM data. This control card interfaces with analog and digital test trunks, service circuits, and alarm circuits.

NT2X58AL components



NT2X58AM

Description

The NT2X58AM maintenance trunk module (MTM) for the digital recorded announcement machine (DRAM) contains circuits. These circuits store recorded phrases and, with the DMS control module (CM), route the recorded phrases to speech channels. The module is like the NT2X58AC MTM except that a group of circuits replaces the service circuit cards. This group of circuits is the DRAM unit. The intercard bus links the first 10 module slots. The MTM uses even-odd intercard connections.

The DRAM control section makes and maintains connections and controls the operation of the module. The DRAM control section is identical to the control section in the NT2X58AC MTM. The DRAM control section contains an NT2X59AA group coder-decoder (CODEC) and tone circuit cards. The DRAM control section includes an NT4X65AB single combination control circuit card. The NT4X65AB single unit control circuit card contains an NT2X45AB network interface card, an NT2X70AA processor card and a control section.

The DRAM unit consists of a speech processor, a microprocessor controller, and speech memory. Circuit cards house the speech processor, microprocessor controller, and speech memory. The microprocessor controller and speech processor are located on the NT1X75BA enhanced digital recorded announcement (DRA) controller card. Cards that can provide speech memory are as follows:

- NT1X76AA PROM
- NT1X77AA RAM
- NT1X79AA EEPROM.

The unit must contain a minimum of one PROM or RAM card. The unit can use a maximum of eight PROM, EEPROM, and RAM cards.

Parts

The DRAM contains RAM cards and the following components:

- NT0X50AA-Filler face plate or panel.
- NT0X50AC-Filler face plate or panel.
- NT1X75BA-Enhanced DRA controller card.
- NT1X76AA-PROM cards.
- NT1X77AA-RAM card.
- NT1X79AA-EEPROM cards.

- NT2X06AB-Power converter.
- NT2X09AA-Power converter.
- NT2X59AA-Group CODEC and tone circuit card.
- NT4X65AB-Combination control circuit card.

Design

The following table and figure describe the design of the NT2X58AM.

NT2X58AM components (Sheet 1 of 3)

PEC	Slot	Description
NT0X50AA	19F	*Filler face plate* The filler face plate or panel fills empty card slots in the shelves. A maximum of five spare card slots can be present in each module. Slots 15, 16, and 17 have access to the signaling processor (SP) address bus and the parallel speech bus. Slots 13 and 19 do not have access to the address bus and parallel speech bus.
NT0X50AC	11F-16F	*Filler face plate* The filler face plate or panel fills empty card slots in the shelves. A maximum of five spare card slots can be present in each module. Slots 15, 16, and 17 have access to the SP address bus and the parallel speech bus. Slots 13 and 19 do not have access to the address bus and the parallel speech bus.
NT1X76AA	3F-5F	*Programmable read-only memory cards* The PROM card holds standard recorded announcements. These announcements are programmed in the card on manufacture. These announcements are programmed in digital form. The two-letter suffix at the end of the product engineering code (PEC) indicates the type and language of the announcement. You cannot change, extend, or erase these announcements.
NT1X75BA	6F	*Enhanced digital recorded announcement controller card* The NT1X75BA enhanced digital recorded announcement (DRA) processor card provides a maximum of 64 recorded announcements or phrases for DMS-100 equipment.

NT2X58AM (continued)

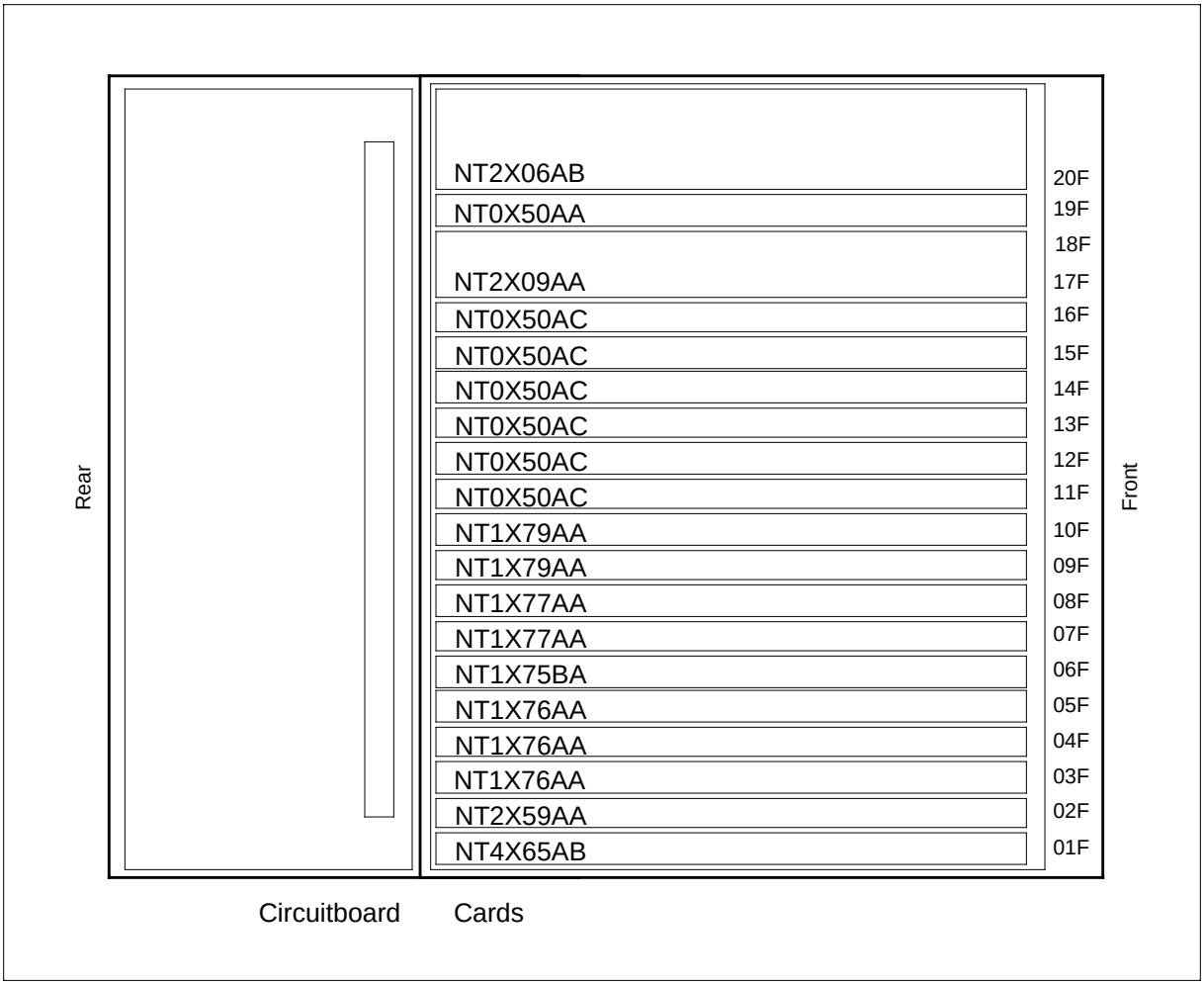
NT2X58AM components (Sheet 2 of 3)

PEC	Slot	Description
NT1X77AA	7F, 8F	*Digital recorded announcement recordable memory* The RAM card stores announcements on site. The RAM card stores announcements in part or stores complete announcements. These announcements are made over a PCM-channel network connection. The announcements are lost if you remove the card from the slot.
NT1X79AA	9F, 10F	*Electronically erasable programmable read-only memory card* The EEPROM card stores messages recorded on site, but the messages are not lost when you remove the card. To remove the messages you must erase the memory electrically.
NT2X06AB	20F	*Power converter* The power converter converts the -48V dc to the lower voltages that the circuit cards in the module require. The NT2X06AB converter produces a 5-V, 40-A output. The converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The converter includes face plate test jacks and a face plate light-emitting diode (LED) state indicator.
NT2X09AA	17F	*Power converter* The power converter converts the -48V dc to the lower voltages the circuit cards in the module need. The NT2X09AA converter produces -5V, -15V, +5V, +12V, and +24V dc. The converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The converter includes face plate test jacks, and a face plate LED state indicator.
NT2X59AA	2F	*Group CODEC and tone circuit card* The group CODEC and tone circuit card (NT2X59AA) creates pulse-code-modulation (PCM) words from pulse-amplitude-modulated (PAM) analog samples. The group CODEC and tone circuit card (NT2X59AA) decodes PCM word streams into analog samples. These functions are the same functions the group CODEC and tone circuit card performs in the MTM. This circuit card includes the ROMs that contain the digital tones for dialing and signaling.

NT2X58AM components (Sheet 3 of 3)

PEC	Slot	Description
NT4X65AB	1F	*Combination control circuit card* The combination control circuit card contains the interface, processing, and control circuits for the MTM. The interface circuits provide two bi-directional interfaces for the two transmission paths from both network planes. The interface circuits include message registers, bit and channel timing circuits, circuits that check parity, and circuits that format data again. The processing circuit performs or controls the operations that the components of the MTM accomplish. The processing circuit contains a firmware-driven microprocessor. The processing circuit contains two RAM, one RAM to store program information and one RAM to store operational information. Operational information includes connection information for PCM channel-to-trunk assignments. The processor includes circuits that generate the clock signal, check parity, and perform synchronization. The control circuit contains the controllers that handle different messages. The control circuit communicates information with the processor circuit. Communication occurs on data and address buses and produces enabling signals for the circuits on the service and test cards.

NT2X58AM components



NT2X58AT

Description

The NT2X58AT maintenance trunk module (MTM) shelf is part of an NT0X46AB frame. This MTM provides the dial, busy, and ringback tones that international switches require. This MTM links channels from the network modules (NM) to channels on test or service circuit cards in the MTM. The module functions as a switching center for control messages. The control module in the DMS-core and each test or service circuit card exchange these messages. Internally, the MTM provides low-voltage supplies and connections. These low-voltage supplies and connections are needed to exchange data between the test circuit cards and the low-voltage supplies.

The MTM contains a control section that includes the following:

- NT2X45BA trunk module (TM) interface
- NT0X70BA international TM processor
- NT2X53AA TM control cards.

The control cards make and maintain connections. Two buses, maintenance (MAINT) 1 and 2, exchange data between the test circuit cards. The MTM has two power converter cards and a maximum of 12 service or test circuit cards.

The MTM has digital and analog looparound provisions. In digital looparound, the RDAT bus loops back to the XDAT bus and the RDAT/XDAT connections. The RDAT bus loops to the trunk logic circuits (TLC) in the test and service cards. The RPAM bus loops to the XPAM bus for analog looparound. The common control section controls the two looparounds. The common control sections send messages addressed to the different service and test cards.

Looparound circuits are available in each test or service card for channel-specific looparound tests. The common control section controls these circuits. The common control section addresses specified test or service cards through the TLC.

Each NT2X58AT shelf requires one NT2X58AS common circuit pack. This pack includes one of each of the following circuit cards:

- NT2X45BA
- NT0X70BA
- NT2X53AA
- NT2X59BA
- NT2X09AA
- NT2X70AA.

NT2X58AT (continued)

Parts

The MTM contains test and service circuit cards and the following components:

- NT0X50AA-filler faceplate.
- NT0X70BA-international TM processor card.
- NT2X09AA-power converter.
- NT2X45BA-TM interface card.
- NT2X53AA-TM control card.
- NT2X59BA-A-law CODEC and tones circuit card.
- NT2X70AA-power converter.

Design

The following table describes the components of the NT2X58AT.

NT2X58AT components (Sheet 1 of 2)

PEC	Slot	Description
-	5-16F	*Test and service circuit cards* The test and service circuit cards use the RDAT, XDAT, and MAINT buses. Maintenance programs control the test and service circuit cards. Maintenance programs are in the control module of the central switch. The software provides control codes and enabling signals. These codes and signals operate with the test and service cards in the MTM.
NT0X50AA	19F	*Filler faceplate* The filler faceplate or panel fills empty card slots in the module.
NT0X70BA	2F	*International trunk module processor card* The TM processor performs or controls all the operations that the components of the MTM accomplish. The card contains a microprocessor. Firmware drives the microprocessor. The card contains two RAMs. One RAM stores program information, and one RAM stores operational information. Operational information includes connection information for PCM channel-to-trunk assignments. This card includes circuits that generate the clock signal, check parity, and perform synchronization.

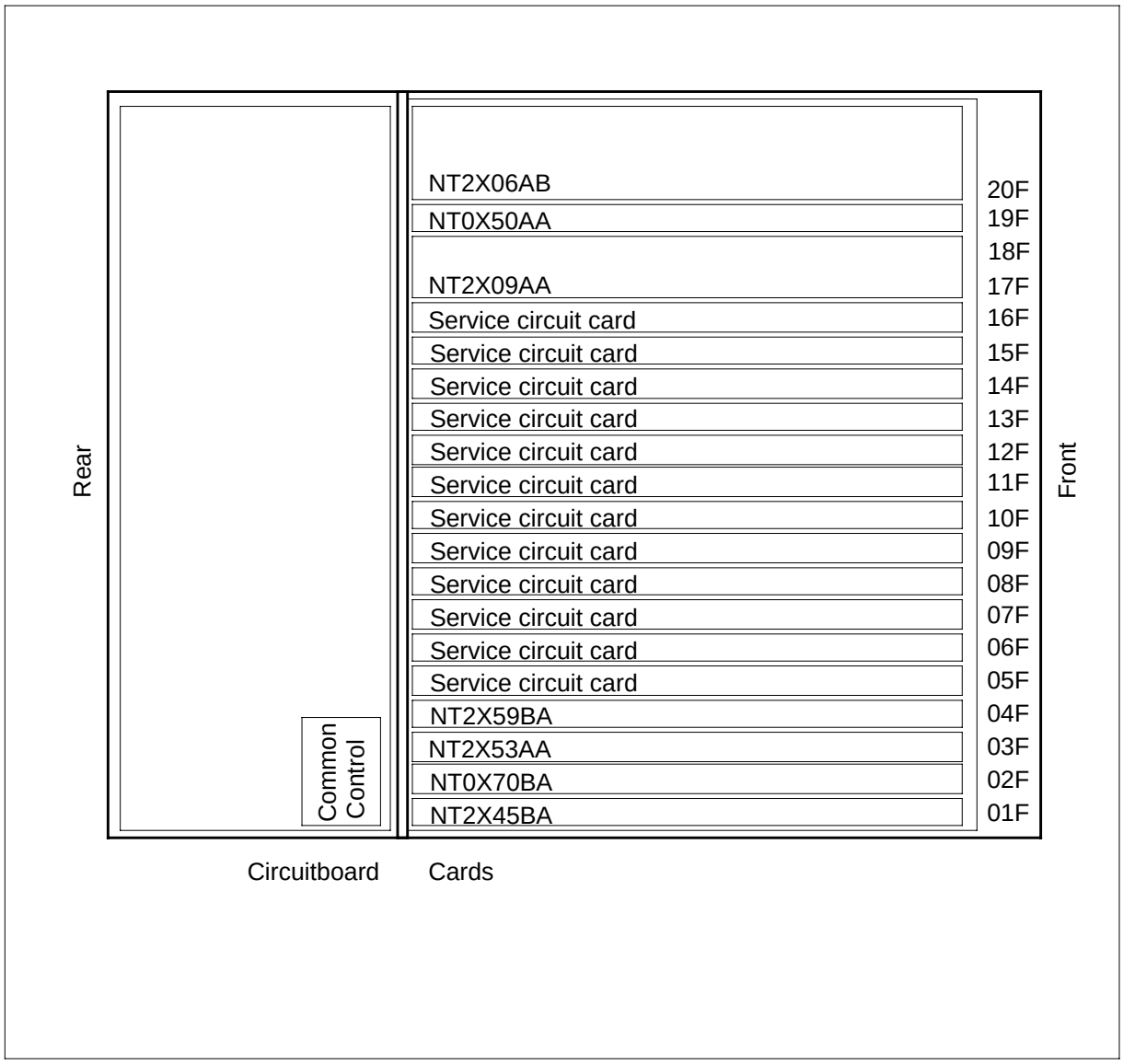
NT2X58AT components (Sheet 2 of 2)

PEC	Slot	Description
NT2X09AA	17F	*Power converter* The power converter converts the dc voltage of -48V to the lower voltages that the circuit cards in the module require. The NT2X09AA converter produces dc voltages of -5, -15, +5, +12, and +24V. The converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The converter includes faceplate test jacks and a faceplate LED state indicator.
NT2X45BA	1F	*Trunk module interface card* The TM interface card serves as the network interface for both planes of the network. The TM interface card provides two-way interfaces for the two transmission paths from both network planes. The TM interface card contains message registers and bit and channel timing circuits. The TM interface card contains circuits that check parity and circuits that format data again.
NT2X53AA	3F	*Trunk module control card* The TM control card contains circuit controllers that handle different messages. The TM control card exchanges information with the processor card. This exchange occurs on data and address buses. The exchange of information produces enabling signals for the circuits on the test and service circuit cards.
NT2X59BA	4F	*A-law CODEC and tones card* The group CODEC and tones card creates pulse code modulation (PCM) words from pulse amplitude modulated analog samples. The group CODEC and tones card decodes PCM word streams to analog samples. The group CODEC and tones card includes the ROMs that contain the digital tones for dialing and signaling.
NT2X70AA	20F	*Power converter* The power converter converts the dc voltage of -48V to the lower voltages that the circuit cards in the module requires. The NT2X70AA converter produces a 5-V, 40-A output. The converter includes a low-voltage monitor circuit and overvoltage and overcurrent protection. The converter includes faceplate test jacks, and a faceplate light-emitting diode (LED) state indicator.

NT2X58AT (end)

The design of the NT2X58AT appears in the following figure.

NT2X58AT components



DMS-100

Hardware Description Manual

Volume 1 of 5

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