

DIMENSION[®] 2000 AND CUSTOM PBX
COMMON CONTROL I/O ALARM
(PROC 501)

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1. GENERAL

- 1.1 This section provides information for interrogating and clearing COMMON CONTROL INPUT and OUTPUT alarms via PROC 501.
- 1.2 Procedure 501 displays (TEST 1) the on - line maintenance HIGH SPEED DATA CHANNEL controller failures (LC130), DUAL SPEED DATA CHANNEL failures (LC34), and I/O and MEMORY DECODE CIRCUIT failures (LC133). TESTS 2 & 3 provide a means of testing and displaying faults related to the I/O portion of LC130, LC132 (TEST 2, only), LC133, and LC34 circuit packs via the internal loop test mode.

2. RECORDS

- 2.1 Form SD-97-1313 is required for recording the results of this test.

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3. MAAP DISPLAY FIELD DESCRIPTIONS

3.1 The following describes the individual MAAP display fields related to PROC 501.

FIELD DESCRIPTION

1 TEST NO. - Displays test number in effect per the following encodes:

ENCODE DESCRIPTION

- 1 Displays on - line maintenance failure history. If failures were detected, the first failure detected would be displayed. This test also allows clearing of the COMMON CONTROL I/O fault records.
- 2 Tests all circuits sequentially, starting with the first high speed data channel controller and ending with the last DUAL SPEED DATA CHANNEL circuit. This test clears the COMMON CONTROL. I/O alarms automatically, if no failures are detected.
- 3 Tests a particular circuit continuously as specified in FIELDS 2 thru 5. When TEST 3 is activated, the default (last circuit failure detected) circuit will be displayed, if a failure(s) was previously recorded.

2 CKT TYPE - for TESTS 1 & 2, displays the type of circuit where a failure was detected. For TEST 3, displays circuit type to be tested. The encodes are as follows:

ENCODE DESCRIPTION

- 0 LC130 - High speed data channel controller
- 1 LC34 - Dual speed data channel

3 CARR TYPE - for TESTS 1 & 2, displays type of carrier where a fault was detected for TEST 3, displays carrier type to be tested. The encodes are as follows:

ENCODE DESCRIPTION

- 0 BASIC CONTROL CARRIER
- 1 GROWTH CONTROL CARRIER

4 SLOT - for TESTS 1 & 2, displays slot number where a failure was detected. For TEST 3, displays slot number to be tested. The encodes are as follows:

ENCODE DESCRIPTION

- 39 LC130 - BASIC CONTROL CARRIER
- 34 LC130 (1st) - GROWTH CONTROL CARRIER
- 39 LC130 (2nd) - GROWTH CONTROL CARRIER

3.1 (Continued)

ENCODE	DESCRIPTION
30 - 38	LC34's - BASIC CONTROL CARRIER*
20 - 33	LC34's - GROWTH CONTROL CARRIER*

* Note: RMA channels are excluded.

- 5 CKT - for TESTS 1 & 2, displays defective circuit location. For TEST 3, displays circuit to be tested. The encodes are as follows:

ENCODE	DESCRIPTION
-	LC130 - HIGH SPEED DATA CHANNEL CONTROLLER
0	LC34 (1st) - DUAL SPEED DATA CHANNEL
1	LC34 (2nd) - DUAL SPEED DATA CHANNEL

- 6 DATA CHANNEL FAIL CODE - for TESTS 1 & 2, displays type of fault detected, if no faults were detected a dash will be displayed. For TEST 3, displays test results. The encode will flash while the test is running and light steadily when the test is stopped. The encodes are as follows:

ENCODE	DESCRIPTION
0	PASS (TEST 3, only)
1	ADDRESSING
2	HIGH SPEED (low address) or DUAL SPEED LOOP AROUND
3	HIGH SPEED (high address) LOOP AROUND
4	HIGH SPEED (low and high address) LOOP AROUND
5	ADDRESSING AND LOOP AROUND

- 7 IO BUFR FAIL CODE - TEST 2, displays I/O BUFFER FAIL CODE. Displays I/O BUFFER failure code only when TEST 2 is executed. The encodes are as follows:

ENCODE	DESCRIPTION
0	PASS
1	LC132 - BASIC CONTROL CARRIER
2	LC132 - GROWTH CONTROL CARRIER
3	LC132 - BOTH CARRIERS

- 8 IO AND MEM DEC FAIL CODE - for TEST 1, displays I/O and MEMORY DECODER circuit fail detected by on - line maintenance. For TESTS 2 & 3, displays fail code detected by the test. The encodes are as follows:

ENCODE	DESCRIPTION
0	PASS
1	POWER OR ALARM CLEAR BIT FAILURE
2	LOOP AROUND FAILURE
3	COMBINATION OF 1 & 2

3.1 (Continued)

- 9 NUMBER OF DUAL SPEED DATA CHANNELS - Displays number of dual speed data channels in each common control carrier (maximum of 46). This number will be displayed when the program is first read from the tape, when the reset key is operated and throughout the rest of the procedure.
- 10 NUMBER OF DUAL SPEED DATA CHANNEL FAILURES - during TESTS 1 & 2, displays number of dual speed data channel (LC34's) failures. A "0" indicates no failures detected.
- 11 FAILED DUAL SPEED DATA CHANNEL INDEX - for TESTS 1 & 2, displays the failure index (maximum of 6 for ~~TEST 1~~). This number indicates the order that the failures were detected.
- 12 NUMBER OF HIGH SPEED DATA CHANNEL CONTROLLERS - throughout the display of procedure 501 and when the tape is read and when the RESET key is operated, displays number of high speed data channel controllers (# of LC130's), (maximum of 3).
- 13 NUMBER OF HIGH SPEED DATA CHANNEL CONTROLLER FAILURES - for TESTS 1 & 2, displays number of high speed data channel controller failures detected. (LC130's). A "0" will be displayed when no failures are detected.
- 14 FAILED HIGH SPEED DATA CHANNEL CONTROLLER INDEX - for TESTS 1 & 2, displays failure index (maximum of 3). This number indicates the order that the failures were detected.

4. MAAP KEY OPERATIONS

- 4.1 The following describes the individual and combinational MAAP control key operations that are allowed.

PROC NO. 5,0,1, ENTER - Loads PROC 501 program from tape to memory. When the ENTER key is operated the WAIT lamp will light. When the WAIT lamp turns off the craftsperson should see a 1 in FIELD 1 indicating that the procedure has been loaded and is in the TEST 1 state.

CLEAR DATA, EXECUTE - (Valid only in TEST 1), clears failure history. The failure history should be recorded before the data is cleared.

EXECUTE - Starts the test displayed in FIELD 1. In TEST 1 the failure history is displayed. In TEST 2 a test of all of the high speed data channel controllers and then a test of all of the DUAL SPEED DATA CIRCUITS is initiated. In TEST 3 continuous testing of the circuit displayed in FIELDS 2 thru 5 is initiated. Note: See paragraph 6 of this section for a more detailed test description.

NEXT CIRCUIT - in TESTS 1 & 2, advances to the next circuit that failed. When all failed circuits have been displayed, the MAAP display is dashed and then re-operating the NEXT CIRCUIT key again will display the first circuit failure found. In TEST 3 (if a valid circuit is defined in FIELDS 2 thru 5 and if the test is idle) advances to the next circuit within the specified carrier.

NEXT TEST - Advances to the next test number (maximum of three tests).

NEXT UNIT - (Valid only in TEST 3), advances to the first valid HIGH SPEED DATA CHANNEL CONTROLLER or DUAL SPEED DATA CIRCUIT (in that order) in the other control carrier type (if equipped) and if the test is idle.

RESET - Resets the program to the beginning.

STOP - (Valid only in TEST 3), stops the testing performed in TEST 3. The STOP key must be operated before the EXECUTE, NEXT CIRCUIT, and NEXT UNIT keys are operated if TEST 3 is running.

5. REPAIR PROCEDURES

- 5.1 The following describes the repair procedures that should be followed in the event that the craftsperson is directed to procedure 501 to clear a COMMON CONTROL I/O alarm.
- 5.11 Read in the procedure from the tape and execute TEST 1.
- 5.12 Record the failure history generated by on - line maintenance, (the same circuit may be shown as the last 6 failures).
- 5.13 Execute TEST 2 and record the results. If a failure results, use the following steps:
- A) If I/O and MEMORY DECODE FAIL CODE (shown in FIELD 8) is a 2 or 3, replace I/O MEMORY and DECODE circuit pack (LC133). (Use HALT/GO sequence).
 - B) If I/O BUFFER FAIL CODE (shown in FIELD 7) = 0, replace circuits displayed in FIELDS 2 thru 5. (Use HALT/GO sequence).
 - C) If I/O BUFFER FAIL CODE (shown in FIELD 7) = 1, replace I/O BUFFER circuit pack (LC132) in BASIC CONTROL CARRIER. (Use HALT/GO sequence).
 - D) If I/O BUFFER FAIL CODE (shown in FIELD 7) = 2, replace I/O BUFFER circuit pack (LC132) in GROWTH CONTROL CARRIER. (Use HALT/GO sequence).
 - E) If I/O BUFFER FAIL CODE (shown in FIELD 7) = 3, replace I/O BUFFER circuit pack (LC132) in both carriers. (use HALT/GO sequence).
 - F) If MEMORY DECODE FAILURE ENCODE (shown in FIELD 8) = 1, this may not be service affecting. Replace LC133 when convenient. (Use HALT/GO sequence).
- 5.14 If there were no failures recorded during TEST 2, use TEST 3 to continuously test each circuit displayed in TEST 1 to verify if intermittent faults exist. If a fault is detected use repair procedure prescribed in paragraph 5.13. The results of this test should also be recorded.
- 5.15 After the trouble(s) has been cleared go to TEST 1 and clear the on-line maintenance records (use CLEAR DATA, EXECUTE keys).

6. TROUBLESHOOTING AIDS

6.1 GENERAL TEST INFORMATION

6.11 TEST 1 - TEST 1 is the default test when the procedure is first read in from the tape or when the MAAP - RESET key is operated. When the MAAP - EXECUTE key is operated, data accumulated by on - line maintenance procedures, is displayed on the MAAP starting with the first failure (maximum of 6 failures can be displayed). If there are no failures FIELDS 10 and 13 will be zero. If there are one or more DUAL SPEED DATA CHANNEL (LC34) failures and no HIGH SPEED DATA CHANNEL CONTROLLER failures (LC130), the number of failures will be displayed in FIELD 10 and a number 1 will be displayed in FIELD 11 (indicating first DUAL DATA CHANNEL failure found). FIELD 13 under these conditions will be zero.

If there are one or more HIGH SPEED DATA CHANNEL CONTROLLER failures and no DUAL DATA CHANNEL failures the number of failures will be displayed in FIELD 13 and a number 1 will be displayed in FIELD 14. FIELD 10 under these conditions will contain a zero.

If both types of circuit failures occur, then the first failed HIGH SPEED CONTROLLER will be displayed. The number of failed DUAL SPEED DATA CHANNEL circuits will be displayed in FIELD 10, while the number of failed HIGH SPEED DATA CHANNEL CONTROLLERS will be displayed in FIELD 13. FIELD 14 will display a NUMBER 1 while FIELD 11 will be dashed.

The number of DUAL SPEED DATA CHANNEL circuits and HIGH SPEED DATA CHANNEL CONTROLLERS remains displayed in all cases in FIELDS 9 and 12, respectively. In cases of failure, the equipment location of the first failed circuit is displayed in FIELDS 2 - 5 and the failure code for the circuit is displayed in FIELD 6. If the I/O and MEMORY DECODE circuit failed the on-line maintenance test, the appropriate failure code will be displayed in FIELD 8.

Operation of the MAAP - NEXT CIRCUIT key displays the next failed circuit. All HIGH SPEED DATA CONTROLLERS are displayed before the DUAL SPEED DATA CIRCUITS. The individual failure index in FIELD 11 or FIELD 14 (depending on which type circuit failure is being displayed) is incremented by 1. The failure index associated with the type circuit not currently displayed is dashed. If a NEXT CIRCUIT key operation occurs when no failures have occurred or when all failures have been displayed, the MAAP will be dashed to indicate that there are no more failures to be displayed. Another NEXT CIRCUIT key operation will then cause the test to re-execute.

Operation of the CLEAR DATA, EXECUTE keys, clears the fault records and alarms.

- 6.12 TEST 2 - The purpose of TEST 2 is to test all HIGH SPEED DATA CHANNEL CONTROLLERS (LC130) and all DUAL SPEED DATA CIRCUITS (LC34). To display the failed circuits, and to control ALARM PANEL COMMON CONTROL I/O alarms.

The test is initiated when the MAAP - EXECUTE key is operated, which turns on the MAAP - WAIT lamp and begins testing the I/O and MEMORY DECODE CIRCUIT (LC133). The appropriate failure code is displayed in FIELD 8, the WAIT lamp is turned off, and the test is terminated if the I/O and MEMORY DECODE CIRCUIT fails the test. If the LC133 test passed, the HIGH SPEED DATA CHANNEL CONTROLLERS are tested and then the DUAL DATA SPEED CIRCUITS are tested.

If a failure is detected, the COMMON CONTROL I/O and MAJOR alarm lamps are turned on. All failed circuit data is stored and at the conclusion of the test, the first failed circuit will be displayed in FIELDS 2 - 5 (any failed HIGH SPEED DATA CHANNEL CONTROLLER will be shown first) and the associated failure code will be displayed in FIELD 6. If it has been determined during the test that an I/O BUFFER failure has occurred the appropriate failure code will be displayed in FIELD 7.

The number of failures for the HIGH SPEED CONTROLLERS and DUAL SPEED DATA CIRCUITS will be displayed in FIELDS 13 and 10, respectively. FIELD 14 will contain a 1 and FIELD 11 will be dashed if a HIGH SPEED CONTROLLER failed. The contents of the two fields will be reversed if only DUAL DATA SPEED circuits failed. FIELDS 11 and 14 will contain zeroes if no failures occur, and also if no failures occur any existing COMMON CONTROL I/O ALARMS will be turned off. Operation of the NEXT CIRCUIT key at the conclusion of the test will cause the next failed circuit to be displayed (if there are any failures found initially). At the conclusion of the test the WAIT lamp is turned off.

- 6.13 TEST 3 - The purpose of TEST 3 is to test a circuit continuously and to light the COMMON CONTROL I/O and MAJOR alarm lamps if a failure occurs. If a default circuit (last failure displayed) is not displayed, the craftsperson must enter a circuit. If the displayed circuit is not the circuit desired to test, it can be changed by the CHANGE FIELD key sequence, or by operating the NEXT CIRCUIT key (advances to the next circuit within the specified control carrier type), or by operating the NEXT UNIT key (advances to the first circuit in the other control carrier type if equipped).

The test is started by operating the EXECUTE key. The WAIT lamp is not turned on since the test is continuous. The failure code is flashed (60 IPM) in FIELD 6 to indicate that the test is running. If a failure occurs, the test continues to run and FIELD 6 flashes the appropriate failure code. The test can be stopped by operating the STOP key.

6.2 GENERAL TROUBLESHOOTING INFORMATION

- 6.21 DATA CHANNEL FAILURES - (FIELD 6), PROC 501 checks data channels (LC130's, and LC34's) by (1) first setting the LOOP TEST flip flop in LC133, to cause data sent, to be internally looped back at the circuit pack under test, and (2) addressing the DATA CHANNEL circuit and sending data patterns 0000, FFFF, and AAAA (HEX) and verifying that the response to each of the data patterns is correct.

For high speed data channel controller, circuits HEX I/O addresses used are (1) 6008 for the BASIC CONTROL CARRIER LC130, (2) 6048 for the first TRANSMITTER/RECEIVER CKT and 6058 for the second TRANSMITTER/RECEIVER CKT located at LC130 (slot 34) in the GROWTH CONTROL CARRIER, (3) 6068 for the first transmitter/receiver ckt and 6078 for the second transmitter/receiver ckt located at LC130 (slot 37) in the GROWTH CONTROL CARRIER.

For the DUAL SPEED DATA CHANNEL circuits, hex I/O addresses used are (1) 610C to 611D for the BASIC CONTROL CARRIER LC34's, (2) 6140 to 615B for the GROWTH CONTROL CARRIER LC34's

Attachment 1 shows the formats for addressing both the high speed data channel controller circuits and the dual speed data channel circuits.

The following describes possible causes to failure codes displayed in FIELD 6 as follows:

ENCODE	DESCRIPTION
1	Failure to receive an I/O DONE signal
2	Failure to receive correct data response either at first transmitter/receiver of the HIGH SPEED DATA CHANNEL CONTROLLER or the transmitter/receiver of the DUAL SPEED DATA CHANNEL circuit displayed in FIELDS 2 thru 5.
3	Failure to receive correct data response from second transmitter/receiver of the HIGH SPEED DATA CHANNEL displayed in FIELDS 2 thru 5.
4	Failure to receive correct data response from both transmitter/receivers in the HIGH SPEED DATA CHANNEL CONTROLLER displayed in FIELD 2 thru 5.

ENCODE	DESCRIPTION
5	Failure to receiver I/O DONE signal or correct data from circuit displayed in FIELDS 2 thru 5.

Note: In all cases the circuit pack associated with the carrier number and slot displayed in FIELDS 3 and 4 should be replaced before any test points are checked.

6.22 I/O BUFFER FAILURES - (FIELD 7), I/O BUFFER failures are determined on the basis that if more than one channel circuit pack failure exists then the I/O BUFFER associated with the failed channel circuits is flagged defective.

Note: Replace the LC132 associated with the channel circuit displayed in FIELDS 2 thru 5, as the LC132 circuit location will not be displayed. In both carriers, the LC132 will be located in slot 19. The above should be performed before any test points are checked.

6.23 I/O AND MEMORY DECODE FAILURES - (FIELD 8), the I/O and MEMORY DECODE circuit (LC133) is the first circuit tested when TEST 2 or 3 is executed. The hex address used is 6001 and the hex data messages sent are 0000 thru 0007. For each of the data messages sent a check is made to determine that the message sent is the same as the one received.

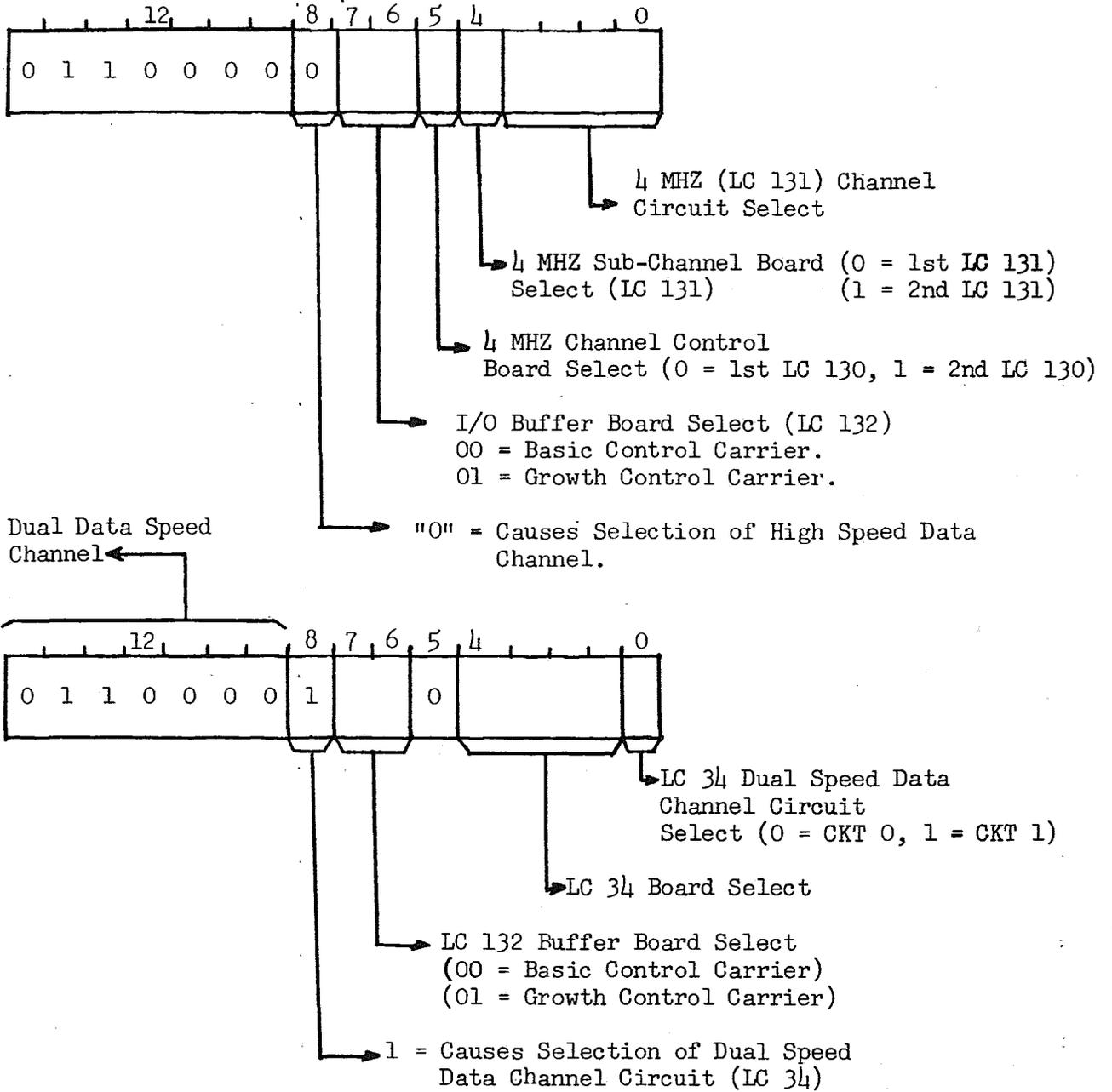
The purpose of the above is to determine that the three maintenance flip flops contained in the LC133 can be set and cleared. The loop test flip flop (LPTST) is associated with the 1st LSB (least significant bit (data)), the POWER flip flop is associated with the 2nd LSB and the ALARM CLEAR flip flop is associated with the 3rd LSB.

The encodes and possible causes are as follows:

ENCODE	DESCRIPTION
1	Failure to either set or clear the POWER or ALARM clear flip flops
2	Failure to set the LOOP TEST flip flop
3	Failure to clear the LOOP TEST flip flop. Note: This type of failure will probably stop all communications with the network modules.
4	Cobination of 1, 2, or 3 above.

Note: Replace LC133 in slot 24 of the basic control carrier before checking test points for other possible causes.

HIGH SPEED DATA CHANNEL CONTROLLER



<p>TEST 1: DISPLAYS FAILURE HISTORY. USE 'NEXT CIRCUIT' TO DISPLAY NEXT FAILED CIRCUIT. USE 'CLEAR DATA', 'EXECUTE' TO CLEAR FAILURE HISTORY.</p> <p>TEST 2: TESTS ALL CKTS. USE 'NEXT CIRCUIT' TO DISPLAY NEXT FAILED CIRCUIT.</p>	<p>TEST 3: TESTS A PARTICULAR CIRCUIT CONTINUOUSLY. USE 'NEXT CIRCUIT' TO DISPLAY NEXT CIRCUIT WITHIN A CARRIER TYPE. OPERATE 'NEXT UNIT' TO ADVANCE TO OTHER CARRIER TYPE.</p>	<p>NOTES: 1. CARR TYPE - 0=BASIC CARRIER 1=GROWTH CARRIER 2. CKT TYPE - 0=HIGH SPEED CHANNEL CONTROL CIRCUIT 1=DUAL SPEED DATA CHANNEL CIRCUIT</p>	<p>DATA CHAN FAIL CODES (FLD 6): 0=PASS 1=ADDRESSING 2=HI SPEED (LO ADDRESS) OR DUAL SPEED LOOP AROUND 3=HI SPEED (HI ADDRESS) LOOP AROUND 4=HI SPEED (HI & LO ADDRESS) LOOP AROUND 5=1 AND 2 OR 3 OR 4.</p>	<p>IO BUF FAIL CODES (FLD 7): 0=PASS 1=BASIC CARRIER 2=GROWTH CARRIER 3=BOTH 1 AND 2</p>	<p>IO AND MEMORY DECODE FAIL CODES (FLD 8): 0=PASS 1=POWER OR ALARM CLEAR 2=CANT LOOP AROUND 3=STUCK IN LOOP AROUND 4=MORE THAN ONE OF 1,2 OR 3</p>
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ISSUE L7.9

PROC 501

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COMMON CONTROL I/O TESTS

TEST NO	TEST 3				DATA CHAN FAIL CODE	IO BUF FAIL CODE	IO AND MEM DEC FAIL CODE	NUMBER OF DUAL SPEED DATA CHANNELS	NUMBER OF DUAL SPEED DATA CHANNEL FAILURES	FAILED DUAL SPEED DATA CHANNEL INDEX	NUMBER OF HIGH SPEED DATA CHANNEL CONTROLLERS	NUMBER OF HIGH SPEED DATA CHANNEL CONTROLLER FAILURES	FAILED HIGH SPEED DATA CHANNEL CONTROLLER INDEX	PROC 501
	EQUIP LOCATION AND TYPE													
	CKT TYPE	CARR TYPE	SLOT	CKT										
1	2	3	4	5	6	7	8	9	10	11	12	13	14	

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