

**INPUT/OUTPUT PROCESSOR**  
**DESCRIPTION AND THEORY OF OPERATION**  
**3B PROCESSOR**

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## 1. GENERAL

**1.01** This section provides a physical and functional description and theory of operation of the input/output processor (IOP) used in the 3B Processor and its application.

**1.02** When this section is reissued, the reason(s) for reissue will be listed in this paragraph.

## PURPOSE

**1.03** The IOP is a flexible 3B peripheral which provides:

- An interface between terminals, data links, other small peripheral units, and the 3B Central Control (3B CC).
- An autonomous input/output (I/O) function via use of the direct memory access (DMA) into the 3B main store (MAS).
- Autonomous controls for the transfers of data blocks to and from peripheral devices (PDs).
- Buffering and data formatting as required by the different PDs.
- A common 3B software driver for all IOP peripherals. (This provides control data to the IOP for 3B output and receives control data from the IOP on the 3B input. Also, the common driver provides an interface between 3B host client software and the various peripherals connected to the IOP.)
- The IOP growth unit is capable of use with the 1A basic unit in the 1A Processor.

**1.04** The IOP can support the following PDs:

- Model 40 teletypewriter (KDP, KD, ROP, EIA RS232C, 1200 baud, 1800 baud, 2400 baud, or 4800 baud) via TTY peripheral controller
- Teletypewriter (compatible Model 40, EIA RS232C, 1200 baud, 1800 baud, 2400 baud, or 4800 baud) via TTY peripheral controller

- Other similar teletypewriters up to 9600 baud asynchronous via TTY peripheral controller
- Standard Bell System (or compatible) RS232C private line or direct distance dialing half or full duplex asynchronous data sets with data rates equal to or greater than 1800 bps via TTY peripheral controller
- Minidisk peripheral controller
- Scanner/distributor peripheral controller
- Application-supplied peripheral controller
- Sync data link peripheral controller
- Bi-synchronous peripheral controller (BYSC PC)
- 9-track tape systems.

## CONFIGURATION

**1.05** The IOP interfaces the 3B processor with as many as four groups of four (16 total) PDs (Fig. 1), so that transfers of data between the PDs and MAS may be made without requiring 3B CC control functions. This reduces real-time requirements on the 3B CC for much of the load of routine control of data transfers and increases the effectiveness of the 3B CC as a system controller. The IOP is connected to the 3B processor via a dual serial channel (DSCH) associated with a direct memory access controller (DMAC) unit. The DMAC facilitates transmission of data blocks between the IOP and the MAS.

## 2. PHYSICAL DESCRIPTION

**2.01** The 3B system may be equipped with as many IOP units as required by the application system (Fig. 2). These units are located in a peripheral control frame (Fig. 3). The IOP is partitioned into two major units: a main unit housing the peripheral interface controller (PIC) and peripheral controller (PC) communities 0 and 1, and a growth unit housing PC communities 2 and 3. Power units are integrated within each of the two communities.

**2.02** The main unit is subdivided into three groups: (1) PIC circuits, (2) PC community 0, and

(3) PC community 1. The PIC circuitry consists of the following:

- One ABB1 3B power switch
- One TN69 duplex dual serial bus selector (DDSBS)
- One TN70 bus interface controller (BIC)
- Two TN62 PICs (microcontrol store)
- One TN61 PIC (controller)
- One UN24 input/output microprocessor interface (IOMI)
- One 136H power converter.

**2.03** Each PC community consists of the following:

- One, two, three, or four peripheral controllers
- One TN71 power monitor/converter
- One 136H power converter.

**2.04** When the 3B system IOP growth unit is used with a No. 1A Electronic Switching System (1A), one UN60 fanout circuit is required to interface with the 1A DMAC unit.

### 3. INTERFACES

**3.01** The IOP interfaces the 3B CC via the DMAC unit and its periphery (Fig. 1). This periphery consists of a DSCH and a DDSBS. The DSCH is located in the DMA I/O unit in the processor frame, and the DDSBS is located in the peripheral control frame and is considered part of the IOP. The DDSBS interfaces the IOP to the DSCH, the DSCH interfaces the DDSBS to the DMAC, and the DMAC interfaces the DSCH to the 3B processor (3B CC and MAS).

**3.02** Interfacing between the IOP and the PDs is provided by the peripheral controllers (PCs). The PC is a single board microcomputer system which functions as an intelligent interface between the IOP controller (peripheral interface controller - PIC) and slow-to-medium speed peripheral units (up to four per PC).

**3.03 DDSBS:** The DDSBS functions as the interface between the IOP and the DSCH. Two ports are provided on the DDSBS to facilitate duplex access to the IOP. Each DDSBS interfaces the DSCH via two bidirectional data leads, a transmit clock, a receive clock, and a request lead. Data is simultaneously transferred via both data leads in conjunction with either transmit or receive clock pulses. The frequency of the clock pulses is determined by the length of cable between the DSCH and DDSBS (10 MHz for distances up to 100 feet, 5 MHz for distances up to 250 feet).

**3.04** Identical start codes transmitted on each channel data lead identify the beginning of a message. All start codes begin with a logic 1 followed by a 1-out-of-3 code. Three start codes are available: 0011 (3), 0101 (5), and 1001 (9). The start codes transmitted to the DDSBS specify the operation to be performed. The start codes are listed in Table A.

**3.05** Identical return messages from the DDSBS to the 3B CC (via DSCH and DMAC) are coded to specify the success or failure of the operation. The return codes are listed in Table B.

**3.06** The DDSBS receives and decodes incoming serial data, executes the specified operation with the IOP (the bus interface controller), and transmits serial reply data to the DSCH. Each DDSBS has a peripheral bus interface (PBI) to interface the peripheral device with the DDSBS. The PBI consists of 46 active low transistor-to-transistor logic (TTL) signals which are: 36 bidirectional data leads, 5 control signals, and 5 response signals.

**3.07 PBI Signals:** The 36 bidirectional data leads are used to send data or commands to the IOP or to receive data or status from the IOP. The data path is 4 bytes wide (36 bits total, 8 bits and 1 parity bit per byte). Parity is odd over each byte and even over the entire 4-byte word. The 3B CC sends control signals to the IOP via the DDSBS (PBI) over five control leads:

- Command Present (CP) - the IOP is instructed to interpret the contents on the data (INF) leads as an IOP command
- Data Present (DP) - the IOP is instructed to interpret the contents on the data (INF) leads as data

- Data Request (DR) - the IOP is requested to gate its data onto the data (INF) leads
- Sense Status (SST) - the IOP is requested to gate its status onto the data (INF) leads
- End-of-Transfer (EOT) - the DMAC sends this signal to the IOP to signify the end of a DMA data block transfer.

**3.08** The IOP responses are gated to the DDSBS (PBI) on the five response leads.

- Synchronization (SYNC) - Upon reception of a control signal, the IOP performs the specified operation and sets the SYNC lead. The SYNC signal is cleared (inactive) in response to the removal of the control signal.
- Error (ER) - The IOP sets the ER lead whenever an abnormal condition has been detected. The DDSBS checks the ER lead after reception of the SYNC signal.
- Interrupt (INTP) - When the IOP requests 3B CC actions (used to report job completions and detection of errors), it sets the INTP lead as an indication to the 3B CC of its request.
- Transfer (XFER) - The IOP sets the XFER lead to signal the DMAC that it is ready to send or receive another word during an autonomous DMA block transfer.
- SETUP - The IOP initiates a DMA setup by activating its SETUP lead. The DMAC will acknowledge the request by transmitting the data request control signal to retrieve the setup information.

**3.09** Data transfers may be performed in one of two modes (32-bit word mode or 16-word block mode). When operating in the 32-bit word mode, **write** operations require 23 shift cycles for transmission (4-bit start code, 16-bit data, 2 parity bits, and 1 dead cycle between data and the start code, simultaneously transmitted over both serial links). Four shift cycles are required for reception. **Read** operations require 4 shift cycles for transmission and 23 shift cycles for reception. Data signals are transmitted in a non-return-to-zero format.

**3.10** When operating in the 16-word block mode, a single start code and a single return code will accompany 16 data words, each word containing 32 data bits and 4 parity bits. Each data word is separated by a single bit cell of dead time to facilitate transferring the next data word between its shift register and its first-in first-out (FIFO) buffer (in the DSCH and BIC). The IOP interrupt and DMA requests are received by the DSCH (via DDSBS) over the single request lead. Pulse width modulated signals are used to make a service or interrupt (maintenance) request. Two types of service requests are provided to accommodate DMA transfers (DMA setup request and DMA data transfer request). An XFER request generates a 150-nanosecond wide pulse, a setup request generates a 350-nanosecond wide pulse, and an interrupt request generates a 550-nanosecond wide pulse. Special circuitry is provided in the DDSBS to resolve conflicts caused by simultaneous multiple request. Included in the DSCH circuitry are three 16-bit registers which store mask bits to individually inhibit requests from each of the 16 PDs it controls. When masked, the request receivers are locked in an inactive state.

**3.11** The PC unit interfaces the IOP to peripheral units. Each PC unit may consist of up to four PC subdevices (PCSDs) and each PCSD controls the PD which requires its function.

#### 4. FUNCTIONAL DESCRIPTION

**4.01** The IOP functions as a front-end processor to control input/output transfers between the 3B MAS and various peripheral units, thereby reducing the load on the 3B CC. A 16-bit bipolar microprocessor called the peripheral interface controller (PIC) interfaces the 3B CC (via DDSBS, DSCH, and DMAC) with up to four PC communities. Each PC community contains four individual PCs and each PC can be equipped with one to four PCSDs. The PIC will autonomously transfer blocks of data between PCs and the 3B MAS. Additionally, the 3B driver program and the PIC will communicate via protocol tables stored in the 3B MAS to initiate jobs and report job completion.

**4.02** Essentially an IOP consists of the following units:

- Duplex dual serial bus selector (DDSBS)
- Bus interface controller (BIC)

- Peripheral interface controller (PIC), which consists of a PIC controller (CONT) and 8K words of microcontrol store (MCS)
  - Input/output microprocessor interface (IOMI)
  - Peripheral controller (PC) which consists of up to four peripheral controller subdevices (PCSDs)
  - Power circuitry.
- 4.03** The IOP contains several autonomous processors.
- A single high-speed bipolar microprocessor, the PIC (also used in the 3B disk file controller), multiplexes up to 16 separate microprocessors onto the 3B dual serial channel on a time-shared basis.
  - The PIC functions as a bus interface, multiplexer, DMA setup processor, error reporting interface, intermediate command buffer, and intermediate data buffer.
  - Each of the 16 separate microprocessors attached to the PIC is a separately functioning PC and each resides on a single board. Each PC is capable of addressing and controlling up to four separate subdevices, peripherals, or separate entities in a single peripheral.
  - The PCs function as data formatters, data buffers, electrical/mechanical interfaces, diagnostic processors, and controllers. Each PC is designed to interface with specialized peripherals on one side and to provide a common interface for data transmission to PIC on the other side.
- 4.04** Communication to the IOP is via the DSCH.
- Thirty-two bit commands are transferred with each operation. Commands may be data transmission from 3B main store in the DMA mode or control commands from the 3B IOP driver in the programmed I/O mode. (The DMA is used for base priority jobs and the I/O is used for high-priority jobs.) Data to and from the IOP is generally transferred in the 3B DMA block mode, 16 data words at a time.
  - The DSCH provides a standardized 3B serial data interface to the IOP.
- 4.05** The DDSBS is considered part of the IOP and provides the interface between the IOP and the DSCH. This unit and its operation are covered in Section 254-301-100.
- 4.06 *Bus Interface Controller (BIC):*** The BIC functions as a buffer between the 32-bit DDSBS and the 16-bit PIC (Fig. 4). Contained in the BIC are a 16-word by 32-bit data FIFO, a 32-bit command register, 32 bits of status flags, and a 16-bit sanity and interval timer. Each is segmented into two 16-bit fields for access by the PIC. The BIC buffers data and commands to the PIC, buffers data and status information from the PIC, and performs the necessary handshaking protocols to communicate with the DDSBS.
- 4.07** The BIC FIFO may be operated in a single 32-bit word mode or in a 16-word block mode. Also, the FIFO may be accessed by either the PIC or the DDSBS but not both at any one time. The 32-bit command register records commands from the 3B CC to the PIC. The PIC may read this register and for maintenance functions write data in the register.
- 4.08** The sanity and interval timer inputs are derived from a 16-bit counter (sanity) on the BIC. Also, the PIC is provided read/write access to this counter.
- 4.09** The flag circuits (32 bits) within the BIC are used to request interrupt and DMA functions from the 3B CC, to signal the PIC of the presence of a 3B CC command or data transfer request, and to record the detection of error conditions. These flags are segmented into status flags (16 bits) and error flags (16 bits). The status flags are:
- Command
  - Command in Progress
  - Data
  - Transfer Mode
  - Data FIFO Word Count
  - Interrupt
  - DMA Transfer
  - End of Data Expected
  - DMA Setup
  - PIC Data Bus Parity Check Enable
  - Interface Enable.

The error flags are:

- Command Register Overflow
- Data Register Overflow
- Data Bus Parity
- Sanity Failure
- PIC Fatal Error Summary
- End of Data
- Setup Overwrite
- Information Parity Failure.

#### 4.10 *Peripheral Interface Controller (PIC):*

The PIC is a general purpose controller used in the disk file and IOP. It consists of a controller (CONT) and up to 65K words of microcontrol store (MCS); the IOP, however, uses an 8K MCS. The MCS circuit pack (TN62) contains a 4K by 40-bit program store and the PIC clock circuit. The MCS circuit pack contains parity check circuits for the microdata word and microaddress decoding circuits for seven additional 4K-word microstore circuit packs. The IOP is equipped with two MCS circuit packs (TN62). Additionally, the PIC controller contains a 16-bit register and arithmetic/logic unit (RALU), a 16-bit microprogram sequencer, and a condition test multiplexer.

4.11 The PIC controller (Fig. 5) also contains a 4K by 18-bit (16 data and 2 parity) random access memory (RAM) used for data storage. Associated with the RAM is a 12-bit RAM address sequencer (RAD), which provides a 4-level stack onto which interim addresses can be gated and retrieved. An incrementer is provided for automatic incrementing capability.

4.12 The functions performed by the PIC are divided into two levels: the base level and the interrupt level. Deferrable tasks are performed during base level processing and nondeferrable tasks at interrupt level. The PC service requests (SR) are processed during the PIC base level loop. The PIC interrogates the PC service request register to determine which PCs are requesting service. The PIC then reads the PC status register to identify the type of job to be performed and executes that job. Job sizes are restricted to a maximum transfer size of 2048 bytes. The PC will segment the message into small blocks.

4.13 After responding to a PC request, the PIC compares the load and unload pointers for the job queue stored in the 3B MAS. If the queue is not empty, the PIC unloads up to eight jobs and distributes these to the designated PCs. Next

the PIC scans the status bits for changes in the PC units out-of-service status to detect power converter failures. Then the PIC scans for PC error report messages and, if errors are present, gates the message to the 3B CC.

4.14 Interrupts are used to initiate time critical tasks. A timed interrupt routine will be entered at a fixed rate (normally 100 milliseconds). The sanity timer is reset at this time. Additionally, the job completion queue is interrogated and, if not empty, loaded into the response buffer in the 3B MAS. The PIC then interrupts the 3B CC. High priority jobs and programmed I/O commands use the interrupt level.

#### 4.15 *Input/Output Microprocessor Interface (IOMI):*

The IOMI functions as the interface between the 16-bit PIC and up to four PC communities (Fig. 6) of four 8-bit PCs each. The interface between the IOMI and each PC community consists of a 16-bit memory address, an 8 + 1 parity bit bidirectional data bus, and eight control leads. In addition, a private PC select lead is connected to each of the 16 PCs. The selected PC acknowledges the reception of a control signal by setting its control signal acknowledge (CSA) signal. The 16 CSA bits are compared to the 16 PC select signals to indicate to the PIC when the acknowledgement has been received.

4.16 Each PC has three request leads which are used to report errors or to request service. Each PC is assigned a dedicated bit in each of the three 16-bit request registers.

4.17 The PIC maintains control over its PCs via 8 bused control pulses and 16 private PC select signals (one per PC). The selected PC acknowledges receipt of the control pulse by setting a private CSA lead. The PIC verifies that only the appropriate PC responded by matching the 16 PC selects with the 16 CSA signals.

4.18 The eight control pulses are divided into two classes; four pulses control PC memory access operations and four perform miscellaneous maintenance functions. Four fanout branches are provided to isolate communities. The sequence of events corresponding to the PIC reading or writing the PC memory is outlined below:

- The PIC issues a DMA request (DMARQ) to the selected PC. The PIC then waits for

up to 20 microseconds for the corresponding CSA. The PC will not acknowledge the request until the memory is available for exclusive use by the PIC.

- After the receipt of CSA, the PIC issues a succession of DMA read and/or write pulses (DMARD and DMAWR). To avoid holding the microprocessor out of the memory for a period long enough to cause problems, the PIC is constrained to perform no more than 16 accesses during any one request.
- After the completion of the sequence of DMARDs and DMAWRs, the PIC issues a DMA operation complete pulse (DMAOC) to return control of the PC memory to the microprocessor.

**4.19** The four remaining pulses are as follows. The interrupt command lead (CINT) is utilized by the PIC to request interrupt service from the PC. Interrupts are used to initiate high-priority job commands. Two signals are provided to allow the PIC to set and clear the bus isolation flip-flop resident on the PC. When the flip-flop is set, the PC bus driver circuits are forced into a high impedance state, isolating them from other circuits on the same bus. In this manner, faulty circuits can be removed from the shared buses without degrading the service of the remaining PCs. Resetting the isolation flip-flop enables the bus drivers. The last control signal, called clear (CLR), provides a means by which the PIC can initialize an individual PC.

**4.20 Error Summary Signals:** The detection of hardware failures in the PC circuitry is reported to the PIC via a private error signal per PC. Activation of this signal sets an error indicator in the IOMI. The PIC periodically scans the IOMI error register and, upon detecting an error, isolates the faulty PC from the bus, marks the PC out-of-service, and issues a high-priority error report to the 3B driver.

**4.21 Work Request Signals:** Two private signals are provided for each PC to request service from the PIC. The detection of pulses is latched in two 16-bit request registers in the IOMI. One register stores service request (SR) pulses and is scanned by the PIC to determine which PCs require normal job servicing. The other register accumulates interrupt requests (INT) which are

employed by the PC to request immediate high-priority service. Each of the 16 PCs has a unique SR and INT request pair.

**4.22 Memory Address and Data Buses:**

The PIC accesses the PC over an 8 + 1 parity bit bidirectional data bus and a 16-bit memory address bus. The data bus is reversed during the presence of the DMARD control pulse. Odd parity is generated by the sender and checked by the receiver during all data bus operations. Four fanout branches are provided for the data and address buses to isolate PC communities.

**4.23 Peripheral Controller (PC):** The PC is a single circuit pack microcomputer system which functions as an interface between the PIC and slow-to-medium speed peripheral devices. The PIC can directly address up to four subdevices (4 PCSDs per PC). Each PCSD is capable of initiating several types of work requests and providing the interface to the PD.

**4.24** Each PC unit consists of the following circuitry:

- PCSD
- Microprocessor (MP)
- Read only memory (ROM)
- Random access memory (RAM)
- Pulse source generator
- Isolation circuitry
- Error detection logic
- Scan back circuitry
- Dual access memory (DAM).

**4.25** The power circuitry used in the IOP is described in Part 6 of this section.

**4.26 Communications Summary:** The 3B CC generates the programmed I/O instructions to the PIC (via DMAC, DSCH, DDSBS, and BIC). These instructions define job storage locations in the 3B MAS. The PIC uses the DMAC functions to receive the job operation and transmit the operation to the designated PD (via the PC).

**4.27** The PIC drives four internal buses, each connected to a maximum of four PC communities. Each PC community can support as many as four PDs (via PCSD). The PC community is comprised of microprocessor-based circuits performing the actual peripheral control, while the PIC performs the DMA data transfers between the 3B MAS and local memories in the PC communities. The assigned job is interrogated by the PC microprocessor, which then initiates the procedure to complete the assigned job. These jobs may consist of operational tasks or maintenance tasks.

**4.28** Operational tasks include data transfers from the 3B MAS to a data link, file store, or PC memory, or data transfers to the 3B MAS from the PDs or PC memory. Each PC community segments the 3B MAS job into sizes it can process and initiates the DMA access by setting service request flags which are detected by the PIC. Upon completion of a task, the PC community responds to the 3B with a task completion message.

**4.29** Maintenance tasks include looping of messages, diagnosing PCSDs, self-diagnosing of the PC, PC isolation, PCSD removal/restoral to service, and other maintenance functions.

## 5. THEORY OF OPERATION

**5.01** The IOP consists of the following units:

- Duplex dual serial bus selector (DDSBS)
- Bus interface controller (BIC)
- Peripheral interface controller which consists of a PIC controller and 8K words of microcontrol store
- Input/output microprocessor interface (IOMI)
- Peripheral controller
- Power circuitry.

**5.02** *Bus Interface Controller (BIC):* The BIC functions as a buffer between the 32-bit DDSBS and the 16-bit PIC. The BIC contains:

- 16-word by 32-bit data FIFO buffer
- 32-bit command register

- 32-bit status flag circuit
- 16-bit sanity and interval timer.

Each of these elements is divided into 16-bit segments for PIC use. The BIC buffers data and commands from the DDSBS to the PIC and data and status information from the PIC to the DDSBS. It also performs handshaking protocols with the DDSBS for communication operations.

**5.03** The BIC data FIFO can be operated in a single 32-bit word mode or in a 16-word block mode. It may be accessed by either the DDSBS or the PIC but not both at once. Parity checks on transfers between the BIC and the DDSBS are always performed by the BIC and, if a parity error is detected, an error flag is set. Parity checks on transfers between the BIC and PIC are performed if the state of an internal flag (controlled by the PIC) is not set.

**5.04** The 32-bit command register contains command data for the PIC from the 3B CC. When the PIC is signaled that a command is present and the PIC is not busy, the contents of the command register are gated to the PIC. For maintenance purposes the PIC may write data into this register.

**5.05** Sanity and timed interrupts are derived from the 16-bit sanity and interval timer counter. The PIC is provided read/write access to this counter. The counter is incremented every 2.5 or 5 microseconds (depending upon optional wiring). A timed interrupt is triggered whenever the two most significant bits of the counter are 1s (counter contents  $\geq 50,000$ ). A sanity error flag is set whenever the counter overflows. To prevent sanity errors, the timed interrupt routine must be entered within 75 milliseconds after it is triggered. The interrupt routine will then restore the counter to its initial value. Interrupt intervals from 0 through 250 milliseconds can be obtained by loading an initial value of 50,000 through 0 respectively into the counter. The timed interrupt routine will report job completions that have occurred during the last timed interval via an interrupt entry to the IOP driver. Sanity failures set a status bit in the BIC to report detection of an error to the 3B CC.

**5.06** Flags within the BIC are used to request interrupt and DMA functions from the 3B

CC, to alert the PIC of the presence of a 3B CC command pending or data transfer request, and to record detection of errors. There are 16 status flag bits and 16 error flag bits.

## BIC STATUS FLAGS

**5.07** The **command flag** reports the status of the BIC command register. The command flag is set upon registration of a command from the 3B CC in the command register and cleared when the command is read by the PIC. The PIC reads the register in two stages: the most significant 16 bits first and then the 16 least significant bits. The command flag is automatically cleared after the PIC reads the 16 least significant bits. When the command flag is set by the 3B CC, a PIC interrupt is generated and the PIC will then retrieve the command and execute it.

**5.08** The **command in progress flag** is automatically set when a command is received from the 3B CC. After the PIC has executed the command, it clears the command in progress flag to signal the 3B CC that the command was executed.

**5.09** The **data flag** is used to specify which interface (PIC or DDSBS) may access the data FIFO buffer. When the data flag is set, the PIC may read or write data out of or into the buffer. When cleared, the 3B CC may access the buffer via the DDSBS. The flag toggles between set and clear during data transfers and toggles alternately for the PIC to write data into the buffer and the 3B CC to read it and vice versa. When the buffer is in the 16-word block mode, the flag will be toggled every 16th transfer. When in the 32-bit word mode, the flag is toggled after every data transfer.

**5.10** The **transfer mode flag** is set when the buffer is in the 16-word block transfer mode and cleared when the buffer is in the single word transfer mode. Both the PIC and the 3B CC (via DDSBS) have access to this flag in order to determine/specify the buffer mode at any time.

**5.11** The **data buffer word count flag** is a 5-bit flag indicating the number of words stored in the data buffer (from 0 through 16). The count is incremented whenever a word is loaded into the buffer and decremented whenever a word is unloaded.

**5.12** The **interrupt flag** is set whenever the PIC requests service from the 3B CC. An interrupt mask is included in the DSCH to permit the 3B CC to block interrupt requests.

**5.13** The **DMA transfer and setup flags** are set by the PIC to request DMAC functions. A mask is provided in the DSCH to permit the 3B CC to block DMA requests.

**5.14** The **end of data expected flag** is set by the PIC at the end of a DMA block transfer. The BIC will verify that the DMAC acknowledges the transfer is complete. Any errors will result in the generation of an error signal (end-of-data error) and transmission of the error signal to the 3B CC. The successful completion of a transfer is indicated by the BIC setting the end-of-data-received flag. The PIC reads the BIC status flags to determine when the operation is completed.

**5.15** The **PIC data bus parity checks enable flag** enables or inhibits parity checks over the PIC data bus. Correct parity is always forced by the BIC regardless of the state of the flag. When parity check circuits are disabled, the PIC may write information from the arithmetic/logic unit (ALU) into the BIC and the BIC will provide the parity bits (parity is not gated through the PIC ALU).

**5.16** The **interface enable flag**, when cleared by the 3B CC, prevents the PIC from communicating with the BIC. The BIC is disabled for diagnostics by this flag.

**5.17** The **command register overflow error flag** may be cleared by both the PIC and 3B CC. This flag is set if the PIC reads the command register while the command flag is cleared (register is empty) or attempts to write data into the command register while the command flag is set (the PIC essentially attempts to overwrite a 3B CC command). The write operation is inhibited when the command flag is set.

**5.18** The **data register overflow error flag** may be cleared by both the PIC and the 3B CC. It is set if the PIC attempts to access the data buffer while the data flag is in the 3B CC operation state. Also, the flag is set if the PIC attempts to read an empty buffer or the PIC attempts to write data into a full data buffer. The data buffer is not loaded or unloaded when this error occurs.

**5.19** The **data bus parity error flags** may be cleared by either the PIC or the 3B CC. The flags are set if the parity check enable flag is set and even parity is detected during a PIC read or write operation of the command register or data buffer. Separate flags are provided to record errors over the high and low bytes. Write operations are inhibited when this flag is set.

**5.20** The **sanity failure error flag** may be cleared only by the the 3B CC. It is set if the PIC sanity and interval timer overflows.

**5.21** The **PIC fatal error summary error flag** may be cleared only by the 3B CC. It is set under program control by the PIC to report an unrecoverable error. Sanity failures also set this flag.

**5.22** The **end of data error flag** may be cleared only by the 3B CC. It is set if the end-of-data-expected flag is set and the 3B CC requests a read or write data operation (data transfer underrun error) or if the end-of-data-expected flag is not set and the end-of-transfer signal (EOT) is received (data transfer overrun error).

**5.23** The **setup overwrite error flag** may be cleared only by the 3B CC. It is set if a DMA setup request is pending and the 3B CC performs a write data operation. This will overwrite the setup information stored in the data buffer.

**5.24** The **INF parity failures error flags** may be cleared only by the 3B CC. These are set if even parity is detected over the information (INF) bus during read and write operations of the data buffer and during write operations of the command register. Individual flags are provided to record failures over each of the four bytes. Parity is neither checked nor generated during 3B CC read status operations.

**5.25** The 3B CC can address commands to the BIC to manipulate these flags. The BIC commands are not loaded in the command register and do not set the command flag. The BIC commands are differentiated from PIC commands by the presence of 00 in bits 1 and 2. Bit 0 is assigned for DSCH and DDSBS maintenance functions. The BIC command layout is shown in Table C.

**5.26** The BIC status is interrogated via the sense status control signal (SST) in the peripheral bus interface in the DDSBS. The BIC does not maintain parity over its status word. The BIC status word layout is shown in Table D.

**5.27** The PIC reads and writes various data within the BIC over its data bus. The PIC specifies a 5-bit code (SRC) defining the register data to be gated onto the bus and a 5-bit code (DST) defining the register to be loaded from the bus. The PIC can interrogate the state of the BIC status error flags via codes 8 and 9 (decimal) respectively. Source codes define transmitting circuit and destination defines receiving circuit. Layouts of the bit fields are shown in Table E.

**5.28** The PIC manipulates various BIC flags via destination code 8 as shown in Table F.

**5.29** The PIC reads and writes the various entities within the BIC via source and destination codes 8 through 15. See Table G.

### **5.30 Peripheral Interface Controller (PIC):**

The PIC consists of a controller and up to 65K words of microcontrol store (MCS), however, the MCS in the IOP PIC is an 8K-word MCS. The MCS circuit pack (TN62) contains a 4k by 40-bit program store and the PIC clock circuit. Also, the MCS circuit pack contains parity check circuits over the microdata word and microaddress decoding for an additional 4K-word microstore circuit pack (two TN62 circuit packs are used in the IOP). The PIC controller (TN61) contains a 16-bit register and arithmetic/logic unit (RALU) and a 16-bit microprogram sequencer.

**5.31** The four output conditions of the RALU (carry, overflow, sign, and zero), accompanied with the four external conditions, are gated into a condition test multiplexer. The multiplexer is used during conditional branch instructions. The four external test inputs are specified by the application system. The IOP assignments are as follows:

TEST 0	Connected to BIC data flag (DFLG) and used to determine when BIC data buffer is available
TEST 1	Spare
TEST 2	Connected to BIC error summary

TEST 3 IOMI data register parity error.

**5.32** A 4K by 18-bit (16 data and 2 parity) RAM is contained on the controller and used for data storage. Associated with the RAM is a 12-bit RAM address sequencer (RAD), which serves as a 4-level stack for storage of interim addresses as well as an incrementer which provides automatic incrementing of addresses.

**5.33** Eight vectored priority interrupt levels are designed into the PIC circuit. A 7-bit mask register is included to individually block-selected levels. Level 0 is reserved for a reset function and is unmaskable. Level 1 is assigned to parity failures over the microdata word and level 2 is assigned to the instruction timer. The IOP interrupt assignments are as follows:

Level 0	SPARE and left unconnected
Level 1	MCS parity errors
Level 2	Instruction timer
Level 3	Connected to the comand flag (CFLG) in the BIC (this interrupt used to alert PIC of presence of a command from 3B CC awaiting execution in BIC)
Level 4	Spare and left unconnected
Level 5	Connected to the PC interrupt request summary formed in the IOMI
Level 6	Spare and left unconnected
Level 7	Derived from the interval timer on BIC.

**5.34** Sixteen interrupt vectors are stored at locations 3F0 through 3FF. The layout of this interrupt jump table is shown in Table H. Bit 7 of the interrupt mask is used to specify whether the normal or maintenance routine should be entered. This feature, along with the capability to write the interrupt register, is used by the PIC to verify proper operation of the interrupt circuitry.

**5.35** A 32-bit microdata register resides in the controller. The output of this register controls the various entities within the PIC. To select the

instruction operands, 5-bit source (SRC) and destination (DST) fields are used. The first eight source and destination codes are defined internal to the PIC. The IOP source and destination codes are listed in Table I.

**5.36** An overlay field in the PIC instruction word is used to specify parameters of the instruction. A 2-bit field in the microinstruction specifies whether a branch or arithmetic/logic operation is to be performed (ie, how the overlay field contents are to be interpreted). Arithmetic/logic instructions use the overlay field to specify the operation type. A 9-bit instruction is gated into the RALU to specify an operation (FCN field) and its operands (SRC and DST fields). The carry into the RALU is specified by another bit. Internal to the RALU are 16 general registers and a single special register (Q). Instructions specifying pairs of general registers as operands use the A and B address fields. The RALU utilizes a 2-address architecture; ie, all operations are of the form  $B \leftarrow A \text{ op } B$ .

**5.37** Branch instructions can be of two basic types: conditional and unconditional. Unconditional jumps and subroutine calls to an immediate 15-bit address are included as branch functions F and E, respectively. Conditional jumps, subroutine calls and returns, and file movements use a 3-bit condition field and a 12-bit immediate address. The 3-bit condition field controls the test multiplexer to select one of eight test conditions. Both branch if true and branch if false instructions are provided.

**5.38** The overlay field may be used for transferring immediate data to a destination register external to the RALU. Immediate data operations do not permit RALU operations since the fields overlap. To move immediate data into an RALU register, it must first be moved to an external register and then into the RALU. A special scratch register has been provided in the PIC for this purpose (source and destination = SCR = 4).

**5.39** A single bit in the microinstruction is used to specify whether interrupts are enabled or inhibited. When inhibited, requests on interrupt lines 1 through 7 will not be honored. Interrupt level 0 (RESET) cannot be blocked and, when active, will always initiate an interrupt. Each microinstruction contains a 4-bit field which specifies the instruction execution time.

**5.40** Instruction speeds may vary from 100 through 300 ns in increments of 50 ns. The instruction timing circuitry resides on the MCS. Because of the usage of 4-bit wide PROMs, the microcontrol store parity bits are nibble-sliced (4-bit partitioned). Parity is maintained across bit 0 of each PROM, across bit 1 of each PROM, etc. The detection of a parity failure will trigger an interrupt.

**5.41** A 16-bit scratch pad overlay function has been provided. When selected as the operation destination, the data bus contents selected by the source field replaces the overlay field of the microinstruction. This provides a mechanism for implementing table-driven sequences of operations used for diagnostics.

**5.42 *Input/Output Microprocessor Interface (IOMI):*** The IOMI functions as the interface between the 16-bit PIC and the 8-bit PCs. It consists of a 16-bit memory address, a 9-bit (8 data and 1 parity) bidirectional data bus, and eight control signals. Also, a private PC select signal is connected to each of the 16 PCs. The selected PC acknowledges reception of a control signal by setting the control signal acknowledge (CSA) signal. The 16 CSA bits are compared to the 16 PC select signals to indicate to the PIC when the acknowledgment has been received.

**5.43** Each PC has three request leads which are used to indicate errors or to request service. Each PC is assigned a bit in each of the three 16-bit request registers. A low level on the error signal will set the PC error flag. The trailing edge of the active low interrupt and service request signals will set the designated bit in the interrupt and service request registers respectively. A summary bit is provided over the interrupt register contents which triggers a PIC interrupt whenever any bits are set. The PIC reads the data and clears the interrupt and service request registers via destinations 17 and 18. Special circuitry is provided to ensure that requests will not be lost nor sensed twice by the PIC. The PIC can read the contents of the error register using destination 19 and clear the register via destination 25. A read-and-clear operation consists of two sequential operations 200 nanoseconds apart.

**5.44** The four fanout branches of the data, address, and control signals (one per PC community) are driven from three common registers. The 16-bit memory address register is implemented

using binary up/down counters to provide auto-increment and autodecrement capability. The mode of operation is specified by bits 8 and 9 of the control signal register. Special circuitry is provided to ensure 200 nanoseconds of address setup and hold times around the trailing edge of the active low memory read and write control signals. The PC memory access and cycle times are approximately 400 and 600 nanoseconds respectively.

**5.45** The 18-bit (16 data and 2 parity) data register is divided into high and low bytes to be transmitted a byte at a time to and from the 9-bit (8 data and 1 parity) PC data buses. A flag in the control register selects the high or the low byte as the source or destination of the data transfer between the IOMI and the selected PC. An additional bit in the control signal register is used to toggle the data byte selector flag after a memory read or write cycle. A delay timing chain circuit is provided to ensure 50 nanoseconds of data hold time during memory write operations.

**5.46** The control signal register is segmented into two fields: an 8-bit register (the outputs of which directly drive the control signal buses) and an 8-bit field (which controls the internal functions in the IOMI). The control signal register bits and corresponding functions are listed in Table J.

**5.47** The maintenance register output is determined by bits 0 through 3. The function of this register is to force parity errors, requests, and power failures. The maintenance register bits and corresponding functions are as follows:

0	Force power monitor fail
1	Force all INT and SR bits set
2	Force parity error (low byte)
3	Force parity error (high byte)

**5.48** An out-of-service bit is provided for each of the four PC communities. This 4-bit register can be read and written by the PIC. Additionally, a power-down condition within a PC community will automatically set its out-of-service flag. When out of service, the interrupt requests of the four PCs within that community are not ORed into the interrupt register summary.

**5.49** The IOMI source and destination codes are listed in Table K.

**5.50 *Peripheral Controller (PC):*** The PC is a microcomputer that functions as the interface between the PIC and slow-to-medium speed PDs. The PIC can directly address the four peripheral controller subdevices (PCSD) of the PC community. The PCSD also indicates to the PIC (via the PC using service request signals) jobs to be performed. The PIC reads the PC service request status information to determine the type of job to be performed.

**5.51** A PCSD activates a service request in order to transfer data to or from the MAS or to indicate that a job has been completed. The PCSD may initiate an interrupt request which results in a PIC interrupt request status information read operation. The interrupt request is activated by a PCSD to transfer high-priority information to or from the MAS or to indicate completion of a high-priority job.

**5.52** All communication between the PIC and the PC is accomplished via a dual access memory (DAM) circuit in the PC. Dedicated memory locations are reserved within the DAM which contains pointers used by the PIC to locate PCSD data buffers, data transfer parameters, and status and command areas. In addition, the DAM contains memory locations that contain PC data. An asynchronous response register is provided for each PCSD. The PC data consists of service and interrupt request data and PC command area pointers. The PIC gates commands to the PC to set up data transfer jobs and to administer error detection and fault recovery action. The PC and each PCSD has a command area located in the DAM. The PC interprets the commands and initiates appropriate action as required.

**5.53** The PC consists of the following circuits:

- Microprocessor (MP)
- Read only memory (ROM)
- Random access memory (RAM)
- Pulse source generator
- Isolation circuitry
- Error detection logic
- Scan back circuitry.

**5.54 *Microprocessor (MP):*** The PC uses an MP to administer the transfer of data between its PDs (via PCSD) and MAS. The MP receives inputs from the PD and the PIC with the PIC inputs assigned control priority.

**5.55 *Read Only Memory (ROM):*** The PC contains a bootstrap program stored in the ROM, which is entered when power is initially applied or when the PC reset function is activated by the PIC. The bootstrap program, when used, causes the MP to initialize the PDs (via PCSDs) and to scan for PIC commands. In addition to the bootstrap program, the ROM may contain operational and diagnostic programs (determined by application system).

**5.56 *Random Access Memory (RAM):*** The PC uses RAM memory to store operational program, buffer transient data, and PIC communication parameters. The portion of the RAM containing data buffers and communication parameters is accessed by both the PIC and PC MP. Some PCs have separated program and data store. In such cases, the PIC has direct access only to the data store.

**5.57 *Isolation Circuitry:*** The isolation circuitry provides the capability of removing all response signals generated by the PC from the communication bus connected to the PIC. Isolation is provided by removing +5 volt power from the device(s) generating the response signals. An isolation control logic (ICL) circuit on the PC accomplishes this isolation. Upon receiving a set isolation flip-flop or clear signal from the PIC, the isolation control logic circuit will remove the +5 volt power from the designated device(s). The PC isolation state will remain in effect until a reset isolation flip-flop signal is sent from the PIC. This circuit is used to inhibit MPs from overloading the communication bus with invalid data if a fault condition develops.

**5.58** Error detection uses parity check, clock check, and sanity check circuits. Routine maintenance diagnostics are also provided. The PC provides parity checking and parity generation for the data contained in the RAM memory. Routine diagnostics have the responsibility of error

detection in the RAM memory. The sanity check is provided to detect ROM data failures. Also, a parity error flip-flop is used to store the indication of a RAM parity failure.

**5.59** The PC operates autonomously with respect to PIC activity and provides its own internal system clock. A system clock check circuit is provided by the PC to detect clock activity failures. A clock error flip-flop is used to store a clock failure indication. The resulting signal is gated to the PIC to report detection of these failures via the error lead.

**5.60** The PC uses routine maintenance diagnostics (RMD) to increase error detection capabilities. Redundant software (instead of redundant hardware circuits) is used to detect fault conditions. The PC MP periodically (dependent upon application system) executes routine maintenance diagnostics during nonpeak data transmission time intervals. An RMD flip-flop is provided to store the RMD failure indications.

**5.61** To ensure program execution, the PC provides a sanity check circuit. This circuit is used to detect MP failures and to prevent an MP failure from resulting in a fatal IOP operation. A sanity failure flip-flop is used to store the sanity failure indication.

**5.62** The PC provides four directly addressable read only bytes of information for the scan back circuitry. These are as follows:

BYTE	CONTENTS
0	Status and error information
1	Address lower loop-around data
2	Address upper loop-around data
3	PC type identity code.

**5.63** The PIC retrieves the information located at the associated address by activating the corresponding PC select lead, sending the correct DMA address code, and activating the DMARDO signal. Only the two least significant address bits are used to select one of the scan back bytes. The remaining address bits are not used and can be in any state. The scan back data is returned to the PIC via the common data bus. The scan

back circuitry is disabled during a PIC access of the PC DAM to prevent interaction with the DAM data (this is selected by the DMARQ signal).

**5.64** The DMA address leads are connected to scan back locations 1 and 2. The PIC uses the scan back address data in a loop-around mode to check the integrity of the DMA address and data buses to verify that the designated PC is receiving the complete address information. The PC type identity code is located at scan back address 3 and is used by fault recovery and administration programs to determine and verify the PC type.

**5.65** The PC generates a service request (SR) or an interrupt request (IR) whenever a data transfer to or from the MAS is required or to indicate a command completion response is available. The PC provides a separate pulse source for the IR and SR indications. The PIC IOMI circuit pack uses the trailing edge of the active low SR or IR to set the associated job pending indicator flip-flop. The PC should not gate a new SR or IR until the previously sent request has been detected by the PIC. The PIC indicates recognition of an SR or IR by clearing the associated request pending flag in the PC DAM.

**5.66** Each PCSD within the PC is assigned four bytes of the DAM, which contains status information for the assigned PCSD. The status information is comprised of generic and user-defined data.

**5.67** The DDSBS is described in detail in Section 254-301-100. Also, the power circuitry and requirements are discussed in Part 6 of this section.

## **6. POWER**

### **INTRODUCTION**

**6.01** The IOP power circuits (Fig. 7) require 15 amperes at -48 Vdc which is supplied by the peripheral control frame from the -48V office source. See Section 254-301-020 for system power requirements. The voltages produced by the IOP power circuits are partitioned into the PIC circuit and each PC community. These voltages are:

- -48V for each PC community (TTY current loop)

- +12V and -12V for each PC community (EIA RS232C line drivers and receivers)
- +12V and -5V for each PC community (TN71 for the memory devices)
- +5V for each PC community and PIC circuit (TTL)
- +12V for reference circuits on the TN71 circuit pack.

**6.02** When power is applied, the 3B power switch (ABB1) first enables the 136H dc-to-dc converter start leads to produce +5V. In the PIC, this lead is interlocked by the BIC and in each PC community, it is interlocked by the converter/monitor circuit (TN71). (If any of these circuit packs are not equipped, power cannot be supplied.) Approximately 600 milliseconds later, the start B sequence occurs which starts the memory power converters (TN71). The TN71 circuitry will internally sequence memory power so that -5V is on before the +12V.

**6.03** Approximately 1 second after the beginning of the voltage sequence, the power clear (INIT) and bus power enable (BPEN) signals become active. The input voltage to the power switch (ABB1) is sensed to verify that the sequence has been completed prior to activation of these signals.

**6.04** When power is removed, the reverse sequence occurs. Power clear (INIT) and bus power enable (BPEN) signals become inactive. Then the +12V (memory) and -5V (memory) powers, which are self-sequenced by the TN71 circuitry, are removed. Finally, the +5V logic power is removed before the OFF lamp on the power switch (ABB1) is lit.

**6.05** Power is segmented in the IOP so that any PC community may be individually powered down without affecting the remaining active portions of the IOP. There are interlocking switches on the 136H dc-to-dc converter and the TN71 power monitor/converter so these may not be removed from the frame without first removing power from the PC community. Removal of the TN71 circuit pack also removes -48V from the IOP. Also, if the PIC is powered down, the entire IOP unit will be automatically powered down.

**6.06** All voltages except for the +12V (memory) and the -5V (memory) are fused. The +12V

and -12V (EIA) and -48V powers are fused on a PC community basis. The -48V backplane and -48V input voltages to the TN71 circuit pack are fused by one fuse. Each circuit pack in the PIC has a fuse in the +5V lead. Each pair of circuit packs in the PC community has a fuse in the +5V lead.

**6.07** In the event of a fuse failure in any PC community, the power alert lamp is lit on the power switch (ABB1). This closes a set of contacts which can be connected to the office minor alarm circuit. If a fuse failure causes the loss of all +5V power from a PC community, memory power will be sequenced down by the converter/monitor (TN71) circuit and that PC community will be marked out-of-service to the IOMI. If any fuse fails in the PIC circuit, the entire IOP unit will be powered down by the power switch (ABB1). This will also close a set of contacts which can be connected to the office major alarm circuit.

**6.08** Due to the volatile nature of the memory on each PC community and the potential for problems which exist should bad data be transmitted or received, each voltage in the PC community is monitored as follows:

- EIA voltages are regulated by the 136H dc-to-dc converter to be no greater than 18V. The converter/monitor (TN71) circuit checks to verify that voltage is greater than  $\pm 4.5V$  (backplane).
- Memory voltages are generated and checked on the converter/monitor (TN71) to verify the voltages are between 8 and 10 percent of nominal value.
- Logic voltages generated by the 136H dc-to-dc converter are checked to verify the voltages are between 8 and 10 percent of nominal value.

In the event that any of these conditions are not met, the power alert lamp on the power switch (ABB1) is lit. Also, the PC community is marked out-of-service by the IOMI.

**6.09** Five light-emitting diodes (LEDs) are mounted on the front of the converter/monitor (TN71) circuit pack. These indicate:

- +5V (TTL) out of tolerance (OOT) - Red LED.

- +12V or -12V (EIA) OOT - Red LED.
- -5V or +12V (memory) OOT - Red LED.
- TN71 internal voltages OOT - Red LED. The TN71 converter/monitor circuit generates its own logic power and reference voltages from the -48V.
- PC unit marked out-of-service (OOS) by the IOMI - Yellow LED.

#### ABB1 POWER CONTROL SWITCH

**6.10** The ABB1 power control switch (Fig. 8) controls the application and removal of frame power. Five indicator lights on the front of the switch indicate the state of the unit being controlled. These lights are OFF, ALM (alarm), OOS (out-of-service), RQIP (request in progress), and ROS (request out of service). Five pushbutton switches provide power control. These are located on the front and are ON, OFF, ROS/RST (request out of service/request restore), ACO/T (lamp test/retire major alarm), and MOR (manual override). Input voltage requirements are -48V from the office supply and +5V from the 136H dc-to-dc converter controlled by the switch.

**6.11** Three-phased start signals are provided by the power switch to control the application sequence of logic power, memory power, and input/output bus power. The following functions may be performed by the craft:

- Sequentially supply or remove power
- Initiate system request to remove from service or restore to service the associated unit
- Test indicator lights on the power switch
- Retire a major office alarm generated at the associated unit.

**6.12** The 3B power switch controls are as follows:

(a) **Lamps/Switches:** Figure 8 shows a front view of the 3B power switch. The ON, OFF, and MOR are momentary pushbutton switches and ROS/RST and ACO/T are two position-latching switches. The five indicators are 549-type LEDs.

(b) **On Switch:** Momentarily depressing the ON switch when the ACO/T switch is not in its retire alarm state initiates the power-up sequence. Depressing the ON switch when the ACO/T switch is in its retire-alarm state or when frame power is up causes no change in state of the power switch.

(c) **Off Switch:** Momentarily depressing the OFF switch when the unit is in its out-of-service state initiates the power-down sequence. Depressing the OFF switch when the unit is in service or when power is off causes no change in state of the power switch.

(d) **ROS/RST Switch:** Depressing the ROS/RST switch to the ROS position requests the unit be taken out-of-service via scan point SCX and lights the ROS LED. Depressing the ROS/RST switch to the RST position requests the unit be restored to service.

(e) **ACO/T Switch:** Depressing the ACO/T switch to the retire-alarm state tests all lamps on the power switch, provides an external lamp test signal, silences the office major alarm originated at the power switch, and extinguishes the ALM LED, if lit.

(f) **MOR Switch:** Simultaneously depressing the OFF and MOR (manual override) switches defeats the interlock between the OFF switch and unit out-of-service state and initiates the power-down sequence.

(g) **OFF LED:** The red OFF lamp is lit when the unit is in its power-off state and extinguished when the unit is in its power-up state.

(h) **ALM LED:** The red ALM lamp lights to indicate the presence of power-related faults.

(i) **OOS LED:** The yellow OOS (out-of-service) lamp is system activated via the OOS signal distribute point when the unit is marked out of service.

(j) **RQIP LED:** The green RQIP (request in progress) lamp lights to indicate the system has received a request to take the unit out of service or restore it to service. This lamp, which is system-activated via the RQIP signal

distribute point, flashes to indicate the request has been denied.

(k) **ROS LED:** The green ROS (request out of service) lamp is lit when the ROS/RST switch is in its ROS state.

**6.13 Scan, Alarm, and Signal Distribute Points:** Three scan points (SCX, SCY, BPP - not presently used), two alarm points (MJ, PA), and two signal distribute points (OOS, RQIP) are provided. Each scan and alarm point consists of an isolated metallic contact. The active "1" state appears as a resistance of less than 200 megohms. The inactive "0" state appears as an open circuit. Each distribute point consists of an opto-isolator input diode.

**6.14 Scan and Alarm Points:** Table L summarizes the scan and alarm point states of the ABB1. On automatic power off, the MJ scan point closes and remains closed until the ACO/T switch is depressed. When power is left up in the presence of a fault, the MJ scan point remains closed until either the fault is removed (PA scan point also goes inactive) or the ACO/T switch is depressed (PA scan point remains active).

**6.15 Signal Distribute Points:** The active "1" state of the RQIP signal distribute point indicates a system software acknowledgement that a request for removal from service or restoral to service of the associated unit has been made. If the request is granted, the RQIP SD point will become inactive ("0" state). If it is denied, the RQIP SD point will intermittently flash under system control. The OOS signal distribute point becomes active when the unit has been taken out of service. The RQIP and OOS indicator lamps provide a visual indication of the state of the RQIP and OOS signal distribute points respectively. Table M summarizes the signal distribute point states.

#### POWER-UP SEQUENCE

**6.16 Start Signals:** Power up is initiated by momentarily depressing the power ON switch. Control circuitry ensures that frame power is supplied in the proper sequence via three start signals and an initialization phase. In the power-off state, the initialization circuit which starts the power-up sequence is powered from a fused -48V source through a normally open ON switch (momentary

contact). Initialization signals enable +5V frame converters which power TTL sequence circuitry and initialize power control and alarm circuitry. This allows the power switch to be inserted with -48V present without the danger of enabling frame converters until the power ON switch is pressed. Start signals STA and STB are opto-isolator outputs used to control converters associated with the power switch. Start signal STC is an open-collector relay driver which enables I/O bus power. On power up, logic power precedes memory power by approximately 1300 ms, and memory power precedes start signal by approximately 500 ms. The power-off LED is lit in the power-off state and does not extinguish until the power-up sequence is complete.

#### POWER-DOWN SEQUENCE

**6.17 Normal Power Down:** To prevent inadvertent removal of frame power, the power OFF switch (momentary contact) is interlocked with a system-granted out-of-service (OOS) signal. Depressing the power OFF switch causes no change in state of the circuit pack unless the OOS signal distribute point is active, in which case frame power is sequentially removed. On power down, the initialization signals and I/O bus power are removed approximately 500 ms before memory power is removed. The start signal is removed approximately 500 ms before logic power is removed. The power-off LED remains extinguished until the power-down sequence is complete.

**6.18 Emergency Power Down:** Craft personnel have the option of overriding the power OFF switch/OOS interlock under emergency conditions. Simultaneously depressing the power OFF and MOR (manual override) switches sequentially removes frame power as in the normal power-down case. Additionally, a separate backup timing circuit (approximately 1500 ms) will release the +5V frame power in the event the power-down sequence circuit fails. With the release of +5V power to the circuit pack, all start signals and hence all frame power controlled by the power switch will release.

#### 7. MAINTENANCE

**7.01** Each 3B CC is equipped with dedicated peripheral units, however, the IOP may be accessed by either 3B CC. If a fault is detected in the IOP, recovery action is initiated; if the recovery action fails to correct the fault, the IOP

is placed out of service. When the IOP is placed out of service, an appropriate alarm is given accompanied by a TTY printout. If the fault is detected in the 3B CC, MAS, or DMA units, a switch to the duplicated 3B CC and its dedicated periphery will be made.

**7.02** A fault in a PD connected to the IOP will result in the PD being placed out-of-service. The functions provided by the PD will be lost by the system until it is repaired or replaced.

**7.03** The maintenance provided is mainly software; the IOP uses loop-around messages to check its circuits. These loop-around messages are used when the IOP is placed in the maintenance state (start code) by the 3B CC to detect circuit faults. The IOP also implements status messages to signal the 3B CC of faults detected during normal operations.

**7.04** The IOP also uses internal software to detect internal faults (ie, the DAM in the PIC) and initiate fault recovery. Also, hardware checks are provided in the IOP for fault detection, such as start code, parity, error detection logic, and power error circuits. Additionally, the IOP is provided with clock checks for timing, sanity check circuit, and routine maintenance diagnostics.

**8. REFERENCES**

**8.01** The following documents contain information relevant to this section:

SECTION	TITLE
254-301-010	3B Central Control, Description and Theory of Operation, 3B Processor
254-301-020	Power Systems, Description and Theory of Operation, 3B Processor
254-301-100	Input/Output Interfaces, Description and Theory of Operation, 3B Processor
254-301-200	3B Main Store, Description and Theory of Operation, 3B Processor
254-391-000	3B Processor, Task Oriented Practices

SECTION	TITLE
254-341-000	Duplex Multi-Environment Real-Time Operating System, Software Subsystem Description, 3B Processor
254-341-100	Input/Output and Data Management, Software Subsystem Description, Duplex Multi-Environment Real-Time Operating System, 3B Processor.

**9. GLOSSARY**

**9.01** A glossary of terms is provided to aid in the understanding of this section.

**Asynchronous** —Functional units operate or interface without a fixed time relationship.

**Autonomous** —The device can perform its primary function without external assistance.

**Buffer** —A storage device used to compensate for a difference in the rate of flow of information or time of occurrence of events when transmitting from one device to another. Normally a register.

**Bus** —One or more conductors over which information is transmitted from any of several sources to any of several destinations.

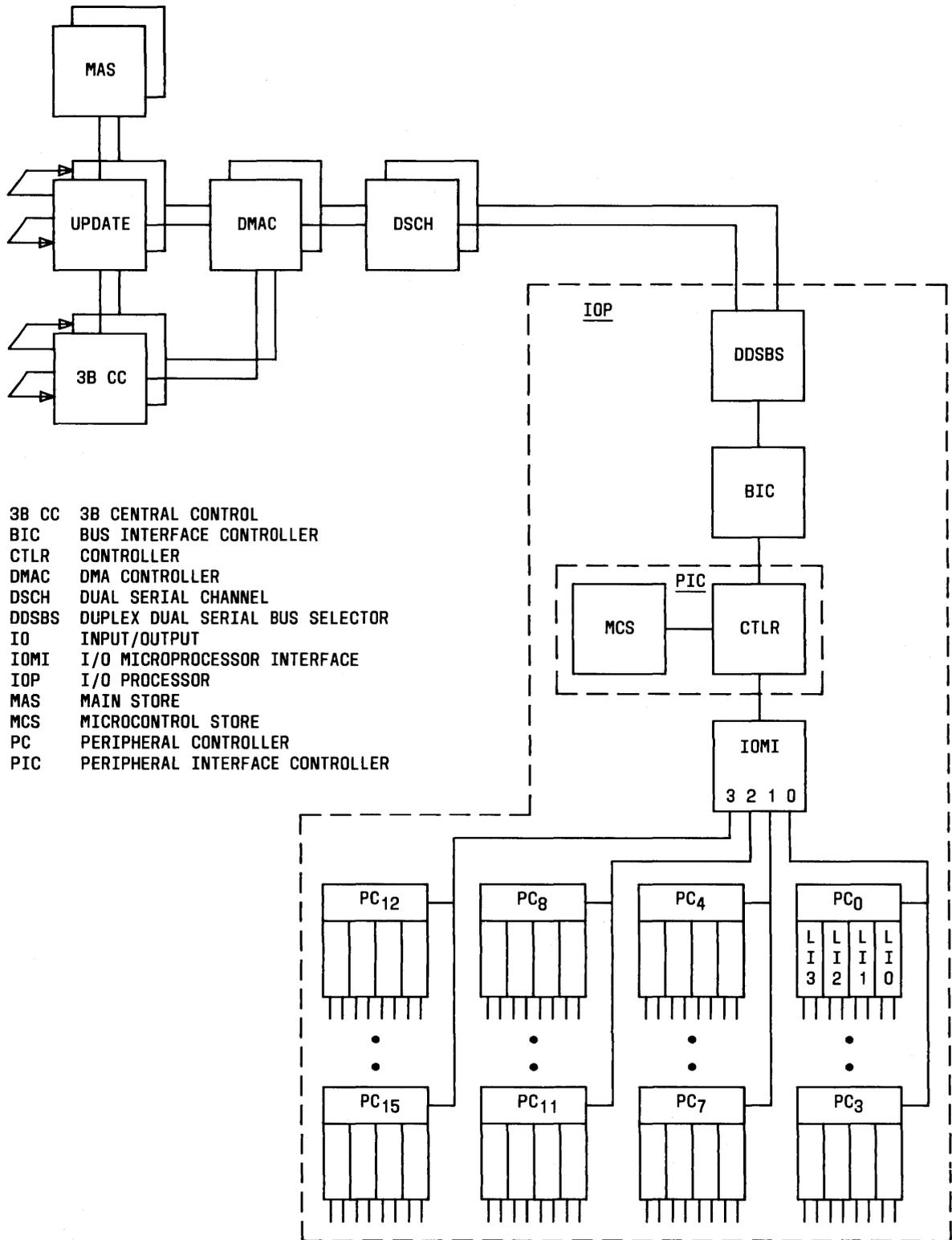
**Diagnostic** —A program which functions to isolate a fault within the unit under test.

**Flip-Flop** —A device capable of assuming two stable states (set or clear), thereby storing a bit of information. It remains in either state until a signal changes it to the other state.

**Gate** —A circuit which has the ability to produce an output dependent upon specified type or the coincident nature of the input(s).

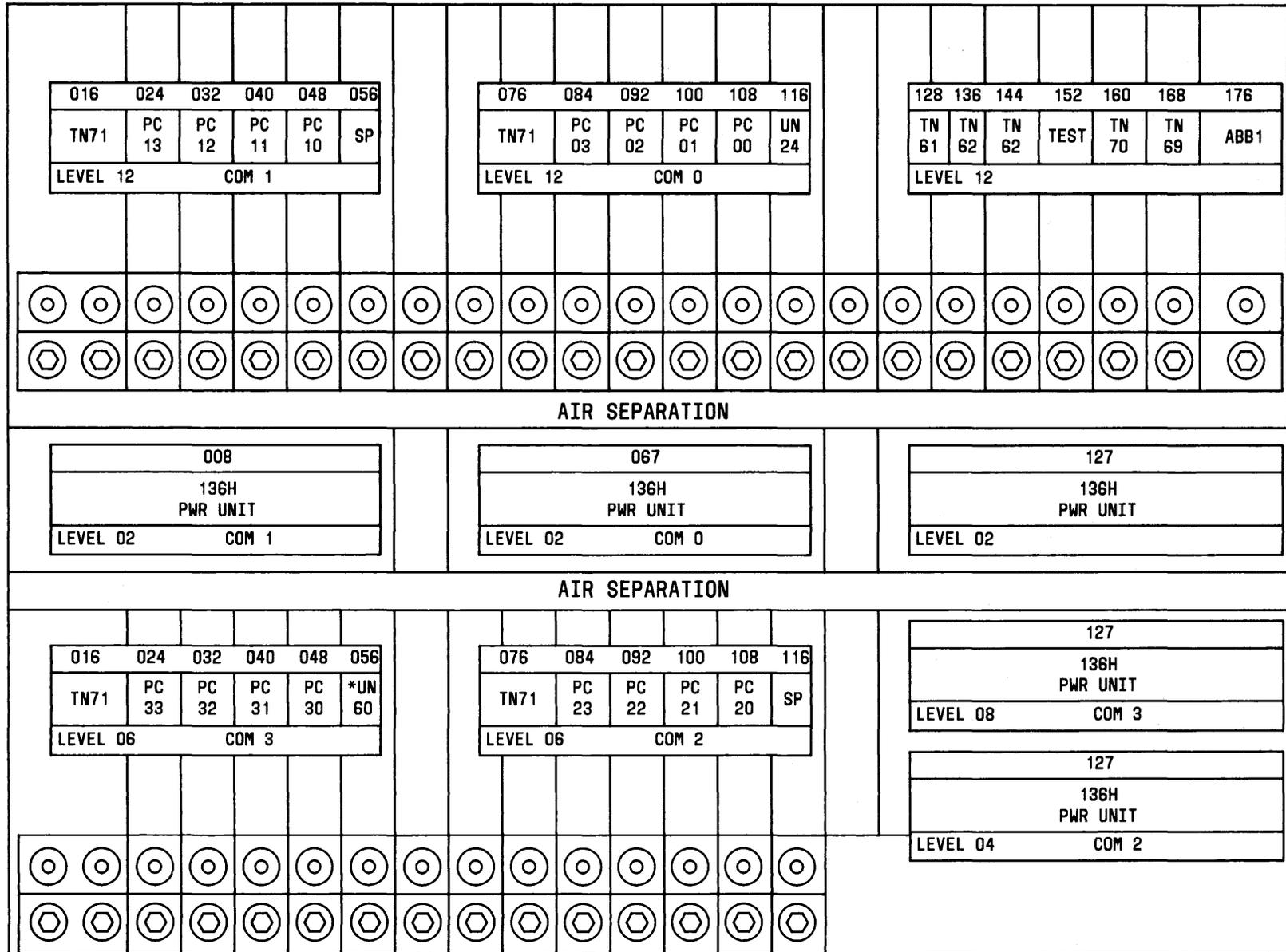
**Interrupt** —A signal generated by a device to notify the 3B CC that the device requires attention.

**Interrupt Vectoring** —A method whereby the identity (ie, address) of an interrupting device is provided automatically to the processor along with the device interrupt signal.



3B CC 3B CENTRAL CONTROL  
 BIC BUS INTERFACE CONTROLLER  
 CTLR CONTROLLER  
 DMAC DMA CONTROLLER  
 DSCH DUAL SERIAL CHANNEL  
 DDSBS DUPLEX DUAL SERIAL BUS SELECTOR  
 IO INPUT/OUTPUT  
 IOMI I/O MICROPROCESSOR INTERFACE  
 IOP I/O PROCESSOR  
 MAS MAIN STORE  
 MCS MICROCONTROL STORE  
 PC PERIPHERAL CONTROLLER  
 PIC PERIPHERAL INTERFACE CONTROLLER

Fig. 1—IOP Configuration



\* USED ONLY WITH 1A PROCESSOR

Fig. 2—IOP Unit

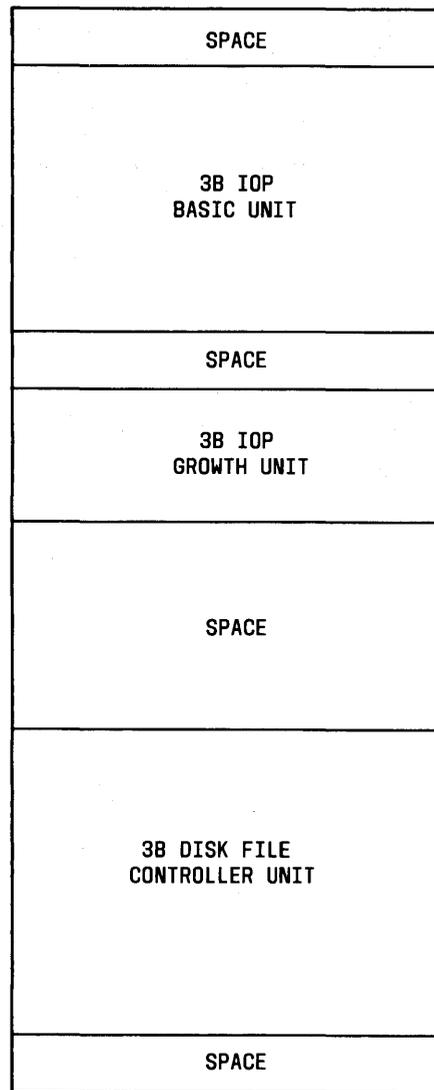


Fig. 3—Peripheral Control Frame

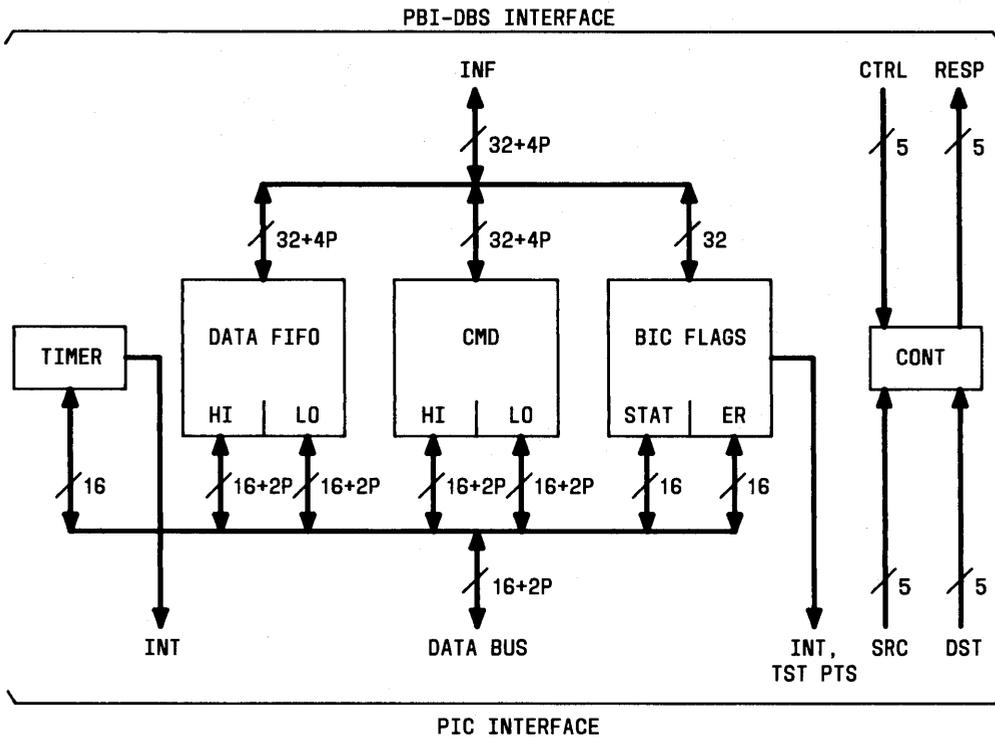


Fig. 4—Bus Interface Controller

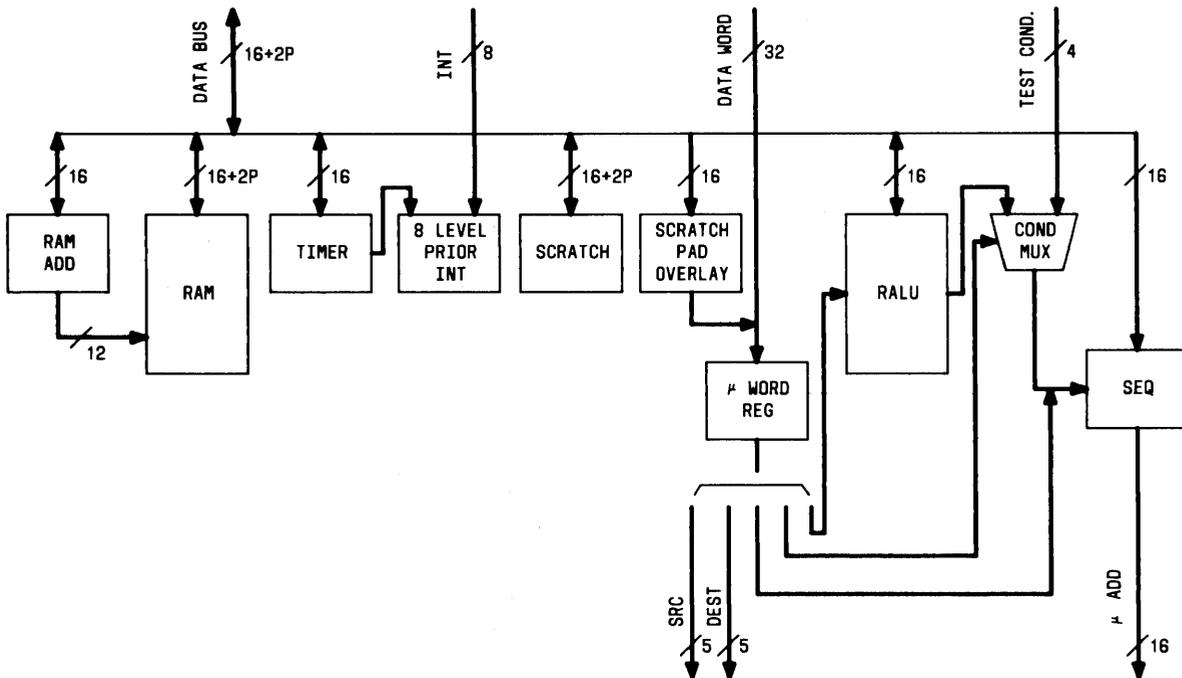


Fig. 5—Peripheral Interface Controller (Controller)

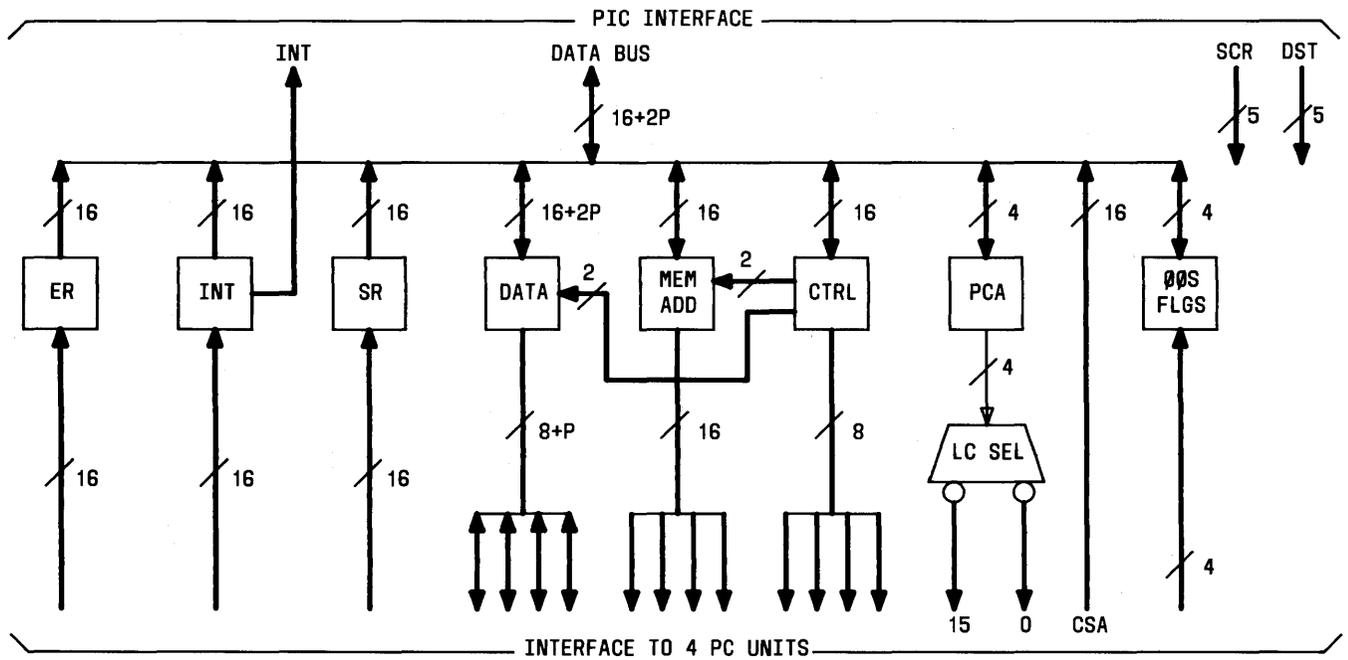


Fig. 6—Input/Output Microprocessor Interface

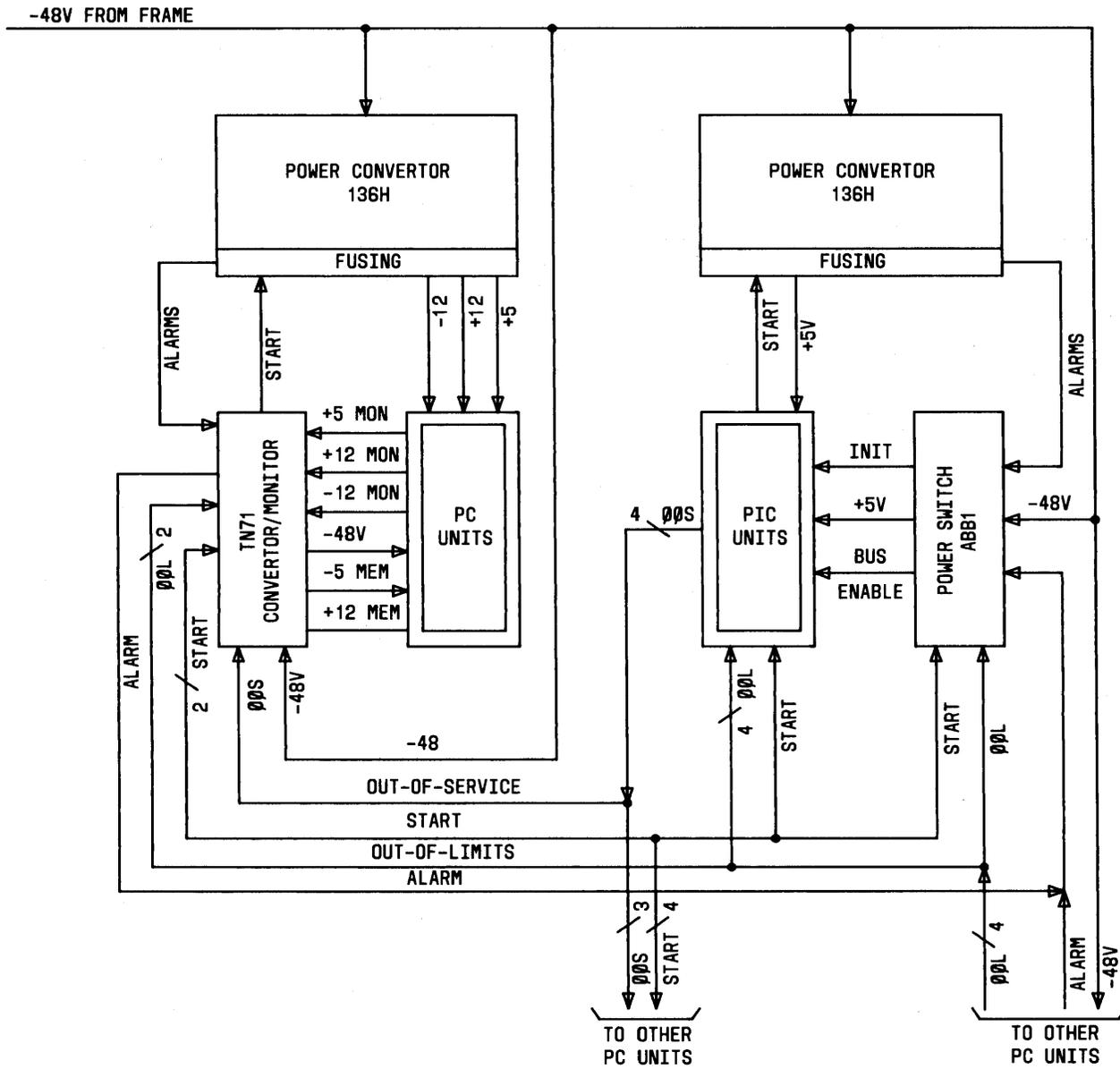


Fig. 7—3B IOP Power Functional Block Diagram

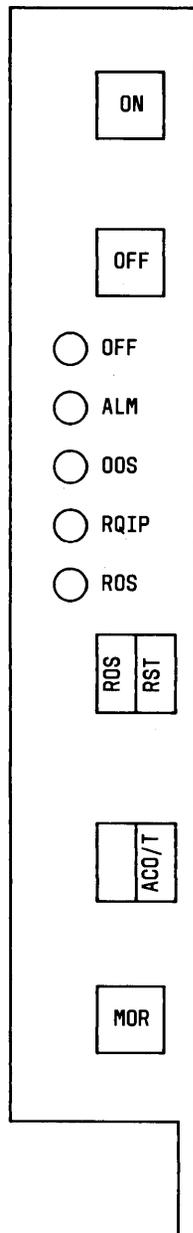


Fig. 8—ABB1 Front Panel

TABLE A  
START CODES

HI	LO	OPERATION
0011	0011	Write data (word mode)
0011	0101	Send device command
0011	1001	Write data (block mode)
0101	0011	Read data (word mode)
0101	0101	Sense status
0101	1001	Read data (block mode)
1001	0011	End-of-transfer (EOT)

TABLE B  
RETURN CODES

HI	LO	SPECIFIES
0011	0011	All seems well
0011	0101	Device reported error
0101	0011	Invalid DDSBS command
0101	0101	Illegal start code received

TABLE C  
BIC COMMAND LAYOUT

INF BIT	FUNCTION
0—2	000
3	Set DMA XFER request
4	Set DMA setup request
5	Set end of data expected
6	Clear command in progress
7	Set interrupt
8	Reset interrupt
9	Set word transfer mode
10	Set block transfer mode
11	Set interface enable
12	Clear data FIFO
13	Clear BIC
14	Reset PIC
15—31	Spare

TABLE D  
BIC STATUS WORD LAYOUT

INF BIT	FUNCTION
0—3	Device address
4	DMA setup over write error
5	INF parity failure over byte 0 (most significant)
6	INF parity failure over byte 1
7	INF parity failure over byte 2
8	INF parity failure over byte 3 (least significant)
9	End-of-data error
10	PIC fatal error summary
11	PIC sanity error
12	PIC data bus parity error — low byte
13	PIC data bus parity error — high byte
14	PIC data FIFO overflow
15	PIC command register overflow
16—20	Data FIFO word count
21	Interrupt
22	DMA XFER request
23	DMA setup request
24	End of data expected
25	End of data received
26	Data transfer mode (0-word, 1-block)
27	Enable PIC data bus parity checks
28	PIC interface enabled
29	Data flag
30	Command in progress
31	Command flag

TABLE E  
BIC BIT FIELD LAYOUTS

BIC STATUS FLAGS – SOURCE 8	
DB BIT	FUNCTION
0–4	Data buffer word count
5	Interrupt request
6	DMA XFER request
7	DMA setup request
8	End of data expected
9	End of data received
10	Data transfer mode (0-word, 1-block)
11	Enable PIC data bus parity checks
12	PIC interface enabled
13	Data flag
14	Command in progress
15	Command flag
BIC ERROR FLAGS – SOURCE 9	
DB BIT	FUNCTION
0–1	Unused (0)
2	PIC data bus parity error – low byte
3	PIC data bus parity error – high byte
4	PIC data buffer overflow
5	PIC command register overflow
6	PIC sanity error
7	INF parity error – byte 0
8	INF parity error – byte 1
9	INF parity error – byte 2
10	INF parity error – byte 3
11	3B DMA setup overwrite
12	End-of-data error
13	PIC soft error summary
14	PIC fatal error summary
15	3B error summary

TABLE F  
PIC WRITE FLAGS OPERATION – DESTINATION 8

DB BIT	FUNCTION
0	Set DMA XFER request
1	Set DMA setup request
2	Set interrupt
3	Clear end of data expected and end of data received
5–6	Set word/block transfer mode
7	Set/reset data bus parity checks enable
8	Set PIC fatal error flag
9	Clear PIC soft errors
10	Clear data FIFO
11	Toggle data flag
12–13	Set/reset command in progress

TABLE G  
PIC TO BIC ENTITIES

SOURCE	DESTINATION	FUNCTION
8	8	BIC status flags
9	—	BIC error flags
10	10	Command high
11	11	Command low
12	12	Data high
13	13	Data low
14	14	Data low, set XFER
15	15	Timer

TABLE H  
INTERRUPT JUMP TABLE

LOCATION	MICRODATA WORD
3F0	Jump to normal interrupt subroutine for INT. 0
3F1	Jump to normal interrupt subroutine for INT. 1
3F2	Jump to normal interrupt subroutine for INT. 2
3F3	Jump to normal interrupt subroutine for INT. 3
3F4	Jump to normal interrupt subroutine for INT. 4
3F5	Jump to normal interrupt subroutine for INT. 5
3F6	Jump to normal interrupt subroutine for INT. 6
3F7	Jump to normal interrupt subroutine for INT. 7
3F8	Jump to maintenance interrupt subroutine for INT. 0
3F9	Jump to maintenance interrupt subroutine for INT. 1
3FA	Jump to maintenance interrupt subroutine for INT. 2
3FB	Jump to maintenance interrupt subroutine for INT. 3
3FC	Jump to maintenance interrupt subroutine for INT. 4
3FD	Jump to maintenance interrupt subroutine for INT. 5
3FE	Jump to maintenance interrupt subroutine for INT. 6
3FF	Jump to maintenance interrupt subroutine for INT. 7

TABLE I  
IOP SOURCE AND DESTINATION CODES

SRC	DST	REGISTER	CIRCUIT
0	0	RAM Address	PIC CONTROLLER
1	1	Instruction counter	PIC CONTROLLER
2	2	Interrupt	PIC CONTROLLER
3	—	Immediate data	PIC CONTROLLER
—	3	Sequencer macro register	PIC CONTROLLER
4	4	Scratch register	PIC CONTROLLER
5	5	RAM	PIC CONTROLLER
—	6	Scratch pad overlay	PIC CONTROLLER
7	—	ALU	PIC CONTROLLER
—	7	Sequencer	PIC CONTROLLER
8	8	BIC status flags	BIC
9	—	BIC error flags	BIC
10	10	Command high	BIC
11	11	Command low	BIC
12	12	Data high	BIC
13	13	Data low	BIC
14	14	Data low (also sets XFER)	BIC
15	15	Sanity and interval timer	BIC
16	—	Control signal acknowledge	IOMI
17	—	Service request register	IOMI
18	—	Interrupt register	IOMI
19	—	IOMI error register	IOMI
20	20	IOMI data register	IOMI
21	21	PC memory address register	IOMI
22	22	Control register	IOMI
23	23	PC address register	IOMI
24	23	PC community out-of-service flags	IOMI
—	25	Clear error register	IOMI
23	26	Maintenance register	IOMI

TABLE J

## CONTROL SIGNAL REGISTER BITS

BIT	FUNCTION
0	CLR0 — clear PC
1	RISL80 — reset PC isolate flip-flop
2	SISL80 — set PC isolate flip-flop
3	CINT0 — command interrupt (PIC->PC)
4	DMAWR0 — DMA memory write
5	DMARD0 — DMA memory read
6	DMAOC0 — DMA operation complete
7	DMARQ0 — DMA request
8—9	Memory address register mode 00 autoincrement 01 autodecrement 1X hold present contents
12	DRVDAT0 — enable data to be gated on PC community buses
13	Force high data byte to be selected
14	Force low data byte to be selected
15	Toggle data byte selector

TABLE K

## IOMI SOURCE AND DESTINATION CODES

SRC	DST	FUNCTION
16	—	Control signal acknowledge
17	—	Service request register
18	—	Interrupt register
19	—	Error register
20	20	Data register
21	21	Memory address register
22	22	Control register
23	23	PC address register
24	23	PC community out-of-service flags
—	25	Clear error register
23	26	Maintenance register

TABLE L

## SCAN AND ALARM POINT STATES

CONDITION	BPP	SCX	SCY	MJ	PA
Normal in service	1	0	0	0	0
Request out of service	1	1	0	0	0
Manual power off	0	1	1	0	0
Automatic power off	0	1	1	1	0
Power up with major fault present	1/0	0	1	1	1
Power up with minor fault present (such as supply out of tolerance)	1	0	1	0	1

TABLE M

## SIGNAL DISTRIBUTE POINT STATES

CONDITION	RQIP	OS
Normal in service	0	0
Removal from service or restoral to service requested with disposition pending	1	0
Request denied	FLASH	0
Diagnostic failure after a restore-to-service request	FLASH	0
System grants out-of-service request	0	1