TELETYPEWRITER AND TELETYPEWRITER CONTROLLER DESCRIPTION AND THEORY OF OPERATION COMMON SYSTEMS

CONTENTS PAGE

Figures

1. GENERAL

1.01 This section contains the physical and functional description and theory of operation of the teletypewriter and the teletypewriter controller provided with the 3A Processor common systems.

1.02 When this section is reissued, the reason for reissue will be listed in this paragraph.

1.03 The terms ***local*** and ***remote*** are used throughout this section. Both terms refer to location in relationship to the office in which the TTY facility is installed. Local refers to a location within the office. Remote refers to a location beyond the immediate vicinity or outside the office.

1.04 Teletypewriter (TTY) facilities refer to the TTY controller (TTYC) units and the TTY devices. These facilities provide the primary means of communication between operating personnel and the system. Operating personnel may request, via TTY input messages, specific actions to be performed (or reported) by the system. The system sends replies, via TTY output messages, along with information or reports such as periodic printouts of system status and error conditions.

1.05 When the office is attended, operating personnel use the local TTY device to monitor or control system actions. When unattended, remote maintenance capability is provided to personnel at a switching control center (SCC). A remote TTY device provides the same TTY functions to operating personnel at the SCC as those provided by the local TTY in the office.

2. PHYSICAL DESCRIPTION

2.01 Normally, one TTY and its associated TTYC are located in the lower half of the maintenance frame (Fig. 1). Space is provided in the maintenance frame for two TTYC units. Additional TTYs and TTYC units may be connected depending upon equipment requirements of the system.

TELETYPEWRITER AND ASSOCIATED EQUIPMENT

2.02 Most offices may use either a current loop-type or an Electronic Industries Association (EIA) voltage signal TTY. A 33- or 35-type keyboard send-receive TTY (current loop) is located in the midsection of the maintenance frame and occupies approximately 16 inches of vertical frame space.

2.03 The TTYs have a four-row keyboard similar to the standard office typewriter. The TTYs operate at ten characters per second and receive and/or transmit information by means of an 11-bit binary message (Fig. 2). This message contains three synchronizing bits (one start bit and two stop bits) and an 8-bit code (seven data bits and one parity bit). The 8-bit code is based on the American Standard Code for Information Interchange (ASCII) approved by the American Standards Association. The seven data bits of the 8-bit code provide 128 code combinations. Of these combinations, 64 are assigned to letters of the alphabet, numbers, and symbols; 35 are used for control purposes. The remaining 29 combinations are unassigned.

2.04 A TTY may be equipped with a stunt box which decodes certain TTY characters to operate or release a set of contacts. These contacts are used to activate auxiliary equipment (eg, an alarm).

2.05 A TTY may also be provided with an idle line control unit, which enables TTY motor control to be performed automatically by the program. The idle line control unit responds to the first character received by turning on the motor.

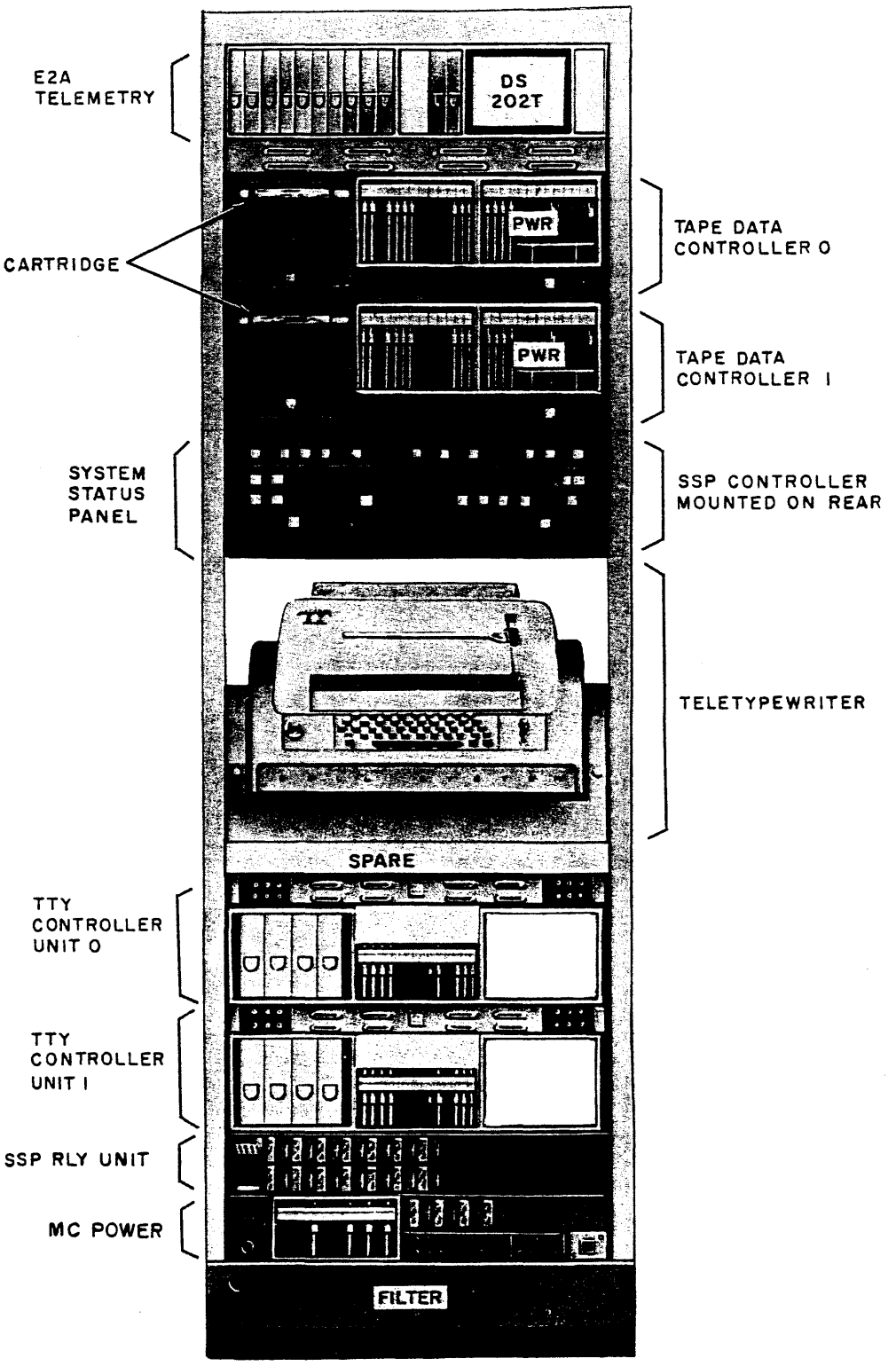

Fig. 1—Typical Maintenance Frame

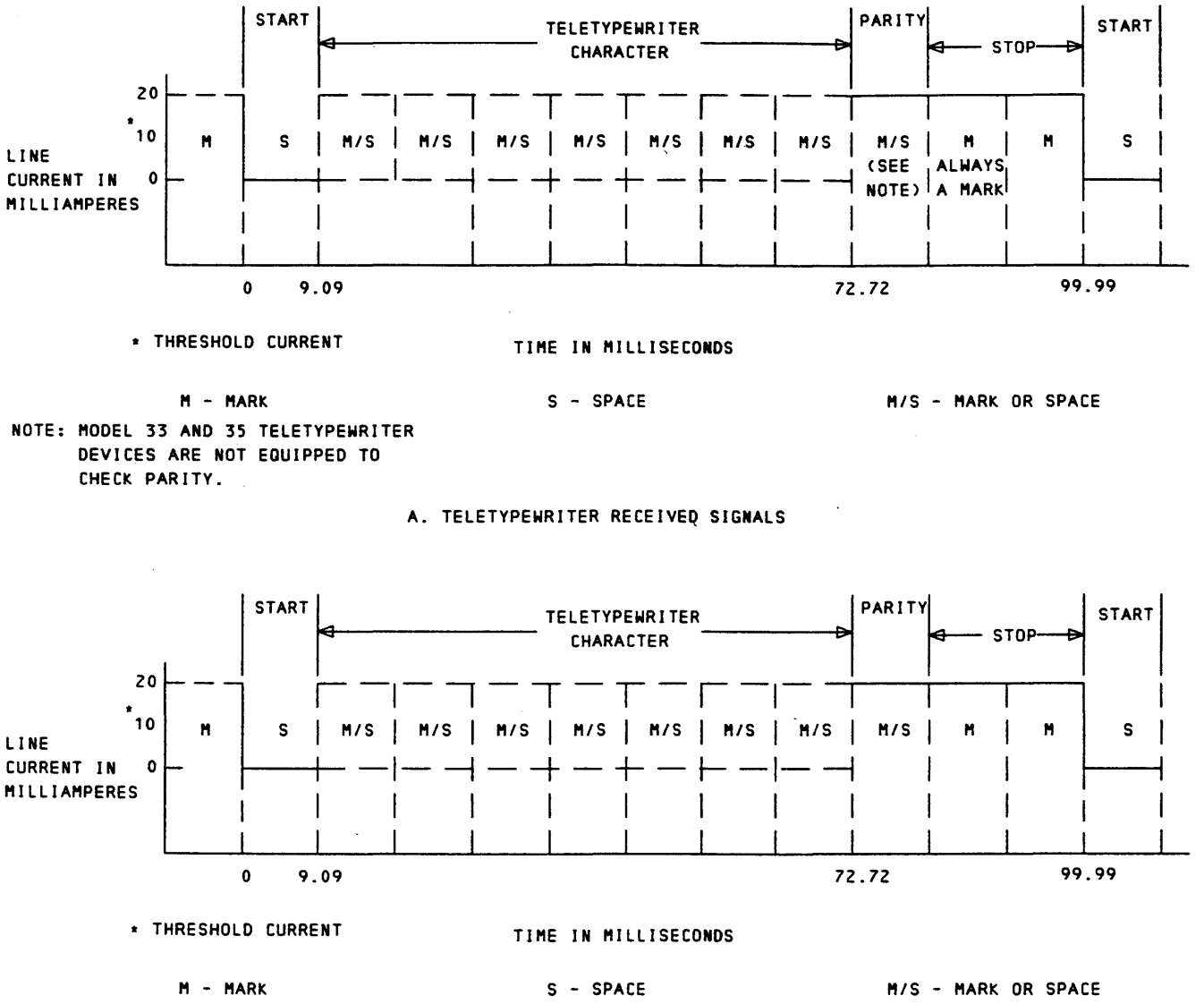

Fig. 2—Teletypewriter Signal Format

The unit will automatically turn off the motor if no data is received within a predetermined period of time. The time adjustment is made at the idle line control unit as a user option.

2.06 A paper-tape punch (reperforator) may be included with the TTYs as a method of providing a coded, eight-level punched paper-tape copy of information entered on the TTY keyboard or received by the TTY. This punched tape may be used as backup for information entered into the system and as a record of information to be entered into the system at a later time.

2.07 A paper-tape reader (transmitter-distributor) may be included with the TTY. This reader provides a means to input the contents of the paper tape into the system.

TELETYPEWRITER CONTROLLER

2.08 Each TTYC unit (Fig. 3) provides space to equip (except for power) two independent

TTY channels (four ports are referred to as one TTY channel). Channel assignments are dependent upon the system requirements and may be designated for specific functions, such as maintenance channel.

2.09 An 8-inch mounting plate accommodates two 58C apparatus mountings, one 80C apparatus mounting, and a connector plate assembly.

2.10 A 58C apparatus mounting is installed on each end of the 8-inch mounting plate. Each 58C mounting provides space for a maximum of four 108D data sets or four AR17 port interface circuit packs or any combination of the two. See 2.15 through 2.18 for functions of the 108D data set and the AR17 circuit pack.

2.11 An 80C apparatus mounting is inserted between the two 58C apparatus mountings. This 80C mounting provides space for the controller logic of two TTY channels (three circuit packs per channel, FA1058, FA1059, and FC200), one dc-to-dc converter (J87389F, +3 volts), the -24 volt regulator circuit pack (FB494), the +3 volt power reference and filter circuit pack (FC21), and the +12 volt power reference circuit pack (FB152).

2.12 Directly above the three apparatus mountings is a connector plate assembly. This assembly provides the connectors required to interface the TTYC unit with the 3A Central Controls (3A CCs) and the TTYs. Six coaxial connectors are mounted on each end of the plate to provide the three inputs/outputs (R and S for input/output subchannel; I for demand interrupt lead) per TTY channel from each 3A CC. Eight 25-terminal line connectors provide the means for connecting or interfacing with local and/or remote TTYs. A TTYC POWER switch lamp is mounted in the center of the plate assembly and is used to control the -48 volt and +24 volt input power.

INTERFACES

2.13 The TTYC is a transmit/receive buffer between the TTY and 3A CC. Six coaxial

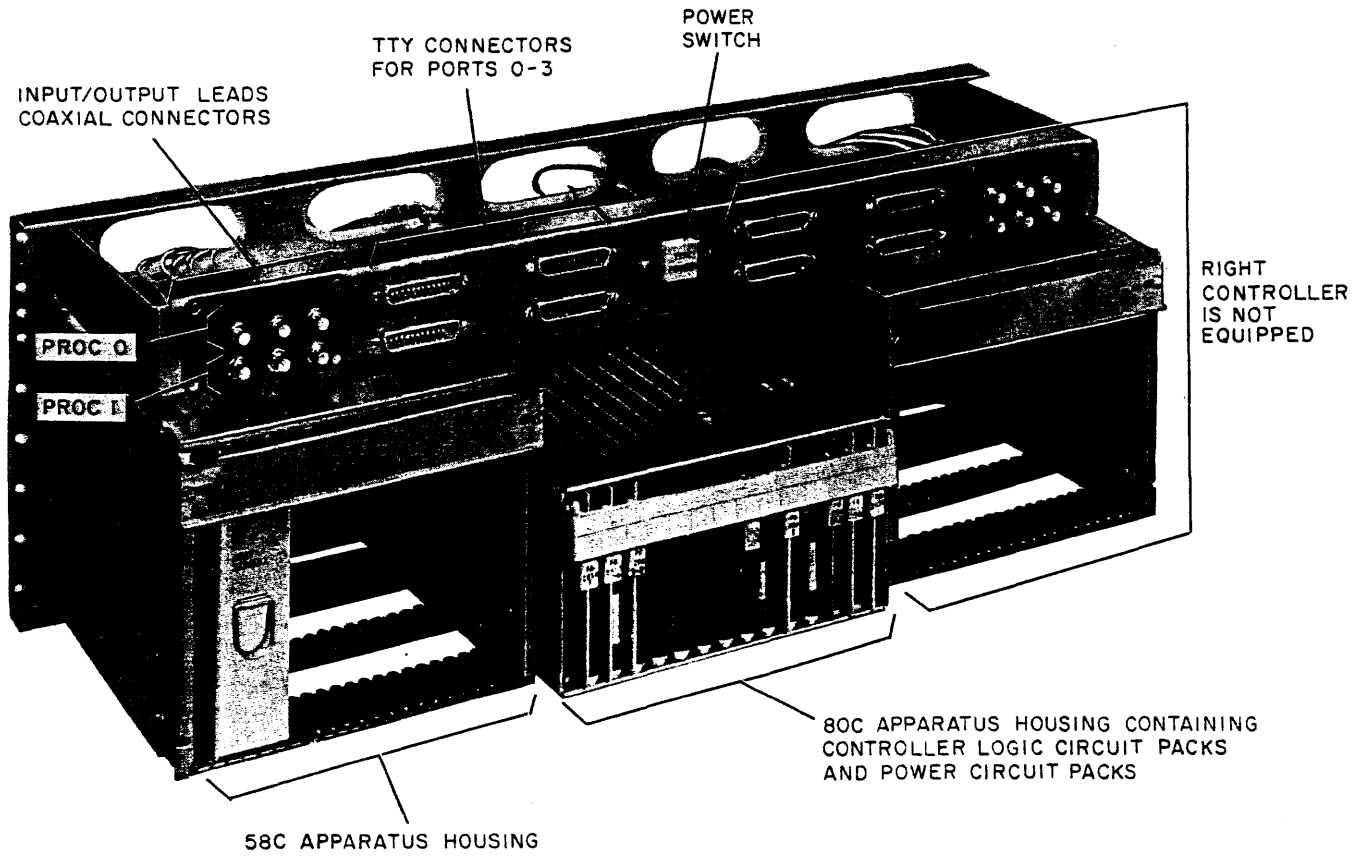

Fig. 3—Teletypewriter Controller

cables connect each TTYC to the 3A CCs (0 and 1). These cables provide the three input/output leads (R, receive input; S, transmit output; and I, demand interrupt output) per TTY channel from each 3A CC (Fig. 4 and 5). The TTYs are connected by cable to the TTYC at one of the eight 25-terminal line connectors.

2.14 Each TTYC can serve a maximum of four ports, each of which may access either a local or remote TTY. With the appropriate apparatus, each port can accommodate an EIA signal or current loop TTY for either local or remote operation. If a local EIA signal TTY is installed to a port line connector, no circuit pack is inserted in the corresponding port location. The EIA signals appear directly at the line connector to which the EIA device is connected. When a local current loop TTY is installed to a port line connector, an AR17 circuit pack is inserted into the corresponding port location. When the TTY is a remote device, the 108D data set is inserted into the corresponding port location. If the port is unassigned, no circuit pack is inserted into the corresponding port location (Fig. 4). In some installations, No. 2B ESS for example, the TTY interrupts are on a scheduled basis, rather than on demand. In these cases, the I connections to the TTY and TTYC are not used.

OPTIONS

2.15 The following options may be supplied with the TTY facilities:

(a) ***Local EIA:*** No circuit pack is equipped in the optional circuit pack connector.

(b) ***Local Current Loop:*** A three-wire current loop is employed with a common source and a separate send and receive lead. An AR17 circuit pack is equipped in the optional circuit pack position to perform EIA-to-current loop conversion.

(c) ***Remote Operation:*** A 108D data set is equipped in the optional circuit pack connector for remote operation.

(d) ***Autoconnect Facility.***

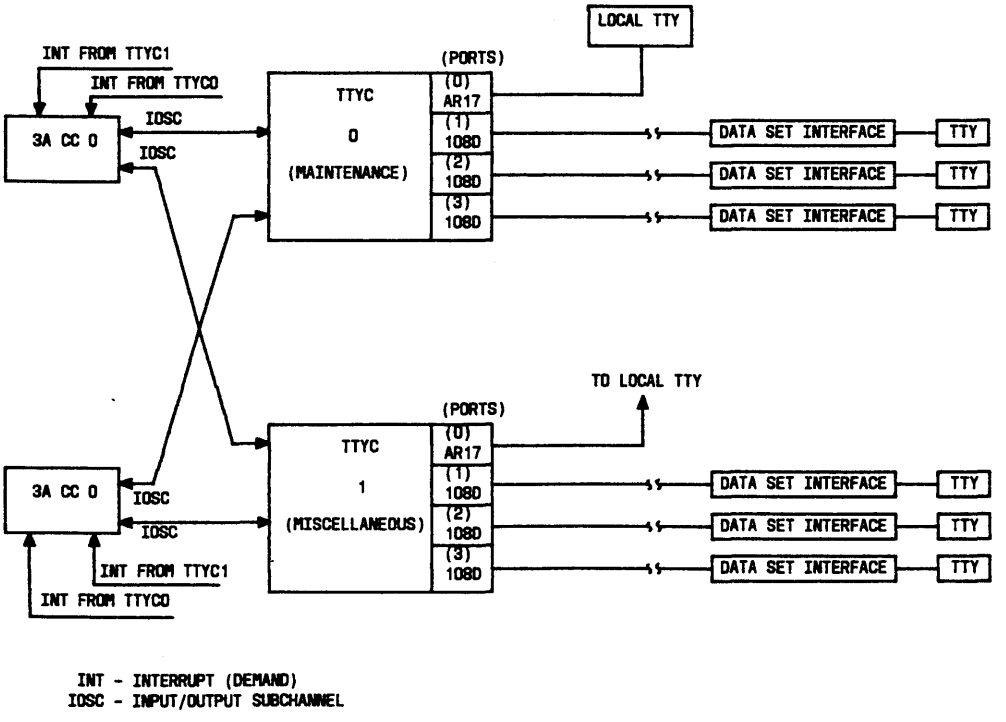

Fig. 4—Typical System—Block Diagram, Showing TTY Interfaces

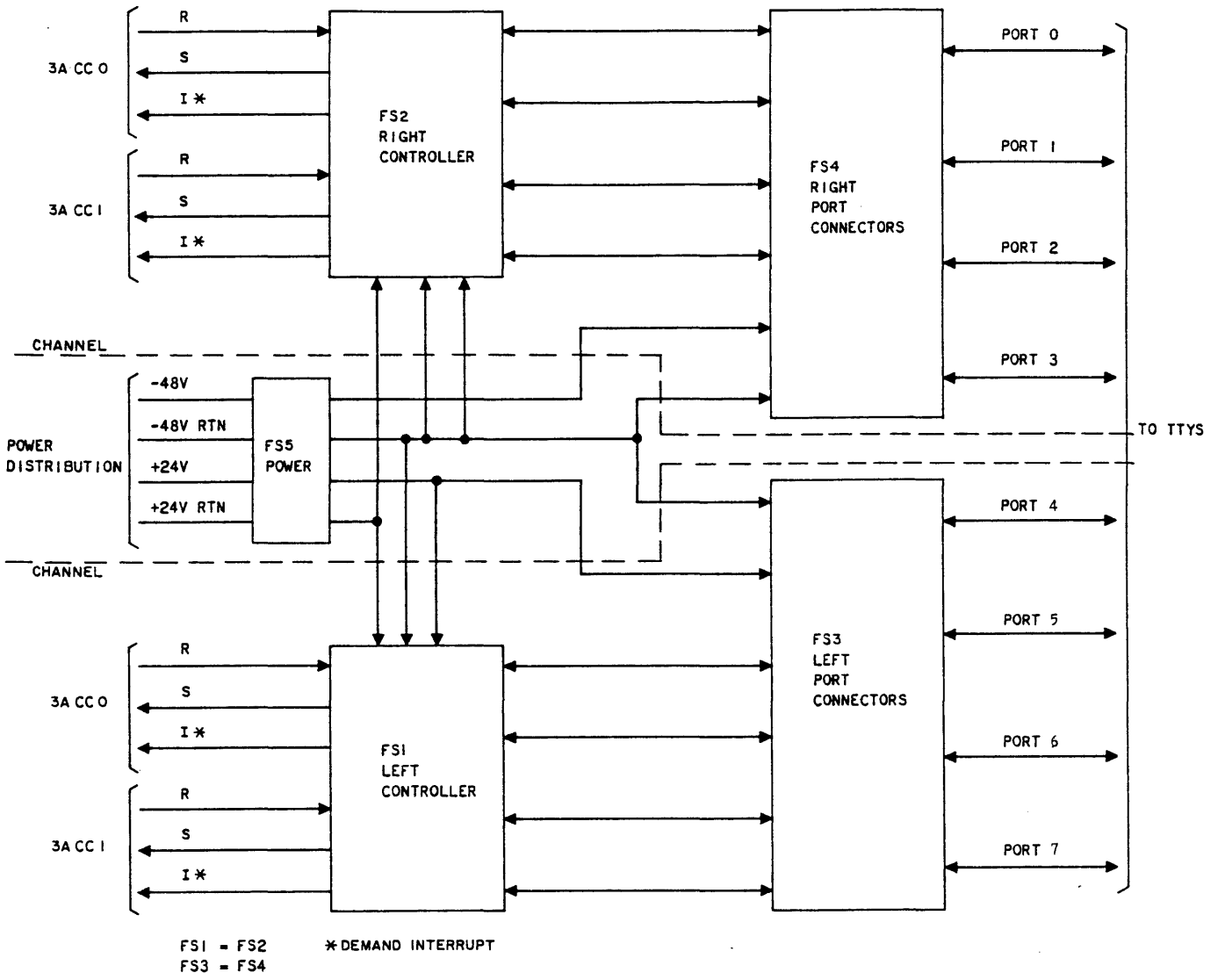

Fig. 5—TTYC (FS)—Block Diagram

2.16 ***Local EIA:*** A circuit pack is not required in the optional circuit pack connector as an interface to an EIA TTY.

2.17 ***Local Current Loop:*** An AR17 circuit pack is required in the optional circuit pack connector as an interface to a current loop TTY. The AR17 circuit pack not only converts the EIA signals from the TTYC logic to current signals for the TTY but also converts the current signals from the TTY to EIA signals for TTYC logic.

2.18 ***Remote Operation:*** A 108D data set is required in the optional circuit pack position for interfacing to a remote TTY. The 108D data set converts the EIA signals from the TTYC logic to frequency shift data for transmission to a remote location and also converts the frequency shift data received from a remote location TTY to EIA signals for the TTYC logic.

2.19 ***Autoconnect Facility:*** The autoconnect facility provides a means for establishing dial-up connections to TTY channels to handle remote TTY functions. This minimizes the need for using trunks to perform remote TTY functions.

2.20 To provide autoconnect for a remote office, the data set of the remote TTY is connected to a data coupler. The use of a data coupler in

connection with a standard data telephone set provides manual answering and call origination features. The standard data telephone set is equipped with an exclusion feature to be used to switch between voice and data modes. The exclusion feature is wired so that the coupler set is on-line in the voice mode and the data telephone set is on-line in the data mode.

3. FUNCTIONAL DESCRIPTION

TELETYPEWRITER CHANNELS

3.01 As indicated in 2.08, the various TTY channels may be assigned specific functions. The following two functions are presented as examples:

(a) Maintenance teletype channel

(b) Miscellaneous teletypewriter channel.

A. Maintenance Teletypewriter Channel

3.02 The maintenance TTY channel is the basic communication link between the office and the operating personnel at the SCC. Input messages from the SCC are normally requests for specific diagnostic tests or special reports on internal conditions. The output message to the SCC consist of alarm status conditions, trouble indications, results of trouble diagnostics, and replies to interrogation requests.

3.03 When an office is designed to operate as an unattended office, the maintenance of the office will be the primary responsibilty of a remote location (SCC). Both the local and remote maintenance TTYs receive the same messages from the system.

B. Miscellaneous Teletypewriter Channel

3.04 The miscellaneous TTY channel serves as the backup for the maintenance channel and is capable of performing the same functions as the maintenance channel. When malfunctions occur in the maintenance TTY channel (TTYC 0), the 3A CC detects the malfunction, switches the miscellaneous TTY channel (TTYC 1) to the active state, and prints a maintenance message on the maintenance TTY.

CONTROLLER LOGIC OF A TELETYPEWRITER CHANNEL

3.05 A block diagram of TTY channels is shown in Fig. 4. Each TTY channel provides controller logic, four ports, and from one to four TTYs, depending upon port assignments. A TTY channel is connected to each 3A CC via an input/output subchannel and a demand interrupt control lead. There are two types of interrupts available: demand interrupt which requires an interrupt lead and scheduled interrupt which does not require an interrupt lead. When scheduled interrupt is used, the interrupt is 3A CC initiated on a predetermined time interval. However, most TTYs function with the 3A CC on a demand (rather than scheduled) interrupt basis. A demand interrupt is activated to the 3A CC at the end of the last bit for both input and output characters. The normal response of the 3A CC to a TTY interrupt is to poll the controller with a control message. This allows the controller logic of a TTY channel to return the character just received, or sent, or to return a status message.

3.06 The controller logic is the transmit/receive means between 3A CCs and TTYs on a TTY channel. The controller logic enables character transmission from the 3A CC to the TTY and from the TTY to the 3A CC. The controller logic contains channel and line circuits (Fig. 6). Channel circuits contain the buffer, control, and interface between the 3A CC and line circuits. Line circuits contain the buffer, control, and interface between the TTY ports and channel circuits. Within the channel circuits is the line status buffer, which contains four enable bits and four alarm bits. Enable bits determine the selection of the port and TTY to receive a character from the 3A CC. Normally, all four ports are enabled, but this is a function of the TTY programs. Alarm bits of the buffer give a trouble indication for each TTY device connected in the TTY channel.

3.07 Each one of the four ports may access either a local or remote TTY (option of the operating company). However, only one TTY (regardless of whether it is local or remote) is used per port.

3.08 TTY output information can be distributed to each port independently or to any combination of ports, including all four in parallel. Although the TTYs may receive messages simultaneously, they cannot transmit messages to the controller logic at the same time. Basically,

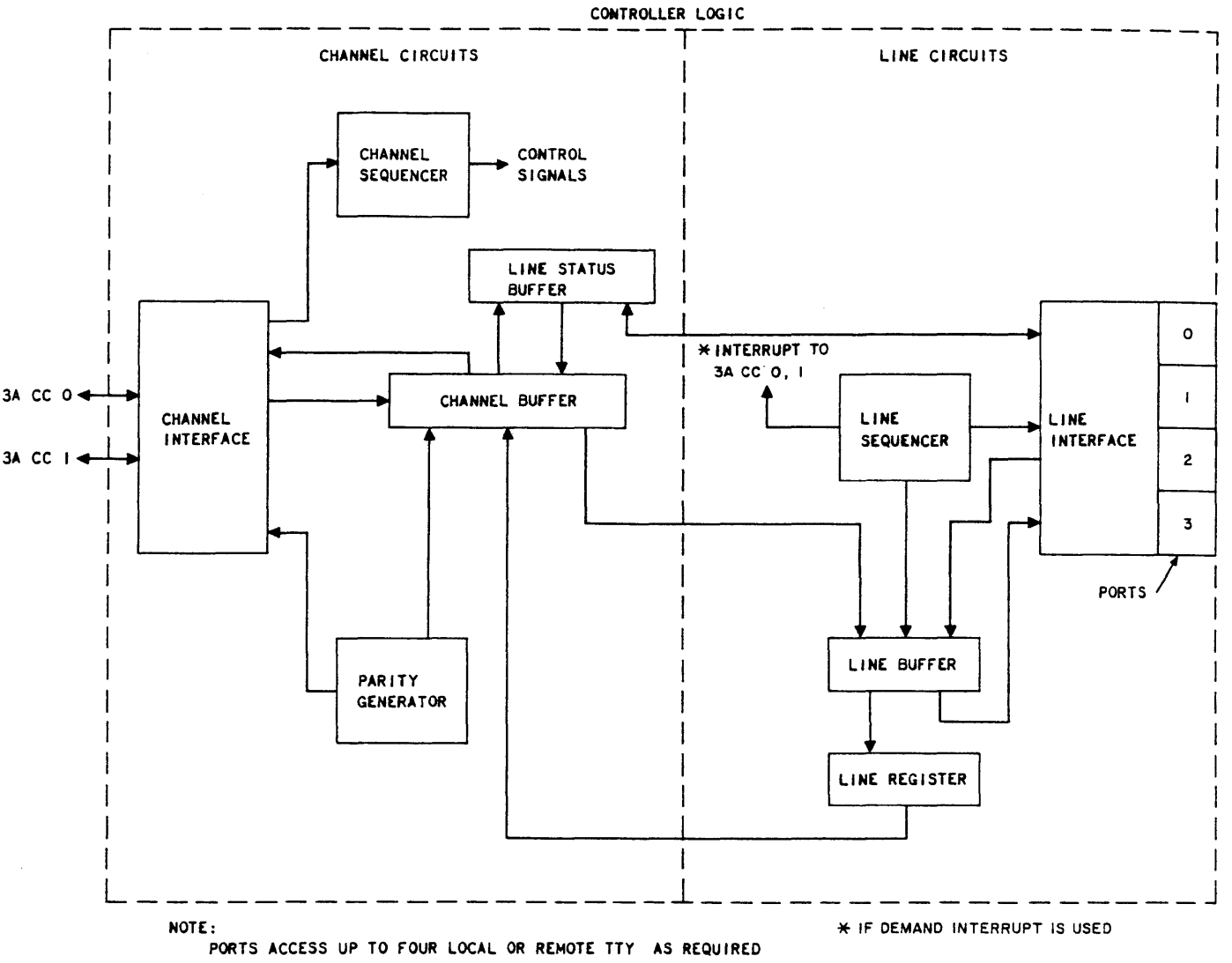

Fig. 6—Teletypewriter Controller Logic—Block Diagram

the TTY that requests service first should be given service first. However, when more than one TTY tries to transmit characters to the controller logic at the same time, the message is garbled, and the appropriate response is given at the TTY.

4. THEORY OF OPERATION

INTRODUCTION

A. Teletypewriter

4.01 The communication between the 3A CC and the TTY is serial in nature, consisting of an 11-bit binary message and 10 zeros which make up the 21-bit serial bipolar pulse messages. The TTYs receive and transmit a character or function by means of an 11-bit binary message (Fig. 2). This 11-bit transmission pattern contains 7 data bits, 1 parity bit, and 3 synchronizing bits (1 start and 2 stop bits). The first transmit or receive sequence bit is always a space (0) called the start bit. The next 7 bits are the ASCII code bits which define the desired letter, number, symbol, or function. These bits are followed by the parity bit. (The rightmost bit of the binary code is the first code bit.) The entire 8-bit character is passed to the 3A CC application program. Eight bits are also sent to the TTYs even if they do not check parity. The last 2 bits of the 11-bit message are the stop bits and are always marks (1). Since a character (11 bits) is transmitted in 100 milliseconds,

each bit is approximately 9.09 milliseconds in duration.

4.02 Descriptions and detailed operations of the TTYs are given in the following Bell System Practices:

(a) Section 574-100-101—The 33-Type TTY Sets

(b) Section 574-201-100—The 35-Type TTY (RO and KSR) Sets

(c) Section 574-202-100—The 35-Type TTY (ASR) Set.

B. Teletypewriter Controller

4.03 The TTYC consists of the following functional circuits:

(a) Channel circuits, which provide buffer and interface between the 3A CC and TTYC line circuits to the TTY. The channel circuits also contain a line status buffer which selects the port and TTY that will receive a character from the 3A CC.

(b) Line circuits, which provide the buffer and interface between the TTYs and the TTYC (channel circuits to the 3A CC).

States of the channel and line circuits are as follows:

Channel	Line
—	Rest
Receive	Transmit
Process	Hit
Transmit	Receive

4.04 There are two basic types of data messages transmitted between the 3A CC, TTYC, and TTYs—character and status. The normal start code is always used with the character message while the status message uses the maintenance start code (Fig. 7).

COMMUNICATION

A. 3A CC to TTYC to TTY

4.05 The channel circuits are initially in the receive state. When the 21-bit serial bipolar message starts coming into the TTYC (via input/output subchannel), the channel circuits are in the receive state. The first 15 bits (3-bit start code, 1 parity bit, 8 data bits, and 3 zero bits) are loaded in the channel buffer (for code, see Fig. 7). The remaining bits (all zeros) are counted and used for shifting and gating. After loading the data, the channel circuits are switched into the process state. The channel sequencer examines the contents of the channel buffer to determine whether it is message data or control information. Parity is also checked (odd parity). The channel circuits then gate the contents of the channel buffer to the line buffer only if the incoming message contains a character. A reply which contains a 1-out-of-3 bit return code is sent to inform the 3A CC that (1) parity of received information is not valid, (2) the line sequencer is busy, and (3) the line sequencer is idle (character will be transmitted).

4.06 The line circuits are in the rest state when the character is gated to the line buffer from the channel buffer. The line circuits are switched into the transmit state, and the character is sent to either one TTY or all the TTYs, depending on which ports (0 through 3) are enabled. After the last stop bit, a demand interrupt is sent to the 3A CC, indicating that the character was sent to the TTY. The character is also looped back into the line buffer. After the TTY character is transmitted, the TTYC line circuits return to the rest state.

B. TTY to TTYC to 3A CC

4.07 When an input from a TTY is received at any one of the TTYC ports, the line circuits are switched from the rest state to the hit state for one-fourth of a normal bit period. If a mark (1) is indicated after the one-fourth bit period, the line circuits return to the rest state because the input resulted from a hit or noise on the line and not by a TTY input. If a space (0) is indicated after the one-fourth bit period, a character is coming in from one of the TTYs. The line circuits are switched to the receive state, and the character is loaded in the line buffer.

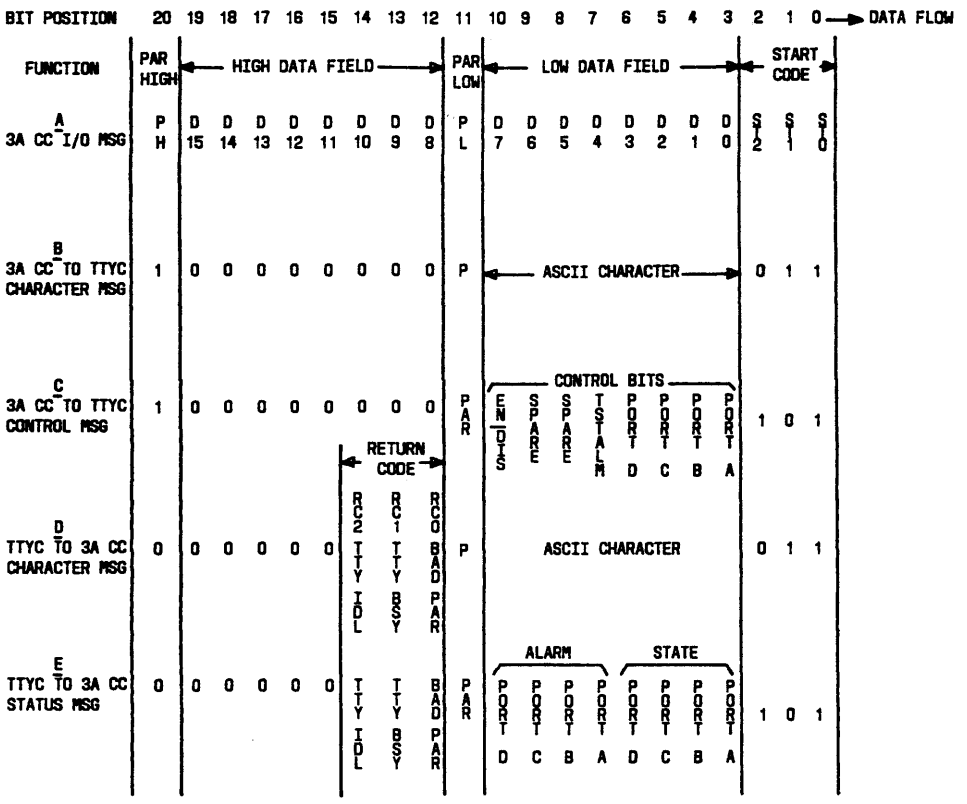

Fig. 7—Message Format

4.08 When the complete character is loaded in the line buffer, it is gated to a second register, the line register. Simultaneously, when the ready (RDYG10) signal is given, the line controller goes to rest. An interrupt (since the TTY functions with the 3A CC on a demand rather than scheduled basis) is generated, indicating to the 3A CC that a character from the TTY is available. This interrupt is generated at the end of the last stop bit. This provides time to service the interrupt and to read each character before the next character arrives. A poll acknowledge interrupt message is sent from the 3A CC to the TTYC. The channel circuit, which is in the receive state, loads the poll message into the channel buffer. The channel circuits are then switched into the process state. The channel sequencer examines the channel buffer and gates the contents of the line register into the channel buffer. The channel circuits switch into the transmit state, parity is generated, and the character (in 21-bit format) is sent to the 3A CC via the input/output subchannel. The channel circuits return to the receive state.

CONTROLLERS (FS1 AND FS2)

4.09 The left (FS1) and right (FS2) controllers (Fig. 5 and 8) are identical and contain the following circuits:

(a) Channel interface (part of FC200)

(b) Channel controller (FA1058)

(c) Line controller (FA1059)

(d) Line interface (part of FC200)

(e) Line timer (part of FC200).

A. Channel Interface

4.10 Channel interface provides the interconnecting circuitry between the 3A CCs and the TTYC. In the following discussion, leads having designations that end in 0 are at the low level (0) when active. Leads having designations that end in 1 are at the high level (1) when active. Prior to the reception

of data from the 3A CC, the control lead (IDP0) is high. When data is sent from a 3A CC, it is transformer-coupled into the channel interface. The presence of data gates the control lead (IDP0) active. When data is not present, the control lead (IDP0) is not active. This low-to-high transition of the control lead (IDP0) is coupled back into the channel interface and develops a 1/2-microsecond pulse on the initializing lead (IDOV1). This 1/2-microsecond pulse (1) is coupled to the channel interface and used to initialize the channel buffer register so that all zeros are loaded in the register. The 3A CC select lead (ZACT0 for 3A CC 0; OACT0 for 3A CC 1) for the data-sending 3A CC is gated and held low while data is being received. This low is also fed to the inhibit lead of the other 3A CC (INHOI0 for 3A CC 1; INHZI0 for 3A CC 0) and is used to block the gating of input data from the other 3A CC. The data received from the active 3A CC is converted from bipolar pulses to 3-volt logic levels and gated to the channel controller via the data lead (ID0) in serial form. The channel interface provides the clocking of the data (ID0). This clock, derived from the data stream of the active 3A CC, is gated into the channel controller channel buffer register via the enable lead (SHFT0). SHFT0 pulses low and back to high during each data bit period. The low-to-high transition shifts the state of the ID0 lead into the channel buffer.

4.11 The data reply for the 3A CC is fed serially from the channel controller circuitry via the data reply lead (OD0). Prior to data transmission, the interrupt lead (SINT0) is not active. SINT0 goes active to indicate that a character is ready in the line register. The transmit enable signal (3A CC 0—ENZ00; 3A CC 1—ENO00) will go from the active to not active state. This transition is derived from the 3A CC select lead (3A CC 0—ZACT0; 3A CC 1—OACT0). Data reply (OD0) is converted from 3-volt logic levels to bipolar pulses and gated to the active 3A CC via the transmit leads (3A CC 0—DO0P/DO0N; 3A CC 1—DO1P/DO1N). Timing for the outgoing data reply is derived from the zero data stream sent by the 3A CC. The data reply is a 15-bit bipolar message plus zeros as long as the input data stream continues.

B. Channel Controller

4.12 Before the data (ID0) is sent to the channel controller, an initializing signal (IDOV1), which is high, is received from the channel interface at the end of the previous message. This initializing signal clears the 15-bit channel buffer register; that is, loads it with all zeros. The data (ID0) is then shifted into the 15-bit channel buffer register using the enable pulses (SHFT0) high-to-low-to-high supplied by the channel interface as clocking pulses. Data is shifted into the channel buffer until a valid one (1) is detected in the low bit position. The leading one of the start code data freezes the message in the register. The start code and message parity of the input data are checked. The character ready flag flip-flop (RDYG10) is checked to verify that a character is ready for transmission to the 3A CC. (RDYG10 is high when not ready and low when ready.) The TTY state (RSTA0) is checked to see if the TTY is busy or idle. (RSTA0 is high when idle and low when busy.) These checks enable the channel controller to determine the proper actions as follows:

INCOMING MESSAGE	PARITY	READY (RDYG10)	REST (RSTAO)	TTYC ACTION	OUTPUT MESSAGE
Control	Good	No	Yes	Update status	Status
Control	Good	No	No	Update status	Status
Control	Good	Yes	No	Update status	Character
Control	Good	Yes	Yes	Update status	Character
Character	Good	No	Yes	Send character to TTY	Status
Character	Good	No	No	None	Status
Character	Good	Yes	No	None	Character
Character	Good	Yes	Yes	None	Character
Control / Character	Bad	Any	Any	None	Status

4.13 When the character message with good parity is received with no character ready flag (RDYG10) and the TTY state (RSTA0) indicates that the TTY is idle, the character can proceed. The 8-bit line buffer in the line controller is cleared; ie, it is set to all zeros by the line buffer clear signal (CLRLB0) from the channel controller. (CLRLB0 is high when not clear and low when clear.) The data message is then parallel shifted

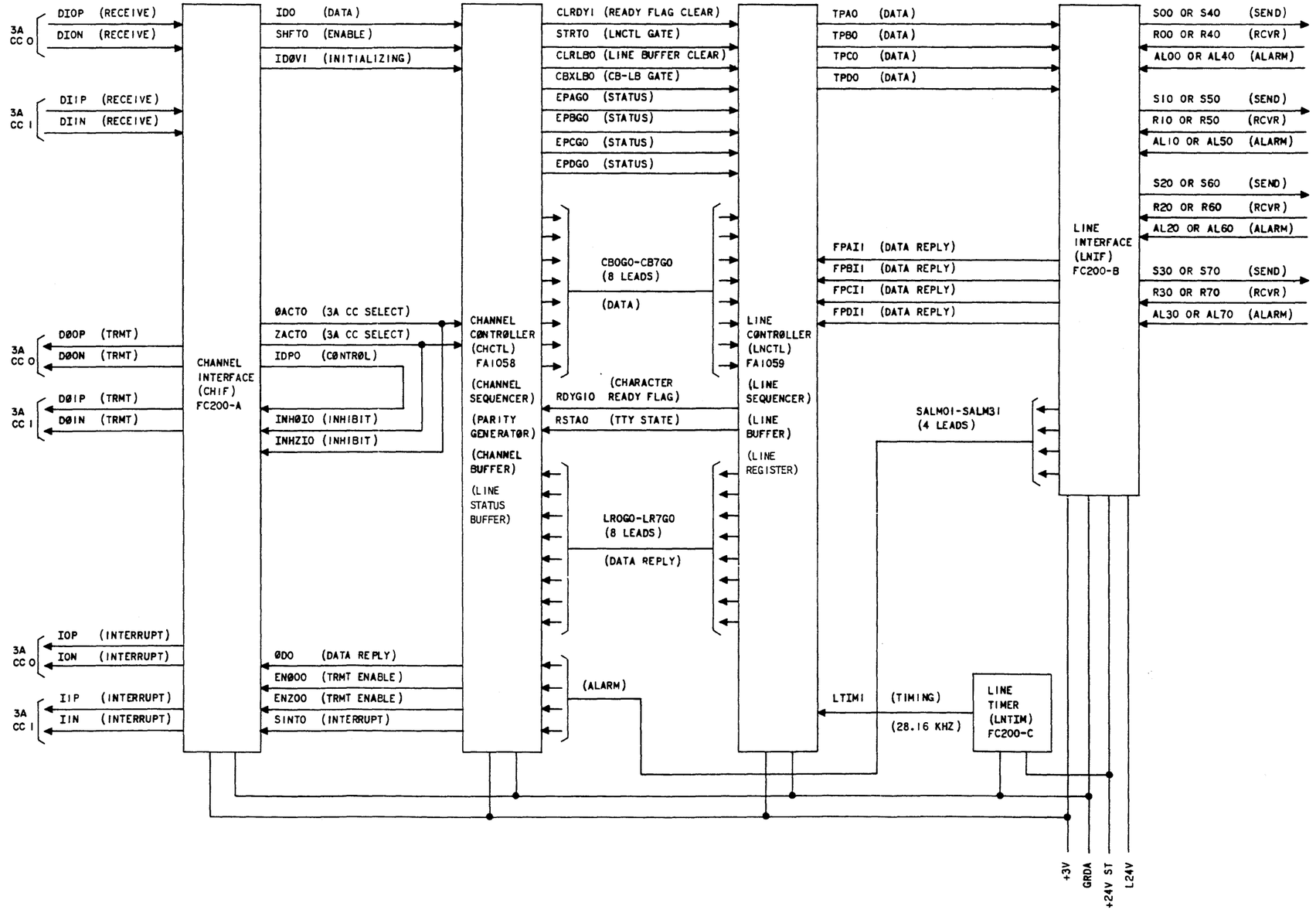

Fig. 8—FS1 and FS2 Controllers

from the channel buffer register via data leads (CB0G0 through CB7G0) into the 8-bit line buffer. The shifting of data from the channel buffer register to the line buffer register is accomplished by the gating of the channel buffer-line buffer gate signal (CBXLB0). (CBXLB0 is low when clear and high when not clear.) The channel controller then sends a line controller gate signal (STRT0). (STRT0 is high when not ready and low when ready.) STRT0 signals the line controller circuits to transmit the character to the TTY.

4.14 The line status buffer in the channel controller is an 8-bit register which contains two bits, enable and alarm, per port. The enable bits are activated by a control message. Status signals are passed to the line controller circuits via status leads (EPAG0, EPBG0, EPCG0, and EPDG0) where enabling and disabling functions are used to enable or disable a port. Port alarm bits are used to monitor the conditions on the alarm signal leads (SALM01, SALM11, SALM21, and SALM31). An alarm may be simulated by setting a test condition via a control message.

4.15 When a character is ready for transmission to the 3A CC, the character ready flag (RDYG10) is in the active state. Prior to loading of the reply data into the channel buffer, the channel controller internal circuitry clears and enables the channel buffer. The reply data (character) is then parallel loaded into the channel buffer from the line controller via data reply leads (LR0G0 through LR7G0). The channel controller generates the proper start code and parity bit. The data reply with the correct start code, parity bit, and number of bits (zeros in those bit positions not furnished) is gated to the channel interface. Before the data reply is sent, the appropriate transmit enable (ENZ00 for 3A CC 0; ENO00 for 3A CC 1) is made active. The demand interrupt tells the 3A CCs that a message is ready, and the transmit enable signal (derived from active 3A CC select lead) ensures that the data reply goes to the correct 3A CC.

C. Line Controller

4.16 The line controller directs the transfer of information between the channel circuits and the TTYs. A character to be printed is parallel loaded into the 8-bit line buffer register via data leads (CB0G0 through CB7G0) from the channel buffer. Before loading, the line buffer is cleared (CLRLB0 goes low) and the data is gated to the line buffer via the channel buffer-line buffer gate (CBXLB0 goes low). A sequence is started, whereby the contents of the line buffer are shifted out serially via any or all of the four data leads (TPA0—port 0, TPB0—port 1, TPC0—port 2, and TPD0—port 3), depending on which port or ports were enabled (status). The line buffer contents are preceded by a space (0) bit and followed by two mark (1) bits consistent with the start-stop signaling technique.

4.17 Bit timing (9.09 milliseconds per bit) is derived by counting down (dividing) the 28.16-kHz output from the line timer via the timing lead (LTIM1). The line buffer contents are shifted out and are looped back into the line buffer. This is done so that when the character has been completely transmitted to the TTY it is still in the line buffer in its original position. At the end of the second stop bit, the line buffer content is gated to the line register, and a demand interrupt occurs. The character ready flag (RDYG10) goes low telling the channel controller that a character is ready for the 3A CC. The channel controller circuit then receives the output of the line register (in parallel) via reply data leads (LR0G0 through LR7G0) on the next incoming message with good parity. The interrupt lead (SINT0) then goes low indicating to the 3A CC that reply data is ready.

4.18 Reply data from the TTY (typed character) is gated to the line controller circuits from the line interface via one of the four data reply leads (FPAI1—port 0, FPBI1—port 1, FPCI1—port 2, and FPDI1—port 3). This character is serially shifted into the line buffer and is transmitted to the other enabled ports (status). The incoming reply data from line interface is sampled at a 9.09-millisecond rate derived from the 28.16-kHz timing lead (LTIM1). At the end of the second stop bit, the character is gated from the line buffer to the line register and the same sequence as described in 4.17 and 4.18 is initiated to provide the data reply to the 3A CC.

4.19 The line controller also supplies the character ready flag (RDYG10) to inform the channel controller when a character is ready to be transmitted to the 3A CC. In addition, a TTY state signal (RSTA0) is supplied to inform the channel controller of the TTY condition, busy or idle.

4.20 Hit timing is provided in the line controller circuitry so that the character input sequence will not start unless the initial mark (1) to space (0) transition (start bit) is greater than 4.5 milliseconds.

D. Line Interface

4.21 The line interface provides the level conversions on the signals transmitted between the TTYC and the TTYs. An EIA-compatible source or termination is provided for send signals (S00 through S70), receive signals (R00 through R70), or alarm signals (AL00 through AL70). Incoming signals (alarm and receive) from the TTYs are converted to 3-volt logic levels and sent to the appropriate circuit. Receive signals are transmitted serially to the line controller via data reply leads (FPAI1—port 0, FPBI1—port 1, FPCI1—port 2, and FPDI1—port 3), depending on which port was active. Alarm signals are transmitted to the channel controller via alarm leads (SALM0)—port 0, SALM11—port 1, SALM21—port 2, and SALM31—port 3). Alarm signals indicate to the 3A CC that the local TTY is low on paper or that the remote TTY has lost carrier frequency to the 108D data set.

E. Line Timer

4.22 The line timer is a transistor oscillator that operates at a frequency of 28.16 kHz. The output of the line timer is transmitted to the line controller via the timing lead (LTIM1). The line controller uses the 28.16-kHz timing signal to derive the 9.09-millisecond bit timing.

PORT CONNECTORS (FS3 AND FS4)

4.23 Left (FS3) and right (FS4) port connectors are identical. Each port (total of four per port connector) can operate with a local or remote TTY in a current loop or voltage (EIA) mode. Any combination of available modes for the four ports is valid. Each port has a circuit pack (CP) connector and line connector. The type of output at a port is determined by the circuit pack equipped in the circuit pack connector and wiring in the plug that mates with the line connector (Fig. 9). The types of outputs at a port are listed in the following paragraphs.

A. Local EIA

4.24 When a local EIA TTY is used, no circuit pack is placed in the optional circuit pack connector. EIA levels from the line interface circuit appear directly at the line connector. These are as follows (EIA designations shown with TTYC designation in parentheses for port 0):

(a) AB (GRDA)—Signal ground

(b) BA (S00)—Transmitted data

(c) BB (R00)—Received data

(d) CF (AL00)—Carrier fail (alarm).

B. Local Current Loop

4.25 When a local current loop TTY is used, an AR17 circuit pack is equipped in the optional circuit pack position to perform the EIA-to-current loop conversion (a three-wire current loop is used with a common source and a separate send and receive lead). The -24 volt loop source is provided at terminal 10 of the line connector. Characters to be printed appear as EIA signals (S00). These are looped through terminals 11 and 14 of the line connector to terminal 9 of the circuit pack connector. They are converted to opens (off) and closures (on) at terminal 3 of the circuit pack connector and appear at terminal 2 of the line connector. The TTY receive loop is through line connector terminals 2 and 10. Appropriate opens (off) and closures (on) of these loops cause the proper character to be printed by the TTY.

4.26 Operation of the TTY keyboard causes signaling over the TTY send loop through line connector terminals 10 and 3. These appear at circuit pack connector terminal 2 and are converted to EIA signal levels and sent to CP connector terminal 4 and R00. The printing of a typed character involves that character being received and outputted by the TTYC on the TTY receive loop.

C. Remote Operation

4.27 For remote operation, a 108D data set is equipped in the circuit pack connector. The EIA output from the line interface (S00) is looped through terminals 14 and 2 of the line connector to terminal 3 of the circuit pack connector. The

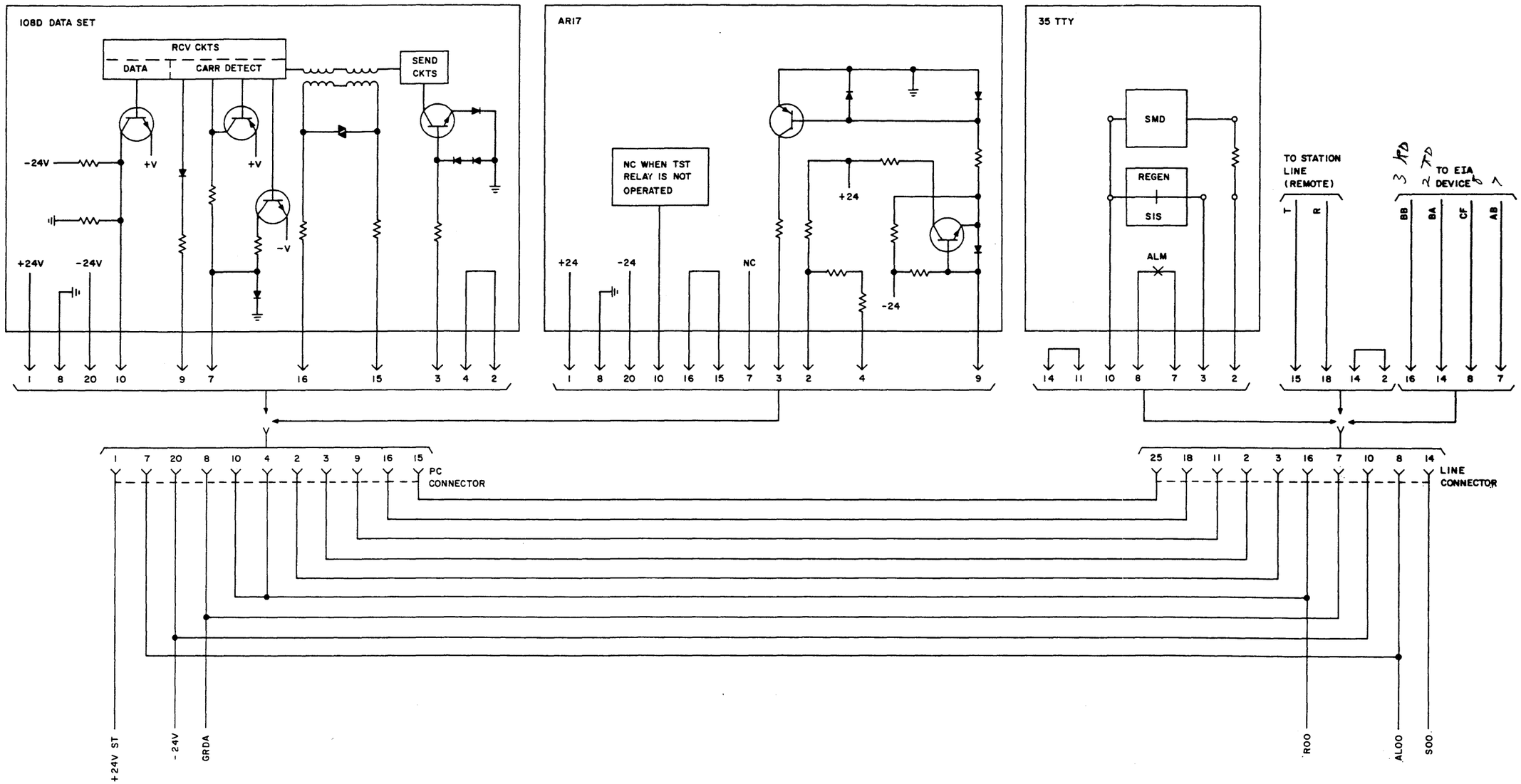

Fig. 9—Port Connector

data set converts these signals to frequency shift data on circuit pack connector terminals 15 and 16. This data is transmitted through the line connector, over a private telephone line, to the remote location. Provisions are made at the remote location to convert the frequency shift data into a proper signal to operate the remote TTY. Frequency shift data received from the remote location via the telephone line is converted to EIA levels by the 108D data set at circuit pack terminal 10 and R00. Fading and loss of the received carrier will be detected by the 108D data set and will cause an alarm condition on lead AL00 which will be detected by the channel controller.

5. POWER

5.01 The TTYC utilizes self-contained power supplies and requires only the standard -48 volt and +24 volt inputs. The dc-to-dc converter (J87389F) supplies the regulated +3 volts required by controller logic, and the FB494 regulator supplies -24 volts required for the 108D and AR17 circuit packs (Fig. 10).

POWER AND ALARM CIRCUITS

5.02 The TTYC power supply contains:

- J87389F [+3 volt power converter (A8)]
- FC21 (+3 volt power reference and filter pack)
- FB494 (-24 volt converter, major alarm circuitry control, and minor alarm circuit control)
- FB152 (+12 volt power reference circuit pack).

5.03 The -48 volt and +24 volt (control) power is supplied to the TTYC from the maintenance frame power circuit. The maintenance frame power circuits provide -48 volt source control, fusing, and alarms for the TTYC. The fuse panel contains power fuses for protecting the TTYC.

5.04 The A8 converter (+3 volts) and the FB494 converter (-24 volts) are started by depressing the TTYC POWER switch on the front of the TTYC. This applies the +24 volt start signal to the A8 and applies the -48 volt source voltage to the FB494 converter. When the TTYC POWER switch is depressed, operating the A8 and FB494 to the ON state, the TTYC POWER lamp is lighted. To remove power from the TTYC, depress the TTYC POWER switch. Operating voltage will be removed, and the TTYC POWER lamp will extinguish.

5.05 The alarm circuitry has the capability for a number of different alarms. The A8 power converter has an overvoltage and overcurrent (fuse) alarm. When an overvoltage or overcurrrent condition occurs, A8 is off and the light emitting diode (LED) indicator (on the A8) is lighted. Also, an FA signal is sent to the appropriate relay in the maintenance frame power unit. The A8 converter and the FB152 reference board also have an out-of-voltage limit alarm. When an out-of-voltage condition occurs, the LED on A8 and FB152 is lighted, and the PA signal is sent to the appropriate relay in the maintenance frame power unit. The lighted LEDs in the A8 converter and FB152 board can also be extinguished by placing an NPA signal (GRD) on the NPA lead.

5.06 The alarm circuit has the facility for power alarm test. The system operates the PAT relay, and a PAT signal is sent to both the A8 converter and the FB152 board. After test, an NPA signal is sent to the A8 converter and FB152 reference board to extinguish the LEDs.

6. MAINTENANCE

INTRODUCTION

6.01 If a failure occurs in either TTY channel, that channel can be taken out of service without affecting the service provided by the office. However, if a channel is out of service, operating personnel lose the control and monitoring capabilities provided by that TTY channel. For this reason, the TTY channel should be repaired as soon as possible. If the maintenance TTY channel is the channel taken out of service, a previously selected alternate TTY channel is used until the maintenance TTY channel is repaired. Primarily, these features are controlled by software programs.

BUILT-IN FEATURES

6.02 At the start of each TTY output message, a detection check is made by the 3A CC to guarantee channel integrity. The check consists of sending an inquiry character [who are you (WRU)] to a TTY, which will respond with a fixed

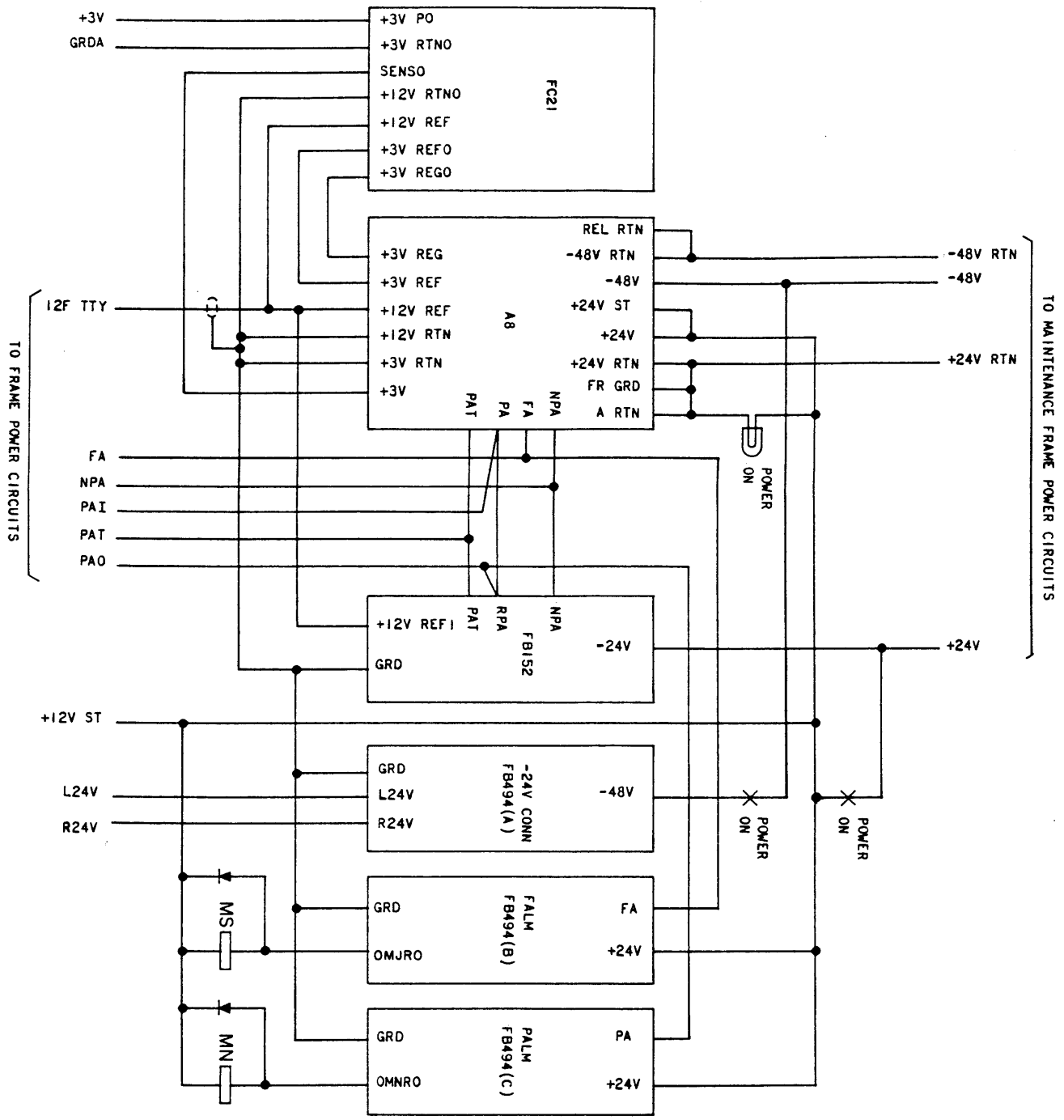

Fig. 10—Power Diagram

answer. After three of the four ports are disabled, the inquiry character is sent to the TTY connected to the one enabled port. If the inquiry character is not answered, a second inquiry character trial is made. If no response is received from any TTY or port, the TTY channel will be taken out of service. If a TTY channel is taken out of service, a request is entered to run complete diagnostics on it.

6.03 The TTYC sends back a single character when interrogated by the WRU character from the 3A CC. This informs the 3A CC that the TTYC is capable of receiving a message.

6.04 Each input/output message from the 3A CC to the TTYC is checked for correct start code and parity in the TTYC channel controller. Each character from the TTY to the 3A CC can be checked for correct parity by software. If an output character (input/output message from 3A CC to TTY) contains bad parity when received by the controller logic, no action is taken to transmit the character to the TTY. The appropriate status message which contains a maintenance code and return code indicating bad parity received from the 3A CC is returned to the 3A CC. In the case of no channel action to a 3A CC input/output message, a 3A CC software time-out will indicate an error when a response is not received from the controller logic in a specified time.

6.05 A check is made for TTY failures which cause a continuous input character to be sent to the 3A CC (such as BREAK, etc). In this case, the ports are temporarily quarantined from further input/output operations until the condition is corrected.

6.06 False reply data initiated by noise, etc, is prevented by the built-in hit timing feature in the line controller circuitry.

SOFTWARE

6.07 Software information pertaining to maintenance is contained in Section 254-340-090.

7. REFERENCES

7.01 The following Bell System Practices contain information relevant to this section.

Section 574-100-101—33-Type Teletypewriter

Section 574-201-100—35-Type (RO and KSR) Teletypewriter

Section 574-202-100—35-Type (ASR) Teletypewriter

8. GLOSSARY

8.01 The following terms and definitions are used in this section.

ASCII—Abbreviation for American Standard Code for Information Interchange.

Input Character—Character transmitted from the TTY to the 3A CC.

Local—Location within the office.

Output Character—Character transmitted from the 3A CC to the TTY.

Parity—The quality of being equal; that is, each data word to contain an odd or even number of 1 bits (including parity bit, if used).

Remote—Location beyond the immediate vicinity or outside the office.

Shift Register—A device that can shift data from one bit position to another and maintain the integrity of the original data pattern.

Start Code I/O—A 3-bit code used to notify a device of an input/output message and the type of input/output message, normal or maintenance.

Switching Control Center—Remote office which monitors and controls several offices.