

TAPE DATA CONTROLLER DESCRIPTION AND THEORY COMMON SYSTEMS

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PURPOSE

- 1.03 The TDC unit provides the following:
- Backup storage of system generic and translation programs which are resident in the main store (MAS) during normal operations
 - Storage of nonresident programs (not normally in MAS) which are needed by the office for administrative and diagnostic (maintenance) purposes
 - The capability for rapid and accurate access to information on the magnetic tape.

EQUIPMENT CHARACTERISTICS

1.04 The TDC unit (Fig. 1) contains a tape transport and the necessary electronics to provide power for the TDC unit and to provide access to the magnetic tape for read/write purposes. Data on the magnetic tape is stored in a serial phase-encoded format. The TDC operates asynchronously with the 3A central control (3A CC) in performing its data handling routines.

- 1.05 The TDC unit utilizes:
- (a) **Duplication:** Two complete units (TDC 0 and TDC 1) are provided to ensure reliability.
 - (b) **Circuit Packs:** The control and power electronics are plug-in circuit packs.
 - (c) **Cartridge Tape:** The cartridge tape offers handling advantages over reel-to-reel magnetic tape.
 - (d) **Connectorization:** Connectorized cables are used both internally and externally to the TDC.

1. GENERAL

INTRODUCTION

- 1.01 This section describes the physical and functional characteristics and the theory of operation of the tape data controller (TDC) unit.
- 1.02 Whenever this section is reissued, the reason for reissue will be contained in this paragraph.

2. PHYSICAL DESCRIPTION

TAPE DATA CONTROLLER UNIT

2.01 The TDC unit (Fig. 1 and 2) is comprised of equipment, wiring, and apparatus which, when assembled, is 8 inches high, 23 inches long, and 12 inches deep. This unit is duplicated and the two units are located on the maintenance frame (Fig. 3).

A. Interfaces

2.02 Fig. 2 provides a rear view of the TDC unit showing the multilayer printed wiring board (MLPWB) connector pins, backplane cable, and termination for a data set. The backplane cable is connectorized and interconnects the MLPWB, connecting blocks, and cartridge tape transport (CTT) jacks (J5 and J6). Coaxial connector terminals MYSA, MYRA, and MYINTA and MYSB, MYRB, and MYINTB interconnect (Fig. 4) with coaxial cables between TDC units and 3A CC units 0 and 1, respectively, on input or output subchannels (IOSC). Each TDC unit interconnects with each 3A CC unit via three 100-ohm coaxial cables. A cable (maximum length of 50 feet) may connect to a synchronous data set (SDS) on either TDC unit.

2.03 Each TDC unit consists of the TDC circuits, CTT, tape cartridge (TC) and power, which consists of two J87421A dc-to-dc power converters and associated equipment (Table A).

B. Tape Data Controller Circuit

2.04 The TDC unit (Fig. 1) consists of plug-in circuit packs (Table A). Two 87B apparatus mountings house the JK-type circuit packs and the two J87421A power converters. The 130A designation strips identify each JK-type circuit pack and its position. The equipment positions (0 through 44) are located horizontally (front view), left to right, on 1/2-inch centers. The equipment positions (00 through 08) are located vertically, bottom to top, on 1-inch centers.

2.05 The JK-type circuit packs plug into the 947A connectors as shown in Fig. 5. The MLPWB consists of four 4- by 7-inch layers and connects the +5 volt power and ground pins of the 947A connectors and the 347A ground pins of the coaxial terminal fields (CTFs) to appropriate layers.

C. Cartridge Tape Transport

2.06 The CTT (Fig. 6) is a KS-21447 mini-recorder which may be removed as a unit from each TDC unit. A connectorized cable plugs into jacks J5 and J6 to connect the CTT to the TDC circuit (Fig. 2).

Caution: Do not replace or repair CTT circuit packs at office level. Replace entire CTT instead.

2.07 The front panel is removable (held in place with two beryllium copper strip springs) and provides access to four plug-in circuit packs designated CP1 through CP4, respectively. These packs provide the following circuitry: logic and control, servo, write, and read. The CTT also contains a 4-track read-after-write head, a 4-track erase head, tape mark sensor (beginning of tape or end of tape status), cartridge-in-place (CIP) microswitch, a write-protect microswitch, and two pushbutton switches for manual rewind and unload operation. All tape motion is provided by the capstan motor assembly located in the front center of the CTT.

2.08 The CTT is equipped with a vent plate to provide ventilation for the interior components. A cartridge cover (snaps in place) is provided to house the TC and prevent contamination of the tape. When the cartridge is in place, the CIP microswitch is operated. When the write-protect plug of the TC is in the nonsafe position, a second microswitch is operated that enables the write circuitry for tracks 2, 3, and 4. Both the CIP and write-protect switches must show that the cartridge is in place and that the write-protect plug is in the nonsafe position for proper operation of the TDC unit.

D. Tape Cartridge

2.09 A TC (KS-21439,L1) consists of a magnetic tape covered with a transparent plastic case that measures 0.66- by 4- by 6-inches. This transparent plastic case has been removed in Fig. 7. The TC also consists of an aluminum base plate which acts as a reference mounting plane for the two belt guide rollers, supply and take-up hubs, two fixed tape guides, belt capstan, mirror, and write-protect plug. This unit is equipped with a tape shield (door) which automatically closes when the cartridge is removed from the transport and opens as the cartridge is inserted.

2.10 The capacity of the supply and take-up hubs is approximately 300 feet of 1/4-inch magnetic tape. The CTT drive capstan friction drives the belt capstan (Fig. 7) which in turn moves the flat drive belt and maintains the proper tension of the tape across the heads. The supply hub is equipped with an enlarged set of plastic flanges (top and bottom) that completely cover the tape when it is at the beginning-of-tape (BOT) position.

2.11 A hole pattern punched at specific locations in the tape (Fig. 8) in conjunction with the TC mirror and CTT infrared light sensor assembly (Fig. 9) provides sensing of BOT mark, end-of-tape (EOT) mark, load point (LP) mark, and early warning (EW) mark positions of the tape. These holes are used as reference points for starting and stopping the tape. An EW mark indicates that the physical EOT is approaching when the tape is moving forward. An LP mark indicates that the physical BOT is approaching when the tape is moving in a reverse (rewind) direction. The physical BOT or EOT location is any point between the physical ends of the tape and the last BOT and EOT marker. The logical BOT or EOT is any point between the last BOT and LP mark or the EW and EOT mark, respectively.

3. FUNCTIONAL DESCRIPTION

TAPE DATA CONTROLLER UNIT

A. General

3.01 Fig. 4 shows each 3A CC and its interconnections between the TDC units and each MAS.

3.02 The main store is grouped into three areas: temporary store, generic program, and translation data.

3.03 The temporary store is used by the 3A CC to store transitory data. Because this data is temporary, it will not be recorded on tape.

3.04 The system (generic) program is write-protected and is stored on magnetic tape in segments of 4K (4096) words, with the first and last of 32 blocks being marked to indicate the segment. There are 4 tracks with 34, 4K segments on each. The generic program is stored on track 1 and translation data on track 2 with the overflow on track 3. [Track 1 is the only track that is write-protected with the write-protect plug in the nonsafe (normal) operating position.]

B. Tape Data Controller Circuit

3.05 The functional block diagram of the TDC circuit (Fig. 10) identifies the combination of circuits required to interface between the 3A CC, the CTT, and a data set. Each of these circuits has a particular function which may be addressed (enabled) as required under software

control. The function of each is described in the following paragraphs.

Serial Peripheral Interface (SPI)

3.06 The SPI (Fig. 10) is the interface between the serial input/output channel (IOSC) at the 3A CC and the associated devices on the common parallel bus. It provides the means to communicate with the 3A CC and establishes the timing (clock), control (commands), and data signals (information and reply) over the common parallel bus to the other circuits of the TDC circuit.

Buffer (BUF)

3.07 The BUF (Fig. 10) provides two serial buffer memories (two shift registers, BUF 0 and BUF 1, each containing 1024 bits, their associated counters, and flags) which temporarily store data in transit to or from the CTT or synchronous data set (SDS).

Cartridge Tape Transport Controller (CTTC)

3.08 The CTTC (Fig. 10) handles the control and timing signals and data transfers to or from the CTT. It also provides automatic generation of preamble and postamble characters and performs a read-after-write check of data written on the magnetic tape.

Synchronous Data Set Controller (SDSC)

Note: The SDSC and local SDS are optional equipment required when the telephone company desires that MAS data be transferred to or from the regional data center.

3.09 The SDSC (Fig. 10) provides the interfacing and control circuits required for the origination of a call or the answering of an incoming call and the transfer of data to or from (one direction at a time) the local data set. The TC must be idle during the transfer of data by the data set and vice versa. The SDSC is compatible with SDSs transferring data at rates of 2K, 2.4K, 4.8K, and 9.6K bits per second. The data transfer rate of the local SDS must match that of the regional data center. When a data set (typically a 201C type) is provided, it must be connected manually to TDC0. The cable between the local SDS and TDC unit must not exceed 50 feet.

Bus Terminator (BT)

3.10 The BT (Fig. 10) provides the proper electrical terminations for the serial and parallel buses used within the TDC circuit. It also generates parity for status words originating from other circuits (BUF, SDSC, and CTTC) in the TDC and serves to verify the operation of the buses within the TDC circuit.

C. Cartridge Tape Transport

3.11 The CTT (Fig. 10) provides four circuit packs (CP1 through CP4) and a capstan motor. The circuit packs and their functions are listed as follows:

Circuit Pack 1

3.12 CP1 provides a logic and control circuit that decodes motion commands from the CTTC and indicates the status of the CTT system. The decoded motion commands are sent to CP2. The status indicators are sent to CP3 and CP4 to control writing and reading of the TC. These indicators are also sent to the input/output connector (J5 and J6) for use by the CTTC.

Circuit Pack 2

3.13 CP2 responds to the motion commands to control the direction and speed of the capstan motor that drives the tape. It also decodes the marker detectors to provide the indications of BOT, LP, EW, and EOT.

Circuit Pack 3

3.14 CP3 decodes the commands for the write and track select (1-out-of-4) and provides write current to the write head in serial, phase-encoded format. Input from the logic and control circuit (CP1) can inhibit the writing of data. CP3 permits the writing of data on magnetic tape at a tape speed of 30 IPS.

Circuit Pack 4

3.15 CP4 reads information from the magnetic tape at 30 IPS, decoding it into digital data. This circuit selects 1-out-of-4 tracks based on the input from CP1.

Note: Tape tracks are addressed as 0 through 3 and named 1 through 4 per American National Standards Institute (ANSI).

D. Tape Cartridge

3.16 A TC (Fig. 7) contains a 1/4-inch wide, 4-track magnetic tape wound on 2 hubs. As the tape is transported to the take-up hub (forward direction), it builds up to where the tape extends between the plastic flanges of the supply hub (which serve to prevent the tape from rubbing against any stationary surface by providing proper tape alignment).

Caution: *Setting off camera flash bulbs in the immediate vicinity, high ambient lighting, or direct sunlight may cause erratic operation of the cartridge tape transport.*

3.17 The tape between LP and EW is between 300 and 310 feet in length with 4 data tracks. Each track (Fig. 8) is divided into data blocks varying in length from 0.66 through 9.62 inches, dependent on system use. The number of data blocks varies from 306 through 1503 per track, depending on system use. The interblock gap (IBG) is constant at 1.55 inches.

3.18 Data blocks are used for storing the system information. The TC is equipped with a write-protect plug that inhibits accidental writing on any of the four tracks when in the safe position. When this plug is in the nonsafe (normal operating) position, only track one is write-protected.

3.19 The IBG is a magnetized gap which is automatically timed for 1.55 inches in length each time a block is written on the tape.

3.20 The basic entry of the tape is the data block (Fig. 11). The data block, less postamble and preamble, is multiple 16-bit words and is the combined contents of sequentially loaded 1024-bit shift registers. The tape handling program desires that the block be a multiple of 64 16-bit words (1024 bits), the capacity of one shift register. However, partial messages (less than 1024 bits) are handled via a BUF SET STUFF STATE command. Blocks are stored serially on the tape, but the block address system is such that they may be accessed in a random fashion.

4. THEORY OF OPERATION—SIGNAL AND CONTROL CIRCUITS

TAPE DATA CONTROLLER UNIT

4.01 The TDC unit (Fig. 10) is comprised of the TDC circuit, CTT, TC, and TDC power. Individual devices combine to form TDC circuit and CTT as shown within the broken lines of Fig. 10. These devices and circuits are interconnected with the common parallel bus (Fig. 12), serial buffer bus (Fig. 13), and interconnection leads (Fig. 14 and 15). These leads carry the messages and data that enable the TDC unit to perform its function of writing or reading data on or from the magnetic tape and transmitting or receiving data from the optional local SDS.

BUSES AND INTERCONNECTIONS

A. Common Parallel Bus

4.02 Fig. 12 shows the common parallel bus by individual leads and the devices that are connected to it. The bus extends from SPI to BT with BUF, CTTC, and SDSC connected in parallel. Negative logic is used on all (except clock) bus leads. On the information leads, a high level (2.4 volts to 5 volts) designates a logical zero (false) and a low level (0 volts to 0.4 volts) designates a logical one (true). On the command (control) and reply (response) leads, a low level indicates an active state and a high level indicates an inactive state of the signal designated for this lead. The clock lead supplies a 1.67-MHz pulse train.

4.03 Lead names and mnemonics identify the lead functions, for example, the information leads transmit information bidirectionally in the 21-bit message format (Fig. 16) and command leads identify with their command, for example, send data (SD0) is a request to an addressed device to gate data onto the information leads. Addressed devices can gate onto the information leads during send status (SST) or send data (SD) commands which are sent over leads SST0 and SD0, respectively. WAIT0 and SYNC0 are response leads and have a signal only in response to a command from the SPI.

4.04 Table B provides in detail the function of each common parallel bus lead.

B. Serial Buffer Bus

4.05 Fig. 13 shows the serial buffer bus by individual leads and the devices that are connected to it. The bus extends from BUF to BT with CTTC and SDSC connected in parallel. Negative logic is used on all of these leads except buffer clock (BCLK) which supplies a square wave with a nominal 600 ns period. These leads provide for signaling and serial transmission of data between the BUF, CTTC, and SDSC. Lead names and mnemonics identify the lead function, for example, the serial data out (SDOT0) lead carries data serially out of the BUF to BT and any device on the serial bus, and vice versa for the serial data in (SDIN0) lead.

4.06 Table C provides in detail the function of each serial buffer bus lead.

C. Interconnection Leads Between Cartridge Tape Transport Controller and Cartridge Tape Transport

4.07 Fig. 14 shows the interconnection leads between CTTC and CTT. Negative logic is used on all of these leads. Lead names and mnemonics identify the function, for example, data detect (DATDET0) being low indicates that the data area (Fig. 11) of the data block is passing across the read head.

4.08 Table D provides in detail the function of each interconnection lead.

D. Interconnection Leads Between Tape Data Controller Unit and Synchronous Data Set

4.09 Fig. 15 shows the interconnection leads between SDSC and SDS. Negative logic is used on all of these leads. Lead names and mnemonics identify the lead functions, for example, transmit data (TRDN) indicates that data is transferred to the SDS over this lead.

4.10 Table E provides in detail the function of each interconnection lead.

COMMANDS

4.11 The 3A CC communicates with the TDC unit over a serial channel at 6.67 MHz with a 21-bit serial message (Fig. 16). This message contains coded commands or data, start codes, and device addresses, and will return confirmation,

status, and data. The addressable devices are SPI, BUF, CTTC, SDSC, and BT.

A. Serial Peripheral Interface

4.12 The common parallel bus extending from SPI to the BT with associated devices BUF, CTTC, and SDSC is a master-slave arrangement. The 3A CC via the SPI is the master.

4.13 The SPI is the interface providing an input/output buffer (IOB) register (Fig. 25) which receives a 21-bit serial message (Fig. 16) of which the first bit (bit zero of the start code or least significant bit position) is always a one. A "one" arriving in the IOB least significant bit position indicates that the message from the 3A CC has fully shifted into the IOB. This bit and the other two bits of the 3-bit start code in the three least significant bit positions of the IOB are decoded to determine whether the information in the message is a command or data. Start code 101 indicates a command and 011 indicates a data message.

4.14 The SPI decodes the state of bits 0 through 5 (3 out of 6 code) to determine the address of a command. When the SPI is addressed (device address 7s), it interprets the SPI command (Fig. 17, Format A) by the combination of bit states of bits 12 through 15 to determine which of the commands on Fig. 17, Table A is present. Only addressed devices will gate onto the information leads.

4.15 Table F provides in detail the function of each command shown in Fig. 17, Table A.

B. Buffer

4.16 The basic function of the BUF (Fig. 26) is to temporarily store serial data that is in transit (either direction) between the 3A CC and CTTC or SDSC. Two 1024-bit shift registers BUF 0 and BUF 1 (JK13 position 27) provide the memory for storing the serial data. Each shift register is switchable on-line/off-line with the CTTC or SDSC always being associated with the register that is in the on-line position (BUF 1 in Fig. 26) via the serial bus leads. The 3A CC is always associated with the shift register that is in the off-line position (BUF 0 in Fig. 26) via the parallel bus leads and intermediate transfer register (ITR). The ITR (JK12 position 28) converts parallel data to serial and serial to parallel for transfer over the

information leads of the parallel bus. The shift registers interface directly to the serial bus.

4.17 Circuit pack JK10 position 31 (Fig. 26) provides circuitry for address decoder (bits 0 through 5, device address 13s), command decoder (bits 13 through 15), and state register (bits 9 through 12). A combination of bit states in each of these categories determines the action taken by BUF (Fig. 18, Table A and Format A).

4.18 Circuit pack JK11 position 29 (Fig. 26) provides two sequencers, off-line and on-line for sequencing BUF0 and BUF1. The off-line sequencer processes state register commands LOAD, UNLOAD, and STUFF and the on-line processes FILL commands initiated by the 3A CC, CTTC, or SDSC.

4.19 Table G provides in detail the function of each BUF command shown in Fig. 18, Table A. Table H provides the function of each BUF status reply shown in Fig. 18, Format B.

C. Cartridge Tape Transport Controller

4.20 The CTTC provides the interface between the TDC circuit and CTT (Fig. 27). It decodes the commands (Fig. 19, Table A, B, and Format A) from the 3A CC and initiates the proper sequencing of the control leads to the CTT and the BUF to effect proper tape motion, tape track selection, and proper data transfer between the CTT and the BUF. The CTTC (device address 15s) provides automatic generation of data preamble and postamble characters and performs a read-after-write check of data written on tape. Data to be written on the tape is shifted from the BUF, phase encoded, and presented to the write-head driver circuits in the CTT under control of the CTTC. During a read operation, the phase-encoded data residing on the tape is sensed by the CTT read heads. The data and clock components are decoded and separated by the CTT circuit, and the data is transferred to the BUF under control of the CTTC. The interconnection leads which carry the control and timing signals and data transferred to or from the CTT are shown in Fig. 14.

4.21 Fig. 27 shows the basic function of various parts of each circuit pack. JK-17, position 21, reads data from tape, strips preamble and postamble from the data, performs a cyclic redundancy

check (CRC), and then transfers the data over the SDIN0 lead to the on-line buffer. JK-18, position 20, receives data from the on-line buffer over the SDOT0 lead, adds preamble and postamble, and presents it to the write head to be written serially on the tape in the phase-encoded format. In order for JK-17 and 18 to perform their functions, JK-16, position 22, must be addressed and receive commands as required (Fig. 19, Table A, B, and Format A).

4.22 Table I provides in detail the function of each CTTC command shown in Fig. 19 Table A.

4.23 JK-16 also provides a primary status reply message (Fig. 20, Format A) that returns a combination of bit states on bits 8 through 11 which indicate the operation (Fig. 20, Table A) that is presently in progress. JK-16 interprets track selection and tape motion commands that are associated with the reading and writing process performed by JK-17 and 18.

4.24 JK-19, position 19 provides a secondary status reply message (Fig. 20, Format B) in response to a secondary status request command.

4.25 Table J provides in detail the function of each secondary status reply (Fig. 20, Format B).

D. Synchronous Data Set Controller

4.26 The SDSC (Fig. 28) is a user specified option and provides the interface between the TDC circuit and SDS. It decodes the commands (Fig. 21, Table A) from the 3A CC and initiates the proper sequencing of the control leads to the SDS and the BUF to effect the proper data transfer between the regional center and the MAS. Table K defines in detail the function of each command. The SDSC performs five major functions; address decoding, control, transmit, receive, and buffer unloading and loading.

Address Decoding

4.27 The device decoding and handshaking logic provides communication capability to and from the parallel bus. Leads RC0, RD0, SST0, and INIT0 carry the commands from the parallel bus; leads ER0, SYNC0, WAIT0, and GP0 carry the response to commands from the parallel bus. Information leads INF000—INF050 are decoded (3-out-of-6) by the SDSC (device address 16s) to

enable response to 3A CC commands. During an SDSC status command, information leads INF010, INF020, and INF030 are set to ones to identify the device to the 3A CC (Fig. 21, Format B). ER0 lead is set to a one during the time that information leads 010, 020, 030, and RC0 or BOFL0 are set to ones.

Control

4.28 The 4-bit control register (bits 12 through 9) determines the mode of operation of the SDSC. These bits are under direct control of the 3A CC via common parallel bus leads INF090—INF140. Leads INF130 and INF140 control the state of the 4-bits in the control register. The DTR bit when set proceeds to establish a talking path between the regional center and the SDS. With the talking path established, a key in the telephone set may be operated to transfer to the data mode which causes the talking path to become a data link. This causes the SDS to assert the data set ready (DSR) bit (bit-13), which indicates to the SDSC that the SDS is connected and ready to communicate with it. An SDSC status command (Fig. 21, Table A) received by the control register will return status (Fig. 21, Format B) over leads INF060—INF150 (Fig. 28). Table L defines each status in detail.

Transmit

4.29 The 3A CC asserts a request to send (RTS); the SDS responds with a clear to send (CTS) indication and the transmit clock pulse (TCP) on their designated leads. The transmit logic synchronizes this information to transfer data from the on-line BUF over the SDOT0 lead to the SDS over the TRDN lead. The transmit logic also generates the buffer shift pulse (BSHP0 lead) to clock the data out of the buffer circuit.

Receive

4.30 The set receive command sets the receive bit in the control register which in turn enables the receive logic. When the receive logic is enabled, bit and character synchronization can be established. Once character synchronization has been established new message (NMSG) bit goes active and an end of message (EOM) detector is enabled. The data is received over the RD lead and sent to the on-line BUF over the SDIN0 lead. The EOM detector monitors the receive clock pulse (RC lead) and carrier detect (DCD lead) from the

data set. When the absence of either is detected, the EOM detector signals the buffer circuit to effect a fill (FILL0 lead), a fast right-adjustment of the currently on-line BUF.

Buffer Unloading and Loading

4.31 The SDSC transfers a serial data stream of 8-bit characters (2 characters per 16-bit data word) to and from the on-line BUF (the off-line BUF is always associated with the 3A CC). Preceding and following the data stream are characters that define the start and end of the data block.

E. Bus Terminator

4.32 The BT (Fig. 22) provides a far-end electrical termination for the common parallel and serial buffer buses. Circuit pack JK9, position 16, provides a 16-bit holding register into which data may be loaded from the parallel bus and from which the data may be subsequently dumped back to the bus for return to the 3A CC. The basic function of this register is to provide parity generation over replies to the 3A CC; ie, when SPI requests SST or SD from BUF or CTTC, the BT assumes control over the 16-bit data word until it settles down (flag bits may be in the process of changing state) and then returns the reply to the 3A CC. The settling down period assures that the 3A CC sees the true state of the parallel bus.

4.33 Leads GP0 and GPR0 provide control between BT and associated devices. GP0 is asserted while the device (BUF, CTTC, or SDSC) is gating a 16-bit data word onto the information leads. The BT recognizes the GP0 signal and along with the device, asserts lead WAIT0. The BT clocks bit states of the data word into its holding register and asserts GPR0 to notify the device that it has control. Then the device will gate its bits off the information leads and negate its control on WAIT0. BT gates the contents of its holding register onto the information leads and negates WAIT0. SPI notes the negation of WAIT0 and clocks the states of the information leads into its (IOB) register and removes the SST0 and SD0 command signal. The device responds by negating SYNC0 and BT responds by negating GPR0 and gating itself off the information leads.

4.34 The BT (when addressed with device code 00s or 77s) will respond to a receive data (RD) command from the 3A CC and store the 16-bit

data word in the holding register. An SST following the RD will gate the data word onto the information leads and back to the 3A CC.

4.35 Circuit pack JK8 (position 17) responds to BT address and a 5 (101) start code. The BT will not respond to a send data command (SD) but will assert the SYNC lead in response to either acknowledge interrupt (ACKI) or INIT to complete the handshaking with SPI. The SPI prefixes all BT replies to the 3A CC with a 5 start code because the BT asserts the ER0 lead whenever it is addressed. The addressing feature of the BT allows the 3A CC to verify the operation of the SPI and information leads of the parallel bus.

4.36 Serial buffer bus leads terminate on BT as shown in Fig. 22.

CARTRIDGE TAPE TRANSPORT

4.37 The CTT responds to commands issued by the CTTC (Fig. 19, Table A) with the following equipment:

- Logic and control circuit (CP1)
- Servo circuit (CP2)
- Capstan motor
- Write and track select circuit (CP3)
- Read and track select circuit (CP4).

Logic and Control Circuit

4.38 The logic and control circuit (CP1) decodes motion requests from the CTTC and indicates the status of the system. The motion requests and transport status are carried on leads entering the CTT on J6 (Fig. 14). The decoded motion requests are sent to the servo circuit (CP2). The other control signals are sent to the write and track select circuit (CP3) and read and track select circuit (CP4) to control writing and reading of the tape cartridge. The tape and transport status is also sent to the CTTC (Fig. 20, Formats A and B) and is available to the 3A CC upon request (when a CTTC secondary status request command is issued.)

Servo Circuit

4.39 The servo circuit (CP2) receives the decoded motion commands from CP1 and controls the speed of the DC capstan motor in a stop, forward, reverse, slow, or fast mode. The forward and reverse directions may be slow or fast, 30 inches per second (IPS) or 90 IPS, respectively. The direction and speed are dependent upon the command issued (Fig. 19, Table A).

4.40 The servo circuit also decodes the outputs from the tape mark (tape holes) detectors to provide the indications as shown in Fig. 20, Format B.

Capstan Motor

4.41 This motor is friction-coupled to the TC via a rubber drive puck and moves the tape as required under control of the servo circuit.

Write and Track Select Circuit

4.42 This circuit (CP3) decodes the write-track signals (1-out-of-4) and provides write current to the proper write-head and erase-head tracks. The direction of current flowing through the write head is directly controlled by the write data signal from the CTTC. Data is written serially on the tape in a phase-encoded format at the rate of 48K bits per second. The write-protect plug on the TC may be used to inhibit the writing of data on the tape.

Read and Track Select Circuit

4.43 This circuit (CP4) reads the phase encoded signals from the tape, decoding them into digital data. The read head reads data at 1600 bits per inch from a tape moving at 30 IPS. Therefore, the data transfer rate is 48K bits per second.

TAPE CARTRIDGE

4.44 The TC is a data storage device consisting of approximately 300 feet of 1/4-inch wide magnetic tape. When inserted in the CTT, the tape makes contact with stationary read, write, and erase heads.

4.45 The data on the tape is divided into blocks (Fig. 8) separated by IBGs. The data block

is assigned as shown in Fig. 11. The CTTC adds the 16-bit preamble and postamble words during a write operation (this is a synchronization code) and automatically strips it off during a read operation; therefore, this code is never stored in the BUF shift registers. The shift registers (BUF0 and BUF1) will store the block identifier word (address, track, double end of file, and end of file bits) and cyclic redundancy check character (CRCC) as well as data. The shift registers (Fig. 26) store data in multiples of 64 16-bit words; hence, the two registers filled twice will store up to 256 words. This is equal to the contents of one No. 3 ESS data block.

4.46 The block address and track number enable the data blocks to be identified without knowing the absolute tape position. This requires that the block contain a position number relative to the BOT. The data detect lead (Fig. 14) and bit 11 (Fig. 20, Format B) may be used to count the blocks passing over the read head and, therefore, determines the tape position without reading the blocks into the 3A CC.

4.47 The last word of the data block is used to store the CRCC. This is a 16-bit check character used to validate the data written on or read off the tape.

5. THEORY OF OPERATION—POWER AND ALARM CIRCUITS

INTRODUCTION

5.01 The TDC unit utilizes self-contained power supplies and requires no additional power other than the standard -48V and +24V inputs. Two J87421A dc-to-dc converters convert -48V to +5V to supply the individual JK-type circuit packs in the TDC circuit via the multilayer printed wiring board (MLPWB) and the CTT via Jack 6.

POWER AND ALARM CIRCUITS

5.02 The power source (Fig. 23) for the TDC units 0 and 1 is the maintenance frame power unit located at the bottom of the maintenance frame (Fig. 3). The fuse panel (part of this unit) provides 70-type fuses with 3/4, 1-1/3, and 2 amp protection for the +24V and -48V supplied to the two J87421A (Fig. 23) power converters which generate the required +5V power. Any (TDC unit) blown fuse will operate the MJ3 (major alarm)

relay (Fig. 23) which initiates a visual and audible office alarm.

5.03 A switch designated TDC POWER, mounted on the right side of the switch bracket assembly (Fig. 1), turns the power converters on and off (via 24V ST leads) and applies -48V power to the BUF, CTT, and SDSC and +24V power to the SDSC, CTT, and switch lamp. This switch is an alternate action device which, when depressed, applies power to the TDC circuit and lights a lamp inside the switch. When depressed a second time, it removes power from the TDC circuit and extinguishes the switch lamp. The +24V and -48V supply is fused and wired directly from the maintenance frame power unit to the converters and is not controlled by the TDC power switch.

5.04 The J87421A (Fig. 24) converters utilize a pulse-width controlled transistor circuit to provide the regulated +5V output.

5.05 Each converter contains an out-of-voltage limit alarm (over and under), an overvoltage shutdown, and an overcurrent shutdown, each of which produces a visual alarm on the converter. The visual alarm is a red light emitting diode (LED) mounted on the front of the converter face plate that lights as a result of any of the above conditions.

6. MAINTENANCE

INTRODUCTION

6.01 The objective of the overall maintenance plan is to maintain and repair or replace faulty equipment as quickly and as efficiently as possible.

PROCEDURES

6.02 Before performing maintenance procedures on the TDC units, the system documentation numerical index should be consulted. This index will direct the craftsperson to TDC cleaning, adjustment, replacement, and tape operating procedures.

BUILT-IN FEATURES

6.03 The built-in features are redundancy, detection, and recovery and are described in the following paragraphs.

Redundancy

6.04 There are two TDC units and the information on each TC should be identical. The TC provides a backup image (or copy) of write-protected main store (MAS) programs (current and past). The TC also stores infrequently used diagnostic and service order programs.

Detection

6.05 There are two built-in checks on data transferred to and from the TDC, parity, and cyclic redundancy character (CRC). The two parity bits (high and low) maintain odd parity over their respective 8-bit field. The parity bits are not stored on tape. The CRC (Fig. 11) is the last word stored on the data block. This 16-bit check character is used to validate the data read off or written on the tape.

Recovery

6.06 Each 3A CC has high-speed facilities to switch duplicated TDC units in and out of service upon request or when an emergency condition exists. For an emergency condition, the TC stores bootstrap information on the first data blocks of tracks 1 and 2. This program and associated microinstructions provide the capability to rapidly reload the MAS from tape.

SOFTWARE

6.07 The TDC unit is controlled by commands from the 3A CC. The 3A CC may issue these commands such that various trouble conditions may be tested and detected.

7. REFERENCES

7.01 Additional information is available from the following Bell System Practices:

- Section 034-362-701—Mini-Recorder KS-21447,L1 and L2 Requirements and Adjusting Procedures
- Section 254-300-110—3A Central Control Description Common Systems
- Section 254-300-120—3A Central Control (3A CC) Theory of Operation Common Systems

- Section 254-300-160—Maintenance Frame Description and Theory of Operation Common Systems
- Section 254-300-180—System Status Panel Description and Theory of Operation Common Systems.

8. GLOSSARY

8.01 A glossary of terms is provided to aid in understanding this section.

Bipolar Pulse—A pulse that has both a positive and a negative polarity.

Bootstrap—An operation utilizing software to generate a complete, workable active system.

Command—A combination of bit states that forms a message conveyed to an addressed device which causes it to perform a particular function.

Cyclic Redundancy Check Character—An error detection technique in which the data in a data block is operated on by an algebraic expression ($\chi^{16} + \chi^{15} + \chi^2 + 1$) and the remainder is compared with the CRC word.

Start Code (I/O)—A 3-bit prefix (101 or 011) within the 21-bit message used to identify command or data (input) and normal or error (output) conditions.

Device—A solid state component or group of components that forms an electrical circuit whose operation depends on the control signals inputted.

Device Address—A 3-out-of-6 (a 6-bit binary code in which 3 of the bits are logical ones) code assigned to the device that enables it to identify commands destined for that device.

Enable Pulse—A pulse that permits a device or circuit to become operative.

Fault—A condition that causes a device or component to fail to perform in a required manner.

Light Emitting Diodes—LEDs are chemically grown gallium phosphide crystals that convert direct current into a visible light output without benefit of energy-consuming filaments.

Parity Bit—A bit attached to a word to make the total number of ones including the parity bit either odd or even (always odd for the TDC unit).

Shift Register—A device that can shift data from one bit position to another and maintain the integrity of the original data pattern.

Tape Mark—A hole punched in the tape used to identify the position of the tape.

TABLE A

SUMMARY OF TAPE DATA CONTROLLER
UNIT EQUIPMENT AND LOCATION

CIRCUIT DESIGNATION	EQUIPMENT	
	DESIGNATION	POSITION
CTT	KS-21447 L2	1-15
BT	JK9	16
	JK8	17
CTTC	JK19	19
	JK18	20
	JK17	21
	JK16	22
SDSC (OPTIONAL)	JK15	24
	JK14	25
BUF	JK12	28
	JK11	29
	JK10	31
SPI	JK7	32
	JK6	33
	JK5	34
TWO DC-TO-DC POWER CONVERTERS	J87421A L 1	35-44

TABLE B

COMMON PARALLEL BUS LEADS DESIGNATION AND FUNCTION (FIG. 12)

BUS LEADS	
DESIGNATION	FUNCTION
INFPH0	This lead maintains odd parity of leads INF080 through INF150. (This lead is bidirectional.)
INFPL0	This lead maintains odd parity of leads INF000 through INF070. (This lead is bidirectional.)
INF000 Through INF150	These 16 information leads are bidirectional and either send data or commands to the devices or receive data or status from the devices.
SD0 (Send Data)	When this lead is set to a 1, the information leads are conditioned to receive data from the devices enroute to 3A CC.
INIT0 (Initialization)	When this lead is set to a 1, all devices on the bus are reset to a predefined state.
ACKI0 (Acknowledge Interrupt)	This lead is used to identify the devices which are requesting interrupts. When ACKI0 is set to a 1, each of the devices which are requesting interrupts should set a predefined information lead to a 1. When the 3A CC receives the reply from the SPI, the devices which are requesting interrupts can be identified by the set bits of the reply. The ACKI0 results during a parallel get reply time state as a result of a command which uses the SPI 3-out-of-6 device address. BT responds to the command to complete the handshaking with the SPI.
SST0 (Send Status)	When this lead is set to a 1, the addressed device is requested to gate the contents of the register (that was addressed by a previous command) to information leads INF000 through INF150. (The device address code is returned along with the status.)
RC0 (Receive Command)	When this lead is set to a 1, the devices are requested to receive a command. The information leads contain a 3/6-code device address on INF000 through INF050 and a 10-bit coded command on INF060 through INF150. Only the addressed device (Fig. 10) will respond to the command and turn itself on to receive the succeeding command from the bus. All other devices should turn themselves off to disregard the succeeding command on the bus until a command with their specific address is issued. The addressed device responds to the SPI over a response lead (SYNC0) to indicate that it has received the message.
RD0 (Receive Data)	When this lead is set to a 1, the addressed device (3/6 code, Fig. 10) is requested to receive data from the information leads enroute from 3A CC.

TABLE B (Contd)

COMMON PARALLEL BUS LEADS DESIGNATION AND FUNCTION (FIG. 12)

BUS LEADS	
DESIGNATION	FUNCTION
GP0 (Generate Parity)	A device signals the bus terminator (BT) to generate parity over the 16-bit reply placed on the information leads by the device. A device may set GP0 to a 1 only during SST0 or SD0 command states. The BT clocks the state of the information leads into its 16-bit holding register at the trailing or low-to-high (1-to-0) transitions of GP0.
GPR0 (Generate Parity Reply)	The BT responds to the GP0 signal by setting GPR0 to a 1. The device must remove the signals from the information leads and remove the WAIT0 control signal input.
WAIT0	When this lead is set to a 1, it indicates that a command is given to the addressed device on the bus before the device is ready to accept it. The command and the data on the information leads will be held steady until the device has properly responded to the command and reset WAIT to zero.
SYNC0 (Synchronization)	SYNC0 is a quick loop-around echo response to the RC. SYNC0 should be set to 1 within 250 nanoseconds (ns) after an RC is issued and set to zero within 250 ns after an RC is removed. If a command is issued when the device is ready to receive it, SYNC0 is set to 1 to indicate that the RC has been understood and data has been gated onto or from the information leads. If a command is issued when the device is not ready to accept it, SYNC0 is set to 1 to merely indicate that the RC has been received by the device and WAIT0 lead is set to 1 to indicate that the information will be held steady until the device responds.
ER0 (Error)	When this lead is set to a 1, it indicates that the addressed device has discovered an abnormal condition.
INTR0 (Interrupt Processor)	This lead is set to a 1 when any device on the bus (device does not have to be addressed) wishes to interrupt the 3A CC.
CLK (Clock)	This lead provides a 1.67-MHz pulse train to the devices. This pulse will be present when the SPI is in communication with the 3A CC.

TABLE C

SERIAL BUFFER BUS LEADS DESIGNATION AND FUNCTION (FIG. 13)

BUS LEADS	
DESIGNATION	FUNCTION
BSHP0 (Buffer Shift Pulse)	<p>This lead is the clock line for the on-line shift register (Fig. 26) and performs or initiates the following:</p> <ul style="list-style-type: none"> (a) Clock pulses supplied by an associated device shift data into and out of the on-line shift register. (b) All devices must be off this line except when in the data transfer mode. (c) Any low-to-high (1-to-0) transition on this lead increments the on-line shift register counter. (d) The state of the SDIN0 lead is clocked into the register on the trailing edge of the shift pulse. (e) The output of the on-line shift register becomes valid on lead SDOT0 in response to the leading edge of the shift pulse and stays valid until the next leading edge. (f) Data will be lost in the shift register if the shift pulse is at ground level for more than about 10 microseconds.
SDOT0 (Serial Data Out)	<p>This lead is the serial data output of the on-line shift register (Fig. 26). Data shifted out of the on-line shift register appears in nonreturn to zero information (NRZI) format in response to shift pulses on the BSHP0 lead. This data will not be valid prior to the leading edge of the first clock pulse.</p>
SDIN0 (Serial Data In)	<p>This lead is the serial data input of the on-line shift register (Fig. 26). An associated device may gate information onto this lead only during a read mode.</p>
BOFLO (Buffer Overflow)	<p>This lead becomes set (to one) at the coincidence of BR being set to zero and the trailing edge of the active shift register counter carry pulse. The last active shift register will remain in the on-line position and no more clock pulses will be accepted from the associated devices.</p>
BACR0 (Buffer Active Counter Carry)	<p>A pulse on this lead indicates to the associated devices that the on-line shift register counter has been clocked with 1024 pulses on the BSHP0 lead. The carry pulse is nominally as wide as the 1024th pulse on the BSHP0 lead.</p>
BA16CR0 (Buffer Active 16-Bit Counter Carry)	<p>A pulse on this lead indicates to the associated devices that the on-line shift register counter has been clocked with 16 pulses on the BSHP0 lead. The 16-bit carry pulse is nominally as wide as every 16th pulse on the BSHP0 lead.</p>

TABLE C (Contd)

SERIAL BUFFER BUS LEADS DESIGNATION AND FUNCTION (FIG. 13)

BUS LEADS	
DESIGNATION	FUNCTION
FILL0 (Fill the On-Line Buffer)	<p>An associated device, by pulsing this lead, may cause right adjustment of a partial message in the on-line shift register.</p> <p><i>Note:</i> This feature is required for devices which handle data blocks that are not in even increments of the shift register size (1024 bits). A pulse on this lead performs or initiates the following:</p> <ul style="list-style-type: none"> (a) Starts the fill operation in the buffer. (b) The associated device may keep the SDIN0 lead high so that zero bits are recirculated into the on-line shift register behind the partial message bits. Also, the associated device must not put shift pulses on the BSHP0 lead. (c) The buffer clock (square wave with 600-ns period) is used to right-adjust (fill) the on-line shift register. (d) The fill operation is complete when the on-line shift register counter produces a carry pulse on the BACR0 lead. (e) The associated device must release FILL0 in response to or before the leading edge of the BACR0 pulse. (f) The buffer unit has a status bit-15 (set to a 1) to indicate that the fill operation is in progress. (g) Bit 15 is reset to zero when the operation is complete. <p><i>Note:</i> No memory is provided as to how many data bits were received from the associated device before the fill operation was started. Therefore, if the BR flag is reset (to a zero) by the time the fill operation is done, the on-line shift register switches off-line and the BR bit is set to a 1. If the BR flag is set when fill is done, the BOFL flag is set and the just-filled shift register remains on-line.</p>
BCLK (Buffer Clock)	<p>This lead furnishes a square wave with a nominal 300 ns on and 300 ns off time. The buffer unit requires a free-running clock for the purpose of commands STUFF and FILL.</p>

TABLE D

**INTERCONNECTION LEADS BETWEEN CARTRIDGE TAPE TRANSPORT CONTROLLER
AND CARTRIDGE TAPE TRANSPORT, DESIGNATION AND FUNCTION (FIG. 14)**

INTERCONNECTION LEADS	
DESIGNATION	FUNCTION
DATDETO (Data Detect)	<p>When this lead is set to a 1, it indicates that data (data block, Fig. 11) is passing under the addressed read head. When set to zero, it indicates that the head is crossing an interblock gap (IBG) (Fig.8) or the CTT is stopped.</p> <p>This lead, enabled when the CTT is selected, provides the following:</p> <ul style="list-style-type: none"> (a) Search at high speeds, ie, move a known number of blocks across the tape at 90 inches per second (IPS) in either direction simply by monitoring this lead and counting the number of transitions to the 1 state. (b) Indication of when a data block is being read. (c) The preamble detection circuitry in the CTT will cause data detect to become set to a 1 when eight consecutive zeros have been detected. Data detect will remain 1 until the addressed read head is a distance of 8-bit periods into the next IBG. See Fig. 11 for assignment of data on the data block. <p><i>Note:</i> This lead is a 1 during all times in which the CTTC is in the maintenance mode of operation.</p>
WTA00 (Write Track Address 0) and WTA10 (Write Track Address 1)	<p>The combination of these two leads which are binary coded decimal (BCD) controls the track selection for writing. Each lead may be a logic "1" (0 volts to 0.4 volts) or a logic "0" (2.8 volts to 5 volts). With this combination applied to these two leads, tracks are selected as follows: 00 = track 1, 01 = track 2, 10 = track 3, and 11 = track 4.</p>
RTA00 (Read Track Address 0) and RTA10 (Read Track Address 1)	<p>These are read address leads 0 and 1 and will control which track the read circuitry is addressing.</p>
WRENAB0 (Write Enable)	<p>This lead set to a 1 will enable the write current on in the write and erase heads for the track being addressed. This lead shall be set to a 1 before motion occurs and remain until the write operation and the CTT come to a complete stop. This eliminates the possibility of leaving residue on the tape between write operations when overwrites are being done.</p>

TABLE D (Contd)

INTERCONNECTION LEADS BETWEEN CARTRIDGE TAPE TRANSPORT CONTROLLER
AND CARTRIDGE TAPE TRANSPORT, DESIGNATION AND FUNCTION (FIG. 14)

INTERCONNECTION LEADS	
DESIGNATION	FUNCTION
WRDATA (Write Data)	<p>This lead is used to input data to be written by the CTT. This data is phase encoded with the proper timing to be written directly on the tape. While the CTT is moving and the write enable lead is set to a 1, an IBG may be written by holding the write data lead in the 1 state (0 V to 0.4V).</p> <p><i>Note:</i> The write data lead should always be in the 1 state before the CTT is write enabled or disabled to ensure that no marks are made in the IBG.</p>
RDDATA0 (Read Data)	<p>This lead is used to output data from the CTT. The data output will be accompanied by a read data clock, where the read data lead shall be stable a minimum of 1 microsecond before the leading edge of the clock pulse. A logical 1 will be 0V to 0.4V, and a logical 0 will be 2.8V to 5V. The IBGs shall hold the read data lead in the logical 0 state which will allow for easier framing of the data by the CTTC. The preamble will be 15 zeros followed by a single 1 (Fig. 11). When starting a read operation, the CTTC need only look for a 1 on the read data lead to identify the end of the preamble.</p>
RDCLK0 (Read Data Clock)	<p>This lead designates when a data bit is valid on the read data lead. This is indicated when the read data clock lead is at a logic 1. These clock pulses should be greater than 0.5 microseconds and less than 2 microseconds in width. No clock pulses should occur before the preamble detector is satisfied that a valid data block is being read. After the preamble has been read, the number of clock pulses which follow should be exactly the number of bits in that data block plus the postamble (Fig. 11). The read data clock lead shall remain in the false state whenever data is not passing under the addressed read head winding.</p>
TTMSTP0 (Tape Transport Maintenance Stop)	<p>When this lead is set to a 1, it completely disables the CTT. It stops any operation in progress and will not allow motion commands to be accepted.</p>
TTF0 (Tape Transport Fast Forward Search)	<p>When this lead is set to a 1, the CTT will move the tape in the forward direction at 90 IPS until one of the following takes place:</p> <ol style="list-style-type: none"> (a) Stop command is issued. (b) End of Tape (EOT) marker is detected. After detecting the EOT marker, the CTT will only accept a motion command which will move the tape in the reverse direction.
TTSF0 (Tape Transport Slow Forward)	<p>When this lead is set to a 1, the CTT will move the tape in the forward direction at 30 IPS. All other action is the same as for the TTF0 lead.</p>

TABLE D (Contd)

**INTERCONNECTION LEADS BETWEEN CARTRIDGE TAPE TRANSPORT CONTROLLER
AND CARTRIDGE TAPE TRANSPORT, DESIGNATION AND FUNCTION (FIG. 14)**

INTERCONNECTION LEADS	
DESIGNATION	FUNCTION
TTFR0 (Tape Transport Fast Reverse Search)	<p>When this lead is set to a 1, the CTT will move the tape in the reverse direction at 90 IPS until one of the following takes place:</p> <p>(a) Stop command is issued.</p> <p>(b) Beginning of Tape (BOT) marker is detected.</p> <p>After detecting BOT marker, the CTT will only accept a motion command which will move the tape in the forward direction.</p>
TTSR0 (Tape Transport Slow Reverse)	<p>When this lead is set to 1, the CTT will move the tape in the reverse direction at 30 IPS. All other action is the same as for the TTFR0 lead.</p>
TTSEL0 (Tape Transport Select)	<p>When this lead is set to a 0, all gating to or from the CTT is disabled. This also includes data transfer and status leads. The select lead acts as an inhibit to all inputs and outputs with the exception of manual operation enable. The data detect lead will be set to a 1 when this lead is a 1.</p>
TTREWCO (Tape Transport Rewind)	<p>When this lead is set to a 1, the CTT will move the tape in the reverse direction at 90 IPS until BOT is reached. The CTT stops the tape and then starts it again and proceeds at 30 IPS to load point (LP) and stops. The rewind sequence once started, inhibits all commands to the CTT except MTCE STOP until the rewind sequence has been completed. It also inhibits the write amplifiers and erase heads to ensure that no erroneous data or noise is accidentally written on the tape.</p>
MANENO (Manual Operation Enable)	<p>When this lead is set to a 1, the manual controls rewind, and unload switches (located on the front panel of the CTT) are enabled. This lead is enabled via a teletype command which removes the TDC unit from service.</p>
TTRDY0 (Tape Transport Ready)	<p>When this lead is set to a 1, it indicates that the cartridge is in place, initialization has been completed, the select input is a logic 1, and a rewind operation is not in progress.</p>
RWDINGA0 (Rewinding)	<p>When this lead is set to a 1, it indicates that the CTT is rewinding the tape. This rewind can be initiated by either a rewind command, pressing the rewind switch on the front panel of the transport, or insertion of a cartridge into the CTT.</p>
TOR0 (Tape Off Reel)	<p>When this lead is set to a 1, it indicates that the cartridge is in place but that the tape is broken or off one of the reels, or that one of the tape mark holes is aligned with the tape mark sensor in the CTT.</p>
TIMA0 (Tape in Motion)	<p>When this lead is set to a 1, it indicates that the tape is in motion; when zero, it indicates that the tape is not moving.</p>

TABLE D (Contd)

**INTERCONNECTION LEADS BETWEEN CARTRIDGE TAPE TRANSPORT CONTROLLER
AND CARTRIDGE TAPE TRANSPORT, DESIGNATION AND FUNCTION (FIG. 14)**

INTERCONNECTION LEADS	
DESIGNATION	FUNCTION
TTBOTO (Tape Transport Beginning of Tape)	When this lead is set to a 1, it indicates that the CTT heads are positioned between the BOT mark and the load point mark (Fig. 8).
TTEOTA0 (Tape Transport End of Tape)	When this lead is set to 1, it indicates that the CTT heads are positioned between the EOT mark and the early warning mark (Fig. 8).
LPEW0 (Load Point or Early Warning)	When this lead is set to 1, it indicates that the load point (LP) or early warning (EW) markers are crossing the sensors. This pulse is 0.5 microseconds in width. LP and EW are combined because the sensors cannot distinguish the difference between them.
CARTWE0 (Cartridge Write Enabled)	When this lead is set to a 1, it indicates that the cartridge in place is not write protected by the write protect plug.
TTINIT0 (Tape Transport Initialize)	When this lead is set to 1, it will cause the CTT to rewind the tape to the BOT and will stop and advance the tape to the load point and stop again. Upon stopping at the load point, the rewinding lead becomes 0 and the tape transport ready lead becomes a 1.
Power Leads	Refer to Part 5 for theory of operation for power and alarm circuits.

TABLE E

**INTERCONNECTION LEADS BETWEEN TAPE DATA CONTROLLER UNIT AND
SYNCHRONOUS DATA SET – DESIGNATION AND FUNCTION (FIG. 15)**

INTERCONNECTION LEADS	
DESIGNATION	FUNCTION
TRDN (Transmit Data)	This lead carries the serial data output of the on-line BUF to the SDS.
RDN (Receive Data)	This lead carries the serial data output of the SDS to the on-line BUF.
RTSP (Request to Send)	A signal on this lead is interpreted by the SDS as a request by the SDSC to transmit data.
CTS (Clear to Send)	A signal on this lead is in response to an RTS and indicates to the SDSC that it can transmit data over the TRD lead.
DSR (Data Set Ready)	A signal on this lead indicates to the SDSC that the SDS is connected and ready to communicate.
DTR (Data Terminal Ready)	A signal on this lead indicates to the SDS that the SDSC is connected and wants to communicate.
RC (Receive Clock Pulse)	This lead carries clock pulses from the SDS to the receive logic circuit (Fig. 28) in the SDSC. The leading edge of each clock pulse retriggers the monpulser. Therefore, when the clock pulse stops (at end of message), the monpulser times out and a reset pulse is generated to clear the receive mode.
TCP (Transmit Clock Pulse)	This lead carries clock pulses from the SDS to the transmit logic circuit (Fig. 28) in the SDSC. The transmit logic synchronizes the CTS indication and the TCP from the SDS with the data from the BUF. The transmit logic also generates the buffer shift pulse to clock the data out of the buffer circuit.
RNG (Ring Indicator)	A ringing current on the SDS telephone line will cause the RNG lead to go to the one state indicating that a call is present. No other logical function is performed within the SDSC.
DCD (Data Carrier Detect)	A carrier frequency on the SDS telephone line will cause the DCD lead to go to the one state, indicating that this frequency is present. RC is gated by this signal.
SG (Signal Ground)	This lead supplies a signal ground from the SDSC to the SDS.
FG (Frame Ground)	The TDC unit supplies the SDS with the frame ground over this lead.

TABLE F

SERIAL PERIPHERAL INTERFACE COMMANDS AND FUNCTIONS (FIG. 17)

OCTAL	COMMAND NOTE	FUNCTION
020	*SST (Send Status)	<p>This command returns to the 3A CC a 16-bit status word from the addressed device with correct parity over the information leads of the common parallel bus (Fig. 12).</p> <p><i>Note:</i> The 011 start code is normally returned. If there is an error in a device, the 101 start code is returned except by the bus terminator (BT) which always returns the 101 start code. If no device is addressed, the 3A CC does not get a reply.</p>
040	ACKI (Acknowledge Interrupt)	<p>This command identifies the device(s) which are requesting to interrupt the 3A CC. The ACKI command returns all zeros with correct parity and the normal start code (011). Also, if the buffer ready (BR) flag (bit 7 set to a 1) and the buffer interrupt are enabled (bit 9 set to a 0), the reply will be bit 1 set to a 1 and the normal start code (011). Refer to Table B for function of the ACKIO lead.</p>
100	INIT (Initialize)	<p>This command sends an initializing pulse to all devices (no device is addressed) connected to the SPI (Fig. 25).</p> <p><i>Note:</i> For the devices to respond to a command issued by the 3A CC, they must all start from a known state, thus the necessity of this command.</p> <p>Conditions that may set the devices to an unknown state are as follows:</p> <ul style="list-style-type: none"> (a) Application of power to the units. (b) A hit or noise pulse on the line. (c) A partial message being sent by the 3A CC.
200	*SD (Send Data)	<p>This command returns (over the information leads) to the 3A CC (from the off-line shift register) a 16-bit data word with correct parity and the normal start code (011). The bus terminator (BT) always responds with the 101 start code.</p> <p><i>Note:</i> If no device is addressed, the 3A CC will not get a reply.</p>
NONE	RD (Receive Data)	<p>This command is a 21-bit message from the 3A CC to the SPI, consisting of data, device address, and 011 start code. The 011 start code enables the RDO lead which directs the addressed device to receive data.</p>

* SST and SD will cause an addressed device to return a 16-bit status word or data word and normal start code (011) over the information leads of the common parallel bus.

TABLE F (Contd)

SERIAL PERIPHERAL INTERFACE COMMANDS AND FUNCTIONS (FIG. 17)

OCTAL	COMMAND NOTE	FUNCTION
NONE	RC (Receive Command)	This command is a 21-bit message from the 3A CC to the SPI, consisting of command, device address, and 101 start code. The 101 start code enables the RC0 lead which directs the addressed device to receive a command.
NONE	SPE (Serial Parity Error Reply)	The SPI returns (to the 3A CC) the reply shown in Fig. 17, format B to any 21-bit message which contained an odd number of ones. This indicates that an error was detected on a message between the 3A CC and SPI. The signal stops at the SPI and the reply is sent back immediately.

TABLE G

BUFFER COMMANDS AND FUNCTIONS (FIG. 18)

OCTAL	COMMAND NOTE	FUNCTION
0	BSTAT (Buffer Status)	This command is a no-operation command (Fig 18, Table A). The reply is the 16-bit status word shown on Fig. 18, Format B, with the 011 start code.
1	BCLRBRF (Clear Buffer Ready Flag)	This command resets the buffer ready flag (status bit 7 is set to 0), indicating the 3A CC has completed servicing the off-line buffer. BR set to a 1 is requesting that the 3A CC service the off-line buffer.
2 <i>Note:</i> Bits 10, 11, and 12 of command word are set to a 0. Bit 9 is set to a 1.	BSINTON (Buffer Set Interrupt On)	This command enables the BR flag (status bit 7 set to a 1) to allow a demand interrupt of the 3A CC over the INTPO lead (Fig. 12).
	BSINTOFF (Buffer Set Interrupt Off)	<i>Note:</i> Bits 10, 11, and 12 are load, unload, and stuff command bits, respectively (Fig. 18, Format A). This command inhibits the BR flag (status bit 7) to prevent a demand interrupt of the 3A CC.
2 <i>Note:</i> Bit 10 of command word is set to a 1.	BSLDON (Buffer Set Load State Interrupt On)	This command primes the buffer to accept 16-bit data words from the 3A CC via the intermediate transfer register (ITR) (Fig. 26).
	BSLDOFF (Buffer Set Load State Interrupt Off)	This command disables the interrupt by setting bit 9 to a 1 (Fig. 18, Format A).

TABLE G (Contd)

BUFFER COMMANDS AND FUNCTIONS (FIG. 18)

OCTAL	COMMAND NOTE	FUNCTION
2 <i>Note:</i> Bit 11 is set to a 1.	BSUNLDON (Buffer Set Unload State Interrupt On)	This command primes the buffer to respond to succeeding send data (SD) commands. The reply is the 16-bit status word shown in Fig. 18, Format B, with the 011 start code.
	BSUNLDOFF (Buffer Set Unload State Interrupt Off)	This command disables the interrupt by setting bit 9 to a 1 (Fig. 18, Format A).
2 <i>Note:</i> Bit 12 is set to a 1.	BSTFON (Buffer Set Stuff State Interrupt ON)	This command right-adjusts a partial message in the off-line shift register and increments the off-line shift register counter to the number of bits stuffed behind the partial message.
	BSTFOFF (Buffer Set Stuff State Interrupt Off)	This command disables the interrupt by setting bit 9 to a 1 (Fig. 18, Format A).
3	BFILL (Fill On-Line Buffer)	This command right-adjusts the on-line shift register. The fill function is performed in response to an associated device signal or command. The BR flag is set to a 1 upon completion of this operation indicating to the 3A CC that this is now the off-line BUF and ready for servicing.
4	Not Used	
5	BCLROCN (Buffer Clear The Off-Line Counter)	This command clears the counter (CNT0) associated with the off-line BUF (BUF0 in Fig. 26).
6	BSWB (Switch Buffers)	This command switches the position (on-line to off-line and vice versa) of the shift registers and their associated counters.
7	BINIT (Buffer Initialize)	This command resets the buffer unit and clears all counters. BUF 1 is set on-line; STUFF, FILL, LOAD, and UNLOAD states are reset to 0.

TABLE H

BUFFER STATUS REPLY FUNCTIONS (FIG. 18, FORMAT B)

BUFFER STATUS		
DESIGNATION	BIT	FUNCTION
PARITY HIGH (For Bits 15-8)	PH	This bit is set to a 1 to maintain odd parity. When at 0, it indicates that odd parity exists.
FILL (Fill State)	15	When this bit is set to a 1, it indicates to the 3A CC that the BUF unit is processing a fill on-line buffer command.
		This bit reset to 0 indicates that a fill operation is not in progress.
BOFL (Buffer Overflow)	14	When this bit is set to a 1, it indicates that the 3A CC did not service the last BR flag before the associated device filled or emptied the currently active shift register. This bit is set to a 1 at the trailing edge of the 1024th shift pulse of the on-line shift register if BR is set. <i>Note:</i> The shift registers will not toggle. Any further shift pulses from the associated devices are ignored.
		When this bit is reset to 0, it implies that the buffer is not overflowing.
1ACT (Active Buffer Number)	13	When this bit is set to a 1, it indicates to the 3A CC that BUF 1 is on-line (Fig. 26).
		When this bit is reset to a 0, it indicates to the 3A CC that BUF 0 is on-line (Fig. 26).
STUFF (Stuff State)	12	When this bit is set to a 1, it indicates to the 3A CC that the buffer unit is processing a stuff command.
		This bit reset to 0 indicates that a stuff command is not in progress.
UNLOAD (Unload State)	11	When this bit is set to a 1, it indicates to the 3A CC that the buffer unit has been primed with the set unload state command.
		This bit reset to 0 indicates that the set unload state is not active.
LOAD (Load State)	10	When this bit is set to a 1, it indicates to the 3A CC that the buffer unit has been primed with the set load state command.
		When this bit is reset to 0, it indicates that the load state is not active.

TABLE H (Contd)

BUFFER STATUS REPLY FUNCTIONS (FIG. 18, FORMAT B)

BUFFER STATUS		
DESIGNATION	BIT	FUNCTION
INTOFF (Interrupt Disabled)	9	When this bit is set to a 1, it indicates to the 3A CC that the demand interrupt capability of the buffer has been inhibited.
		When this bit is reset to 0, it enables the demand interrupt capability of the buffer.
RDY (Buffer Unit Ready)	8	When this bit is set to a 1, it indicates to the 3A CC that the buffer is not presently engaged in any operation on the off-line buffer and is ready to accept a command.
		<p>When this bit is set to a 0, it indicates to the 3A CC that the buffer unit is engaged in the following off-line operation:</p> <p>(a) The 3A CC sees this bit set to 0 on the status request reply (Fig. 18, Format B) being returned immediately following the stuff command and on all subsequent status replies until the stuff operation is completed.</p> <p>This bit is set to 0 whenever the ITR (Fig. 26) is being shifted as follows:</p> <p>(a) The 3A CC sees this bit set to 0 on the status request reply (Fig. 18, Format B) being returned immediately following the set unload command.</p> <p>(b) The 3A CC sees this bit set to 0 on the status request reply (Fig. 18, Format B) being returned immediately following each receive data command to the buffer.</p> <p>(c) The 3A CC may see this bit set to 0 in the reply of a status request sent by the 3A CC immediately following a send data command.</p>
PARITY LOW (For Bits 7-0)	P_L	This bit is set to a 1 to maintain odd parity. When at 0, it indicates that odd parity exists.
BR (Buffer Ready Flag)	7	When this bit is set to a 1, it indicates to the 3A CC that the last active shift register has been filled or emptied and placed off-line. Bit 9 (Interrupt Disabled) inhibits or enables this bit to demand interrupt the 3A CC.
		When this bit is set to a 0, it indicates to the 3A CC that the buffer unit is not ready for servicing.
PPE (Parallel Parity Error)	6	When this bit is set to a 1, it indicates to the 3A CC that the buffer unit detected a parity error on the last 16-bit data word received from the SPI and returns a 101 start code.
		When this bit is set to a 0, it indicates that data received from the SPI has correct parity.

TABLE H (Contd)

BUFFER STATUS REPLY FUNCTIONS (FIG. 18, FORMAT B)

BUFFER STATUS		
DESIGNATION	BIT	FUNCTION
Buffer Address Code	5	Bits 3, 1, and 0 are set to ones (001011), the 3-out-of-6 (3/6) code is address of the buffer. The address converted to octal is 13.
	4	
	3	
	2	
	1	
	0	
Buffer Status Reply Start Code	2	Bits 1 and 0 are set to ones (011) and indicates to the 3A CC that everything is alright in both the SPI and BUF.
	1	
	0	
	2	Bits 2 and 0 are set to ones (101) and indicates to the 3A CC that something abnormal has happened in either the SPI or BUF.
	1	
	0	

TABLE I

CARTRIDGE TAPE TRANSPORT CONTROLLER COMMANDS AND FUNCTIONS (FIG. 19, TABLE A)

	OCTAL	COMMAND	FUNCTION
BIT 7 IS SET TO A 0 FOR THESE CMDS	00	TSTOP (Tape Stop)	This command stops the tape. If the read head is crossing a data block (Fig. 8), the stop order will be issued at the next interblock gap (IBG). <i>Note:</i> The read/write heads will stop in an IBG of the addressed track from read/write speeds (30 IPS) unless the stop command is issued near the end of the IBG. The heads may not be in a gap if stopped from a fast speed (90 IPS) because of the coast time.
	01	TRWD (Tape Rewind)	This command moves the tape in the reverse direction (Fig. 8) at 90 IPS until BOT is reached and then stops, starts, and proceeds forward at 30 IPS to load point (LP) and stops. Whether initiated by software or manually, this command performs the same function. It also aborts any operation in progress (if any).
	02	TSCRC (Tape Shift CRC)	This command causes the 16 bits of the cyclic redundancy check character (CRCC) to be shifted from the check circuit to the BUF. After the CRC has been shifted, a fill on-line buffer command will be issued, and the CRC word will be right-adjusted to the beginning of the BUF, which will automatically switch off-line.
	03	TWIB1-TWIB4 (Tape Write IBG)	This command starts writing at 30 IPS in the forward direction on a preselected track (1 of 4), a magnetized gap. <i>Note:</i> This operation would normally be terminated by a tape stop command.
	04	TSTAT (Tape Secondary Status Request)	This command is issued when the status of the CTTC and tape is desired. Figure 20, Format B, shows various status conditions, and Table J provides a detailed explanation of the function of each.
	05	TFF1-TFF4 (Tape Fast Forward)	This command starts the tape moving in the forward direction at 90 IPS. Though the data is ignored, the data detect bit 11 (Fig. 20, Format B) constantly monitors the data blocks, and this may be utilized to count the number of blocks crossed on the selected track. <i>Note:</i> This operation would normally be terminated by a tape stop command.

TABLE I (Contd)

CARTRIDGE TAPE TRANSPORT CONTROLLER COMMANDS AND FUNCTIONS (FIG. 19, TABLE A)

	OCTAL	COMMAND	FUNCTION
BIT 7 IS SET TO A 0 FOR THESE CMDS	06	TWSTP (Tape Write Stop)	<p>This command enables the CTTC to stop a write operation at the end of the data coming from the current on-line shift register. The CTTC adds the postamble (Fig. 11), creates a portion of the IBG, and then stops the transport. Track address is not affected by this command, and write stop clears automatically following the sequence.</p> <p><i>Note:</i> The write stop command should only be used during a write operation.</p>
	07	TRB1-TRB4 (Tape Read a Block)	<p>This command reads one block of data from a preselected track (1/4). The transport will stop the read head in the IBG following the block being read. If the shift register being filled by the CTTC is not full at the end of the data block, a fill on-line buffer command will be issued (Table F, Octal 3). This command causes a right-adjust of that shift register so that it can be properly unloaded by the 3A CC.</p> <p><i>Note:</i> There is no indication that a fill operation has occurred, so the 3A CC has to know how much data was in that block or an end-of-file word (Fig. 11) should be used. A CRC check is done as data is transferred to the shift register. CRC error status can be checked at the end of the operation by issuing a buffer status command (Table F, Octal 0), and the status (Fig. 18, Format B) will be returned with the proper start code. Start code 011 indicates that the CRC check passed; and start code 101 indicates that the CRC check failed.</p>
	10	TMAINT (Set Maintenance)	<p>This command disables the CTT by deselecting it. In this mode, any command except rewind may be sent to the CTTC with the expectation of the right reply. Due to the transport being deselected, RDY will be set to 0 (not RDY). While in this mode, the reply from a rewind command will be that of a STOP.</p> <p><i>Note:</i> In this mode, the read, write, and CRC circuits may be exercised; and due to command replies being taken near the CTTC outputs, less a few gates, the CTTC may also be completely exercised.</p>
	11	TFR1-TFR4 (Tape Fast Reverse)	<p>This command moves the tape in the reverse direction at 90 IPS. Though the data is ignored, the data detect bit 11 (Fig. 20, Format B) constantly monitors the data blocks, and this may be utilized to count the number of blocks crossed (from BOT) on any one of the four tracks.</p> <p><i>Note:</i> This operation would normally be terminated by a tape stop command.</p>

TABLE I (Contd)

CARTRIDGE TAPE TRANSPORT CONTROLLER COMMANDS AND FUNCTIONS (FIG. 19, TABLE A)

	OCTAL	COMMAND	FUNCTION
BIT 7 IS SET TO A 0 FOR THESE CMDS	12	TCWS (Tape Write Stop)	This command resets the write stop flag and is generally used only in a maintenance situation to cancel a tape write stop command.
	13	TWT1-TWT4 (Tape Write)	<p>This command initiates the writing of one block of data on a preselected track. This data is phase encoded and is taken from the BUF registers.</p> <p>The CTTC generates and adds a preamble and postamble to the data block (Fig. 11). The preamble and postamble are deleted during a read operation. The end of data to be written is indicated by issuing a tape write stop command to the CTTC. This command causes a postamble to be generated and written on the tape following the end of data from the on-line shift register. It will also cause the transport to stop after writing a portion of the IBG. The write command initiates a read-after-write sequence within the CTTC during which the data being read back from the tape is compared to what is being written on the tape by the CRC circuit.</p>
	14	TCCRC (Tape Clear CRC)	<p>This command clears the CRC register.</p> <p><i>Note:</i> This command is functional only while in the maintenance mode.</p>
	15	TBS1-TBS4 (Tape Back Space)	<p>This command moves the tape in the reverse direction at 30 IPS across one data block (Fig. 8) on any track to an IBG.</p> <p>If the read head is sitting on a data block (ie, after a fast forward operation) when the command is issued, it will move the tape in the reverse direction at 30 IPS to the preceding IBG.</p>
	16	TCMTC (Tape Maintenance)	<p>This command clears or resets the maintenance and maintenance stop modes.</p> <p><i>Note:</i> This command should not be issued unless the CTTC is in the stop mode.</p>

TABLE I (Contd)

CARTRIDGE TAPE TRANSPORT CONTROLLER COMMANDS AND FUNCTIONS (FIG. 19, TABLE A)

	OCTAL	COMMAND	FUNCTION
BIT 7 IS SET TO A 0 FOR THESE CMDS	17	TRT1-TRT4 (Tape Read)	<p>This command initiates a continuous read operation from a preselected track until a stop command is issued.</p> <p>A CRC check is done as the data is transferred to the shift registers. A CRC error status may be checked during any IBG after a time elapse of 200 microseconds (into the IBG). By issuing a CTTC secondary status command (Fig. 19, Table A, Octal 04), the CTTC secondary status reply (Fig. 20, Format B) will be returned with the proper start code. Start code 011 indicates that the CRC check passed, and start code 101 indicates that the CRC check failed during the previous data block read.</p>
	00	TMSTOP (Set Maintenance Stop)	<p>This command functions as follows:</p> <ul style="list-style-type: none"> (a) Completely disables the transport. (b) Stops any operation in progress. (c) Motion commands will not be accepted by the transport. (d) Transport becomes deselected. (e) Ready will be set to 0 (not ready). (f) CTT circuit will go into the maintenance state. <p><i>Note:</i> This command may be cleared by issuing the general INIT command to the SPI, the tape reset maintenance command, or the tape transport initialize command.</p>
	16	TINIT (Tape Transport Initialize)	<p>This command clears all internal flags, and then a rewind operation is initiated.</p>

TABLE J

**CARTRIDGE TAPE TRANSPORT CONTROLLER SECONDARY STATUS REPLY MESSAGE
FUNCTIONS (FIG. 20, FORMAT B)**

		CTTC STATUS
DESIGNATION	BIT	FUNCTION
PARITY HIGH (For Bits 15-8)	P _H	This bit is set to a 1 to maintain odd parity; and when at 0, it indicates that odd parity exists.
MANEN (Transport Manuel Enabled)	15	When this bit is set to a 1, it indicates to the 3A CC that the CTT has been removed from service via a teletypewriter command, and the "rewind" and "unload" switches (located on the front panel of the CTT) are enabled.
		When this bit is reset to a 0, it indicates to the 3A CC that the "rewind" and "unload" switches (located on the front panel of the CTT) are inhibited.
LBOT (Logical Beginning of Tape)	14	When this bit is set to a 1, it indicates that the CTT heads are positioned in front of the LP tape mark (Fig. 8).
		This bit is reset to 0 at all other times.
REWINDING	13	When this bit is set to a 1, it indicates to the 3A CC that the CTT is in the process of rewinding the tape to the load point.
		This bit is reset to 0 at all other times.
MTCE MODE (Maintenance Mode)	12	When this bit is set to a 1, it indicates to the 3A CC that the CTTC is in the MTCE mode.
		When this bit is reset to a 0, it indicates to the 3A CC that the CTTC is in the normal operating mode.
DATA DETECT	11	When this bit is set to a 1, it indicates to the 3A CC that data (see data block, Fig. 8 and 11) is passing under the addressed read head winding or that the CTTC is in the MTCE mode.
		When this bit is reset to a 0, it indicates to the 3A CC that the addressed read head winding is crossing an interblock gap (IBG) or that the tape is not moving.
		<i>Note:</i> The data detect lead is a data monitor and shall be enabled whenever the transport is selected. By counting the transitions to the 1 state, the tape may be searched at 90 IPS in either direction (forward or reverse) and stopped with an accurate indication of the tape position.
TIM (Tape in Motion)	10	When this bit is set to a 1, it indicates to the 3A CC that the tape is in motion.
		When this bit is reset to a 0, it indicates to the 3A CC that the tape is not moving.

TABLE J (Contd)

**CARTRIDGE TAPE TRANSPORT CONTROLLER SECONDARY STATUS REPLY MESSAGE
FUNCTIONS (FIG. 20, FORMAT B)**

		CTTC STATUS
DESIGNATION	BIT	FUNCTION
TOR (Tape Off Reel)	9	When this bit is set to a 1, it indicates to the 3A CC that a cartridge is in place but the tape is broken, off one of the reels, or passing over a tape mark.
		When this bit is reset to a 0, it indicates to the 3A CC that the cartridge is in place and the tape is normal.
LEOT (Logical End of Tape)	8	When this bit is set to a 1, it indicates to the 3A CC that the CTT heads are between the EW and first EOT marks.
		This bit is reset to 0 at all other times.
PARITY LOW (For Bits 7-0)	PL	This bit is set to a 1 to maintain odd parity; and when at 0, it indicates that odd parity exists.
TTRDY (Tape Transport Ready)	7	When this bit is set to a 1, it indicates to the 3A CC that the cartridge is in place and initialization has taken place.
		When this bit is reset to a 0, it indicates to the 3A CC either that the cartridge is not in place, the CTTC is in the MTCE mode, or the tape is rewinding.
CARTWE (Cartridge Write Enabled)	6	When this bit is set to a 1, it indicates to the 3A CC that the write protect plug on the cartridge is in the nonsafe position.
		When this bit is reset to a 0, it indicates to the 3A CC that the write protect plug on the cartridge is in the safe position.
		<i>Note:</i> The No. 3 ESS requires that the write protect plug on the cartridge be in the nonsafe position for normal operation.
CTTC Address Code	5	Bits 3, 2, and 0 are set to ones (001101), the 3-out-of-6 address code of the CTTC device, or Octal 15. This address code is returned to the 3A CC to verify that the status returned is from the correct device.
	4	
	3	
	2	
	1	
	0	
CTTC Secondary Status Reply Start Code	2	When bits 1 and 0 are set to ones (011), this indicates to the 3A CC that the CTTC has not detected a CRC error on the preceding read or read-after-write operation.
	1	
	0	
	2	When bits 2 and 0 are set to ones (101), this indicates to the 3A CC that the CCTC has detected a CRC error and the CRC register is in a nonzero state.
	1	
	0	

TABLE K

SYNCHRONOUS DATA SET CONTROLLER COMMANDS AND FUNCTIONS (FIG. 21, FORMAT A)

OCTAL	COMMAND	FUNCTION
100	SDSC INIT (Initialize)	This command is an initializing pulse issued by the 3A CC to set SPI, BUF, and SDSC to a known state.
400	SDSC STATUS	This command returns to the 3A CC a 16-bit status word (Fig. 21, Format B) from the addressed device with correct parity over the information leads of the common parallel bus. (Fig. 28).
460	DTR (Data Terminal Ready)	This command loads the SDSC control register (Fig. 28) with the DTR bits shown on Fig. 21, Format A which indicates to the SDS that the 3A CC is prepared to establish a data link.
062	Set Receive State	This command loads the SDSC control register (Fig. 28) with the DTR and REC bits shown on Figure 21, Format A which indicates to the SDS that the 3A CC is prepared to establish a data link.
064	SET TRANSMIT STATE (Automatic Line Turn Around Off)	This command loads the SDSC control register (Fig. 28) with the DTR and request to send (RTS) bits indicating to the data set that the 3A CC wants to transmit data over the data link.
474	SET TRANSMIT STATE (Automatic Line Turn Around On)	This command loads the SDSC control register (Fig. 28) with the DTR, RTS, and action-on-buffer-end (ABE) bits. The ABE bit being set instructs the SDSC to switch to the REC state upon completion of the transmit sequence.
466	CLEAR ERROR STATE (Hold DTR Active)	Clears SDSC error state while allowing data line to stay up.

TABLE L

SYNCHRONOUS DATA SET CONTROLLER STATUS REPLY MESSAGE FUNCTIONS (FIG. 21, FORMAT B)

		SDSC STATUS
DESIGNATION	BIT	FUNCTION
PARITY HIGH (For Bits 15-8)	P _H	This bit is set to a 1 to maintain odd parity; and when at 0, it indicates that odd parity exists.
DCD (Data Carrier Detect)	15	When this bit is set to a 1, it indicates to the SDSC that a carrier signal is present at the SDS.
RNG (Ring)	14	When this bit is set to a 1, it indicates to the SDSC that a ringing signal is present at the SDS.
DSR (Data Set Ready)	13	When this bit is set to a 1, it indicates to the SDSC that the SDS is connected and ready to communicate with it.
DTR (Data Terminal Ready)	12	When this bit is set to a 1, it indicates to the SDS that the SDSC is connected and wants to communicate with it. Removal of this signal will hang up the phone line. <i>Note:</i> DTR is set and reset by a command from the 3A CC.
ABE (Action On Buffer End)	11	When this bit is set to a 1 (a command is issued by the 3A CC), it causes the SDSC to change from a transmit to a receive mode upon receipt of next BR (Table H, Bit 7).
RTS (Request to Send)	10	This bit is set to a 1 as long as the transmit flip-flop in the control register (Fig. 28) is set. An RTS signal asserts the request to send a signal to SDS which normally responds with a CTS signal. The RTS state can be terminated by: (a) A command from the 3A CC. (b) A coincidence of the ABE flip-flop being set and the 1024th pulse on the BACR0 lead from BUF.
REC (Receive)	9	When this bit is set to a 1, it indicates that the SDSC has been placed into the receive mode by a command from the 3A CC. The REC state can be terminated by: (a) A command from the 3A CC. (b) Sequential logic within the receive circuitry which detects an NMG or end of message (absence of the serial bit stream from the SDS).
CTS (Clear to Send)	8	When this bit is set to a 1, it is in response to an RTS and indicates that the SDS is ready to accept data.
PARITY LOW (For BITS 0-7)	P _L	This bit is set to a 1 to maintain odd parity; and when at 0, it indicates that odd parity exists.

TABLE L (Contd)

SYNCHRONOUS DATA SET CONTROLLER STATUS REPLY MESSAGE FUNCTIONS (FIG. 21, FORMAT B)

		SDSC STATUS
DESIGNATION	BIT	FUNCTION
NMSG (New Message)	7	When this bit is set to a 1, it indicates that SYNC has been set and the first NON-SYNC character has appeared in the serial bit stream from the SDS. This bit remains set as long as the REC state is set.
SYNC (Synchronization)	6	When this bit is set to a 1, it indicates that two or more consecutive SYNC characters have appeared in the serial bit stream from SDS. The REC bit must be set.
SDSC Address Code	5	Bits 3, 2, and 1 are set to ones (001110). The 3-out-of-6 (3/6) code is address of the SDSC. The address converted to octal is 16.
	4	
	3	
	2	
	1	
	0	
SDSC Status Reply Start Code	2	Bits 1 and 0 are set to ones (011) and indicates to the 3A CC that everything is alright in SPI, BUF, and SDSC.
	1	
	0	
	2	Bits 2 and 0 are set to ones (101) and indicates to the 3A CC that the BUF overflow bit 14 (Fig. 18, Format B) has been set to a 1.
	1	
	0	

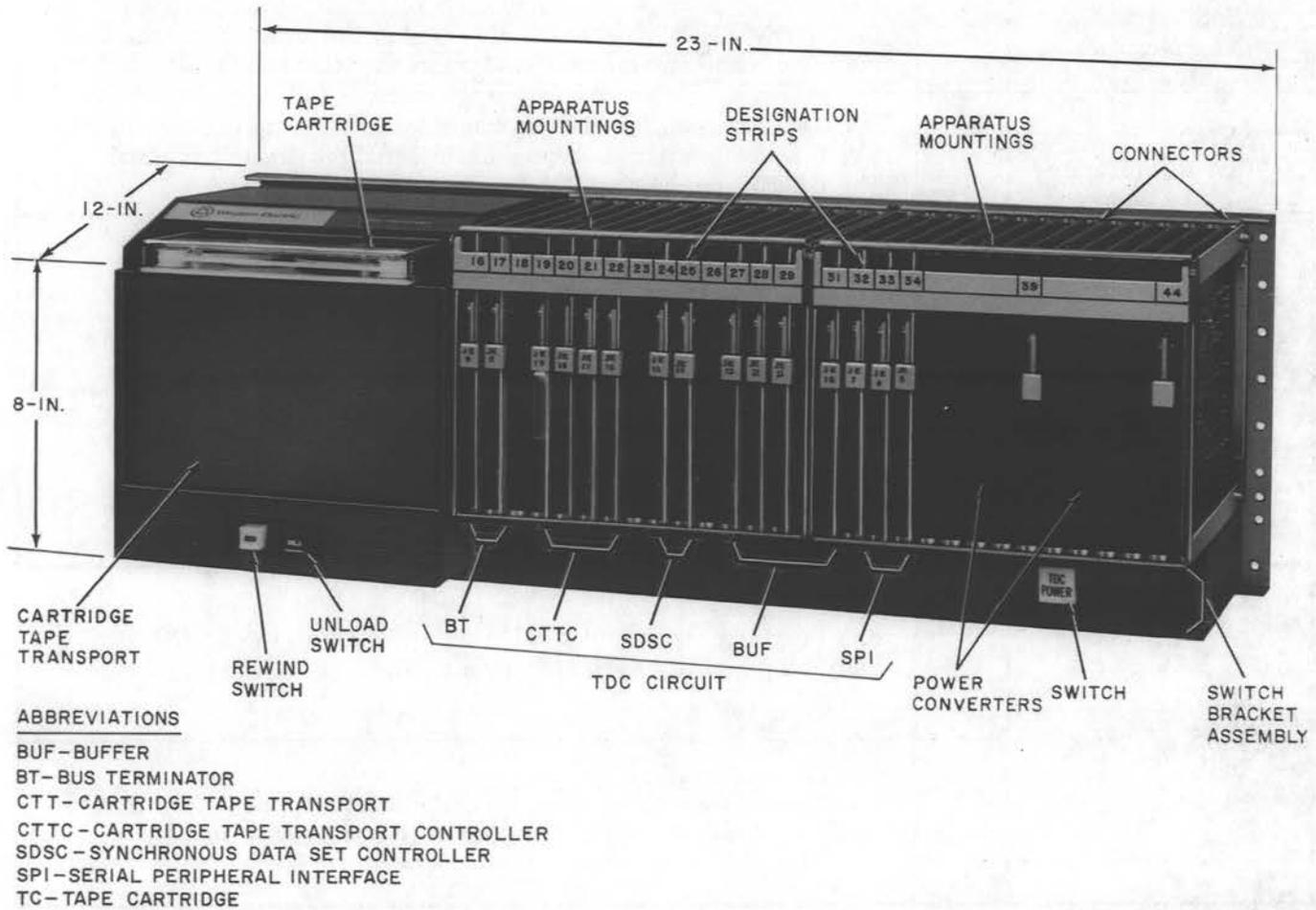
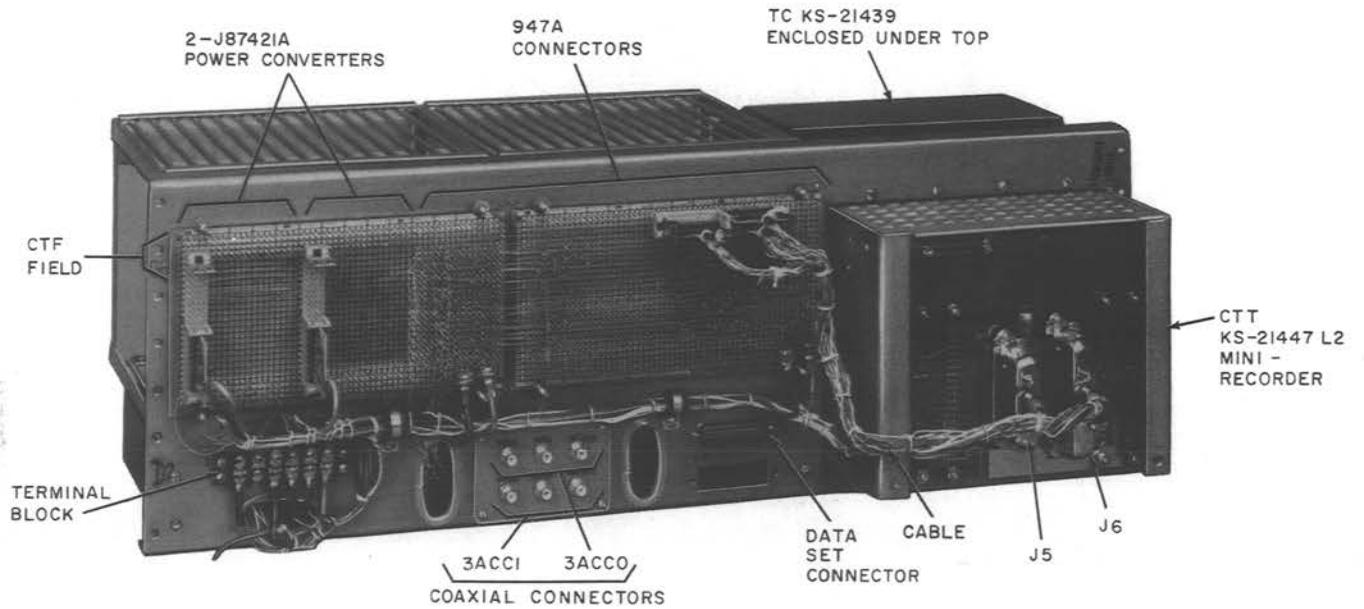


Fig. 1—Tape Data Controller Unit 0 or 1—J1C053A (Front View)



ABBREVIATIONS
 CTT-CARTRIDGE TAPE TRANSPORT
 TC-TAPE CARTRIDGE

Fig. 2—Tape Data Controller Unit 0 or 1—J1C053A (Rear View)

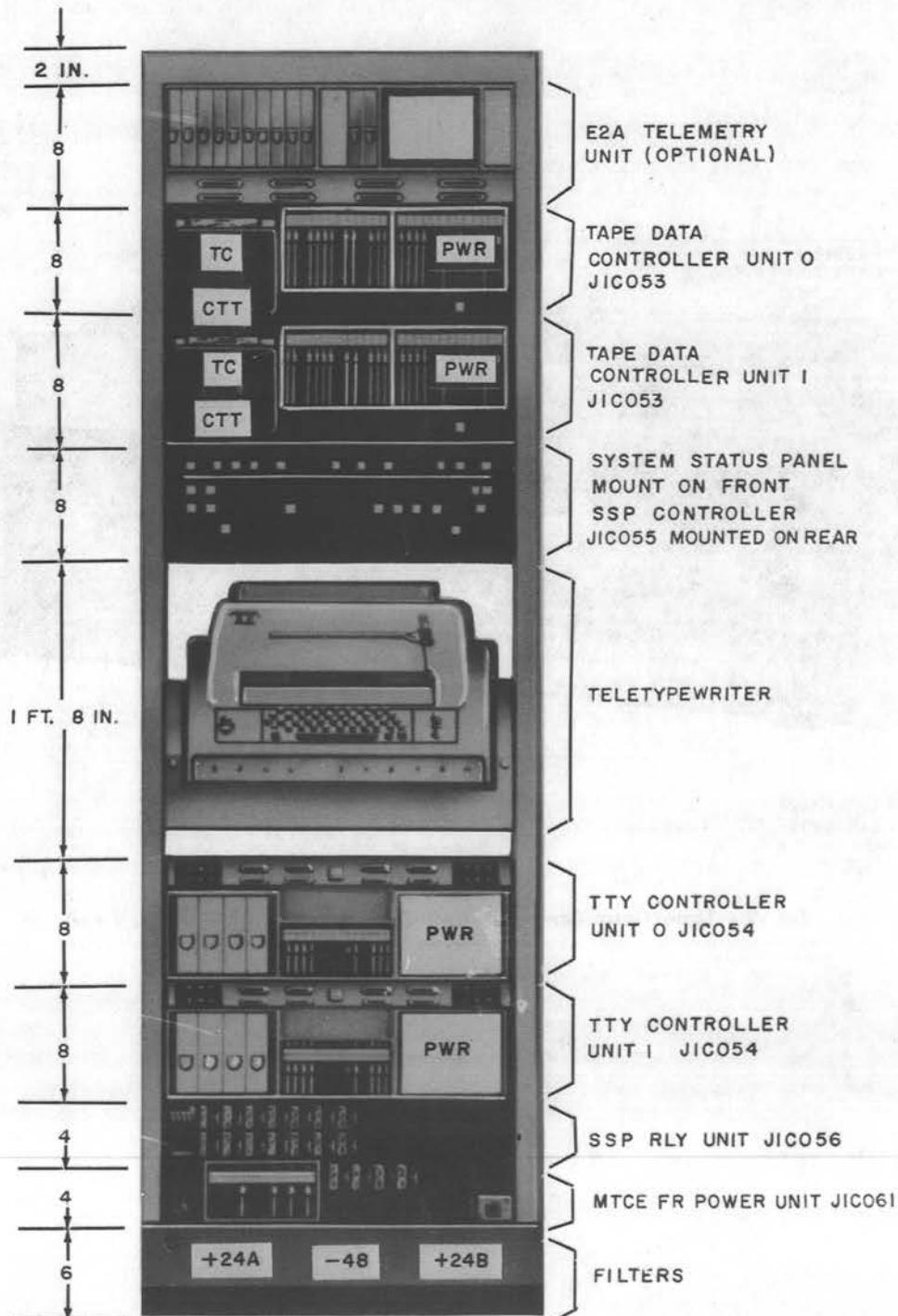
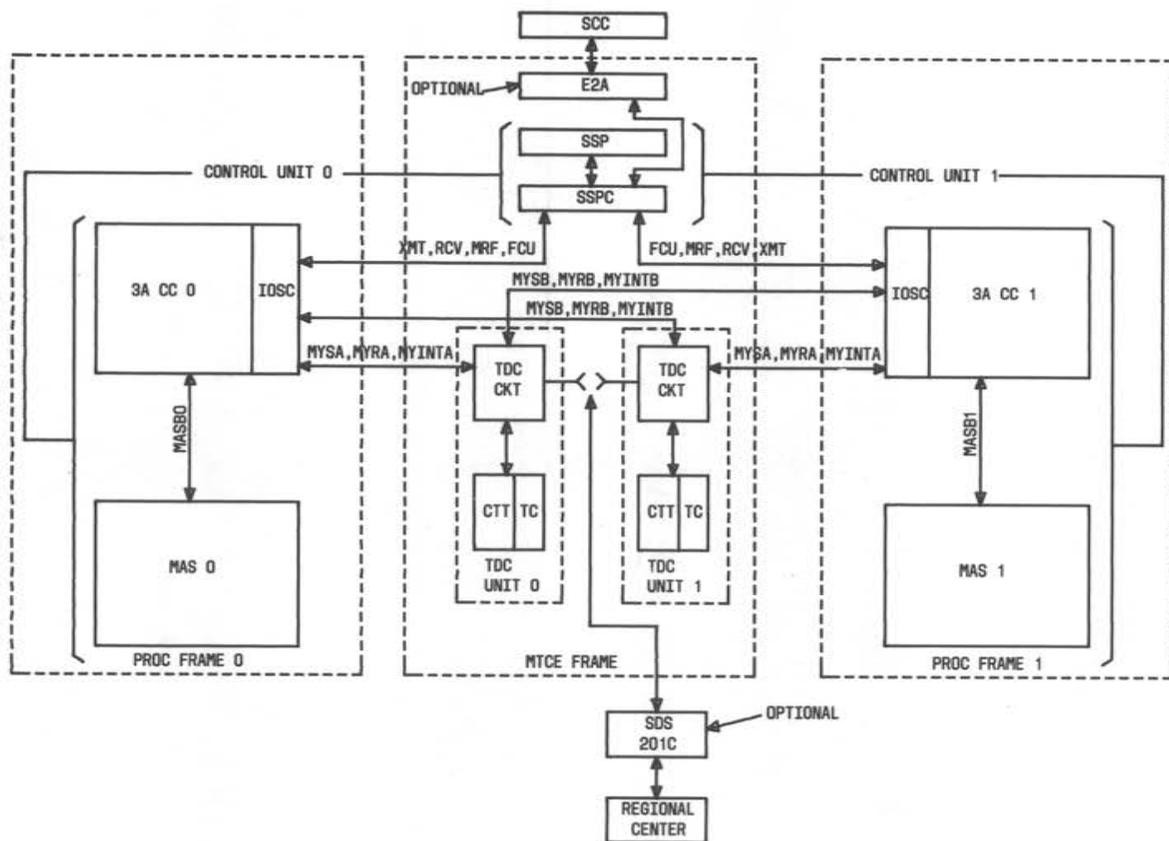


Fig. 3—Maintenance Frame—J1C060A (Front View)



- ABBREVIATIONS:
- CTT - CARTRIDGE TAPE TRANSPORT
 - FCU - FORCE ONE CONTROL UNIT ON-LINE AND THE OTHER OFF-LINE
 - E2A - TELEMETRY UNIT
 - IOISC - INPUT/OUTPUT SUBCHANNEL
 - MAS - MAIN STORE
 - MTCE - MAINTENANCE
 - MASB - MAIN STORE BUS
 - MRF - MAINTENANCE RESET FUNCTION
 - MY-A - INDICATES "A" TERMINALS OF TDC0 ASSOCIATED WITH 3A CC 0 AND TDC1 ASSOCIATED WITH 3A CC 1
 - MYINT - INTERRUPT
 - MYR - RECEIVE
 - MYS - SEND
 - PROC - PROCESSOR
 - RCV - RECEIVE
 - SCC - SWITCHING CONTROL CENTER
 - SDS - SYNCHRONOUS DATA SET
 - SSP - SYSTEM STATUS PANEL
 - SSPC - SYSTEM STATUS PANEL CONTROLLER
 - TC - TAPE CARTRIDGE
 - TDC - TAPE DATA CONTROLLER
 - XMT - TRANSMIT
 - 3A CC - 3A CENTRAL CONTROL

Fig. 4—Tape Data Controller Units 0 and 1—Interfaces

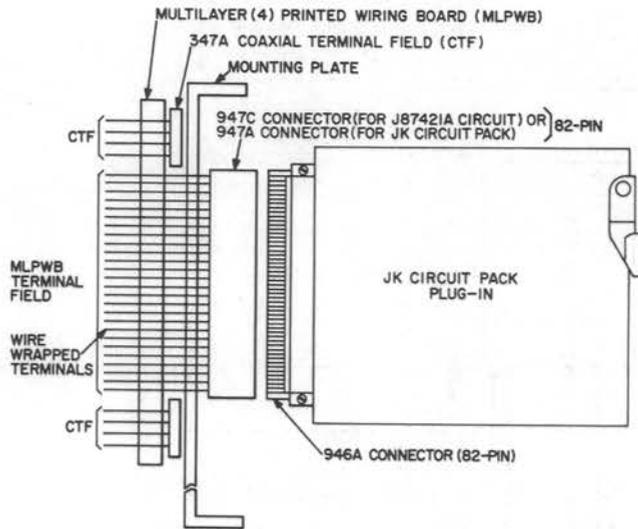


Fig. 5—Side View of TDC Unit, MLPWB Assembly, Associated Connectors, and Circuit Pack

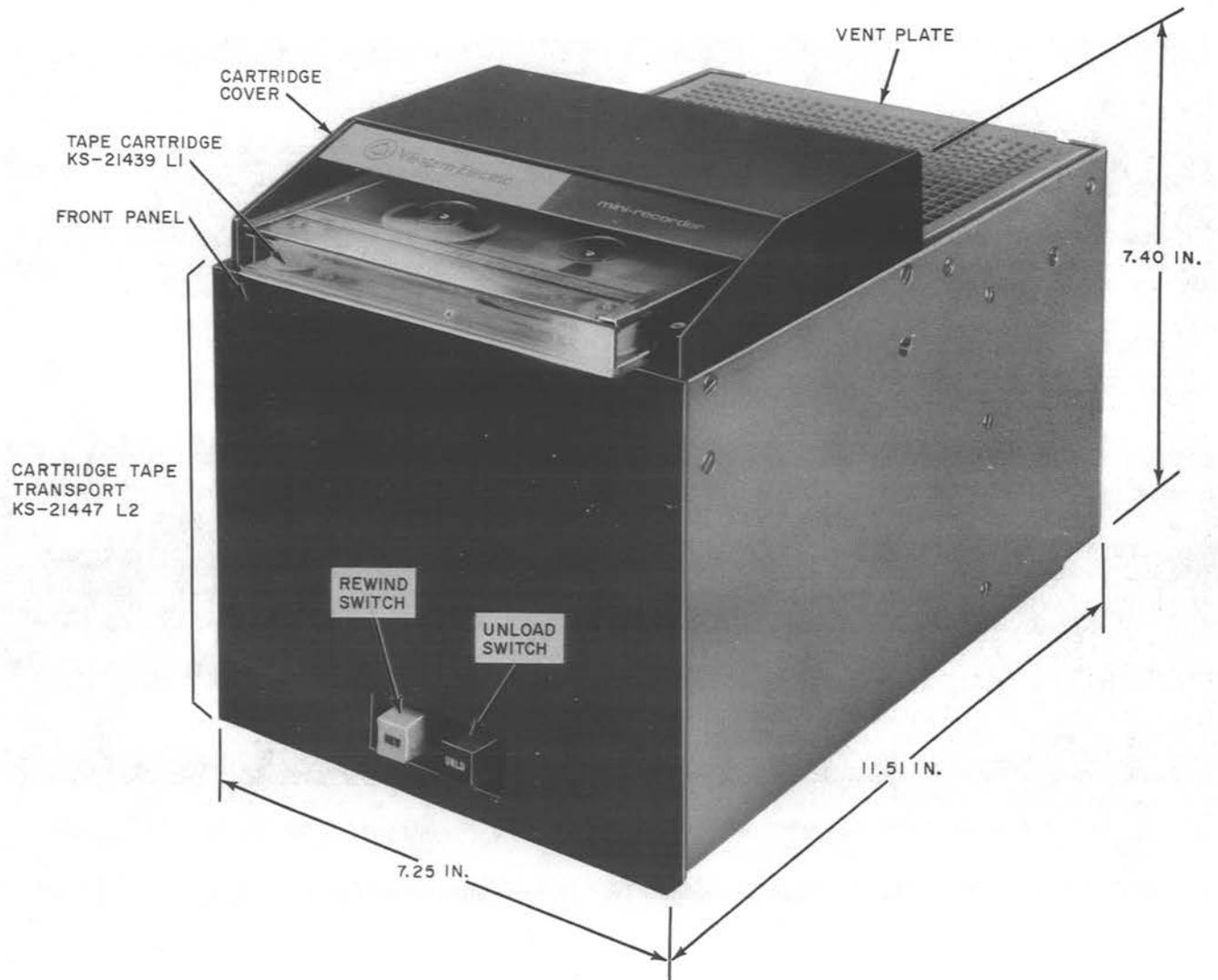


Fig. 6—Cartridge Tape Transport—KS-21447, L2 and Associated Tape Cartridge—KS-21439,L1 (Front View)

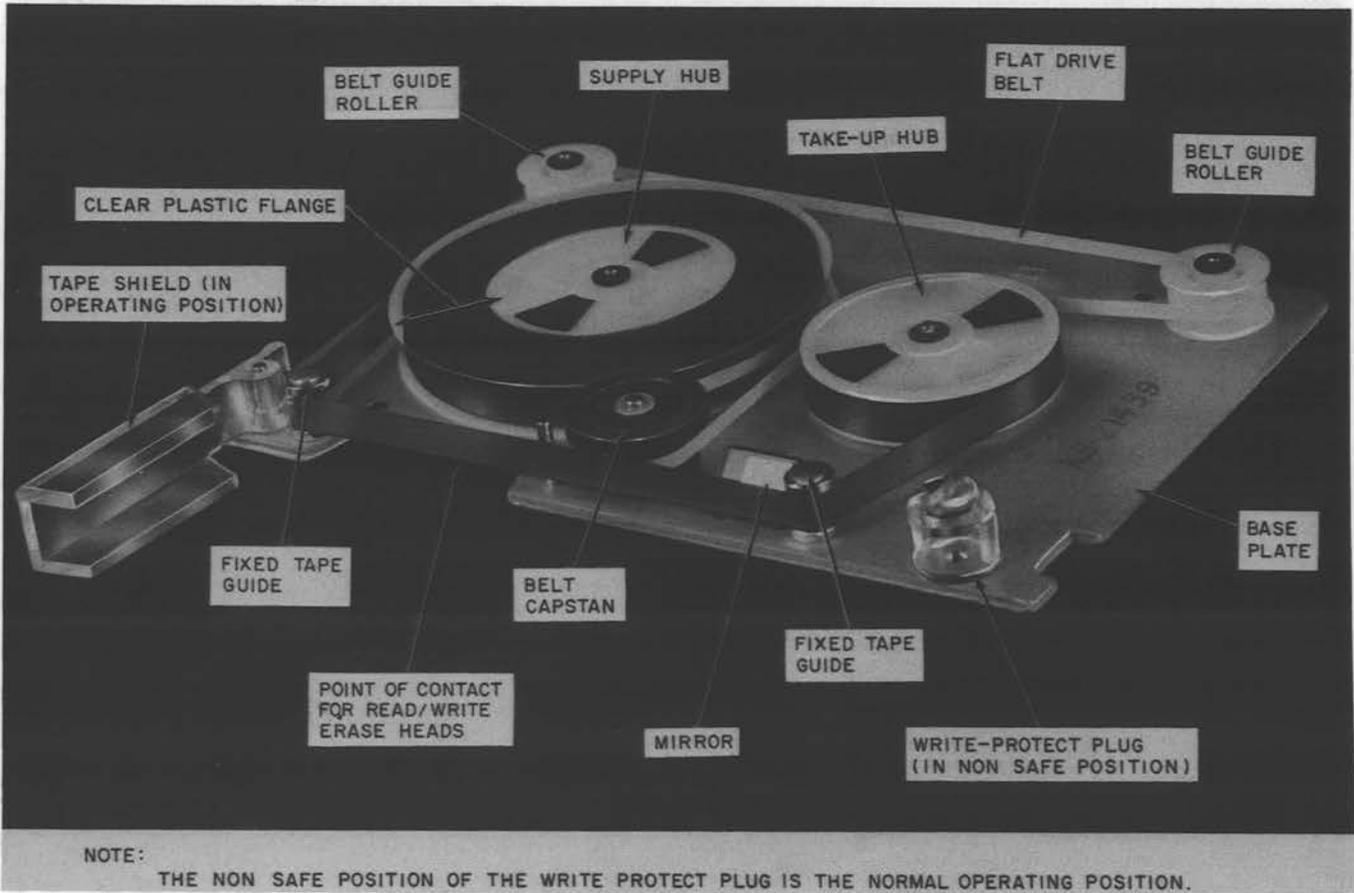


Fig. 7—Tape Cartridge—Less Transparent Plastic Cover

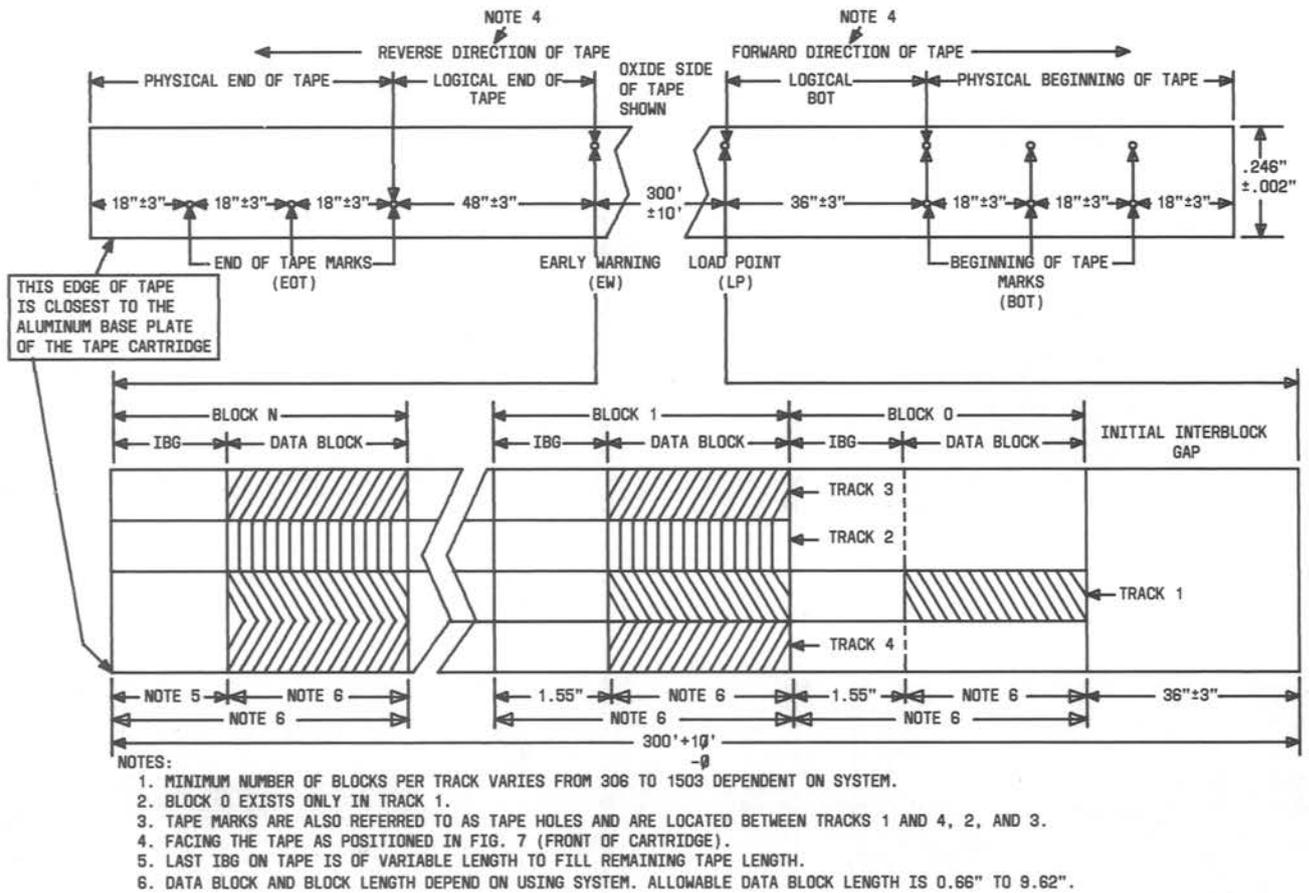


Fig. 8—Tape Cartridge—Tape Hole Pattern and Division of Blocks—Facing Front of Cartridge (Fig. 7)

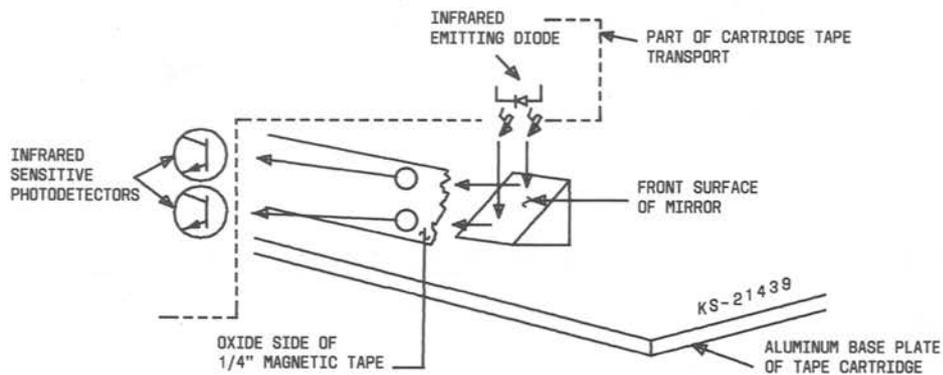
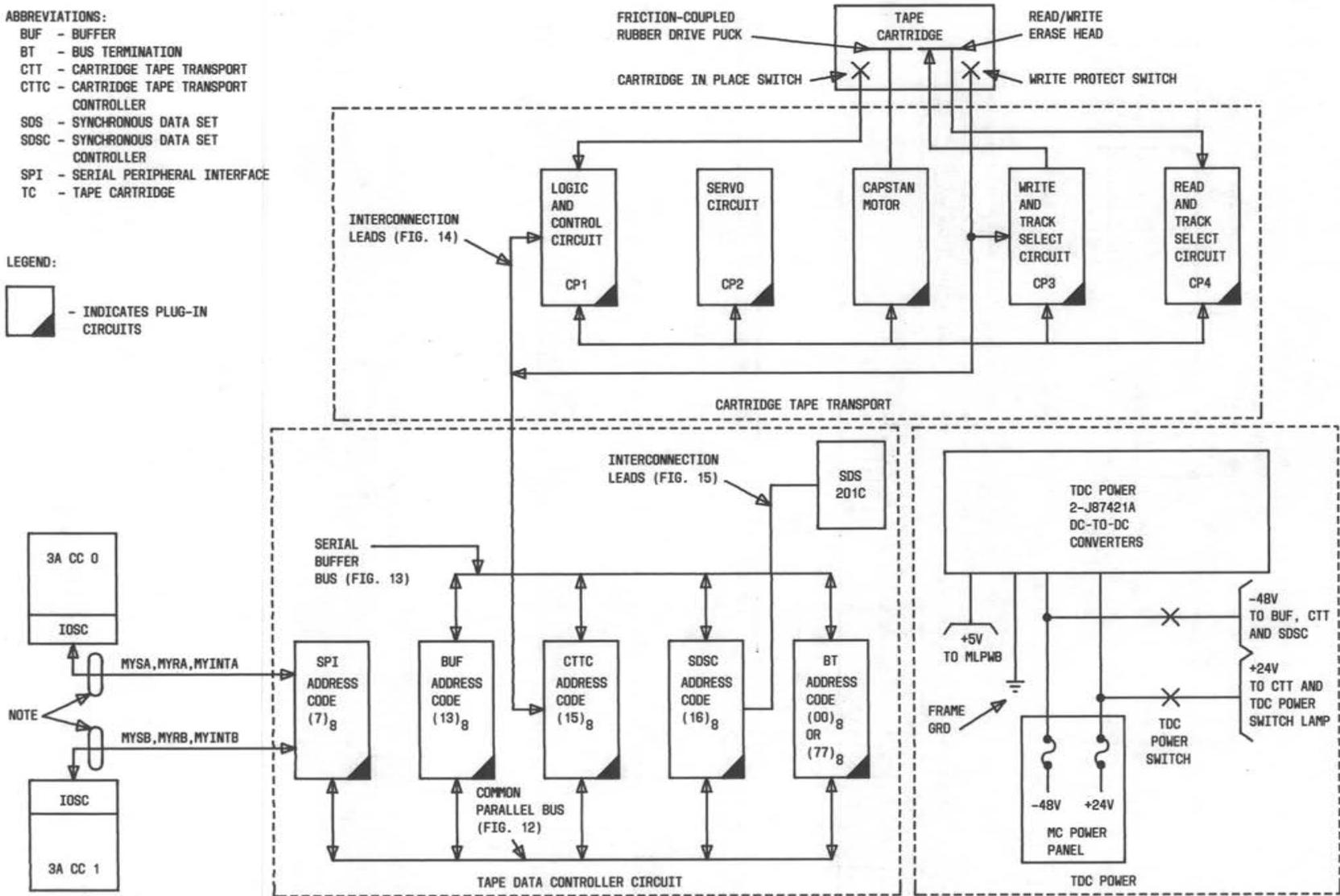


Fig. 9—Cartridge Tape Transport and Tape Cartridge Mark Detection

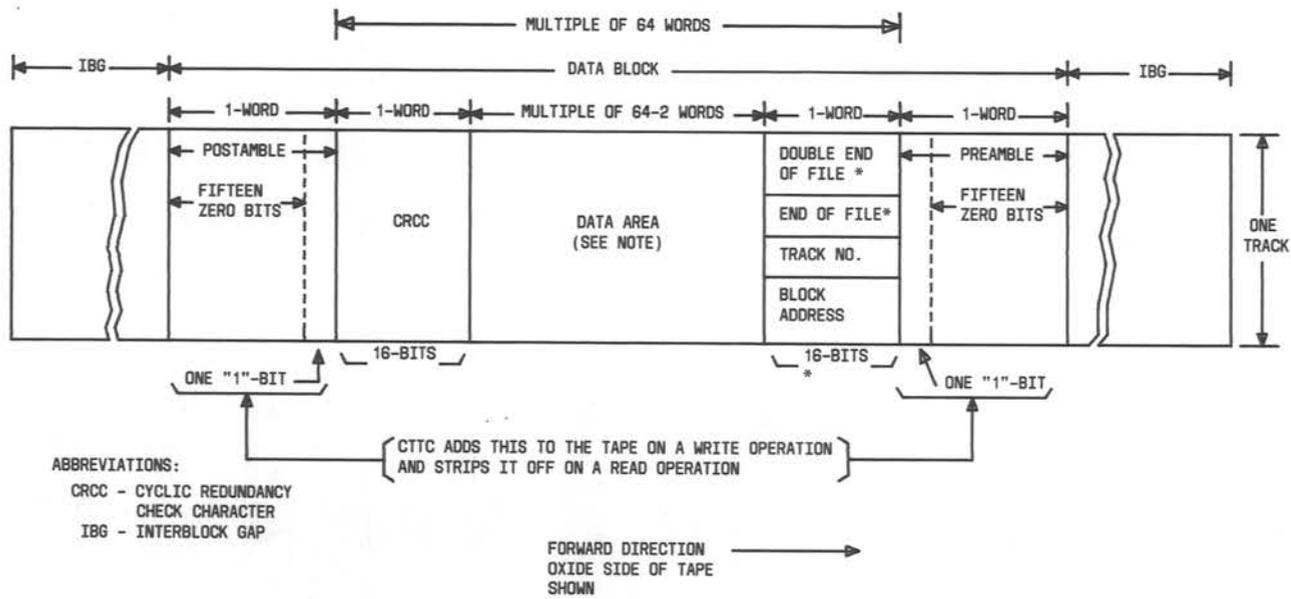
- ABBREVIATIONS:
- BUF - BUFFER
 - BT - BUS TERMINATION
 - CTT - CARTRIDGE TAPE TRANSPORT
 - CTTC - CARTRIDGE TAPE TRANSPORT CONTROLLER
 - SDS - SYNCHRONOUS DATA SET
 - SDSC - SYNCHRONOUS DATA SET CONTROLLER
 - SPI - SERIAL PERIPHERAL INTERFACE
 - TC - TAPE CARTRIDGE

- LEGEND:
-  - INDICATES PLUG-IN CIRCUITS



NOTE: THESE ARE SERIAL SUBCHANNEL BUSES EACH CONSISTING OF THREE COAXIAL CABLES EQUIPPED WITH TWO LEADS EACH (POSITIVE AND NEGATIVE) I.E., MYSAP AND MYSAN.

Fig. 10—Tape Data Controller Unit and Power—Functional Block Diagram

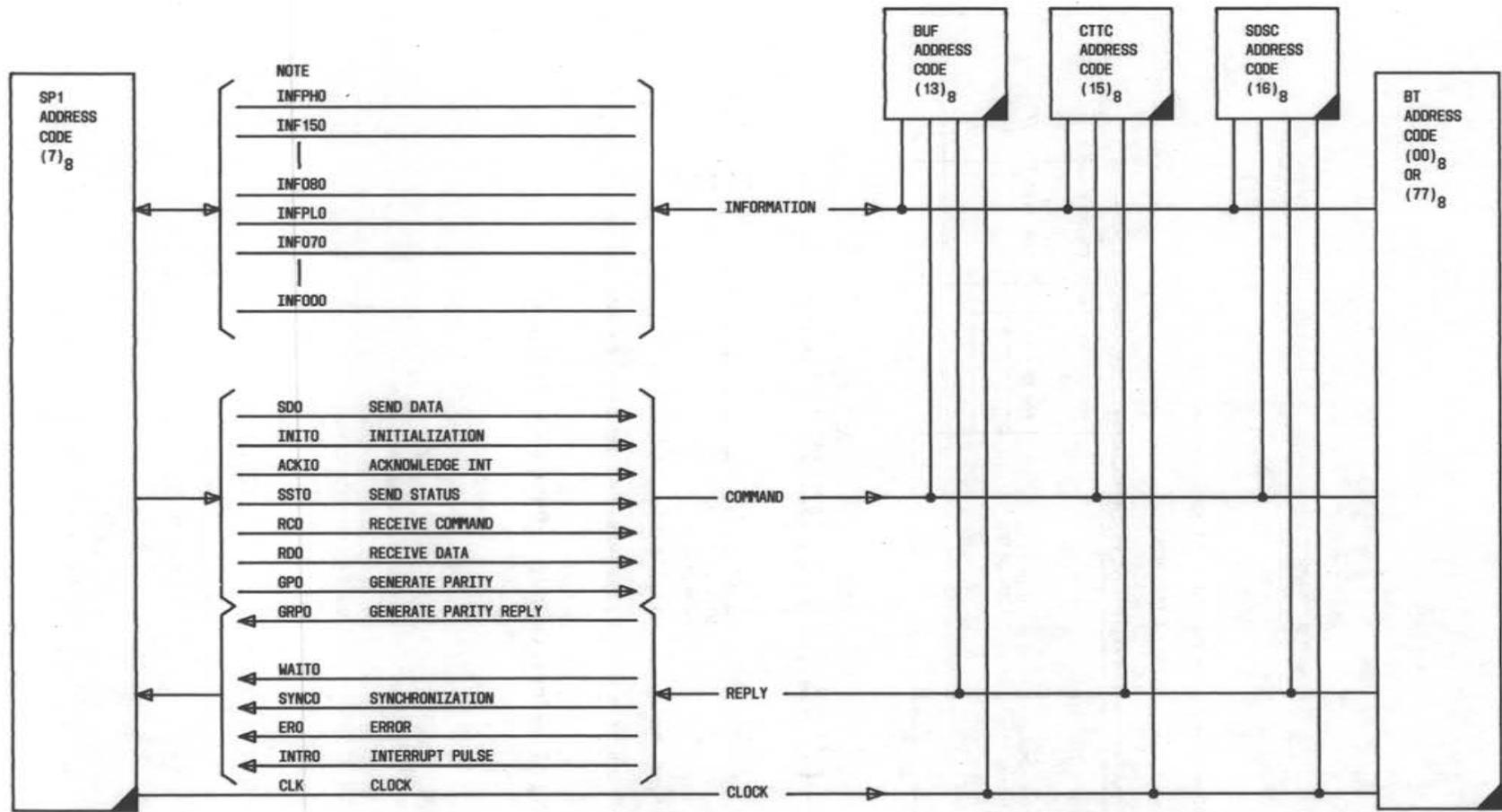


ABBREVIATIONS:
 CRCC - CYCLIC REDUNDANCY CHECK CHARACTER
 IBG - INTERBLOCK GAP

*IF THESE ARE USED, THEY WILL BE ASSIGNED, OTHERWISE THESE BITS ARE 16 ZEROS.

NOTE: NUMBER OF WORDS PER BLOCK IS VARIABLE DEPENDING ON THE USING SYSTEM, SEE PARAGRAPH 3.20

Fig. 11—Tape Cartridge—Data Block Assignments

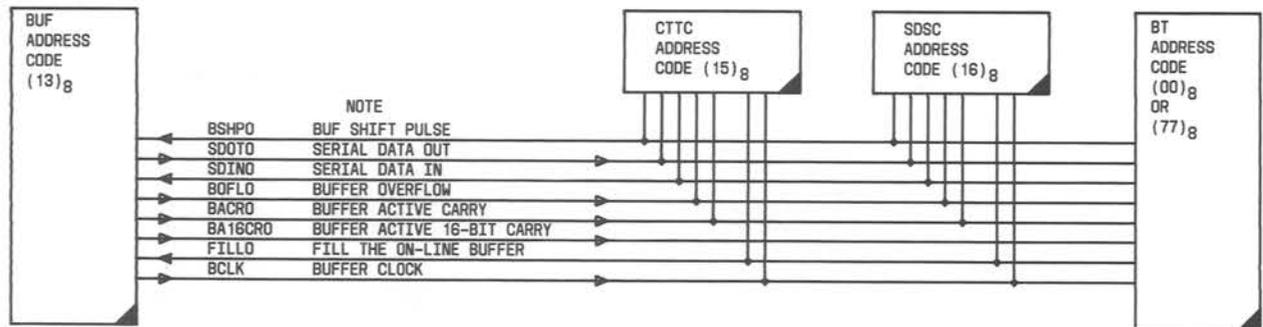


ABBREVIATIONS:
 BUF - BUFFERS
 BT - BUS TERMINATOR
 CTC - CARTRIDGE TAPE TRANSPORT CONTROLLER
 SDSC - SYNCHRONOUS DATA SET CONTROLLER
 SPI - SERIAL PERIPHERAL INTERFACE

LEGEND:
 - INDICATES PLUG-IN JK TYPE CIRCUIT PACKS

NOTE:
 REFER TO TABLE "B" FOR THE FUNCTION OF EACH COMMON PARALLEL BUS LEAD SHOWN.

Fig. 12—Common Parallel Bus Leads Tape Data Controller Circuit

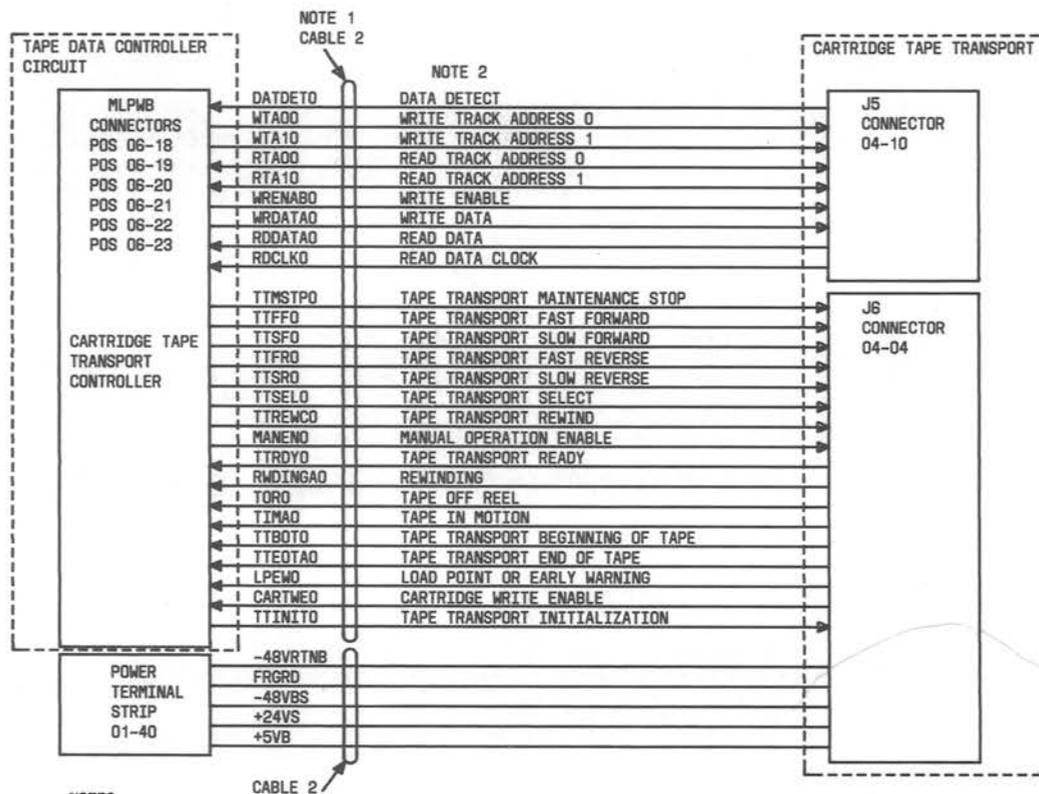


ABBREVIATIONS:
 BUF - BUFFER
 BT - BUS TERMINATOR
 CTTC - CARTRIDGE TAPE TRANSPORT CONTROLLER
 SDSC - SYNCHRONOUS DATA SET CONTROLLER

LEGEND
 -INDICATES PLUG-IN JK TYPE CIRCUIT PACKS

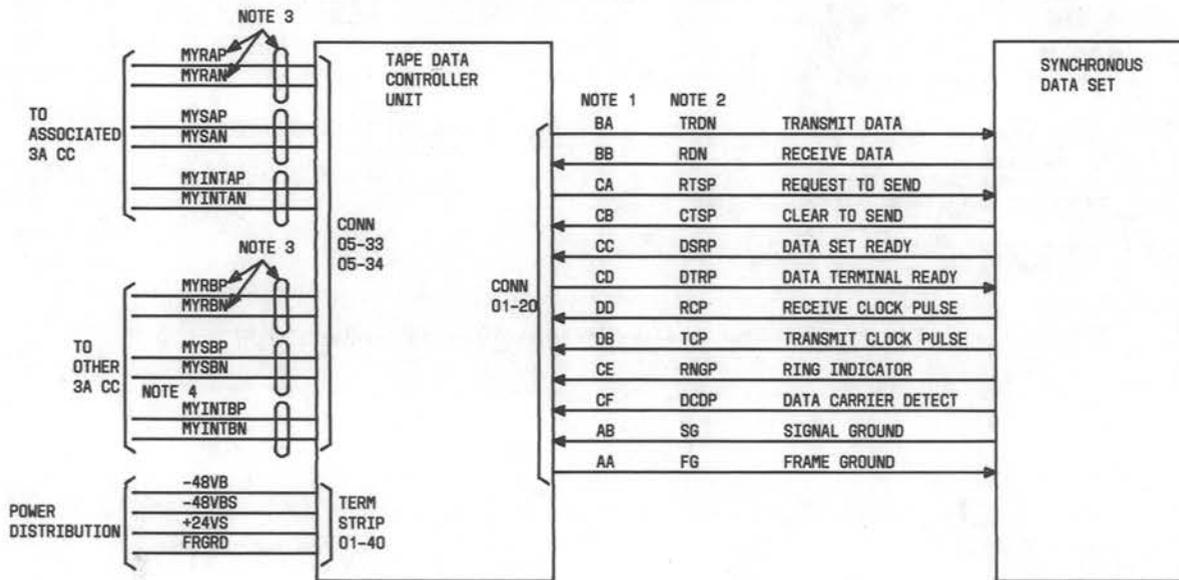
NOTE: REFER TO TABLE "C" FOR THE FUNCTION OF EACH SERIAL BUFFER BUS LEAD SHOWN.

Fig. 13—Serial Buffer Bus Leads Tape Data Controller Circuit



NOTES:
 1. EACH OF THESE LEADS IS PAIRED WITH A GROUND LEAD (NOT SHOWN) IDENTIFIED BY THE LETTER G, IE; DATDETOG.
 2. REFER TO TABLE "D" FOR THE FUNCTION OF EACH LEAD SHOWN.

Fig. 14—Interconnection Leads Between Cartridge Tape, Transport Controller, and Cartridge Tape Transport



NOTES:

1. ELECTRONIC INDUSTRIES ASSOCIATION (EIA) LEAD NAME.
2. LEAD ABBREVIATION, THE "P" INDICATES A PULSE AND "N" INDICATES NEGATIVE LOGIC.
3. THE "P" INDICATES POSITIVE AND THE "N" INDICATES NEGATIVE ON ALL OF THESE COAXIAL CABLE LEADS.
4. USE OF INTERRUPT LEADS IS OPTIONAL.

ABBREVIATIONS

- MY_A - INDICATES "A" TERMINALS OF TDC UNIT 0 ASSOCIATED WITH 3A CC 0 AND TDC UNIT 1 ASSOCIATED WITH 3A CC 1
- MYINT - INTERRUPT
- MYR - RECEIVE
- MYS - SEND

Fig. 15—Interconnection Leads Between Tape Data Controller Unit and Synchronous Data Set

NOTES:

1. PARITY HIGH (PH) BITS MAINTAIN ODD PARITY OVER BITS 8 THROUGH 15. PARITY LOW (PL) BITS MAINTAIN ODD PARITY OVER BITS 0 THROUGH 7.
2. AN ADDRESS CODE OF ALL ONES (OCTAL 77) OR ALL ZEROS (OCTAL 00) MAY BE USED TO ADDRESS THE BT UNIT FOR MAINTAINING THE BUS WITHIN THE TDC.
3. BIT ZERO OF THE START CODE IS THE LEAST SIGNIFICANT BIT POSITION OF THE 21-BIT MESSAGE.
4. BITS 0 THROUGH 15, PH AND PL RELATE TO INFORMATION LEADS INF000 THROUGH INF150, INFP00 AND INFP10, RESPECTIVELY (FIG. 12).
5. THE SPI "INIT COMMAND" IS ILLUSTRATED TO SHOW ITS BINARY CODE AND OCTAL TRANSLATION. THIS COMMAND SETS ALL DEVICES ATTACHED TO THE COMMON PARALLEL BUS TO A KNOWN STATE.

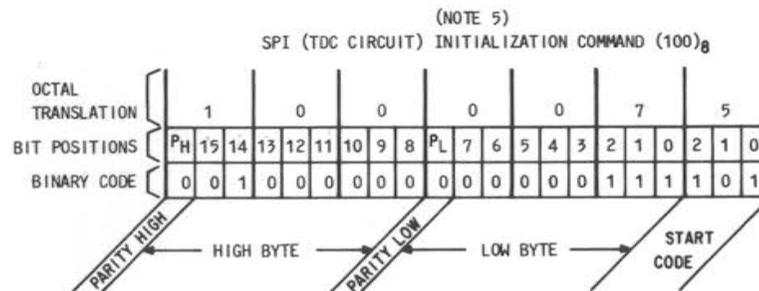
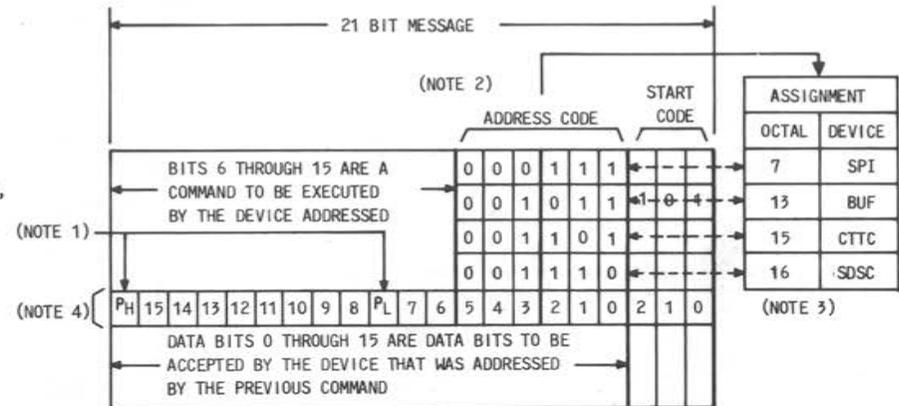


Fig. 16—21-Bit Message Format Used Between the 3A Central Control and Tape Data Controller Unit

TABLE A		
SPI COMMANDS (NOTE 1)		
OCT	COMMAND	START CODE
020	SEND STATUS (SST) (NOTE 2)	101
040	ACKNOWLEDGE INTERRUPT (ACKI)	101
100	INITIALIZATION (INIT)	101
200	SEND DATA (SD)	101
NONE	REC DATA (RD) (NOTE 3)	011
NONE	RECEIVE COMMAND (RC)(NOTE 4)	101

NOTES:

1. REFER TO TABLE 'F' FOR FUNCTION OF THESE COMMANDS.
2. AN SSI COMMAND 020 RETURNS (10 3A CC) NOTHING IF NO ERRORS EXIST, OR NO DEVICE IS ADDRESSED, BUT RETURNS THE 101 START CODE AND SPI DEVICE CODE (7)₈ IF AN SPE (EVEN NUMBER OF ONES) EXISTS.
3. THE RD COMMAND IS ENABLED BY THE 011 START CODE.
4. AN RC COMMAND IS ENABLED BY THE SPI WHEN IT DETERMINES THAT THE ADDRESS CODE IS FOR AN ASSOCIATED DEVICE.

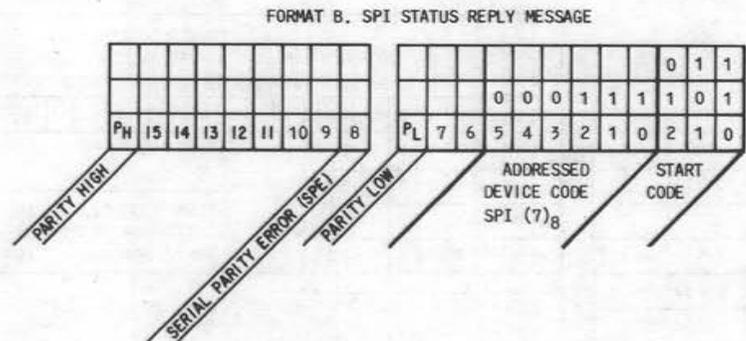
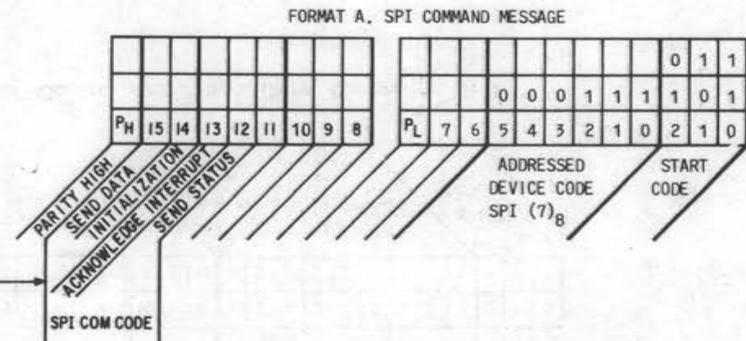


Fig. 17—Serial Peripheral Interface Commands and Reply Format

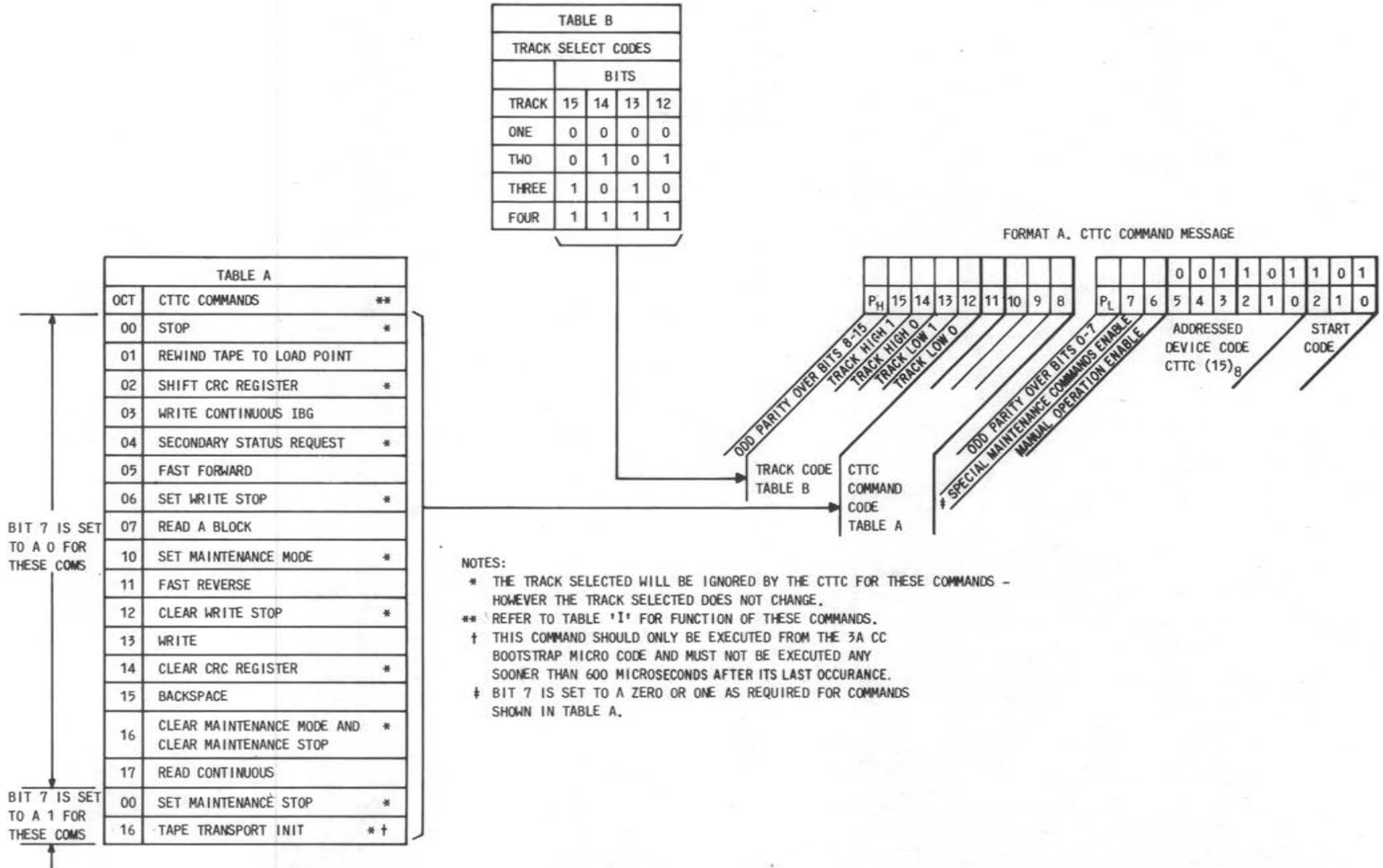


Fig. 19—Cartridge Tape Transport Controller Commands and Command Message Format

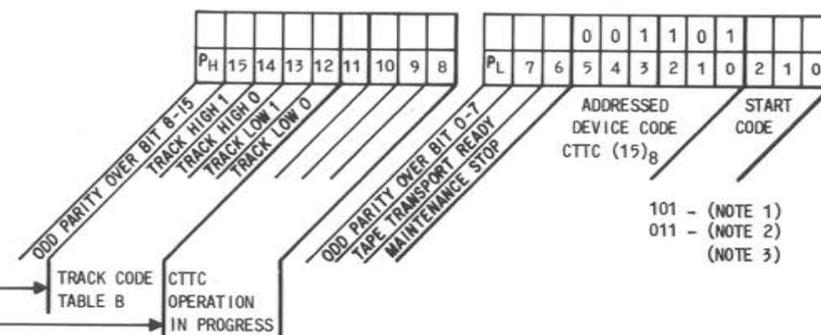
TABLE A	
OCT	OPERATION IN PROGRESS
00	STOPPED OR STOPPING
01	REWIND
02	NOT DEFINED
03	WRITE CONTINUOUS IBG
04	NOT DEFINED
05	FAST FORWARD
06	NOT DEFINED
07	READ-A-BLOCK
10	NOT DEFINED
11	FAST REVERSE
12	NOT DEFINED
13	WRITE
14	NOT DEFINED
15	BACKSPACE
16	NOT DEFINED
17	READ CONTINUOUS

TABLE B				
TRACK SELECT CODES				
	BITS			
TRACK	15	14	13	12
ONE	0	0	0	0
TWO	0	1	0	1
THREE	1	0	1	0
FOUR	1	1	1	1

NOTES:

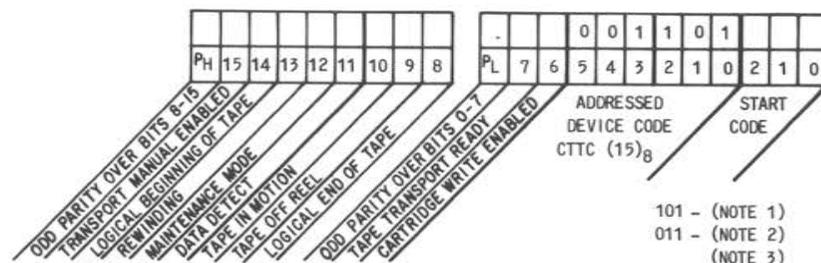
1. THE 101 START CODE INDICATES THAT A CRC ERROR WAS DETECTED.
2. THE 011 START CODE INDICATES THAT NO CRC ERROR WAS DETECTED OR A READ/WRITE OPERATION IS STILL IN PROGRESS.
3. BECAUSE OF THE TIME REQUIRED TO AUTOMATICALLY STRIP OFF THE POSTAMBLE FROM THE END OF THE DATA BLOCK AND PROPERLY FRAME THE 16 BIT DATA WORDS, THE OUTPUT FROM THE CRC CHECK CIRCUIT IS NOT ENABLED UNTIL AFTER A PERIOD OF UP TO 400 MICROSECONDS AFTER WHICH THE DATA DETECT STATUS BIT CHANGES TO A ZERO ON READ OR READ AFTER WRITE OPERATIONS.
4. REFER TO TABLES 'I' AND 'J' FOR FUNCTION OF EACH FORMAT.

FORMAT A. CTTC PRIMARY STATUS REPLY MESSAGE



101 - (NOTE 1)
011 - (NOTE 2)
(NOTE 3)

FORMAT B. CTTC SECONDARY STATUS REPLY MESSAGE



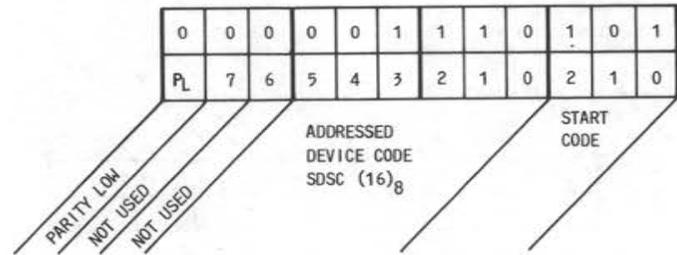
101 - (NOTE 1)
011 - (NOTE 2)
(NOTE 3)

Fig. 20—Cartridge Tape Transport Controller Primary and Secondary Status Reply Message

FORMAT A. SDSC COMMAND MESSAGE

TABLE A		SDSC COMMANDS (NOTES 1, 3)								
OCT	COMMANDS	P _H	15	14	13	12	11	10	9	8
100	SDSC INIT			1						
400	SDSC STATUS	1								
460	DATA TERMINAL READY	1			1	1				
062	SET REC STATE				1	1			1	
064	SET TRN STATE(AUTOMATIC LINE TURN AROUND OFF)				1	1		1		
474	SET TRN STATE(AUTOMATIC LINE TURN AROUND ON)	1			1	1	1	1		
466	CLR ERR STATE (KEEP LINE UP)	1			1	1		1	1	

SDSC COMMAND CODES (NOTE 4)



NOTES:

1. REFER TO TABLE 'K' FOR FUNCTION OF THESE COMMANDS.
2. REFER TO TABLE 'L' FOR FUNCTION OF EACH STATUS.
3. 101 IS THE START CODE FOR ALL OF THESE COMMANDS.
4. BITS THAT ARE NOT USED ARE ALWAYS SET TO ZERO.

ABBREVIATIONS

- INIT - INITIALIZATION
- REC - RECEIVE
- SDSC - SYNCHRONOUS DATA SET CONTROLLER
- TRN - TRANSMIT

FORMAT B. SDSC STATUS REPLY MESSAGE

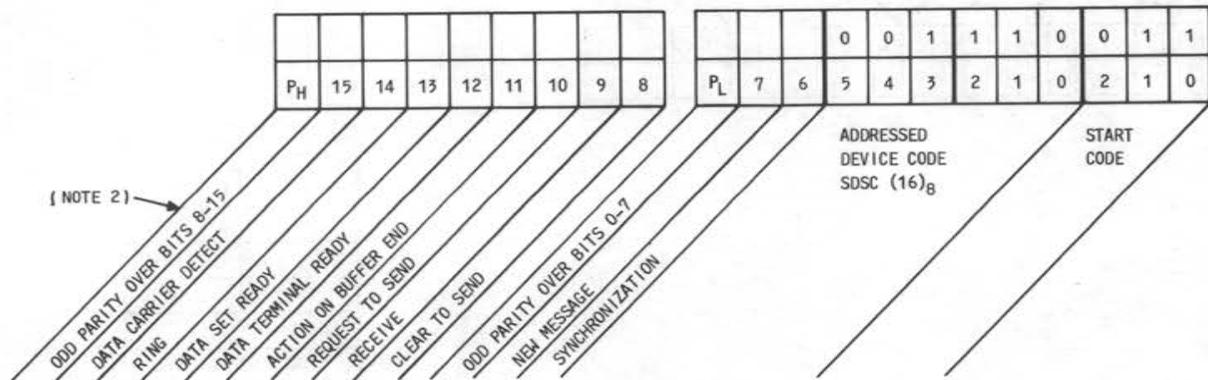


Fig. 21—SDSC Commands and Reply Format

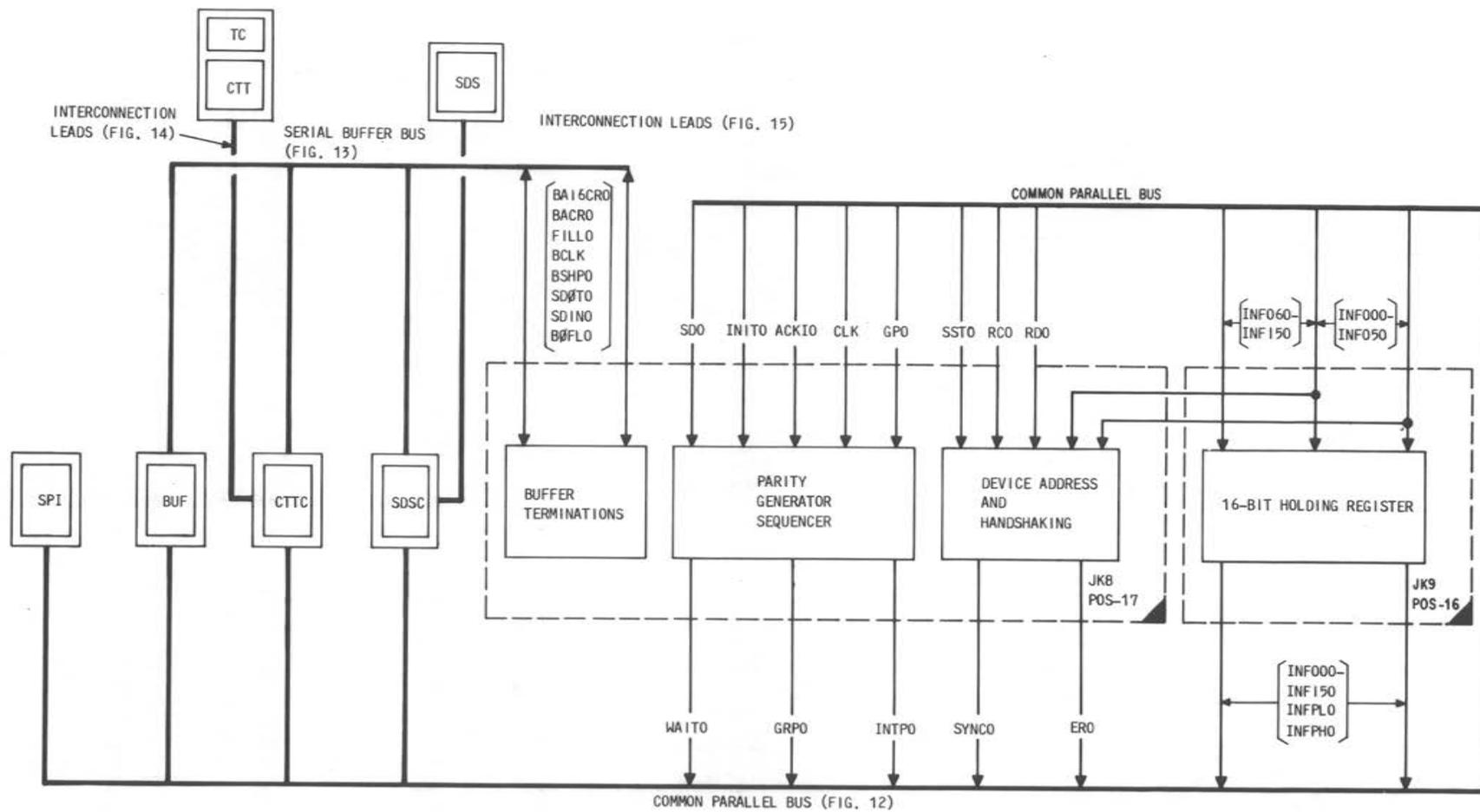


Fig. 22—Bus Terminator—Terminating Serial Buffer Bus and Common Parallel Bus—Functional Block Diagram

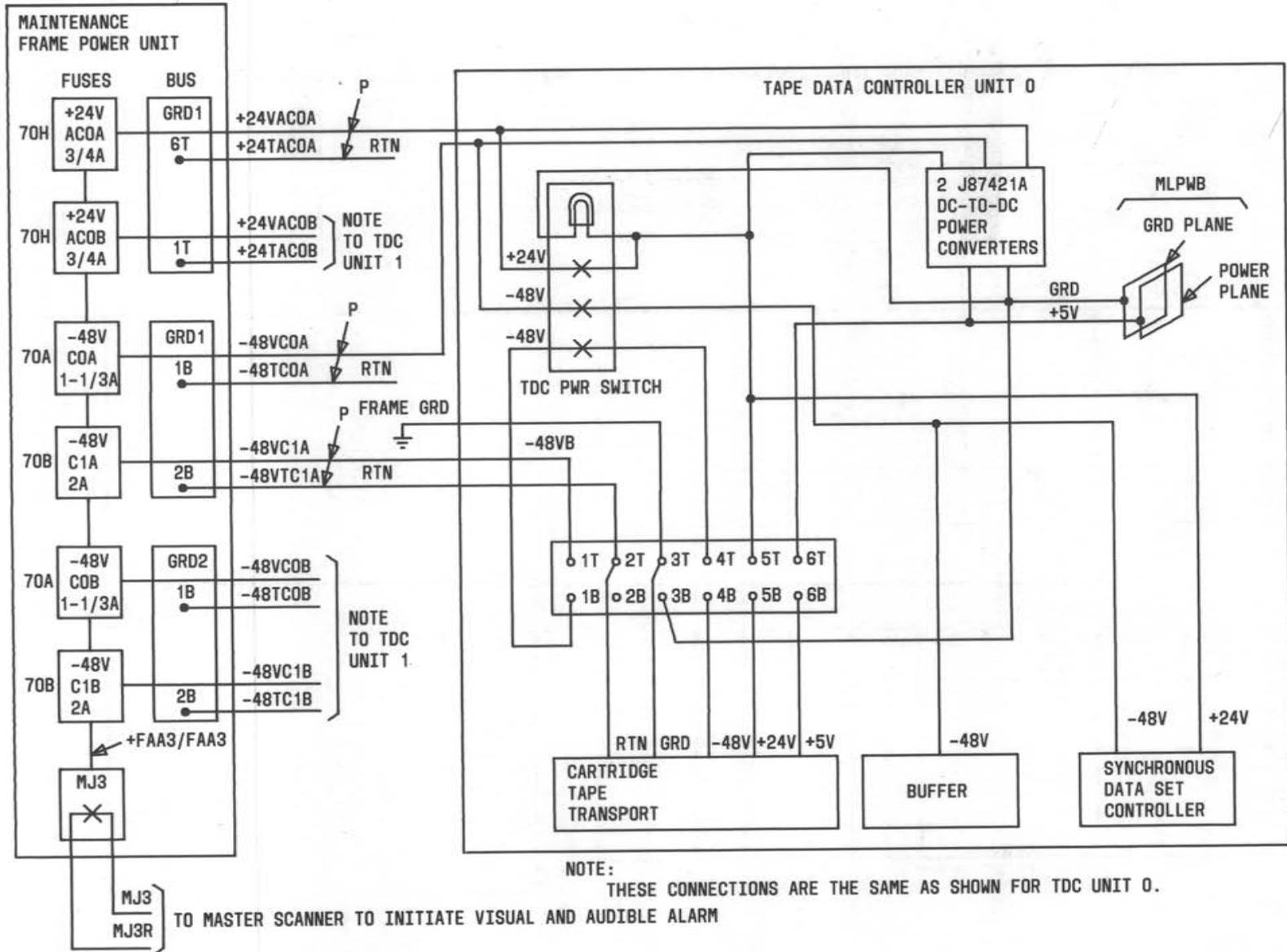


Fig. 23—Tape Data Controller Unit Power

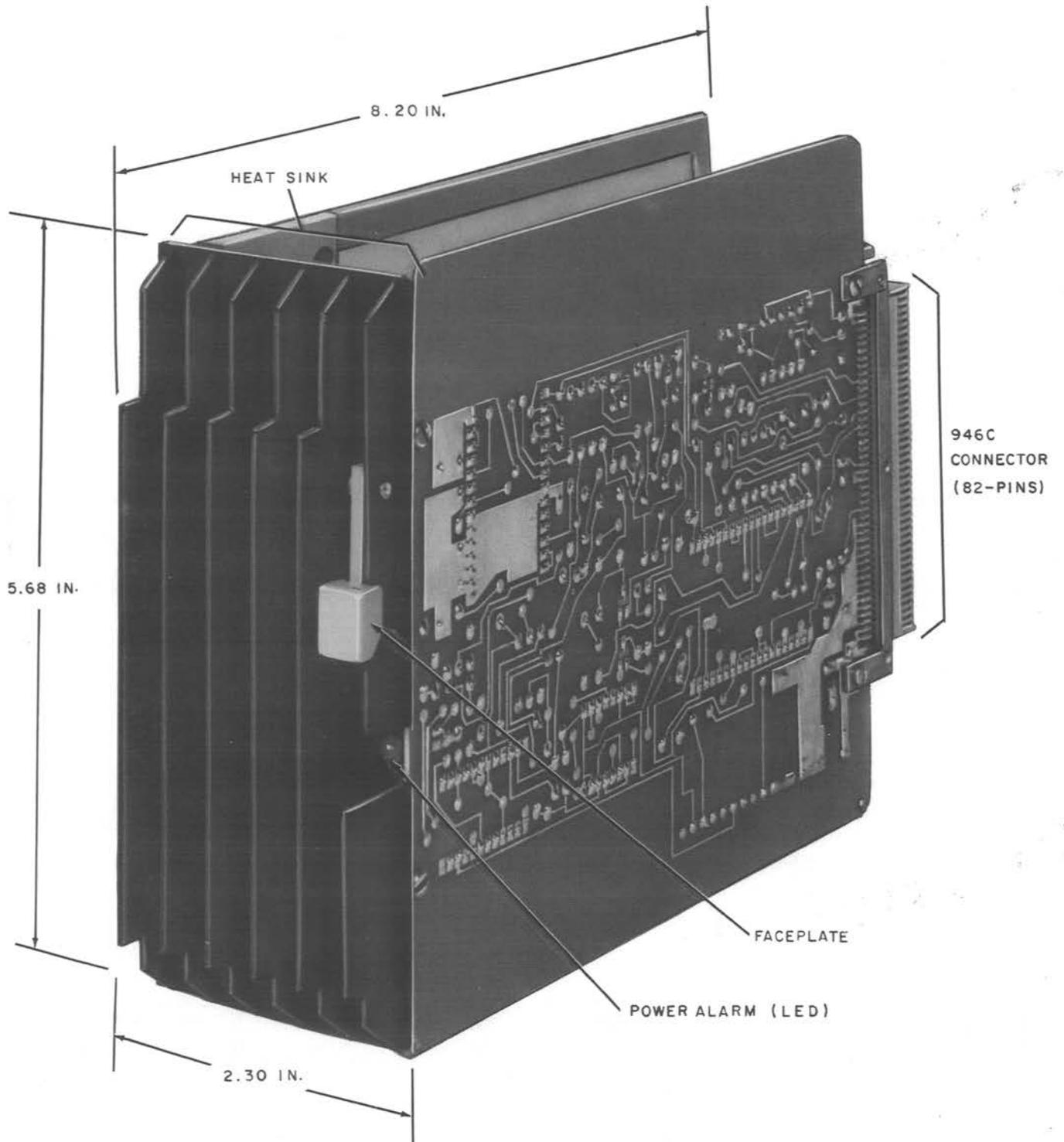


Fig. 24—Power Converter—J87421A

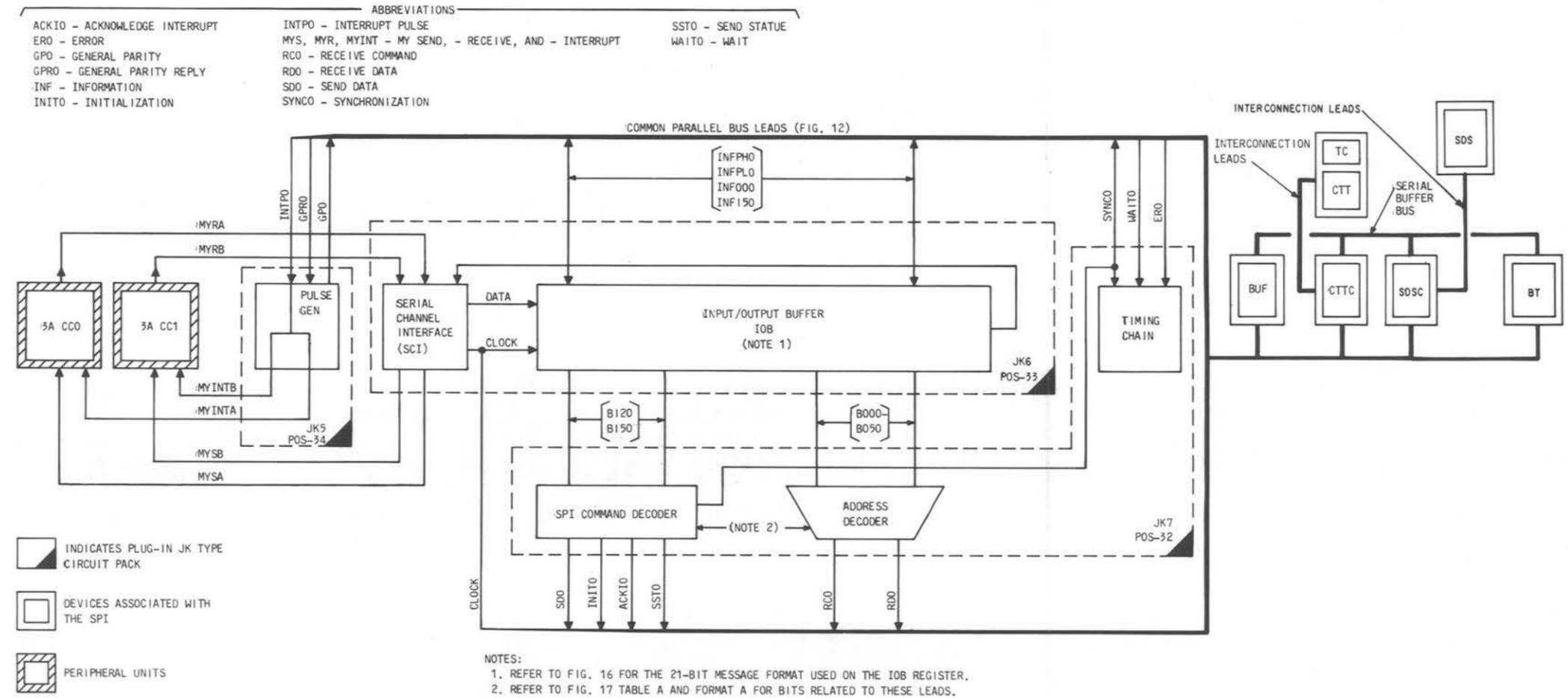


Fig. 25—Serial Peripheral Interface Between 3A CC and Common Parallel Bus—Functional Block Diagram

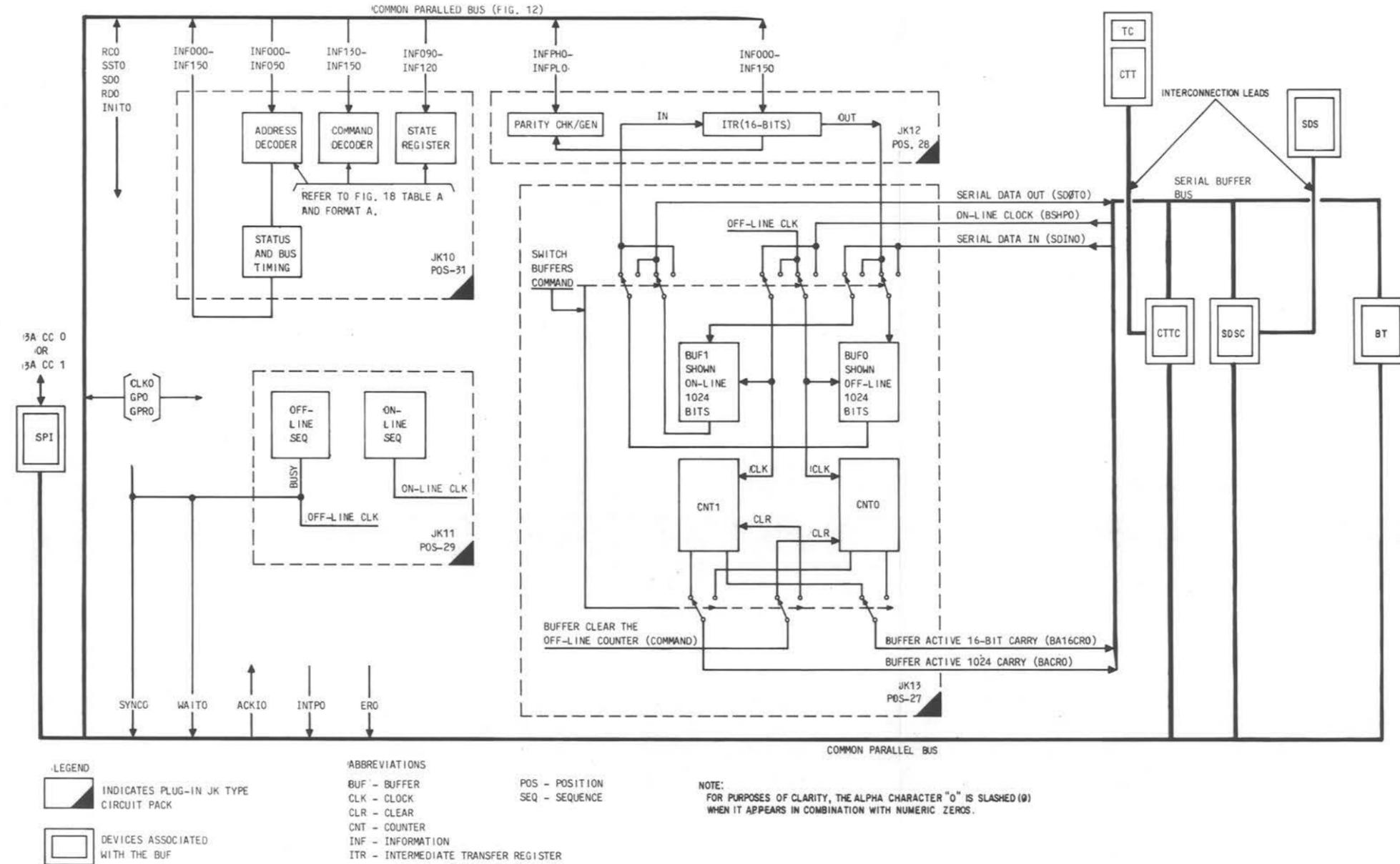


Fig. 26—Buffer Interface Between Serial Buffer Bus and Common Parallel Bus Leads—Functional Block Diagram

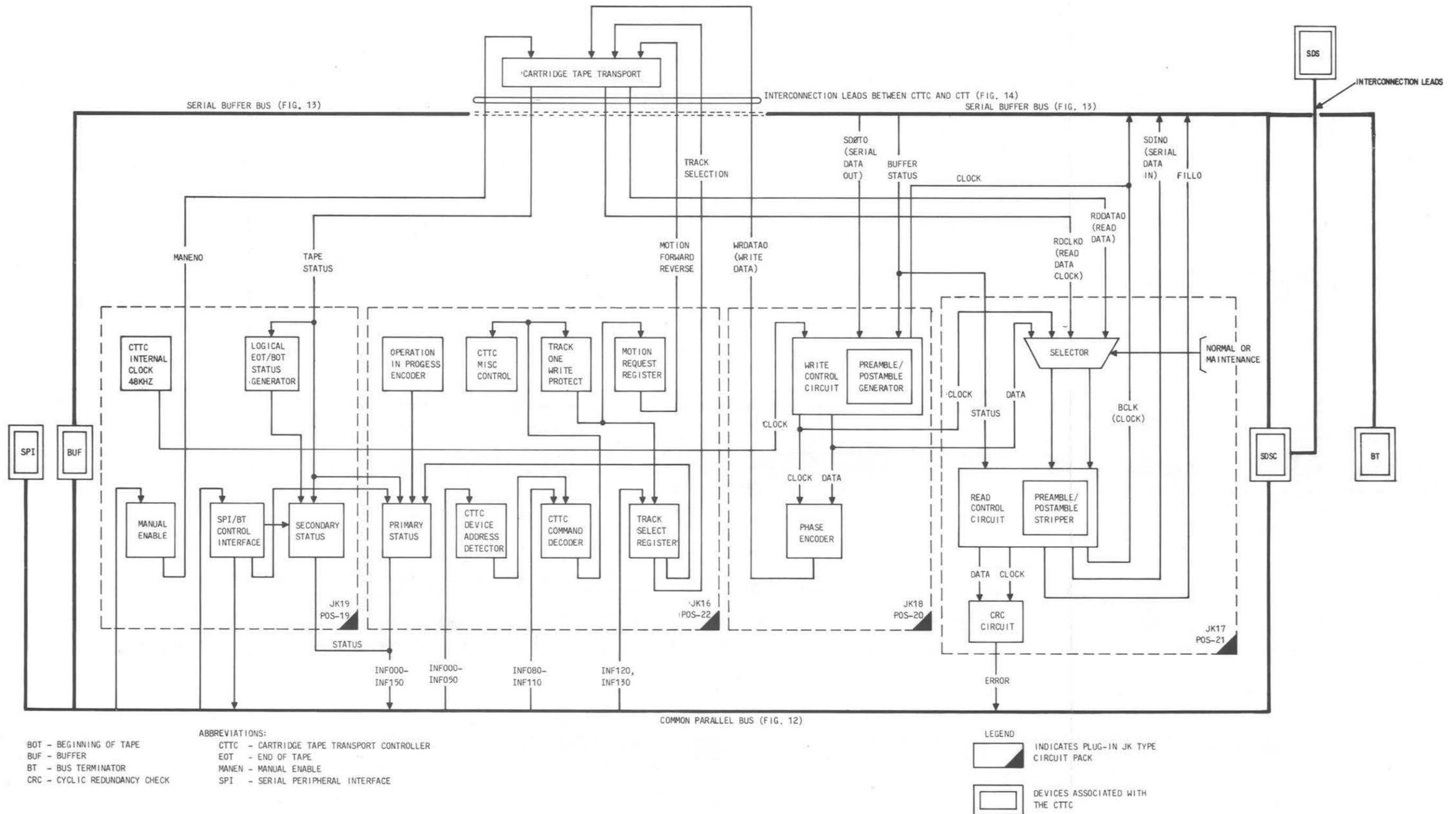
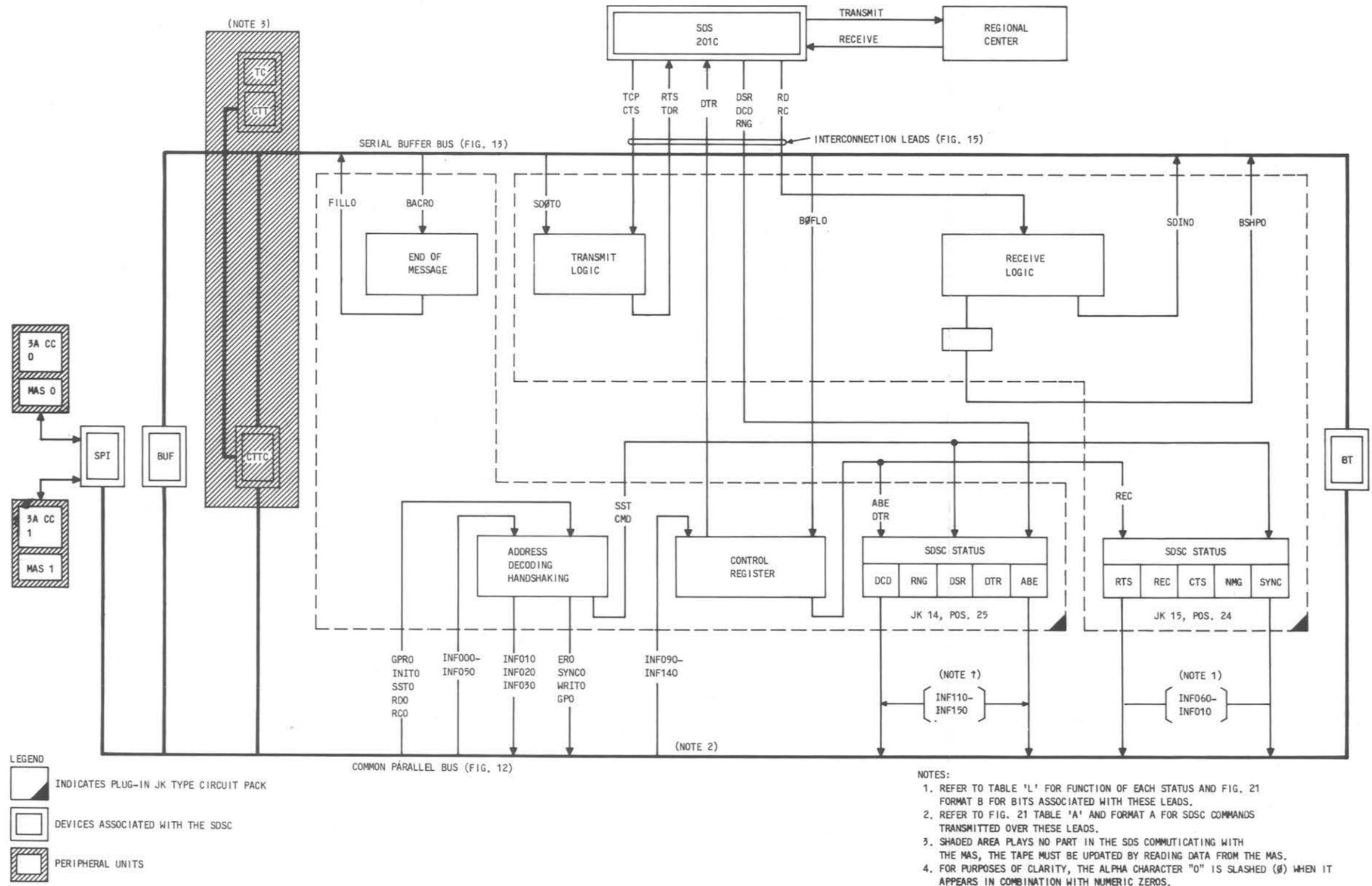


Fig. 27—Cartridge Tape Transport Controller—Interface Between Tape Data Controller Circuit and Cartridge Tape Transport—Functional Block Diagram



LEGEND

- INDICATES PLUG-IN JK TYPE CIRCUIT PACK
- DEVICES ASSOCIATED WITH THE SDSC
- PERIPHERAL UNITS

NOTES:

1. REFER TO TABLE 'L' FOR FUNCTION OF EACH STATUS AND FIG. 21 FORMAT B FOR BITS ASSOCIATED WITH THESE LEADS.
2. REFER TO FIG. 21 TABLE 'A' AND FORMAT A FOR SDSC COMMANDS TRANSMITTED OVER THESE LEADS.
3. SHADED AREA PLAYS NO PART IN THE SDS COMMUNICATING WITH THE MAS, THE TAPE MUST BE UPDATED BY READING DATA FROM THE MAS.
4. FOR PURPOSES OF CLARITY, THE ALPHA CHARACTER "0" IS SLASHED (Ø) WHEN IT APPEARS IN COMBINATION WITH NUMERIC ZEROS.

Fig. 28—Synchronous Data Set Controller—Interface Between Tape Data Controller Circuit and Synchronous Data Set—Functional Block Diagram