3A PROCESSOR MAIN AND SUPPLEMENTAL STORES DESCRIPTION AND THEORY OF OPERATION COMMON SYSTEMS

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1. GENERAL

1.01 This section contains information on the main store (MAS) and supplemental store as utilized with the 3A Processor (Fig. 1). Information is given in terms of physical appearance, functional application, and theory of operation for both the 4K and 16K memory storage devices.

1.02 When this section is reissued, the reason for reissue will be listed in this paragraph.

PURPOSE OF MAIN STORE

1.03 The MAS is the repository for program instructions and data necessary for the 3A Processor not only to perform information processing, but also to perform diagnostics within the system using the 3A Processor. The MAS responds to read or write commands generated by the 3A CC. The No. 2B Electronic Switching System (26 bit) application is covered in Section 232-309-101.

CHARACTERISTICS

1.04 The MAS is a dynamic, volatile, random access semiconductor memory. Dynamic means that the memory (stored) is not permanent and must be refreshed at definite time intervals or the stored information will be lost. Volatile means that if power is interrupted, stored information

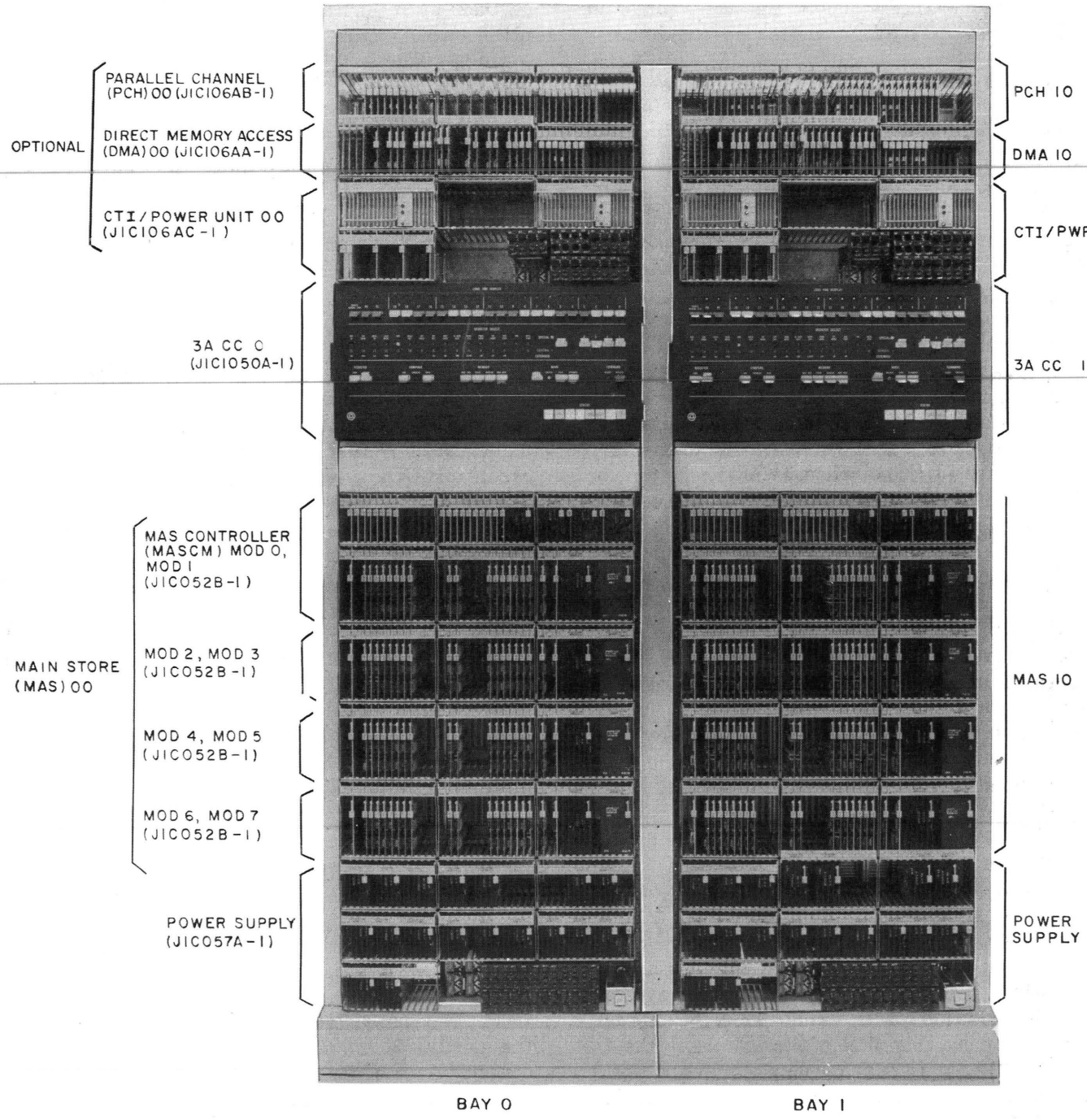


Fig. 1—Typical Processor Frame

is lost. Random access means that any address in the MAS may be read or written on command.

2. PHYSICAL DESCRIPTION

EQUIPMENT DESCRIPTION

2.01 In order to provide continuous processing capability through duplication, each bay of the processor frame contains a 3A CC and dedicated MAS (Fig. 1). The first MAS is located below its dedicated 3A CC and may be either a 4K- or 16K-bit chip configuration. Three additional MASs may be connected to an existing 3A CC—MAS for the 4K-bit chip application. When the 16K-bit chip configuration is used, three MASs may be added (Fig. 2). Main stores must be added in pairs with one dedicated to each 3A CC. Supplementary store frame 0 (J1C065A) houses MASs 01 and 02 dedicated to 3A CC 0 (Fig. 3). It should be noted that the third MAS added is possible only when the second and third MASs are 16K chip configurations. Supplementary store frame 1 (J1C065A) houses MASs 11 and 12 dedicated to 3A CC 1. When facing the front of the 3A Processor frame, supplementary store frame 0 is on the left and supplementary store frame 1 is on the right of the processor frame. The basic MAS unit (Fig. 4) is referred to as a main store controller and memory unit (MASCM) and consists of a main store controller (MASC) and main store memory unit (MASM). The basic MAS provides storage for either 32K or 64K (K = 1024) of 18-bit words in 32K increments. The 32K storage circuitry contains 4K-bit chips and the 128K circuitry contains 16K-bit chips. It should be noted that an MAS is either a 4K or 16K configuration. Beyond the 32K of basic storage, growth is in 32K increments. The basic 128K (16K-bit chip) of storage may grow with the addition of a second 128K of storage. To provide more than 64K of storage using the 4K chips, an MASM is added below the MASCM. A group of memory planes (plugged into the MASM) provides 32K or 128K storage circuitry. An MAS may store up to 256K words.

2.02 An MASCM (Fig. 4, Fig. 5) is mounted on a 10-inch mounting plate and contains the MASC and MASM. The mounting plate includes the connectors into which the MASC and MASM circuit packs and power converters are inserted.

2.03 The MASC (Fig. 5) contains 4 (4 inch by 7 inch) connectorized power converters and 20 (4 inch by 7 inch) circuit packs. A multilayer printed wiring board mounted on the MASC connector terminals connects power, power grounds, signals, and signal grounds to the MASC circuit packs.

2.04 An MASM, when not a part of the MASCM, is contained on a 6-inch plate and mounted below the MASCM (Fig. 4). Two power converters are part of the MASM. A separate MASM is used only with 4K-bit chip memory.

MEMORY PACKAGE

2.05 The KS-21701 random access memory (Fig. 6, Fig. 7) is a 4096-bit (4K), 18-pin dual-in-line package (DIP). Nine memory planes (Fig. 8) are required to store 32K 18-bit words. Each memory plane contains two groups of eight DIPs. Each group (of 8 DIPs) stores 1-bit of the 18-bit word. The W.E. 28A (16K) DIP is used in the same physical configuration as the 4K DIP with the nine memory planes (Fig. 9, Fig. 10) now storing 128K of 18-bit words.

MAIN STORE MEMORY MODULE

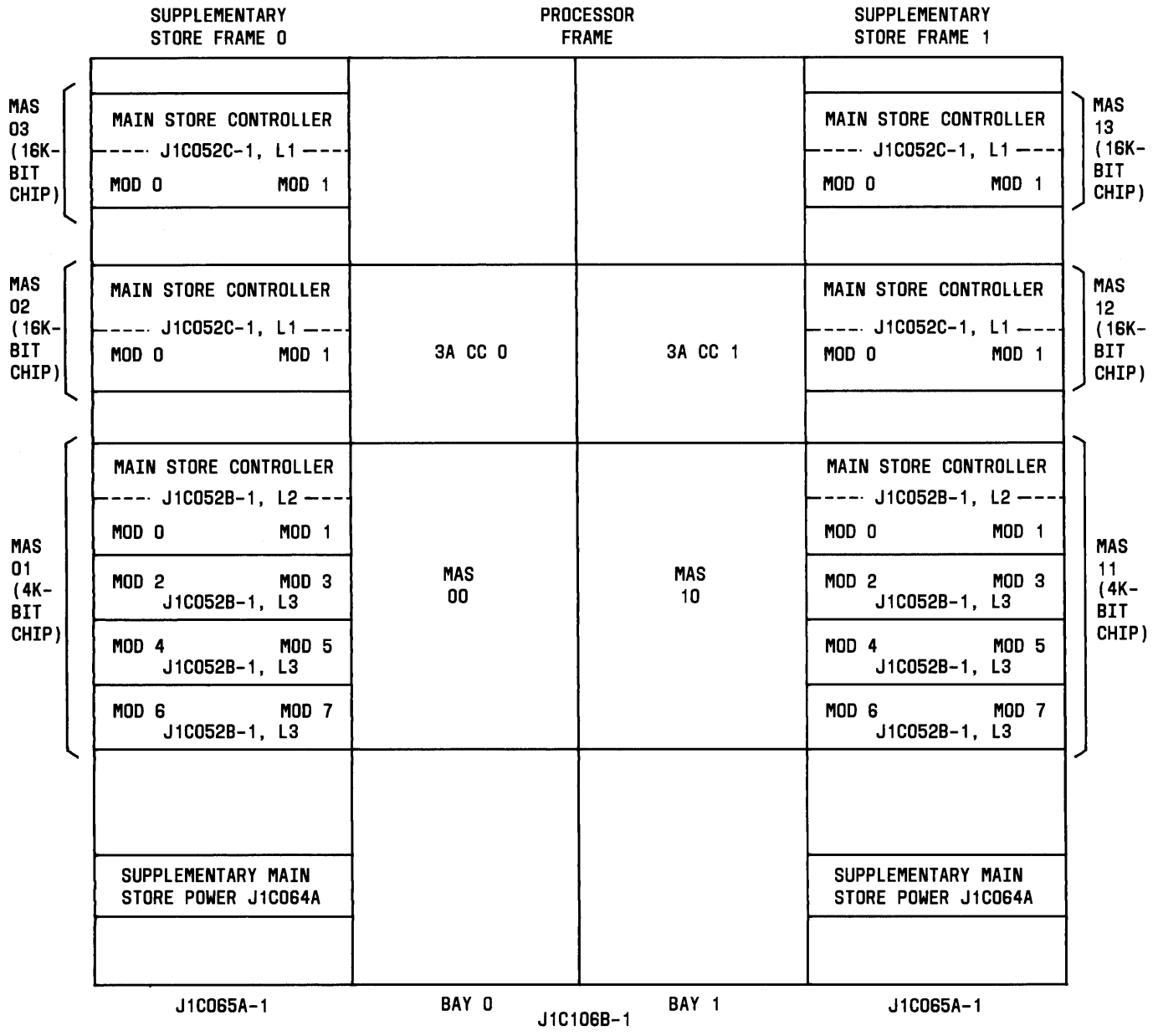
2.06 A main store memory module (MASMO) (Fig. 4, Fig. 5) is an addressable group of circuit packs consisting of one fanout board and nine memory planes. This group is the basic and also the smallest growth increment of either 32K or 128K depending on the KS-21701 or W.E. 28A, respectively.

MAIN STORE MEMORY UNIT

2.07 An MASM (Fig. 5) is an assembly containing two power converters and connectors for the circuit packs of two MASMOs. The MASM contains back-plane wiring for signal and power leads. The MASM back plane is an assembly of signal, power, and ground conductors (in sandwich type construction) connecting the circuit packs and power converters of the MASM.

RESISTOR TERMINATION BOARDS

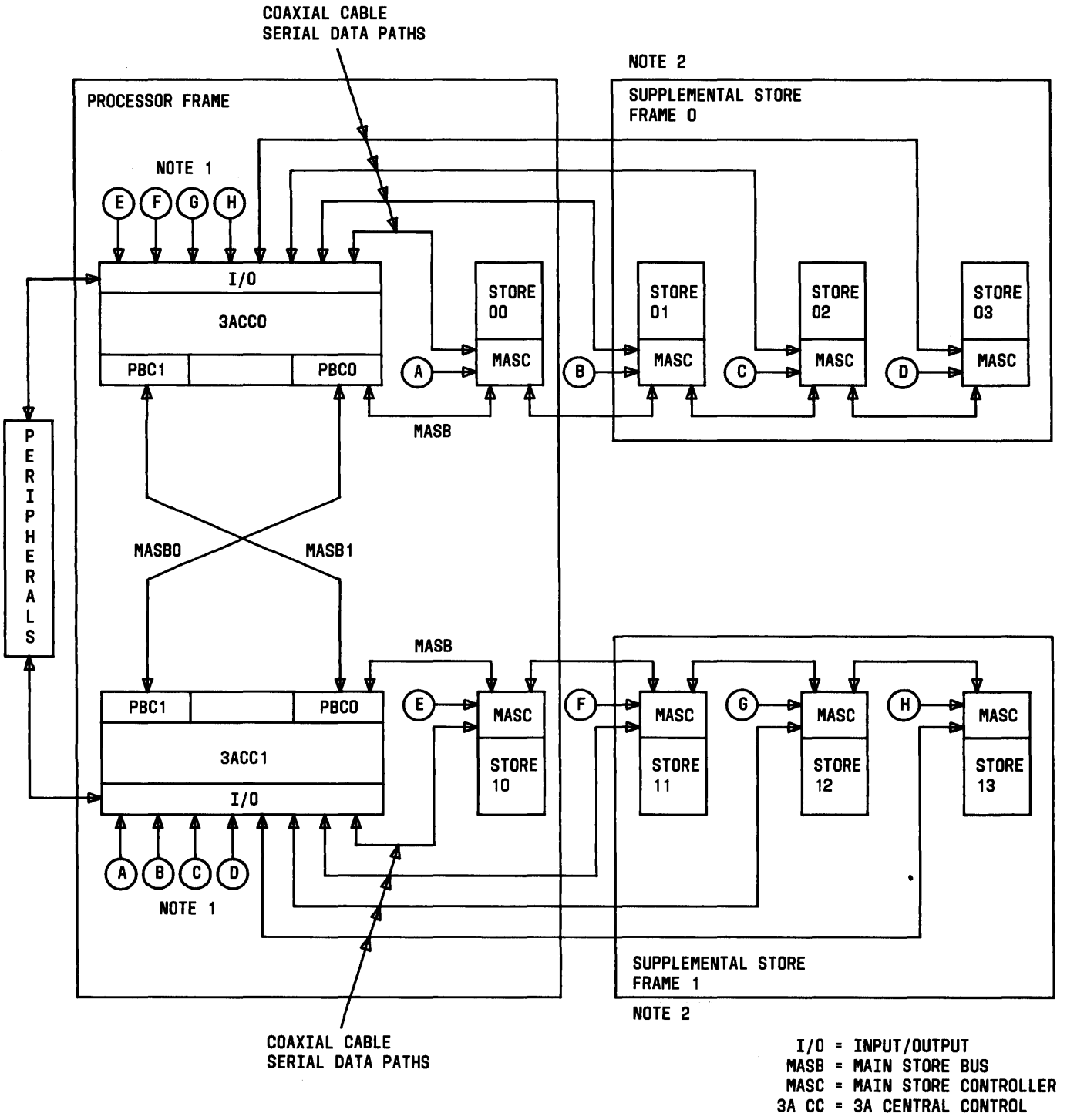
2.08 The 959A and 959B resistor termination boards (Fig. 11) are 1-3/4 inches long and 1-5/16 inches wide and are connected to the terminals of the MASC and MASM, respectively.



NOTE 1: WHEN MASs 00 AND 01 ARE 4K-BIT CHIP CONFIGURATION, ADDITIONAL MAS PAIRS MAY BE EITHER 4K OR 16K-BIT CONFIGURATION. WHEN MASs 03 AND 13 ARE ADDED, MASs 02 AND 12 MUST ALSO BE 16K-BIT CHIP CONFIGURATION.

NOTE 2: WHEN MASs 00 AND 01 ARE 16K-BIT CHIP CONFIGURATION, ADDITIONAL MASs MUST BE 16K-BIT CHIP CONFIGURATION

Fig. 2—Supplementary Main Store Arrangement



1. (A), (B), (C), (D), (E), (F), (G) AND (H), ARE COAXIAL CABLE SERIAL DATA PATHS.
2. SUPPLEMENTAL STORE FRAMES ARE ADDED IN PAIRS, EACH FRAME DEDICATED TO ITS ASSOCIATED 3A CC.

Fig. 3—Block Diagram of 3A CC—MASs

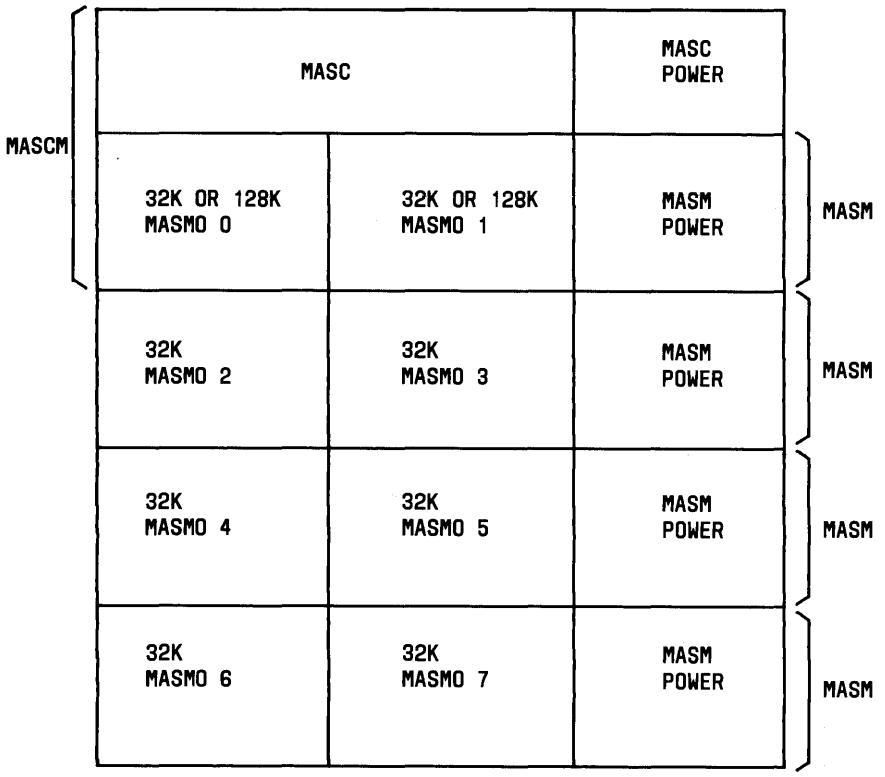


Fig. 4—Main Store Configurations

CABLING

2.09 The MAS interfaces with the 3A CC via three types of cabling:

(a) Flat ribbon cable terminated with plug-in connectors

(b) Twisted pairs terminated with plug-in connectors

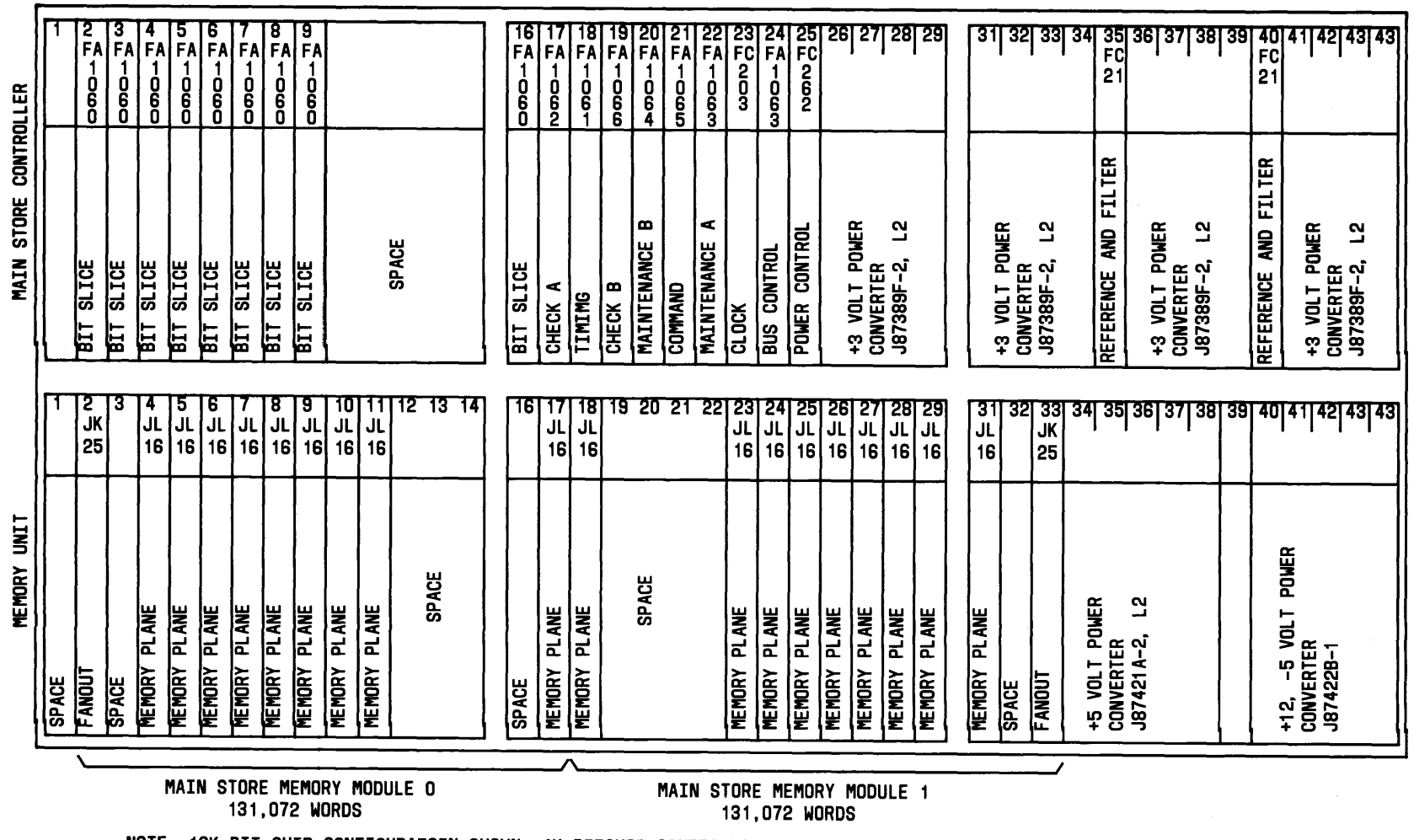
(c) Coaxial cable terminated with coaxial connectors.

Flat ribbon cables (connectorized) make up the parallel bus between the 3A CC and MASC. Twisted pairs (not connectorized) connect the MASC to the first MASM. Flat ribbon (connectorized) cables connect MASM 0 to MASM 2, MASM 2 to MASM 4, and MASM 4 to MASM 6. Flat ribbon cables also connect MASM 1 to MASM 3, MASM 3 to MASM 5, and MASM 5 to MASM 7. With the 16K-bit chip design, only one MASM is used per MAS and therefore only twisted pairs connect the MASC to the MASM. The coaxial cables provide a diagnostic interface between each MASC and 3A CC via a serial data channel. Each MAS has a pair of coaxial cables connecting to each 3A CC. Flat ribbon cables make up the parallel bus which connects one MAS (controller) to the next MAS (controller). Connectorized twisted pairs connect reference voltages, start signals, and alarms between the 3A CC and dedicated MASs.

3. FUNCTIONAL DESCRIPTION

GENERAL

3.01 The 3A CC reads and writes into the MAS via the parallel bus. When a command, address, data (when writing), and a start signal are received, the MAS performs its functions



NOTE: 16K-BIT CHIP CONFIGURATOIN SHOWN. 4K-BITCHIP CONFIGURATION REQUIRES JK-3 AND JL-2 CIRCUIT PACKS AND STORES 32,768 WORDS

Fig. 5—Main Store Controller and Memory Unit Circuit Pack Arrangement

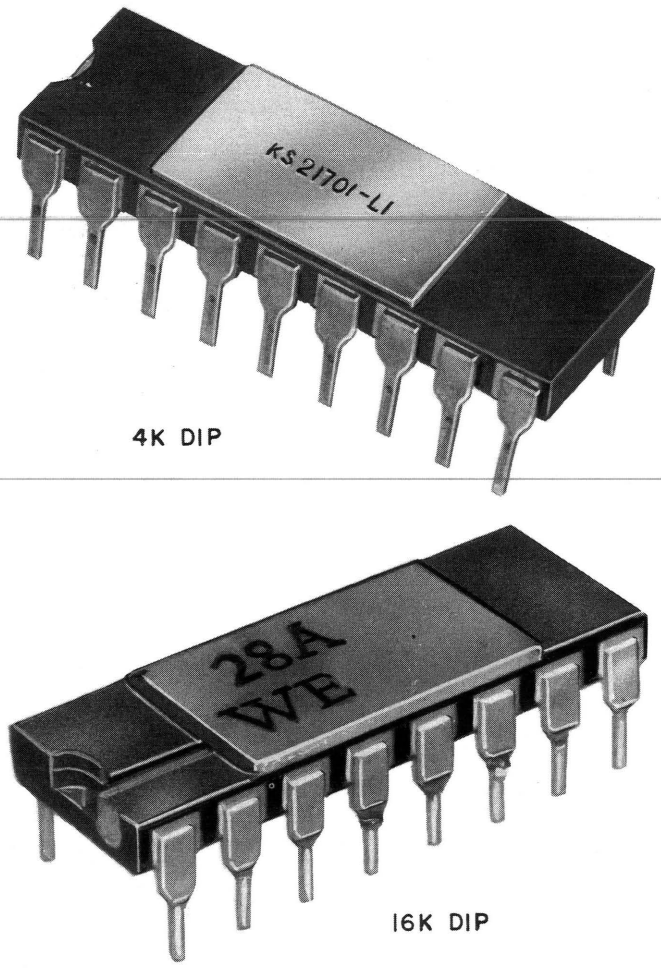


Fig. 6—Dual In-Line Packages

without timing pulses (asynchronously) from the 3A CC. Approximately 800 ns are required by the MAS (closest to the 3A CC) to respond to a memory read or write command; ie, from store go to store complete. The MAS memory may be subdivided functionally into the following areas:

(a) Write-protected areas which are generally designated for program instruction and data

(b) Writable areas for temporary data.

DUPLEX CONFIGURATION

3.02 In system use, the 3A CC and MASs are duplicated for system reliability (Fig. 3). Each 3A CC and dedicated MASs is a switchable entity.

3.03 In normal operation, the on-line 3A CC keeps the standby stores up to date; ie, the on-line 3A CC not only writes into its own MASs, but also into the MASs of the standby 3A CC. This keeps the standby control unit ready to assume control from the on-line control unit in the event of a switch.

MAIN STORE CONTROLLER

3.04 The MASC serves as the interface and control between the 3A CC and the MAS memory modules. The MASC is composed of 20 circuit packs and 4 plug-in power converters (Fig. 5). The MASC circuit packs consist of the following:

- Nine bit-sliced boards
- One timing board

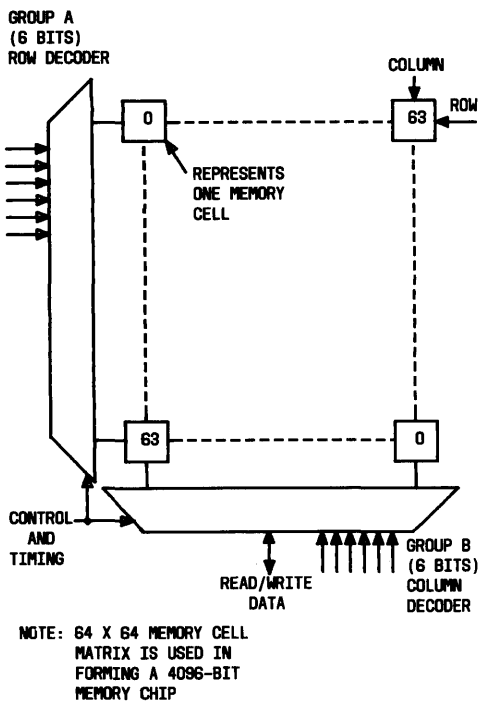


Fig. 7—Organization of Memory Chip

- Two check boards
- One bus control board
- Two maintenance boards
- One command board
- One clock board
- One power control board
- Two power reference and filter boards.

MAIN STORE MEMORY UNIT

3.05 Each MASM (Fig. 5) consists of two power converters and up to two MASMOs.

3.06 Each fanout board consists of the following:

(a) A decoder for determining when an address applies to one of the words stored in this module

(b) Circuitry to distribute address, refresh, and timing information from the controller to memory planes

(c) Address parity check circuitry

(d) Address multiplexing and clock generation timing (16K)

(e) Other checkers.

3.07 Each JL2 (4K chip) memory plane and JL16 (16K chip) memory plane (Fig. 8, Fig. 9) contains:

(a) Sixteen memory DIPs

(b) A package select decoder for determining which two memory DIPs are to be accessed

(c) Data output buffer circuitry for 2 data bits

(d) Data input buffer circuitry for 2 data bits

(e) Address input buffer circuitry

(f) Refresh circuitry.

3.08 The nine memory planes are needed to form an 18-bit word of storage (16 data bits and 2 parity bits). These planes are bit-sliced, and the bit assignments of the DIPs on the memory planes are shown in Table A.

MEMORY PACKAGE

3.09 The KS-21701 DIP and W.E. 28A DIP are dynamic, random access, nondestructive readout memory devices. The matrix organization of the 4K chip (Fig. 10) contains 6 address bits in group A and are dedicated to determine which one of the 64 possible rows is to be accessed. The 6 address bits in group B are decoded to determine which one of the 64 possible columns is to be accessed. Therefore, one memory cell (1 bit) of a chip may be accessed by designating a row and column. A control lead determines the read or write mode, and a common lead is used to read and write a data bit. The W.E. 28A 16K chip is addressed by seven row and seven column bits which are demultiplexed on the W.E. 28A. Separate data leads are used to read or write a data bit.

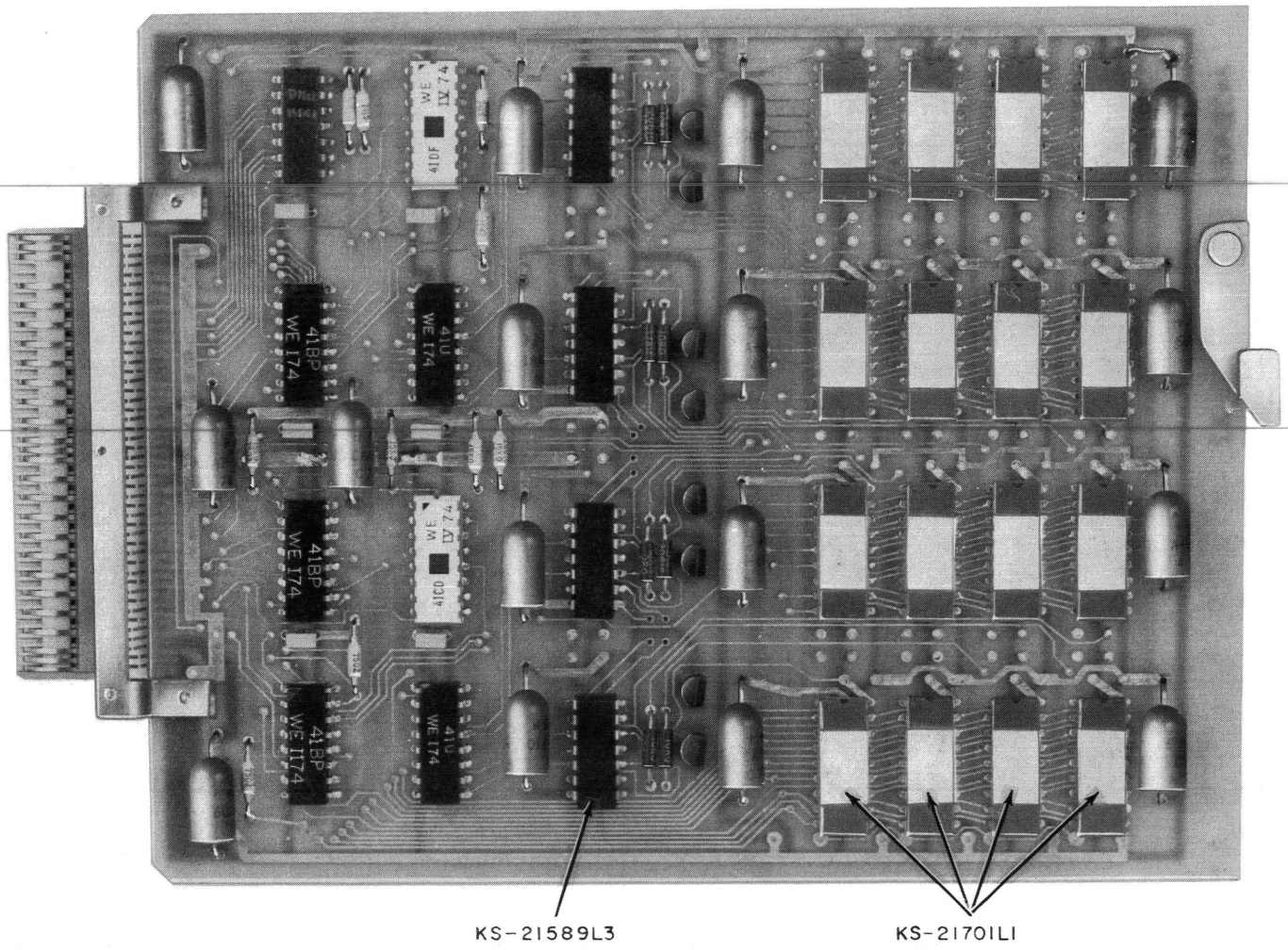


Fig. 8—Typical 4K-Bit Memory Plane

RESISTOR TERMINATION BOARDS

3.10 Each 959A and 959B resistor termination board (Fig. 11) contains eight sets (two resistors in series) of resistors. The 959As connect to the MASC connector terminals and terminate signals from the MASMOs. The 959Bs connect to the bottommost MASM connector terminals (of each MAS) and terminate signals from the MASC. For a 4K-bit chip 256K configuration (Fig. 4), the 959Bs are connected to the terminals serving MASMO 6 and MASMO 7. Power control and alarm leads do not require resistor termination boards.

COMMUNICATION FACILITIES

3.11 The two basic means of communication between the 3A CC and MAS are the main store bus (MASB) and an input/output (I/O) subchannel. The MASB is the normal means of communication, and the I/O subchannel is used for diagnostic purposes.

A. Main Store Bus

3.12 The 3A CC is designed to use a direct-coupled store bus in an asynchronous mode. The asynchronous mode of operation provides the system with the flexibility of memory hardware. The address portion of the bus is unidirectional, while the data portion of the bus is bidirectional.

3.13 The MASB consists of 53 leads between the 3A CC and the first MAS (Fig. 12). A store busy (SBY) lead is added to the MASB between MASs. The 3A CC commands sent to

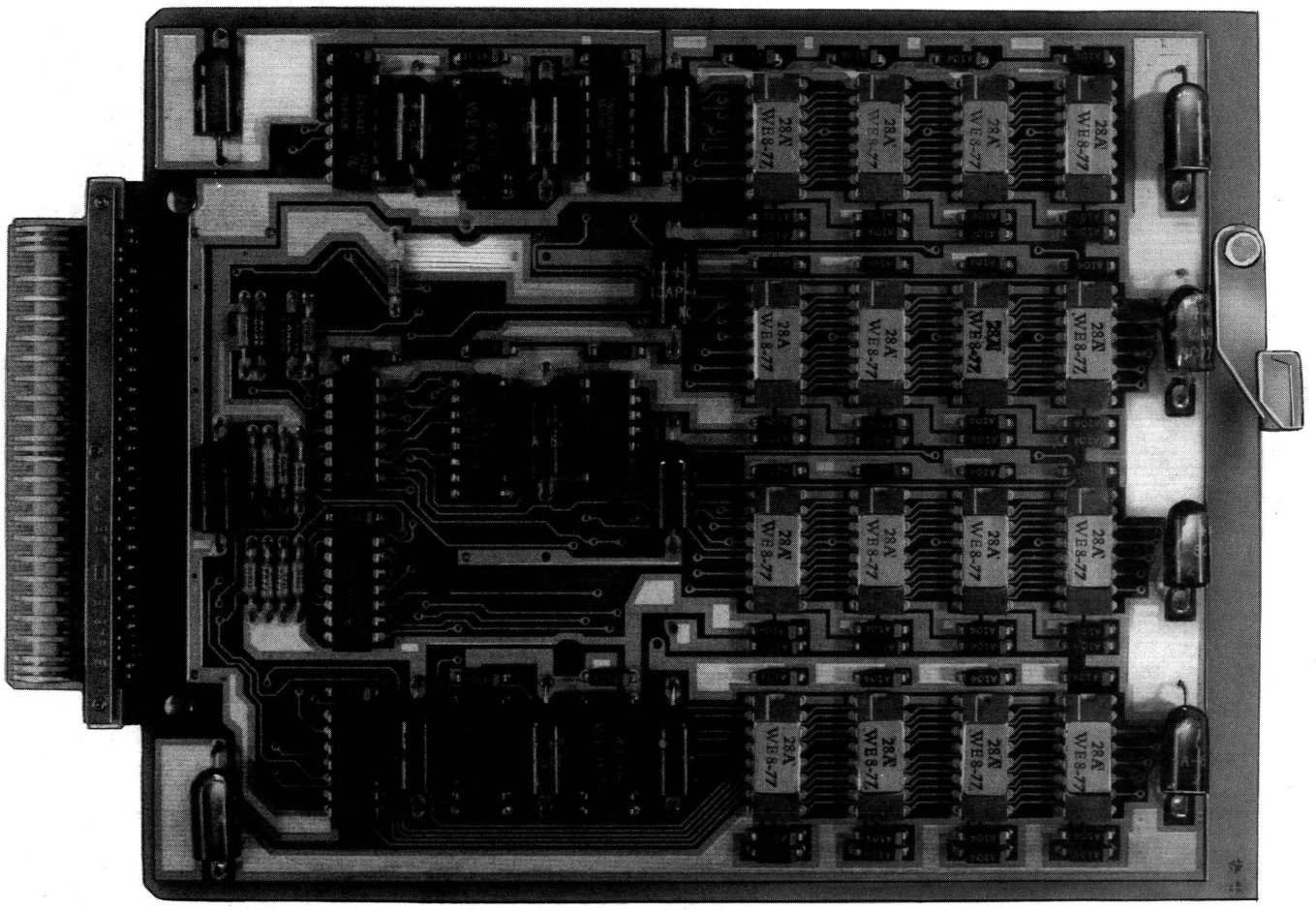


Fig. 9—Typical 16K-Bit Memory Plane

the MAS are encoded in 2-out-of-4 codes which facilitate error detection. Designations and functions of the leads between the 3A CC and MASs are shown in Table B. The store request (SREQ) lead, if used, will be described in the particular application document.

B. Input/Output Subchannel

3.14 An I/O serial subchannel (Fig. 3) is provided to each controller from each 3A CC. The I/O subchannel from the 3A CC of the same control unit as the MAS has priority over the I/O subchannel from the duplicate 3A CC. The higher priority I/O subchannel is used in the initial program loading procedure to initialize the controller so that the store can be loaded. The I/O subchannel permits the on-line 3A CC to access the store of the other 3A CC for diagnostic purposes.

4. THEORY OF OPERATION

GENERAL

4.01 This section describes the theory of operation of the MAS (Fig. 13) as a part of the 3A Processor.

4.02 The MAS operates asynchronously with the 3A CC via the MASB. This makes it possible for the 3A CC to perform other functions during the time the MAS is responding to a 3A CC command and provides flexibility in the MAS response time to the 3A CC. The 2-out-of-4 bit command codes (bus leads SC0—SC3) decoded in the MASC cause a read or write to occur (Table B).

4.03 Memory information is stored as the presence or absence of electrical charges on the

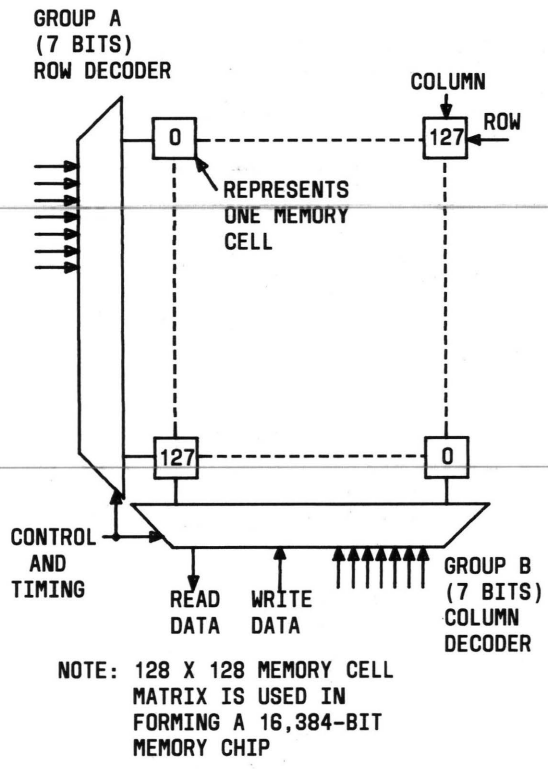
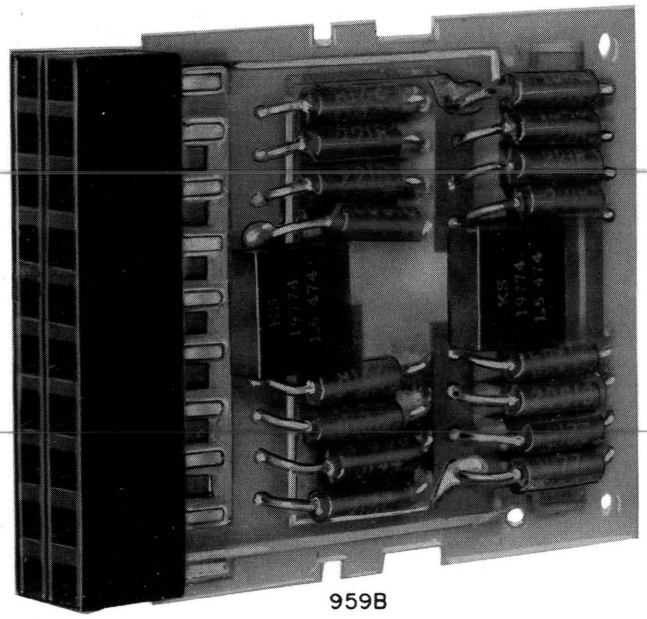


Fig. 10—Organization of 16K-Bit Memory Chip



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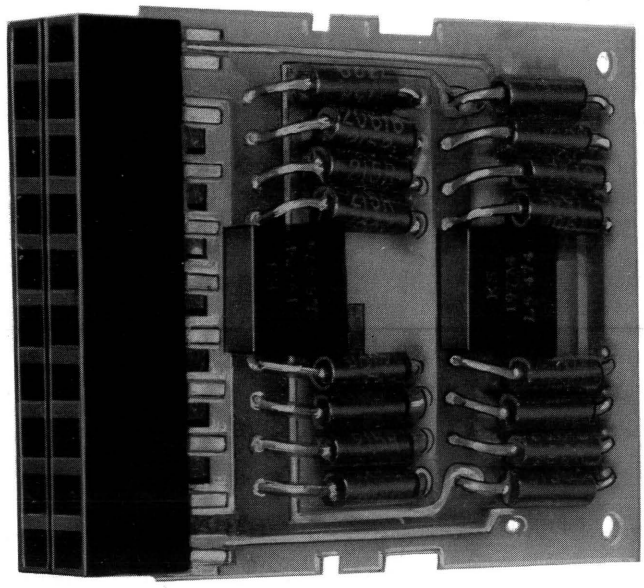


959A

Fig. 11—Resistor Termination Boards

parasitic capacitance of insulated gate field effect transistor (IGFET) memory cells. Memory cells require periodic refreshing to maintain this electrical charge and ensure the integrity of the data. Refresh cycles are interspersed between normal MAS cycles on a periodic basis.

4.04 The MAS reads and writes 18-bit data words (16 data and 2 parity bits) into or from memory storage (Fig. 13) with command lead SC3 controlling the direction of data flow. The MAS requires the following parallel bus information to respond to the 3A CC.

- Store go (SGO)
- Command (read/write)
- Address
- Data (write).

4.05 Timing to perform a read or write is generated in the MASC. Error detection during a read, write, or refresh is performed by the MASC which places an error signal on the bus should a problem occur during the MAS cycle. Store complete (SCM) is placed on the bus to inform the 3A CC that data is available on the bus (read) or that a word has been written (write). The SBY signal prevents the possibility of unselected MAS(s) responding to a 3A CC command.

TABLE A

BIT ASSIGNMENTS OF THE DUAL IN-LINE PACKAGES ON THE JL2 AND JL16 MEMORY PLANES

MEMORY PLANE NUMBER	ASSIGNMENT
0	Bits 0 and 8 of the 32,768 or 131,072 words of storage
1	Bits 1 and 9 of the 32,768 or 131,072 words of storage
2	Bits 2 and 10 of the 32,768 or 131,072 words of storage
3	Bits 3 and 11 of the 32,768 or 131,072 words of storage
4	Bits 4 and 12 of the 32,768 or 131,072 words of storage
5	Bits 5 and 13 of the 32,768 or 131,072 words of storage
6	Bits 6 and 14 of the 32,768 or 131,072 words of storage
7	Bits 7 and 15 of the 32,768 or 131,072 words of storage
8	Bits P_L and P_H of the 32,768 or 131,072 word of storage

4.06 Selected 4K word sections of memory storage are protected against accidental overwrites. Those areas are "write-protected" because they may contain generic program and office data. Write protection is temporarily removed to make corrections and additions, and is then reinstated.

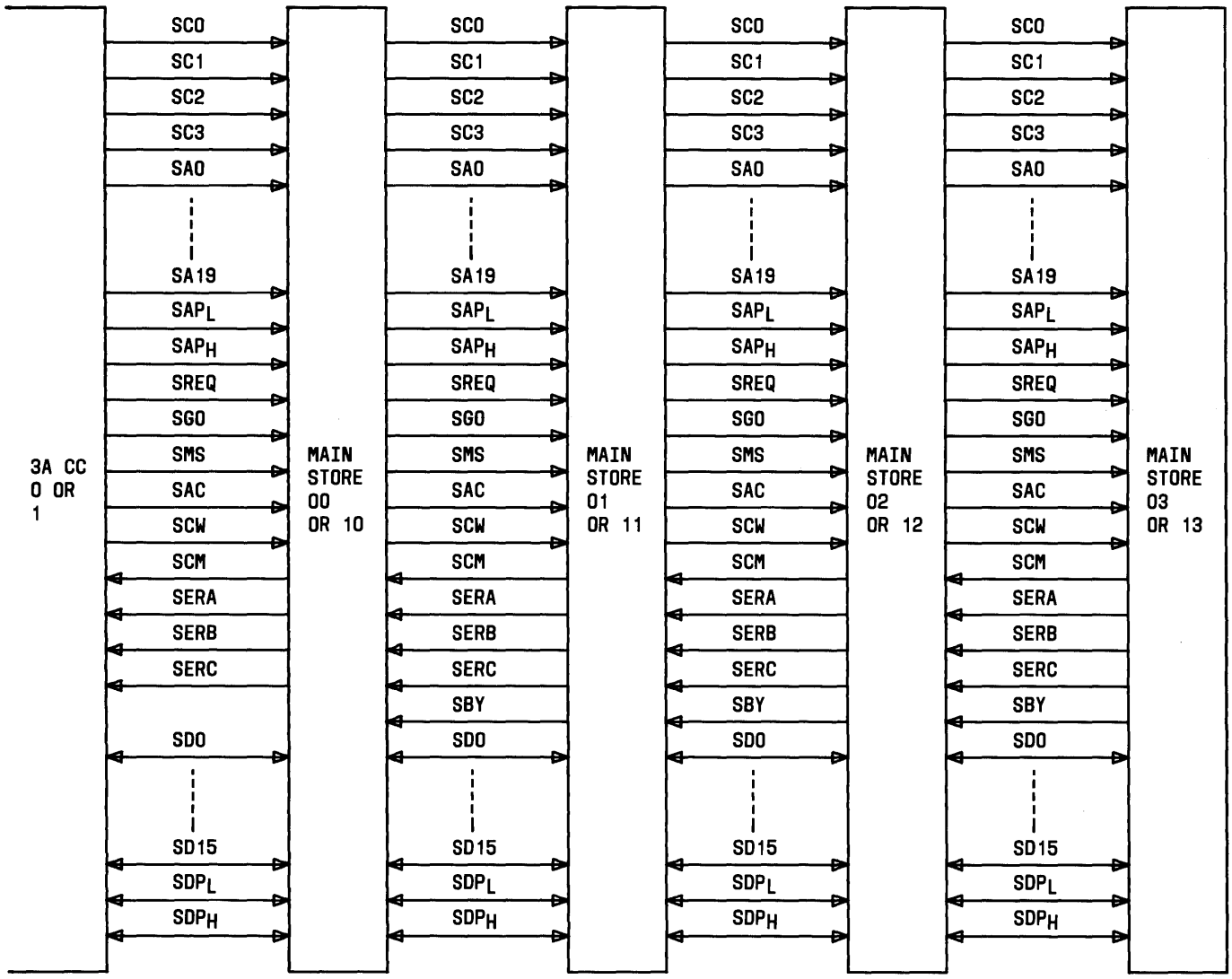
4.07 The MAS error detection circuitry provides the 3A CC with fault indicators via the parallel bus. The bus transfers the following error signals:

- Store error A (SERA)
- Store error B (SERB)
- Store error C (SERC).

4.08 The MAS power converters are self-contained and are discussed in Part 5 of this section.

4.09 For the purpose of this discussion, the MAS is divided into functional areas:

- Address
- Data
- Write-protect
- Error detection
- Memory
- Terminations
- Control and timing
- Refresh control
- Diagnostic access.



SC - STORE COMMAND
SA - STORE ADDRESS BIT
SAP_L - STORE ADDRESS PARITY OVER ADDRESS BITS 7-0
SAP_H - STORE ADDRESS PARITY OVER ADDRESS BITS 19-8
SREQ - STORE REQUEST
SGO - STORE GO
SMS - STORE MAINTENANCE STATE
SCM - STORE COMPLETE
SERA - STORE ERROR A
SERB - STORE ERROR B
SERC - STORE ERROR C
SBY - STORE BUSY
SD - STORE DATA BITS
SDP_L - STORE DATA PARITY OVER DATA BITS 7-0
SDP_H - STORE DATA PARITY OVER DATA BITS 15-8
SAC - STORE AUTOMATIC CORRECTION
SCW - STORE COMPLEMENT WRITE

Fig. 12—Main Store Bus Leads

ADDRESS

4.10 The bus transfers address information (Table B) between the 3A CC and MAS. Address information is active (logic 1) when a low voltage is on the bus leads. Address bits 0 through 19 (plus 2 parity bits) are loaded into a 22-bit address register in the MASC; 18 address and 2 parity bits are gated to the fanout board of each MASMO. From the selected memory module fanout board, address bits 0 through 14 are gated to associated memory planes. Memory plane decoding

TABLE B

DESIGNATIONS AND FUNCTIONS OF THE MAIN STORE BUS LEADS

LEAD	FUNCTION
SC3, SC2, SC1, SC0	*Store Command Leads 0 Thru 3:* These leads are used by the 3A CC to issue a 2-out-of-4 command code to the memory. The assignments of the codes are: 1100 = Read The contents of memory at the location defined on the address leads are returned on the data leads. 0011 = Write The 16 data bits and 2 parity bits on the data leads are written in the store at the location defined on the address leads. 1001 = Load-Write-Protect This operation returns the contents of the write-protect (WP) register in the store controller to the 3A CC. 0110 = Store-Write-Protect This operation loads the WP registers in the store controller. 0101 = Blind-Write This operation (when hardwire enabled) writes data into write-protected areas of memory. Blind-write not intended for field use. 1010 = Spare
SREQ	*Store Request Lead:* This signal is used by a lower priority. 3A CC to inform a higher priority 3A CC that it wants sole ownership of the MASB for a multiple cycle operation. This signal is necessary to prevent inter-write problems with multiple users on an MASB. It is not necessary for a higher priority user to inform a low priority user of a multiple cycle operation, as the high priority user has the ability to prevent store access by a lower priority user.
SGO	*Store Go Lead:* This is a signal that is put on the bus to tell the store that a store operation has been requested. It is removed after the 3A CC has received the store-complete (SCM) signal. In the case of a read operation, the address and command information is present on the bus. In the case of a write operation, the data, as well as the address and command information, is present on the bus.
SCM	*Store Complete Lead:* This signal is sent by the store to indicate that the readout information is present on the bus for read operations. It is also sent on a write operation to indicate that the command, data, go, and address information may be removed from the bus.
SERA	*Store Error A-Lead:* This signal is sent by the store to indicate that a possibly fatal fault has occurred. This signal will cause an initialization of the 3A CC. Some external items to the store which would generate an SERA signal include a parity error on either address or data, an invalid command code, and an unequipped store location address.

TABLE B (Contd)

DESIGNATIONS AND FUNCTIONS OF THE MAIN STORE BUS LEADS

LEAD	FUNCTION
SERB	*Store Error B-Lead:* This signal is sent by the store to indicate that a write-protect error has been detected. This signal will cause an intialization of the 3A CC. An attempt to issue a write command in a section of memory that has been write-protected will result in an SERB signal.
SD0-SD15, SDP_H, SDP_L	*Store Data Leads 0 Thru 15, Parity High, and Parity Low:* These leads are used to provide the means of reading the data from or writing the data into the address on leads SA0 thru SA19.
SA0-SA19, SAP_H, SAP_L	*Store Address Leads 0 Thru 19, Parity High, and Parity Low:* SAP_H — Parity on SA8 thru SA19. SAP_L — Parity on SA0 thru SA7. SA18,SA19 — Defines which one of the possible four main store circuits is to be accessed (only one main store circuit in No. 3 ESS so only one legal code). SA3 thru SA16 — Defines which bits on the memory chips within the defined modules are to be accessed for 16K-bit memory. SA15-SA17 — Defines which one of the eight memory modules within the defined store is to be accessed for 4K-bit memory. SA3-SA14 — Defines which bits on the memory chips within the defined modules are to be accessed for 4K-bit memory. SA0-SA2 — Defines which 4K chips will be enabled on each memory plane.
SERC	*Store Error C-Lead:* This signal is sent by the store to indicate that bad parity was detected on the word accessed. This signal will be sent in lieu of the SCM signal. The bad data and the address at which it is located will be present on the MASB at the time the SERC becomes active.
SMS	*Store Maintenance State:* This signal is sent by the 3A CC to its MAS to override the disabling of the I/O serial channel port from the other 3A CC. This signal will prevent a fault in the off-line 3A CC from interfering with the on-line diagnostics.
SAC	*Store Automatic Correction:* The SAC signal is sent to MASC during Block Double Store Read (BDSR) state. The MASC, when detecting a double parity error on read, complements the data and parity. Parity error signals are disabled.
SCW	*Store Complement Write:* Causes a word with a bad parity bit to be complemented and written into the address from which it was read. Parity bits are also complemented. Write-protect check is disabled in SCW mode. The 3A CC sends SCW signal when required during simplex mode.

circuitry (address bits 0 through 2) determines which 2-out-of-16 4K-bit chips are selected on each of the nine memory planes and which row and column (bits 3 through 14) on the 4K-bit chips will be selected. At the time the MASC loads the address bits, bits 18 and 19 are decoded in the MASC so that the MAS may respond to commands and data. Address bits 18 and 19 are used in a single or multiple store configuration to designate a particular MAS. Address parity high is combined with address bits 18 and 19 to produce a new parity bit which is sent to each fanout board. A new parity bit is necessary to compensate for the parity of bits 18 and 19, which are not gated to the fanout board. The selected memory module fanout board tests address bits 0 through 17, parity low,and the new parity high bit for correct address parity. Address parity errors cause a bit to be set in the MASC error register. Address bits 15 through 17 are decoded by each memory module fanout board to select a single MAS memory module. Only one of the fanout boards will decode bits 15 through 17 as its address to perform parity checks, gate address bits 0 through 14 to the memory planes, and generate enabling signals to its memory planes. Address parity is checked on all MAS cycles. The same address bits are used for the 16K-bit memory chip (Fig. 13), however address bits 3 through 16 are used for row and column select. Address bit 17 is used to select one of two possible fanout boards which in turn select 128K of memory.

DATA

4.11 Data bits 0 through 15 plus 2 parity bits (P_H, P_L) are loaded into an 18-bit data register in the MASC (Table C) and distributed to their respective memory planes. Data parity is checked (for odd parity) on both read and write memory cycles. During a memory write cycle, bad data parity causes a bit to be set in the MASC error register. Data is gated to or from the memory planes by enabling signals derived from the read/write command and MASC timing. Data and parity from memory are loaded into the data register and placed on the bus. The 3A CC reads the bus when SCM becomes active. When bad parity is detected during memory read, the MASC generates an SERC signal instead of a store complete signal to inform the 3A CC (via the bus) to take corrective action.

WRITE-PROTECT

4.12 Individual bits of a 72-bit write-protect register (64 data and 8 parity bits) are selectively set by the 3A CC to protect the 256K words in each fully equipped MAS. The write-protect register is considered to be four 18-bit registers for functional purposes. Each data bit of the register, when set, protects 4K words in memory from being accidentally overwritten. Write-protected areas of memory are generally used to store generic program and office (translation) data. Two of the 2-out-of-4 3A CC commands (Table B) are dedicated to write-protect:

- Load-write-protect
- Store-write-protect.

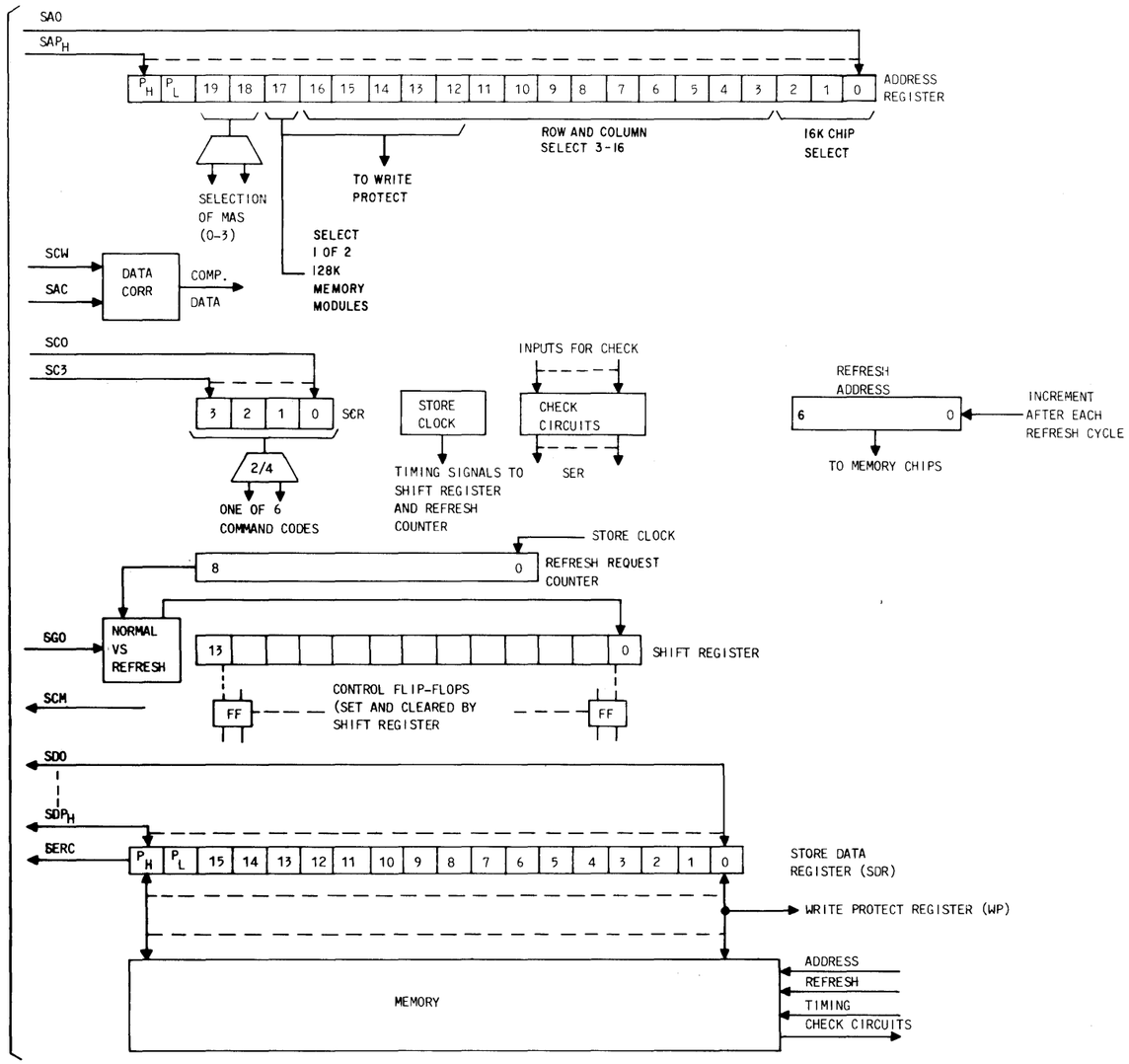
Load-write-protect returns the contents of one of the four write-protect registers (18 bits) to the 3A CC via the bus. The particular write-protect register selected is determined by address bits 15 through 17. Parity is not checked in the main store over the write-protect register data bits. Store-write-protect is the 2-out-of-4 command which causes one of the four write-protect registers to be written. Data parity is also not checked during this command in the MAS. The particular register to be written is determined by address bits 15 through 17. Four MAS cycles are required to write or read the write-protect register of a fully equipped main store.

4.13 Should the 3A CC attempt to write a protected portion of memory, the decoded write command signal is changed to a read signal and an SERB signal is generated by the MASC and placed on the bus.

ERROR DETECTION

4.14 The MASC contains a 16-bit error register (ER) whose bits are set by error conditions detected in the MAS. Timing, select, refresh, diagnostic, and parity errors are monitored. There are three methods of setting the ER flip-flops.

- Normal set input
- External error collect tied to zero outputs of ER under diagnostic control



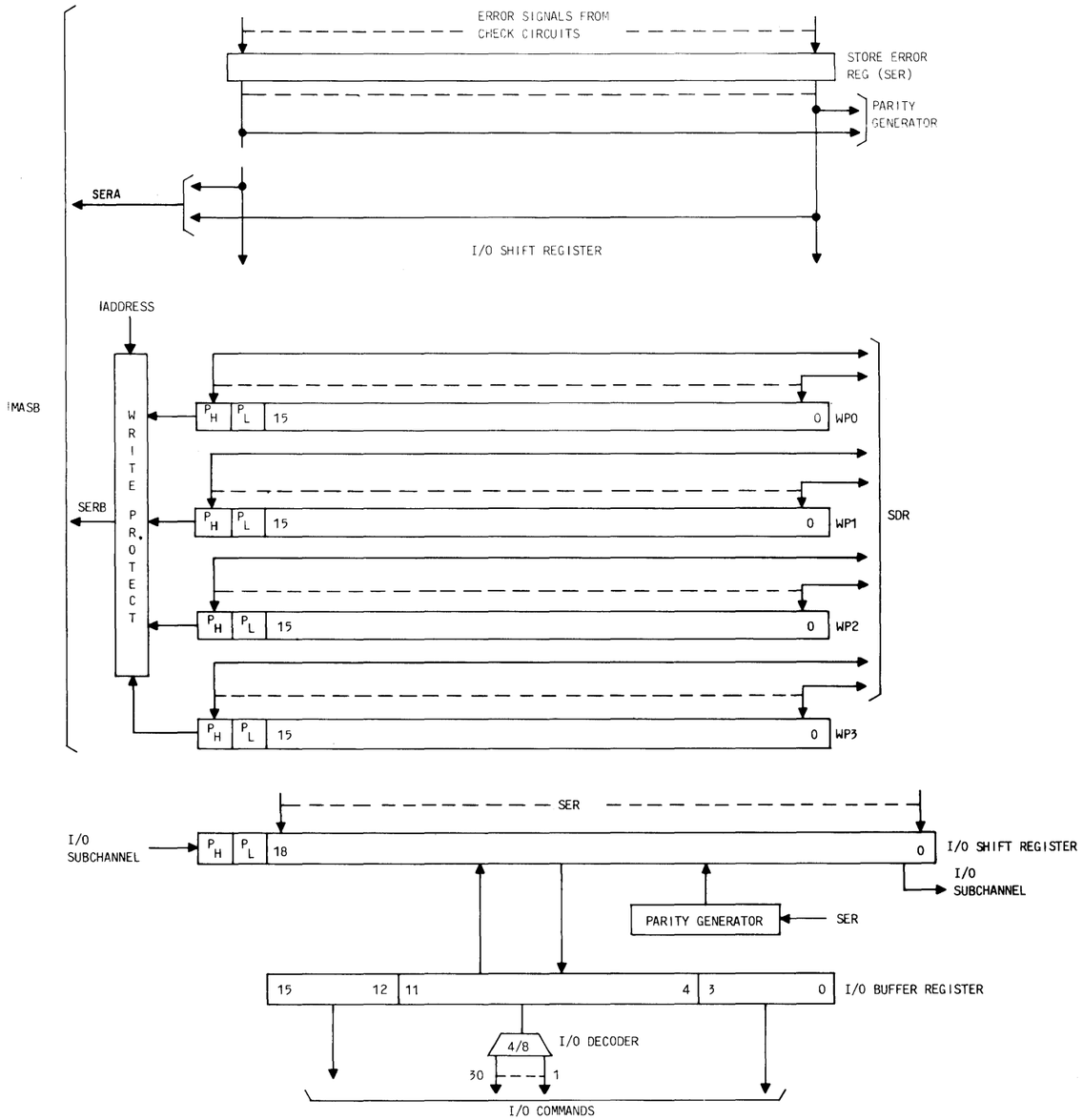


Fig. 13—Main Store Functional Block Diagram

TABLE C

BIT ASSIGNMENTS FOR THE FA1060 BIT-SLICED BOARDS

BIT-SLICED BOARD NUMBER	ASSIGNMENT
0	Bits 0 and 8 of the store address register, store data register, refresh address register, and error register
1	Bits 1 and 9 of the store address register, store data register, refresh address register, and error register
2	Bits 2 and 10 of the store address register, store data register, refresh address register, and error register
3	Bits 3 and 11 of the store address register, store data register, refresh address register, and error register
4	Bits 4 and 12 of the store address register, store data register, refresh address register, and error register
5	Bits 5 and 13 of the store address register, store data register, refresh address register, and error register
6	Bits 6 and 14 of the store address register, store data register, refresh address register, and error register
7	Bits 7 and 15 of the store address register, store data register, refresh address register, and error register
8	Bits P_L and 16 of the store address register and refresh address register; bits P_L and P_H of the store data register (Note)

Note: P_L of the store address register and refresh address register is a parity bit over bits 0 through 7 of the address. P_L of the store data register is a parity bit over bits 0 through 7 of data. P_H is the parity bit over bits 8 through 15 of data.

- Isolation check inputs tied to the zero outputs of ER under diagnostic control

When a bit is set in the ER, an SERA signal is generated and placed on the bus to inform the 3A CC. When the on-line 3A CC recognizes SERA, appropriate action (by the 3A CC) can be taken. The ER contents are read by the 3A CC via the I/O (diagnostic) channel.

MEMORY

4.15 Memory data is stored in 4K-bit or 16K-bit chips located on memory planes. A group of 9 memory planes (and dedicated fanout board) comprise a main store memory module which is an addressable entity of 32K or 128K, 18-bit words. The following signals are provided to the memory planes from the fanout board:

- Read/write
- Row address (multiplexed for 16K)
- Column address (multiplexed for 16K)
- 4K-bit chip select address
- 16K-bit chip select address
- Chip select
- Memory enable (4K only)
- Refresh enable

- Timing signals.

4.16 Read/write, row address, column address, 16K, and 4K-bit chip address are derived from information received on the bus. Chip select and memory enable are derived from the MASC timing shift register. Chip select and the decoded (3 address bits) 4K-bit chip select are combined to provide an enabling signal to the selected 4K-bit chips. Memory enable is necessary to gate memory data from the memory planes to the MASC data register when the 4K chips are used. A refresh signal (from fanout boards) is present on all memory planes of an MAS during a refresh interval. During refresh, the row address (6 address bits) bits are active and determine which one of the 64 rows of each 4K-bit chip in the MAS is to be addressed (Fig. 7). The 16K-bit chip receives a 7-bit row address (Fig. 10). A refresh causes the addressed row to be read from the 4K chips. With the 16K chip, refresh does not cause any stored data to be read. Reading causes the stored data to be rewritten or refreshed.

TERMINATIONS

4.17 The MASC is powered by +3 volts and the MAS memory modules by +5 volts. Logic levels between the two assemblies are different and, therefore, require conversion to be compatible with the circuitry receiving the signals. To provide the necessary logic level conversion at the MASC, resistor termination boards (959A) are mounted on the rear of the MASC. The resistors on these boards are wired to +3 volts and terminate the data and error signals from the MASMO. The resistor termination boards (959B) mounted on the MASM are wired to +5 volts and terminate the data and control signals from the MASC. The resistor combinations on each resistor termination board provide the proper impedance (approximately 100 ohms) and voltage level. Power control and alarms between the MASC and the MASM power are not required to be terminated in the 959A/959B boards.

CONTROL AND TIMING

4.18 The control and timing functional area comprises basic timing for MAS activities. Timing pulses are derived from the outputs of a 14-bit timing shift register (Fig. 13, Fig. 14). This register is activated by SGO or a refresh request. The shift rate, every 67 ns, is controlled by the MAS crystal oscillator clock circuit. The MAS responds to control signals from the 3A CC via the following major bus leads:

- Store complete
- Store error A
- Store error B
- Store error C.

4.19 Before the 3A CC issues a command to MAS, the 3A CC first checks the SCM, SERC, and SGO bus leads to determine whether the MAS is processing a previous 3A CC command. When the 3A CC detects an idle condition, it activates the SGO bus lead which prepares the MAS to receive a command, address, and subsequently data when a write command is to be performed (Fig. 13). An additional MAS bus lead, SBY, is not used by the 3A CC but is used between MASs in a multistore system. The SBY lead between MASs prevents the possibility of more than one MAS responding to a single 3A CC command.

4.20 When the MAS has completed its response to a command, SCM is generated by the MASC and placed on the bus. The 3A CC recognizes SCM and removes SGO. The removal of SGO will enable SBY to be reset when the MAS timing shift register is idle. A reset SBY will cause SCM or SERC to be removed from the bus. The MAS is now available to receive another command or perform a refresh cycle. SERC informs the 3A CC that bad parity was detected by the MAS during a memory read operation. This causes the 3A CC to initiate corrective action. When operating in duplex mode, SERC causes the 3A CC to read the other MAS. When operating in simplex mode, the 3A CC activates the store-complement write (SCW) bus lead and sends a write command to the MAS. The 3A CC then activates the store-automatic-correction (SAC) bus lead and sends a read command. This action double complements (complement correction) the data (and parity) and provides the 3A CC with correct data. Complement correction provides correct (memory read) data when the bad data bit logic level remains constant.

4.21 Another function of control and timing is the decoding of 2-out-of-4 commands from the 3A CC. A command must be present on the bus to read or write the memory or write-protect

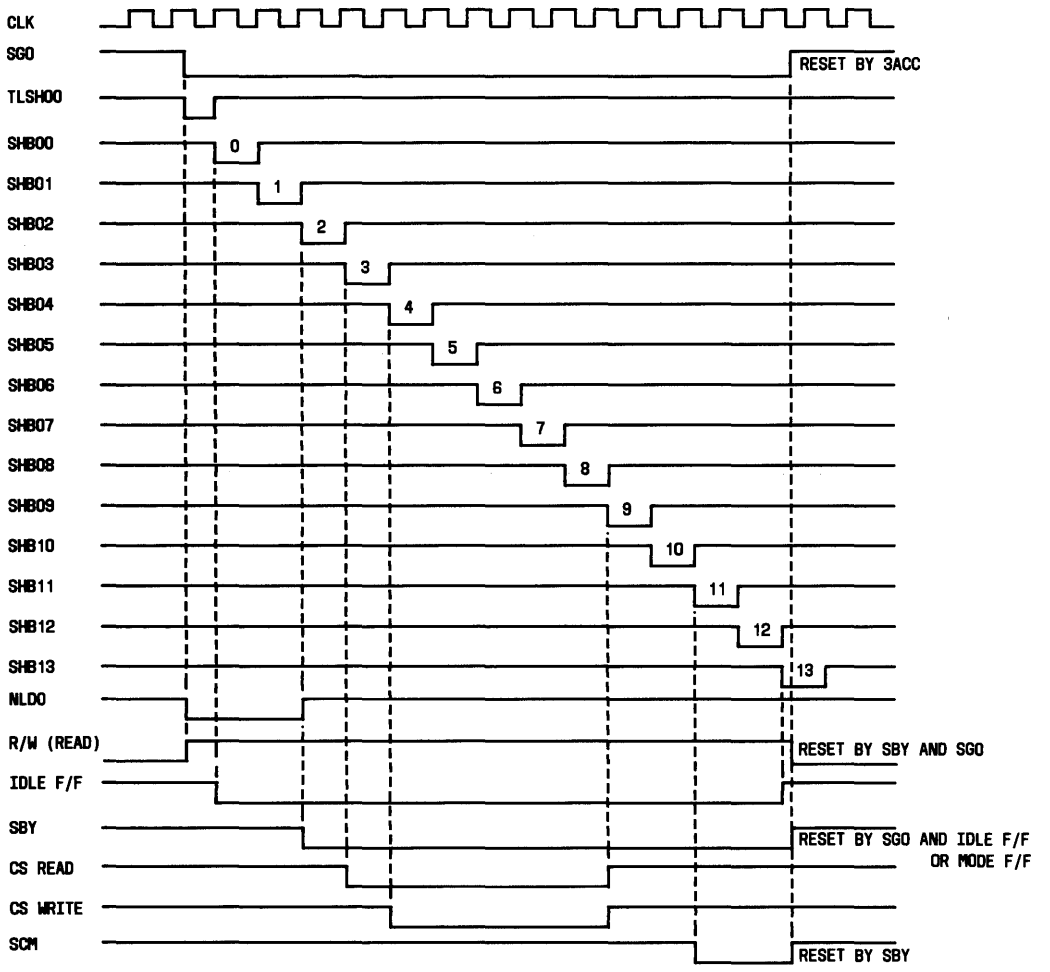


Fig. 14—Main Store Timing

registers. The 3A CC transmits commands to the MAS via bus leads SC0 through SC3. The MASC decodes 2-out-of-4 commands to cause the MAS to read or write. Four active (six possible) commands (Table B) are transmitted from the 3A CC to the MAS. Test circuitry checks for improper commands and sets a bit in the store error register when a command error is detected. Blind-write (not an active command) causes write-protected areas of memory to be written when enabled by an MASC backplane wiring option.

REFRESH CONTROL

4.22 Refreshing is accomplished by reading an addressed row of each memory DIP in an MAS. Circuitry inherent to the DIP causes the stored voltage level to be regenerated during a read. A 6-bit row address register in the MASC determines which of the 64 rows of each DIP will be refreshed. The 16K-bit chip uses a 7-bit row address register to determine which one of the 128 rows will be refreshed. A refresh request counter in the MASC counts the 67 ns clock pulses and generates a refresh enabling pulse every 34.3 μs. The address register is incremented to the next row address at the end of a refresh operation. The refresh request counter output is compared to the output of a duplicate refresh request counter. If the outputs do not occur at the same time, a bit is set in the store error register. The output of the store error register causes an SERA to be generated. When an MAS is responding to a 3A CC command, refreshing is delayed. When an

MAS is in a refresh cycle, response to a 3A CC command is delayed until the refresh cycle is completed.

DIAGNOSTIC ACCESS

4.23 Each 3A CC has a serial I/O channel to its dedicated MAS and an additional channel to the "other" MAS. A serial I/O channel consists of two coaxial cables (one to the MAS and one returning from the MAS) (Fig. 15). Diagnostic access between a 3A CC and the "other" MAS is granted when a store maintenance state (SMS) signal is placed on the parallel bus between a 3A CC and its dedicated store. Diagnostic access to the MAS is principally through the I/O interface. (The parallel bus is also used.) One of the coaxial cables transmits a 21-bit bipolar pulse serial message (Fig. 16) from the 3A CC to the MAS. The other coaxial cable returns the contents of the MAS error register or the same message that was sent by the 3A CC to the 3A CC in a loop-around fashion (Fig. 17). The return message is also a serial 21-bit bipolar pulse message. The parallel bus is also used during some diagnostics such as testing command decoders. To ensure that the MAS has properly received the 21-bit message, two tests are performed in the MAS on the 21-bit message. Bits 0 through 2 form the maintenance start code (101) and are decoded (Fig. 15). Should the MAS circuitry not receive or decode these bits (101) properly, the 21-bit shift register data contents may not be acted on by the MAS and the 3A CC may not receive an MAS I/O response. The 3A CC will time-out if no response is received from the MAS.

4.24 The MAS checks parity over the 21-bit shift register. Should parity be bad, a return start code of 011 and eighteen 1s (21 bits total) are returned to the 3A CC. Start code 011 indicates a message return to the 3A CC. Sixteen bits of the 21-bit message in the shift register are parallel-gated to a buffer. Eight of the bits in the buffer are encoded in a 4-out-of-8 code. The other 8 bits are called option bits and are supplemental to the 4-out-of-8 message. The 4-out-of-8 messages and option bits force MAS circuitry to be exercised to detect problem conditions. One of the 30 decoded 4-out-of-8 commands is an instruction to read the error register. The MAS circuitry generates parity bits (P_H, P_L) for the 16-bit error register and the 18 bits are parallel-gated to the 21-bit shift register. The 21-bit binary bit stream is then serially shifted out through the I/O logic conversion circuitry and appears at the I/O interface as bipolar pulses to the 3A CC. Bipolar pulses received by the MAS are converted to positive logic binary pulses before being shifted into the 21-bit shift register. The 21-bit diagnostic messages sent from the 3A CC to the MAS are formulated from diagnostic tests read from magnetic tape. Table D lists the tests performed by the 3A CC on the MAS.

5. POWER AND ALARM CIRCUITS

INTRODUCTION

5.01 Each MAS contains all necessary power converters except one external +5 volt converter. This power converter supplies the power to the resistor termination boards (on the MASM) and is located in the lower left corner of each bay of the 3A CC processor frame. Table E lists the MAS power converters and control circuit packs used in each bay of the processor and supplementary store frame. Standard -48 volt and +24 volt power is required as input to the converters. Each MAS power converter contains circuitry to generate a power alarm and fuse alarm. These alarms will be discussed in paragraph 5.06. Each supplementary store frame J1C065A contains a J1C064A supplementary main store power unit. The J1C064A contains STA and STB relays, fuses to protect -48 volt and +24 volt power, and one or two +5 volt power converters which provide +5 volts for the 959B resistor termination boards in the supplementary store frame.

POWER CIRCUITS

5.02 Standard -48 volt and +24 volt power, fused in the processor and supplementary store frames, is required for power converter inputs. Circuit pack FB152 (part of the 3A CC) supplies +12 volt reference to the FC21 circuit packs in the MASCs. Resistive voltage dividers on the FC21 circuit packs utilize this +12 volts to provide the +3 volt reference necessary for the +3 volt power converters. When +24 volts is applied to the MAS power converter start leads, the converters are activated.

DISTRIBUTION

5.03 Outputs from the +3 volt power converters are distributed to the circuit packs of the

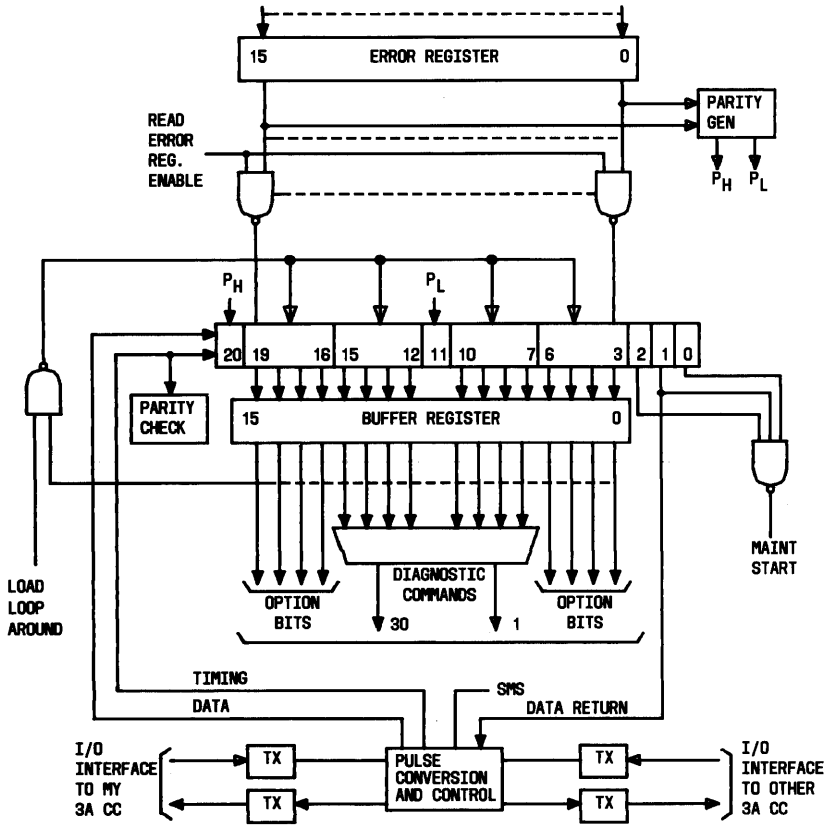


Fig. 15—Main Store I/O and Shift Register

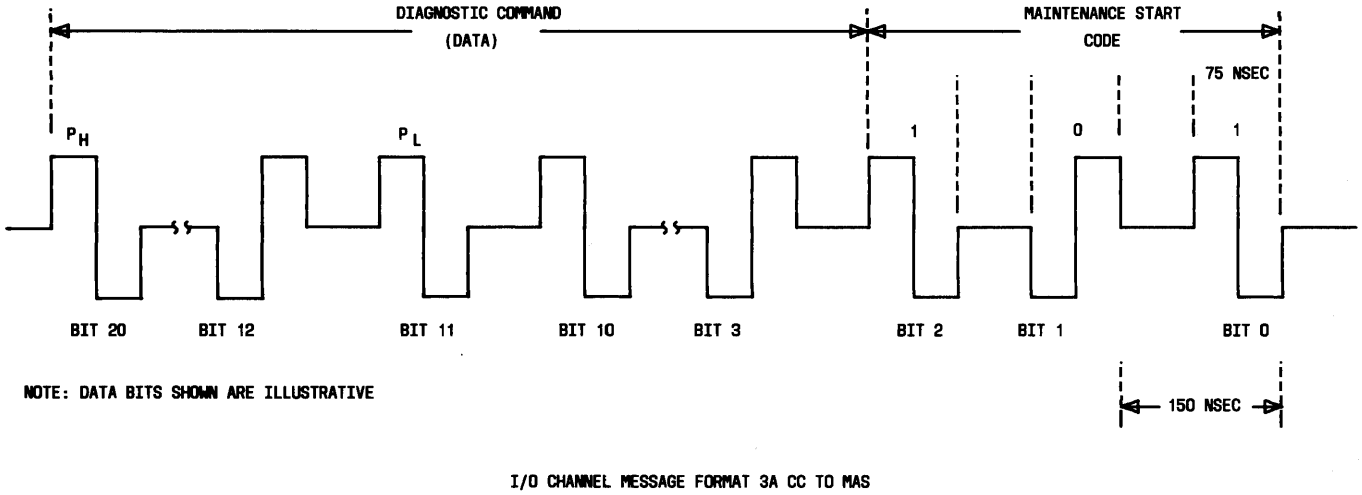


Fig. 16—I/O Channel Diagnostic Message Format 3A CC to MAS

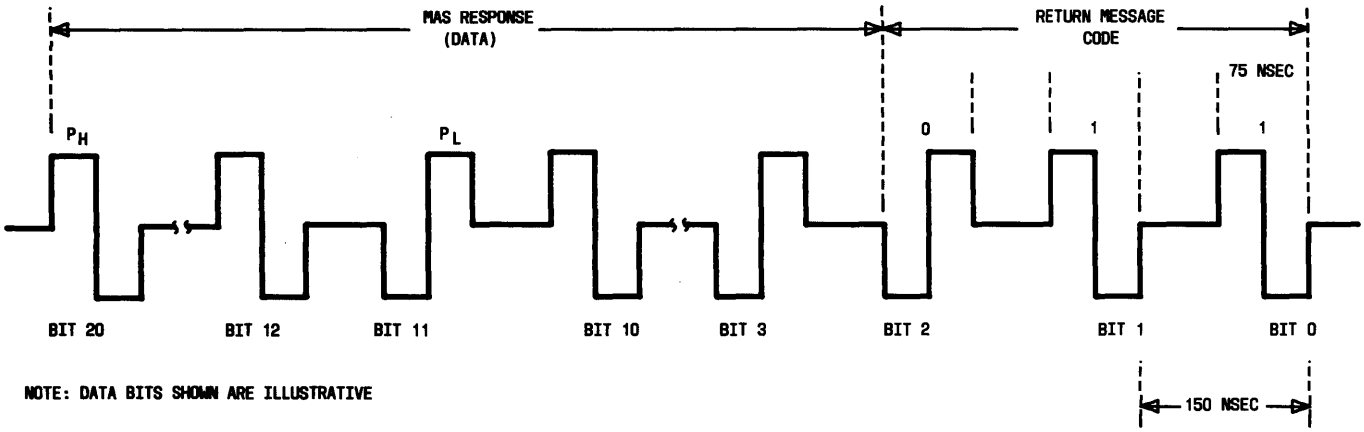


Fig. 17—I/O Channel Message Format MAS to 3A CC

MASC. Outputs from the +12, -5, and +5 volt converters are distributed to their associated memory planes and fanout boards. The MAS circuit packs receive power and ground via multilayer backplane wiring boards. The MASM resistor termination assemblies receive +5 volts from a dedicated power converter in the bottom of the bay.

CONTROL

5.04 Power to the MAS is controlled by applying or removing a +24 volt signal to the start leads of the power converters. These +24 volt start signals are generated by the 3A CC when the POWER ON key on the 3A CC is depressed (Fig. 18). For start-up, the start A (STA) signal is first applied to the +3 volt power converters in the MASC, to the +5 volt power converters in the MAS memory units, and to the +5 volt power converter in the bottom of the bay (Fig. 19). This figure illustrates only the 4K configuration. After a delay of approximately 1/2 second, the start B (STB) signal is applied to the FC262 circuit pack in the MASC. Circuit pack FC262 in turn applies the STB signal to the +12, -5 volt power converters. For normal shut-down, all +24 volt start signals to the MAS are removed simultaneously and the output of all power converters are turned off. Each supplementary store frame contains an STA and STB relay (part of J1C064A) under the control of its associated 3A CC. The relays, when energized, distribute fused +24 volt start voltages within the supplementary store frame.

5.05 The +5 volt and +12, -5 volt power converters on each MAS memory unit are electrically interlocked so that the +12, -5 volt power converters cannot start unless the +5 volt power converter output is at least +4.5 volts. If the STB signal is applied to the +12, -5 volt power converter and the output of its associated +5 volt power converter is below +4.5 volts, a fuse alarm (FA) is generated.

ALARM CIRCUITS

5.06 Each power converter contains alarm circuits to generate a power alarm (PA) and an FA. When any power converter or FC262 circuit pack generates an FA, the 3A CC processor bay alarm circuitry shuts down all power converters in the processor bay and associated supplementary store frame. This is accomplished via the removal of STA and STB voltages. A power converter which generates an FA, shuts itself down but keeps the red light emitting diode (LED) on until turned off by a power reset switch on the processor bay. A power converter generates an FA when its output voltage exceeds a level which could damage the load or when too much current is drawn from the output. A power converter generates a PA, but continues to function, when its output voltage falls outside the normal regulating range.

5.07 The PA signal from the +5 volt (external) power converter and the +5 volt MASM power converters is routed to the FC262 circuit pack which converts this PA to an FA and removes

TABLE D

STORE DIAGNOSTIC TESTS

TEST NO.	DESCRIPTION
27*	Unlock and Test On-Line CC I/O Access to Off-Line Store
28	Store Controller I/O Order Decoder
29	One Half of Store Controller Multiplexor Circuits
30	Other Half of Store Controller Multiplexor Circuits
31	One Half of Store Controller Multiplexor Check Circuits
32	Other Half of Store Controller Multiplexor Check Circuits
33	Store Command Portion of Store Bus
34	Store Address Portion of Store Bus
35	Store Data Portion of Store Bus
36	Store Data Portion of Store Bus
37	Bus Control Circuitry
38	Data Parity Control Circuitry
39	Data Parity Control Circuitry
40	Data Parity Check Circuits
41	Refresh Select Signals to Fanout Boards
42	Normal Select Signals to Fanout Boards
43	Store Address Signals Through Fanout Board
44	Store Address Signals Through Fanout Board
45	Fanout Board Address Parity Checkers
46	Fanout Board Address Parity Checkers
47	Store Timing Signals Through Fanout Boards
48	Store Timing Signals Through Fanout Boards
49	Write Protect Reads and Writes
50	Write Protect Reads and Writes
51	Write Protect Check Circuit
52	Store Bus From On-Line CC to Off-Line CC
53	Data Register To/From Memory Modules
54	Data Register To/From Memory Modules
55	Data Register To/From Memory Modules
56	Data Register To/From Memory Modules
57	Memory Module 0
58	Memory Module 1
59	Memory Module 2 ⎫
60	Memory Module 3 ⎪
61	Memory Module 4 ⎪ These Tests Not Performed
62	Memory Module 5 ⎪ for 128K Memory Modules
63	Memory Module 6 ⎪
64	Memory Module 7 ⎭

* The first 26 tests verify that the 3A CC is ready to test the main store.

the STB signal from all +12, -5 power converters in the MAS. The PA from the (external) +5 volt power converter and the MASM +5 volt power converter is also routed to the processor bay alarm circuitry via the FC262 circuit pack. The PA from the +3 volt power converter and the +12, -5 volt converter bypasses the FC262 circuit pack and is routed to the processor bay alarm circuit. The +12, -5 volt power converter contains an FA not normally found. Should the -5 volt output drop below a predetermined level (toward zero), an FA is generated which causes the removal of

TABLE E

MAIN STORE POWER CONVERTERS AND POWER CIRCUIT PACKS

CONVERTER DESIGNATION	OUTPUT VOLTAGE & CURRENT	NO. USED
J87389F-2	+3 Volts, 5A	4 Per MASC
J97421A-1	+5 Volts, 5.6A	1 Per 64K of Memory
J87421A-2‡	+5 Volts	1 Per 128K of Memory
J87422B-1	+12 Volts, 2A —5 Volts, 0.5A	1 Per 64K or 128K of Memory
J87389J-2*	+5 Volts, 4A	1 Per Processor Frame Bay
J87421A-2†	+5 Volts, 7A	1 or 2 Per Supplemental Store Frame
CIRCUIT PACK	**FUNCTION**	
FC21	+3 Volt Power Reference and Filter	2 Per MASC
FC262	Power Control	1 Per MASC

* Not physically part of main store. Located in bottom part of processor bay.

† Not physically part of main store. Located in power unit of each supplemental store frame. When second and third main stores are added, a second power converter is added.

‡ 16K-bit chip configuration.

STB from the +12, -5 volt power converters of the MAS. Table F lists the causes of FA and PA alarms in the MAS.

5.08 The power alarm feature of all power converters and the FC262 circuit pack (Fig. 20) is tested by applying a power alarm test (PAT) signal from the 3A CC control panel or via software and checking that each power converter generates a PA. During this test, all power converter LEDs are lighted as well as the LED on the FC262 circuit pack. When the test is successful, all LEDs are extinguished at the end of the test.

5.09 The bus termination resistor assemblies are wired such that a path to ground is maintained from the FC262 circuit pack through all the bus termination assemblies in series (Fig. 19). Failure to maintain continuity causes the FC262 circuit pack to generate an FA. When the 3A CC detects an FA, the off-line 3A CC and MAS are switched on-line and the faulty 3A CC—MAS is made available for diagnostics. The MASC FC262 circuit pack senses FAs from the 3A CC and removes STB from the +12, -5 volt power converter to protect the memory chips from possible damage. The LED on each power converter stays lighted as long as an alarm condition exists. The PA signal from the +3 volt and +12, -5 volt power converters does not cause the LED to light on circuit pack FC262.

5.10 Each supplementary store frame power unit (Fig. 2, Fig. 20) generates a +FA signal when a +24 volt fuse blows and a -FA signal when a -48 volt fuse blows (Fig. 18, Fig. 20). Both FAs are cabled to their dedicated processor bay alarm circuitry. An FA causes STA and STB voltages to be removed from the processor bay and supplementary store frame power converters.

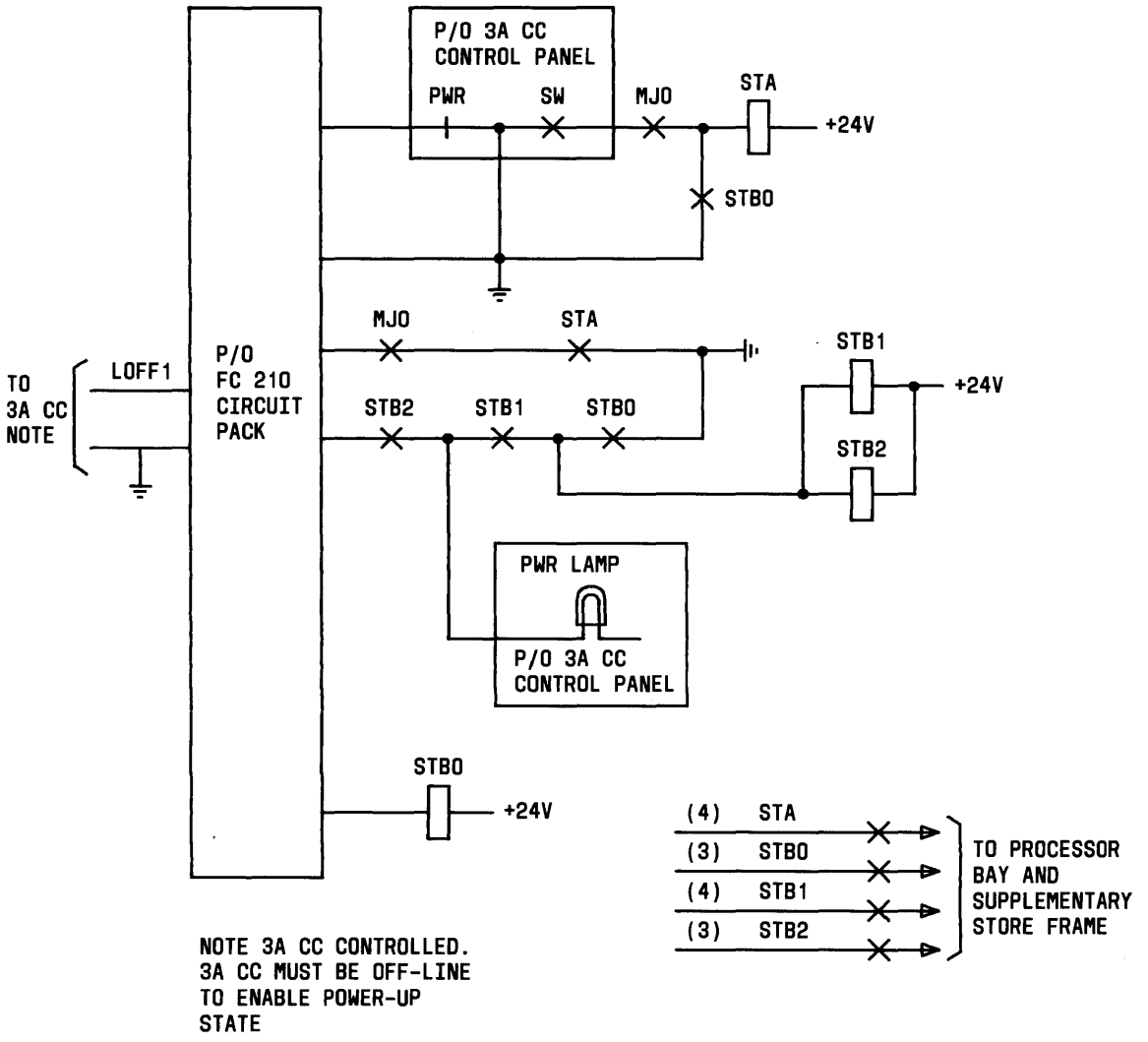


Fig. 18—Processor Frame—Bay Power Control

6. MAINTENANCE

INTRODUCTION

6.01 The capability of the on-line 3A CC to switch control to the off-line 3A CC—MASs helps to ensure uninterrupted service and provides maintenance personnel access to the faulty (off-line) 3A CC—MASs. Maintenance personnel are guided to probable faulty circuit packs via system error messages, power alarms, and error messages generated as as result of software provided diagnostics.

BUILT-IN FEATURES

6.02 The on-line 3A CC has the capability to read the off-line MASs without switching, if the on-line MAS data word has a parity error. When operating in simplex mode, the 3A CC employs SCW and SAC to obtain a valid data word. The MAS error signals and I/O circuitry are the stimulus and access, respectively, for MAS maintenance. The MAS fuse and power alarm conditions cause audible and visual alarms to be activated. The maintenance TTY prints fuse and power alarm conditions, and MAS error messages. The error message condition causes other types of system alarms such as critical, major, and minor.

6.03 The TTY is used to initiate diagnostics (refer to appropriate system diagnostic documentation). Trouble messages resulting from diagnostics are printed by the TTY and direct the craftsperson to appropriate maintenance action via the trouble locating manual. The most probable order of circuit pack failure is listed in the trouble locating manual.

6.04 The 3A CC control panel contains switches and lamps (Table G) to be used in the performance of manual functions on the MAS. This panel is used in diagnosing the MAS if diagnostics have been unsuccessful.

6.05 Instructions for initializing and diagnosing the MAS are contained on magnetic (cartridge) tape. The instructions are accessed via the tape data controller. A typical list of MAS diagnostic tests is contained in Table D. Requests for MAS diagnostic tests are made via the TTY. Diagnostic tests are first stored in the on-line MAS. The on-line 3A CC then diagnoses the off-line MASC via the I/O and parallel buses. Should the MASC pass its tests, the fanout boards (of the MASMOs) are tested. If the fanout boards are found to be good, the first 32K (4K-bit chip) of memory cells (MASMO 0) are tested. When the first 32K of memory is verified good, the on-line 3A CC causes the next test to be stored in MASMO 0 of the off-line MAS. The on-line 3A CC controls and evaluates the remaining tests via the off-line 3A CC. If on-line 3A CC detects a failure during diagnostics, a message is printed on the maintenance teletype. The 16K-bit chip configuration is tested in a similar manner.

7. REFERENCES

7.01 The following is a list of sections and drawings which are germane to this section:

- J1C052A—ESS Common Systems Main Store Controller Unit
- J1C052B—Common Systems Main Store Controller and Memory Unit
- J1C065A—Common Systems ESS Supplementary Store Frame
- Section 232-309-101—2B Processor Description No. 2B Electronic Switching System
- Section 254-300-110—3A Central Control Description Common Systems
- Section 254-300-120—3A Central Control Theory Common Systems
- Section 254-300-180—System Status Panel Common Systems
- 3A Processor Power System Common Systems.

8. GLOSSARY

8.01 A glossary of terms is provided to aid in the understanding of definitive words used in this section.

Asynchronous—Functional units operate/interface without predetermined time relationships.

Bipolar—A square wave pulse representing a logic 1 or 0. Half of the pulse is above a reference line and half below the reference line.

Bit-Sliced—Two bits of data occupy each circuit pack.

Complement—Changing logic 1s to logic 0s and logic 0s to logic 1s.

Control Unit (CU)—That part of a system which consists of a 3A Central Control, main store, store buses, and system status panel.

Dynamic—Memory requires refreshing at definite intervals or stored information will be lost.

Four-Out-of-Eight (4/8)—Four, only four, bits out of eight must be logic 1s.

Fuse Alarm (FA)—A catastrophic alarm generated by the main store to inform maintenance personnel that a power converter output voltage or current has exceeded a safe limit.

Input/Output (I/O)—The diagnostic serial interface between the 3A Central Control and main store.

Insulated Gate Field Effect Transistor (IGFET)—The storage element for one bit of data.

M-Out-of-N Codes—M-out-of-n means that ***m*** number of 1s must be present in ***n*** number of bits. For example, 4-out-of-8 means that no more

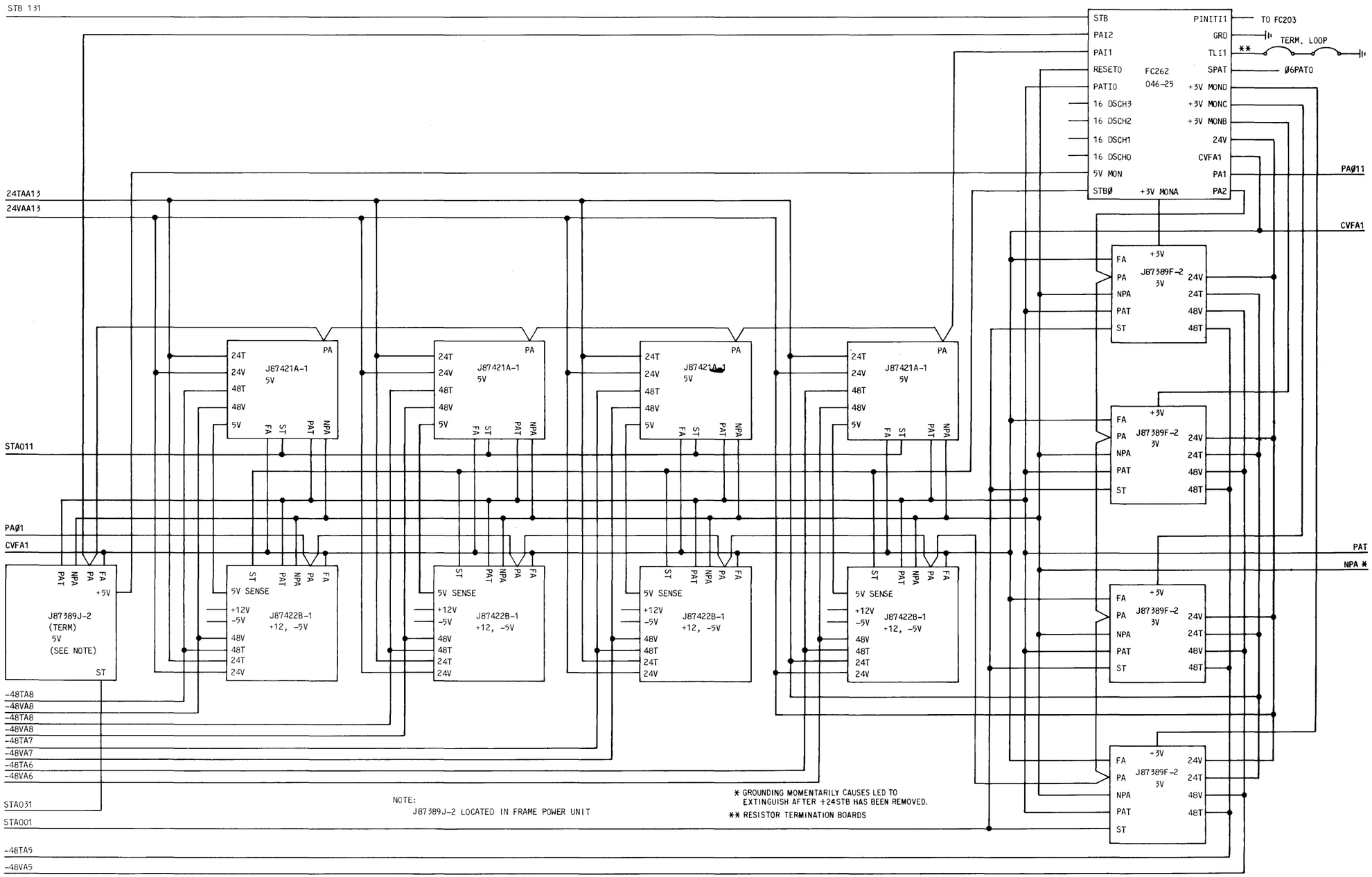


Fig. 19—Main Store Power Block Diagram

TABLE F

MAIN STORE POWER ALARMS

CONVERTER DESIGNATION	FUSE ALARM CONDITION	POWER ALARM CONDITION
J87389F-2 (3V)	Output Missing High Output Current Voltage Out of Range	Voltage Out of Tolerance
J87421A-1 (5V)	Output Missing High Output Current Voltage Out of Range	Voltage Out of Tolerance (Causes FC262 to Generate Fuse Alarm)
J87421A-2	Output Missing High Output Current Voltage Out of Range	Voltage Out of Tolerance (Causes FC262 to Generate Fuse Alarm)
J87422B-1 +12V —5V	High Output Current Voltage Out of Range —5 Volts Low	Voltage Out of Tolerance
J87389J-2* (5V)	Output Missing High Output Current Voltage Out of Range	Voltage Out of Tolerance (Causes FC262 to Generate Fuse Alarm)
J87421A-1†	Output Missing High Output Current Voltage Out of Range	Voltage Out of Tolerance (Causes FC262 to Generate Fuse Alarm)
J87421A-2‡	Output Missing High Output Current Voltage Out of Range	Voltage Out of Tolerance (Causes FC262 to Generate Fuse Alarm)
Bus Termination Resistor Assembly 959A, 959B	Assembly Not Plugged In	Not Applicable

* Not physically part of main store. Located in bottom part of processor bay.

† Not physically part of main store. Located in power unit of each supplemental store frame. Used for 4K-bit chip configuration.

‡ When second and third main stores are added, second power converter is added.

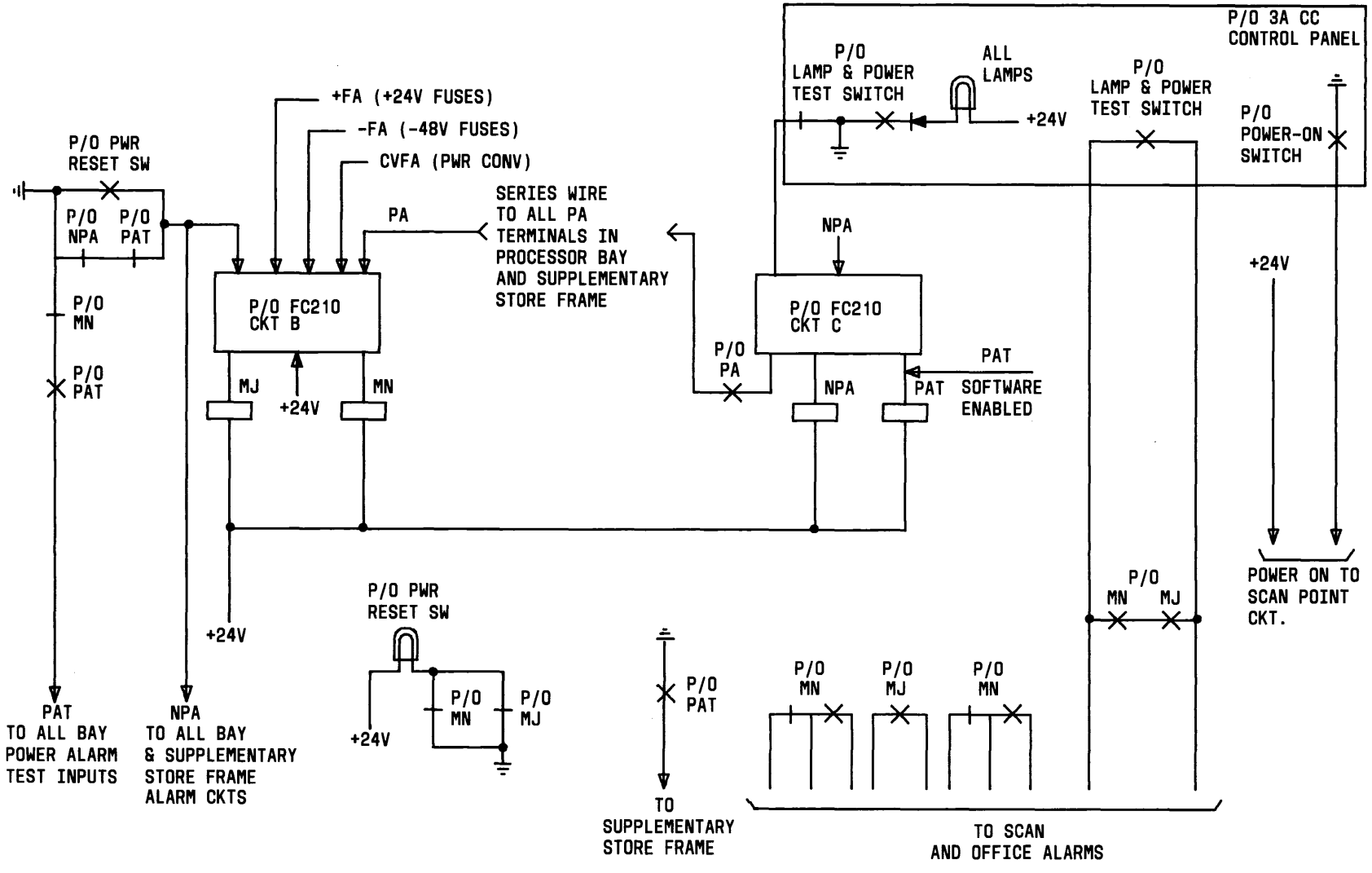


Fig. 20—Processor Frame Power Circuit—Power and Power Alarm Test

TABLE G

3A CC PANEL MEMORY SWITCHES

AREA	DESIGNATION	COLOR	INDICATION OR FUNCTION
MEMORY	INCR ADR (Switch)	White	Increments the contents of the store address register by one.
	STORE (Switch)	White	Writes the contents of the store data register into the main store at address in the store address register.
	DISPLAY (Switch)	White	Reads the main store at the address in the store address register and displays the contents of that location.
	HIGH BITS/ LOW BITS (Switch)	White	This switch in the normal (down) position allows the display or storage of bits 0 through 15 of data in a main store location. This switch in the operated (up) position allows the display or storing of bits 16 through 23 of data in a main store location. The operated (HIGH BITS) position is not effective unless the BASIC/ EXTENDED switch is in the up (EXTENDED) position.

or no less than four 1s will always be present. The associated decoder check circuits ensure that the number of 1s is correct. If an incorrect code is detected, an error is indicated.

Main Store (MAS)—An addressable memory storage unit capable of storing up to 256K 18-bit words.

Main Store Bus (MASB)—The parallel bus (53 leads) connecting the 3A Central Control and the main store, and 54 leads connecting main store to main store.

Main Store Controller (MASC)—A part of the main store which interfaces with the 3A Central Control and controls the internal operations of the main store.

Main Store Controller and Memory Unit (MASCM)—An assembly containing a main store controller and a main store memory unit.

Main Store Memory Module (MASMO)—32K (32,768) words or 128K (131,072) of memory storage capacity. Also the smallest increment of memory growth.

Main Store Memory Unit (MASM)—A subassembly of the main store into which two main store memory modules may be installed to provide 64K of memory storage.

Power Alarm (PA)—A noncatastrophic alarm generated by a power converter in the main store to inform maintenance personnel that a power converter output voltage is outside the normal regulating limits.

Refresh—The act of restoring the stored data bit in an insulated gate field effect transistor memory cell.

Serial—A stream of data bits on a single pair of wires or coaxial cable.

Start A (STA)—A signal which causes selected main store power converters to produce an output.

Start B (STB)—A signal which causes selected main store power converters to produce an output.

Store Automatic Correction (SAC)—A signal from the 3A Central Control to the main store to read and complement a data word.

Store Busy (SBY)—A signal for control of a main store when more than one main store is used in a system. This signal also is used to reset the store-complete and store error C bus signals.

Store Complement Write (SCW)—A signal from the 3A Central Control which causes a data word to be complemented and rewritten into the same memory address.

Store Complete (SCM)—A signal on the parallel bus to inform the 3A Central Control that the main store has completed its response to a command.

Store Error A (SERA)—An error signal from the main store to the 3A Central Control to inform the 3A Central Control that a possible fatal error has occurred.

Store Error B (SERB)—An error signal from the main store to the 3A Central Control to inform the 3A Central Control that an invalid attempt has been made to write a write-protected area of memory storage.

Store Error C (SERC)—An error signal from the main store to the 3A Central Control to inform the 3A Central Control that data read from memory storage has bad parity.

Store Go (SGO)—A signal from the 3A Central Control to the main store to inform the main store that a command is present.

Store Request (SREQ)—An unused main store bus lead, provided for future uses of the main store—3A Central Control.

Transitory Data—Data, usually related to a call in proccess, temporarily stored in memory.

Two-Out-of-Four (2/4)—Two, and only two, of the four bits must be logic 1.

Write-Protect (WP)—Selected 4K groups of words in memory storage which are protected from being accidentally overwritten.