J1H011A SWITCH UNIT DATA DISTRIBUTOR CIRCUIT TESTS USING 124A TEST SET SD-1H070-01 NO. 101 ELECTRONIC SWITCHING SYSTEM

1. GENERAL

1.01 This section describes a method for testing the data distributor circuit when there are indications from the control unit teletypewriter or other sources that this circuit is the cause of switch unit failures.

This test should be performed only on the data distributor circuit associated with the off-line bus. This bus must remain powered.

1.02 The tests covered are:

A. Over-All Data Distributor Circuit Test: This test briefly checks the main functions of the circuit. It is intended to quickly determine if the data distributor circuit is operating properly, and if not, what subsequent tests are most likely to disclose the area at fault. The shift register, switch store transfer gates, parity counter, and wait pulse are tested.

B. Parity Alarm and Go Ahead Pulse: This test checks the ability of this circuit to produce an output pulse when a bad parity condition is simulated. It also checks for the scanner start pulse.

C. T and A Start: This test checks the ability of this circuit to produce an output pulse when a test message is addressed to the transfer and alarms circuit.

D. Attendant Start: This test checks the ability of this circuit to produce an output pulse when a test message is addressed to the attendant circuit.

E. Data Sequence Circuit Test: This test checks the ability of the timing logic to reproduce signals at the data bit rate. The wait, data input, reset 1, and reset 2 outputs are tested.

F. Shift Register Test: This test checks the ability of each shift register stage to be set to either a *0* or *1*. In addition, the shifting function of each associated monopulser is tested.

G. Set Function Test for Shift Register Stages 16 and 17: This test checks the logic associated with the insertion of the two start bits for the latter half of the 47-bit data message.

H. Not Time Slot 0 Test: This test checks the ability of the address gates to recognize a time slot 0 address.

I. Parity Counter Test: This test checks that a binary counter drive pulse is present for each data mark received. It also compares the operation of the parity binary counter with the one in the on-line data distributor circuit. For this latter test, it is assumed normal traffic data messages are being received from the control unit.

J. Comparator and End of Write Function Test: This test checks the *end of write* function. It also checks the operation of the time slot number comparator. For this test, normal traffic data messages are required.

K. Switch Store Transfer Gates Test: This test checks for the proper state of each of the 42 switch store transfer gates when either *all 0* or *all 1* data is present.

1.03 ***Caution: The proximity of the data distributor to on-line circuits makes it imperative that extreme caution be used when attaching test set leads.***

1.04 Part 4 of this section is chronologically arranged to provide an initial over-all test of the data distributor circuit by performing Tests A, B, C, and D. Subsequent tests examine the circuit in more detail.

1.05 Certain tests require assistance at the control unit. Test messages, when required to perform these tests, must be originated by an appropriate ***manual request*** teletypewriter print-in.

1.06 The control unit must be notified whenever an inadvertent disruption of service occurs as a result of testing. This includes blown fuses in both on-line and off-line circuits.

1.07 ***Lettered Steps:*** A letter a, b, c, etc, added to a step number in Parts 3 and 4 of this section, indicates an action which may or may not be required depending on test conditions. The condition under which a lettered step or a series of lettered steps should be made is given in the ACTION column, and all steps governed by the same condition are designated by the same letter within a test. Where a condition does not apply, all steps designated by that letter should be omitted.

2. APPARATUS

All Tests

2.01 124A test set, SD-1H070-01.

2.02 M3BP cord, power cable, 6 feet long (for patching battery from switch unit to test set).

2.03 Four W1BD cords (test lead, 8 feet long, equipped with test point contact spring and pin plug).

2.04 731A (key, extractor) tool (for CP removal).

Tests A, B, C, E, F, G, I, J, K

2.05 Five W1BE cords (test lead, 10 inches long, equipped with test point contact spring and alligator clip).

Tests A, F, K

2.06 W25B cord, testing cord, 6 feet long (for patching switch unit test position to 25 terminal test set connector, INPUTS 1-24).

Tests F, G, H, J, K

2.07 Three P1U cords (test lead, 10 inches long, equipped with pin plugs).

Tests F, H

2.08 W9B cord, testing cord, 6 feet long (for patching various switch unit test points to 9 terminal test set connector, INPUTS 25-32).

3. PREPARATION

STEP	ACTION	VERIFICATION
All Tests		
1	Connect power to test set.	

4. METHOD

STEP	ACTION	VERIFICATION
	A. Over-All Data Distributor Circuit Test	
2	On test set — Connect INPUTS 1-24 to switch unit test socket at 29B17. Rotate DIAL A to test message 1.	
3	Operate DIAL A keys to test message 1.	
4	Request test message 1 be transmitted to switch unit from control unit.	
5	Operate RST1 key momentarily.	On release of RST1 key — MSG IND 1 lamp lighted. ***Note:*** On failure to verify, proceed to Test E and subsequent tests.

STEP	ACTION	VERIFICATION
6	Move test cord from 29B17 to 29B20.	
7	Repeat Step 5.	Same as Step 5.
8	Move test cord from 29B20 to 29B23.	
9	Rotate DIAL A to test message 4.	
10	Operate DIAL A keys to test message 4.	
11	Repeat Step 5.	Same as Step 5.
12	Request test message 2 be transmitted to switch unit.	
13	Rotate DIAL A to test message 5.	
14	Operate DIAL A keys to test message 5.	
15	Repeat Step 5.	Same as Step 5.
16	Move test cord from 29B23 to 29B20.	
17	Rotate DIAL A to test message 2.	
18	Operate DIAL A keys to test message 2.	
19	Repeat Step 5.	Same as Step 5.
20	Move test cord from 29B20 to 29B17.	
21	Repeat Step 5.	Same as Step 5.
22	Request test message 3 be transmitted to switch unit.	
23	Rotate DIAL A to test message 3.	
24	Operate DIAL A keys to test message 3.	
25	Repeat Step 5.	Same as Step 5.
26	Move test cord from 29B17 to 29B20.	
27	Repeat Step 5.	Same as Step 5.
28	Move test cord from 29B20 to 29B23.	
29	Rotate DIAL A to test message 6.	
30	Operate DIAL A keys to test message 6.	
31	Repeat Step 5.	Same as Step 5.
32	Remove test cord from 29B23.	
33	Operate SYNC DELAY to 800.	
34	Operate K1 to PULSE FREQ.	
35	Connect INPUT C to TP4 at 33B5 (CP181).	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. *Note:* No verification indicates a faulty CP181 at 33B5.
36	Connect ground to TP2 at 29D8 (CP307).	
37	Operate K1 to COMPARATOR.	

STEP	ACTION	VERIFICATION
38	Connect INPUT A to TP6 at 33B11 (CP75).	
39	In data distributor of other switch unit half — Connect TP6 at 33B11 (CP75) to INPUT B.	
40	Move INPUT C to TP3 at 29C14 (CP254).	
41	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted. ***Note:*** On failure to verify, proceed to Step 42, then Test I.
42	Remove INPUTS A, B, and C from switch unit.	
43a	If no further tests are to be performed at this time — Remove test set power connection.	

B. Parity Alarm and Go Ahead Pulse

2	On test set — Operate SYNC DELAY to 800.	
3	Operate K1 to PULSE FREQ.	
4	On transfer and alarms circuit (BAY 2) — Connect TP3 at 13A14 (CP276) to ground.	
5	Connect ground to: TP2 at 33A5 (CP87) TP1 at 33B14 (CP157) TP6 at 33B14 (CP157) TP4 at 33B2 (CP177)	
6	Connect INPUT C to TP6 at 33A14 (CP85).	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a bad CP85 at 33A14.
7	Remove ground from TP2 at 33A5 (CP87).	
8	Remove ground from TP3 at 13A14 (BAY 2).	
9	Connect TP6 at 33B17 (CP157) to ground.	
10	Connect TP1 at 33A5 (CP87) to ground.	
11	Move INPUT C to TP5 at 33A17 (CP90).	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a faulty CP90 at 33A17 or CP85 at 33A14.

STEP	ACTION	VERIFICATION
12	Remove grounds from: TP1 at 33A5 TP6 at 33B17 TP4 at 33B2 TP6 at 33B14 TP1 at 33B14	
13	Remove INPUT C from TP5 at 33A17.	
14a	If no further tests are to be made at this time — Remove test set power connection.	
	C. T and A Start	
2a	If scanner 1 is in service — Request test message 21 (switch to scanner 1) be transmitted to switch unit.	
3b	If scanner 2 is in service — Request test message 22 (switch to scanner 2) be transmitted to switch unit.	
4	On test set — Operate SYNC DELAY to 800.	
5	Operate K1 to PULSE FREQ.	
6	Connect TP4 at 33B2 (CP177) to ground.	
7	Connect INPUT C to TP1 at 33A23 (CP159).	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a faulty CP159 at 33A23 or CP75 at 33B11.
8	Remove ground from TP4 at 33B2.	
9	Operate SYNC DELAY to 3.	
10	Move INPUT C to TP5 at 33A14 (CP85).	PULSE FREQ pulses to approximately half scale about once per second. ***Note:*** No verification indicates a faulty CP85 at 33A14 or CP90 at 33A20.
11	Remove INPUT C from TP5 at 33A14.	
12	Request removal of test message transmission.	
13c	If no further tests are to be performed at this time — Remove test set power connection.	
	D. Attendant Start	
2	Notify attendant to ignore the state of the console common lamps during this test.	

STEP	ACTION	VERIFICATION
3	Request a teletypewriter print-in to transmit a test message for console 1 that will cause no change in the loop lamps and cause all common lamps to be dark except EXCL SRC which will light steadily.	
4	On test set — Operate SYNC DELAY to 3.	
5	Operate K1 to PULSE FREQ.	
6	Connect INPUT C to TP3 at 33A14 (CP85).	PULSE FREQ pulses to approximately half scale about once per second. ***Note:*** No verification indicates a faulty CP85 at 33A14 or CP90 at 33A20.
7	Request removal of test message transmission.	
8	Notify attendant 1 that this test is concluded.	
9	Remove INPUT C from TP3 at 33A14.	
10a	If no further tests are to be made at this time — Remove test set power connection.	
	E. Data Sequence Circuit Test	
2	On test set — Operate K1 to PULSE FREQ.	
3	Operate SYNC DELAY to 800.	
4	Connect INPUT C to TP4 at 33B11 (CP75).	
5	Connect TP2 at 29D8 (CP254) to ground.	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a faulty CP75 at 33B11 or CP161 at 33B8.
6	Move INPUT C to TP2 at 33B5 (CP181).	PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a faulty CP181 at 33B5.
7	Move INPUT C to TP4 at 33B5 (CP181).	Same as Step 6.
8	Remove ground from TP2 at 29D8 (CP254).	
9	Connect ground to TP4 at 33B2 (CP177).	
10	Move INPUT C to TP5 at 33B11 (CP75).	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a faulty CP75 at 33B11.

STEP	ACTION	VERIFICATION
11	Move INPUT C to TP1 at 33A23 (CP159).	PULSE FREQ reads 6.9 to 7.7. *Note:* No verification indicates a faulty CP159 at 33A23.
12	Move INPUT C to TP5 at 29C11 (CP75).	PULSE FREQ reads 6.9 to 7.7. *Note:* No verification indicates a faulty CP75 at 29C11.
13	Move INPUT C to TP2 at 33B11 (CP75).	PULSE FREQ reads 6.9 to 7.7. *Note:* No verification indicates a faulty CP75 at 33B11 or 29C11.
14	Move INPUT C to TP3 at 33A23 (CP159).	
15	Connect TP1 at 33B5 (CP181) to ground.	PULSE FREQ reads 6.9 to 7.7. *Note:* No verification indicates a faulty CP159 at 33A23.
16	Remove ground from TP1 at 33B5 (CP181).	
17	Remove ground from TP4 at 33B2 (CP177).	
18a	If no further tests are to be made at this time — Remove test set power connection to switch unit.	

F. Shift Register Test

2 On test set —
Make the following connections to the switch unit and between jacks on test set.

TEST SET INPUT	SWITCH UNIT TEST POINT
24	TP6 at 33B14 (CP157)
25	TP1 at 33B14 (CP157)
26	TP6 at 33B17 (CP157)
27	TP1 at 33B17 (CP157)
28	TP6 at 33B20 (CP157)
29	TP1 at 33B20 (CP157)
30	TP6 at 33B23 (CP157)
31	TP1 at 33B23 (CP157)
32	TP6 at 33C2 (CP157)
A to S+12 B to M3	
C	TP3 at 29C14 (CP254)

3 Connect INPUTS 1-24 to switch unit test socket at 29B17.

4 Connect ground to TP2 at 33B5 (CP181).

STEP	ACTION	VERIFICATION
5	Operate DIAL A keys 1 through 23 to green, 24 to red, and DIAL B keys 25 through 32 to red.	
6	Operate K1 to COMPARATOR.	
7	Operate K2 to COMB.	
8	Operate SYNC DELAY to 8K.	
9	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted. *Note:* On verification, proceed to Step 11. On failure to verify, proceed with Step 10a.
10a	If Step 9 failed to verify — Operate DIAL A or B keys to amber two at a time starting with keys 1 and 2 according to the sequence given in Table A. After each operation — Operate RST3 key momentarily. Check for verification, then restore the two keys to their original positions before proceeding to the next two keys.	If the shift register stages associated with two particular DIAL A or B keys are in trouble — The OK lamp will light when the two keys are put in an amber (don't care) position. *Note:* The second column of Table A lists the circuit packs associated with the corresponding DIAL A and B keys. When an OK indication occurs as a result of setting the keys to amber, the trouble has been localized to the associated circuit pack.

TABLE A

DIAL A OR B KEYS TO AMBER	LOCATION OF CP157 UNDER TEST
1, 2	33B14
3, 4	33B17
5, 6	33B20
7, 8	33B23
9, 10	33C2
11, 12	33C8
13, 14	33C11
15, 16	33C17
17, 18	33C20
19, 20	33C23
21, 22	33D5
23, 24	33D8
25, 26	33D11
27, 28	33D17
29, 30	33D20
31, 32	33D23

11	Remove ground from TP2 at 33B5 (CP181).	
12	Connect TP5 at 29D8 (CP307) to ground.	
13	Connect TP4 at 33B2 (CP177) to ground.	

STEP	ACTION	VERIFICATION
14	Operate DIAL A keys 1 through 23 to red, 24 to green, and DIAL B keys 25 through 32 to green.	
15	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted. *Note:* On verification, proceed to Step 17, then Test G. On failure to verify, proceed to Step 16b.
16b	If Step 15 failed verification — Repeat Step 10a using the test conditions as set up in Steps 11 through 14.	
17	Remove ground from TP5 at 29D8 (CP307).	
18	Remove ground from TP4 at 33B2 (CP177).	
19	Remove test connector at 29B17.	
20	Remove connections made in Step 2.	
21c	If no further tests are to be made at this time — Remove test set power connections to switch unit.	

G. Set Function Test for Shift Register Stages 16 and 17

2	On test set — Operate K1 to COMPARATOR.	
3	Operate K2 to SEP.	
4	Operate SYNC DELAY to 4K.	
5	Operate DIAL B keys 25 and 26 to green, all others to amber.	
6	Make the following connections between test set and switch unit and between jacks on test set.	
7	Connect TP3 at 33B2 (CP177) to ground.	
8	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted. *Note:* No verification indicates a faulty CP85 at 33A14 or CP181 at 33B5.
9	Move INPUT B to TP4 at 33B2 (CP177).	

TEST SET INPUT	SWITCH UNIT TEST POINT
25	TP6 at 33B14 (CP157)
26	TP1 at 33B14 (CP157)
A	TP1 at 33B5 (CP181)
B to M2	
C	TP3 at 29C14 (CP254)

STEP	ACTION	VERIFICATION
10	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted.
11	Move INPUT B to TP3 at 33B11 (CP75).	
12	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted. ***Note:*** No verification indicates a faulty CP85 at 33A14.
13	Remove INPUT B from TP4 at 33B2 (CP177).	
14	Remove ground from TP3 at 33B2 (CP177).	
15	Remove connections made in Step 6.	
16a	If no further tests are to be made at this time — Remove test set power connection to switch unit.	

H. Not Time Slot 0 Test

2	On test set — Operate K1 to COMPARATOR.	
3	Operate K2 to SEP.	
4	Operate SYNC DELAY to 80K.	
5	Operate DIAL B keys 25 through 29 to green, all others to amber.	
6	Make the following connections between test set and switch unit and between jacks on test set.	

TEST SET INPUT	SWITCH UNIT TEST POINT
25	TP1 at 33B17 (CP157)
26	TP6 at 33B20 (CP157)
27	TP1 at 33B20 (CP157)
28	TP6 at 33B23 (CP157)
29	TP1 at 33B23 (CP157)
A	TP4 at 33A17 (CP90)
B to M2	
C	TP3 at 29C14 (CP254)

7	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted. ***Note:*** No verification indicates a faulty CP90 at 33A17 or CP161 at 33B8.
8	Remove connections made in Step 6.	
9a	If no further tests are to be made at this time — Remove test set power connection to switch unit.	

STEP	ACTION	VERIFICATION
	I. Parity Counter Test	
2	On test set — Operate K1 to PULSE FREQ.	
3	Operate SYNC DELAY to 800.	
4	Connect INPUT C to TP4 at 33B8 (CP161).	
5	Connect TP2 at 29D8 (CP307) to ground.	On 0-8 scale — PULSE FREQ reads 6.9 to 7.7. ***Note:*** No verification indicates a faulty CP161 at 33B8.
6	Connect TP4 at 33B2 (CP177) to ground.	
7	Move INPUT C to TP1 at 33A5 (CP87).	On 0-8 scale — PULSE FREQ reads 3 to 4. ***Note:*** No verification indicates a faulty CP87 at 33A5.
8	Move INPUT C to TP2 at 33A5 (CP87).	Same as Step 7.
9	Remove INPUT C from TP2 at 33A5.	
10	Remove ground from: TP2 at 29D8 TP4 at 33B2	
11a	If no further tests are to be made at this time — Remove test set power connection to switch unit.	
	J. Comparator and End of Write Function Test	
2	On test set — Operate K1 to PULSE FREQ.	
3	Operate SYNC DELAY to 40K.	
4	Connect TP2 at 29D8 (CP307) to ground.	
5	Connect TP4 at 33B2 (CP177) to ground.	
6	Connect INPUT C to TP6 at 33A8 (CP160).	On 0-4 scale — PULSE FREQ reads 1.1 to 1.4. ***Note:*** No verification indicates a bad CP158 at 33A2 or CP160 at 33A8.
7	Move INPUT C to TP2 at 33A8 (CP160).	On 0-4 scale — PULSE FREQ reads 2.2 to 2.8. ***Note:*** No verification indicates a bad CP158 at 33A2 or CP160 at 33A8.
8	Operate SYNC DELAY to 80K.	
9	Move INPUT C to TP1 at 33A8 (CP160).	On 0-8 scale — PULSE FREQ reads 3.6 to 4.2. ***Note:*** No verification indicates a bad CP158 at 33A2 or CP160 at 33A8.

STEP	ACTION	VERIFICATION
10	Operate SYNC DELAY to 400K.	
11	Move INPUT C to TP6 at 33A11 (CP160).	On 0-4 scale — PULSE FREQ reads 0.7 to 0.9. ***Note:*** No verification indicates a bad CP158 at 33A2 or CP160 at 33A11.
12	Move INPUT C to TP2 at 33A11 (CP160).	On 0-4 scale — PULSE FREQ reads 1.4 to 1.6. ***Note:*** No verification indicates a bad CP158 at 33A2 or CP160 at 33A11.
13	Remove INPUT C from TP2 at 33A11 (CP160).	
14	Remove grounds from: TP2 at 29D8 TP4 at 33B2	
15	Connect INPUT A to MULT 1.	
16	Connect INPUT E to MULT 1.	
17	Connect MULT 1 to GRD.	
18	Connect INPUT B to TP3 at 33A5 (CP87).	
19	Operate RST3 key momentarily.	On release of RST3 — ERROR lamp lighted. ***Note:*** No verification indicates one of the following defective: CP158 at 33A2 CP85 at 33A14 CP90 at 33A20 CP90 at 33A17 CP87 at 33A5
20	Move INPUT B to TP4 at 33A5 (CP87).	
21	Repeat Step 19.	Same as Step 19.
22	Move INPUT A from MULT 1 to S+12.	
23	Repeat Step 19.	Same as Step 19.
24	Move INPUT B to TP3 at 33A5 (CP87).	
25	Repeat Step 19.	Same as Step 19.
26	Move INPUT B to TP2 at 33A23 (CP159).	
27	Disconnect (but do not remove) CP157 at 33C2.	
28	Operate RST3 key momentarily.	On release of RST3 — ERROR lamp lighted. ***Note:*** No verification indicates a bad CP75 at 33B11 or CP159 at 33A23.

STEP	ACTION	VERIFICATION
29	Move INPUT A from S+12 to MULT 1.	
30	Repeat Step 28.	Same as Step 28.
31	Replace CP157 at 33C2.	
32	Remove INPUT B from TP2 at 33A23.	
33a	If no further tests are to be made at this time — Remove test set power connection to switch unit.	

K. Switch Store Transfer Gates Test

2	On test set — Connect INPUTS 1-24 to switch unit test position at 29B20.	
3	Operate K1 to COMPARATOR.	
4	Operate K2 to SEP.	
5	Operate K3 to DTR2.	
6	Operate SYNC DELAY to 8K.	
7	Make the following connections between test set and switch unit and between jacks on test set.	

TEST SET INPUT	SWITCH UNIT TEST POINT
22	TP3 at 29C11 (CP75)
23	TP1 at 29C11 (CP75)
24	TP2 at 29C11 (CP75)
A to S+12	
B to M3	
C	TP3 at 29C14(CP254)

8	Connect ground to: TP1 at 42A10 (CP159) TP2 at 42A10 (CP159) TP4 at 42A10 (CP159) TP2 at 33B5 (CP181)	
9	Operate DIAL A keys 1 through 23 to green and 24 to red.	
10	Operate RST3 key momentarily.	After release of RST3 — OK lamp remains lighted. *Note:* On verification, proceed to Step 12. On no verification, proceed to Step 11a.

STEP	ACTION	VERIFICATION
11a	If Step 10 failed to verify — Operate DIAL A keys to amber a group at a time starting with keys 1 through 6 according to the sequence given in Table B. After each operation — Operate RST3 key momentarily. Check for verification, then restore the keys to their original positions before proceeding to the next group of keys.	If the gates associated with the particular DIAL A keys are in trouble — The OK lamp will light when the group of keys are put in an amber (don't care) position. ***Note:*** The second column of Table B lists the circuit packs associated with the corresponding DIAL A keys. When an OK indication occurs as a result of setting the keys to amber, the trouble has been localized to the associated circuit pack.

TABLE B

DIAL A KEYS TO AMBER	LOCATION OF CP UNDER TEST
1,2,3,4,5,6	33C5 (CP161)
7,8,9,10,11	33C14 (CP161)
12,13,14,15,16,17	33D2 (CP161)
18,19,20,21	33D14 (CP161) and 29C11 (CP75)

12	Remove ground from TP2 at 33B5 (CP181).	
13	Connect TP2 at 29D8 (CP307) to ground.	
14	Connect TP4 at 33B2 (CP177) to ground.	
15	Operate DIAL A keys 1 through 23 to red and 24 to green.	
16	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted. ***Note:*** On verification, proceed to Step 18. On no verification, proceed to Step 17b.
17b	If Step 16 failed to verify — Repeat Step 11a for test conditions as set up in Steps 12 through 15.	
18	On test set — Move INPUTS 1-24 to switch unit test socket at 29B23.	
19	Operate DIAL A keys 1 through 21 to green, 22 and 23 to red, and 24 to green.	
20	Operate RST3 key momentarily.	After release of RST3 key — OK lamp remains lighted. ***Note:*** On verification, proceed to Step 22. On no verification, proceed to Step 21c.
21c	If Step 20 failed to verify — Repeat Step 11a making reference to the key operations listed in Table C.	See verification and note for Step 11a, making reference to Table C.

STEP	ACTION	VERIFICATION

TABLE C

DIAL A KEYS TO AMBER	LOCATION OF CP UNDER TEST
1,2,3,4,5	33C5 (CP161)
6,7,8,9,10,11	33C14 (CP161)
12,13,14,15,16	33D2 (CP161)
17,18,19,20,21	33D14 (CP161) and 29C11 (CP75)

22 Remove ground from:

TP2 at 29D8 (CP307)
TP4 at 33B2 (CP177)

23 Connect TP2 at 33B5 (CP181) to ground.

24 Operate DIAL A keys 1 through 21 to red, 22 and 23 to green, and 24 to red.

25 Operate RST3 key momentarily.

After release of RST3 key —
OK lamp remains lighted.

Note: On verification, Test K is completed. Proceed to Step 27. On no verification, proceed to Step 26d.

26d If Step 25 failed to verify —
Repeat Step 11a using the test conditions as set up in Steps 22, 23, and 24 and making reference to the key operations listed in Table C.

27 Remove ground from:

TP1 at 42A10
TP2 at 42A10
TP4 at 42A10
TP2 at 33B5

28 Remove test connector at 29B23.

29 Remove test set power connection to switch unit.

Caution: Before attempting to place this data distributor back into service, remove all inhibiting grounds.