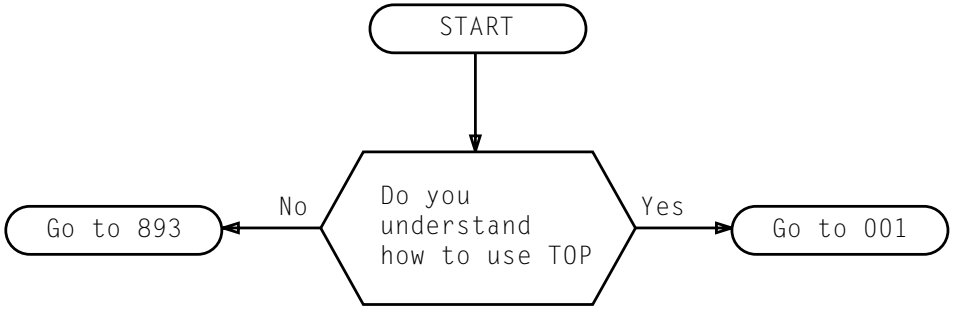
Lucent Technologies
Bell Labs Innovations

Task Oriented Practice (TOP)

4ESS™ Switch With 1B Processor Peripheral Unit Bus System Trouble Clearing



TOP Comments Hot Line:

Monday through Friday
8:00 a.m. - 4:00 p.m. (Eastern)
Call: 1-888-LTINFO6
Or FAX to: 1-336-727-3043

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Notice

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Developed by:

Lucent Technologies Systems for Customer Training and Information Products (CTIP)
Lucent Technologies is the successor to the business and assets of AT&T Network Systems business unit.

FIND YOUR JOB IN THE LIST BELOW	THEN GO TO
Acceptance	NTP-002
Blown Fuse Trouble — DC-to-DC Converter (J87407A) — Clear	TAP-112
Blown Fuse Trouble — PUBB and Loop-Around Unit (J4A005AA-1) — Clear	TAP-111
Buses; Peripheral Unit — Scope	NTP-003
Bus; PU — Equipment Trouble — Clear	TAD-110
Circuit Pack — PUBB Frame — Replace	DLP-527
Converter (J87407A); DC-to-DC — Blown Fuse Trouble — Clear	TAP-112
Converter (J87407A); DC-to-DC — LED Lighted Trouble — Clear	TAP-113
Converter (J87407A); DC-to-DC — PUBB Frame — Replace	NTP-004
DC-to-DC Converter (J87407A) Blown Fuse Trouble — Clear	TAP-112
DC-to-DC Converter (J87407A) LED Lighted Trouble — Clear	TAP-113
DC-to-DC Converter (J87407A) — PUBB Frame — Replace	NTP-004
Diagnostic Failure — Analyzing Raw Data — Clear	TAP-103
Diagnostic Failure — Looping Over First Failing Test and Signal Tracing — Clear	TAP-104
Diagnostic Failure — TLP Suspect Equipment List Generated — Clear	TAP-102
Diagnostic Failure — TLP Inhibit — Clear	TAP-106
Diagnostic Failure — TLP Abort — Clear	TAP-108
Diagnostic Failure — TLP Disk Queue Full — Clear	TAP-107
Diagnostic Failure — TLPQUEUE Blockage — Clear	TAP-105
Diagnostic Failure — TLP Tape Not Mounted — Clear	TAP-109

FIND YOUR JOB IN THE LIST BELOW . . . . . THEN GO TO

FIND YOUR JOB IN THE LIST BELOW . . . . . THEN GO TO

No acceptance test procedures are required for this frame. Readiness of the frame to become part of the working system was established by the successful completion of Installation Handbook test procedures.

DO THE ITEMS BELOW IN THE ORDER LISTED . . . . . FOR DETAILS, GO TO		
	NOTES: 1. Appropriate Input/Output manuals must be used if clarification of input message or output message is necessary 2. Use SREC or Beltline terminal with form enter capability to expedite procedure 3. This procedure must be performed during light traffic periods 4. ***4ESS*** ™ switch operation must be closely monitored while performing this procedure 5. Corrective action must be taken immediately on any activity that may cause any unit to go out of service (OOS) 6. Stability of office must be maintained throughout this procedure	
1	At 1B Processor MTC Terminal, Enter Message **INH:MACLI,CLASS MTCE;REX!** To Inhibit REX	—
2	Enter Message **STOP:TEST;PUSYS!** To Stop Peripheral System Tests	—
	PUB 0 SCOPING	
3	Locate Bus Branch Terminating Resistors at PUBB Frame, or Determine Location of Last Frame on Bus Branch To Be Scoped per Office Record T-nnnn-Hn-3840	—
4	If VIF Frame Was Determined in Item 3, Determine From Office Record T-nnnn-Hn-3840 Frame Where PU Write and Enable Buses Are Terminated	—
5	Store Input Messages on 1B Terminal for PUB 0 Looping Test	DLP-502
6	Remove PUB 0 From Service (**RMV:PUB 0!**)	DLP-522
7	Set Up Storage Oscilloscope	DLP-524
8	Advance Program to Bus Branch To Be Scoped and Set Up Loop To Observe Bit 0 on PU Write and Reply Bus	DLP-505
9	If Last Frame Determined in Item 3 Is Not VIF Frame, Scope Bit 0 on PU Write Bus at BTRs in Last Frame Determined in Item 3	DLP-507
10	If Last Frame Determined in Item 3 Is VIF Frame, Scope Bit 0 on PU Write Bus at BTRs in Last Frame Determined in Item 3	DLP-507
11	Scope Bit 0 on PU Reply Bus at BTRs in Last Frame Determined in Item 3	DLP-508
12	Enter Stop Looping Message (**EX:PUB 0!**)	—
13	Advance Program and Set Up Loop To Observe Bits 1 to 35 on PU Write Bus; Bits 0 to 11 on PU Enable Address Bus; and Bits 1 to 23 on PU Reply Bus	DLP-505

DO THE ITEMS BELOW IN THE ORDER LISTED . . . . . FOR DETAILS, GO TO		
14	If Last Frame Determined in Item 3 Is Not VIF Frame, Scope Bits 1 to 35 on PU Write Bus at BTRs in Last Frame Determined in Item 3	DLP-509
15	If Last Frame Determined in Item 3 is VIF Frame, Scope Bits 1 to 35 on PU Write Bus at BTRs in Last Frame Determined in Item 3	DLP-509
16	If Last Frame Determined in Item 3 Is Not VIF Frame, Scope Bits 0 to 11 on PU Enable Address Bus at BTRs in Last Frame Determined in Item 3	DLP-510
17	If Last Frame Determined in Item 3 Is VIF Frame, Scope Bits 0 to 11 on PU Enable Address Bus at BTRs in Last Frame Determined in Item 3	DLP-510
18	Scope Bits 1 to 23 on PU Reply Bus at BTRs in Last Frame Determined in Item 3	DLP-511
19	Enter Stop Looping Message (**EX:PUB 0!**)	—
20	Set Up Loop To Observe PU Control Bus and Miscellaneous Bus Bits	DLP-512
21	Scope PU Control Bus and Miscellaneous Bus Bits at BTRs in Last Frame Determined in Item 3	DLP-513
22	If Last Frame Determined in Item 3 is VIF Frame, Scope Remaining PU Miscellaneous Bus Bits at BTRs in Last Frame Determined in Item 3	DLP-513
23	Enter Stop Looping Message (**EX:PUB 0!**)	—
24	Stop Maintenance Control Program Client	DLP-506
25	Determine if Last Frame in Item 1.2 Is an SCS or DIFE (Member Numbers 24-31) Frame, or XTSI on Expanded Pollable Bus. If SCS or DIFE (Member Numbers 24-31), or XTSI on Expanded Pollable Bus, Set Up Loop To Observe and Scope Expanded Pollable Bits	
	A. If Last Frame in Step 3 is an SCS Cabinet, DIFE (Member Numbers 24 through 31) Frame, or XTSI on Expanded Pollable Bus, Set up Loop and Scope Expanded Pollable Bits	DLP-525
	B. If XTSI is Being Grown on New Bus Branch With Expanded Pollable Bits, Set Up Loop and Scope Expanded Pollable Bits	DLP-526
26	Restore PUB 0 to Service (**RST:PUB 0!**)	DLP-521
27	Ensure Storage Oscilloscope Is Disconnected From Scoped Frame	—

DO THE ITEMS BELOW IN THE ORDER LISTED . . . . . FOR DETAILS, GO TO

	PUB 1 SCOPING	
28	Locate Bus Branch Terminating Resistors at PUBB Frame, or Determine Location of Last Frame on Bus Branch To Be Scoped per Office Record T-nnnn-Hn-3840	—
29	If VIF Frame Was Determined in Item 27, Determine From Office Record T-nnnn-Hn-3840 Frame Where PU Write and Enable Buses Are Terminated	—
30	Store Input Message on 1B Processor Terminal for PUB 1 Looping Test	DLP-502
31	Remove PUB 1 From Service (**RMV:PUB 1!**)	DLP-522
32	Set Up Storage Oscilloscope	DLP-524
33	Advance Program to Bus Branch To Be Scoped and Set Up Loop To Observe Bit 0 on PU Write and Reply Bus	DLP-505
34	If Last Frame Determined in Item 27 Is Not VIF Frame, Scope Bit 0 on PU Write Bus at BTRs in Last Frame Determined in Item 27	DLP-507
35	If Last Frame Determined in Item 27 Is VIF Frame, Scope Bit 0 on PU Write Bus at BTRs in Last Frame Determined in Item 27	DLP-507
36	Scope Bit 0 on PU Reply Bus at BTRs in Last Frame Determined in Item 27	DLP-508
37	Enter Stop Looping Message (**EX:PUB 1!**)	—
38	Advance Program and Set Up Loop To Observe Bits 1 to 35 on PU Write Bus; Bits 0 to 11 on PU Enable Address Bus; and Bits 1 to 23 on PU Reply Bus	DLP-505
39	If Last Frame Determined in Item 27 Is Not VIF Frame, Scope Bits 1 to 35 on PU Write Bus at BTRs in Last Frame Determined in Item 27	DLP-509
40	If Last Frame Determined in Item 27 Is VIF Frame, Scope Bits 1 to 35 on PU Write Bus at BTRs in Last Frame Determined in Item 27	DLP-509
41	If Last Frame Determined in Item 27 Is Not VIF Frame, Scope Bits 0 to 11 on PU Enable Address Bus at BTRs in Last Frame Determined in Item 27	DLP-510
42	If Last Frame Determined in Item 27 Is VIF Frame, Scope Bits 0 to 11 on PU Enable Address Bus at BTRs in Last Frame Determined in Item 27	DLP-510
43	Scope Bits 1 to 23 on PU Reply Bus at BTRs in Last Frame Determined in Item 27	DLP-511
44	Enter Stop Looping Message (**EX:PUB 1!**)	—

SCOPE PERIPHERAL UNIT BUSES (PUBs) 0 AND 1

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
45	Set Up Loop To Observe PU Control Bus and Miscellaneous Bus Bits	DLP-512
46	Scope PU Control Bus and Miscellaneous Bus Bits at BTRs in Last Frame Determined in Item 27	DLP-513
47	If Last Frame Determined in Item 27 Is VIF Frame, Scope Remaining PU Miscellaneous Bus Bits at BTRs in Last Frame Determined in Item 27	DLP-513
48	Enter Stop Looping Message (**EX:PUB 1!**)	—
49	Stop Maintenance Control Program Client	DLP-506
50	Determine if Last Frame in Item 2.2 Is an SCS or DIFE (Member Numbers 24-31) Frame, or XTSI on Expanded Pollable Bus. If SCS or DIFE (Member Numbers 24-31), or XTSI on Expanded Pollable Bus, Set Up Loop To Observe and Scope Expanded Pollable Bits	
	A. If Last Frame in Step 3 Is an SCS Cabinet, DIFE (Member Numbers 24 through 31) Frame, or XTSI on Expanded Pollable Bus, Set up Loop and Scope Expanded Pollable Bits	DLP-525
	B. If XTSI is Being Grown on New Bus Branch With Expanded Pollable Bits, Set Up Loop and Scope Expanded Pollable Bits	DLP-526
51	Restore PUB 1 to Service (**RST:PUB 1!**)	DLP-521
52	Ensure Storage Oscilloscope Is Disconnected From Scoped Frame	—
53	At 1B MTC Terminal, Enter Message **ALW:MACLI,CLASS MTCE;REX!** To Allow REX	—

DO THE ITEMS BELOW IN THE ORDER LISTED		FOR DETAILS, GO TO
1	At 1B Processor MTC Terminal, Enter Message **RMV:PUB** a! (a = Bus To Be Removed [0 or 1])	—
2	At PUBB Frame Power Switch, Rotate **ROS/OFF** Switch Clockwise to **ROS** (**OFF NORM** and **OS** Lamps Light)	—
3	At PUBB Frame Power Switch, Depress **ROS/OFF** Switch (**PWR OFF** Lamp Lights)	—
4	Replace DC-to-DC Converter (J87407A)	DLP-523
5	At PUBB Frame Power Switch, Rotate **ROS/OFF** Switch Counterclockwise to Normal Position (**OFF NORM** and **OS** Lamps Go Off)	—
6	At 1B Processor MTC Terminal, Enter Message **RST:PUB** a! (a = Bus To Be Removed [0 or 1])	—

GENERAL

The maintenance philosophy contained in this volume is based upon the design of equipment (hardware), diagnostic software, and test equipment employed. Procedures are intended to aid personnel in performing trouble-clearing tasks. The degree to which these procedures accomplish this depends upon input and feedback from the user. Additions, corrections, and improvements to the data are encouraged. Manufacturer, engineering, and software documentation such as input/output (I/O) manuals, SDs, PKs, PRs, etc., are referred to where applicable rather than duplicating that information here. Some portions of those documents may be used utilized in procedures but only as examples for the purpose of explanation. Test equipment (oscilloscopes, voltmeters, etc.) and the parameters involved in the circuits being tested, adjusted, or checked are usually prescribed. However, setup and method of operation are not described unless they are unusual or unique in some manner.

IXL PHILOSOPHY [IXL-001]

The IXL is an alphabetized, permuted index structured to provide fast access to trouble analysis procedures (TAPs), non-trouble procedures (NTPs), and detailed level procedures (DLPs) pertinent to identified symptoms. Procedures unique to a particular modification of a frame are identified by that frame's SD number. If not so identified, the procedure will apply to all modifications.

Power problems are sensed by scan points which generate an alarm. It is assumed that the user following the aisle pilot lights can locate the frame with the power fault which is automatically powered down (**PWR OFF** lamp lighted and **OFF NORM** lamp off), or by reading **REPT:PA** printout which would identify the frame with power fault. The precise structure of the message is given in input/output (I/O) message manuals. Symptoms described in the IXL reflect the previous assumptions listed, and indicate further conditions that are observable at the frame that would enable the user to access the proper trouble-clearing procedure. These conditions are blown fuses and lighted LEDs on converters or power function circuit packs.

TAP PHILOSOPHY

When documenting a procedural approach to trouble clearing, certain assumptions are made. It is assumed that one fault is being cleared at a time. When directing the user to perform an action, it is assumed that the user performs that action correctly. Similarly, when directed to make replacements, the replacement part is always assumed to be good. Equipment used for testing both built-in and commercial hardware and software is assumed to be good. Only consistent fault signatures are covered.

Trouble-clearing TAPs provided for diagnostic failures are provided on three levels. Level one (TAP-102) is referenced when a software **TLP SUSPECTED FAULTY EQUIPMENT** list is generated. This level provides a step-by-step procedure for replacing circuit packs one at a time, and analyzing the results. It is straightforward and only requires some familiarity with the equipment (descriptive and theory practices), 1B Processor MTC terminal techniques, and diagnostic printouts.

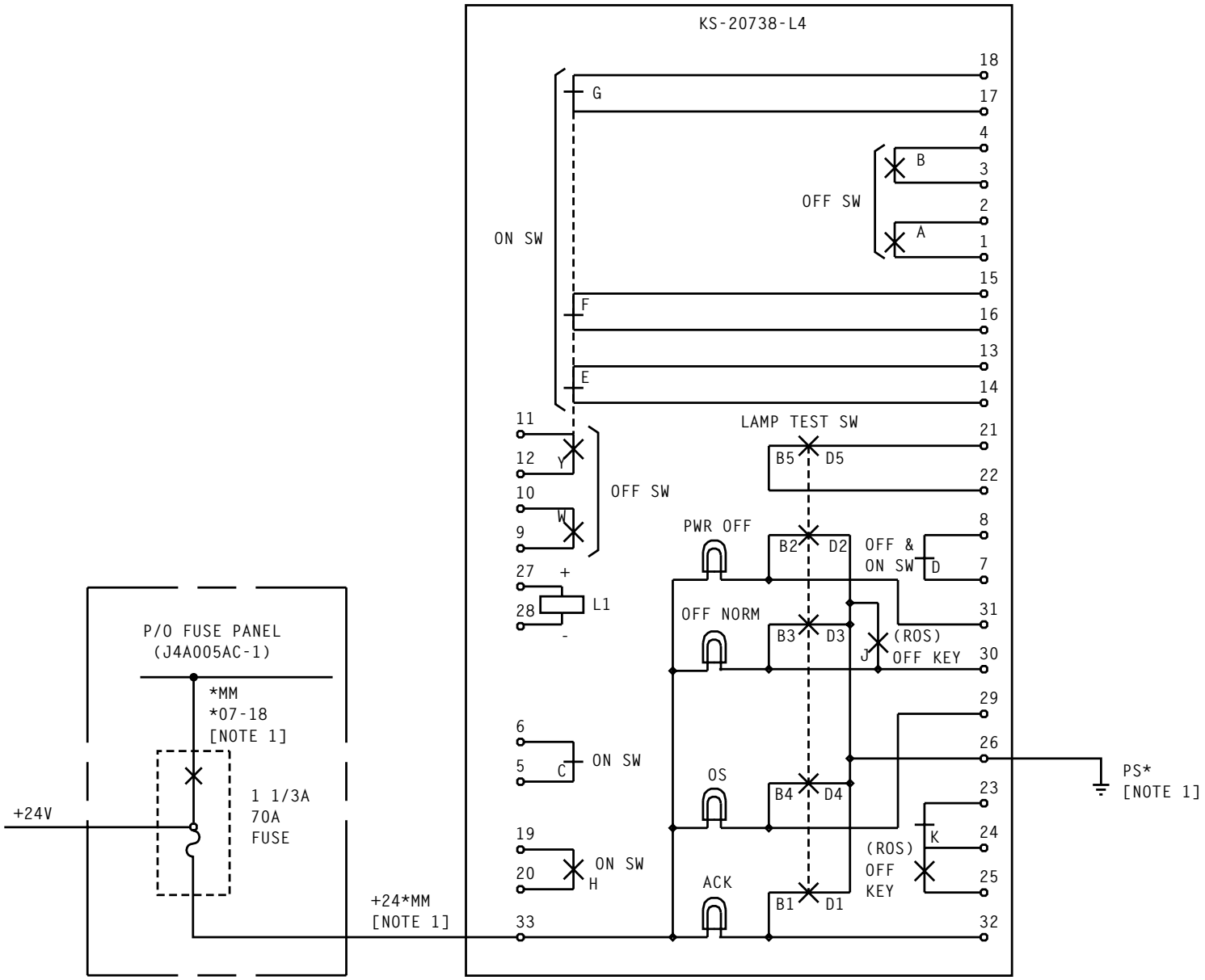
The second level of trouble clearing (TAP-103) is accessed from the first level TAP when the software generated **TLP SUSPECTED FAULTY EQUIPMENT** list has been exhausted without clearing the problem, or it can be accessed directly from the IXL. This level is known as raw data analysis and describes what to do with the summary and supplemental data printed either with or instead of the

TLP SUSPECTED FAULTY EQUIPMENT list. It is expected that this will lead to an identification of faulty circuits within the SD and possibly additional suspect circuit packs not previously identified. This level of trouble clearing is more complex and requires knowledge of the equipment, 1B Processor MTC terminal techniques, and SDs, PKs, PRs, etc.

The third level of trouble clearing is signal tracing using interactive diagnostics (TAP-104). This procedure is accessible only from the previous level (TAP-103) and uses information derived from performance of that procedure. This level of trouble clearing requires an increase in the capabilities cited in the first two levels but with additional knowledge and skill in the setup and use of test equipment (oscilloscopes, voltmeters, etc.).

ALTERNATE METHODS

The more knowledgable and experienced personnel may access TOP documents at a point in trouble clearing where analysis is completed (the faulty component determined) and only repair or replacement is required. Most DLPs are built to support TAPs and NTPs with preconditioning and system restoration steps covered in those procedures. Therefore, access to data (DLPs) on a hunt-and-find basis is a threat to equipment operation and may compound trouble-clearing problems.



NOTE 1
* = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)

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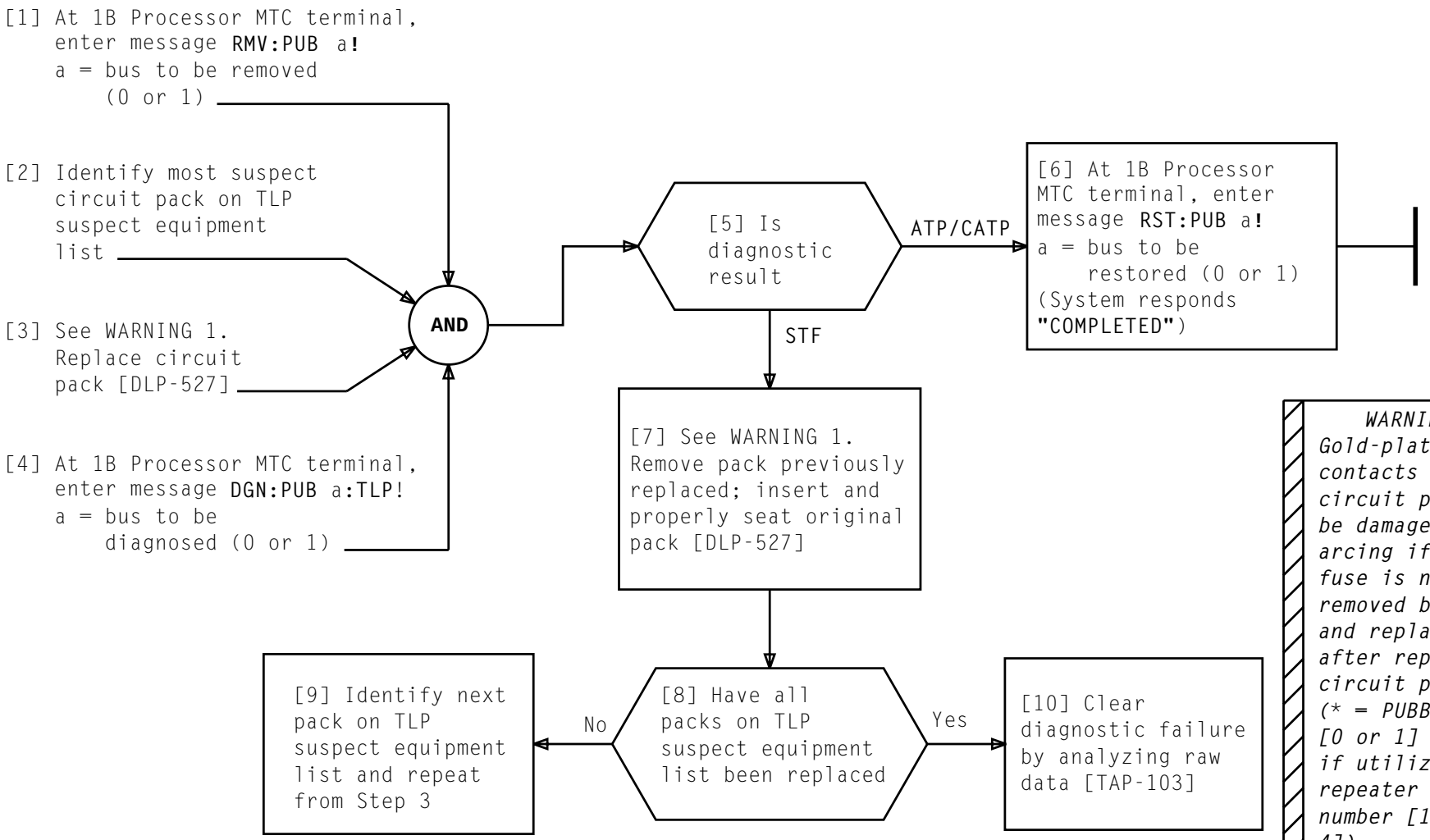
POWER SWITCH LAMP CIRCUIT

SUMMARY

At PUBB bay or repeater frame (if utilized), replace all circuit packs beginning with most suspect pack listed on TLP suspect equipment list. After each pack replacement, check diagnostic results to determine if trouble was cleared. If trouble is not cleared after replacing each pack on TLP list, clear diagnostic failure by analyzing raw data [TAP-103]

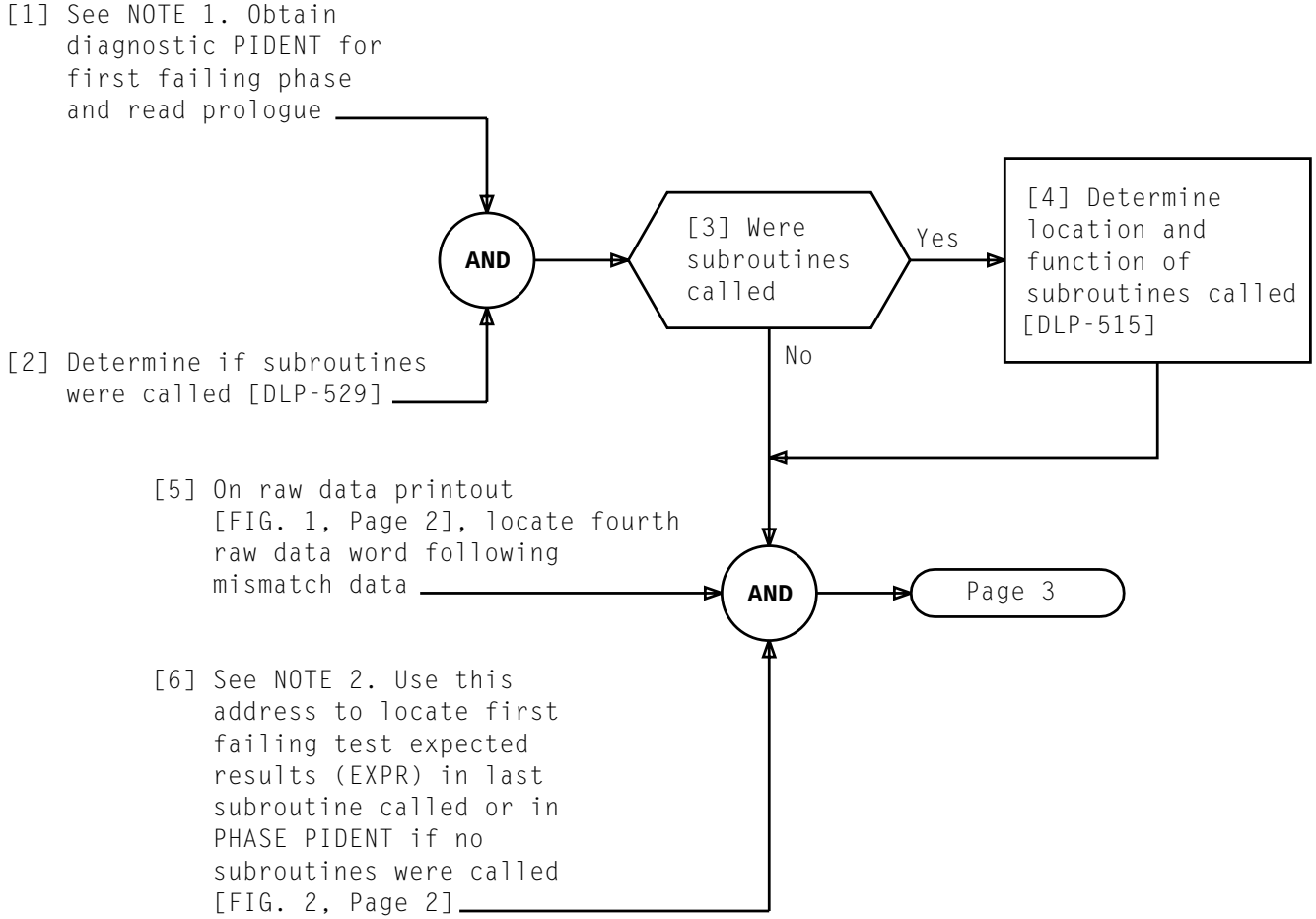


WARNING 1
Gold-plated contacts on **FB152** *circuit pack may be damaged by arcing if *ML fuse is not removed before and replaced after replacing circuit pack (* = PUBB bay [0 or 1] or if utilized, repeater frame number [1 through 4])*

CLEAR DIAGNOSTIC FAILURE, TLP SUSPECT EQUIPMENT LIST GENERATED

SUMMARY

Read first failing phase prologue. Determine if subroutines were used and identify their location and function. Locate first failing test and determine test function. Determine if doloops were used and identify their location and function. Note PK information for failing bits in first failing test. Use PK information and knowledge of first failing test function to identify and replace any suspect packs other than those previously replaced. If trouble is not cleared, clear diagnostic failure by looping over first failing test and signal tracing [TAP-104]



NOTES

1. PR number = 4A510 + phase number. PIDENT is PUDGPBxx (xx = phase number), except for six IPUB phase 99s:
   TMS – PUDGTG99 – 4A705
   TSI – PUDGTI99 – 4A706
   SCLK – PUDGSC99 – 4A697
   SP – PUDGSP99 – 4A703
   EST – PUDGEC99 – 4A692
   TGR – PUDGTA99 – 4A704
2. Phase PIDENT may consist of more than one strip with address appearing in more than one strip. Be sure address located has EXPR data for your test

CLEAR DIAGNOSTIC FAILURE BY ANALYZING RAW DATA

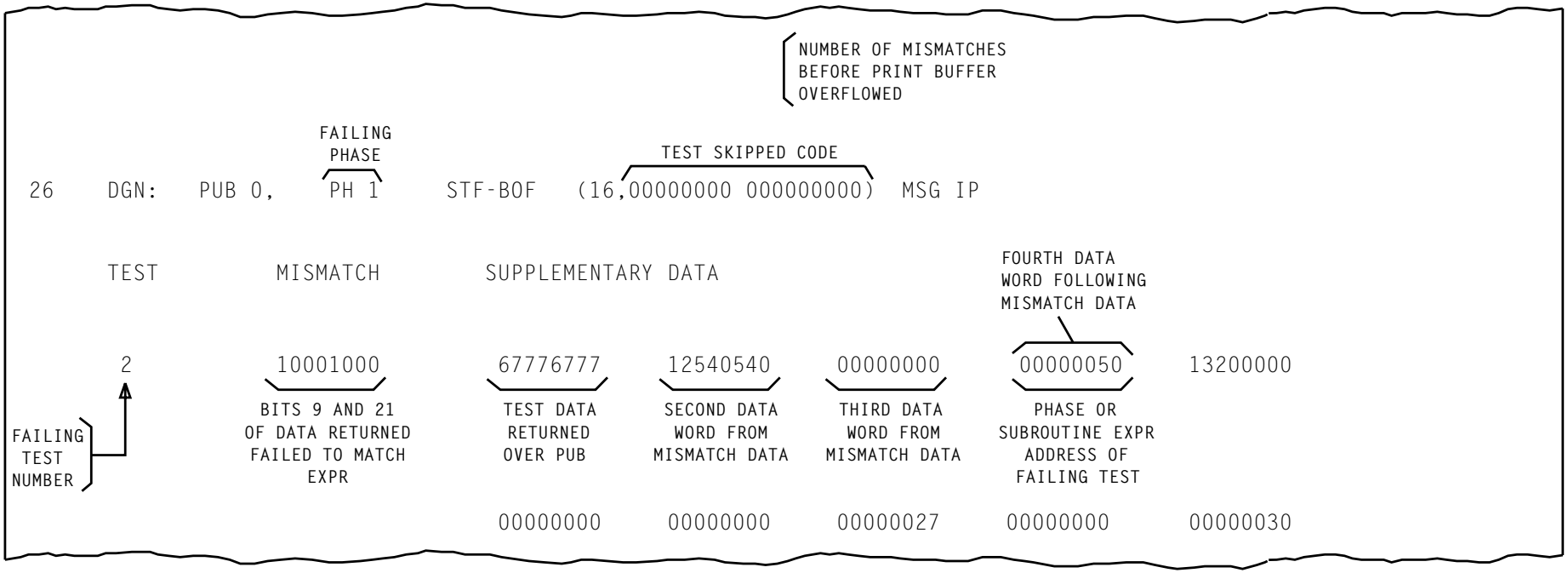


FIG. 1 – Example of PUBB Frame Raw Data Printout

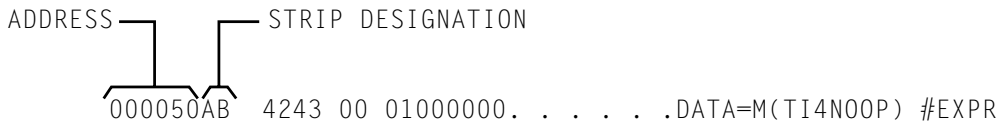
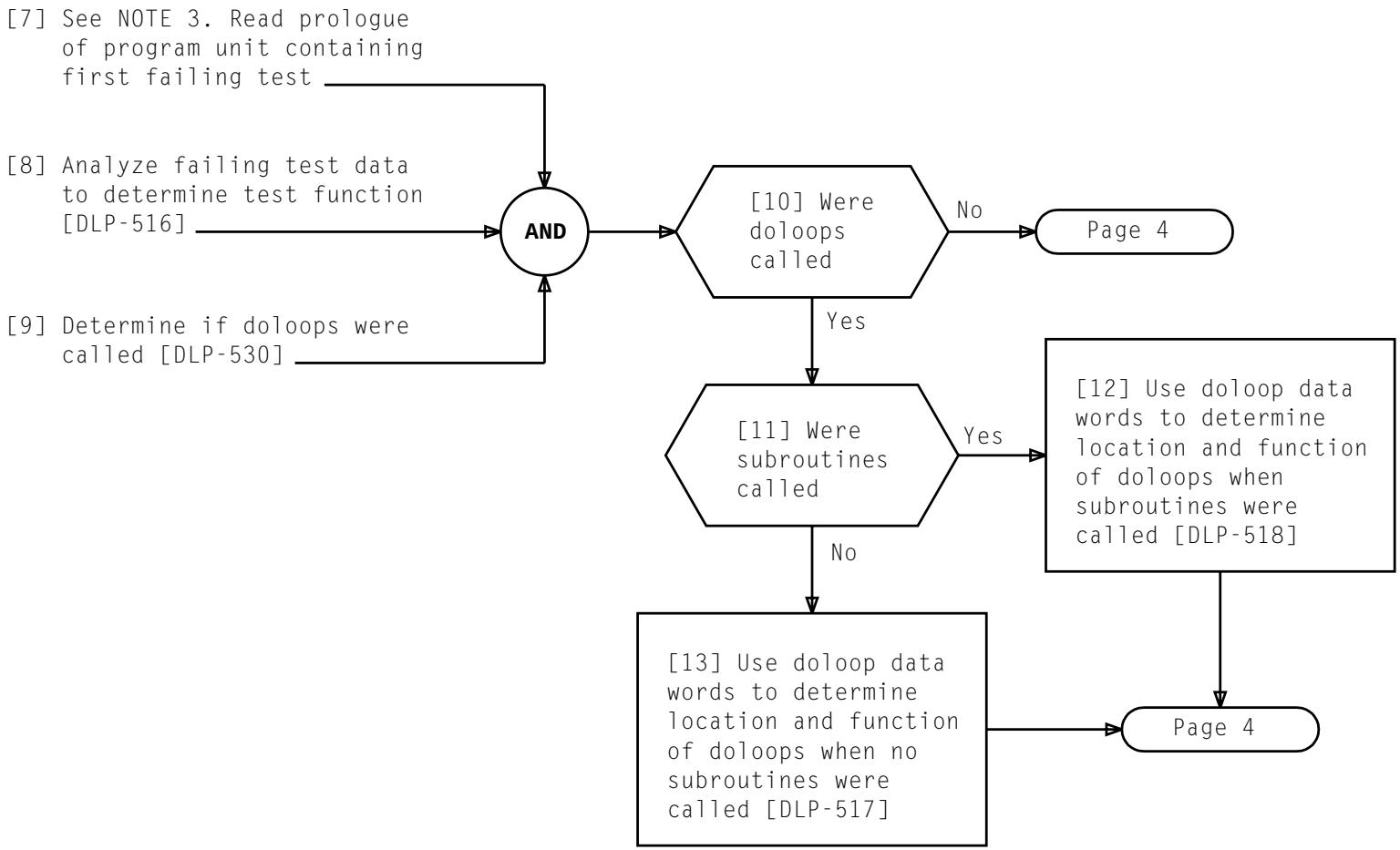
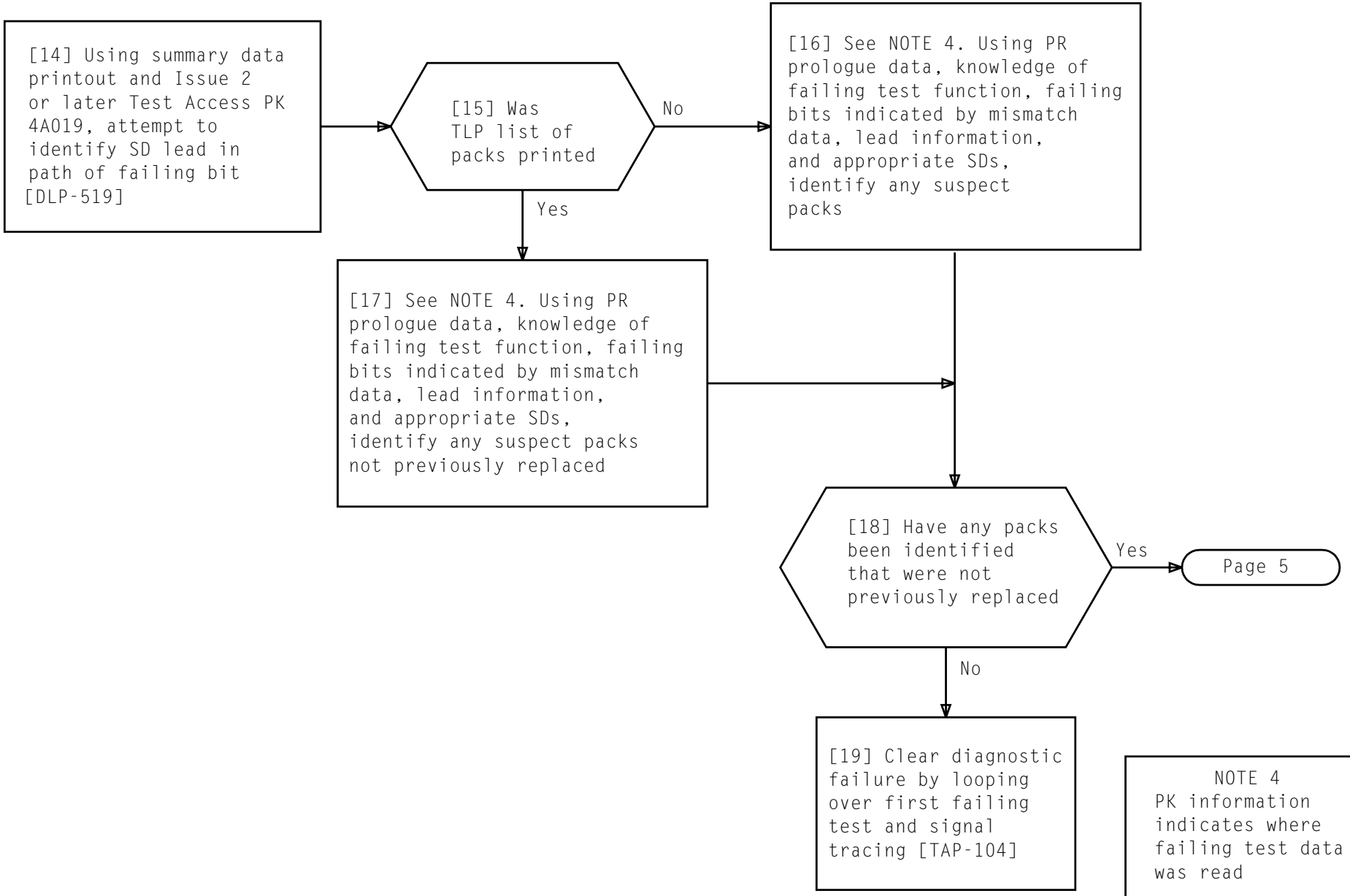


FIG. 2 – Example of EXPR Data in Listing



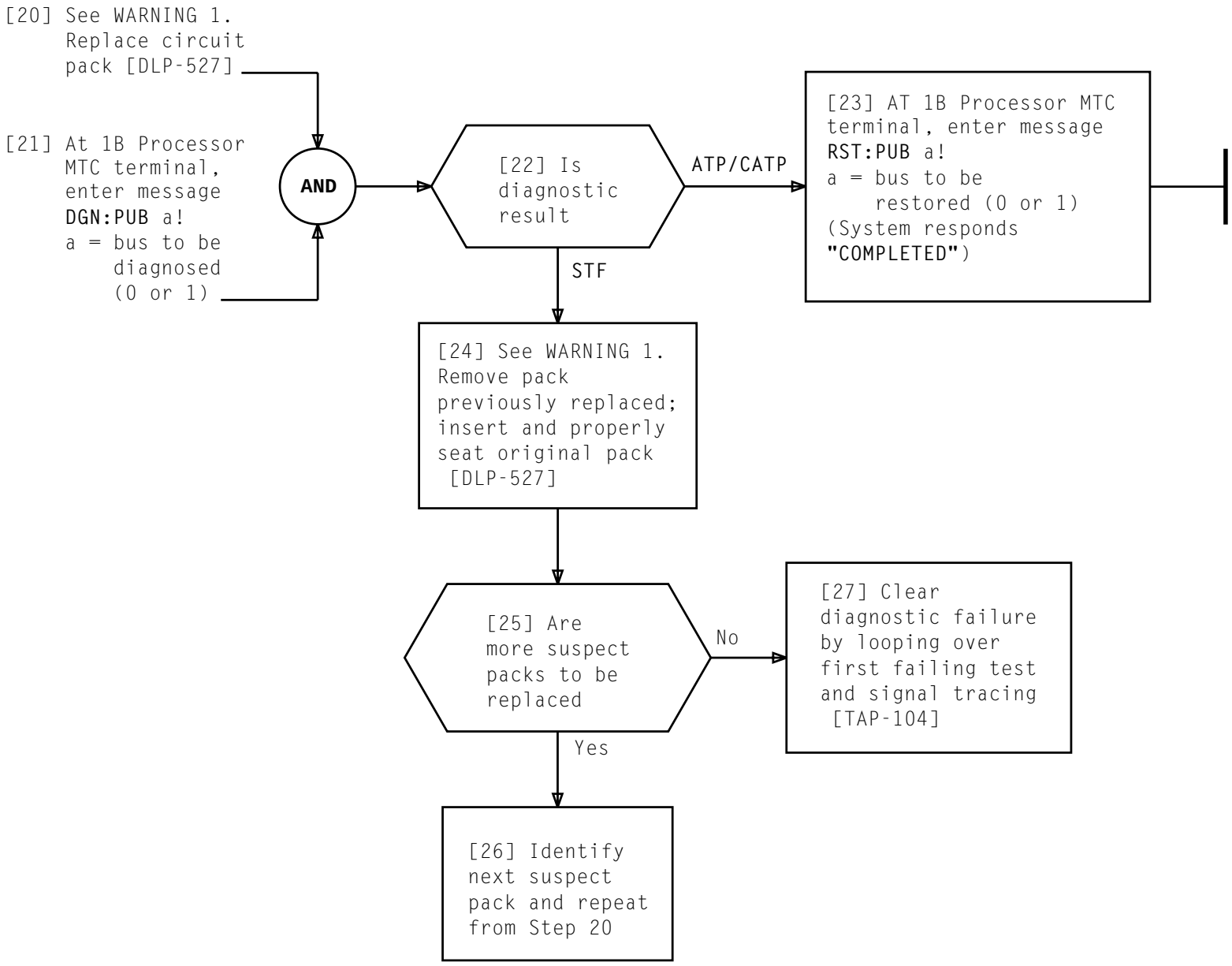
NOTE 3
Program unit name is indicated in upper left of each listing page

CLEAR DIAGNOSTIC FAILURE BY ANALYZING RAW DATA



NOTE 4
PK information indicates where failing test data was read

CLEAR DIAGNOSTIC FAILURE BY ANALYZING RAW DATA



WARNING 1

Gold-plated contacts on **FB152** *circuit pack may be damaged by arcing if *ML fuse is not removed before and replaced after replacing circuit pack (* = PUBB bay [0 or 1] or if utilized, repeater frame number [1 through 4])*

CLEAR DIAGNOSTIC FAILURE BY ANALYZING RAW DATA

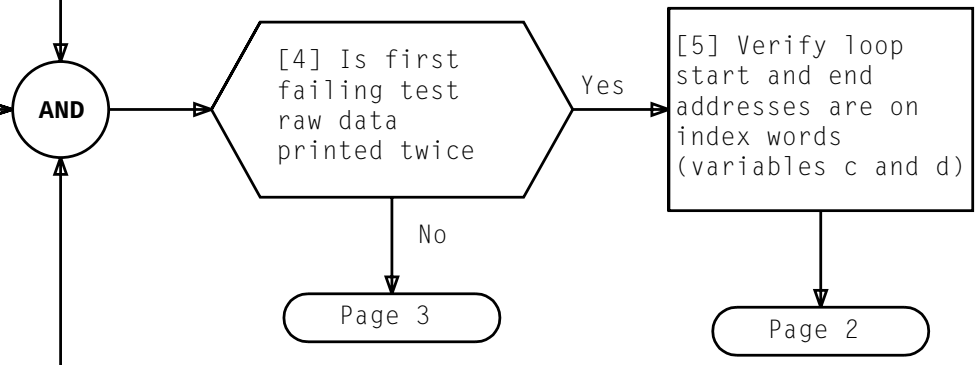
SUMMARY	
Set up loop over first failing test, requesting two diagnostic runs. Verify failing test raw data prints twice. Set up infinite loop over first failing test (**RPT 2** option deleted). Set up scope. If SYNC option is used, attach external sweep trigger to terminal *80-10-015 [NOTE 1].	Using raw data analysis information obtained, SDs/CDs, and circuit pack SDs, signal trace path of failing bits to isolate and clear fault. If F-level interrupt is associated with diagnostic failure, analyze PBFR F-level interrupt [see 234-351-003]

At 1B Processor MTC terminal:

[1] Enter message
EX:PUB a;START! (a=failing PUB [0 OR 1])
RESPONSE: SUSPENDED

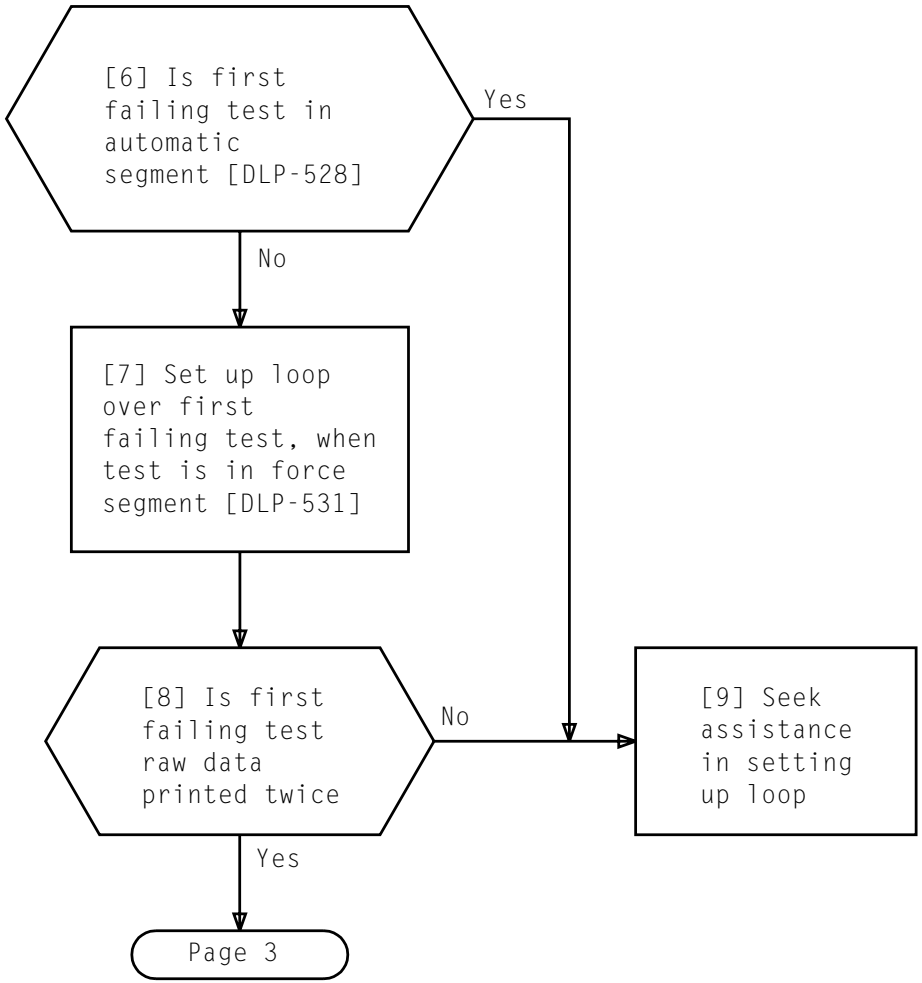
[2] Enter message
EX:PUB a:SYNC c,ENABLE e! (SYNC optional)
(a = failing PUB [0 or 1],
c = address of first failing statement index word,
e = first failing test number)
RESPONSE: SUSPENDED

[3] Enter message
EX:PUB a;RPT 2:PH b,ADR c-d!
(a = failing PUB [0 or 1],
b = first failing phrase number
c = address of first failing statement index word,
d = address of next index word following first failing test index word)
RESPONSE: (RAW DATA)



NOTE 1
* = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)

CLEAR DIAGNOSTIC FAILURE BY LOOPING OVER FIRST FAILING TEST AND SIGNAL TRACING



CLEAR DIAGNOSTIC FAILURE BY LOOPING OVER FIRST FAILING TEST AND SIGNAL TRACING

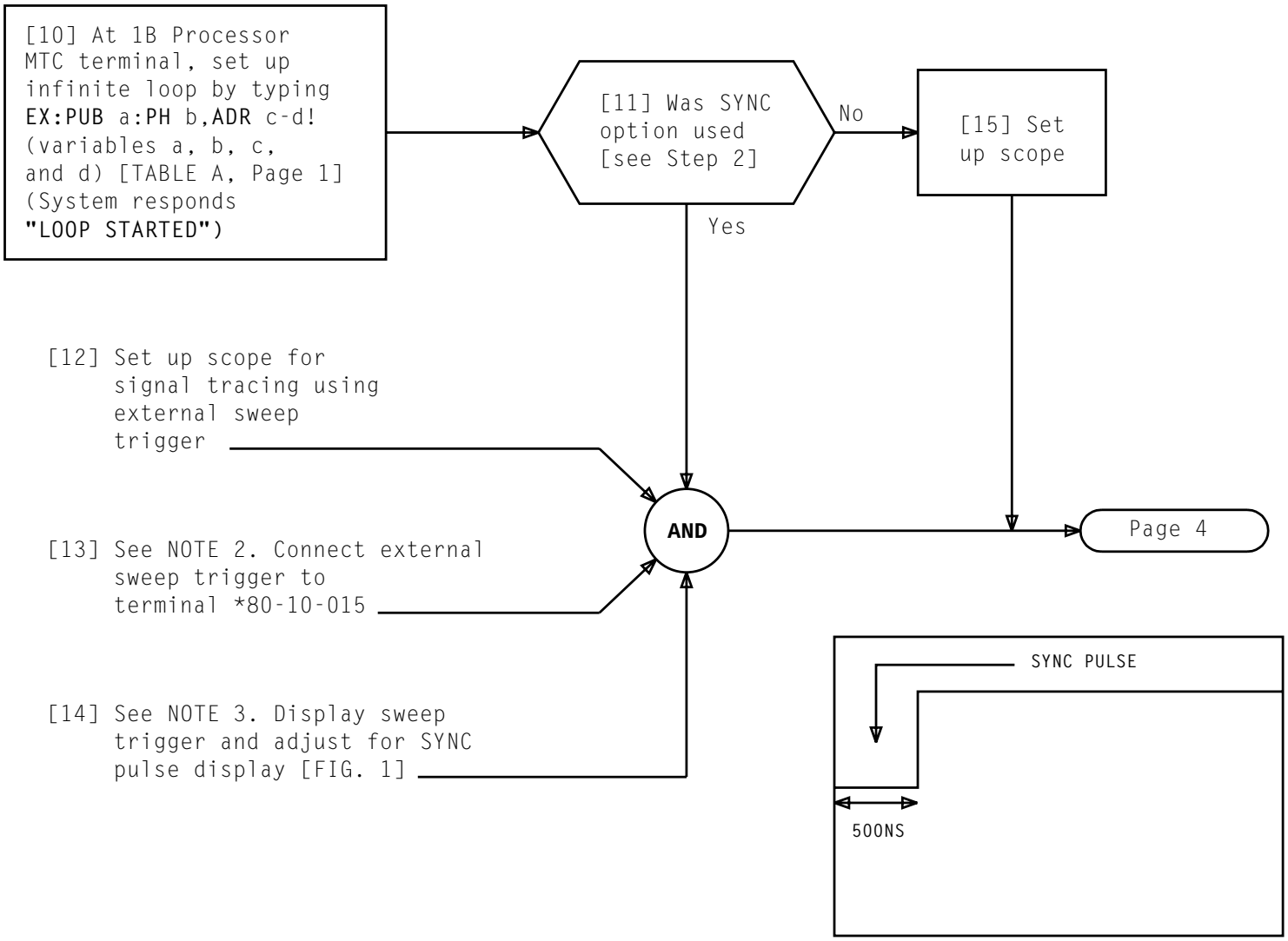
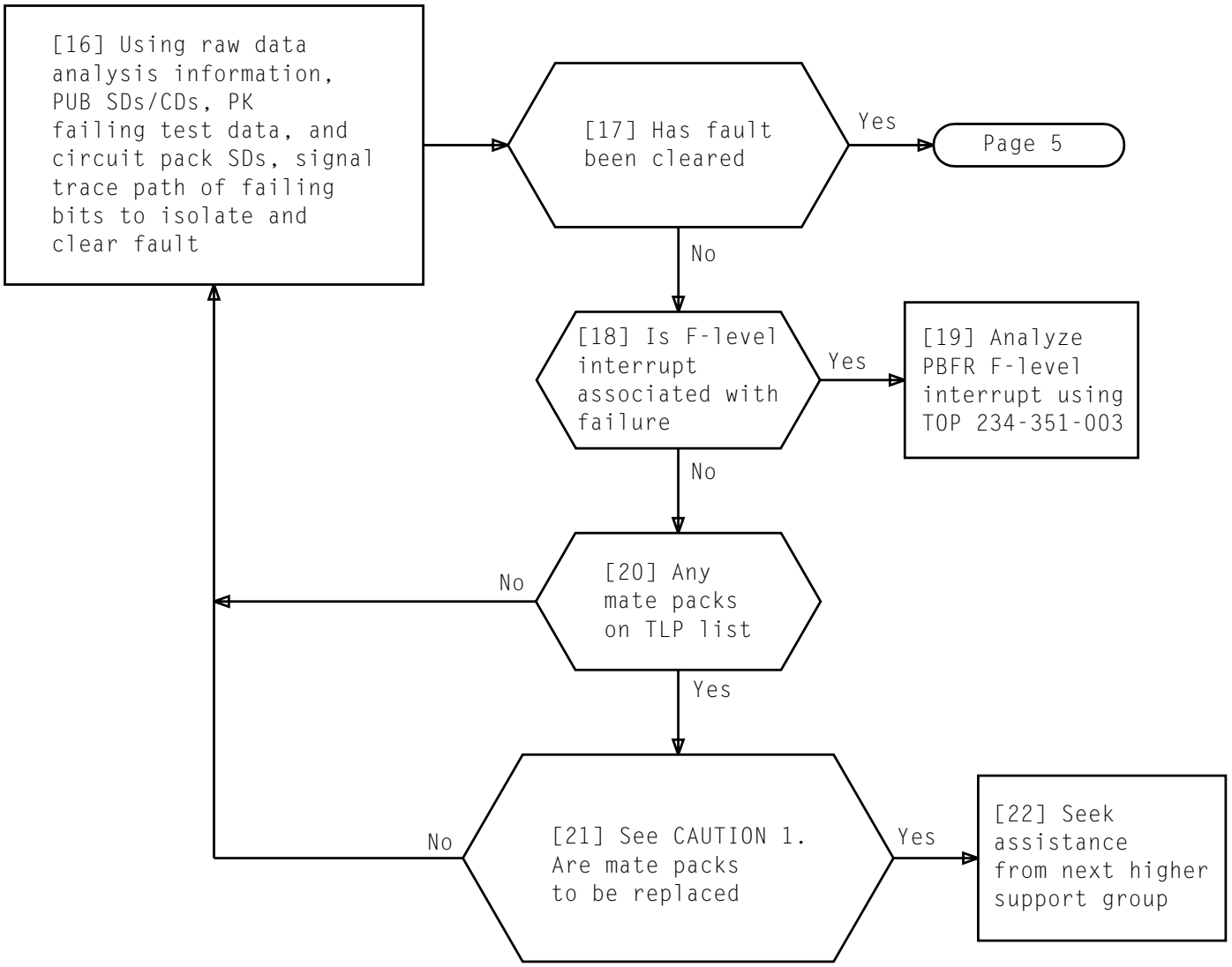


FIG. 1 – SYNC Pulse Display

NOTES

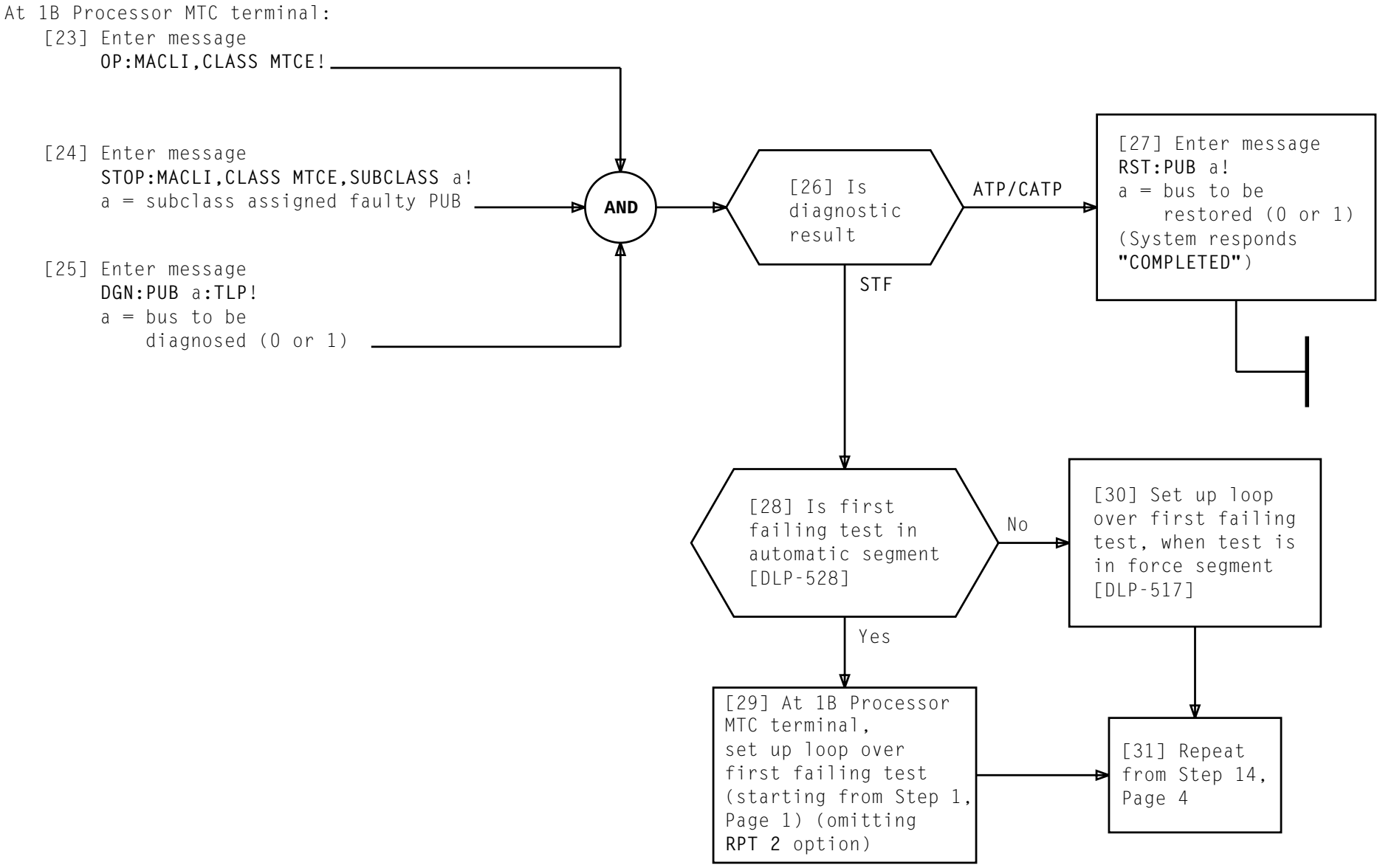
2. * = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)
3. SYNC pulse arrives over PUWB bit 36 which is not tested by PUB diagnostics

CLEAR DIAGNOSTIC FAILURE BY LOOPING OVER FIRST FAILING TEST AND SIGNAL TRACING

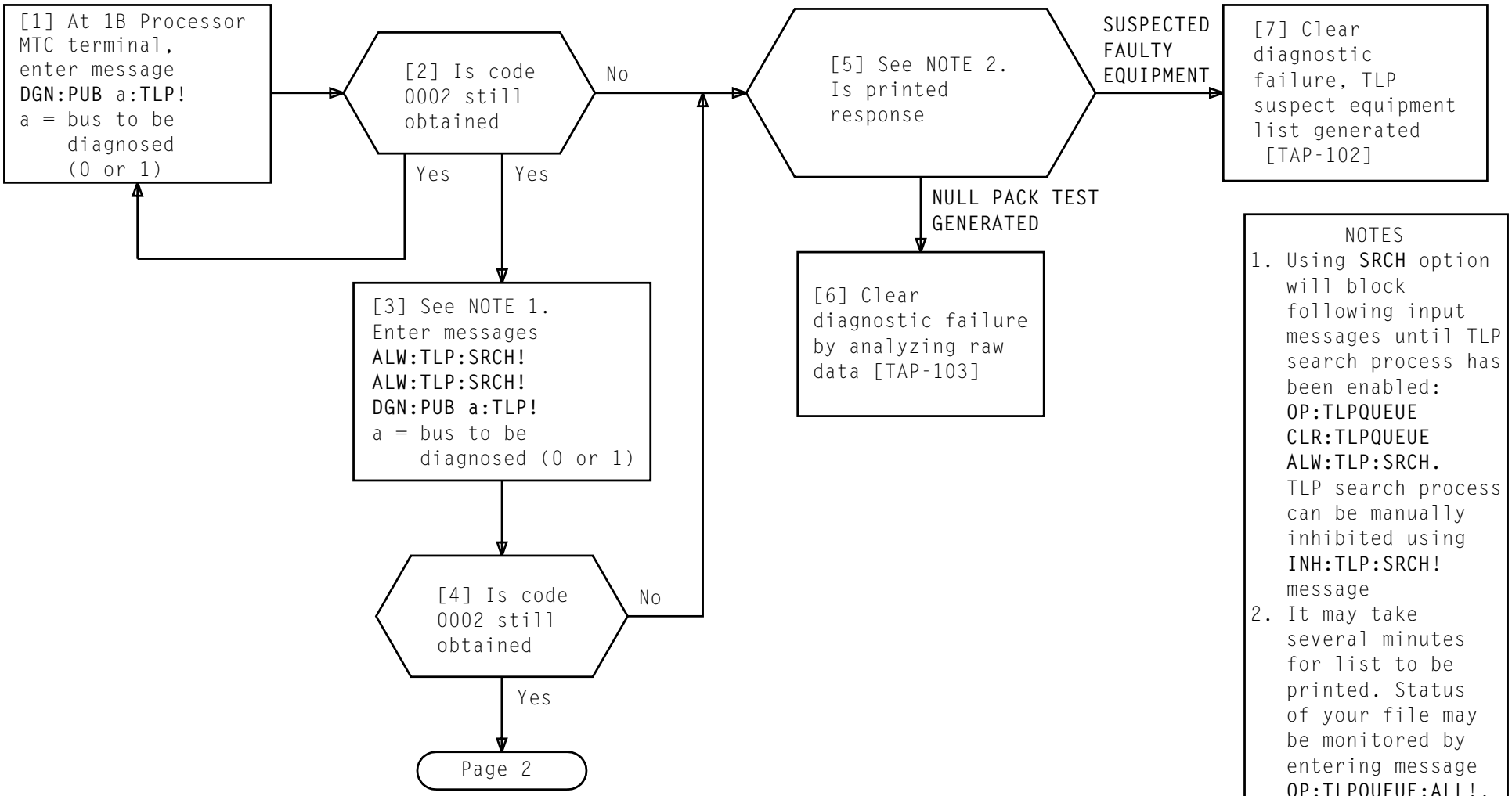


CAUTION 1
Mate pack replacement may cause service degrading condition

CLEAR DIAGNOSTIC FAILURE BY LOOPING OVER FIRST FAILING TEST AND SIGNAL TRACING



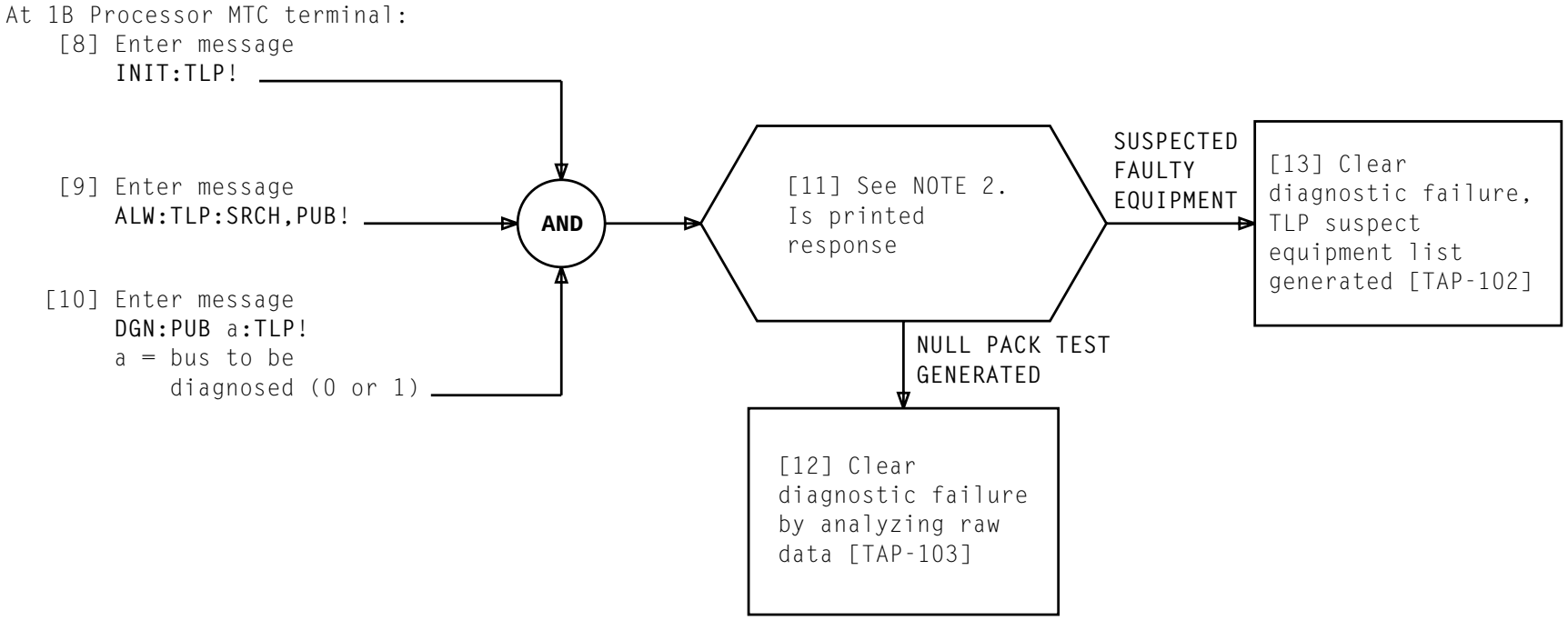
CLEAR DIAGNOSTIC FAILURE BY LOOPING OVER FIRST FAILING TEST AND SIGNAL TRACING



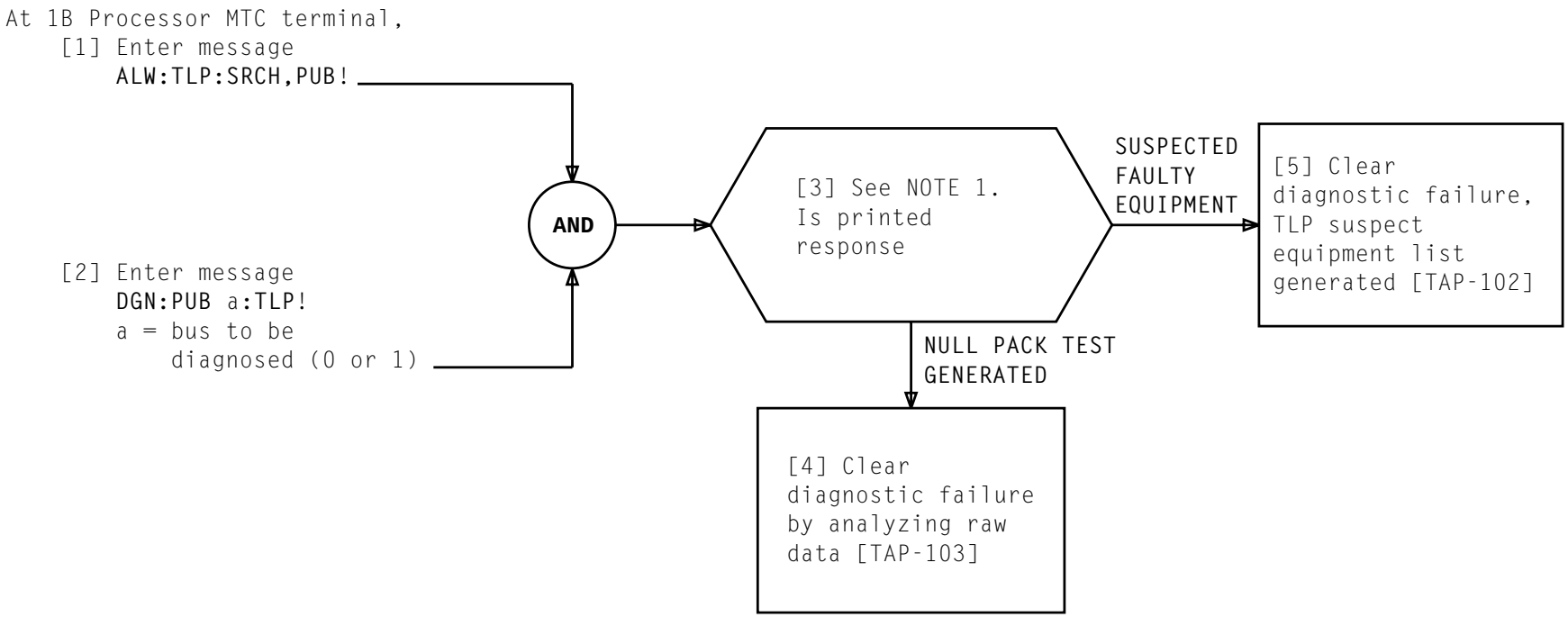
NOTES

1. Using **SRCH** option will block following input messages until TLP search process has been enabled:
   OP:TLPQUEUE
   CLR:TLPQUEUE
   ALW:TLP:SRCH.
   TLP search process can be manually inhibited using **INH:TLP:SRCH!** message
2. It may take several minutes for list to be printed. Status of your file may be monitored by entering message **OP:TLPQUEUE;ALL!.** TLP file currently being processed is indicated by asterisk in priority column

CLEAR DIAGNOSTIC FAILURE, TLPQUEUE BLOCKAGE

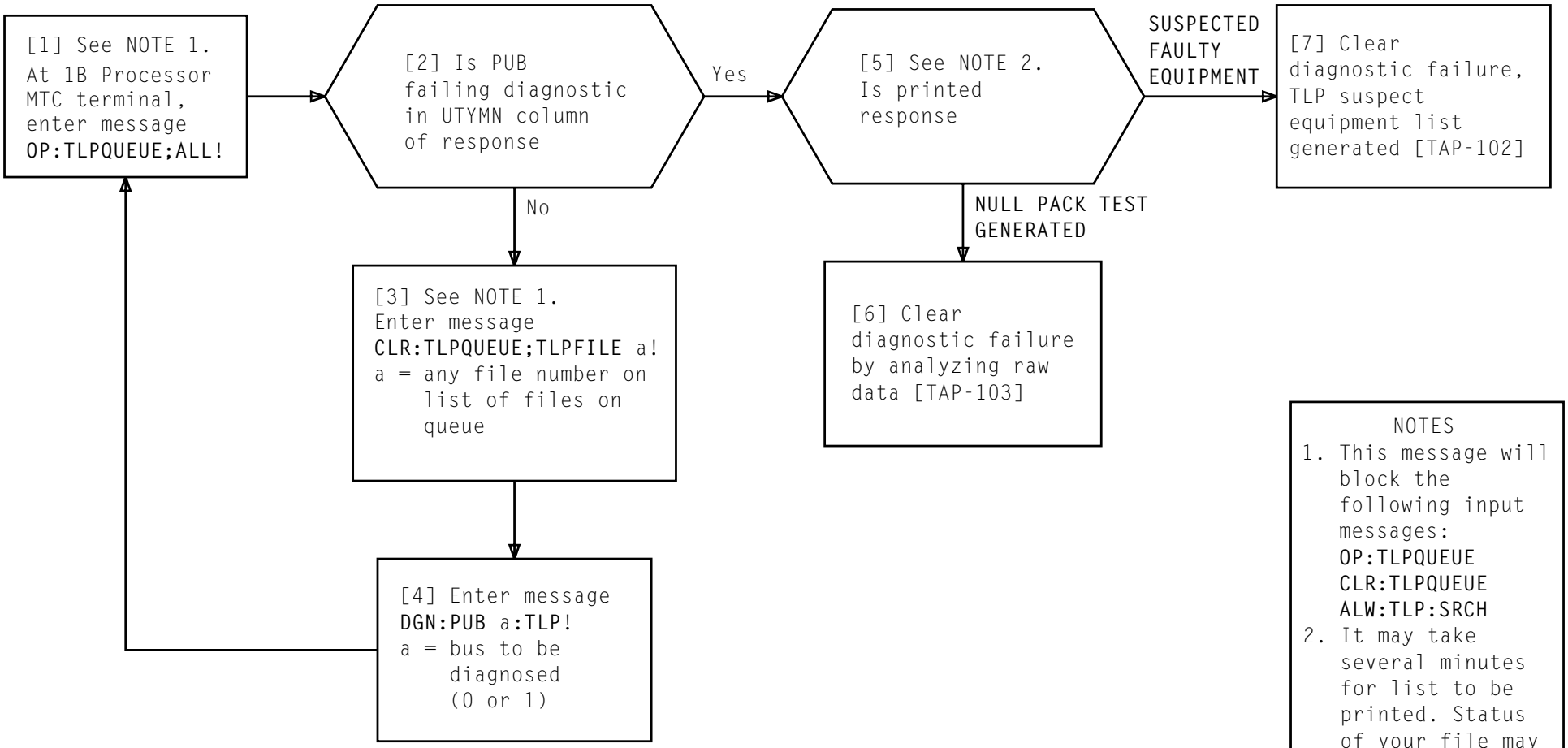


CLEAR DIAGNOSTIC FAILURE, TLPQUEUE BLOCKAGE



NOTE 1
It may take several minutes for list to be printed. Status of your file may be monitored by entering message OP:TLPQUEUE;ALL!. TLP file currently being processed is indicated by asterisk in priority column

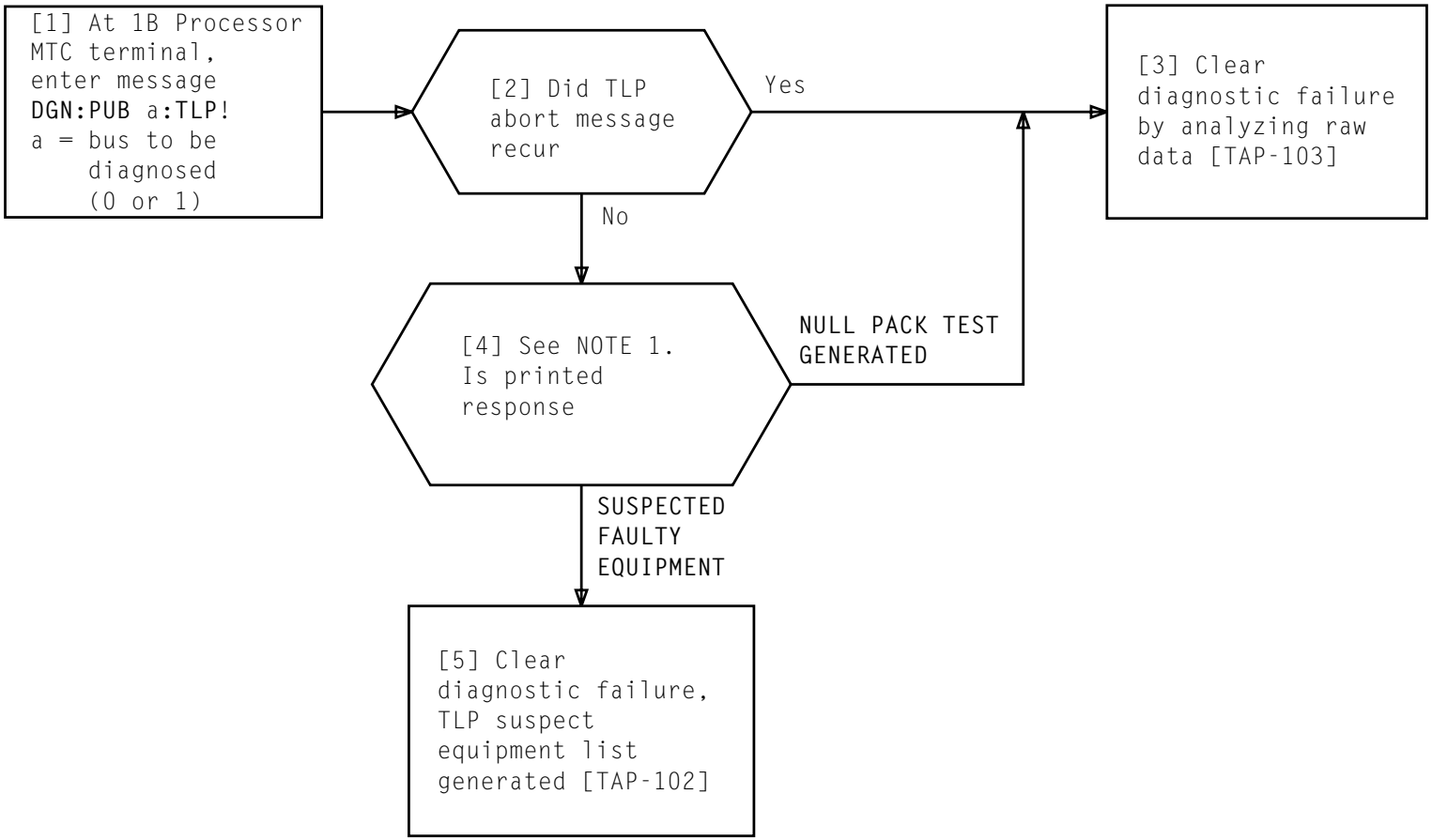
CLEAR DIAGNOSTIC FAILURE, TLP INHIBIT



NOTES

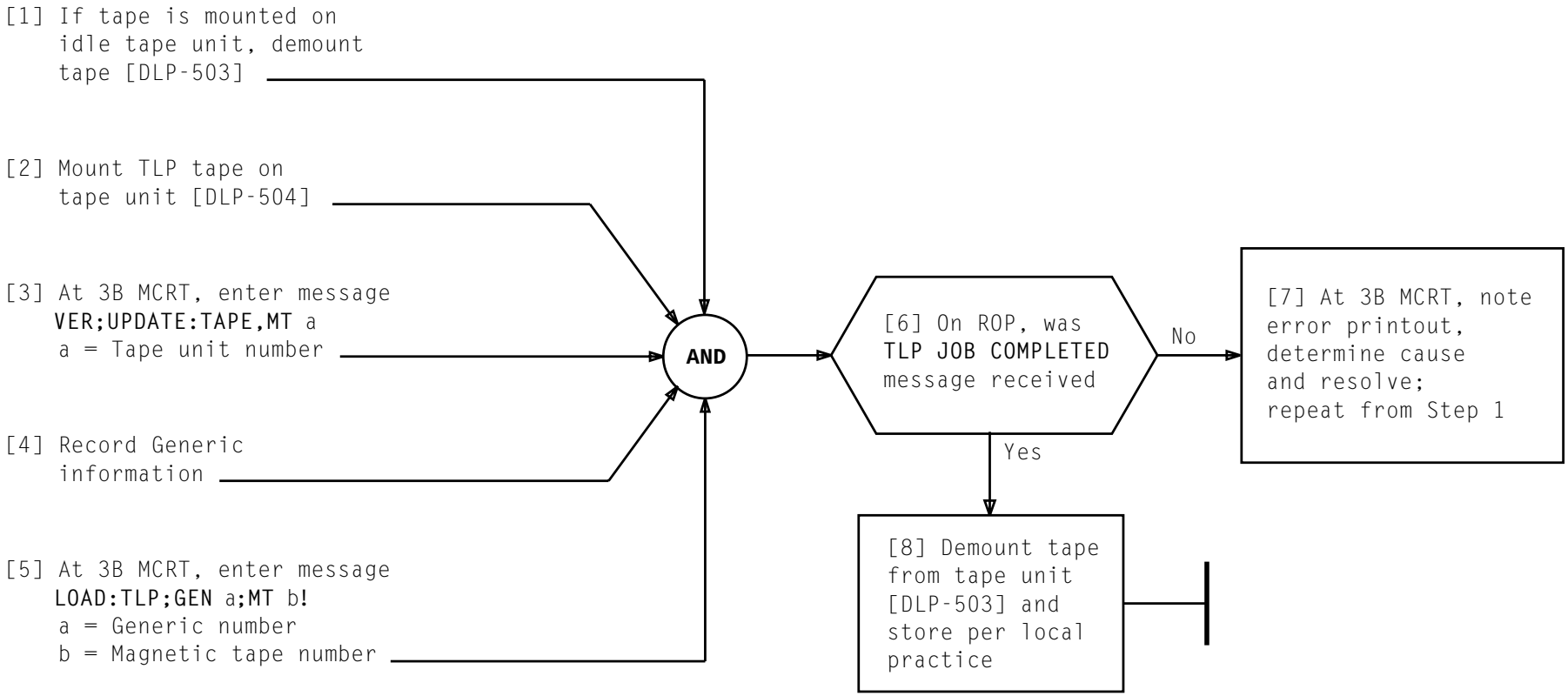
1. This message will block the following input messages:
   OP:TLPQUEUE
   CLR:TLPQUEUE
   ALW:TLP:SRCH
2. It may take several minutes for list to be printed. Status of your file may be monitored by entering message OP:TLPQUEUE;ALL!. TLP file currently being processed is indicated by asterisk in priority column

CLEAR DIAGNOSTIC FAILURE, TLP DISK QUEUE FULL



NOTE 1
It may take several minutes for list to be printed. Status of your file may be monitored by entering message OP:TLPQUEUE;ALL!. TLP file currently being processed is indicated by asterisk in priority column

CLEAR DIAGNOSTIC FAILURE, TLP ABORT



LOAD NEW 1600 BPI/4mm TLP FROM TAPE ONTO DISK FOR 4E22 AND LATER GENERICS

1. Set scope **A** and **B TIME/DIV** settings to 0.5 µsec and note bus bit being scoped

2. Locate waveform that most closely resembles scope pattern [FIG. 1, Page 2]

3. On TABLE A, Page 3, locate waveform chosen (A, B, C, etc); determine probable cause of trouble and perform suggested troubleshooting procedure

End of procedure

CLEAR EQUIPMENT TROUBLE, PU BUS

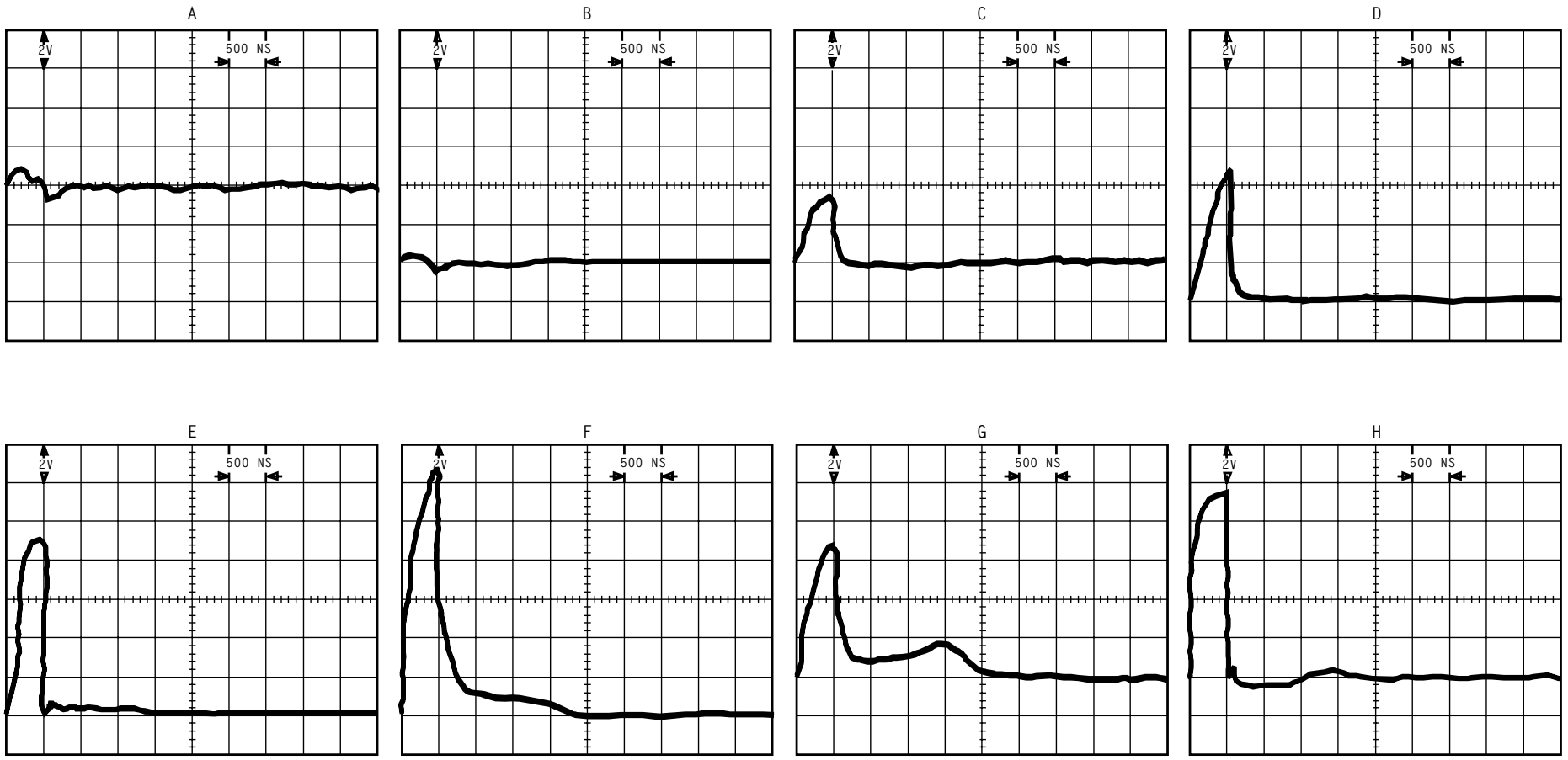


FIG. 1 – BUS Waveforms

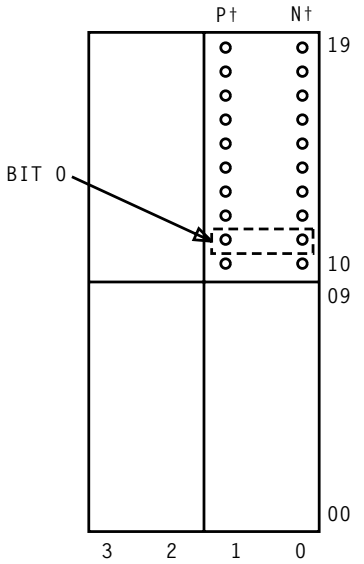
CLEAR EQUIPMENT TROUBLE, PU BUS

TABLE A		
WAVEFORM	**SCOPE PATTERN INDICATES PROBABLE CAUSE OF TROUBLE TO BE:**	**GENERAL TROUBLESHOOTING NOTES**
A	Open P or N wire	If branch is not terminated at PUBB frame, use office record drawing T-nnnn-Hn-3840 to determine what frame is approximately halfway along branch; terminate same bus bit with BTR and scope at that point for normal pulse.* In this manner, narrow location of open between two adjacent frames†
B	Short across bus cable pair — very near scope probes	Use same procedure used for Waveform A
C	Possible high series resistance on bus pair between PUBB frame and BTR	Scope for normal pulse on same bus pair at PUBB frame. If normal, use same procedure used for Waveform A
D	Normal pulse (500 feet from driver	If this pattern is obtained at PUBB frame, it is not normal. Output is too low, or marginal. Output should be between +8.9 and +9.7 volts
E	Normal pulse (pattern at driver)	If this pattern is obtained at 300 to 500 feet at BTR, then BTR could be partially open
F	Open at BTR (500 feet from driver)	Replace BTR assembly with known good assembly and scope same bus bit to verify
G	One side of bus grounded at or near driver (pattern at 500 feet from driver)	Start at PUBB frame and isolate using same procedure used for Waveform A
H	Short P wire to P wire of bit pair/or P wire to N wire of another	Use same procedure used for Waveform A

* Using appropriate figure [FIG. 2 through 39], locate terminal connections for frame being terminated in BTR and bus bit being scoped

† At each frame location where bus pair is scoped, that bus pair should be temporarily terminated in BTR at that point if not normally terminated in BTR

CLEAR EQUIPMENT TROUBLE, PU BUS

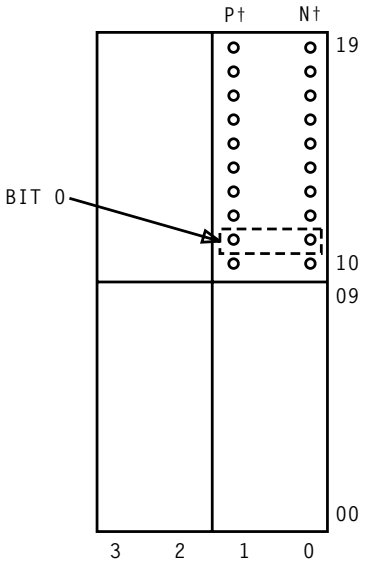


† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FRAME	BIT 0
CCIS	*80-25
EST	
BUS 0	080-17
BUS 1	080-38
IO	
BUS 0	080-03
BUS 1	080-27
IOP	
BUS 0	080-31
BUS 1	076-31
NCLK	*60-40
SP 1 (W/O COMBINED MATRIX FR)	
BUS 0	380-14
BUS 1	480-14
SP 1 (WITH COMBINED MATRIX FR)	
BUS 0	280-32
BUS 1	380-32
SP 2	
BUS 0	180-28
BUS 1	280-28
TMS A-1,2	*80-14
TMS B	
BUS 0	‡76-32
BUS 1	‡80-32
TSI A-1	*80-46
TSI A-2	*80-51
TSI B	*80-55

* 0 FOR BUS 0 OR 1 FOR BUS 1
‡ 0 FOR PUB TERMINATING AT
TMS BAY 0 OR 1 FOR PUB
TERMINATING AT TMS BAY 1

FIG. 2 — Terminal Connections for Write Bus Bit 0 — CCIS, EST, IO, IOP, NCLK, SP, TMS, and TSI Frames



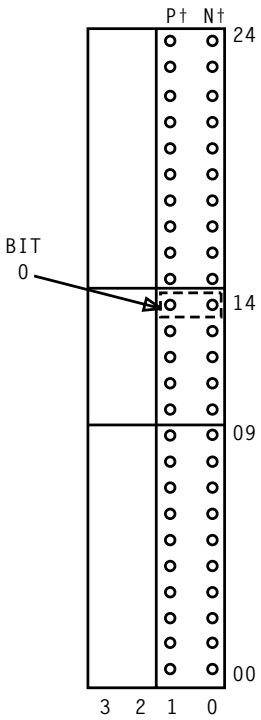
† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

PUBB FRAME	BIT 0
BRANCH A	*76-03
BRANCH B	*72-06
BRANCH C	*76-05
BRANCH D	*72-07
BRANCH E	*64-03
BRANCH F	*60-06
BRANCH G	*64-05
BRANCH H	*60-07
BRANCH K	*48-03
BRANCH L	*44-06
BRANCH M	*48-05
BRANCH R	*44-07
BRANCH T	*36-03
BRANCH V	*32-06
BRANCH W	*36-05
BRANCH X	*32-07

* 0 FOR BUS 0 OR 1 FOR BUS 1

FIG. 3 — Terminal Connections for Write Bus Bit 0 — PUBB Frame

CLEAR EQUIPMENT TROUBLE, PU BUS



FRAME	BIT 0
DIF	
BUS 0	180-109
BUS 1	180-257

† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 4 — Terminal Connections for Write Bus Bit 0 — DIF Frames

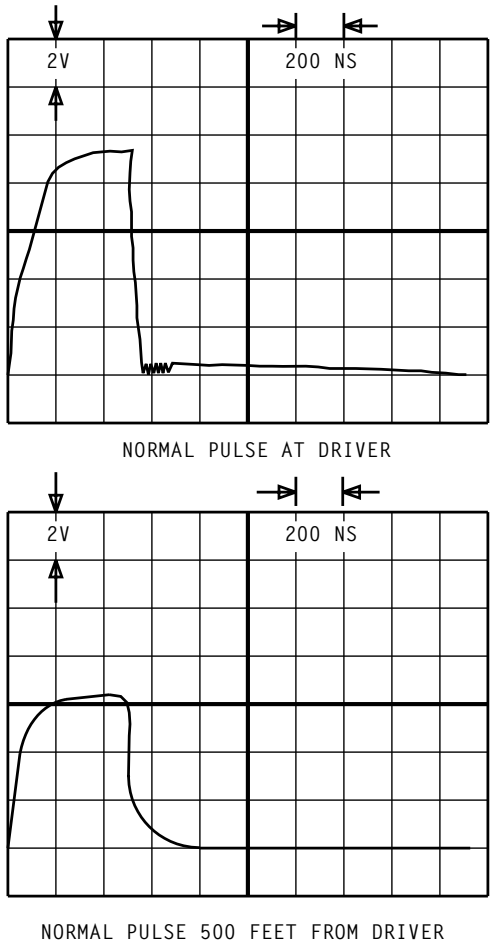
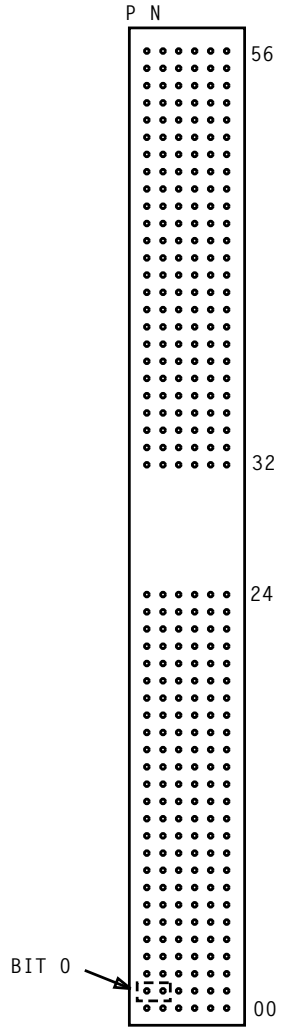


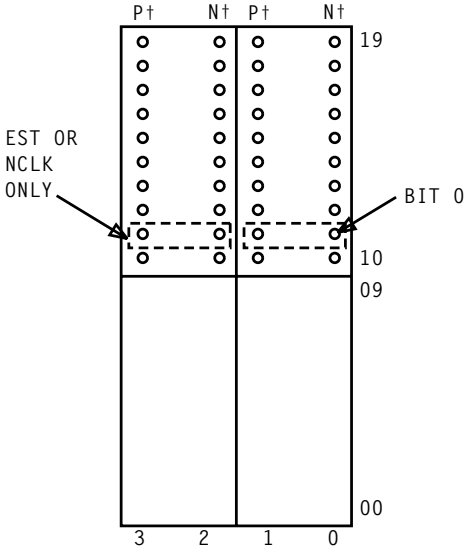
FIG. 5 — Example Waveforms of Normal Pulse at Driver and 500 Feet From Driver for Write Bus Bit 0



SCS		XTSI	
BUS 0	045-168	BUS 0	052-180
BUS 1	053-168	BUS 1	061-180

FIG. 6 — Terminal Connection for Write Bus Bit 0 — SCS and XTSI Frames

CLEAR EQUIPMENT TROUBLE, PU BUS

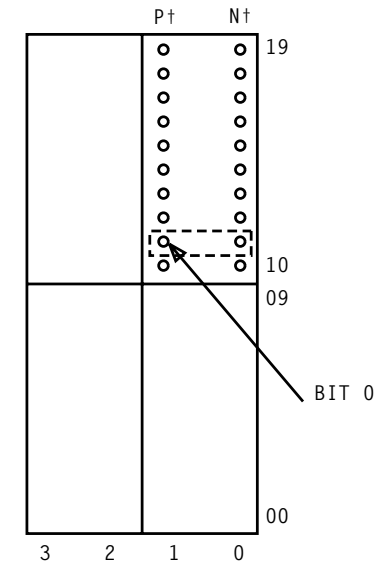


† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FRAME	BIT 0
CCIS	*80-33
EST	
BUS 0	080-02
BUS 1	080-23
IO	
BUS 0	080-11
BUS 1	080-36
IOP	
BUS 0	080-40
BUS 1	076-40
NCLK	*60-48
SP 1 (W/O COMBINED MATRIX FR)	
BUS 0	380-04
BUS 1	480-04
SP 1 (WITH COMBINED MATRIX FR)	
BUS 0	280-20
BUS 1	380-20
SP 2	
BUS 0	180-18
BUS 1	280-18
TMS A-1,2	*80-04
TMS B	
BUS 0	‡76-20
BUS 1	‡80-20
TSI A-1	*80-36
TSI A-2	*80-39
TSI B	*80-43
VIF	
BUS 0	152-15
BUS 1	152-25

* 0 FOR BUS 0 OR 1 FOR BUS 1
‡ 0 FOR PUB TERMINATING AT TMS
BAY 0 OR 1 FOR BUS TERMINATING
AT TMS BAY 1

FIG. 7 — Terminal Connections for Reply Bus Bit 0 — CCIS, EST, IO, IOP, NCLK, SP, TMS, TSI, and VIF Frames



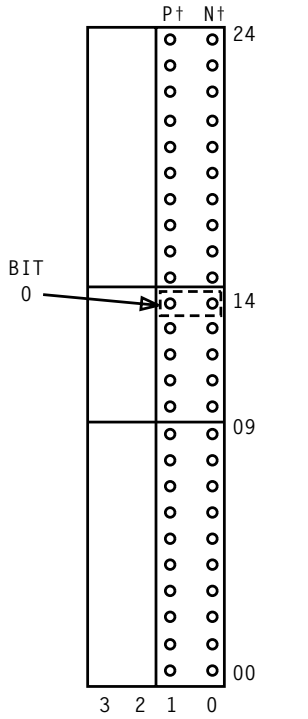
† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

PUBB FRAME	BIT 0
BRANCH A	*76-19
BRANCH B	*72-17
BRANCH C	*76-20
BRANCH D	*72-18
BRANCH E	*64-19
BRANCH F	*60-17
BRANCH G	*64-20
BRANCH H	*60-18
BRANCH K	*48-19
BRANCH L	*44-17
BRANCH M	*48-20
BRANCH R	*44-18
BRANCH T	*36-19
BRANCH V	*32-17
BRANCH W	*36-20
BRANCH X	*32-18

* 0 FOR BUS 0 OR 1 FOR BUS 1

FIG. 8 — Terminal Connections for Reply Bus Bit 0 — PUBB Frame

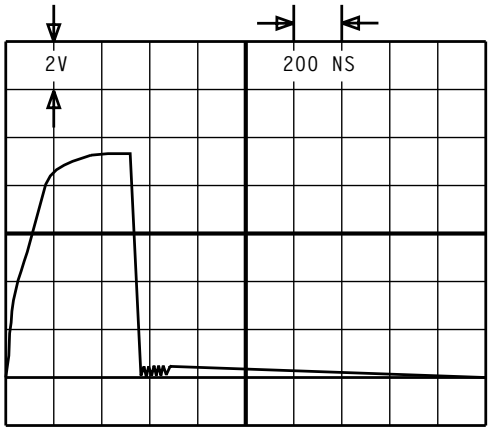
CLEAR EQUIPMENT TROUBLE, PU BUS



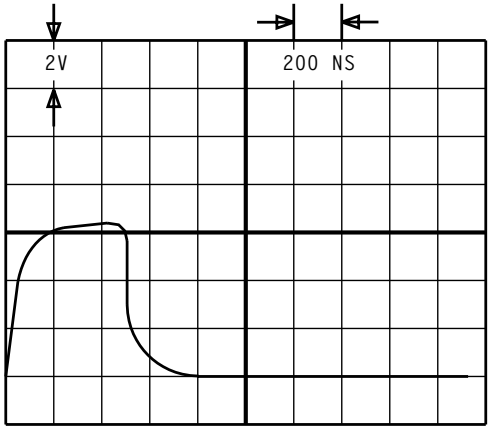
FRAME	BIT 0
DIF	
BUS 0	180-053
BUS 1	180-201

†P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 9 — Terminal Connections for Reply Bus Bit 0 — DIF Frames

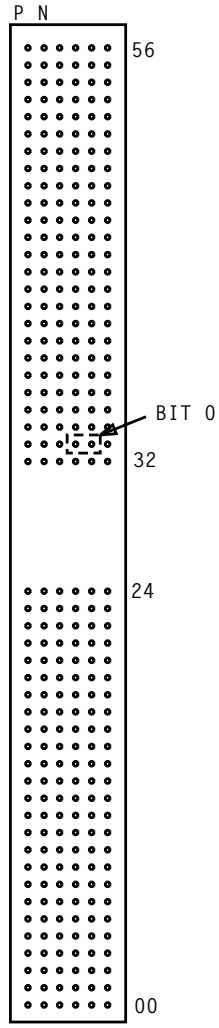


NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

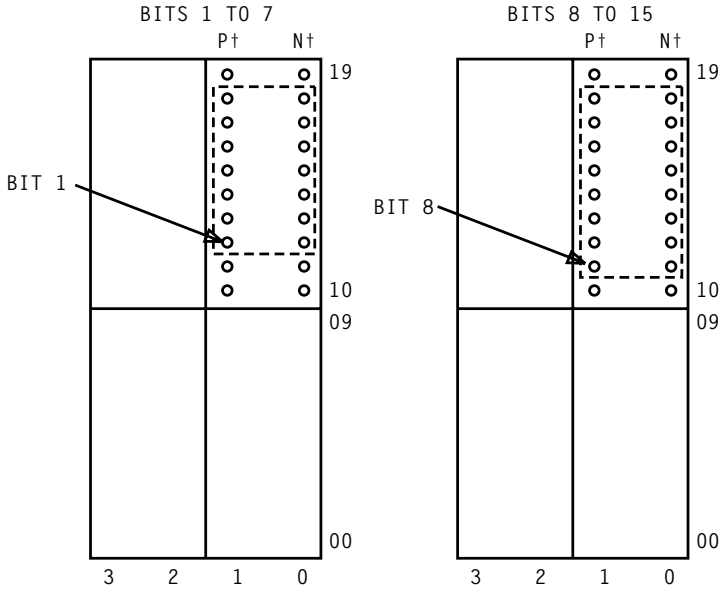
FIG. 10 — Example Waveforms of Normal Pulse at Driver and 500 Feet From Driver for Reply Bus Bit 0



SCS		XTSI	
BUS 0	045-168	BUS 0	052-180
BUS 1	053-168	BUS 1	061-180

FIG. 11 — Terminal Connections for Reply Bus Bit 0 — SCS and XTSI Frames

CLEAR EQUIPMENT TROUBLE, PU BUS



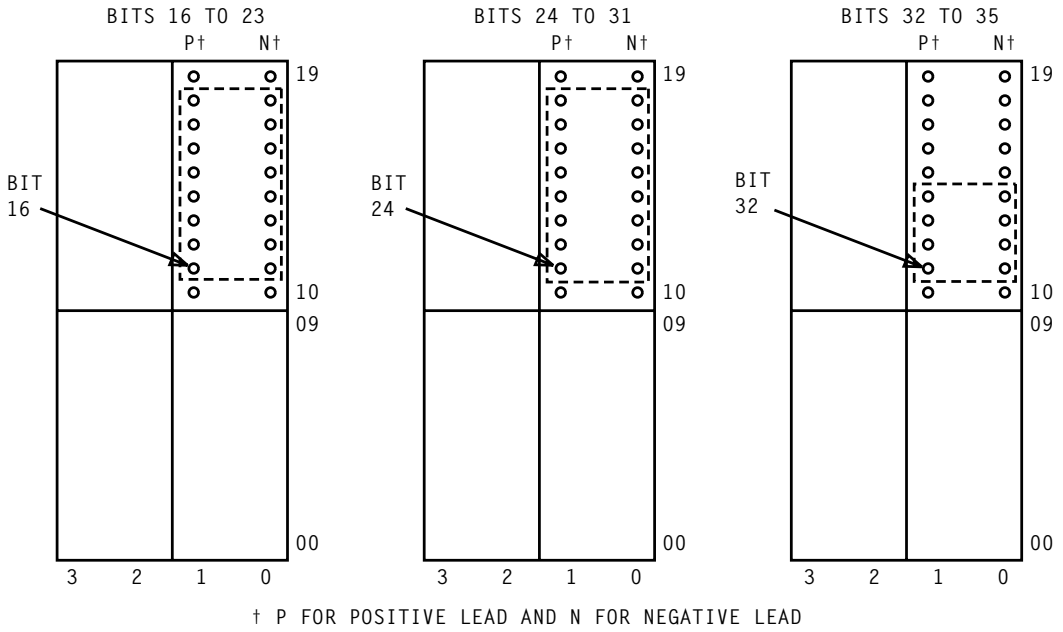
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FRAME	BITS 1 TO 7	BITS 8 TO 15
CCIS	*80-25	*80-23
EST		
BUS 0	080-17	080-16
BUS 1	080-38	080-37
IO		
BUS 0	080-03	080-04
BUS 1	080-27	080-28
IOP		
BUS 0	080-31	080-33
BUS 1	076-31	076-33
NCLK	*60-40	*60-39
SP 1 (W/O COMBINED MATRIX FR)		
BUS 0	380-14	380-13
BUS 1	480-14	480-13
SP 1 (WITH COMBINED MATRIX FR)		
BUS 0	280-32	280-30
BUS 1	380-32	380-30
SP 2		
BUS 0	180-28	180-27
BUS 1	280-28	280-27
TMS A-1,2	*80-14	*80-13
TMS B		
BUS 0	‡76-32	‡76-30
BUS 1	‡80-32	‡80-30
TSI A-1	*80-46	*80-45
TSI A-2	*80-51	*80-49
TSI B	*80-55	*80-53

* 0 FOR BUS 0 OR 1 FOR BUS 1
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 12 — Terminal Connections for Write Bus Bits 1 Through 15 — CCIS, EST, IO, IOP, NCLK, SP, TMS, and TSI Frames

CLEAR EQUIPMENT TROUBLE, PU BUS



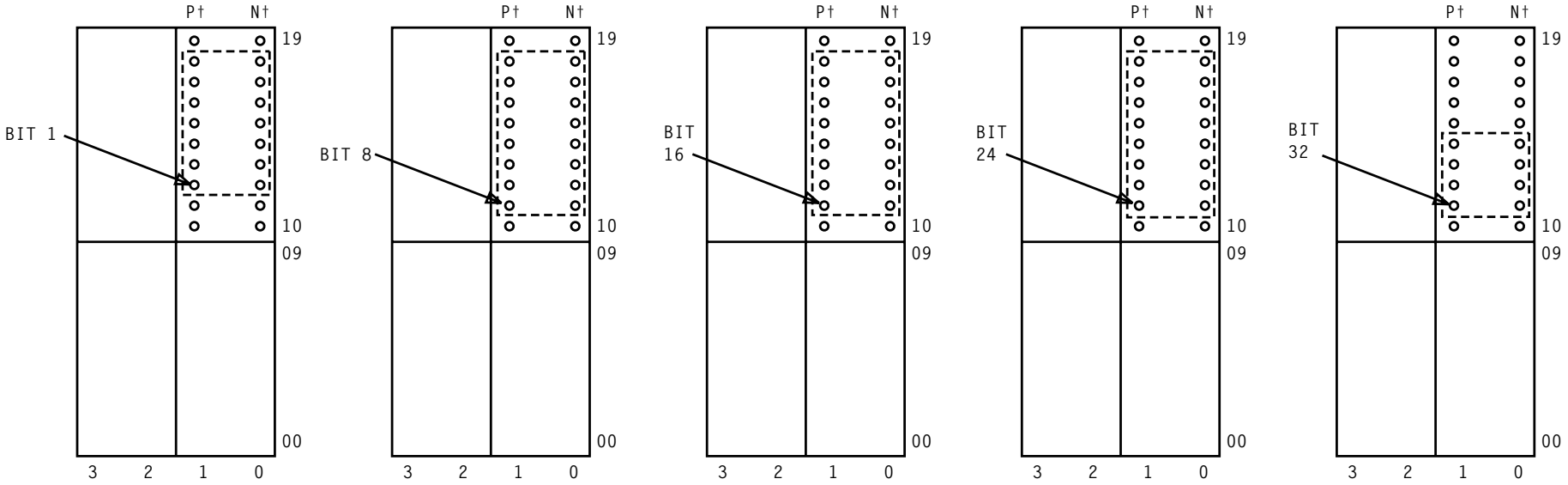
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FRAME	BITS 16 TO 23	BITS 24 TO 31	BITS 32 TO 35
CCIS	*80-21	*80-19	*80-18
EST			
BUS 0	080-15	080-14	080-13
BUS 1	080-36	080-35	080-34
IO			
BUS 0	080-05	080-06	080-07
BUS 1	080-29	080-31	080-32
IOP			
BUS 0	080-34	080-36	080-37
BUS 1	076-34	076-36	076-37
NCLK	*60-38	*60-37	*60-36
SP 1 (W/O COMBINED MATRIX FR)			
BUS 0	380-12	380-11	380-10
BUS 1	480-12	480-11	480-10
SP 1 (WITH COMBINED MATRIX FR)			
BUS 0	280-29	280-27	280-26
BUS 1	380-29	380-27	380-26
SP 2			
BUS 0	180-26	180-25	180-24
BUS 1	280-26	280-25	280-24
TMS A-1,2	*80-12	*80-11	*80-10
TMS B			
BUS 0	‡76-29	‡76-27	‡76-26
BUS 1	‡80-29	‡80-27	‡80-26
TSI A-1	*80-44	*80-43	*80-42
TSI A-2	*80-48	*80-46	*80-45
TSI B	*80-52	*80-50	*80-49

* 0 FOR BUS 0 OR 1 FOR BUS 1
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 13 — Terminal Connections for Write Bus Bits 16 Through 35 — CCIS, EST, IO, IOP, NCLK, SP, TMS, and TSI Frames

CLEAR EQUIPMENT TROUBLE, PU BUS



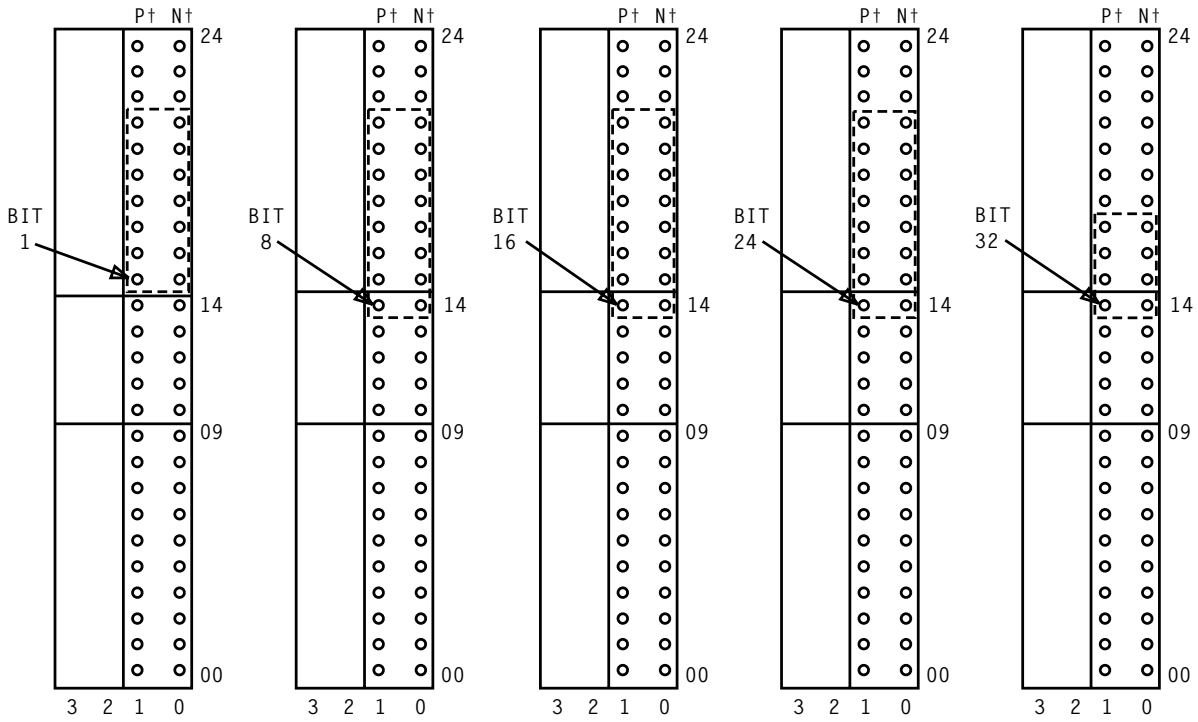
PUBB FRAME	BITS 1 TO 7	BITS 8 TO 15	BITS 16 TO 23	BITS 24 TO 31	BITS 32 TO 35
BRANCH A	*76-03	*76-12	*76-34	*76-06	*76-09
BRANCH B	*72-06	*72-12	*72-34	*72-08	*72-10
BRANCH C	*76-05	*76-14	*76-36	*76-08	*76-11
BRANCH D	*72-07	*72-13	*72-35	*72-09	*72-11
BRANCH E	*64-03	*64-12	*64-34	*64-06	*64-09
BRANCH F	*60-06	*60-12	*60-34	*60-08	*60-10
BRANCH G	*64-05	*64-14	*64-36	*64-08	*64-11
BRANCH H	*60-07	*60-13	*60-35	*60-09	*60-11
BRANCH K	*48-03	*48-12	*48-34	*48-06	*48-09
BRANCH L	*44-06	*44-12	*44-34	*44-08	*44-10
BRANCH M	*48-05	*48-14	*48-36	*48-08	*48-11
BRANCH R	*44-07	*44-13	*44-35	*44-09	*44-11
BRANCH T	*36-05	*36-12	*36-34	*36-06	*36-09
BRANCH V	*32-06	*32-12	*32-34	*32-08	*32-10
BRANCH W	*36-05	*36-14	*36-36	*36-08	*36-11
BRANCH X	*32-07	*32-13	*32-35	*32-09	*32-11

* 0 FOR BUS 0 OR 1 FOR BUS 1

† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 14 — Terminal Connections for Write Bus Bits 1 Through 35 — PUBB Frame

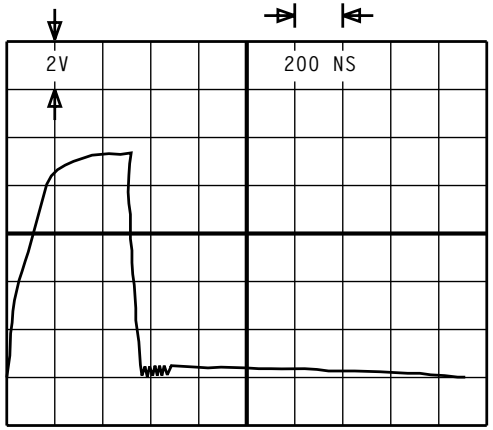
CLEAR EQUIPMENT TROUBLE, PU BUS



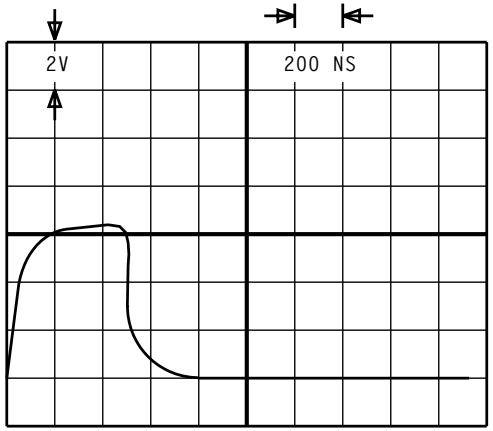
FRAME	BITS 1 TO 7	BITS 8 TO 15	BITS 16 TO 23	BITS 24 TO 31	BITS 32 TO 35
DIF					
BUS 0	180-109	180-103	180-097	180-091	180-085
BUS 1	180-257	180-251	180-245	180-239	180-233

† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 15 — Terminal Connections for Write Bus Bits 1 Through 35 — DIF Frames



NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 16 — Example Waveforms of Normal Pulse at Driver and 500 Feet From Driver for Write Bus Bits 1 Through 35

CLEAR EQUIPMENT TROUBLE, PU BUS

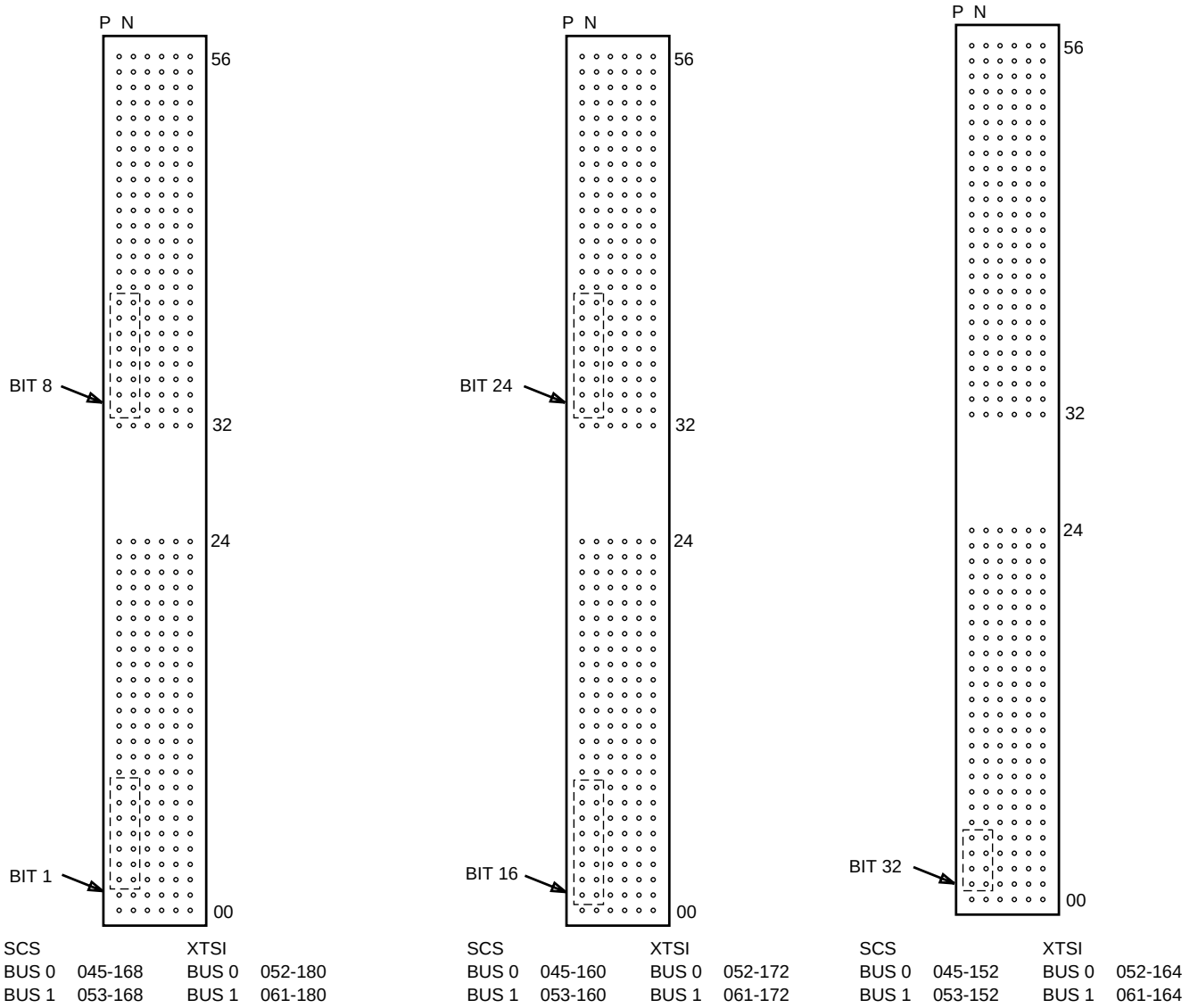
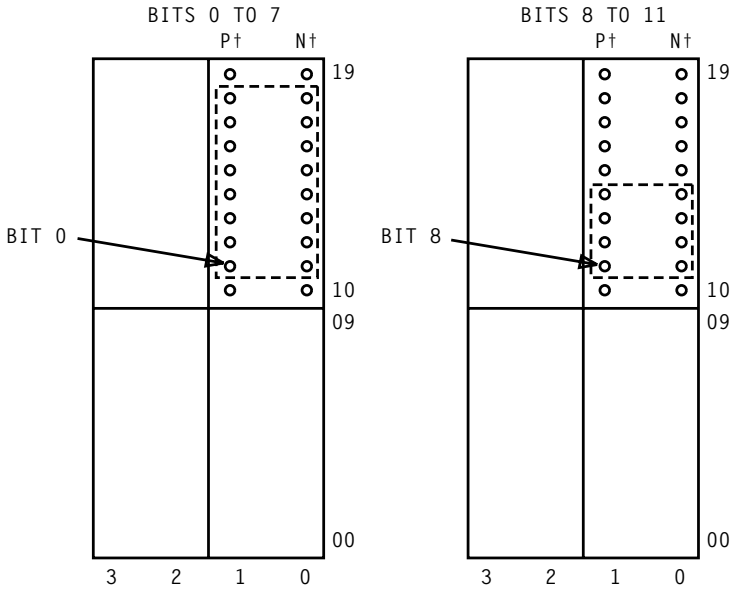


FIG. 17 – Terminal Connections for Write Bus Bits 1 Through 35 – SCS and XTSI Frames

CLEAR EQUIPMENT TROUBLE, PU BUS



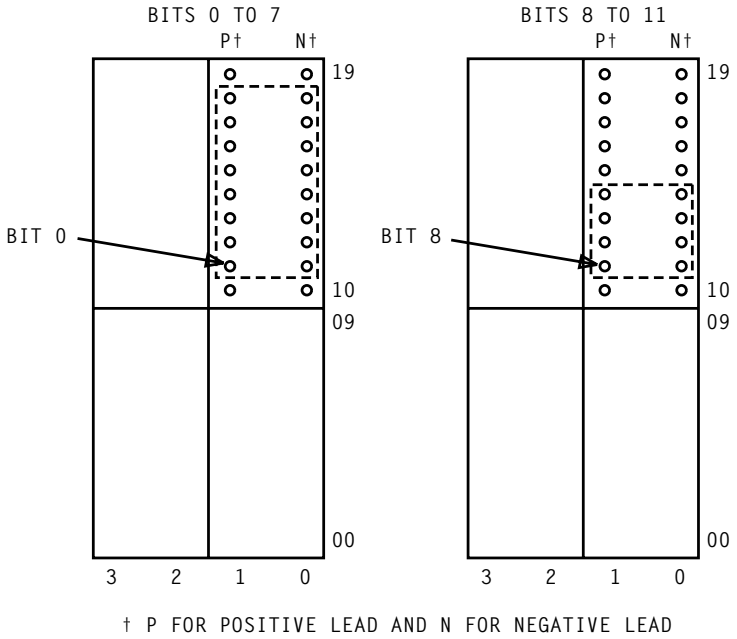
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FRAME	BITS 0 TO 7	BITS 8 TO 11
CCIS	*80-16	*80-15
EST		
BUS 0	080-12	080-11
BUS 1	080-33	080-32
IO		
BUS 0	080-08	080-09
BUS 1	080-33	080-34
IOP		
BUS 0	080-24	080-27
BUS 1	076-24	076-27
NCLK	*60-35	*60-34
SP 1 (W/O COMBINED MATRIX FR)		
BUS 0	380-09	380-08
BUS 1	480-09	480-08
SP 1 (WITH COMBINED MATRIX FR)		
BUS 0	280-24	280-23
BUS 1	380-24	380-23
SP 2		
BUS 0	180-23	180-22
BUS 1	280-23	280-22
TMS A-1,2	*80-09	*80-08
TMS B		
BUS 0	‡76-24	‡76-23
BUS 1	‡80-24	‡80-23
TSI A-1	*80-41	*80-40
TSI A-2	*80-43	*80-42
TSI B	*80-47	*80-46

* 0 FOR BUS 0 OR 1 FOR BUS 1
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR
1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 18 — Terminal Connections for Enable Address Bus Bits 0 Through 11 — CCIS, EST, IO, IOP, NCLK, SP, TMS, and TSI Frames

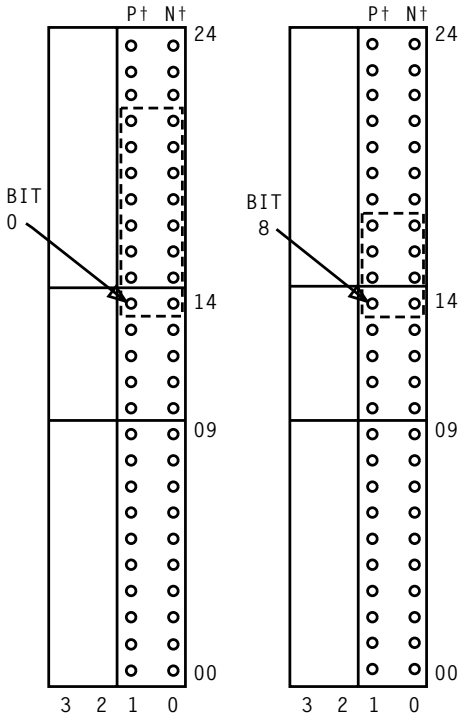
CLEAR EQUIPMENT TROUBLE, PU BUS



PUBB FRAME	BITS 0 TO 7	BITS 8 TO 11
BRANCH A	*76-37	*76-40
BRANCH B	*72-36	*72-38
BRANCH C	*76-39	*76-42
BRANCH D	*72-37	*72-39
BRANCH E	*64-37	*64-40
BRANCH F	*60-36	*60-38
BRANCH G	*64-39	*64-42
BRANCH H	*60-37	*60-39
BRANCH K	*48-37	*48-40
BRANCH L	*44-36	*44-38
BRANCH M	*48-39	*48-42
BRANCH R	*44-37	*44-39
BRANCH T	*36-37	*36-40
BRANCH V	*32-36	*32-38
BRANCH W	*36-39	*36-42
BRANCH X	*32-37	*32-39

* 0 FOR BUS 0 OR 1 FOR BUS 1

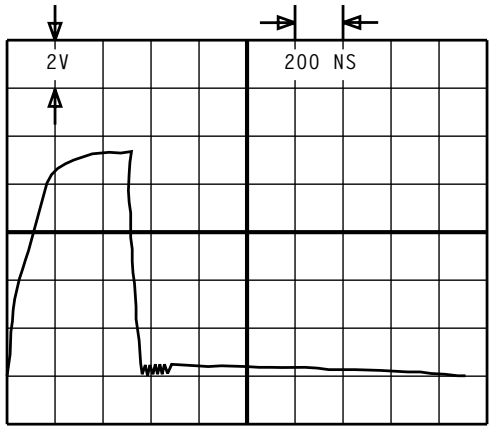
FIG. 19 — Terminal Connections for Enable Address Bus Bits 0 Through 11 — PUBB Frame



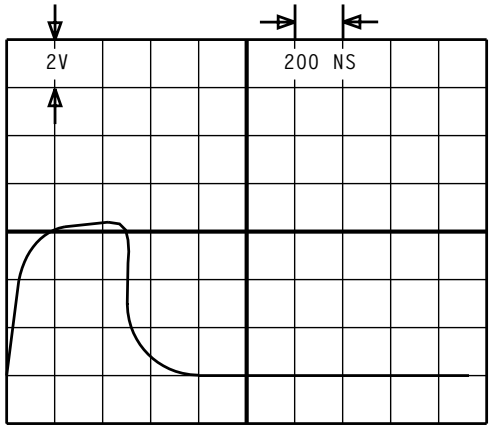
FRAME	BITS 0 TO 7	BITS 8 TO 11
DIF		
BUS 0	180-079	180-073
BUS 1	180-227	180-221

† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 20 — Terminal Connections for Enable Address Bus Bits 0 Through 11 — DIF Frames

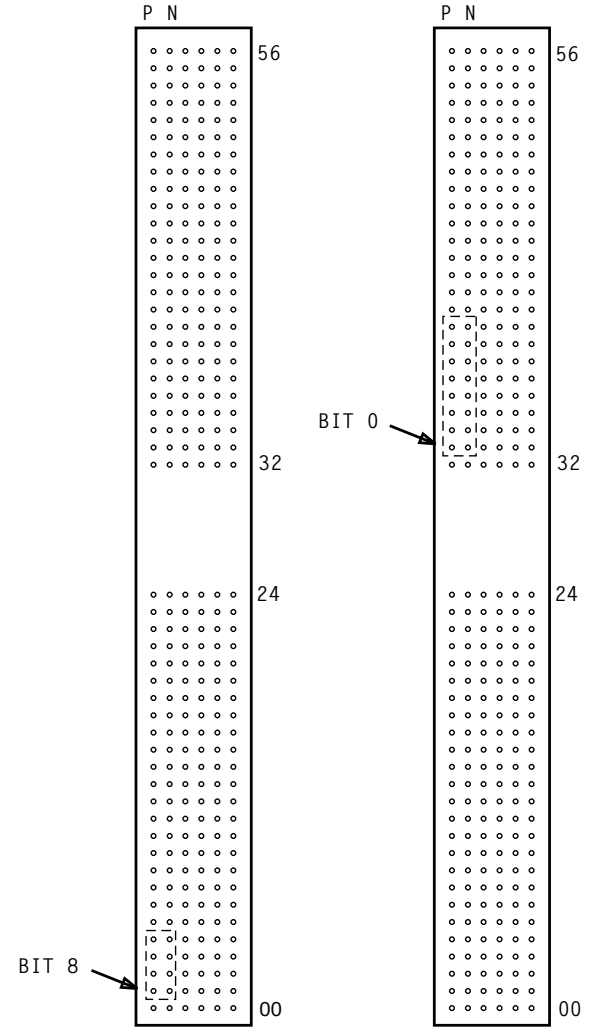


NORMAL PULSE AT DRIVER



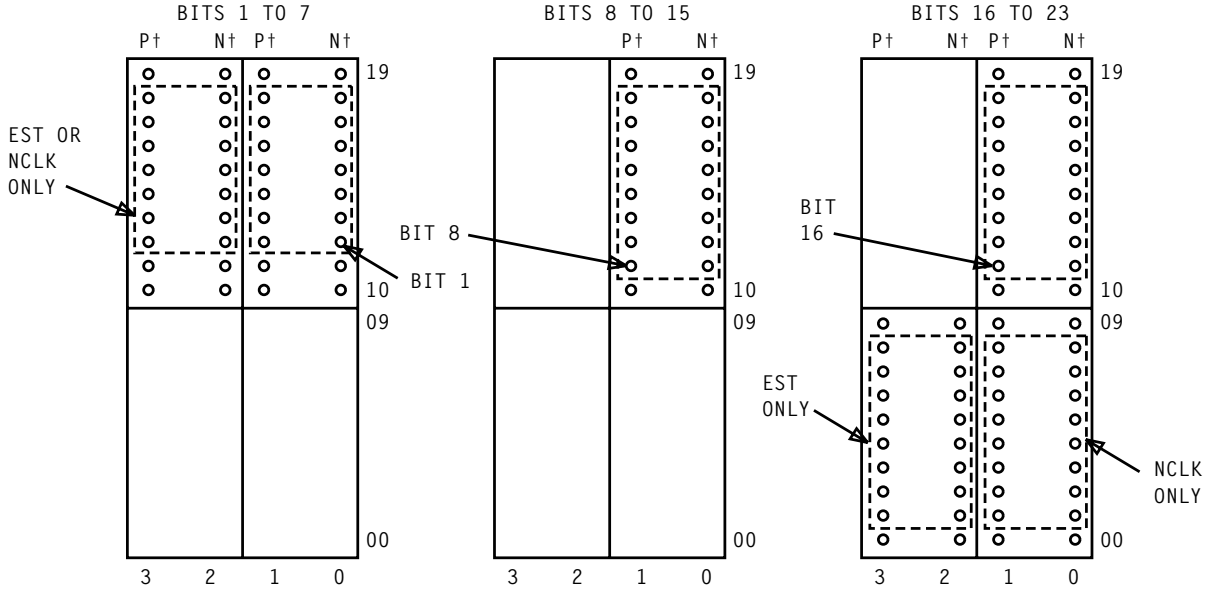
NORMAL PULSE 500 FEET FROM DRIVER

FIG. 21 — Example Waveforms of Normal Pulse at Driver and 500 Feet From Driver For Enable Address Bus Bits 0 Through 11



SCS		XTSI		SCS		XTSI	
BUS 0	045-144	BUS 0	052-156	BUS 0	045-152	BUS 0	052-164
BUS 1	053-144	BUS 1	061-156	BUS 1	053-152	BUS 1	061-164

FIG. 22 — Terminal Connections for Enable Address Bus Bits 0 Through 11 — SCS and XTSI Frames

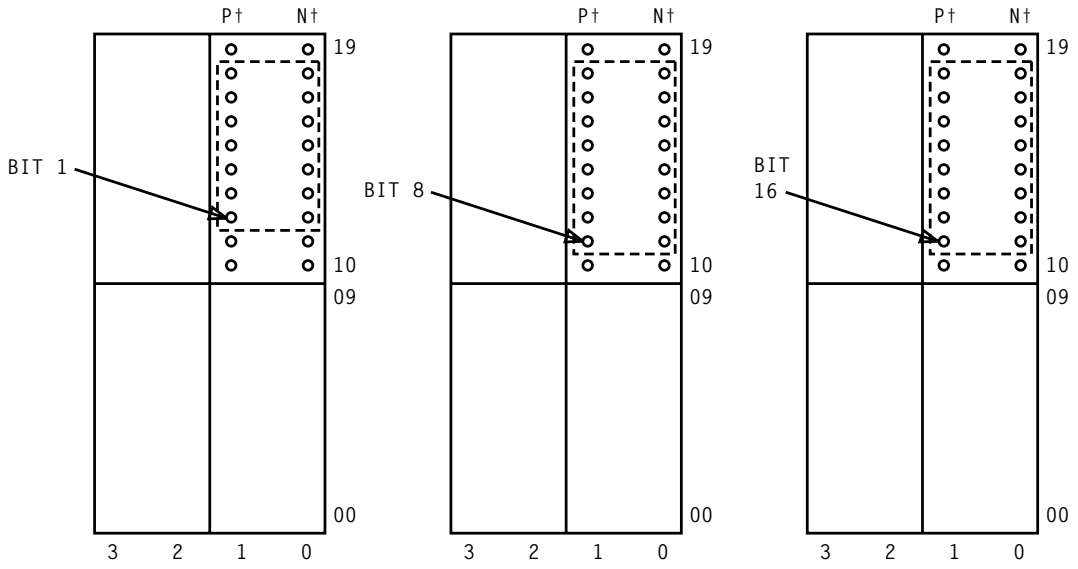


† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FRAME	BITS 1 TO 7	BITS 8 TO 15	BITS 16 TO 23
CCIS	*80-33	*80-32	*80-31
EST			
BUS 0	080-02	080-02	080-02
BUS 1	080-23	080-23	080-23
IO			
BUS 0	080-11	080-12	080-13
BUS 1	080-36	080-37	080-38
IOP			
BUS 0	080-40	080-41	080-42
BUS 1	076-40	076-41	076-42
NCLK	*60-48	*60-48	*60-48
SP 1 (W/O COMBINED MATRIX FR)			
BUS 0	380-04	380-03	380-02
BUS 1	480-04	480-03	480-02
SP 1 (WITH COMBINED MATRIX FR)			
BUS 0	280-20	280-18	280-16
BUS 1	380-20	380-18	380-16
SP 2			
BUS 0	180-18	180-17	180-16
BUS 1	280-18	280-17	280-16
TMS A-1,2	*80-04	*80-03	*80-02
TMS B			
BUS 0	‡76-20	‡76-18	‡76-16
BUS 1	‡80-20	‡80-18	‡80-16
TSI A-1	*80-36	*80-35	*80-34
TSI A-2	*80-39	*80-37	*80-35
TSI B	*80-43	*80-41	*80-39
VIF			
BUS 0	152-15	152-14	152-13
BUS 1	152-25	152-24	152-23

* 0 FOR BUS 0 OR 1 FOR BUS 1
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 23 — Terminal Connections for Reply Bus Bits 1 Through 23 — CCIS, EST, IO, IOP, NCLK, SP, TMS, TSI, and VIF Frames

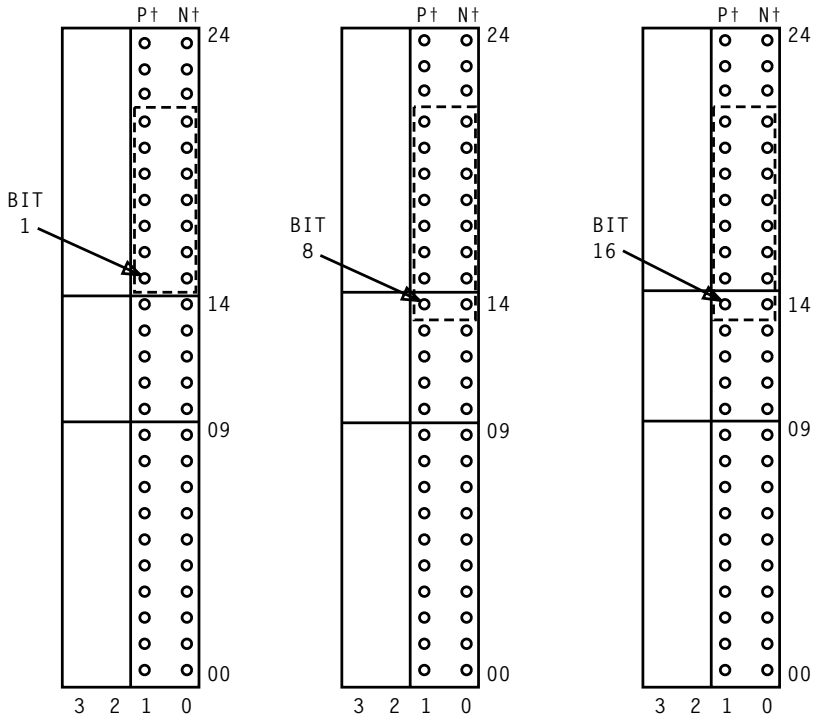


PUBB FRAME	BITS 1 TO 7	BITS 8 TO 15	BITS 16 TO 23
BRANCH A	*76-19	*76-21	*76-23
BRANCH B	*72-17	*72-19	*72-25
BRANCH C	*76-20	*76-22	*76-24
BRANCH D	*72-18	*72-20	*72-26
BRANCH E	*64-19	*64-21	*64-23
BRANCH F	*60-17	*60-19	*60-25
BRANCH G	*64-20	*64-22	*64-24
BRANCH H	*60-18	*60-20	*60-26
BRANCH K	*48-19	*48-21	*48-23
BRANCH L	*44-17	*44-19	*44-25
BRANCH M	*48-20	*48-22	*48-24
BRANCH R	*44-18	*44-20	*44-26
BRANCH T	*36-19	*36-21	*36-23
BRANCH V	*32-17	*32-19	*32-25
BRANCH W	*36-20	*36-22	*36-24
BRANCH X	*32-18	*32-20	*32-26

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 24 — Terminal Connections for Reply Bus Bits 1 Through 23 — PUBB Frame

CLEAR EQUIPMENT TROUBLE, PU BUS



FRAME	BITS 1 TO 7	BITS 8 TO 15	BITS 16 TO 23
DIF			
BUS 0	180-053	180-041	180-035
BUS 1	180-201	180-189	180-183

† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 25 — Terminal Connections for Reply Bus Bits 1 Through 23 — DIF Frames

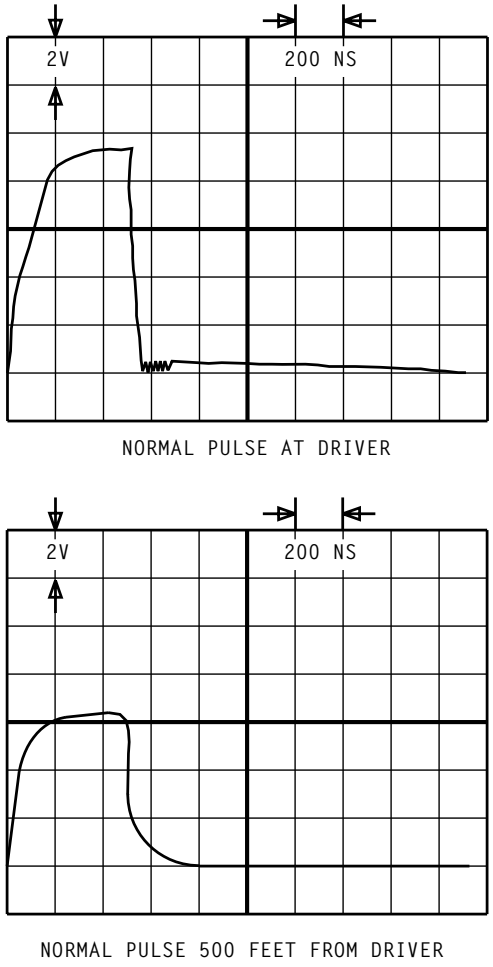


FIG. 26 — Example Waveforms of Normal Pulse at Driver and 500 Feet From Driver for Reply Bus Bits 1 Through 23

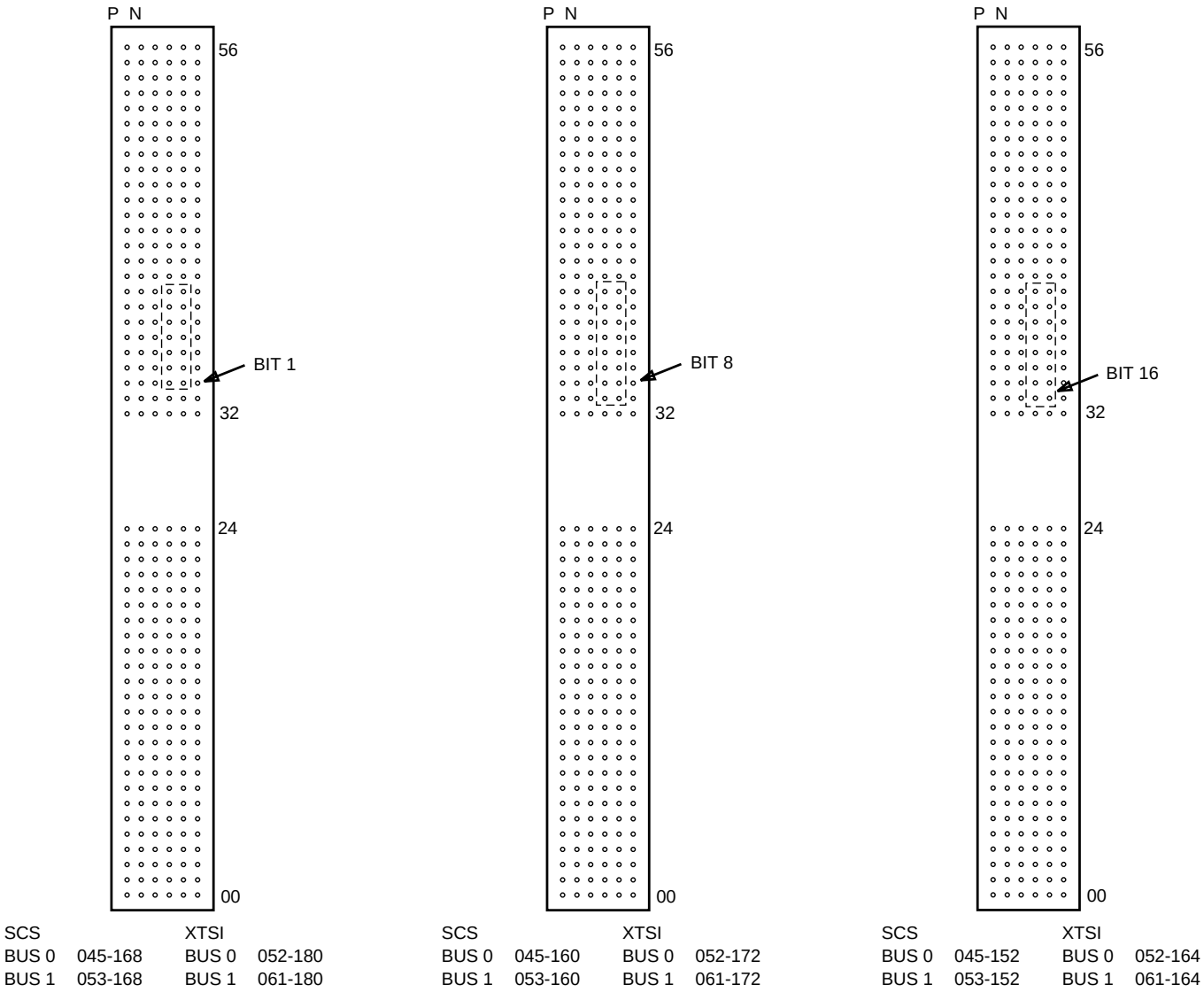
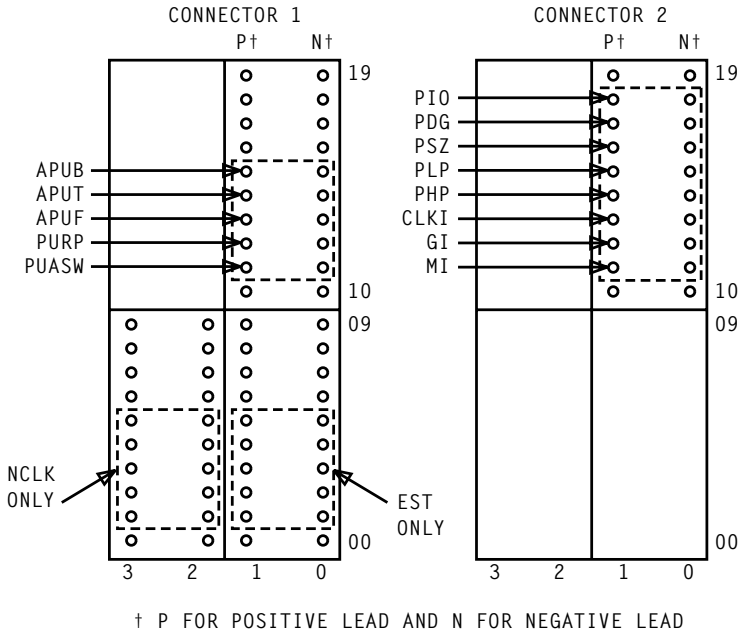


FIG. 27 — Terminal Connections for Reply Bus Bits 1 Through 23 — SCS and XTSI Frames



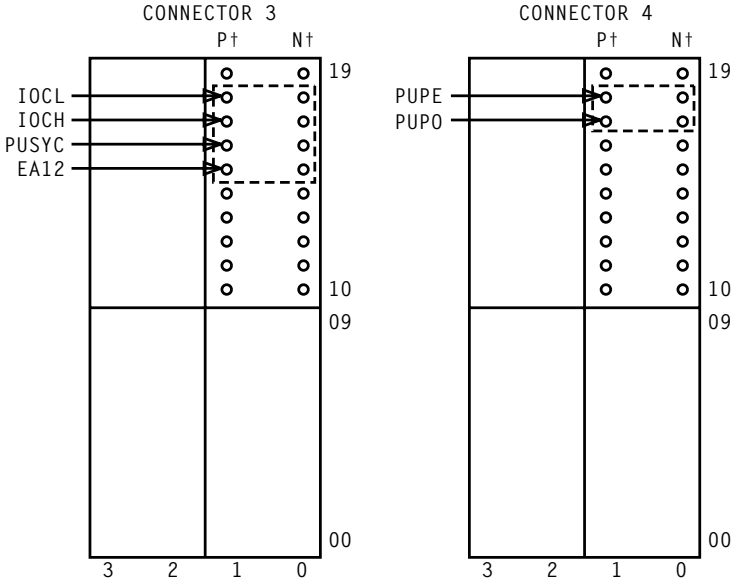
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FRAME	CONNECTOR 1	CONNECTOR 2
CCIS	*80-30	*80-13
EST		
BUS 0	080-02	080-10
BUS 1	080-23	080-31
IO		
BUS 0	080-14	080-10
BUS 1	080-39	080-35
IOP		
BUS 0	080-39	080-29
BUS 1	076-39	076-29
NCLK	*60-48	*60-47
SP 1 (W/O COMBINED MATRIX FR)		
BUS 0	380-01	380-07
BUS 1	480-01	480-07
SP 1 (WITH COMBINED MATRIX FR)		
BUS 0	280-14	280-21
BUS 1	380-14	380-21
SP 2		
BUS 0	180-15	180-21
BUS 1	280-15	280-21
TMS A-1,2	*80-01	*80-07
TMS B		
BUS 0	‡76-14	‡76-21
BUS 1	‡80-14	‡80-21
TSI A-1	*80-33	*80-39
TSI A-2	*80-33	*80-40
TSI B	*80-37	*80-44
VIF		
BUS 0	152-12	152-09
BUS 1	152-22	152-27

* 0 FOR BUS 0 OR 1 FOR BUS 1

‡ 0 FOR PUB TERMINATING AT TMS BAY 0
OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 28 — Terminal Connections for Control Bus and Miscellaneous Bus Bits, Connectors 1 and 2 — CCIS, EST, IO, IOP, NCLK, SP, TMS, TSI, and VIF Frames



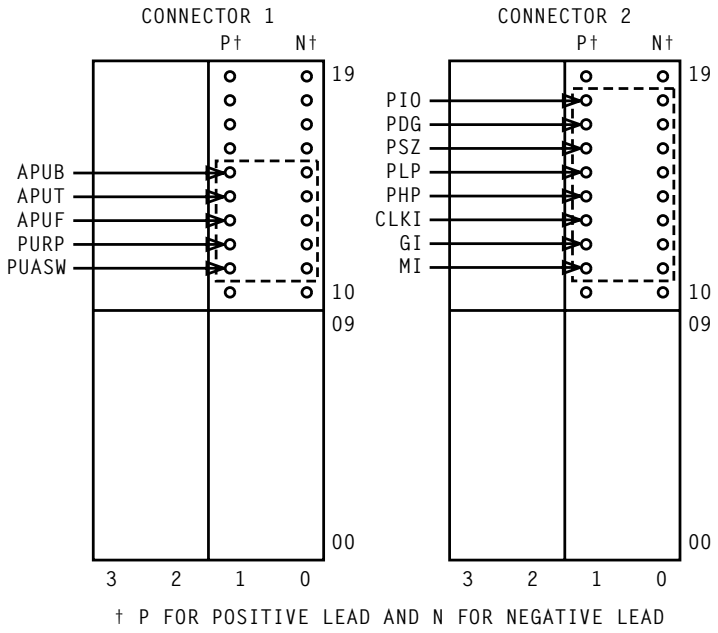
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FRAME	CONNECTOR 3	CONNECTOR 4
CCIS	*80-15	*80-18
EST		
BUS 0	080-11	080-13
BUS 1	080-32	080-34
IO		
BUS 0	080-09	080-07
BUS 1	080-34	080-32
IOP		
BUS 0	080-27	080-37
BUS 1	076-27	076-37
NCLK	*60-34	*60-36
SP 1 (W/O COMBINED MATRIX FR)		
BUS 0	380-08	380-10
BUS 1	480-08	480-10
SP 1 (WITH COMBINED MATRIX FR)		
BUS 0	280-23	280-26
BUS 1	380-23	380-26
SP 2		
BUS 0	180-22	180-24
BUS 1	280-22	280-24
TMS A-1,2	*80-08	*80-10
TMS B		
BUS 0	‡76-23	‡76-26
BUS 1	‡80-23	‡80-26
TSI A-1	*80-40	*80-42
TSI A-2	*80-42	*80-45
TSI B	*80-46	*80-49
VIF		
BUS 0	NONE	NONE
BUS 1	NONE	NONE

* 0 FOR BUS 0 OR 1 FOR BUS 1
‡ 0 FOR PUB TERMINATING AT TMS BAY 0
OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 29 — Terminal Connections for Control Bus and Miscellaneous Bus Bits, Connectors 3 and 4 — CCIS, EST, IO, IOP, NCLK, SP, TMS, TSI, and VIF Frames

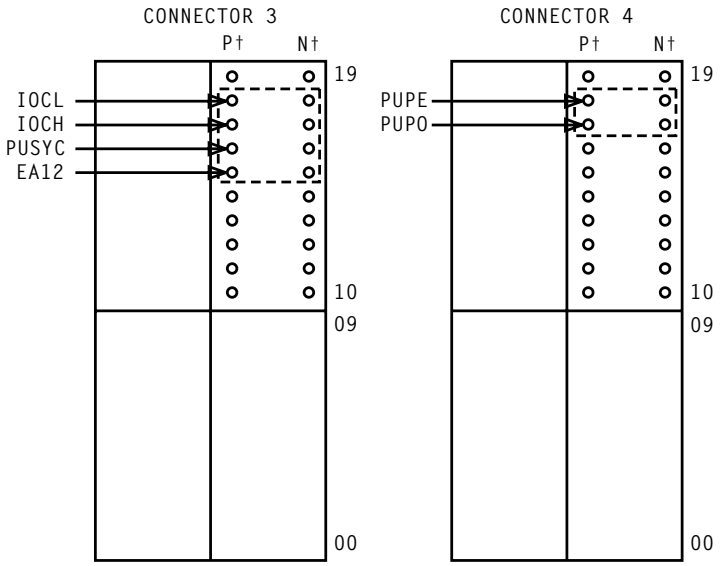
CLEAR EQUIPMENT TROUBLE, PU BUS



PUBB FRAME	CONNECTOR 1	CONNECTOR 2
BRANCH A	*76-25	*76-31
BRANCH B	*72-27	*72-32
BRANCH C	*76-26	*76-33
BRANCH D	*72-28	*72-33
BRANCH E	*64-25	*64-31
BRANCH F	*60-27	*60-32
BRANCH G	*64-26	*64-33
BRANCH H	*60-28	*60-33
BRANCH K	*48-25	*48-31
BRANCH L	*44-27	*44-32
BRANCH M	*48-26	*48-33
BRANCH R	*44-28	*44-33
BRANCH T	*36-25	*36-31
BRANCH V	*32-27	*32-32
BRANCH W	*36-26	*36-33
BRANCH X	*32-28	*32-33

* 0 FOR BUS 0 OR 1 FOR BUS 1

FIG. 30 — Terminal Connections for Control Bus and Miscellaneous Bus Bits, Connectors 1 and 2 — PUBB Frame

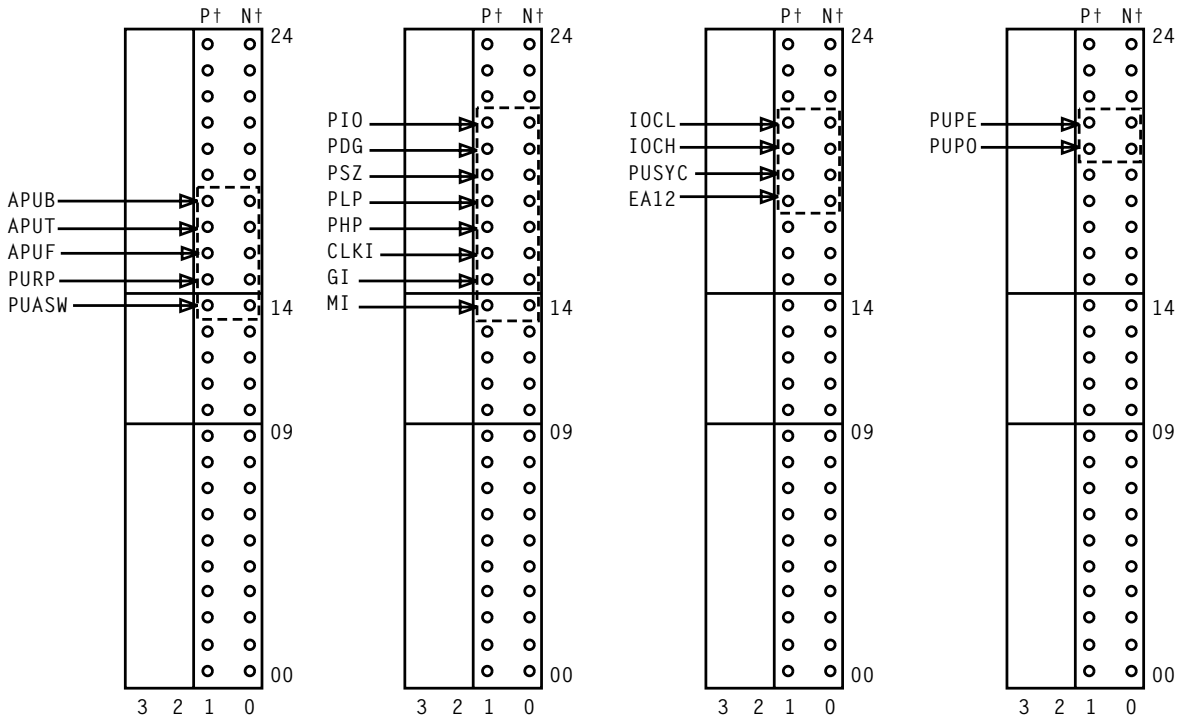


† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

PUBB FRAME	CONNECTOR 3	CONNECTOR 4
BRANCH A	*76-40	*76-09
BRANCH B	*72-38	*72-10
BRANCH C	*76-42	*76-11
BRANCH D	*72-39	*72-11
BRANCH E	*64-40	*64-09
BRANCH F	*60-38	*60-10
BRANCH G	*64-42	*64-11
BRANCH H	*60-39	*60-11
BRANCH K	*48-40	*48-09
BRANCH L	*44-38	*44-10
BRANCH M	*48-42	*48-11
BRANCH R	*44-39	*44-11
BRANCH T	*36-40	*36-09
BRANCH V	*32-38	*32-10
BRANCH W	*36-42	*36-11
BRANCH X	*32-39	*32-11

* 0 FOR BUS 0 OR 1 FOR BUS 1

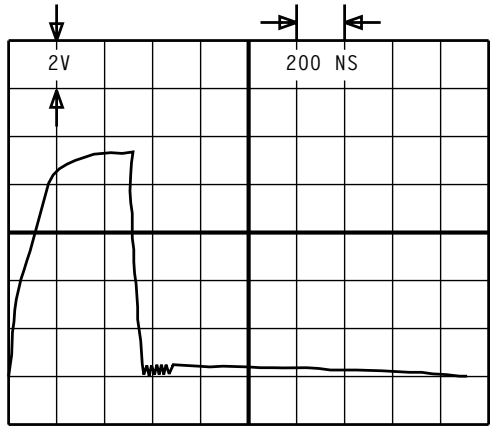
FIG. 31 — Terminal Connection for Control Bus and Miscellaneous Bus Bits, Connectors 3 and 4 — PUBB Frame



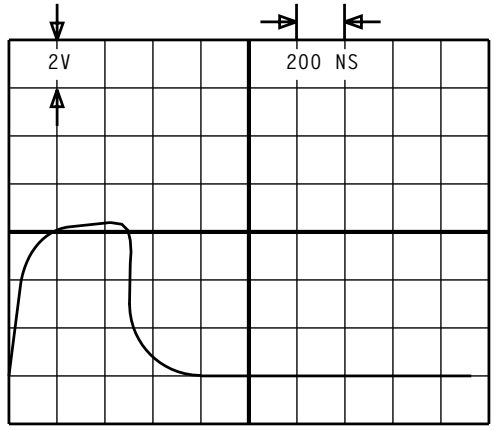
FRAME	CONNECTOR 1	CONNECTOR 2	CONNECTOR 3	CONNECTOR 4
DIF				
BUS 0	180-023	180-067	180-073	180-085
BUS 1	180-171	180-215	180-221	180-233

† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 32 — Terminal Connections for Control Bus and Miscellaneous Bus Bits, Connectors 1, 2, 3, and 4 — DIF Frames



NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 33 — Example Waveforms of Normal Pulse at Driver and 500 Feet From Driver for Control and Miscellaneous Bus Bits — Connectors 1, 2, 3, and 4

CLEAR EQUIPMENT TROUBLE, PU BUS

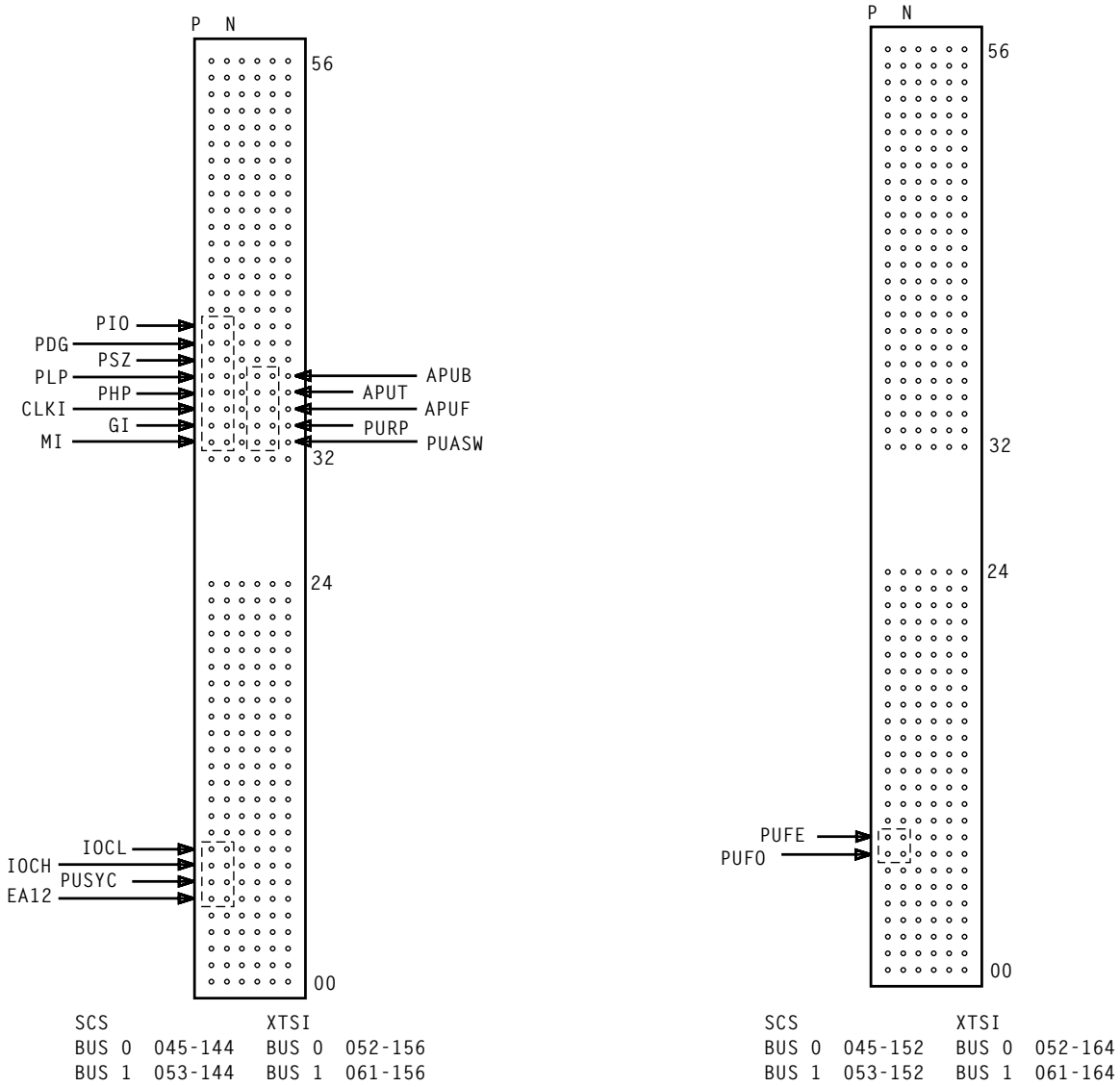
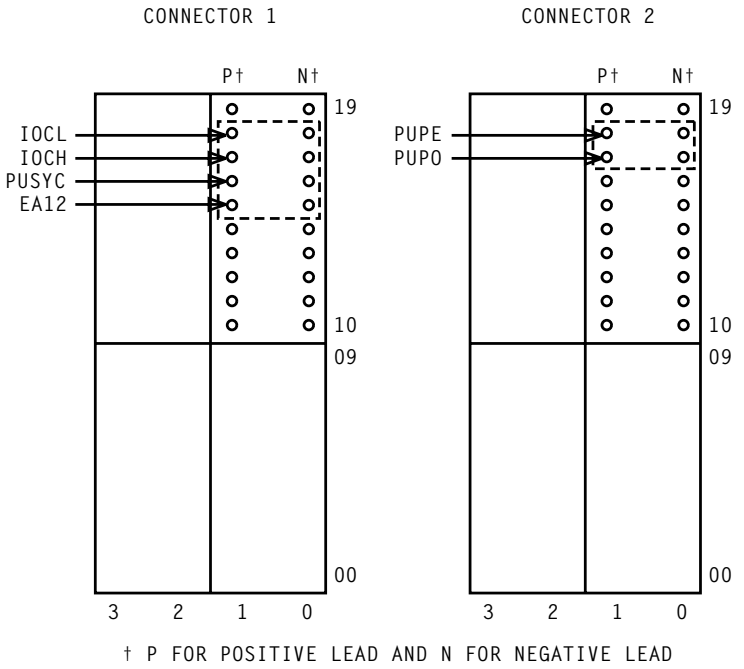


FIG. 34 — Terminal Connections for Control Bus and Miscellaneous Bus Bits — SCS and XTSI Frames



† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

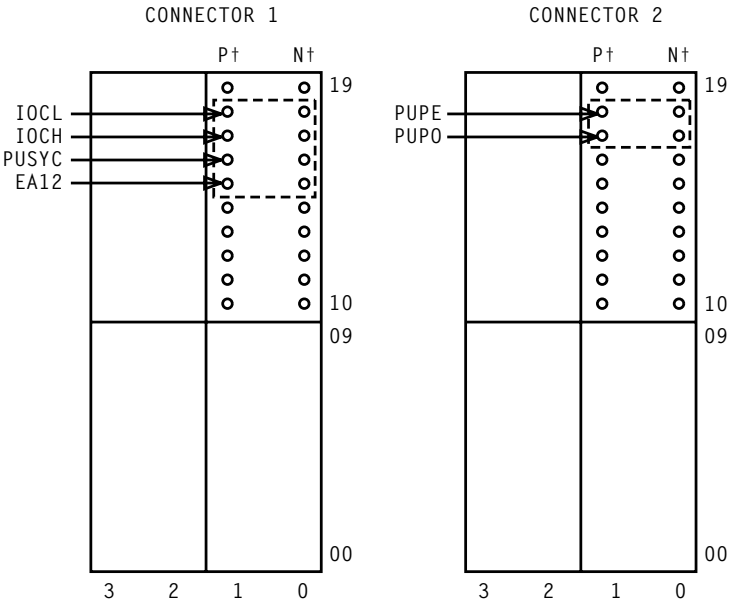
FRAME	CONNECTOR 1	CONNECTOR 2
CCIS	*80-16	*80-15
EST		
BUS 0	080-11	080-13
BUS 1	080-32	080-34
IO		
BUS 0	080-09	080-07
BUS 1	080-34	080-32
IOP		
BUS 0	080-27	080-37
BUS 1	076-27	076-37
NCLK	*60-34	*60-36
SP 1 (W/O COMBINED MATRIX FR)		
BUS 0	380-08	380-10
BUS 1	480-08	480-10
SP 1 (WITH COMBINED MATRIX FR)		
BUS 0	280-23	280-26
BUS 1	380-23	380-26
SP 2		
BUS 0	180-22	180-24
BUS 1	280-22	280-24
TMS A-1,2	*80-08	*80-10
TMS B		
BUS 0	‡76-23	‡76-26
BUS 1	‡80-23	‡80-26
TSI A-1	*80-40	*80-42
TSI A-2	*80-42	*80-45
TSI B	*80-46	*80-49

* 0 FOR BUS 0 OR 1 FOR BUS 1

‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 35 — Terminal Connections for Miscellaneous Bus Bits Not Terminated at VIF Frame, Connectors 1 and 2 — CCIS, EST, IO, IOP, NCLK, SP, TMS, and TSI Frames

CLEAR EQUIPMENT TROUBLE, PU BUS

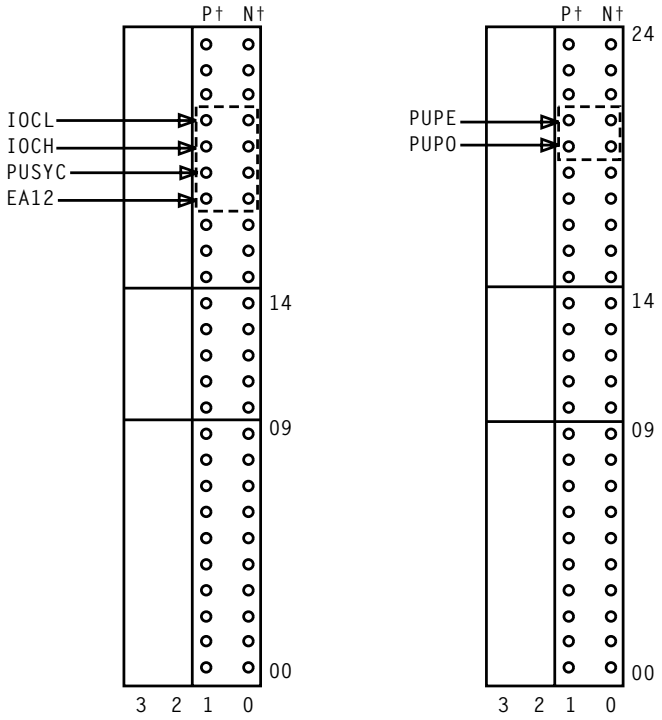


PUBB FRAME	CONNECTOR 1	CONNECTOR 2
BRANCH A	*76-40	*76-09
BRANCH B	*72-38	*72-10
BRANCH C	*76-42	*76-11
BRANCH D	*72-39	*72-11
BRANCH E	*64-40	*64-09
BRANCH F	*60-38	*60-10
BRANCH G	*64-42	*64-11
BRANCH H	*60-39	*60-11
BRANCH K	*48-40	*48-09
BRANCH L	*44-38	*44-10
BRANCH M	*48-42	*48-11
BRANCH R	*44-39	*44-11
BRANCH T	*36-40	*36-09
BRANCH V	*32-38	*32-10
BRANCH W	*36-42	*36-11
BRANCH X	*32-39	*32-11

* 0 FOR BUS 0 OR 1 FOR BUS 1

FIG. 36 — Terminal Connections for Miscellaneous Bus Bits Not Terminated at VIF Frame, Connectors 1 and 2 — PUBB Frame

CLEAR EQUIPMENT TROUBLE, PU BUS



FRAME	CONNECTOR 1	CONNECTOR 2
DIF		
BUS 0	180-073	180-085
BUS 1	180-221	180-233

† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 37 — Terminal Connections for Miscellaneous Bus Bits Not Terminated at VIF Frame, Connectors 1 and 2 — DIF Frames

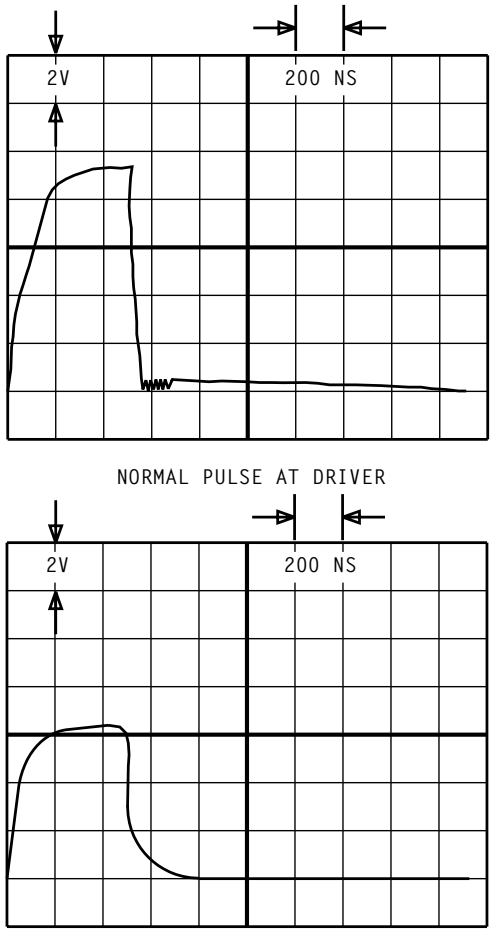
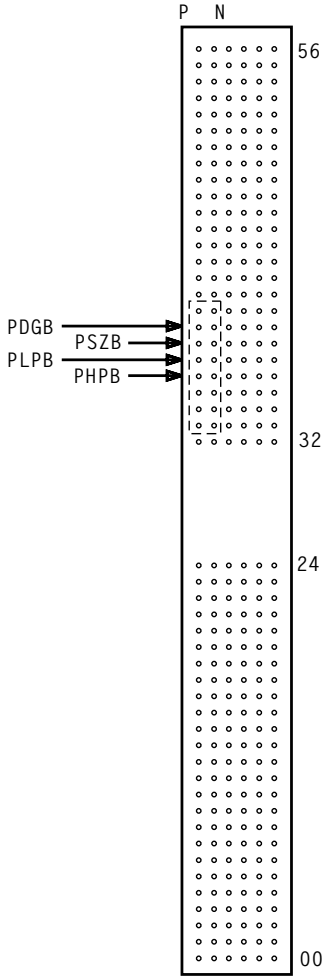
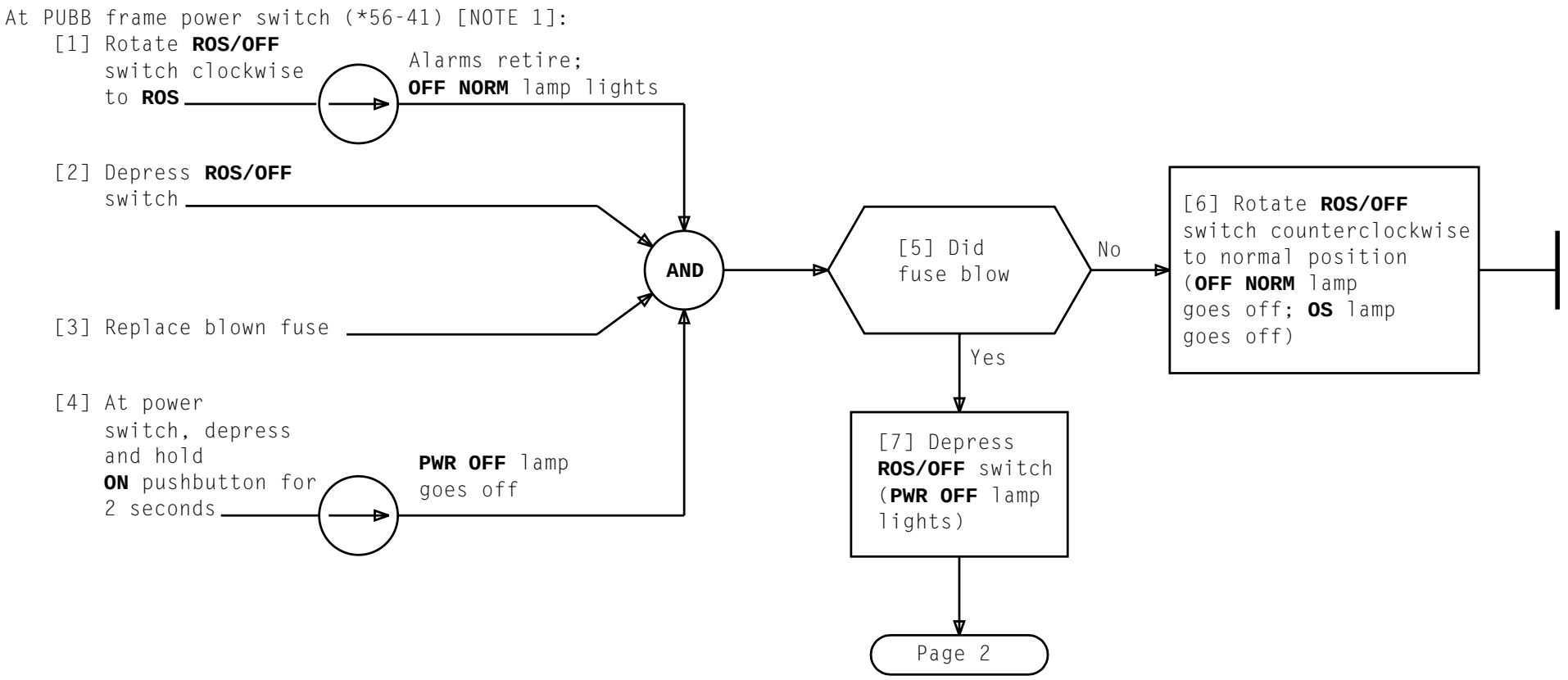


FIG. 38 — Example Waveforms of Normal Pulse at Driver and 500 Feet from Driver for Miscellaneous Bus Bits Not Terminated at VIF Frame



SCS		XTSI	
BUS 0	045-144	BUS 0	052-156
BUS 1	053-144	BUS 1	061-156

FIG. 39 — Terminal Connection for Expanded Pollable Bits at Peripheral Frame for SCS and XTSI Frames



NOTE 1
* = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)

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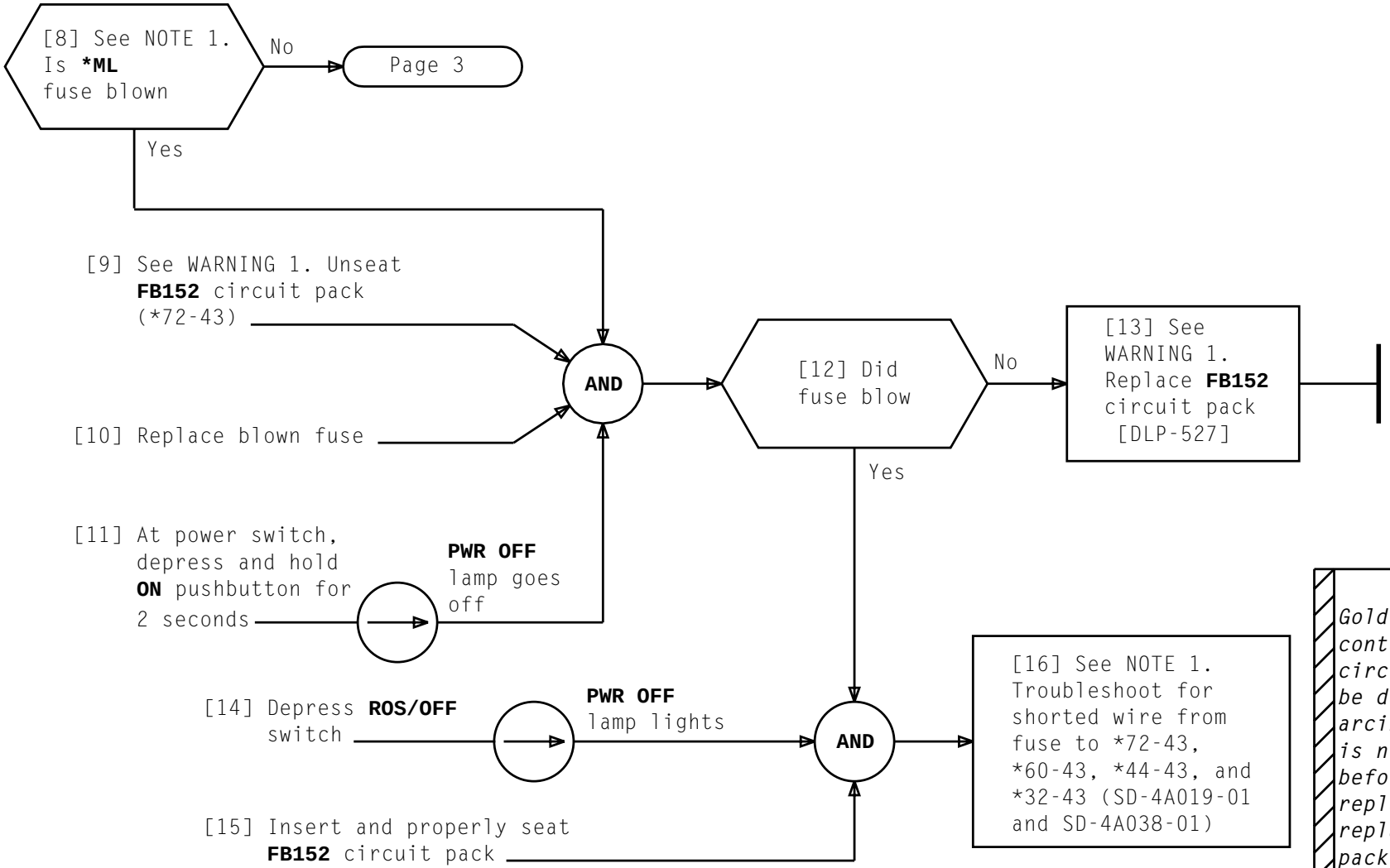
CLEAR PUBB AND LOOP-AROUND UNIT (J4A005AA-1) BLOWN FUSE TROUBLE



WARNING 1

Gold-plated contacts on **FB152** *circuit pack may be damaged by arcing if* ***ML*** *fuse is not removed before and replaced after replacing circuit pack (* = PUBB bay [0 or 1] or if utilized, repeater frame number [1 through 4])*

CLEAR PUBB AND LOOP-AROUND UNIT (J4A005AA-1) BLOWN FUSE TROUBLE

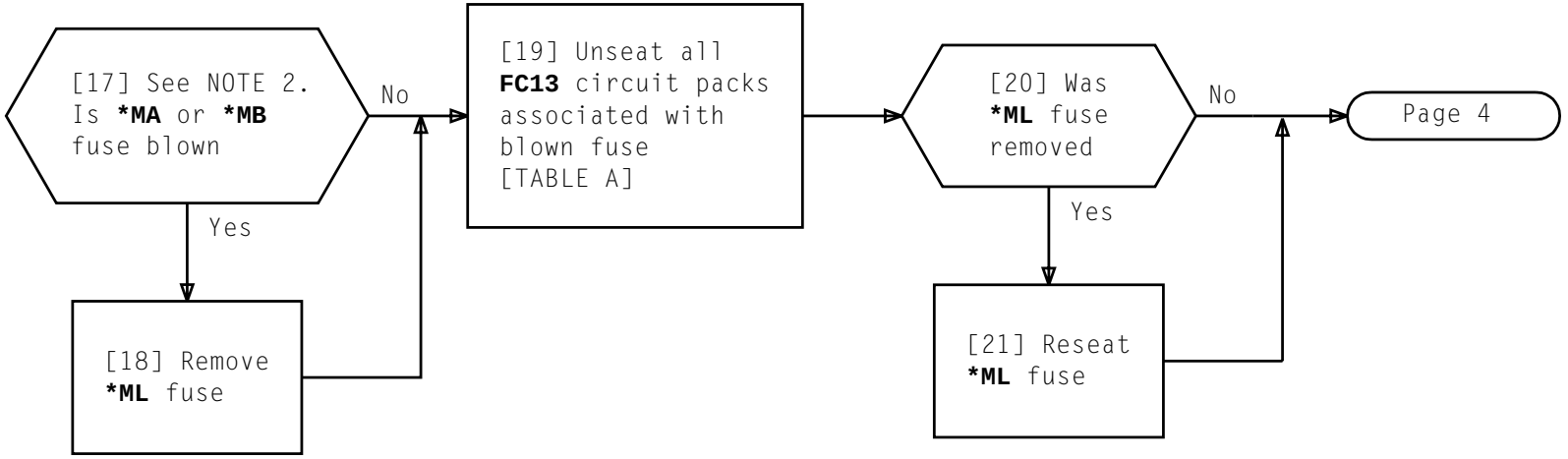
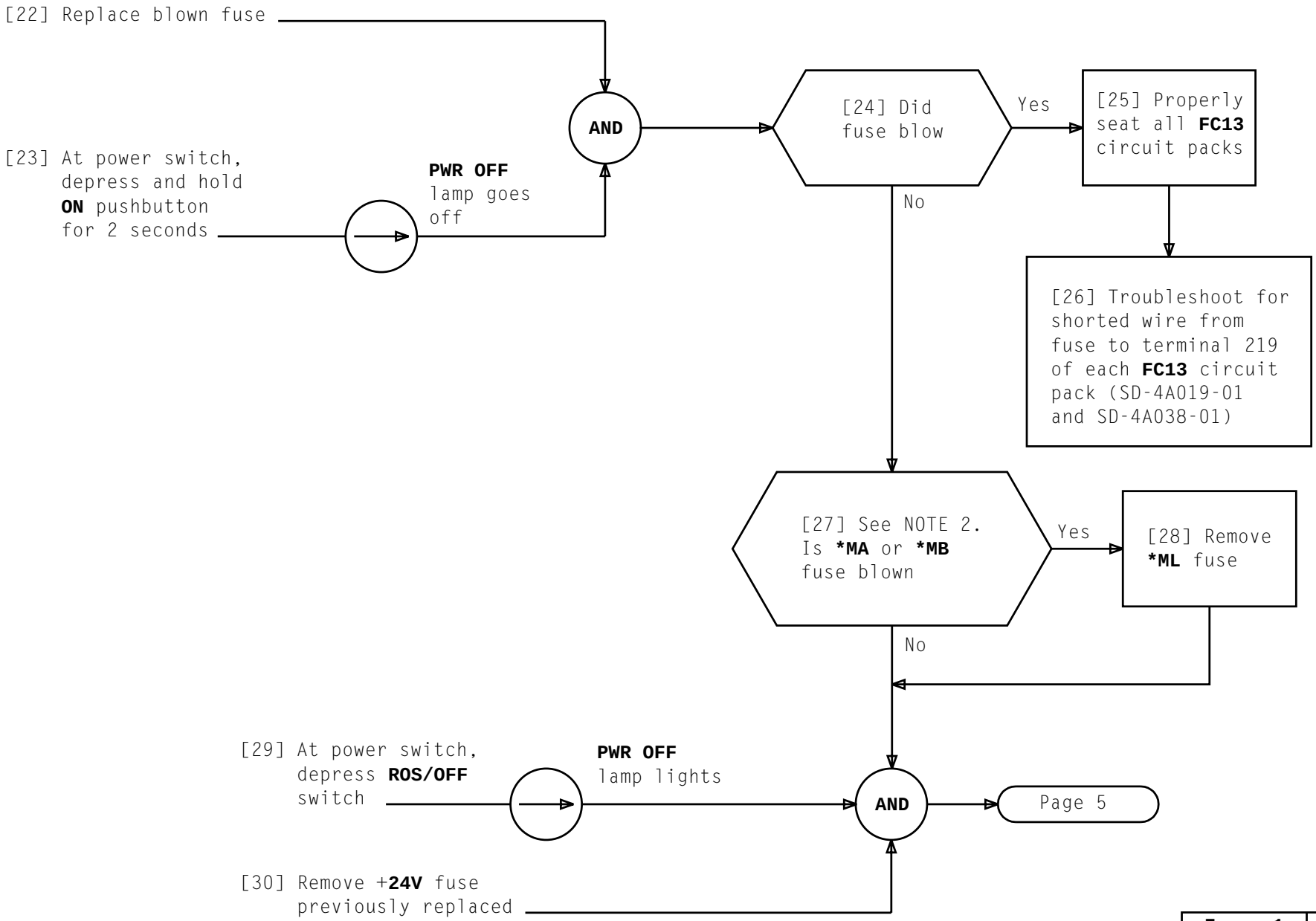


TABLE A
LOCATION OF FC13

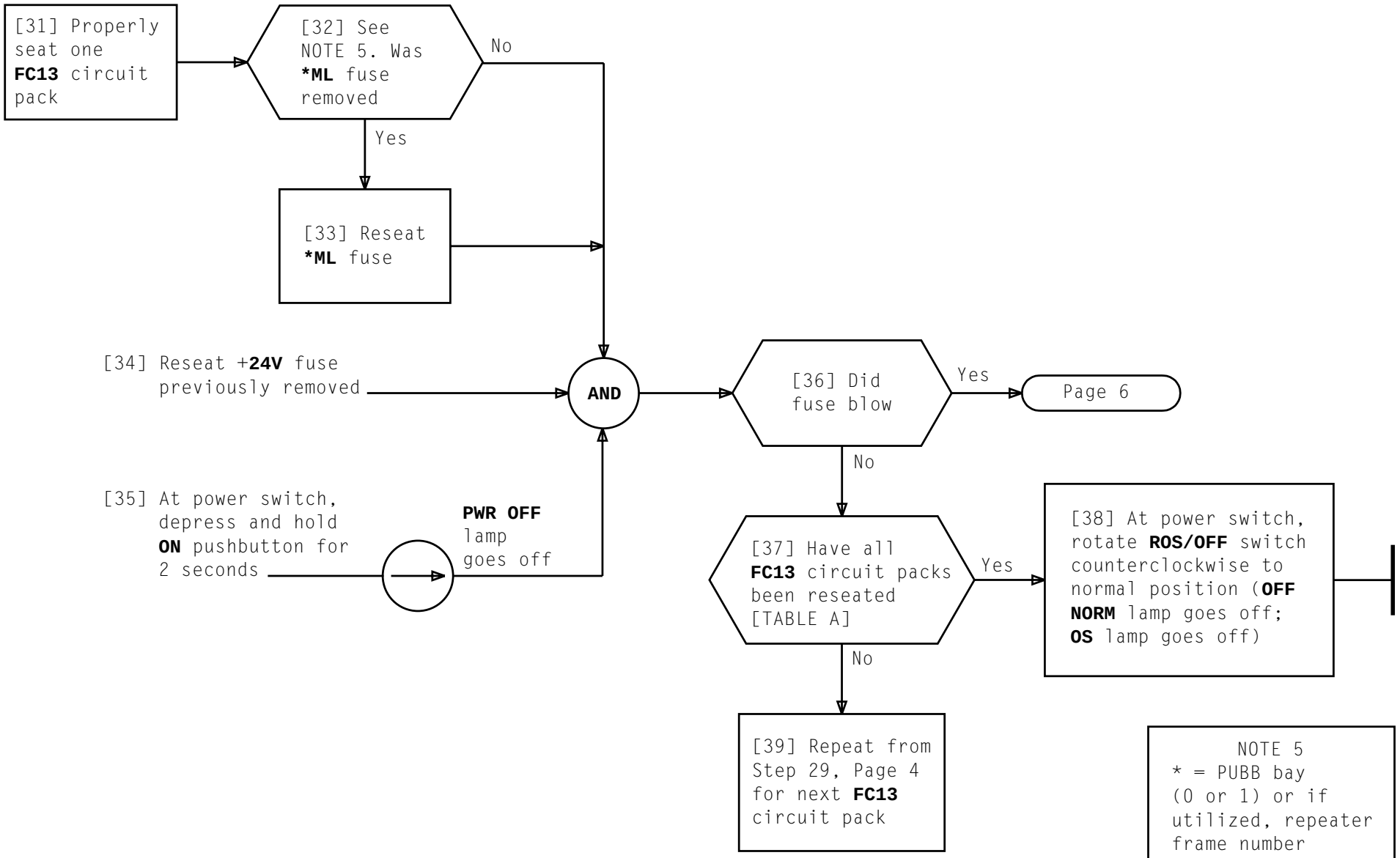
BLOWN FUSE	VERTICAL POSITION [NOTES 2 AND 3]	HORIZONTAL POSITION [NOTE 4]
***MA, *MC, *ME,** or ***MG**	*80, *68, *52, *40	25 and 26
	*76, *64, *48, *36	31, (33), 34, (36), 37, (39), 40, (42)
	*72, *60, *44, *32	25, (26), 27, (28)
***MB, *MD, *MF,** or ***MH**	*80, *68, *52, *40	20 and 21
	*76, *64, *48, *36	03, (05), 06, (08), 09, (11), 12, (14)
	*72, *60, *44, *32	17, (18), 19, (20)

NOTES
2. * = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)
3. PUBB frame may be equipped with two, four, six, or eight peripheral unit bus branching and loop-around units
4. Circled horizontal positions of **FC13** circuit packs are optional bus branches

CLEAR PUBB AND LOOP-AROUND UNIT (J4A005AA-1) BLOWN FUSE TROUBLE

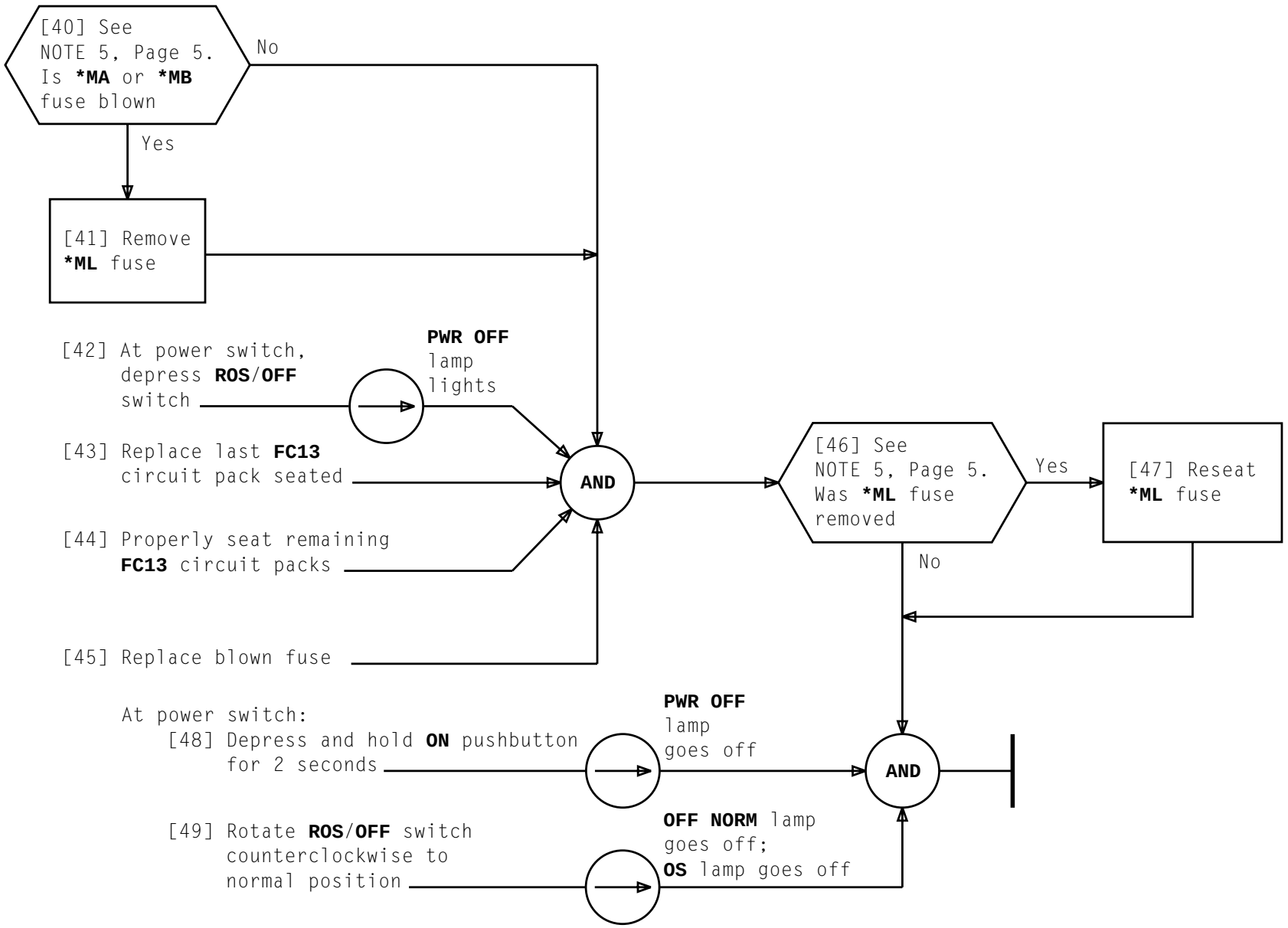


CLEAR PUBB AND LOOP-AROUND UNIT (J4A005AA-1) BLOWN FUSE TROUBLE



NOTE 5
* = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)

CLEAR PUBB AND LOOP-AROUND UNIT (J4A005AA-1) BLOWN FUSE TROUBLE



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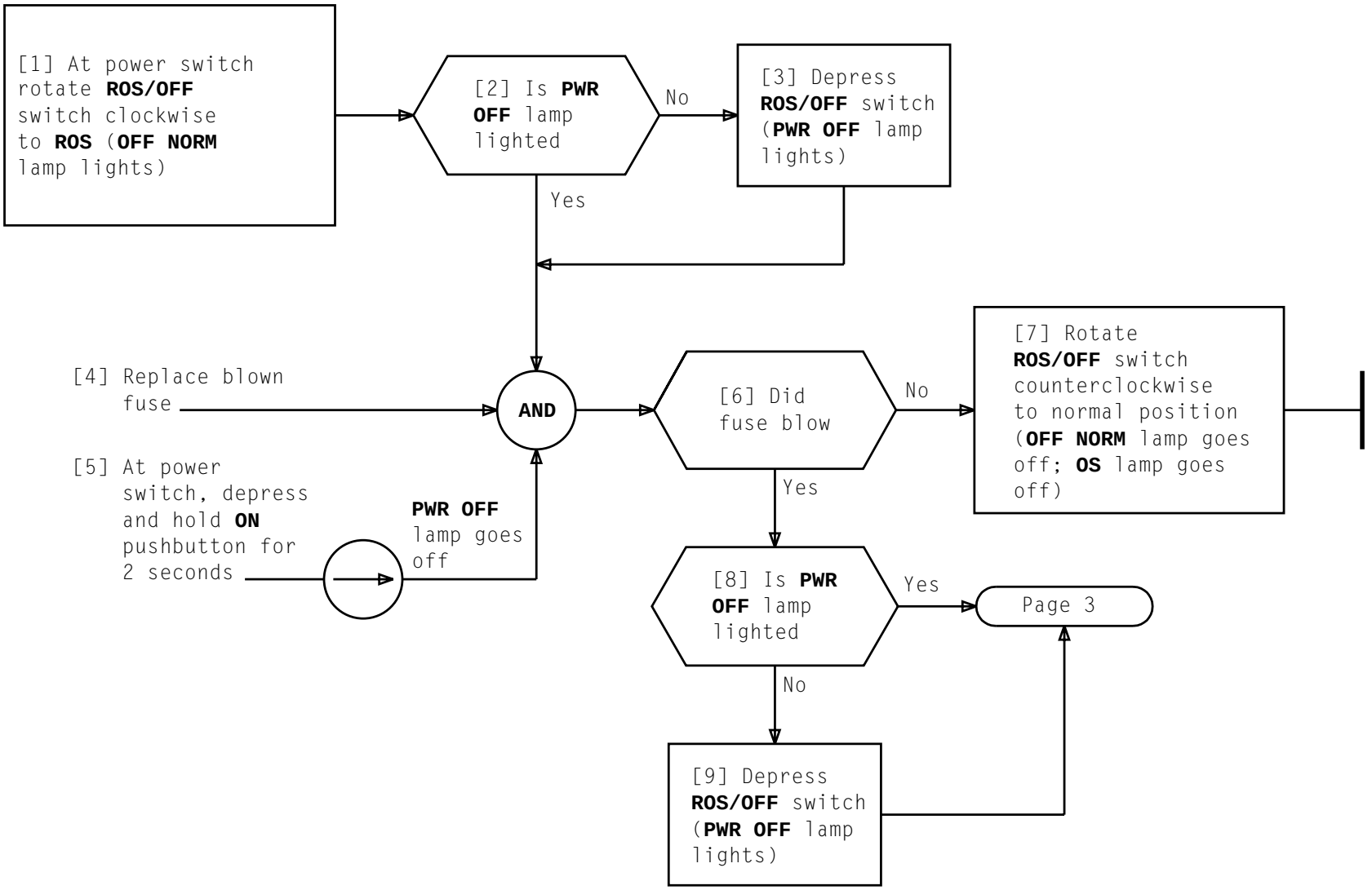
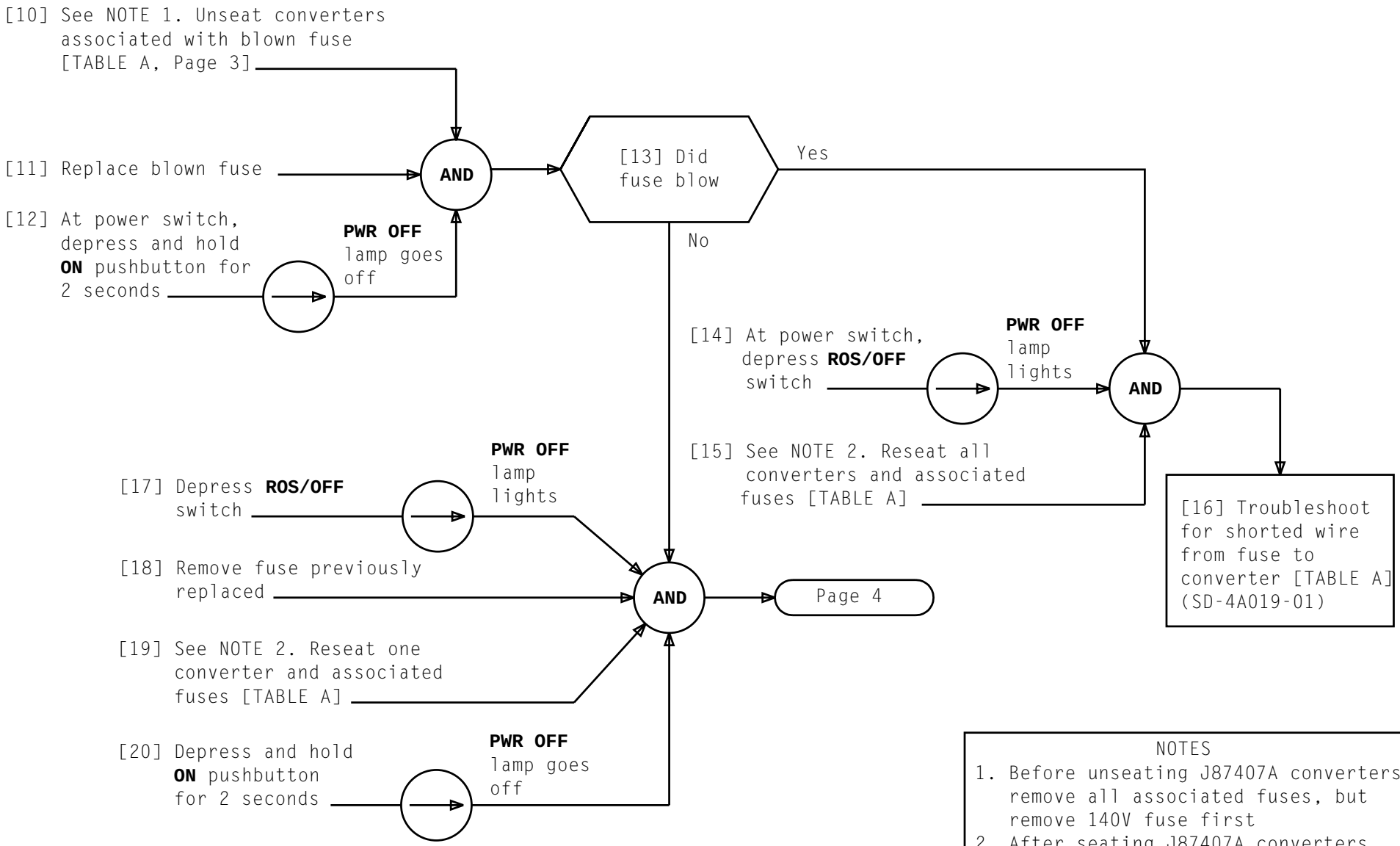
CLEAR PUBB AND LOOP-AROUND UNIT (J4A005AA-1) BLOWN FUSE TROUBLE



CLEAR DC-TO-DC CONVERTER (J87407A) BLOWN FUSE TROUBLE



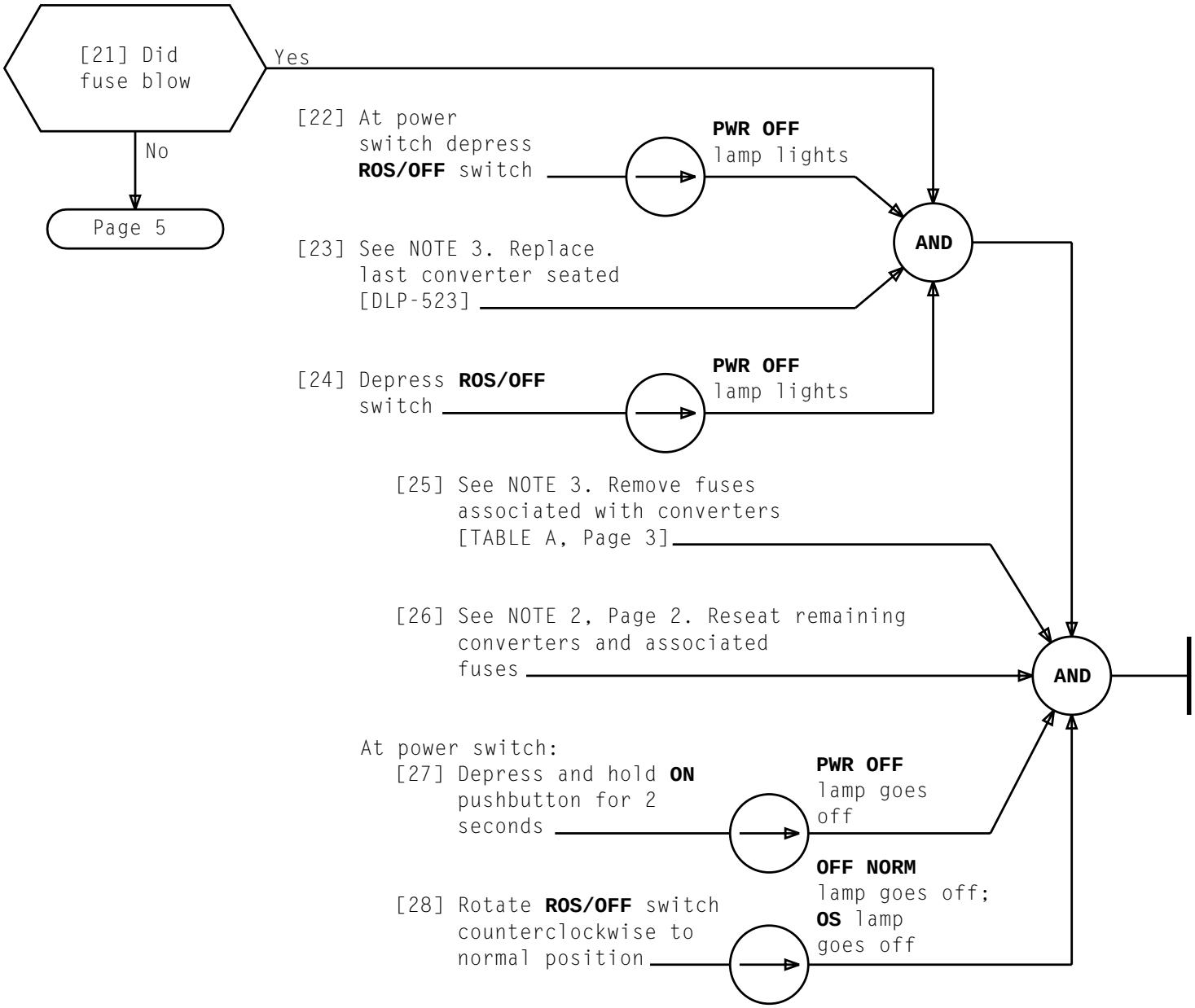
NOTES

1. Before unseating J87407A converters, remove all associated fuses, but remove 140V fuse first
2. After seating J87407A converters, reseat all associated fuses, but reseat 140V fuses last

CLEAR DC-TO-DC CONVERTER (J87407A) BLOWN FUSE TROUBLE

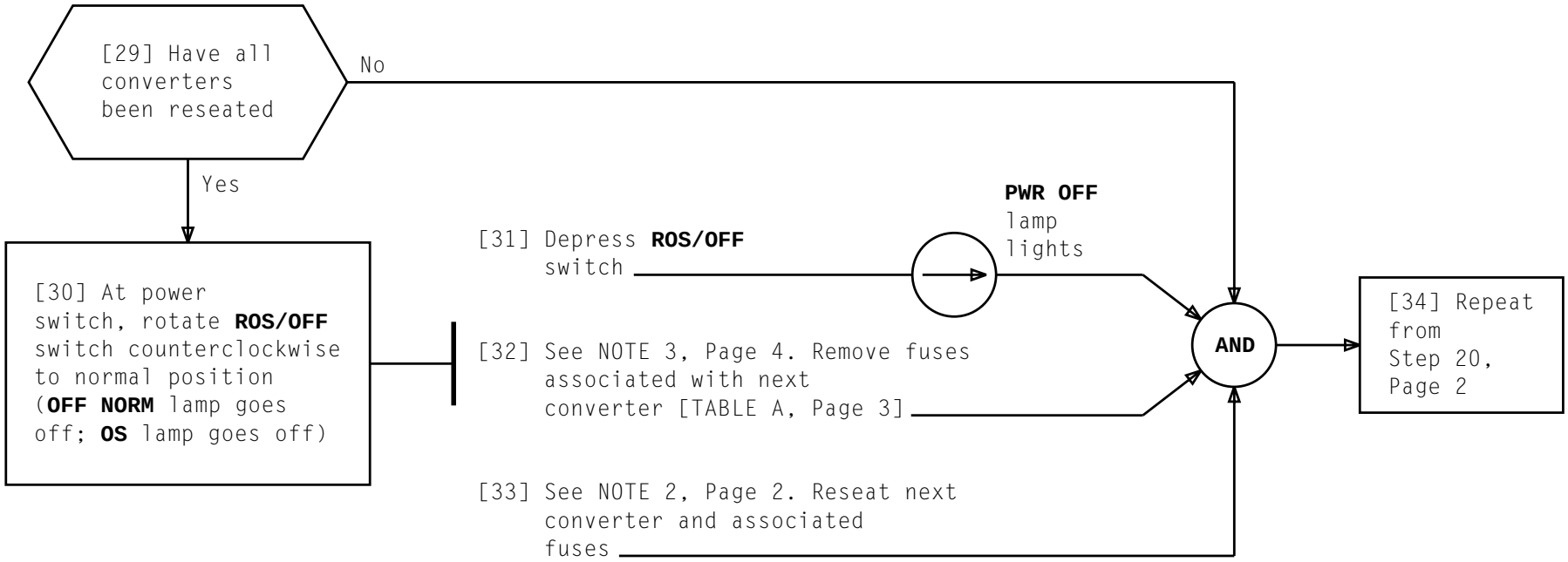
TABLE A				
FUSES			CONVERTER	
+24V DESIGN/LOC	+24V DESIGN/LOC	+140V DESIGN/LOC	LOCATION	DESIGN
*CA *07-25 (3/4 AMP)	*BA *07-25 (1-1/3 AMP)	*AA *07-04 (1-1/3 AMP)	*17-00	CV*00
			*17-03	CV*01
			*17-06	CV*02
		*AB *07-04 (1-1/3 AMP)	*12-00	CV*03
			*12-03	CV*04
			*12-06	CV*05
	*BB *07-25 (1-1/3 AMP)	*AC *07-04 (1-1/3 AMP)	*17-12	CV*06
			*17-15	CV*07
			*17-18	CV*08
		*AD *07-04 (1-1/3 AMP)	*12-12	CV*09
			*12-15	CV*10
			*12-18	CV*11
* = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)				

CLEAR DC-TO-DC CONVERTER (J87407A) BLOWN FUSE TROUBLE

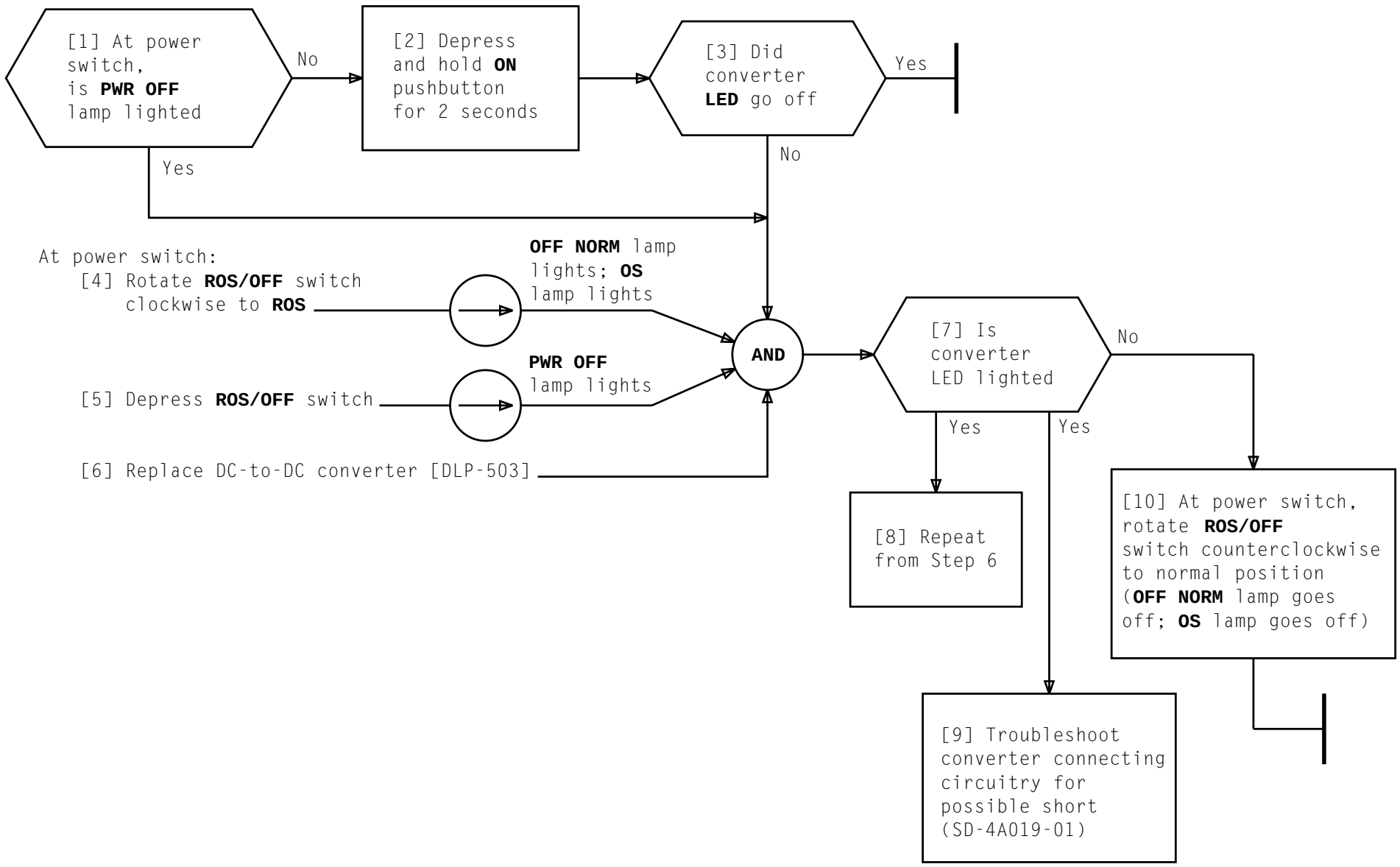


CLEAR DC-TO-DC CONVERTER (J87407A) BLOWN FUSE TROUBLE

NOTE 3
When removing and reseating fuses associated with J87407A converters, remove 140V fuse first, and reseat 140V fuse last



CLEAR DC-TO-DC CONVERTER (J87407A) BLOWN FUSE TROUBLE



CLEAR DC-TO-DC CONVERTER (J87407A) LED LIGHTED TROUBLE

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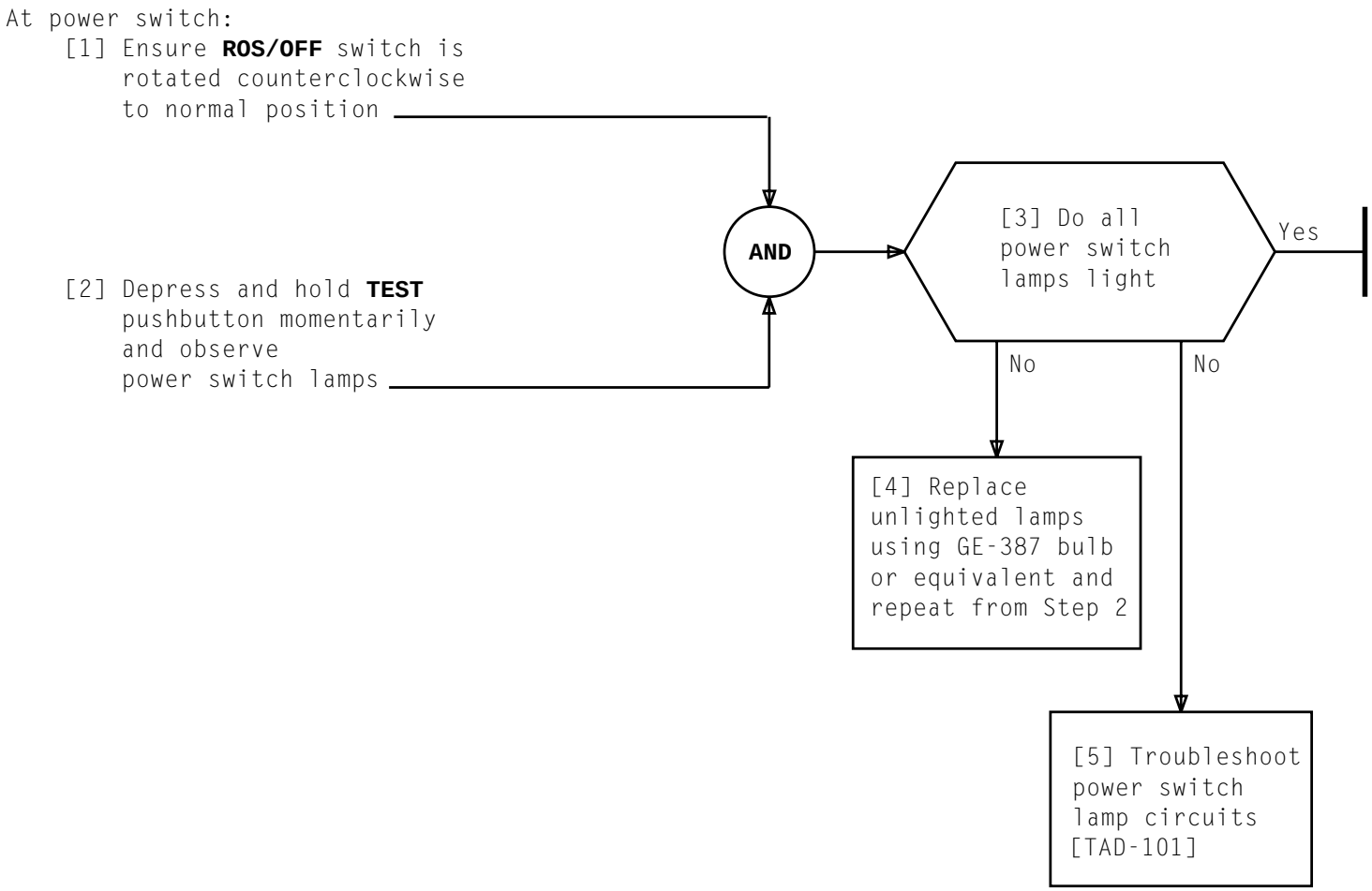


TEST PUBB FRAME POWER SWITCH LAMPS

[1] At 1B Processor MTC terminal, enter message:
RMV:PUB a!
a = bus to be removed (0 or 1)

System responds
RMV:PUB a COMPLETED

At power switch:

[2] Rotate **ROS/OFF** switch clockwise to **ROS**

OFF NORM lamp lights;
OS lamp lights

[3] Depress **ROS/OFF** switch

PWR OFF lamp lights

[4] Remove power switch fuses [TABLE A]

[5] Cover apparatus below switch with clean drop cloth

[6] See NOTE 1. Tag and remove frame wiring on rear of power switch

[7] Remove four mounting screws and withdraw switch from front of frame

AND

Switch removed

Page 2

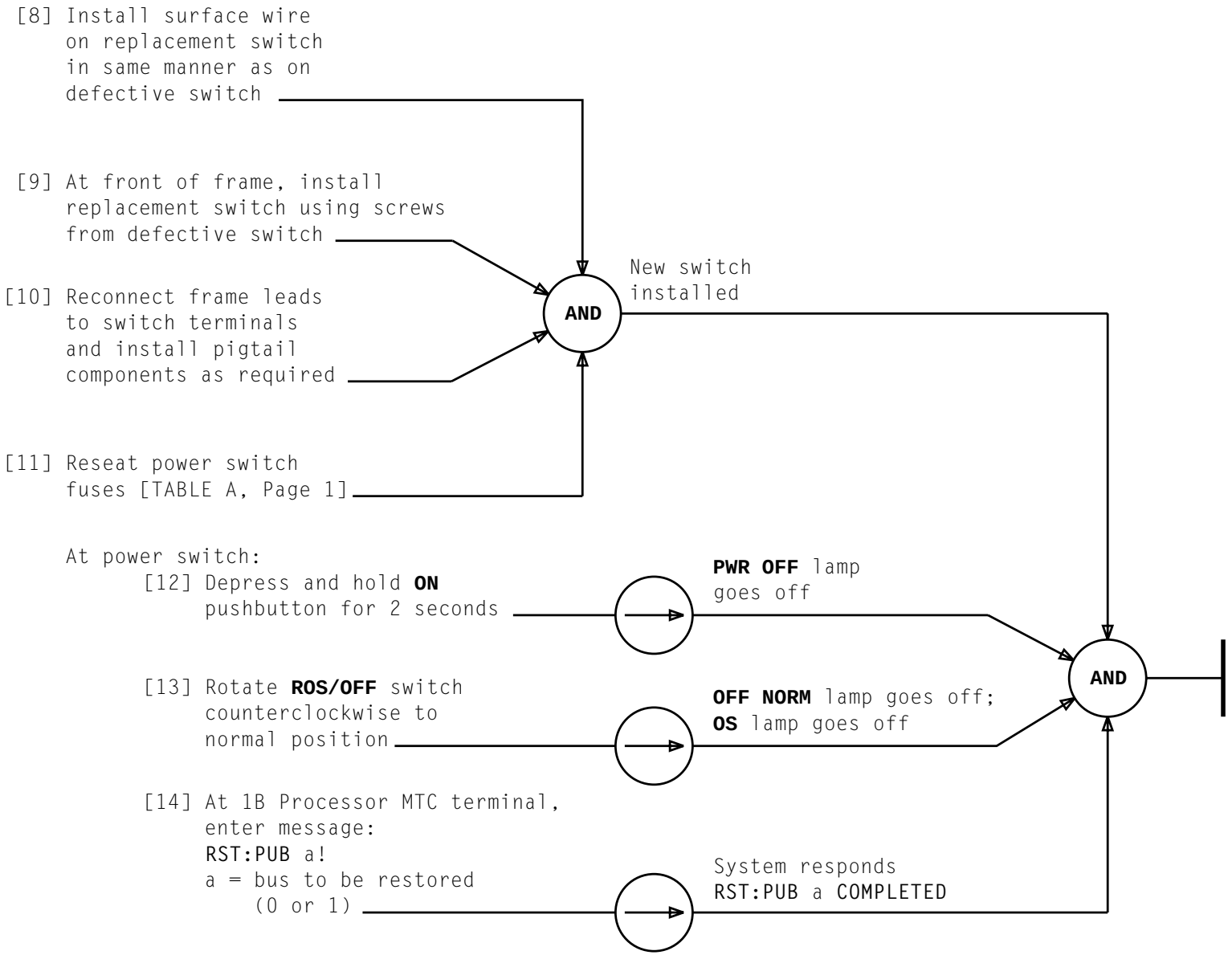
TABLE A

FUSE DESIGNATION	FUSE LOCATION	RATED AMPERES	FUSE CODE
***MJ**	*07-18	3/4A	70H
***MK**	*07-25	1 1/3A	70A
***MM**	*07-18	1 1/3A	70A

* = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)

NOTE 1
Do not remove surface wiring on switch terminals. It will be used as guide to surface wire replacement switch

REPLACE POWER SWITCH, PUBB FRAME



REPLACE POWER SWITCH, PUBB FRAME

1. Get program listings PR-4A510 (PUDGPBGR) and PR-4A512 (PUDGPB02) (See FIG. 1)

2. Using PR-4A512, verify address of ITEM 1 in TABLE A

3. Using PR-4A510, verify address of ITEMS 2 through 6 in TABLE A

TABLE A		
ITEM	**STATEMENT LABEL**	**ADDRESS**
1	STM10600	543
2	PBTS2600	200
3	PBTS2900	207
4	PBTS3600	246
5	PBTS4400	616
6	PBTS13800	1675

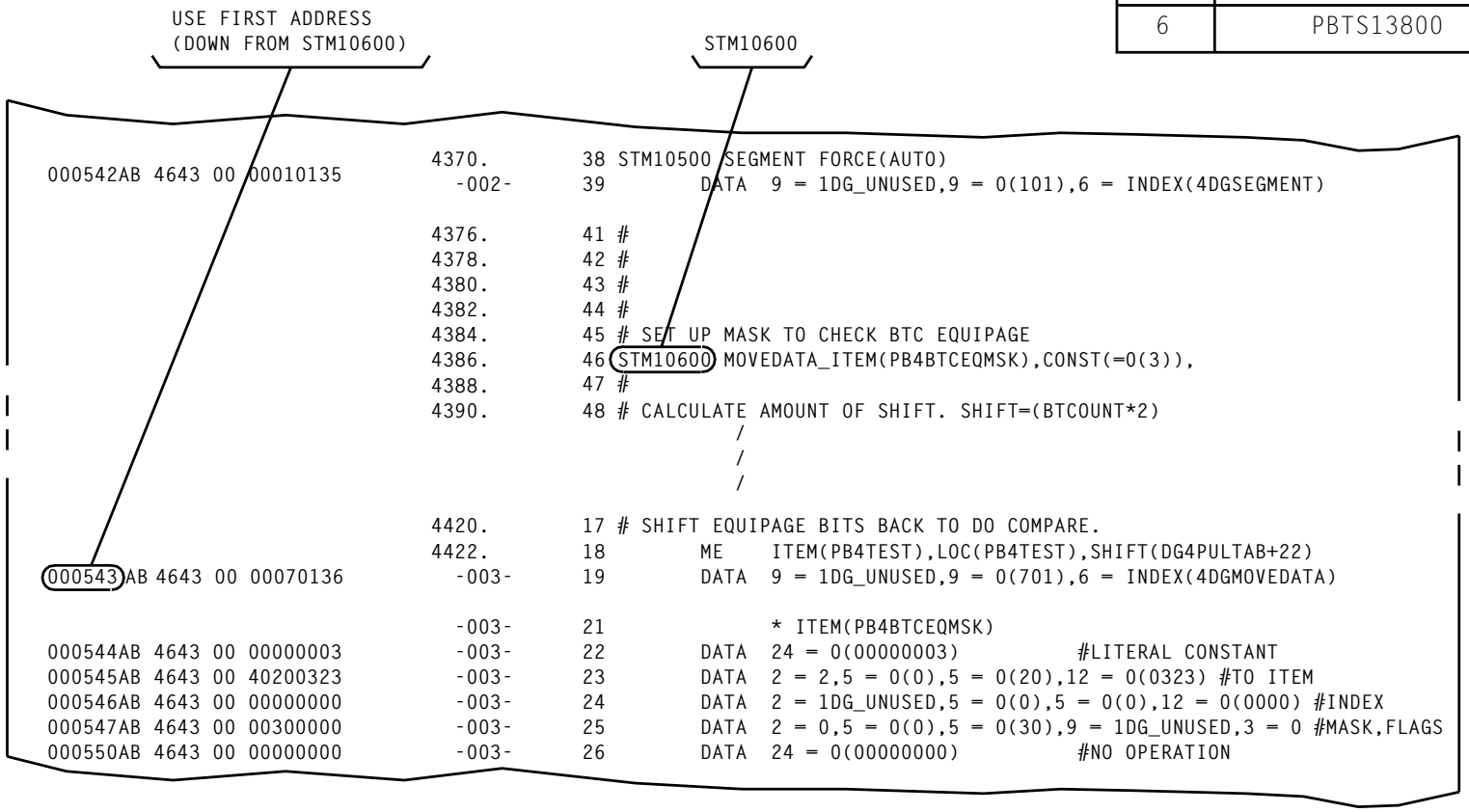


FIG. 1 — Location of STM10600 and Address to Use

STORE INPUT MESSAGES ON 1B PROCESSOR SREC OR BELTLINE TERMINAL FOR PUB LOOPING TEST

At 1B Processor SREC or Beltline terminal:

4. Depress **FORM ENTER** key to ON

   CAUTION: The messages must not be entered into system at this time

5. Type input messages per TABLE B

6. Depress **FORM ENTER** key to OFF

End of procedure

TABLE B

NUMBER	INPUT MESSAGE
1	EX:PUB a;START! a = Bus 0 or 1
2	EX:PUB a:PH 2,ADR 543! a = Bus 0 or 1 543 = Address of statement label STM10600
3	EX:PUB a;STEP ! a = Bus 0 or 1
4	EX:PUB a:ADR 200-207! a = Bus 0 or 1 200 = Address of statement label PBTS2600 207 = Address of statement label PBTS2900
5	EX:PUB a! a = Bus 0 or 1
6	EX:PUB a:ADR 207-246! a = Bus 0 or 1 207 = Address of statement label PBTS2900 246 = Address of statement label PBTS3600
7	EX:PUB a:ADR 616-1675! a = Bus 0 or 1 616 = Address of statement label PBTS4400 1675 = Address of statement label PBTS13800
8	EX:PUB a:ADR 543! a = Bus 0 or 1 543 = Address of statement label STM10600
9	OP:MACLI,CLASS MTCE!
10	STOP:MACLI,CLASS MTCE,SUBCLASS a! a = CLASS MTCE SUBCLASS number from output message assigned to PUB diagnostic*

*To obtain CLASS MTCE SUBCLASS number, type and send OP:MACLI,CLASS MTCE!. From system TTY response, determine which maintenance subclass number is associated with PUB and use that number for "a" for NUMBER 10 message

STORE INPUT MESSAGES ON 1B PROCESSOR SREC OR BELTLINE TERMINAL FOR PUB LOOPING TEST

[1] Office has

3B21D APS → Page 3

3B20 Model 1 APS → Page 3

3B20D Model 2/3 APS

[2] At control panel, if **ON LINE** LED on, touch **RESET** switch

ON LINE LED off

[3] On tape unit control panel, depress **UNLOAD** switch

Tape rewinds onto supply reel

[4] Open tape unit dust cover

[5] On supply (upper) reel hub, depress latch release button and remove reel [FIG. 1]

[6] Close tape unit dust cover

[7] If no tapes are to be mounted, on tape unit control panel depress **LOGIC OFF** switch

AND

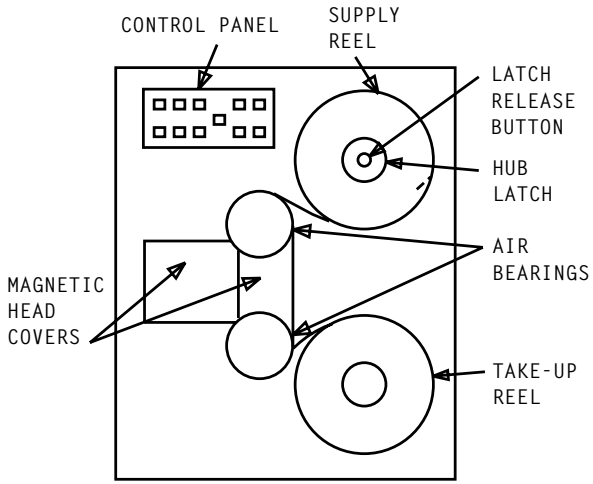


FIG. 1 — APS Keystone Tape Unit

DEMOUNT 1600 BPI/4mm TAPE ON ATTACHED PROCESSOR SYSTEM (APS) TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

[8] On tape unit control panel, is **ON LINE** LED lighted [FIG. 1]

Yes

[9] On tape unit control panel, depress **ON LINE** switch
Response: **ON LINE** LED goes off

No

[10] On tape unit control panel, depress **REWIND** switch

LOAD POINT LED lights

Tape rewinds to end of tape and stops

[11] On tape unit control panel, depress **REWIND** switch

AND

[12] Open tape unit dust cover

[13] Rotate supply (upper) reel hub knob counterclockwise until all of tape is rewound

[14] On supply (upper) reel hub, raise hub tab and remove tape reel [FIG. 2]

AND

[15] Return hub tab to locked (down) position

[16] Close tape unit dust cover

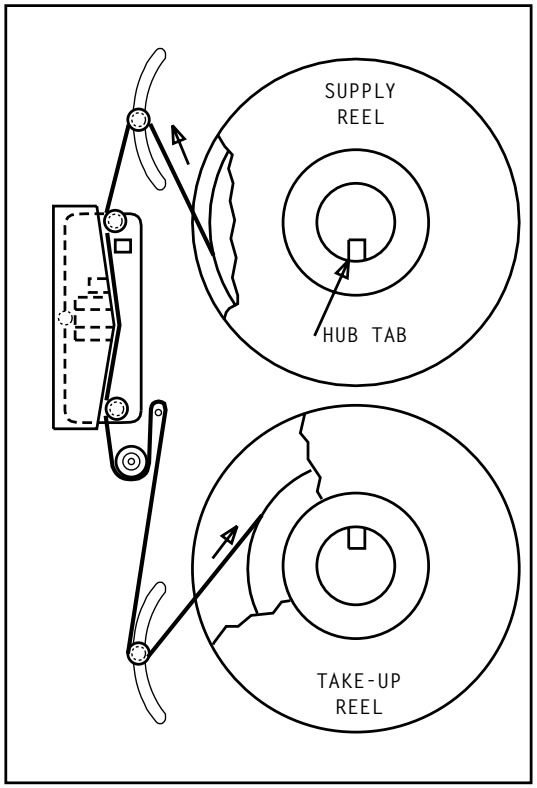


FIG. 2 — APS Kennedy Tape Unit

DEMOUNT 1600 BPI/4mm TAPE ON ATTACHED PROCESSOR SYSTEM (APS) TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

[17] At digital audio tape (DAT) unit that contains tape to be removed, depress eject button [FIG. 3]

[18] Was tape just written

No

Yes

[19] Put write-protect tab in the down (locked) position [FIG. 4]

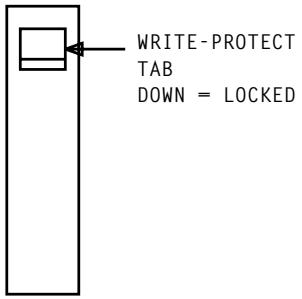


FIG. 4 — 4-mm Tape

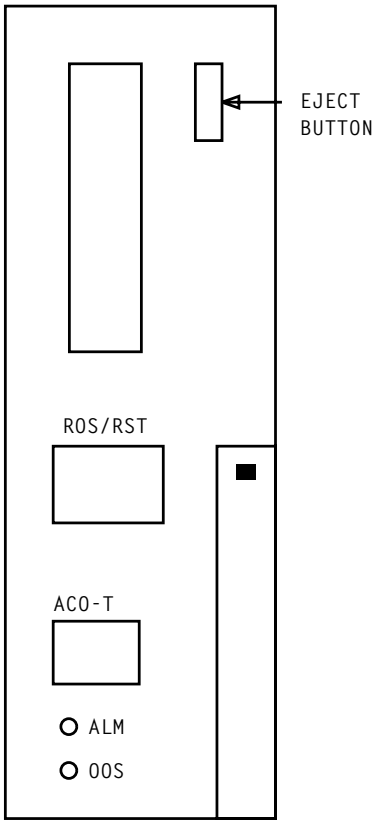
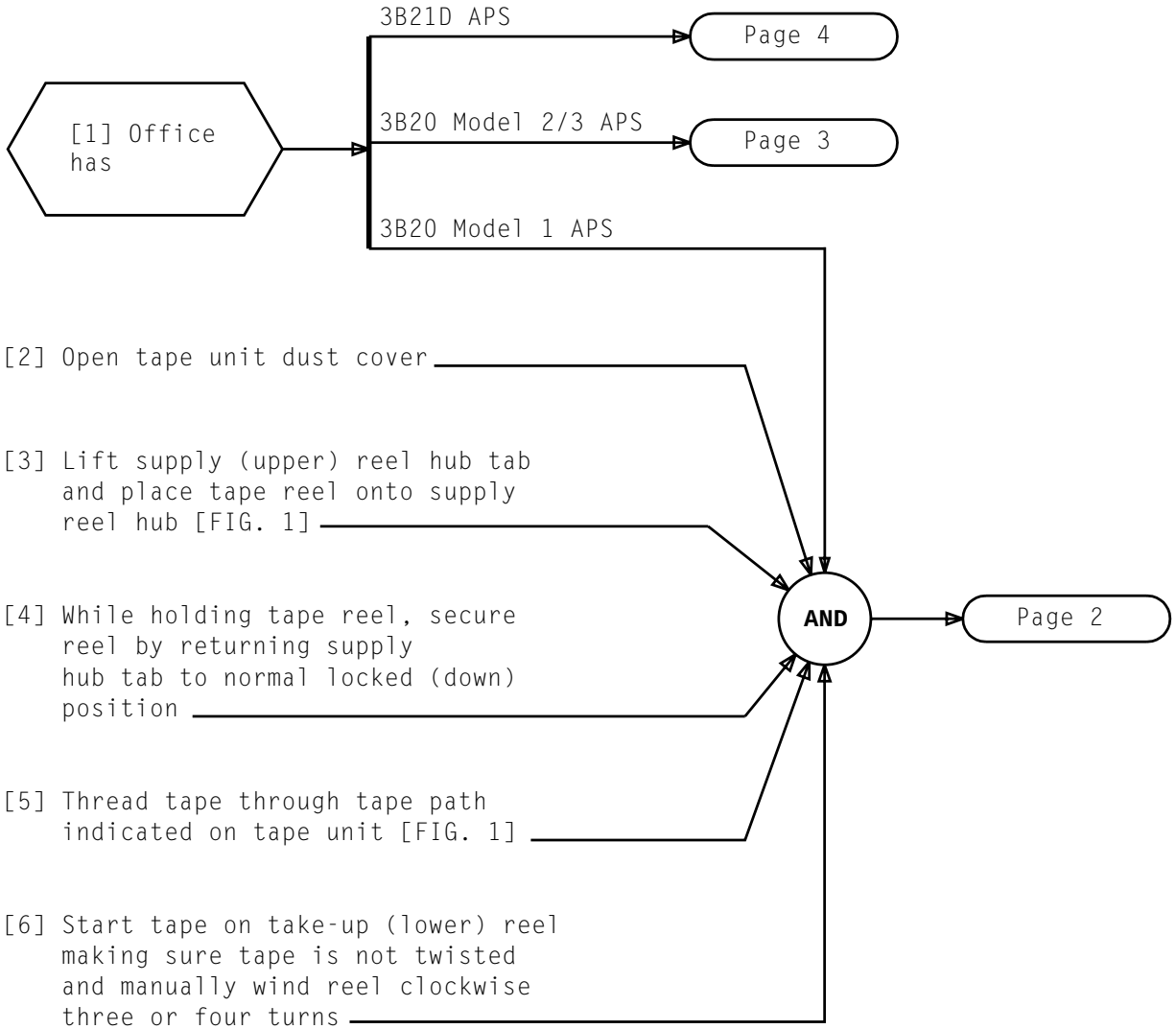


FIG. 3 — DAT Unit

DEMOUNT 1600 BPI/4mm TAPE ON ATTACHED PROCESSOR SYSTEM (APS) TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT



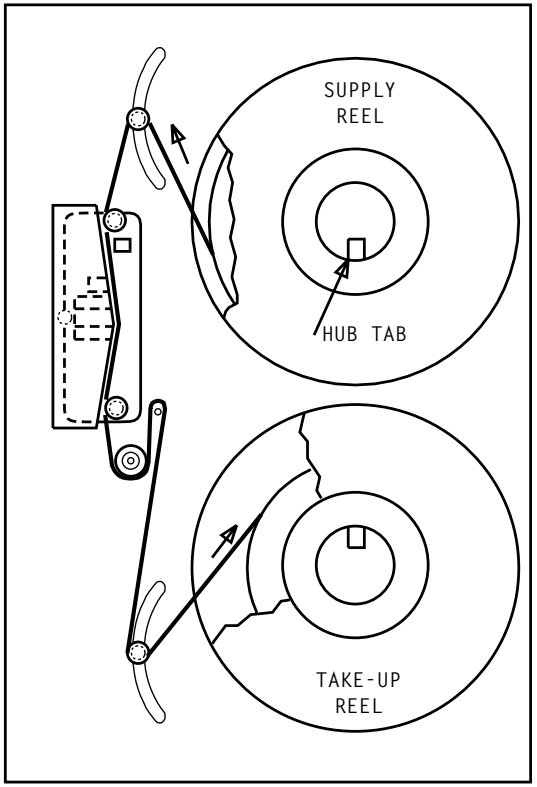
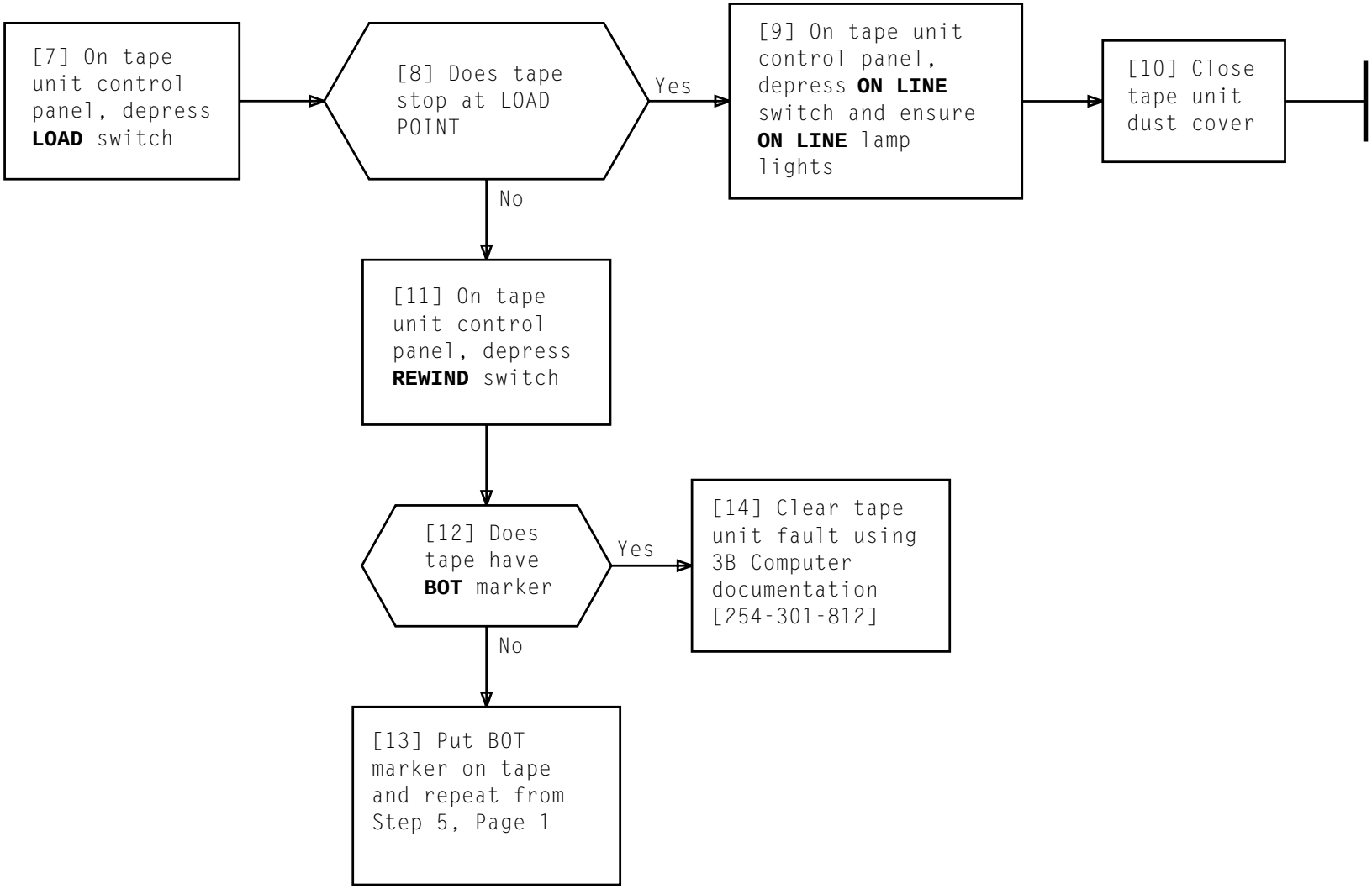


FIG. 1 – APS Kennedy Tape Unit

MOUNT 1600 BPI/4mm TAPE ON ATTACHED PROCESSOR SYSTEM (APS) TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT



MOUNT 1600 BPI/4mm TAPE ON ATTACHED PROCESSOR SYSTEM (APS) TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

[15] On tape unit control panel, is **LOGIC OFF** LED lighted

Yes

[16] On tape unit control panel, depress **LOGIC ON** switch
Response: **LOGIC OFF** LED goes off

No

[17] Open tape unit dust cover

[18] Place supply (upper) reel on hub and depress hub latch [FIG. 2]

[19] Thread tape through tape path indicated on tape drive [FIG. 2]

[20] Start tape on take-up (lower) reel making sure tape is not twisted and manually wind reel clockwise three or four turns

[21] Close dust cover

[22] On tape unit control panel, depress **LOAD/REWIND** switch

AND

[23] Does tape move and stop, and **BOT** LED lighted

Yes

[26] Touch **ON LINE** switch

No

[24] Touch **RESET** switch, attach beginning of tape (BOT) marker, and repeat from Step 19

No

[25] To clear fault, refer to TOP 254-301-812

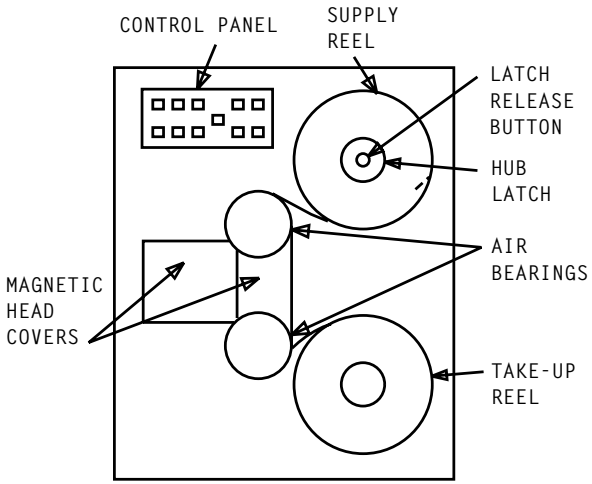


FIG. 2 — APS Keystone Tape Unit

MOUNT 1600 BPI/4mm TAPE ON ATTACHED PROCESSOR SYSTEM (APS) TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

[27] Is tape to be written

No

Yes

[28] Put write-protect tab on 4-mm tape in the up (unlocked) position [FIG. 3]

[29] See NOTE 1 and CAUTION 1. At available in-service digital audio tape (DAT) unit (EQL 11-124 or 62-124), carefully insert 4-mm tape [FIG. 4]

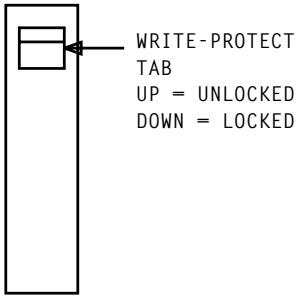


FIG. 3 — 4-mm Tape

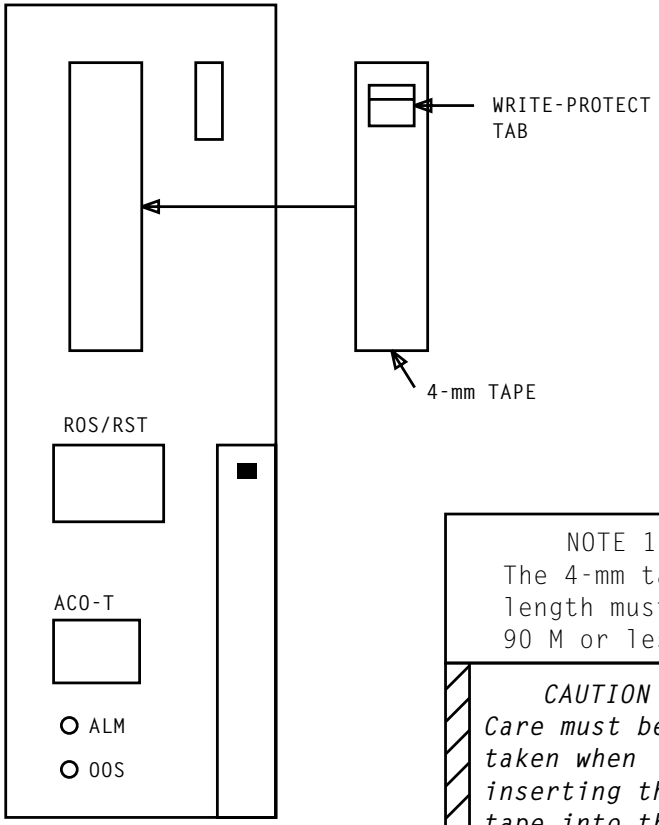


FIG. 4 — DAT Unit

NOTE 1
The 4-mm tape length must be 90 M or less

CAUTION 1
Care must be taken when inserting the tape into the DAT unit. Tape must not be forced

MOUNT 1600 BPI/4mm TAPE ON ATTACHED PROCESSOR SYSTEM (APS) TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

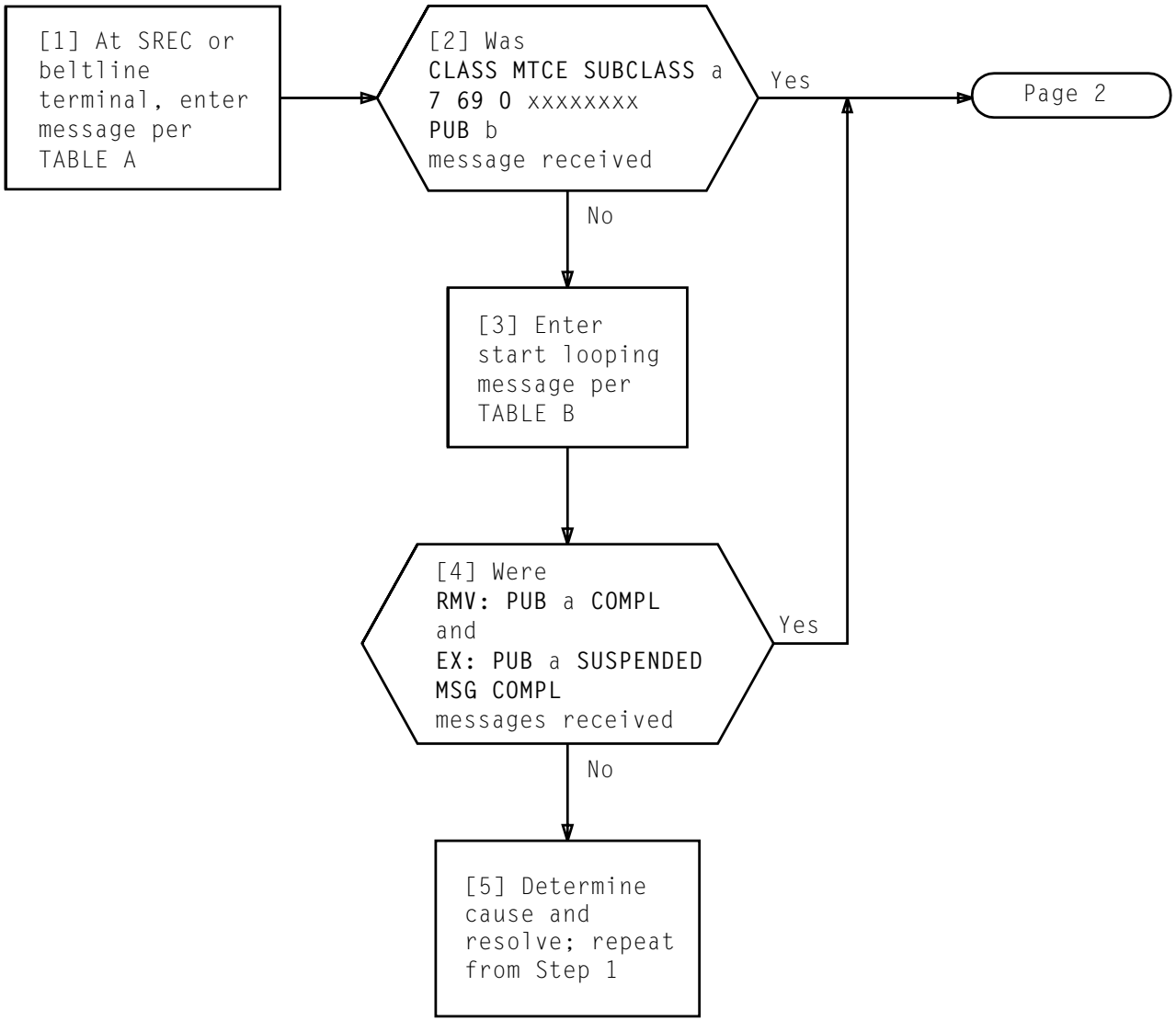


TABLE A

MESSAGE NUMBER	INPUT MESSAGE
1	OP:MACLI,CLASS MTCE!

TABLE B

MESSAGE NUMBER	INPUT MESSAGE
1	EX:PUB a;START!

a = bus 0 or 1

ADVANCE PROGRAM AND SET UP LOOP TO OBSERVE BIT ON PU ENABLE ADDRESS AND/OR WRITE AND REPLY BUSES

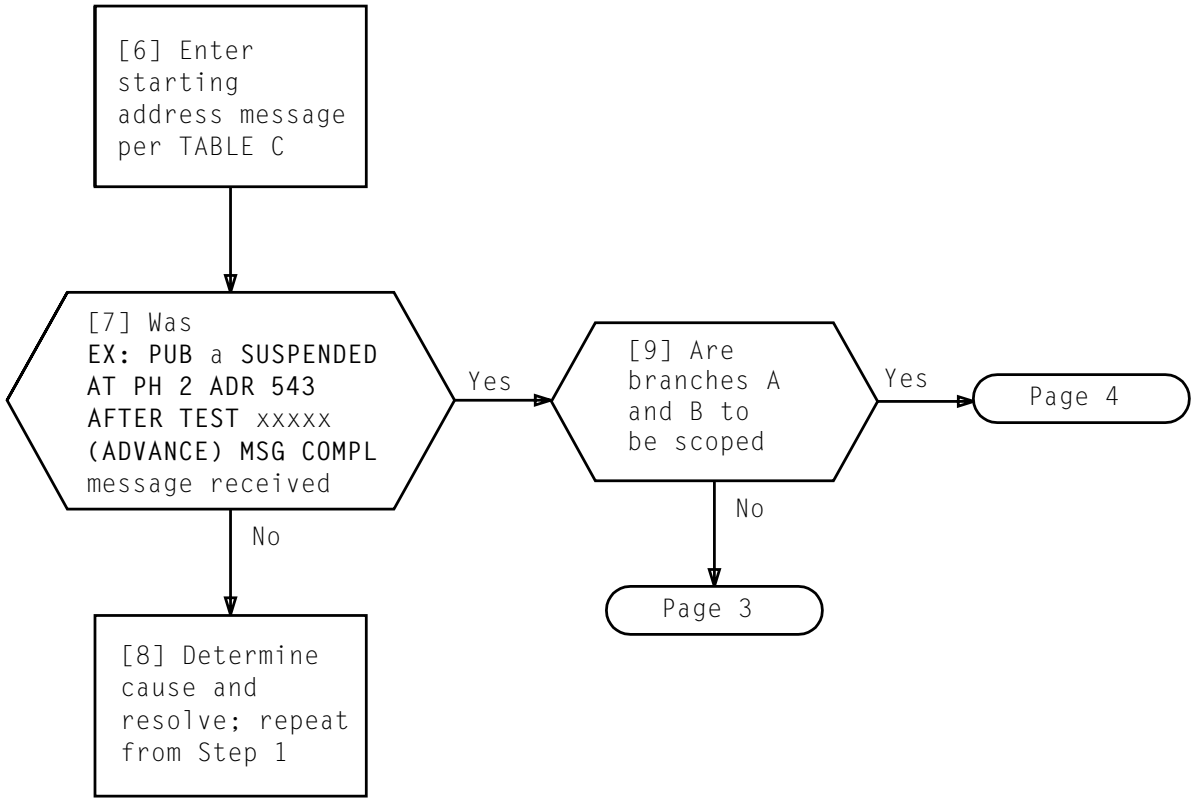


TABLE C	
MESSAGE NUMBER	**INPUT MESSAGE**
1	EX:PUB a:PH 2,ADR 543!
a = bus 0 or 1 543 = Address of statement label STM10600	

ADVANCE PROGRAM AND SET UP LOOP TO OBSERVE BIT ON PU ENABLE ADDRESS AND/OR WRITE AND REPLY BUSES

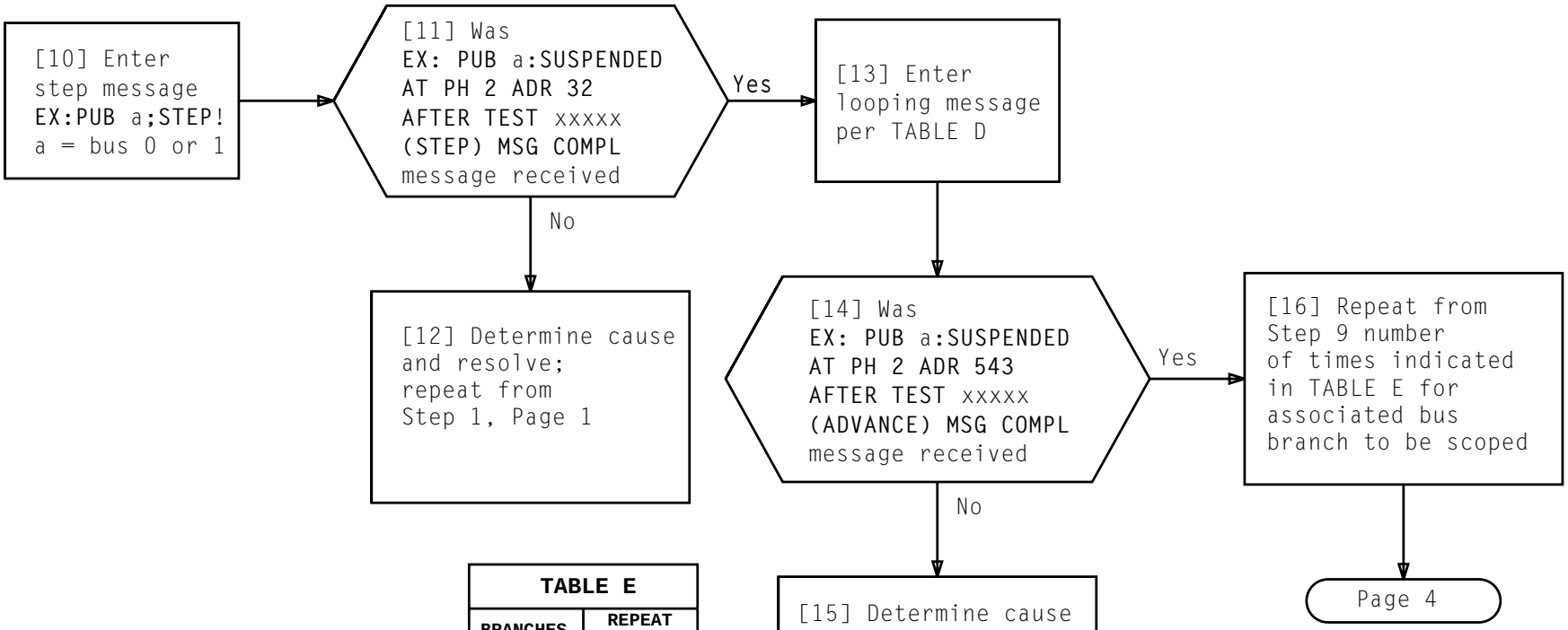


TABLE D	
MESSAGE NUMBER	**INPUT MESSAGE**
1	EX:PUB a:ADR 543!
a = bus 0 or 1 543 = Address of statement label STM10600	

TABLE E	
BRANCHES	**REPEAT NUMBER**
C,D	0
E,F	1
G,H	2
K,L	3
M,R	4
T,V	5
W,X	6

ADVANCE PROGRAM AND SET UP LOOP TO OBSERVE BIT ON PU ENABLE ADDRESS AND/OR WRITE AND REPLY BUSES

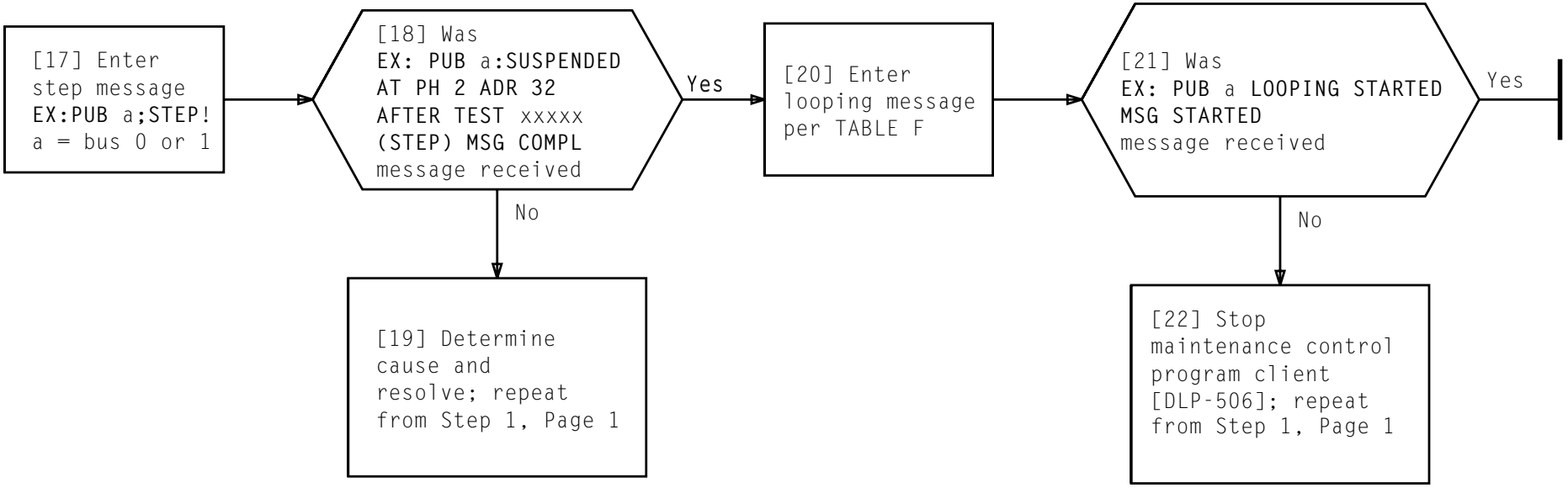


TABLE F

MESSAGE NUMBER	INPUT MESSAGE
1	EX:PUB a:ADR b-c!

a = bus 0 or 1

b = 200, Address of statement label PBTS2600 for bit 0 PU write and reply bus or 207, Address of statement label PBTS2900 for other bits

c = 207, Address of statement label PBTS2900 for bit 0 PU write and reply bus or 246, Address of statement label PBTS3600 for other bits

ADVANCE PROGRAM AND SET UP LOOP TO OBSERVE BIT ON PU ENABLE ADDRESS AND/OR WRITE AND REPLY BUSES

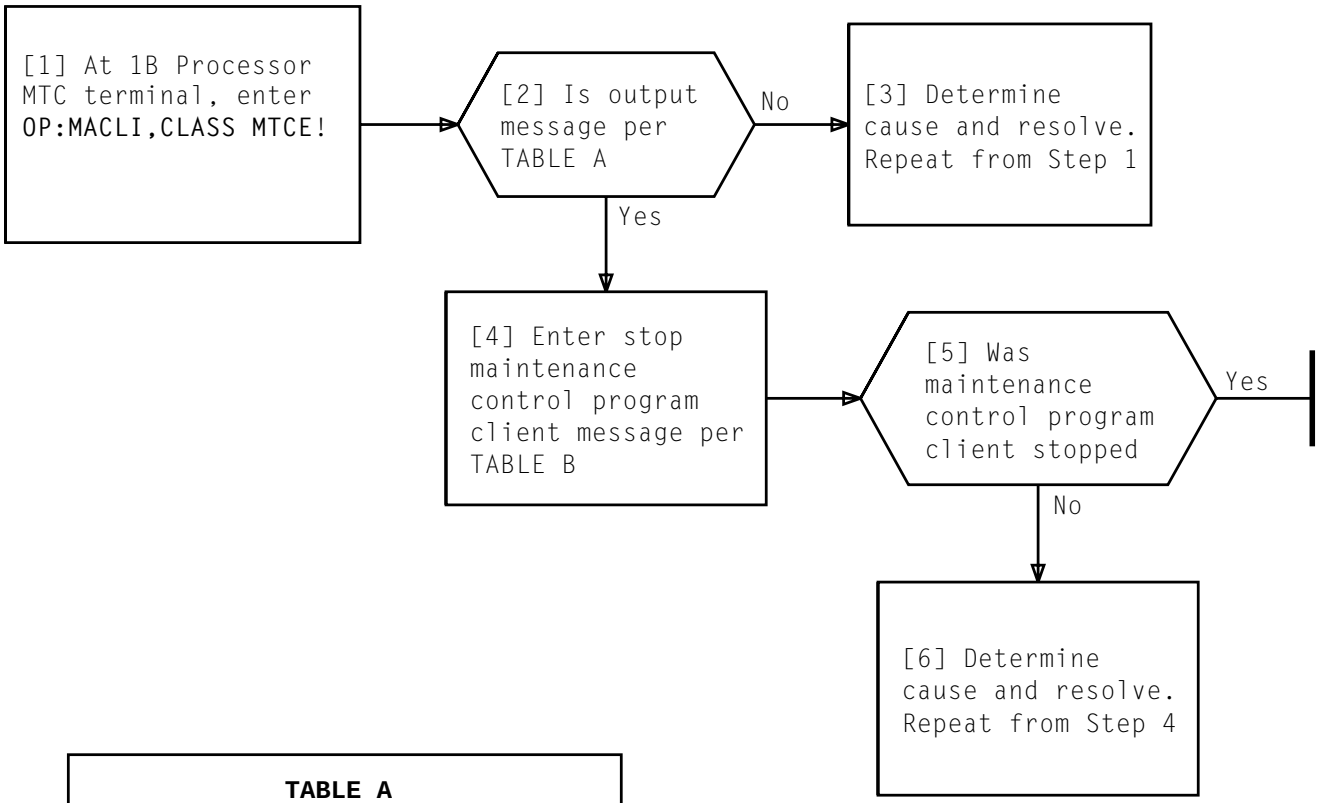


TABLE A
OP:MACLI CLASS MTCE SUBCLASS 0 a - d e f CLASS MTCE SUBCLASS 1 a - d e f CLASS MTCE SUBCLASS 2 a - d e f
a - d = NONE or variable data e = Unit type f = Member number

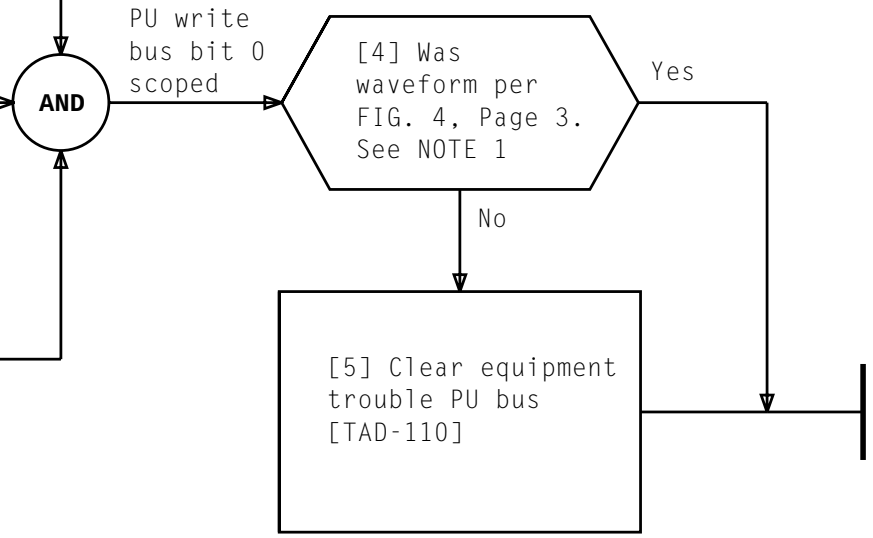
TABLE B
STOP:MACLI,CLASS MTCE,SUBCLASS a!
a = CLASS MTCE SUBCLASS number from output message assigned to PUB diagnostics

STOP MAINTENANCE CONTROL PROGRAM CLIENT

[1] Locate line in FIG. 1, 2, 3, or 5, Pages 2 and 3, that contains last frame where PU write bus is terminated on bus branch to be scoped

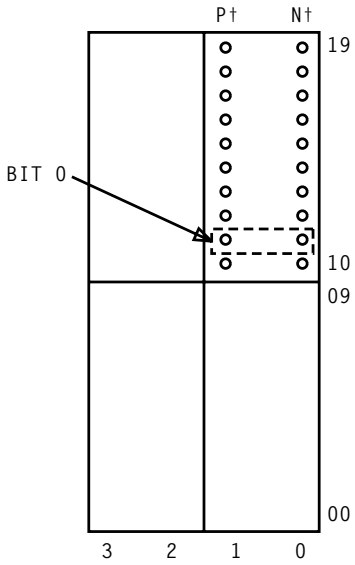
[2] Assure that scope probes are wrapped around each other with positive lead connected to Channel 1 and negative lead connected to Channel 2 and that ground leads are attached together

[3] Scope P- and N-pins in dash line box, per FIG. 1, 2, 3, or 5, Pages 2 and 3, at connector location on line in Step 1. Observe oscilloscope for FIG. 4, Page 3, waveform. See NOTE 1



NOTE 1
Pulse waveform will vary depending on distance away from driver. Waveform measurements should be similar to examples shown in FIG. 4, Page 3

SCOPE PU WRITE BUS BIT 0



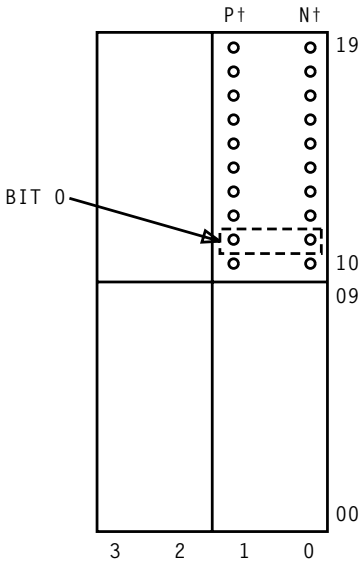
CCIS	*80-25
EST	
BUS 0	080-17
BUS 1	080-38
IO	
BUS 0	080-03
BUS 1	080-27
IOP	
BUS 0	080-31
BUS 1	076-31
NCLK	*60-40
SP 1 (WITH D&SM FRAME)	
BUS 0	380-14
BUS 1	480-14
SP 1 (WITH COMBINED MATRIX FRAME)	
BUS 0	280-32
BUS 1	380-32
SP 2	
BUS 0	180-28
BUS 1	280-28
TMSA	*80-14
TMSB	
BUS 0	‡76-32
BUS 1	‡80-32
TSIA-1	*80-46
TSIA-2	*80-51
TSIB	*80-55

* 0 FOR BUS 0 OR 1 FOR BUS 1

† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

‡ 0 FOR PUB TERMINATING AT TMS
BAY 0 OR 1 FOR PUB
TERMINATING AT TMS BAY 1

FIG. 1



PUBB FRAME

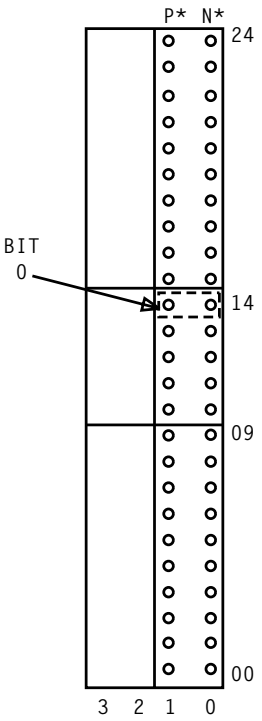
BRANCH A	*76-03
BRANCH B	*72-06
BRANCH C	*76-05
BRANCH D	*72-07
BRANCH E	*64-03
BRANCH F	*60-06
BRANCH G	*64-05
BRANCH H	*60-07
BRANCH K	*48-03
BRANCH L	*44-06
BRANCH M	*48-05
BRANCH R	*44-07
BRANCH T	*36-03
BRANCH V	*32-06
BRANCH W	*36-05
BRANCH X	*32-07

* 0 FOR BUS 0 OR 1 FOR BUS 1

† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 2

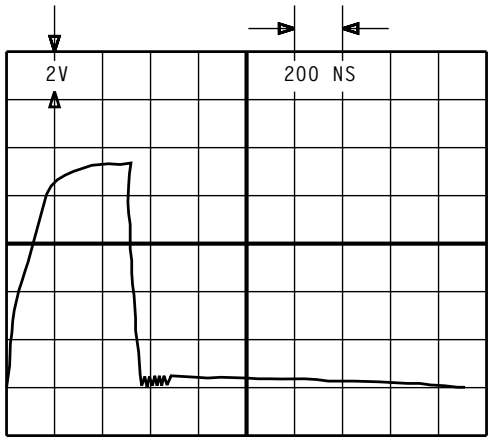
SCOPE PU WRITE BUS BIT 0



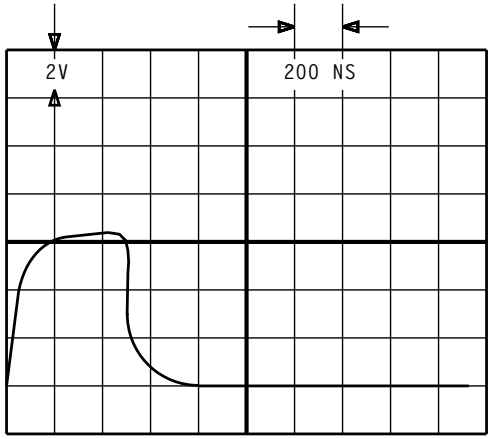
DIF or DIFE (24-31)
BUS 0 180-109
BUS 1 180-257

* P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 3

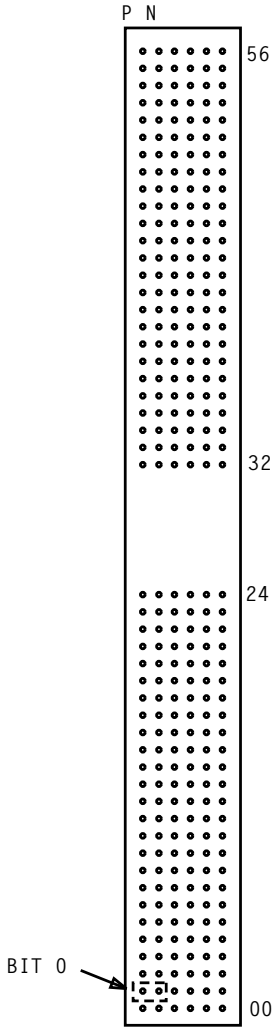


NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 4



SCS		XTSI	
BUS 0	045-168	BUS 0	052-180
BUS 1	053-168	BUS 1	061-180

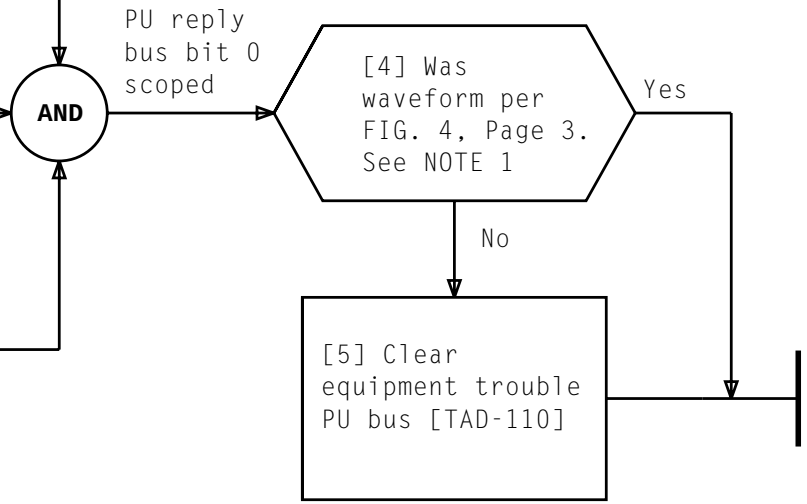
FIG. 5

SCOPE PU WRITE BUS BIT 0

[1] Locate line in FIG. 1, 2, 3, or 5, Pages 2 and 3, that contains last frame where PU reply bus is terminated on bus branch to be scoped

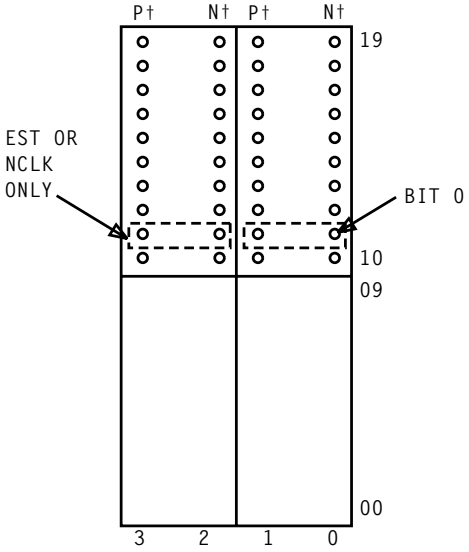
[2] Assure that scope probes are wrapped around each other with positive lead connected to Channel 1 and negative lead connected to Channel 2 and that ground leads are attached together

[3] Scope P- and N-pins in dashed line box, per FIG. 1, 2, 3, or 5, Pages 2 and 3, at connector location on line in Step 1. Observe oscilloscope for FIG. 4, Page 3 waveform. See NOTE 1



NOTE 1
Pulse waveform will vary, depending on distance away from driver. Waveform measurements should be similar to examples shown in FIG. 4, Page 3

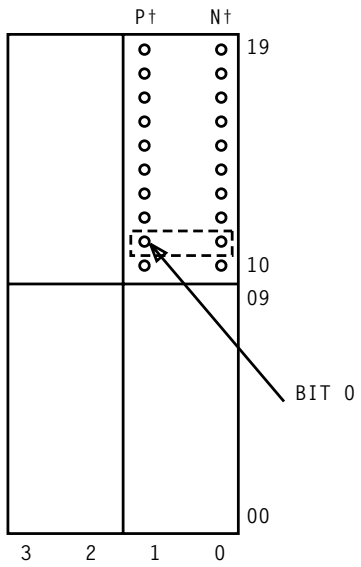
SCOPE PU REPLY BUS BIT 0



CCIS	*80-33
EST	
BUS 0	080-02
BUS 1	080-23
IO	
BUS 0	080-11
BUS 1	080-36
IOP	
BUS 0	080-40
BUS 1	076-40
NCLK	*60-48
SP 1 (WITH D&SM FRAME)	
BUS 0	380-04
BUS 1	480-04
SP 1 (WITH COMBINED MATRIX FRAME)	
BUS 0	280-20
BUS 1	380-20
SP 2	
BUS 0	180-18
BUS 1	280-18
TMS A	*80-04
TMS B	
BUS 0	‡76-20
BUS 1	‡80-20
TSIA-1	*80-36
TSIA-2	*80-39
TSIB	*80-43
VIF	
BUS 0	152-15
BUS 1	152-25

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD
‡ 0 FOR PUB TERMINATING AT TMS
BAY 0 OR 1 FOR PUB TERMINATING
AT TMS BAY 1

FIG. 1



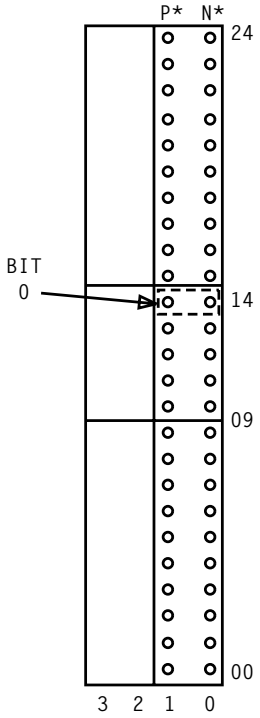
PUBB FRAME

BRANCH A	*76-19
BRANCH B	*72-17
BRANCH C	*76-20
BRANCH D	*72-18
BRANCH E	*64-19
BRANCH F	*60-17
BRANCH G	*64-20
BRANCH H	*60-18
BRANCH K	*48-19
BRANCH L	*44-17
BRANCH M	*48-20
BRANCH R	*44-18
BRANCH T	*36-19
BRANCH V	*32-17
BRANCH W	*36-20
BRANCH X	*32-18

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 2

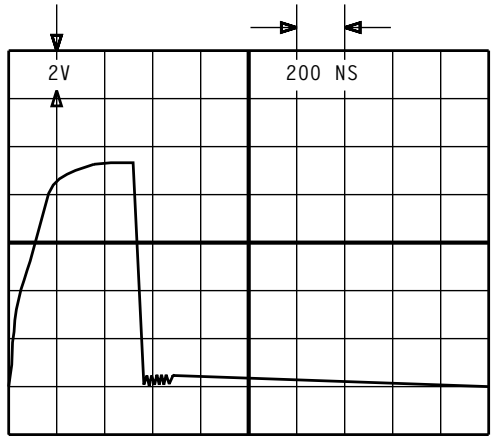
SCOPE PU REPLY BUS BIT 0



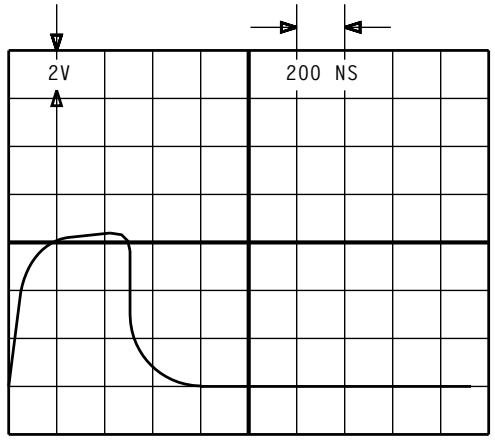
DIF or DIFE (24-31)
BUS 0 180-053
BUS 1 180-201

*P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 3

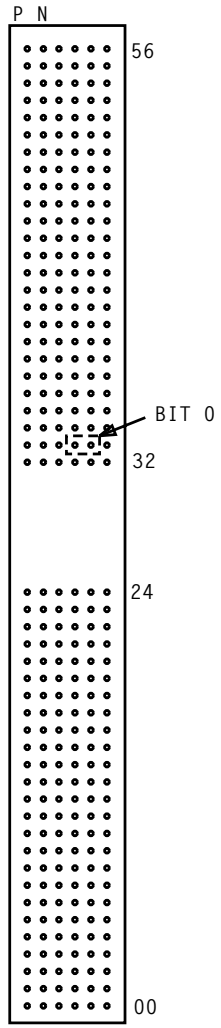


NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 4



SCS		XTSI	
BUS 0	045-168	BUS 0	052-180
BUS 1	053-168	BUS 1	061-180

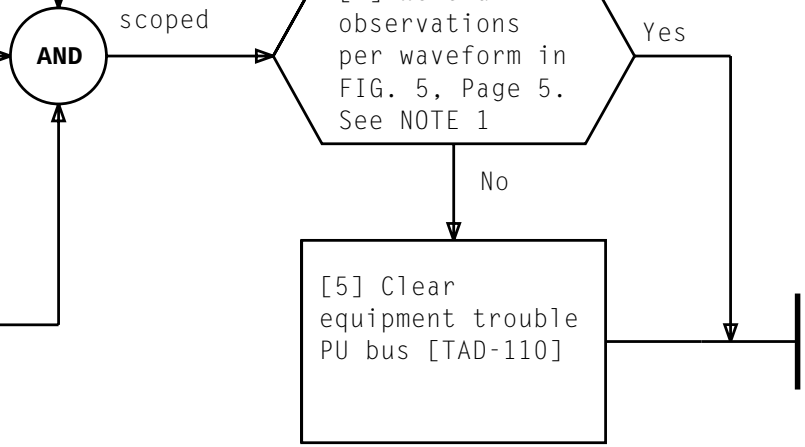
FIG. 5

SCOPE PU REPLY BUS BIT 0

[1] Locate line in FIG. 1, 2, 3, 4, or 6, Pages 2, 3, 4, 5, and 6, respectively, that contains last frame where PU write bus is terminated on bus branch to be scoped

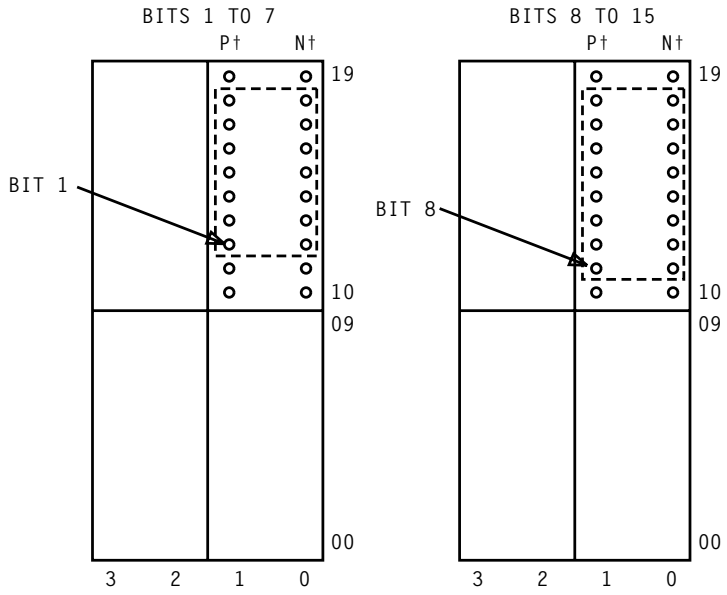
[2] Assure that scope probes are wrapped around each other with positive lead connected to Channel 1 and negative lead connected to Channel 2 and that ground leads are attached together

[3] Scope P- and N-pins in each dashed line box, per FIG. 1, 2, 3, 4, or 6, Pages 2, 3, 4, 5, and 6, respectively, at connector locations on line in Step 1. Observe oscilloscope for FIG. 5, Page 5, waveform. See NOTE 1



NOTE 1
Pulse waveform will vary, depending on distance away from driver. Waveform measurements should be similar to examples shown in FIG. 5, Page 5

SCOPE PU WRITE BUS BITS 1 TO 35

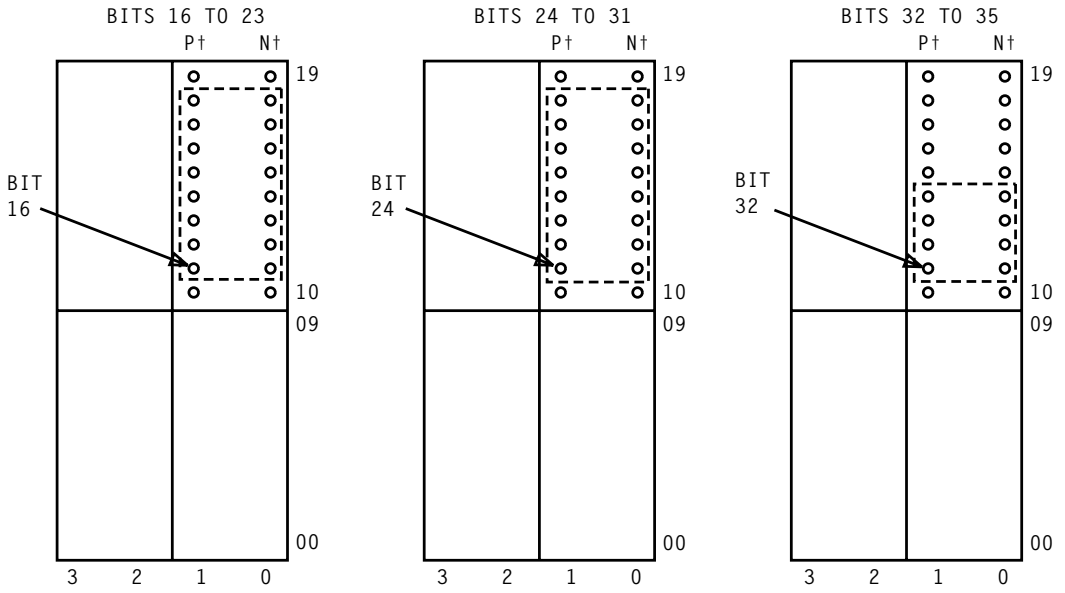


FRAME	BITS 1 TO 7	BITS 8 TO 15
CCIS	*80-25	*80-23
EST		
BUS 0	080-17	080-16
BUS 1	080-38	080-37
IO		
BUS 0	080-03	080-04
BUS 1	080-27	080-28
IOP		
BUS 0	080-31	080-33
BUS 1	076-31	076-33
NCLK	*60-40	*60-39
SP 1 (WITH D&SM FRAME)		
BUS 0	380-14	380-13
BUS 1	480-14	480-13
SP 1 (WITH COMBINED MATRIX FRAME)		
BUS 0	280-32	280-30
BUS 1	380-32	380-30
SP 2		
BUS 0	180-28	180-27
BUS 1	280-28	280-27
TMS A	*80-14	*80-13
TMS B		
BUS 0	‡76-32	‡76-30
BUS 1	‡80-32	‡80-30
TSI	*80-46	*80-45
TSIA-1	*80-51	*80-49
TSIB	*80-55	*80-53

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 1

SCOPE PU WRITE BUS BITS 1 TO 35

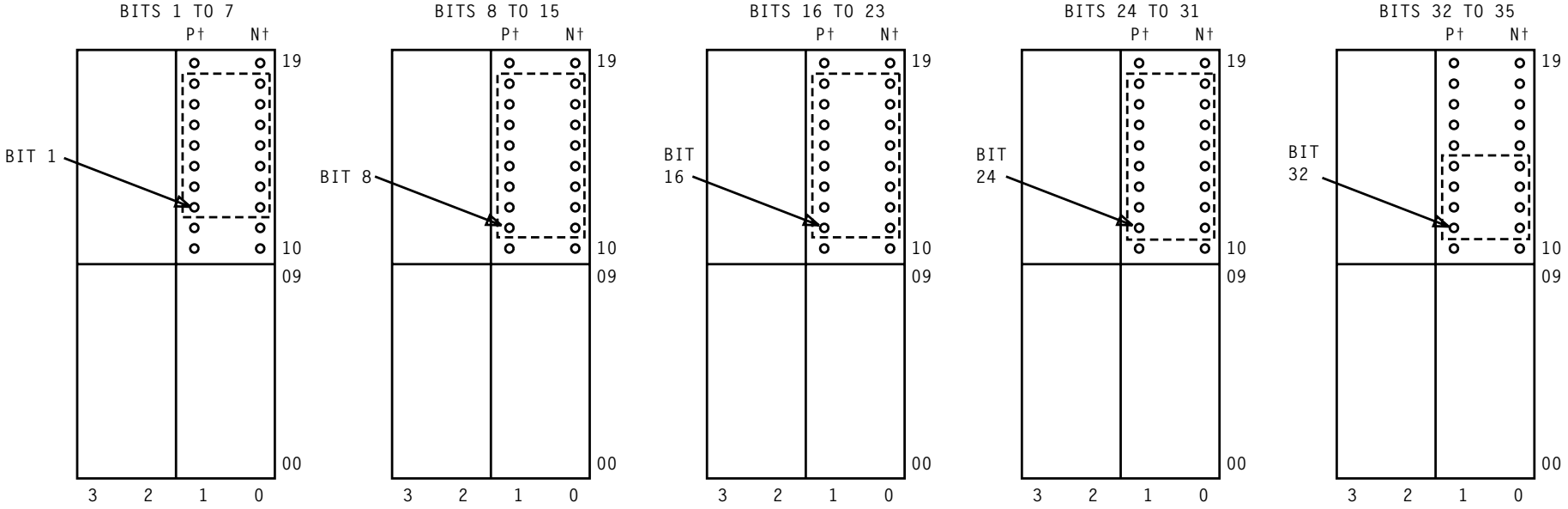


FRAME	BITS 16 TO 23	BITS 24 TO 31	BITS 32 TO 35
CCIS	*80-21	*80-19	*80-18
EST			
BUS 0	080-15	080-14	080-13
BUS 1	080-36	080-35	080-34
IO			
BUS 0	080-05	080-06	080-07
BUS 1	080-29	080-31	080-32
IOP			
BUS 0	080-34	080-36	080-37
BUS 1	076-34	076-36	076-37
NCLK	*60-38	*60-37	*60-36
SP 1 (WITH D&SM FRAME)			
BUS 0	380-12	380-11	380-10
BUS 1	480-12	480-11	480-10
SP 1 (WITH COMBINED MATRIX FRAME)			
BUS 0	280-29	280-27	280-26
BUS 1	380-29	380-27	380-26
SP 2			
BUS 0	180-26	180-25	180-24
BUS 1	280-26	280-25	280-24
TMS A	*80-12	*80-11	*80-10
TMS B			
BUS 0	‡76-29	‡76-27	‡76-26
BUS 1	‡80-29	‡80-27	‡80-26
TSIA-1	*80-44	*80-43	*80-42
TSIA-2	*80-48	*80-46	*80-45
TSIB	*80-52	*80-50	*80-49

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 2

SCOPE PU WRITE BUS BITS 1 TO 35



PUBB FRAME

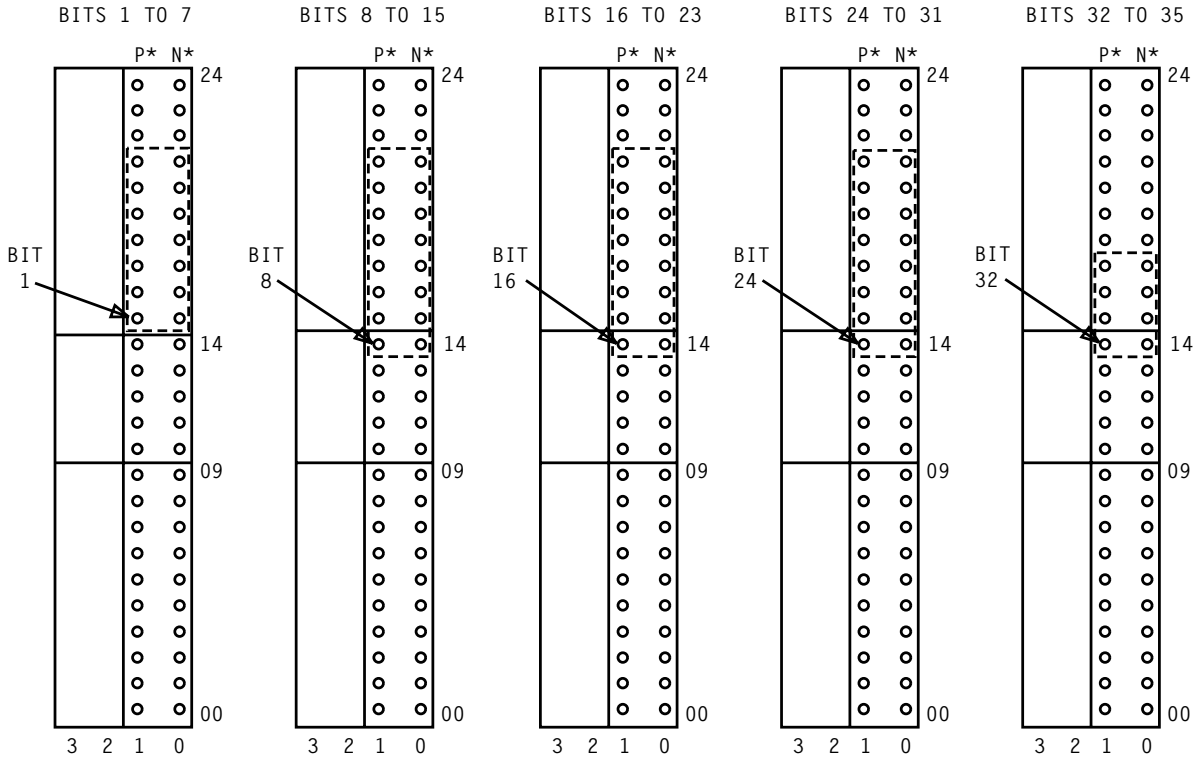
BRANCH A	*76-03	*76-12	*76-34	*76-06	*76-09
BRANCH B	*72-06	*72-12	*72-34	*72-08	*72-10
BRANCH C	*76-05	*76-14	*76-36	*76-08	*76-11
BRANCH D	*72-07	*72-13	*72-35	*72-09	*72-11
BRANCH E	*64-03	*64-12	*64-34	*64-06	*64-09
BRANCH F	*60-06	*60-12	*60-34	*60-08	*60-10
BRANCH G	*64-05	*64-14	*64-36	*64-08	*64-11
BRANCH H	*60-07	*60-13	*60-35	*60-09	*60-11
BRANCH K	*48-03	*48-12	*48-34	*48-06	*48-09
BRANCH L	*44-06	*44-12	*44-34	*44-08	*44-10
BRANCH M	*48-05	*48-14	*48-36	*48-08	*48-11
BRANCH R	*44-07	*44-13	*44-35	*44-09	*44-11
BRANCH T	*36-03	*36-12	*36-34	*36-06	*36-09
BRANCH V	*32-06	*32-12	*32-34	*32-08	*32-10
BRANCH W	*36-05	*36-14	*36-36	*36-08	*36-11
BRANCH X	*32-07	*32-13	*32-35	*32-09	*32-11

* 0 FOR BUS 0 OR 1 FOR BUS 1

† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 3

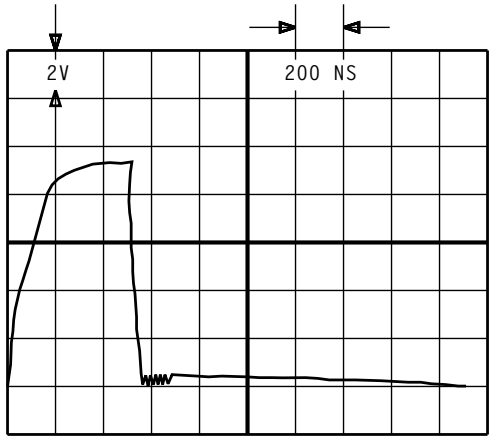
SCOPE PU WRITE BUS BITS 1 TO 35



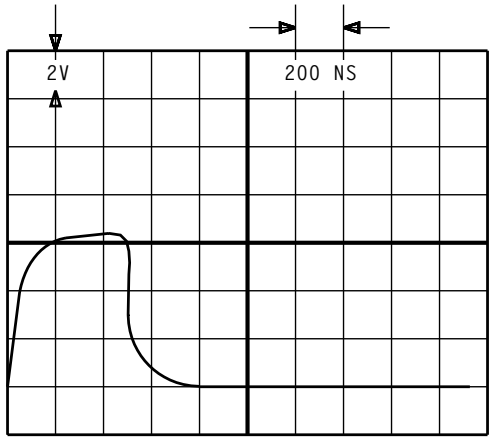
DIF or DIFE (24-31)					
BUS 0	180-109	180-103	180-097	180-091	180-085
BUS 1	180-257	180-251	180-245	180-239	180-233

* P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 4



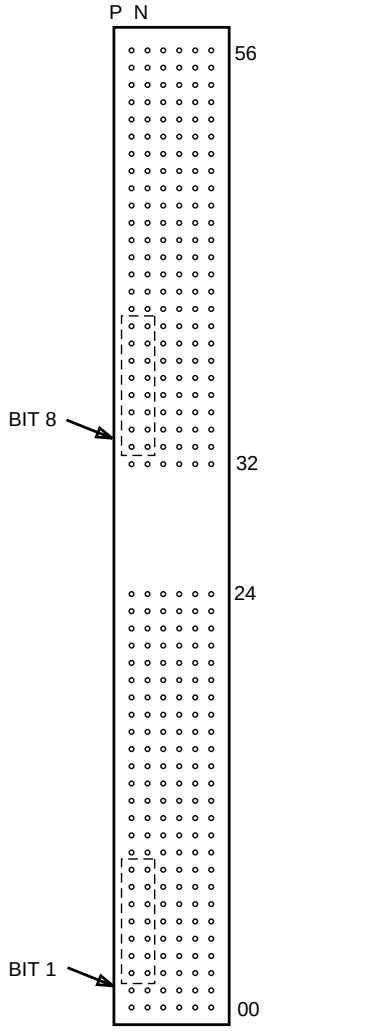
NORMAL PULSE AT DRIVER



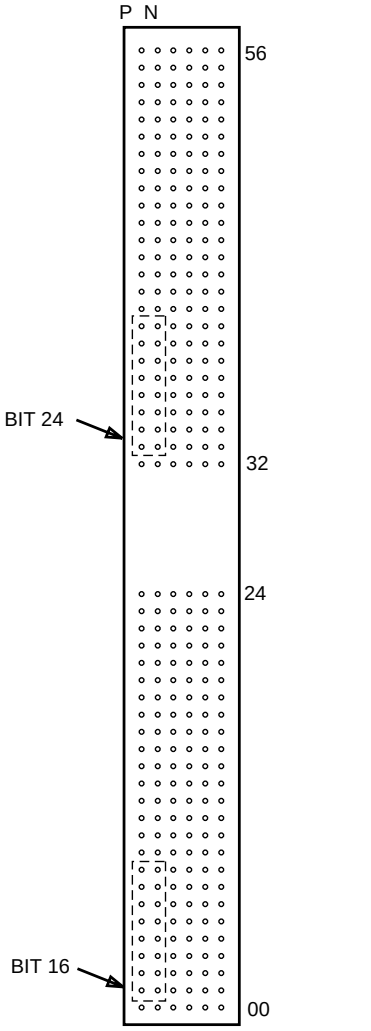
NORMAL PULSE 500 FEET FROM DRIVER

FIG. 5

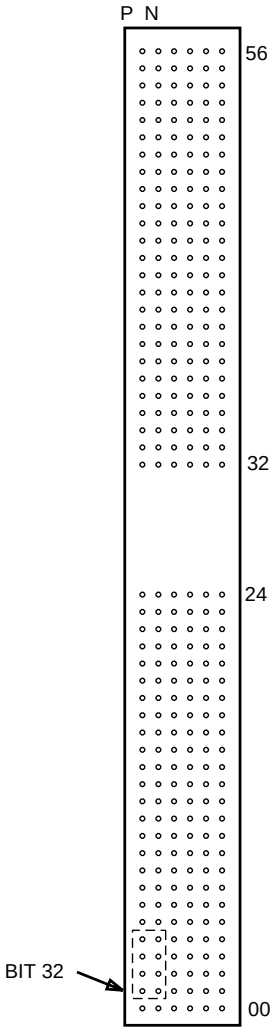
SCOPE PU WRITE BUS BITS 1 TO 35



SCS		XTSI	
BUS 0	045-168	BUS 0	052-180
BUS 1	053-168	BUS 1	061-180



SCS		XTSI	
BUS 0	045-160	BUS 0	052-172
BUS 1	053-160	BUS 1	061-172



SCS		XTSI	
BUS 0	045-152	BUS 0	052-164
BUS 1	053-152	BUS 1	061-164

FIG. 6

SCOPE PU WRITE BUS BITS 1 TO 35

[1] Locate line in FIG. 1, 2, 3, 4, or 6, Pages 2, 3, 4, 5, and 6, that contains last frame where PU enable bus is terminated on bus branch to be scoped

[2] Assure that scope probes are wrapped around each other with positive lead connected to Channel 1 and negative lead connected to Channel 2 and that ground leads are attached together

[3] Scope P- and N-pins in each dashed line box, per FIG. 1, 2, 3, 4, or 5, Pages 2, 3, and 4, at connector locations on line in Step 1. Observe oscilloscope for FIG. 4, Page 4, waveform. See NOTE 1

AND

PU write bus bits 1 to 35 scoped

[4] Were all observations per waveform in FIG. 4, Page 4. See NOTE 1

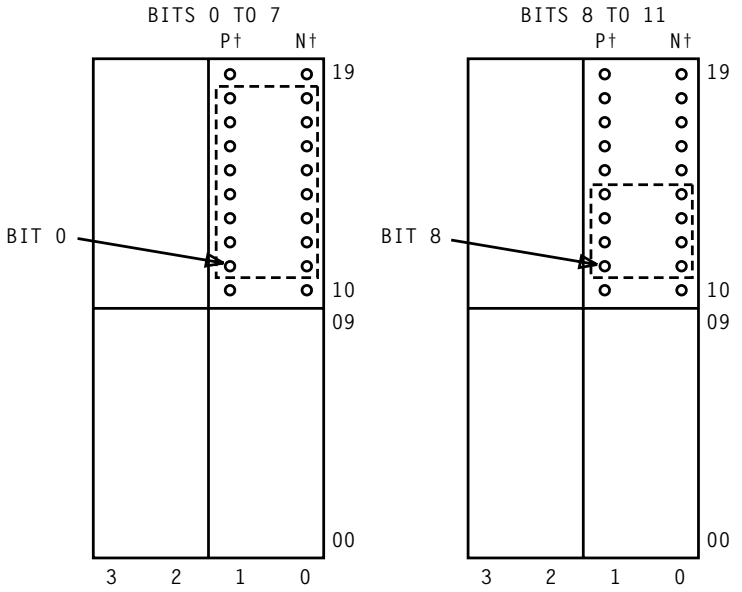
Yes

No

[5] Clear equipment trouble PU bus [TAD-110]

NOTE 1
Pulse waveform will vary, depending on distance away from driver. Waveform measurements should be similar to examples shown in FIG. 5, Page 5

SCOPE PU ENABLE BUS BITS 0 TO 11

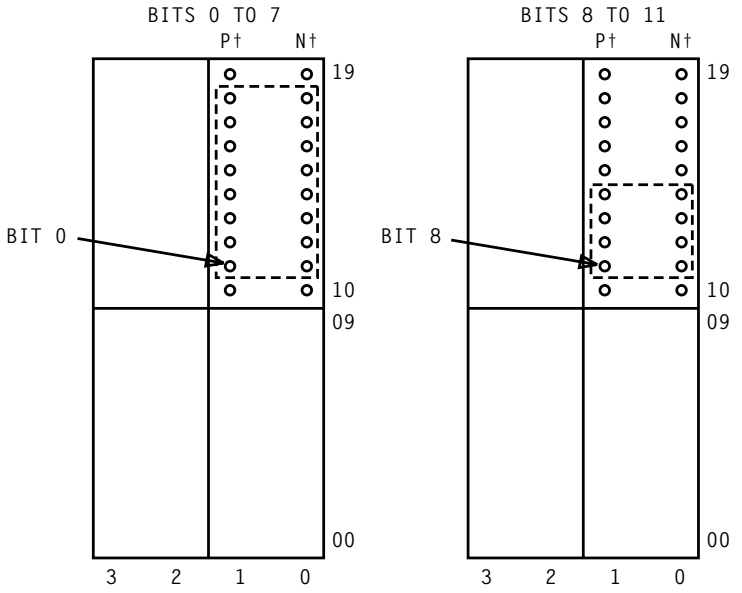


FRAME	BITS 0 TO 7	BITS 8 TO 11
CCIS	*80-16	*80-15
EST		
BUS 0	080-12	080-11
BUS 1	080-33	080-32
IO		
BUS 0	080-08	080-09
BUS 1	080-33	080-34
IOP		
BUS 0	080-24	080-27
BUS 1	076-24	076-27
NCLK	*60-35	*60-34
SP 1 (WITH D&SM FRAME)		
BUS 0	380-09	380-08
BUS 1	480-09	480-08
SP 1 (WITH COMBINED MATRIX FRAME)		
BUS 0	280-24	280-23
BUS 1	380-24	380-23
SP 2		
BUS 0	180-23	180-22
BUS 1	280-23	280-22
TMS A	*80-09	*80-08
TMS B		
BUS 0	‡76-24	‡76-23
BUS 1	‡80-24	‡80-23
TSIA-1	*80-41	*80-40
TSIA-2	*80-43	*80-42
TSIB	*80-47	*80-46

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 1

SCOPE PU ENABLE ADDRESS BUS BITS 0 TO 11

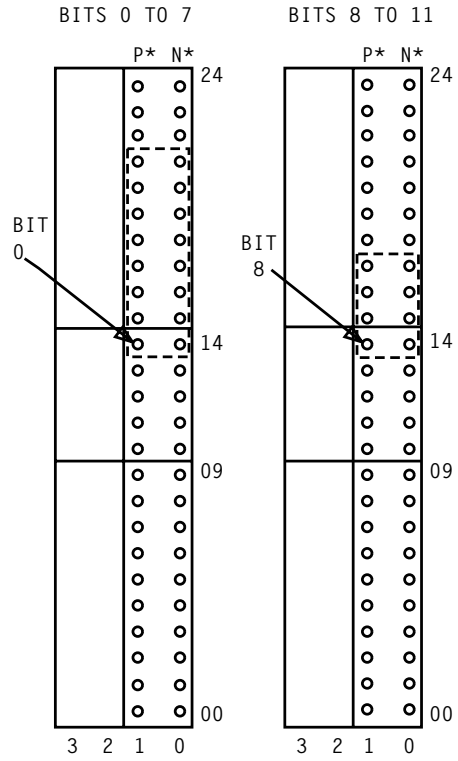


PUBB FRAME	BITS 0 TO 7	BITS 8 TO 11
BRANCH A	*76-37	*76-40
BRANCH B	*72-36	*72-38
BRANCH C	*76-39	*76-42
BRANCH D	*72-37	*72-39
BRANCH E	*64-37	*64-40
BRANCH F	*60-36	*60-38
BRANCH G	*64-39	*64-42
BRANCH H	*60-37	*60-39
BRANCH K	*48-37	*48-40
BRANCH L	*44-36	*44-38
BRANCH M	*48-39	*48-42
BRANCH R	*44-37	*44-39
BRANCH T	*36-37	*36-40
BRANCH V	*32-36	*32-38
BRANCH W	*36-39	*36-42
BRANCH X	*32-37	*32-39

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 2

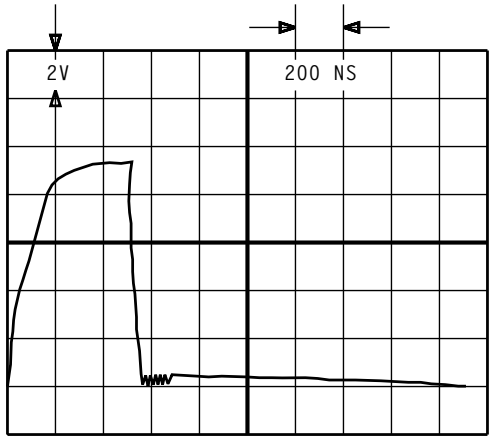
SCOPE PU ENABLE ADDRESS BUS BITS 0 TO 11



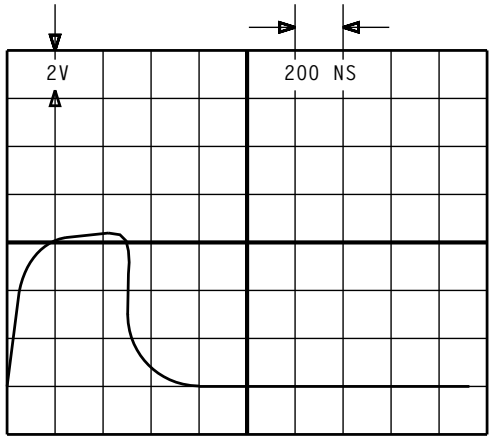
DIF or DIFE (24-31)		
BUS 0	180-079	180-073
BUS 1	180-227	180-221

* P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 3

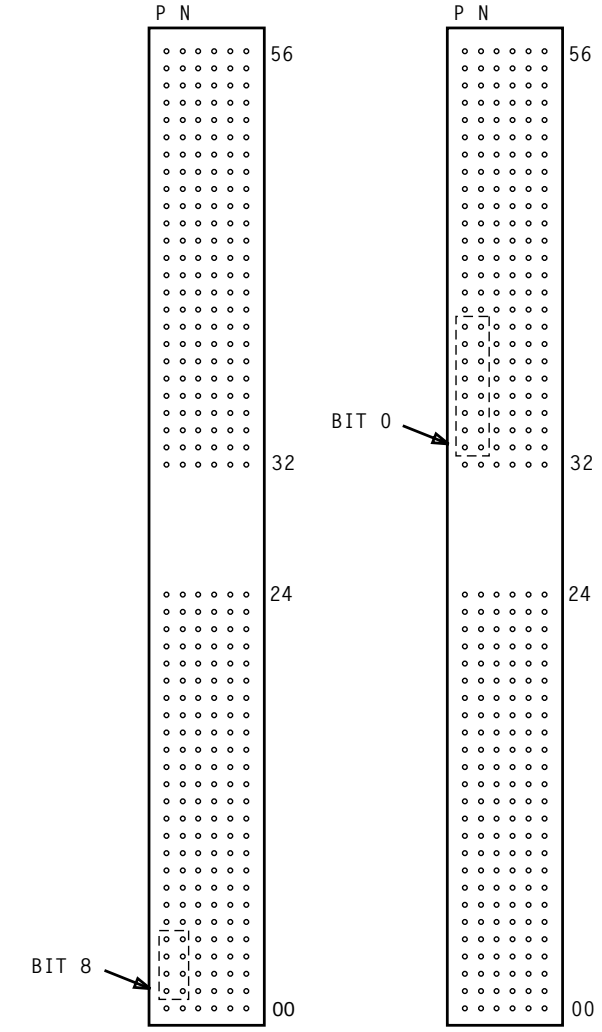


NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 4



SCS		XTSI		SCS		XTSI	
BUS 0	045-144	BUS 0	052-156	BUS 0	045-152	BUS 0	052-164
BUS 1	053-144	BUS 1	061-156	BUS 1	053-152	BUS 1	061-164

FIG. 5

SCOPE PU ENABLE ADDRESS BUS BITS 0 TO 11

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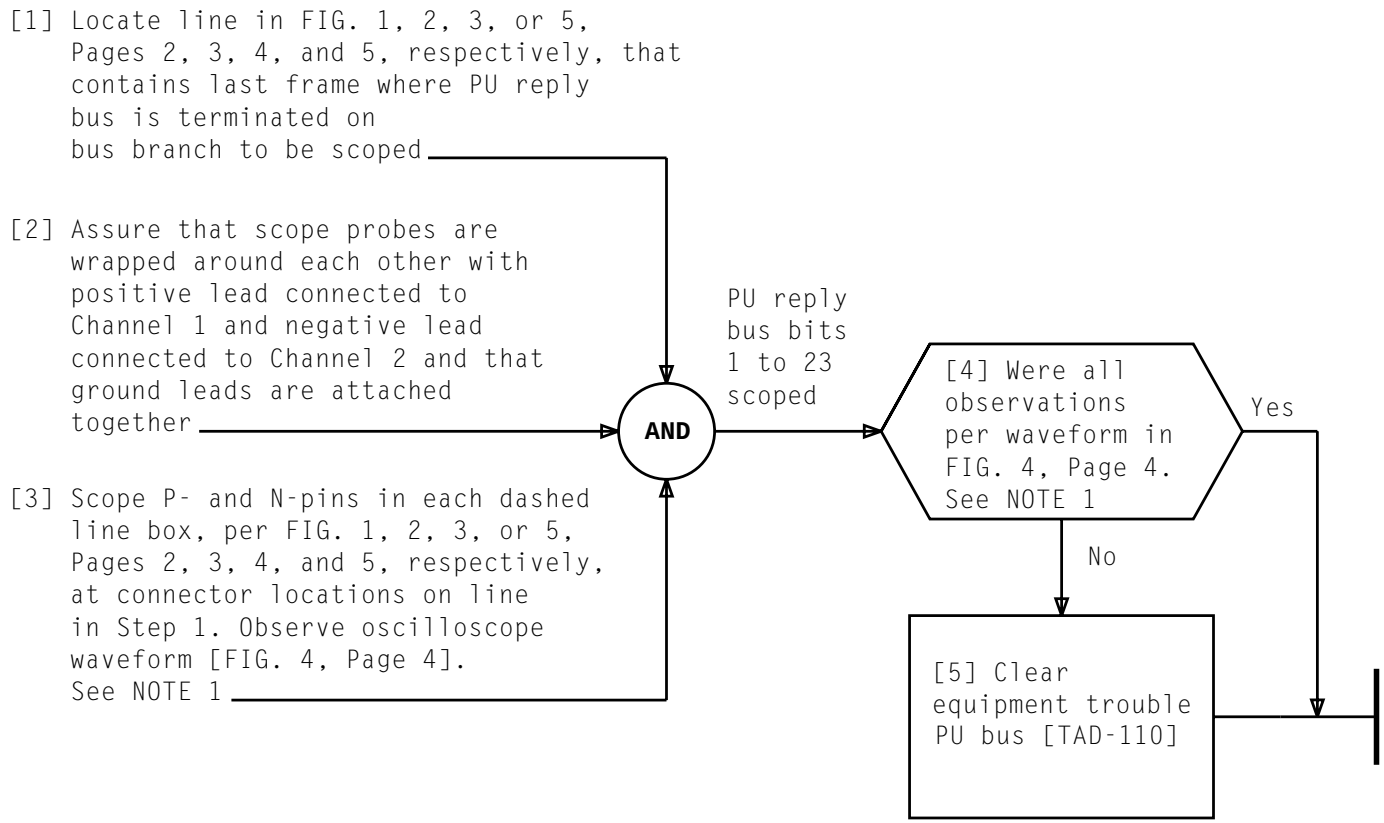
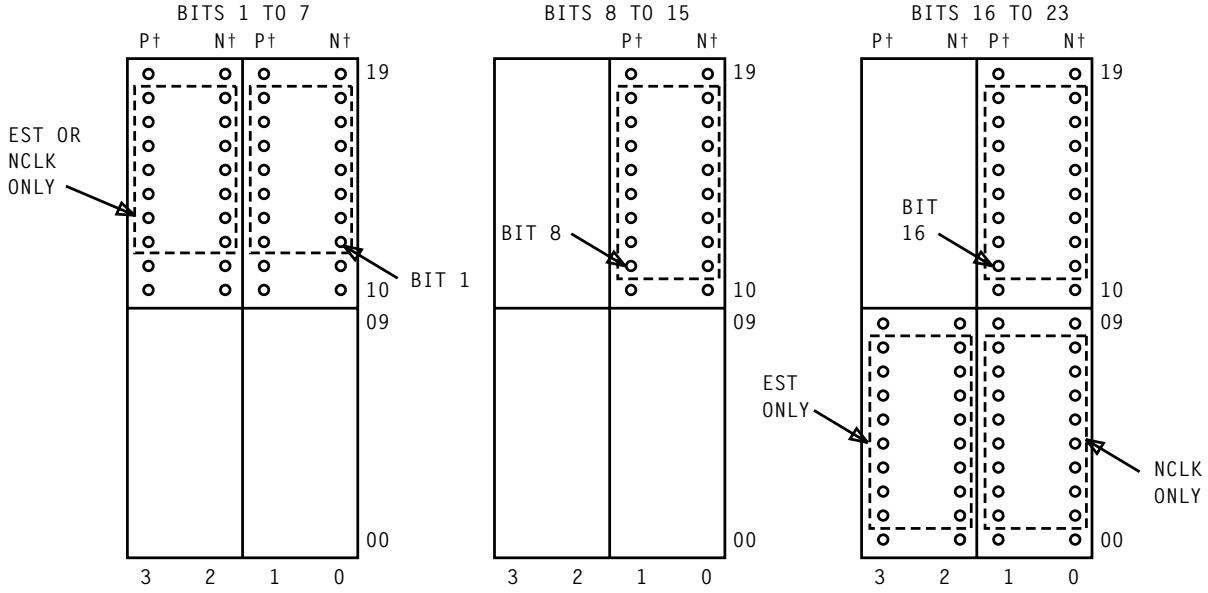
SCOPE PU REPLY BUS BITS 1 TO 23



NOTE 1
Pulse waveform will vary, depending on distance away from driver. Waveform measurements should be similar to examples shown in FIG. 4, Page 4

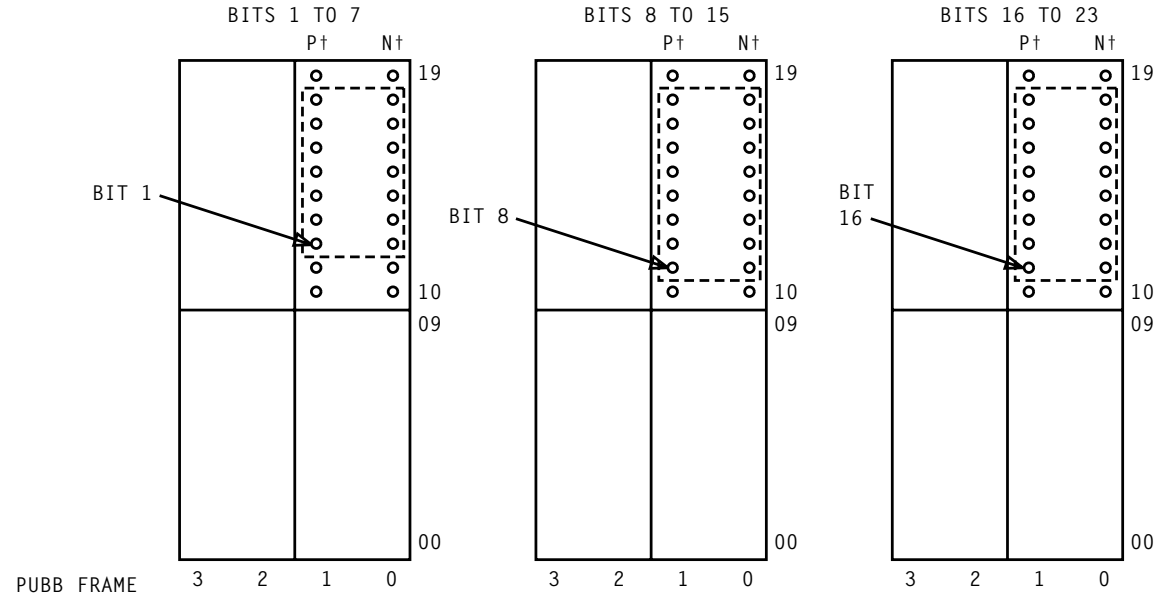


FRAME	BITS 1 TO 7	BITS 8 TO 15	BITS 16 TO 23
CCIS	*80-33	*80-32	*80-31
EST			
BUS 0	080-02	080-02	080-02
BUS 1	080-23	080-23	080-23
IO			
BUS 0	080-11	080-12	080-13
BUS 1	080-36	080-37	080-38
IOP			
BUS 0	080-40	080-41	080-42
BUS 1	076-40	076-41	076-42
NCLK	*60-48	*60-48	*60-48
SP 1 (WITH D&SM FRAME)			
BUS 0	380-04	380-03	380-02
BUS 1	480-04	480-03	480-02
SP 1 (WITH COMBINED MATRIX FRAME)			
BUS 0	280-20	280-18	280-16
BUS 1	380-20	380-18	380-16
SP 2			
BUS 0	180-18	180-17	180-16
BUS 1	280-18	280-17	280-16
TMS A	*80-04	*80-03	*80-02
TMS B			
BUS 0	‡76-20	‡76-18	‡76-16
BUS 1	‡80-20	‡80-18	‡80-16
TSIA-1	*80-36	*80-35	*80-34
TSIA-2	*80-39	*80-37	*80-35
TSIB	*80-43	*80-41	*80-39
VIF			
BUS 0	152-15	152-14	152-13
BUS 1	152-25	152-24	152-23

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 1

SCOPE PU REPLY BUS BITS 1 TO 23

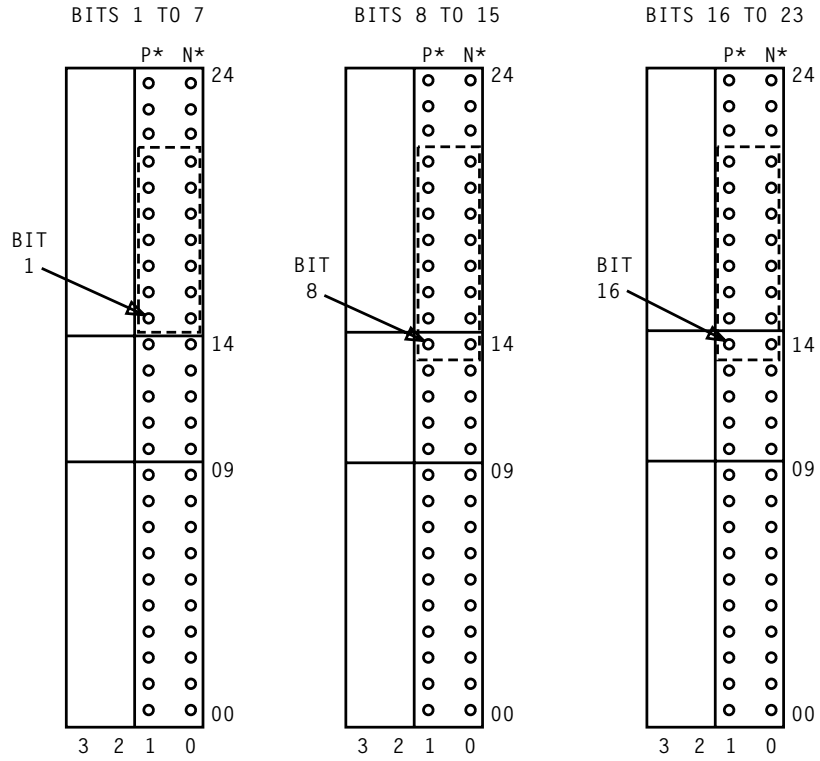


PUBB FRAME			
BRANCH A	*76-19	*76-21	*76-23
BRANCH B	*72-17	*72-19	*72-25
BRANCH C	*76-20	*76-22	*76-24
BRANCH D	*72-18	*72-20	*72-26
BRANCH E	*64-19	*64-21	*64-23
BRANCH F	*60-17	*60-19	*60-25
BRANCH G	*64-20	*64-22	*64-24
BRANCH H	*60-18	*60-20	*60-26
BRANCH K	*48-19	*48-21	*48-23
BRANCH L	*44-17	*44-19	*44-25
BRANCH M	*48-20	*48-22	*48-24
BRANCH R	*44-18	*44-20	*44-26
BRANCH T	*36-19	*36-21	*36-23
BRANCH V	*32-17	*32-19	*32-25
BRANCH W	*36-20	*36-22	*36-24
BRANCH X	*32-18	*32-20	*32-26

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 2

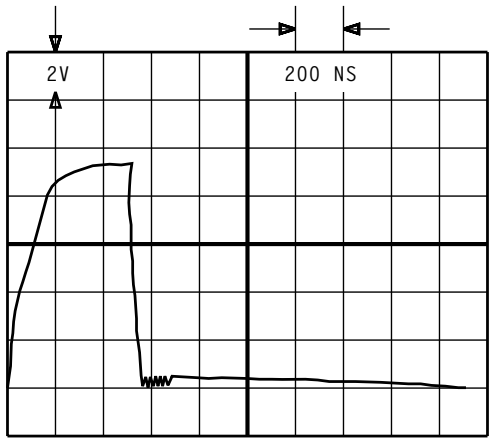
SCOPE PU REPLY BUS BITS 1 TO 23



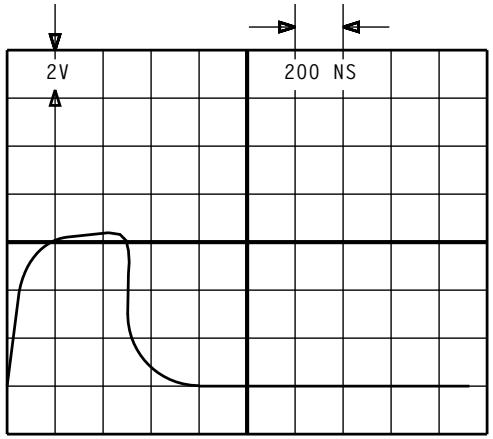
DIF or DIFE (24-31)			
BUS 0	180-053	180-041	180-035
BUS 1	180-201	180-189	180-183

* P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 3



NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 4

SCOPE PU REPLY BUS BITS 1 TO 23

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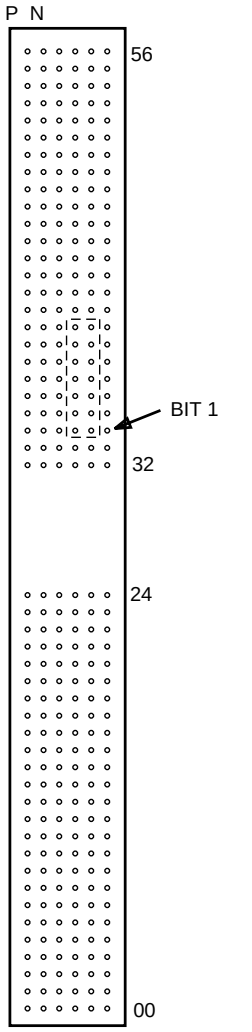
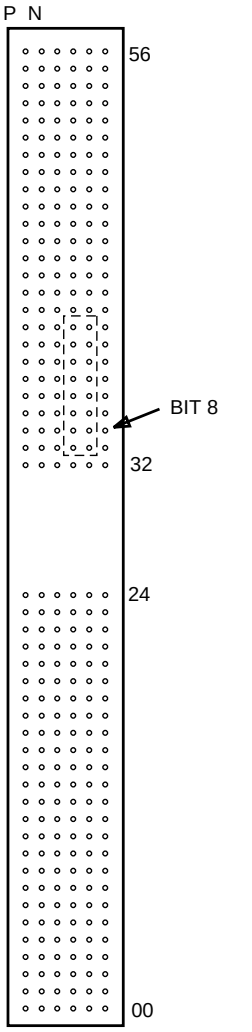
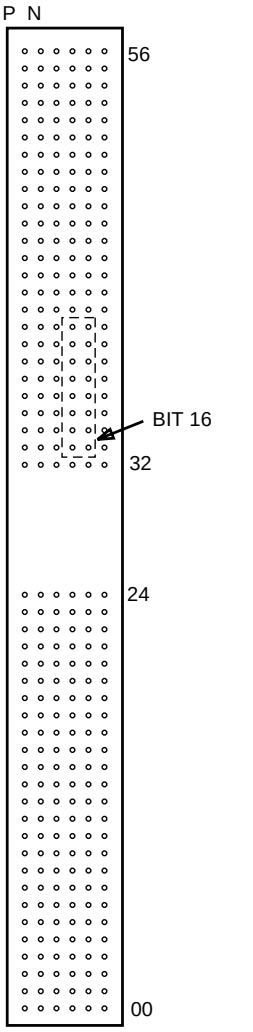


SCS		XTSI	
BUS 0	045-168	BUS 0	052-180
BUS 1	053-168	BUS 1	061-180



SCS		XTSI	
BUS 0	045-160	BUS 0	052-172
BUS 1	053-160	BUS 1	061-172



SCS		XTSI	
BUS 0	045-152	BUS 0	052-164
BUS 1	053-152	BUS 1	061-164

FIG. 5

SCOPE PU REPLY BUS BITS 1 TO 23

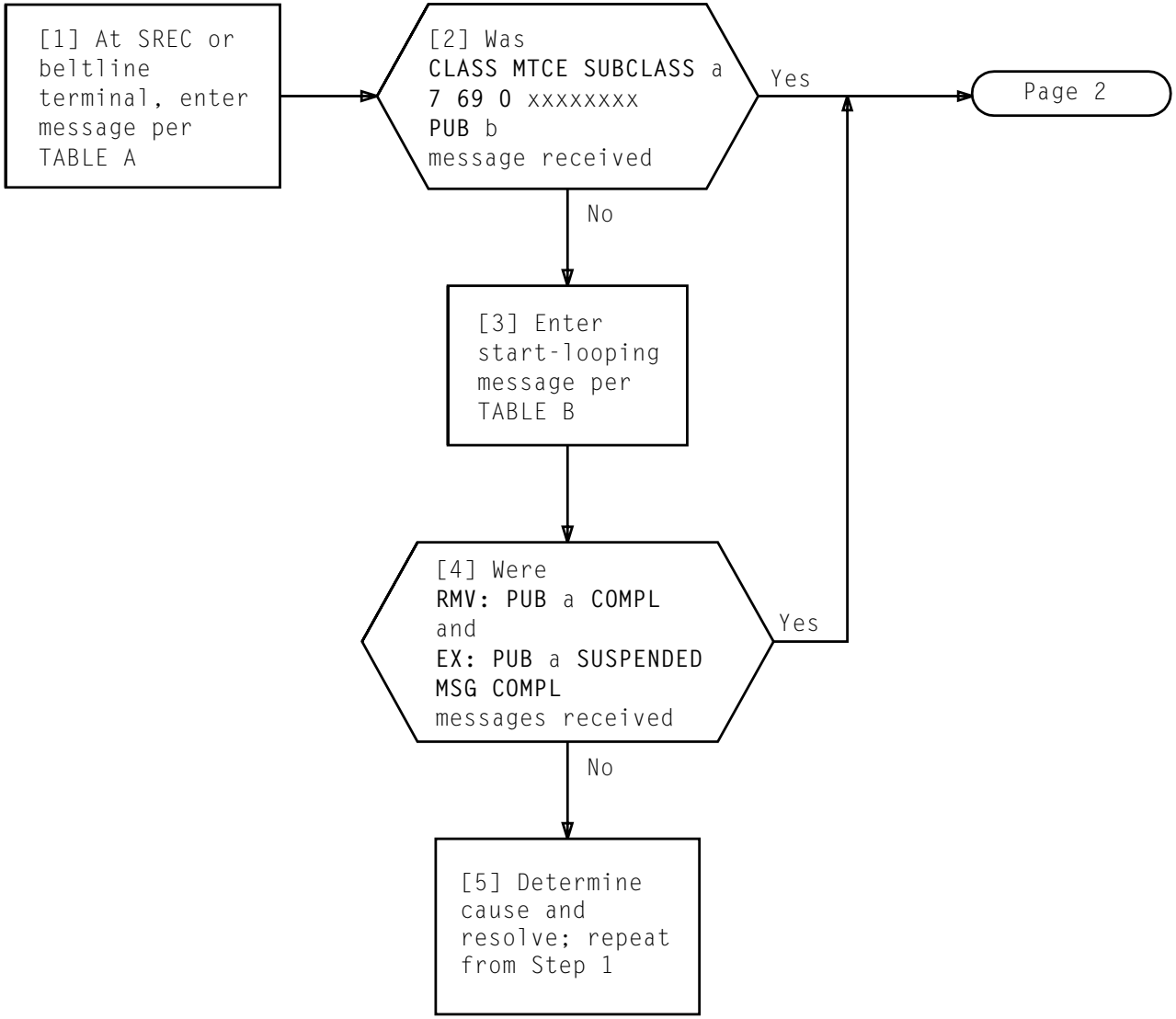


TABLE A

MESSAGE NUMBER	INPUT MESSAGE
1	OP:MACLI,CLASS MTCE!

TABLE B

MESSAGE NUMBER	INPUT MESSAGE
1	EX:PUB a;START!

a = bus 0 or 1

ADVANCE PROGRAM AND SET UP LOOP TO OBSERVE PU CONTROL BUS AND MISCELLANEOUS BUS BITS

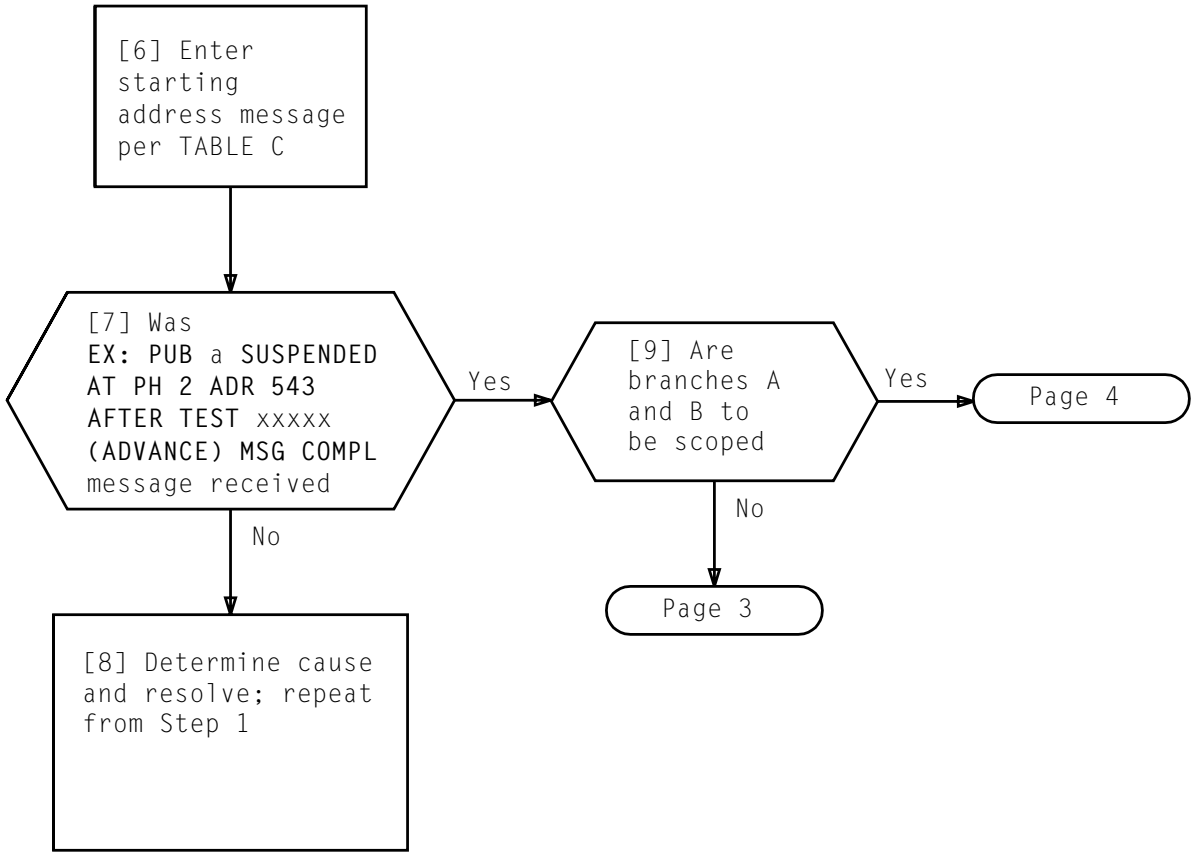


TABLE C	
MESSAGE NUMBER	**INPUT MESSAGE**
1	EX:PUB a:PH 2,ADR 543!
a = bus 0 or 1 543 = Address of statement label STM10600	

ADVANCE PROGRAM AND SET UP LOOP TO OBSERVE PU CONTROL BUS AND MISCELLANEOUS BUS BITS

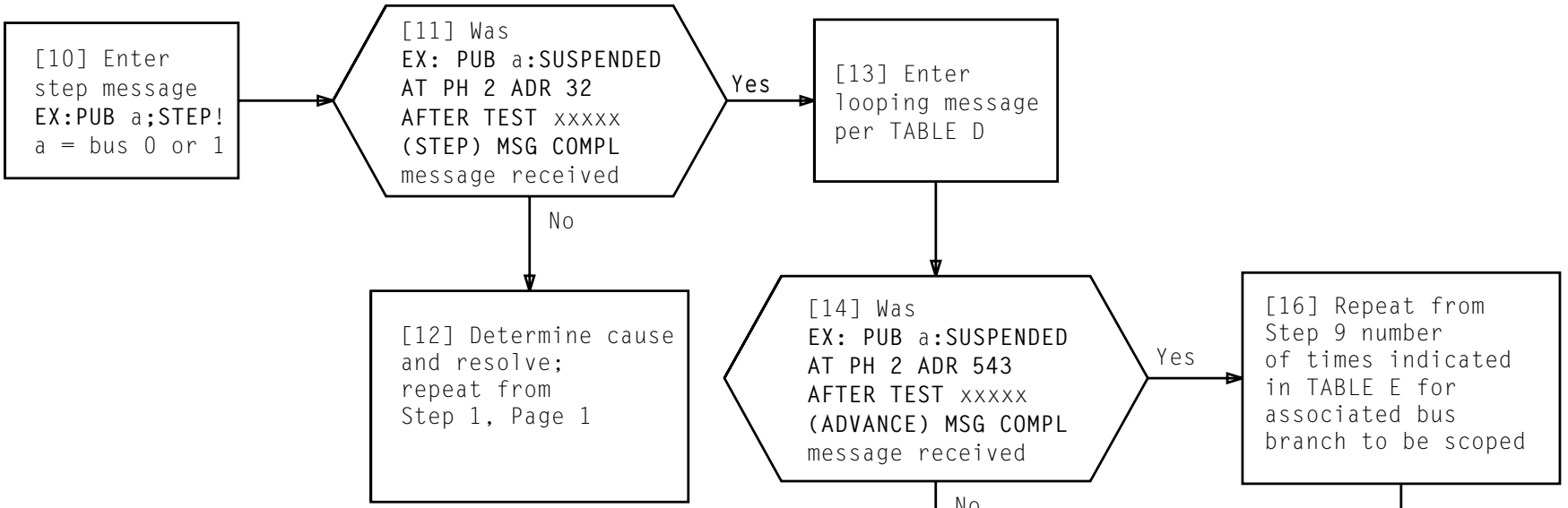


TABLE D	
MESSAGE NUMBER	INPUT MESSAGE
1	EX:PUB a:ADR 543!

a = bus 0 or 1
543 = Address of statement label STM10600

TABLE E	
BRANCHES	REPEAT NUMBER
C,D	0
E,F	1
G,H	2
K,L	3
M,R	4
T,V	5
W,X	6

ADVANCE PROGRAM AND SET UP LOOP TO OBSERVE PU CONTROL BUS AND MISCELLANEOUS BUS BITS

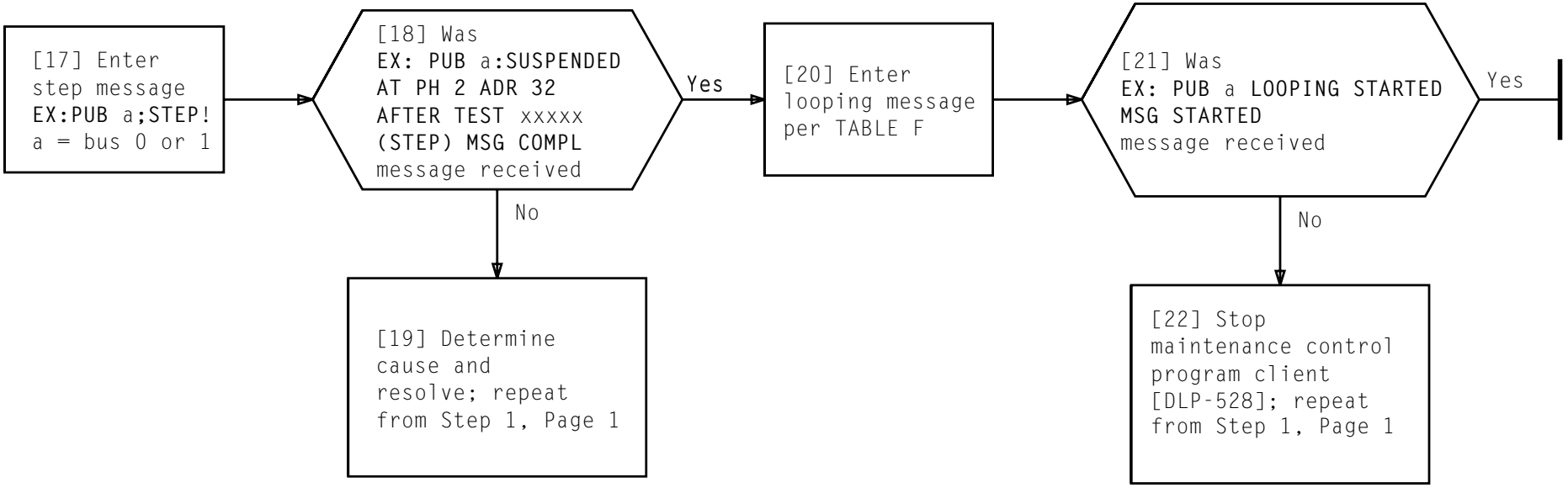


TABLE F

MESSAGE NUMBER	INPUT MESSAGE
1	EX:PUB a:ADR b-c!

a = bus 0 or 1
616 = Address of statement label PBTS4400
1675 = Address of statement label PBTS13800

ADVANCE PROGRAM AND SET UP LOOP TO OBSERVE PU CONTROL BUS AND MISCELLANEOUS BUS BITS

[1] Locate line in FIG. 1, 2, 3, 4, or 6, Pages 2, 3, 4, 5, and 6, respectively, that contains last frame where PU control bus and miscellaneous bus bits are terminated on bus branch to be scoped

[2] Assure that scope probes are wrapped around each other with positive lead connected to Channel 1 and negative lead connected to Channel 2 and that ground leads are attached together

[3] Scope P- and N-pins in dashed line box of connector 1, per FIG. 1, 3, 4, or 6, Pages 2, 4, 5, and 6, respectively, at connector location on line in Step 1. Observe oscilloscope waveform [FIG. 5, Page 5]. See NOTE 1. If problem occurs in seeing bit, use external trigger on scope and connect to trigger bit associated with faulty bit. See TABLE A and FIG. 1, 3, or 4, Pages 2, 4, and 5, respectively

[4] Scope P- and N-pins in each dashed line box of connectors 2 through 4, per FIG. 1, 2, 3, 4, or 6, Pages 2, 3, 4, 5, and 6, respectively, at connector locations on line in Step 1. Observe oscilloscope waveform [FIG. 5, Page 5]. See NOTE 1

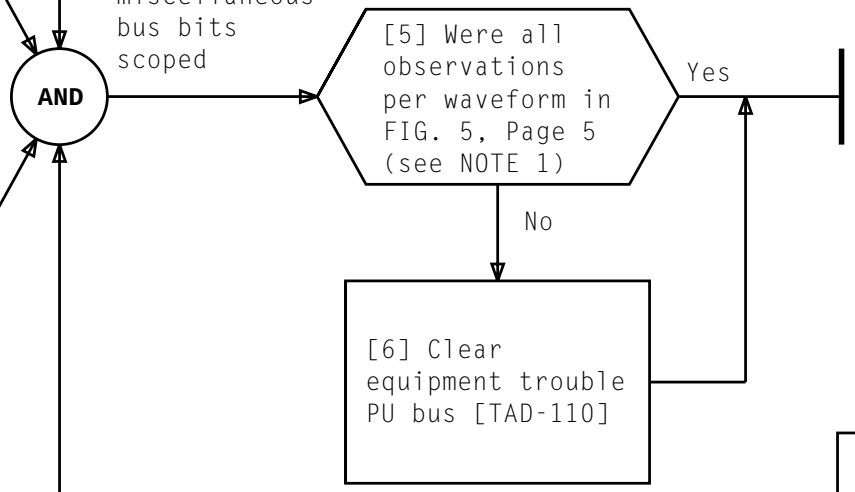
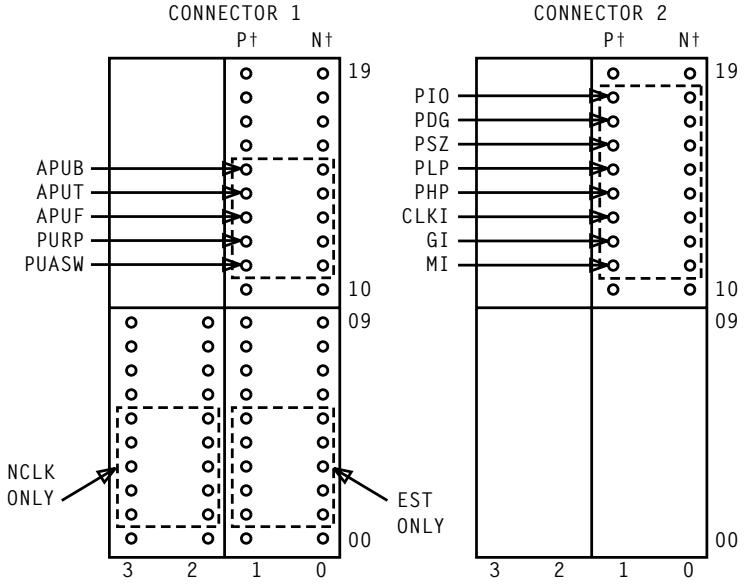


TABLE A	
FAULTY BIT	TRIGGER BIT
APUB	PSZ
APUF	CLKI
APUT	PLP
PUASW	MI
PURB	GI

NOTE 1
Pulse waveform will vary, depending on distance away from driver. Waveform measurements should be similar to examples shown in FIG. 5, Page 5

SCOPE PU CONTROL BUS AND MISCELLANEOUS BUS BITS

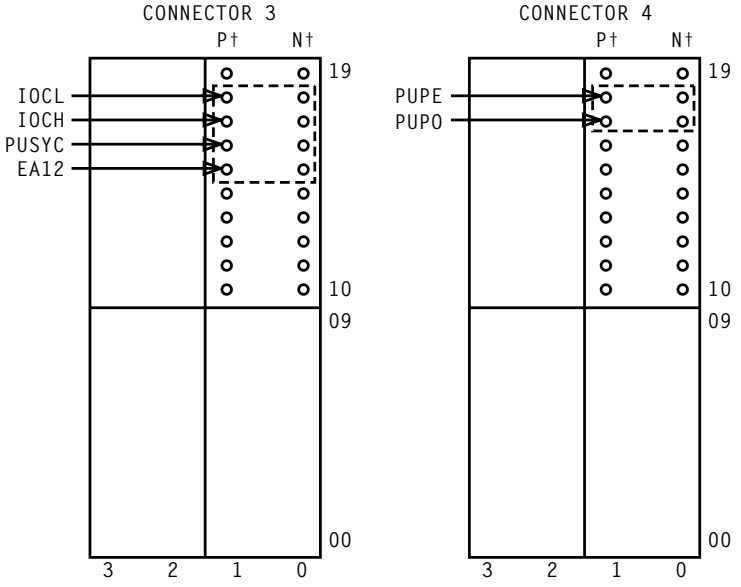


FRAME	CONNECTOR 1	CONNECTOR 2
CCIS	*80-30	*80-13
EST		
BUS 0	080-02	080-10
BUS 1	080-23	080-31
IO		
BUS 0	080-14	080-10
BUS 1	080-39	080-35
IOP		
BUS 0	080-39	080-29
BUS 1	076-39	076-29
NCLK	*60-48	*60-47
SP 1 (WITH D&SM FRAME)		
BUS 0	380-01	380-07
BUS 1	480-01	480-07
SP 1 (WITH COMBINED MATRIX FRAME)		
BUS 0	280-14	280-21
BUS 1	380-14	380-21
SP 2		
BUS 0	180-15	180-21
BUS 1	280-15	280-21
TMS A	*80-01	*80-07
TMS B		
BUS 0	‡76-14	‡76-21
BUS 1	‡80-14	‡80-21
TSIA-1	*80-33	*80-39
TSIA-2	*80-33	*80-40
TSIB	*80-37	*80-44
VIF		
BUS 0	152-12	152-09
BUS 1	152-22	152-27

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 1

SCOPE PU CONTROL BUS AND MISCELLANEOUS BUS BITS



FRAME	CONNECTOR 3	CONNECTOR 4
CCIS	*80-15	*80-18
EST		
BUS 0	080-11	080-13
BUS 1	080-32	080-34
IO		
BUS 0	080-09	080-07
BUS 1	080-34	080-32
IOP		
BUS 0	080-27	080-37
BUS 1	076-27	076-37
NCLK	*60-34	*60-36
SP 1 (WITH D&SM FRAME)		
BUS 0	380-08	380-10
BUS 1	480-08	480-10
SP 1 (WITH COMBINED MATRIX FRAME)		
BUS 0	280-23	280-26
BUS 1	380-23	380-26
SP 2		
BUS 0	180-22	180-24
BUS 1	280-22	280-24
TMS A	*80-08	*80-10
TMS B		
BUS 0	‡76-23	‡76-26
BUS 1	‡80-23	‡76-26
TSIA-1	*80-40	*80-42
TSIA-2	*80-42	*80-45
TS1B	*80-46	*80-49
VIF		
BUS 0	NONE	NONE
BUS 1	NONE	NONE

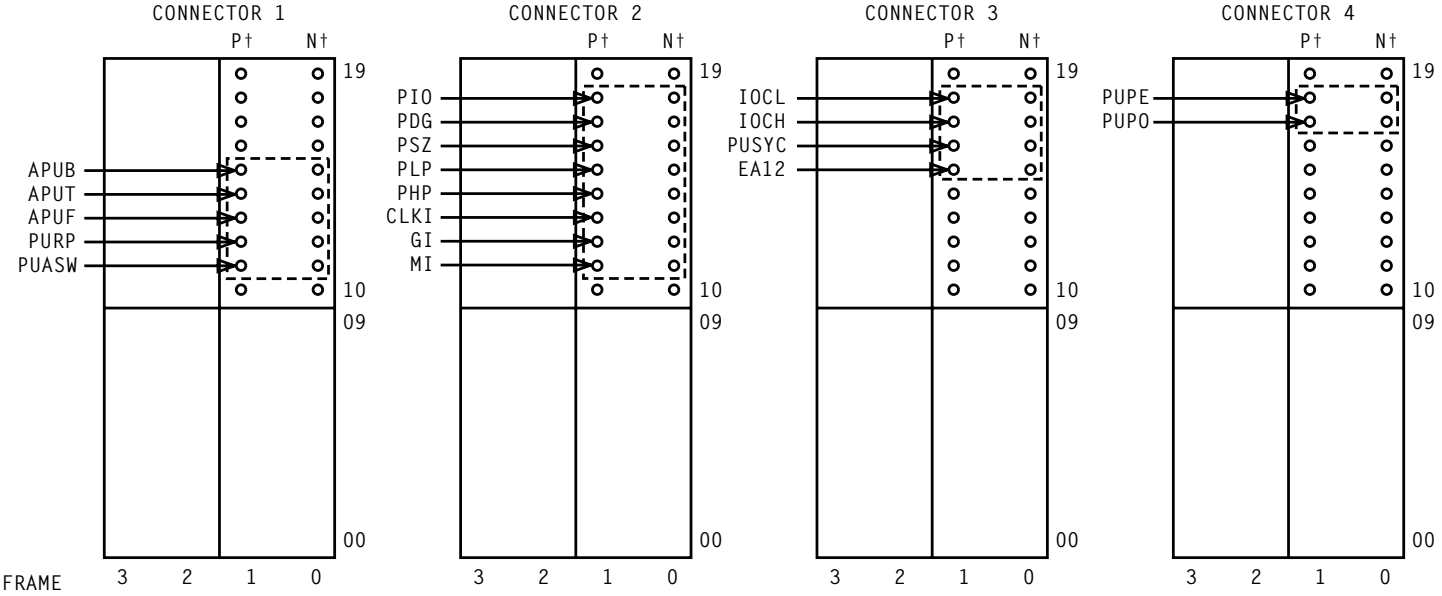
* 0 FOR BUS 0 OR 1 FOR BUS 1

† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 2

SCOPE PU CONTROL BUS AND MISCELLANEOUS BUS BITS

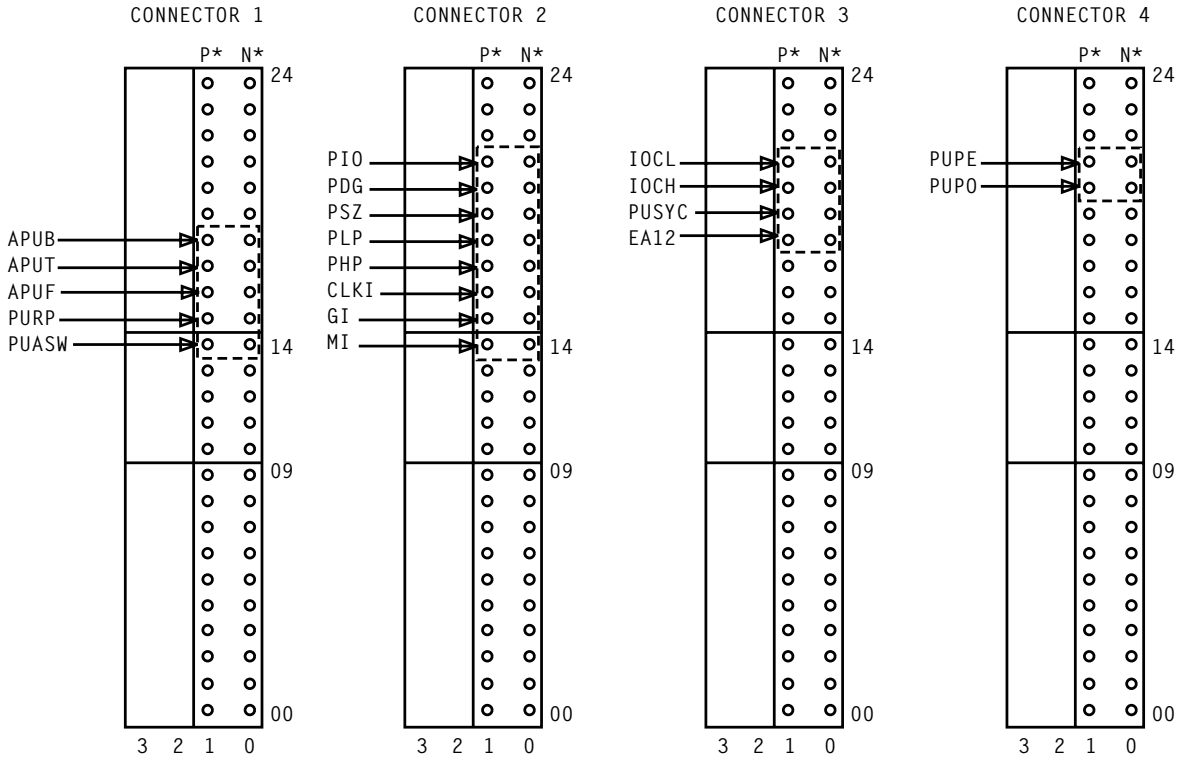


PUBB FRAME				
BRANCH A	*76-25	*76-31	*76-40	*76-09
BRANCH B	*72-27	*72-32	*72-38	*72-10
BRANCH C	*76-26	*76-33	*76-42	*76-11
BRANCH D	*72-28	*72-33	*72-39	*72-11
BRANCH E	*64-25	*64-31	*64-40	*64-09
BRANCH F	*60-27	*60-32	*60-38	*60-10
BRANCH G	*64-26	*64-33	*64-42	*64-11
BRANCH H	*60-28	*60-33	*60-39	*60-11
BRANCH K	*48-25	*48-31	*48-40	*48-09
BRANCH L	*44-27	*44-32	*44-38	*44-10
BRANCH M	*48-26	*48-33	*48-42	*48-11
BRANCH R	*44-28	*44-33	*44-39	*44-11
BRANCH T	*36-25	*36-31	*36-40	*36-09
BRANCH V	*32-27	*32-32	*32-38	*32-10
BRANCH W	*36-26	*36-33	*36-42	*36-11
BRANCH X	*32-28	*32-33	*32-39	*32-11

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 3

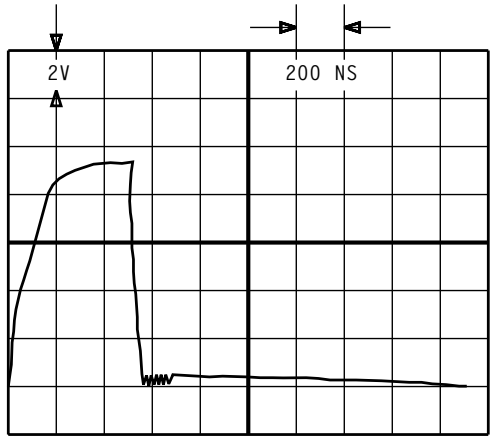
SCOPE PU CONTROL BUS AND MISCELLANEOUS BUS BITS



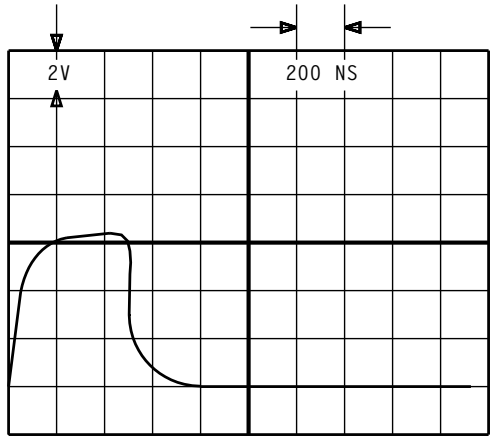
DIF or DIFE (24-31) (See Note.)				
BUS 0	180-023	180-067	180-073	180-085
BUS 1	180-171	180-215	180-221	180-233

* P FOR POSITIVE LEAD AND
  N FOR NEGATIVE LEAD

FIG. 4



NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 5

NOTE:
PHPB, PDGB, PLPB, and PSZB are expanded pollable bits.
For DIFE 24, these expanded pollable bits will not appear.
For DIFE 25-31, more testing of these bits is required (see DLP-525).

SCOPE PU CONTROL BUS AND MISCELLANEOUS BUS BITS

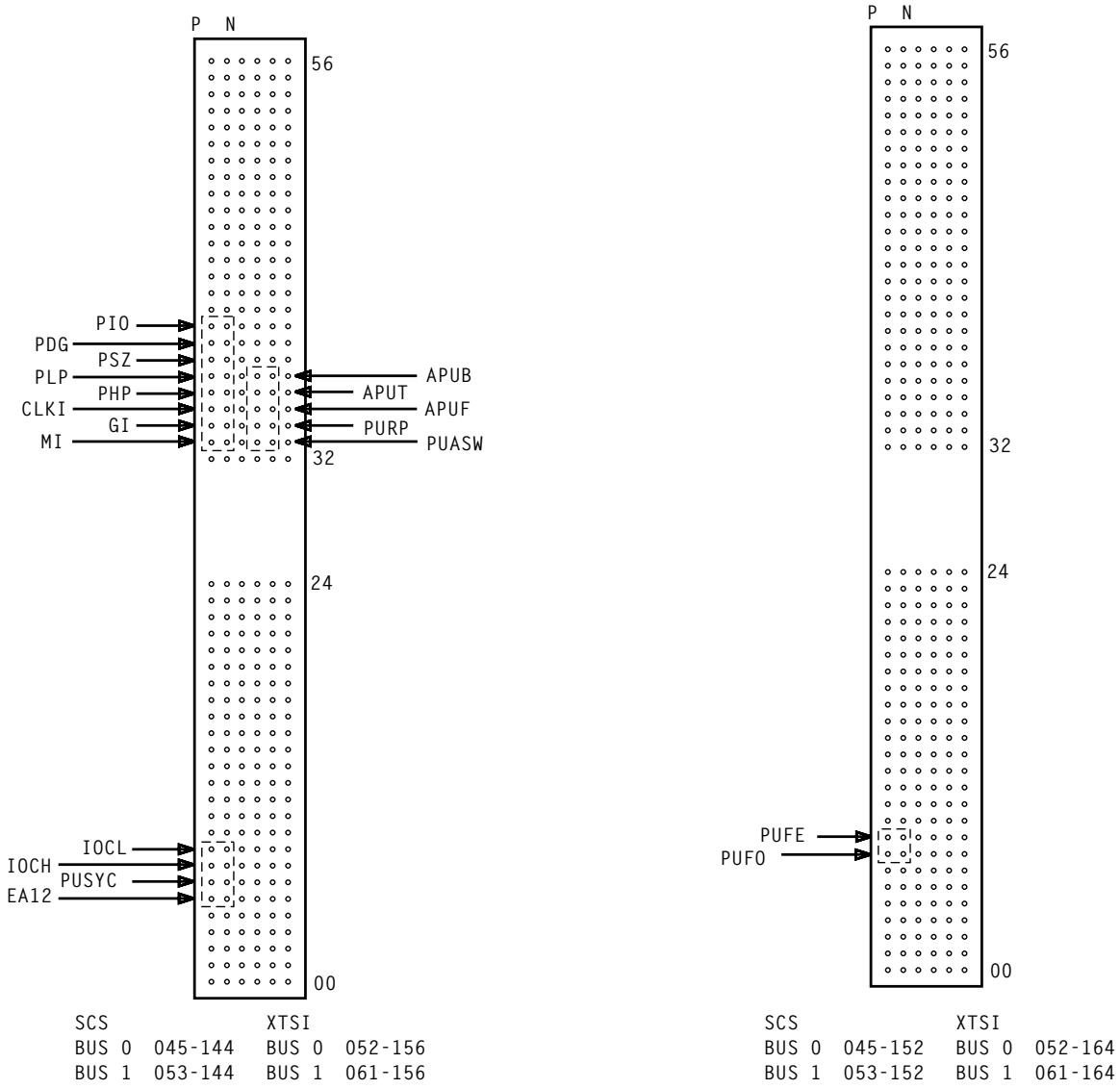


FIG. 6

SCOPE PU CONTROL BUS AND MISCELLANEOUS BUS BITS

[1] Locate line in FIG. 1, 2, 3 or 4, Pages 2, 3, and 4, that contains last frame where PU miscellaneous bus bits are terminated on bus branch to be scoped

[2] Assure that scope probes are wrapped around each other with positive lead connected to Channel 1 and negative lead connected to Channel 2 and that ground leads are attached together

[3] Scope P- and N-pins in each dashed line box, per FIG. 1, 2, or 3, Pages 2, 3, and 4, at connector locations on line in Step 1. Observe oscilloscope waveform [FIG. 4, Page 4]. See NOTE 1

AND

PU miscellaneous bus bits scoped

[4] Were all observations per waveform in FIG. 4, Page 4 (see NOTE 1)

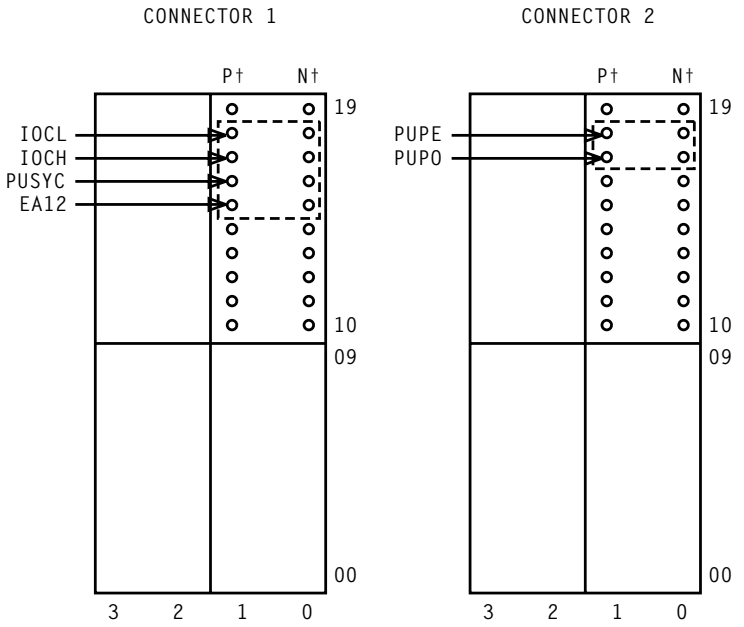
Yes

No

[5] Clear equipment trouble PU bus [TAD-110]

NOTE 1
Pulse waveform will vary, depending on distance away from driver. Waveform measurements should be similar to examples shown in FIG. 4, Page 4

SCOPE REMAINING PU MISCELLANEOUS BUS BITS NOT TERMINATED AT VIF

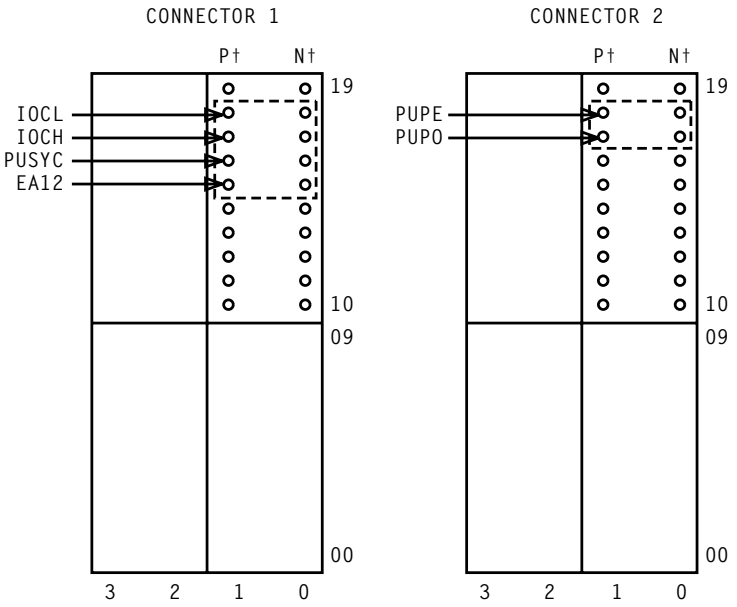


FRAME	CONNECTOR 1	CONNECTOR 2
CCIS	*80-15	*80-18
EST		
BUS 0	080-11	080-13
BUS 1	080-32	080-34
IO		
BUS 0	080-09	080-07
BUS 1	080-34	080-32
IOP		
BUS 0	080-27	080-37
BUS 1	076-27	076-37
NCLK	*60-34	*60-36
SP 1 (WITH D&SM FRAME)		
BUS 0	380-08	380-10
BUS 1	480-08	480-10
SP 1 (WITH COMBINED MATRIX FRAME)		
BUS 0	280-23	280-26
BUS 1	380-23	380-26
SP 2		
BUS 0	180-22	180-24
BUS 1	280-22	280-24
TMS A	*80-08	*80-10
TMS B		
BUS 0	‡76-23	‡76-26
BUS 1	‡80-23	‡80-26
TSIA-1	*80-40	*80-42
TSIA-2	*80-42	*80-45
TSIB	*80-46	*80-49

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD
‡ 0 FOR PUB TERMINATING AT TMS BAY 0 OR 1 FOR PUB TERMINATING AT TMS BAY 1

FIG. 1

SCOPE REMAINING PU MISCELLANEOUS BUS BITS NOT TERMINATED AT VIF

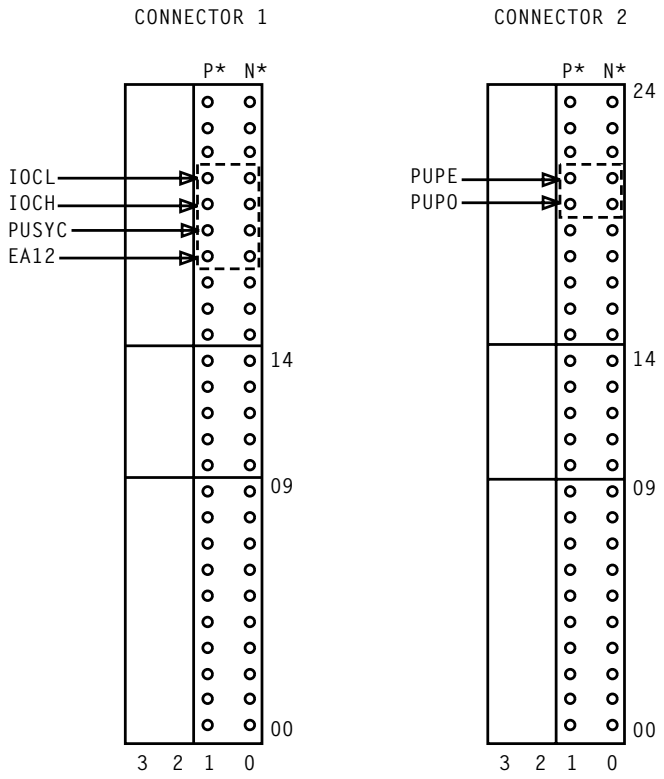


PUBB FRAME	CONNECTOR 1	CONNECTOR 2
BRANCH A	*76-40	*76-09
BRANCH B	*72-38	*72-10
BRANCH C	*76-42	*76-11
BRANCH D	*72-39	*72-11
BRANCH E	*64-40	*64-09
BRANCH F	*60-38	*60-10
BRANCH G	*64-42	*64-11
BRANCH H	*60-39	*60-11
BRANCH K	*48-40	*48-09
BRANCH L	*44-38	*44-10
BRANCH M	*48-42	*48-11
BRANCH R	*44-39	*44-11
BRANCH T	*36-40	*36-09
BRANCH V	*32-38	*32-10
BRANCH W	*36-42	*36-11
BRANCH X	*32-39	*32-11

* 0 FOR BUS 0 OR 1 FOR BUS 1
† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 2

SCOPE REMAINING PU MISCELLANEOUS BUS BITS NOT TERMINATED AT VIF

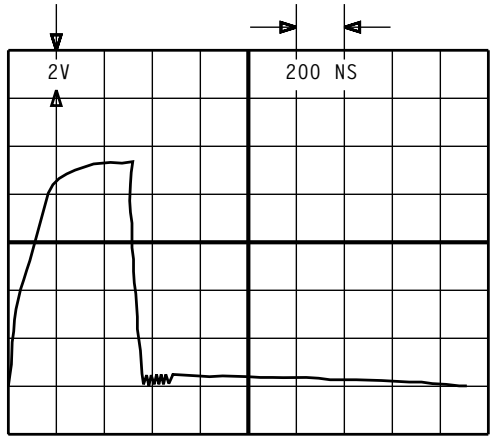


DIF or DIFE (24-31)

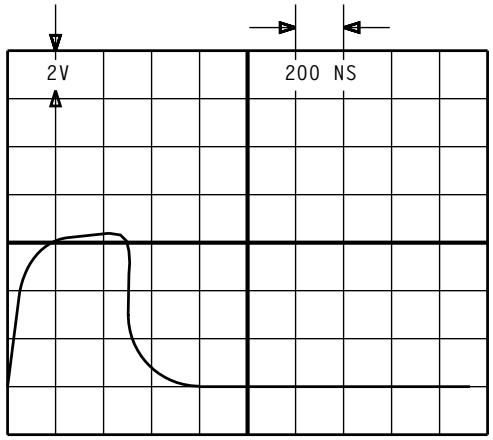
BUS 0	180-073	180-085
BUS 1	180-221	180-233

* P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

FIG. 3



NORMAL PULSE AT DRIVER

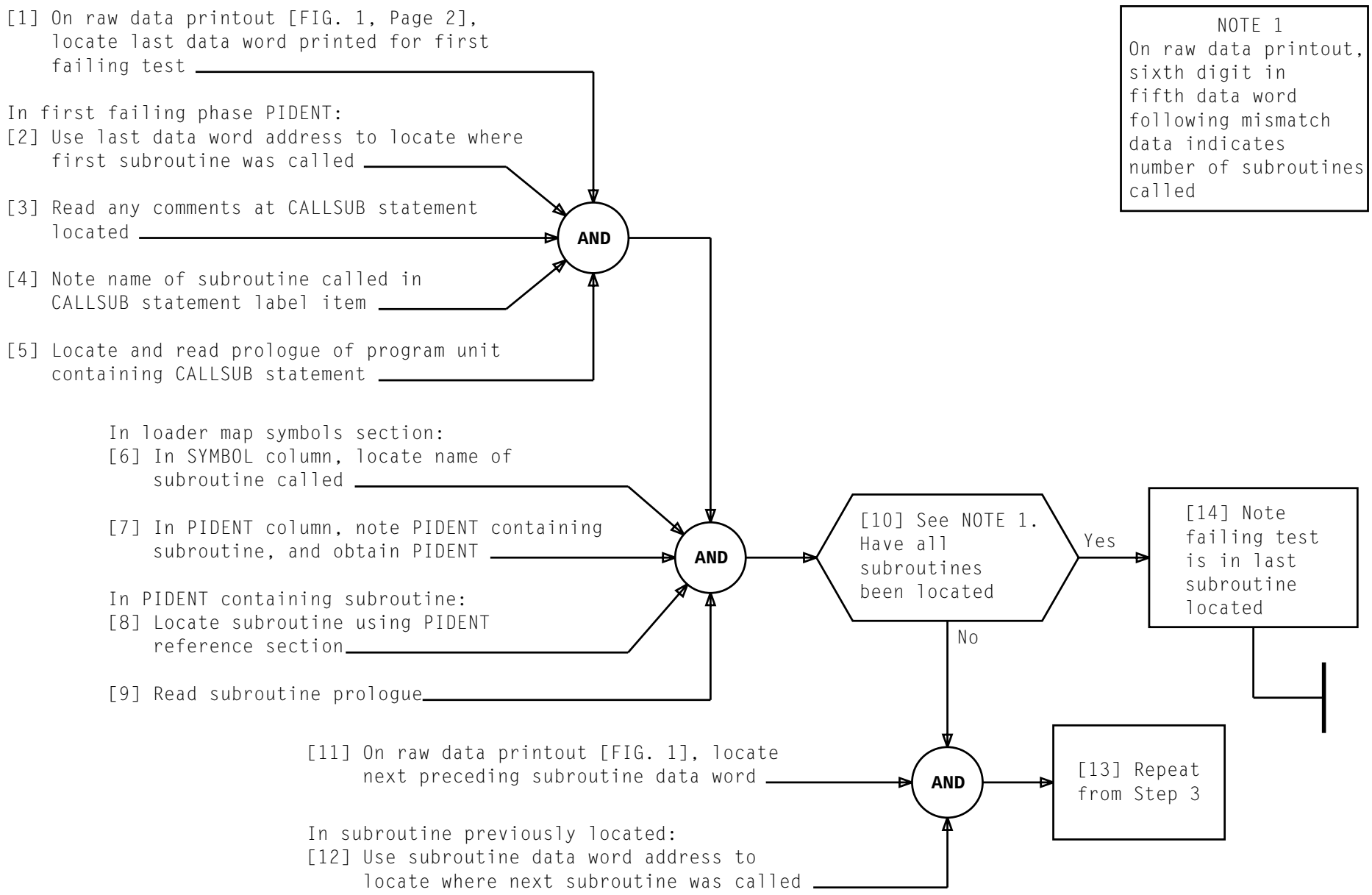


NORMAL PULSE 500 FEET FROM DRIVER

FIG. 4

SCOPE REMAINING PU MISCELLANEOUS BUS BITS NOT TERMINATED AT VIF

DETERMINE LOCATION AND FUNCTION OF SUBROUTINES CALLED



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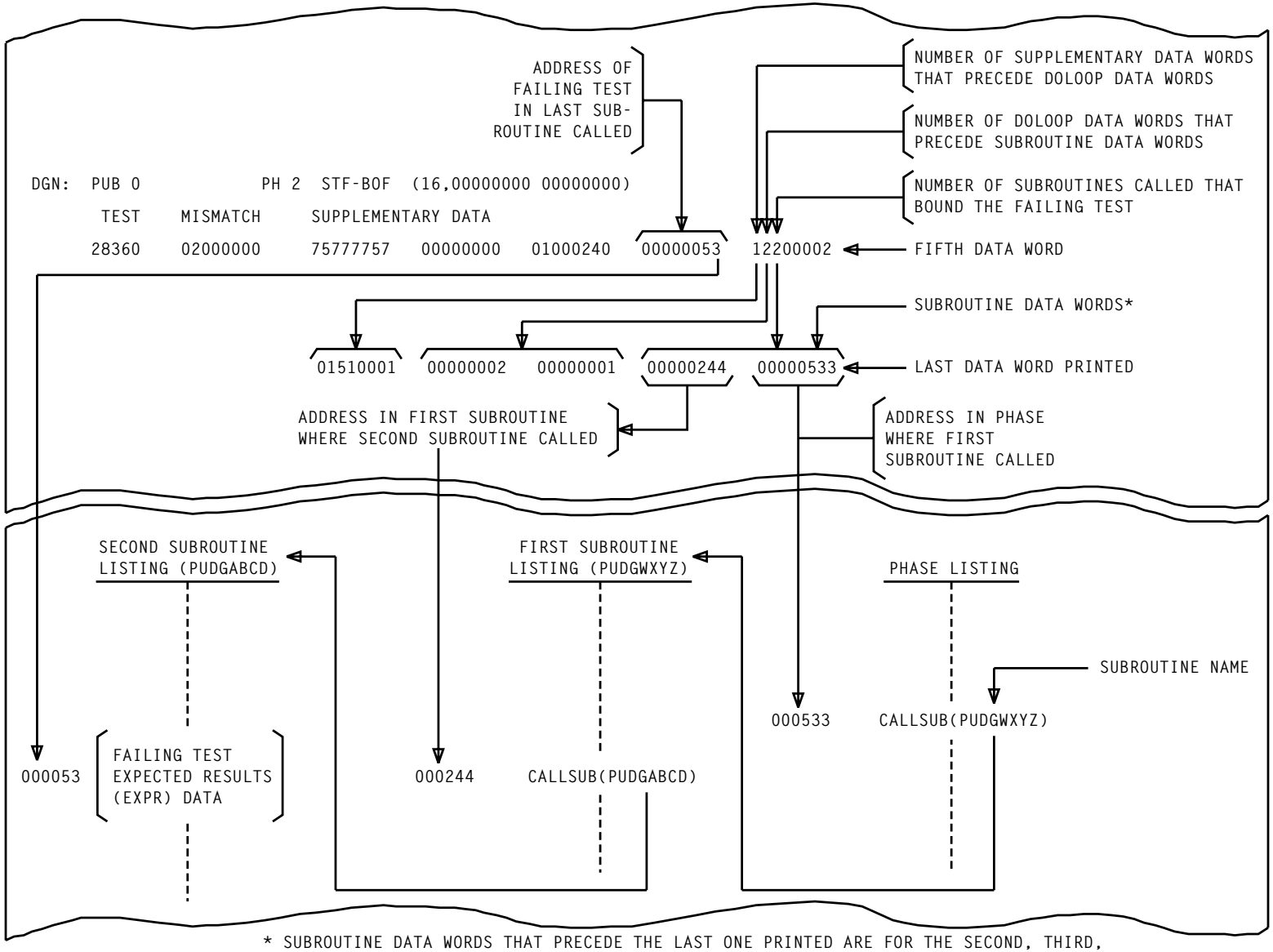


* SUBROUTINE DATA WORDS THAT PRECEDE THE LAST ONE PRINTED ARE FOR THE SECOND, THIRD, ETC., SUBROUTINES CALLED (RIGHT TO LEFT)

FIG. 1 — Relationship of Subroutine Data Words to Phase and Subroutine Listings

DETERMINE LOCATION AND FUNCTION OF SUBROUTINES CALLED

1. Read several DIAL statements just before failing test to determine what was occuring prior to test failing

   NOTE: Section 234-180-020 contains description of DIAL statements

2. Read failing test DIAL statement and any comments

3. Note "asterisk data" that follows failing test number in listing

4. Note relationship of asterisk line data to first five raw data words that follow mismatch data [FIG. 1]

5. In TABLE A, Page 2 locate failing DIAL statement and use description column to determine meaning of data contained in second and third raw data words following mismatch data

End of procedure

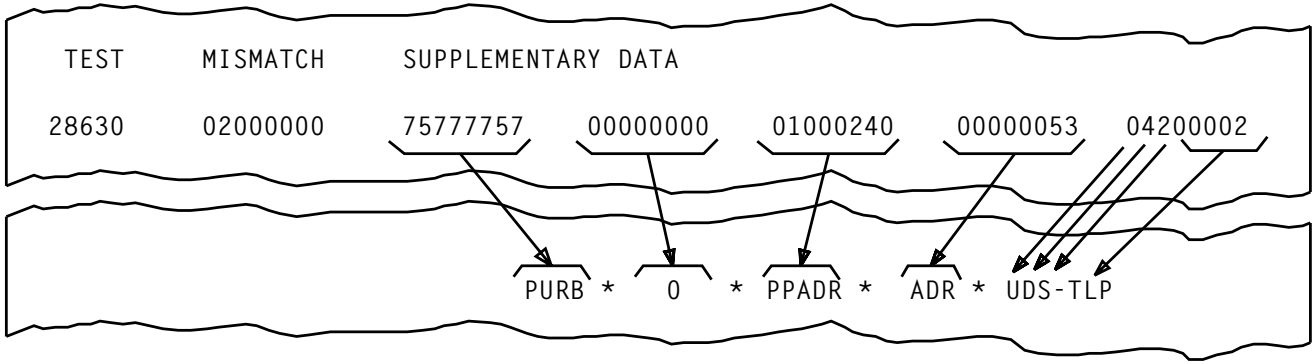


FIG. 1 — Example of Raw Data Printout Relationship to Asterisk Line at Failing Test

ANALYZE FAILING TEST DATA TO DETERMINE TEST FUNCTION

TABLE A
DESCRIPTION OF DATA CONTAINED IN SECOND AND THIRD DATA WORD FOR EACH TYPE DIAL TEST STATEMENT

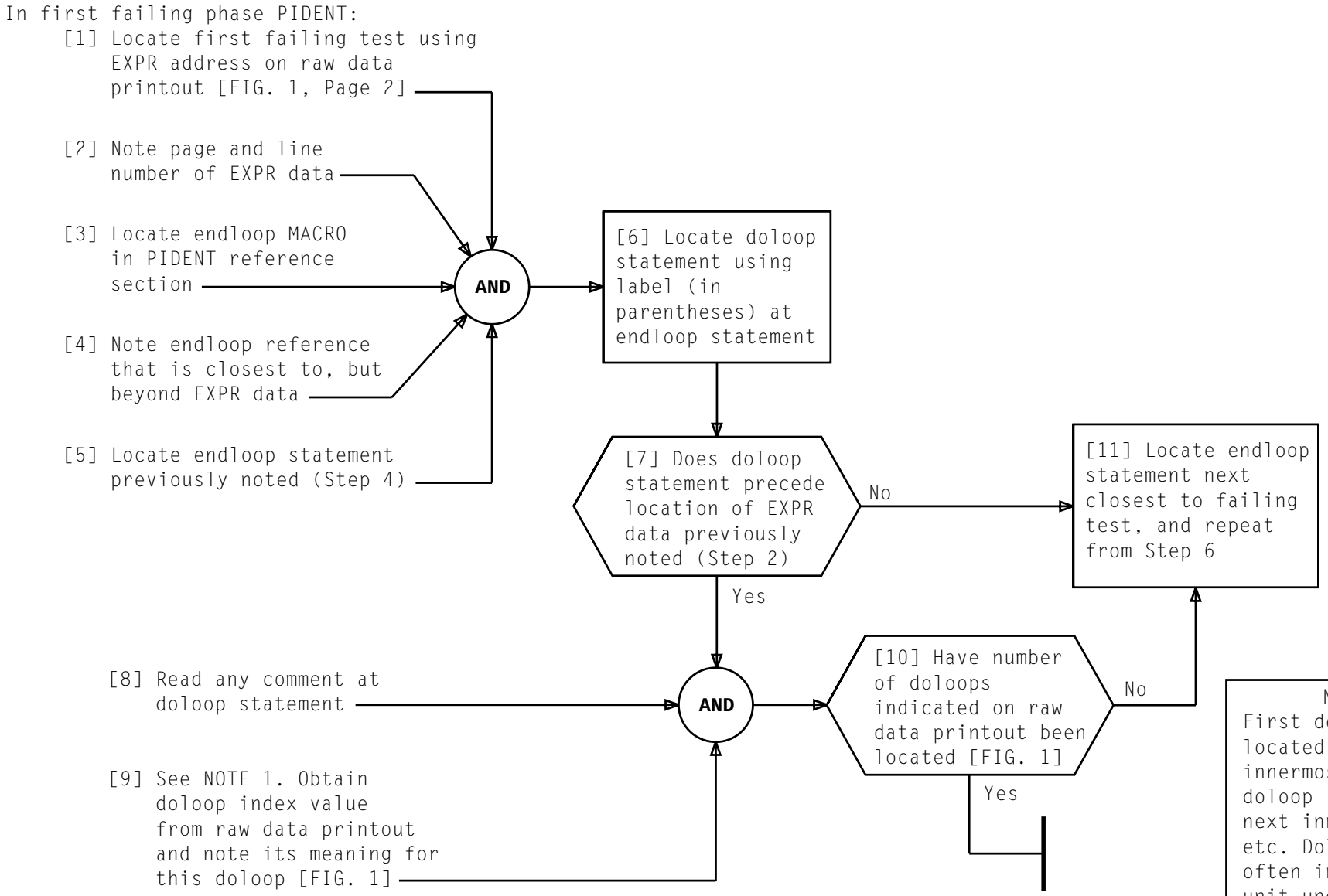
DIAL TEST STATEMENT	DESCRIPTION*
CCBB	A = B = 0, C = buffer bus address
CITOP CITOPI	Standard PUB format†
CLKOP	A = fault chain, B = reply bus C = CC pulse point address
MEMOPI	Standard PUB format† PUWB bits 16-10 = address of memory accessed PUWB bits 9-7 = memory level For time slot memories and busy-idle map Memories bit 0 = switching and permuting CKT
MTXMOP	Standard PUB format† PUWB bits 8-0 = matrix under test
PLOP	"MA" pulse point accessed by an SP: A (bits 11-2) = SP-K code B = SP OPCODE to bit pulse point 0/ (1640) C = address of point "MA" pulse point accessed by CC pulse point A = B = 0, C = CC pulse point address
PUDROP PUDROPI	Standard PUB format†
PULSE	A = B = 0, C = CC pulse point address
PLUSI	Same as PLOP statement
PUOP PUOPI	Standard PUB format†
PUOPBBR PUOPIBBR	PUOP part: standard PUB format† BBR part: A = B = 0, C = buffer bus address

DIAL TEST STATEMENT	DESCRIPTION*
SCANI	A (bits 11-2) = SP K-code B = SP OP code to read scan points 0/(1540) C = address of point
SDI	A (bits 11-2) = SP K-code B = SP OPCODE to read SD points 0/(1440) C = address of point
SESOP	Standard PUB format†
STORE	A = B = 0, C = specified expected result for VIC diagnostic, B = VIC failing test
TMSOP TMSOPI	Standard PUB format† PUWB bits 16-10 = address of memory accessed
TSIESR	Standard PUB format† except C = do not care
TSIMOP	Same as MEMOPI statement

*The following format relates A, B, and C to the second and third data words following mismatch data:

SECOND WORD	THIRD WORD
AAAABBBB	CCCCCCCC

†The standard PUB format is:
A = PUEA/PUAB
B = PUWB (bits 35-24) = OPAD, (bits 35-29) = OPCODE
C = PUWB (bits 23-0) = ADDRESS



NOTE 1
First doloop located is innermost, next doloop located is next innermost, etc. Doloop values often indicate unit under test, memory, etc.

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DETERMINE LOCATION AND FUNCTION OF DOLOOPS, NO SUBROUTINES CALLED

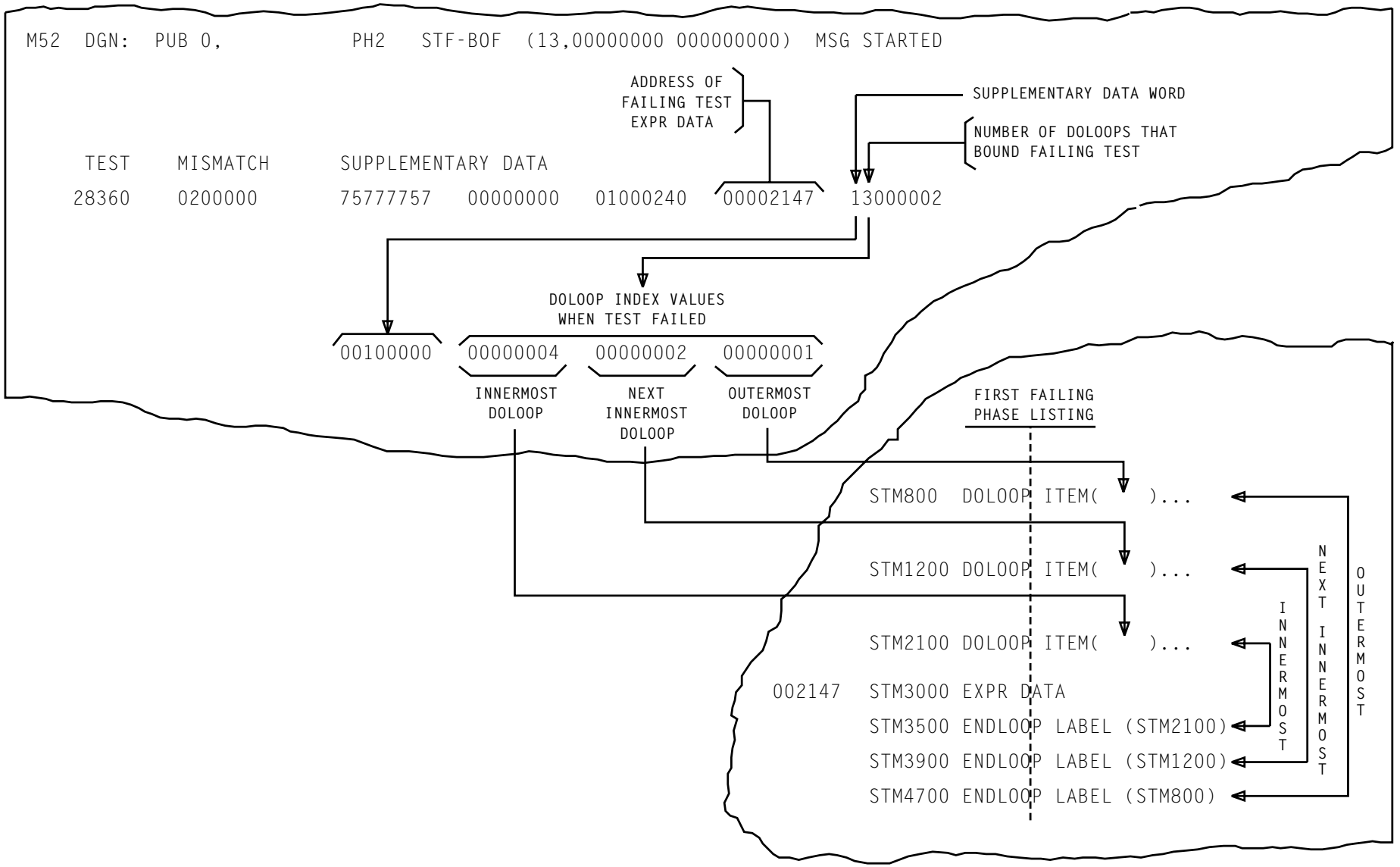
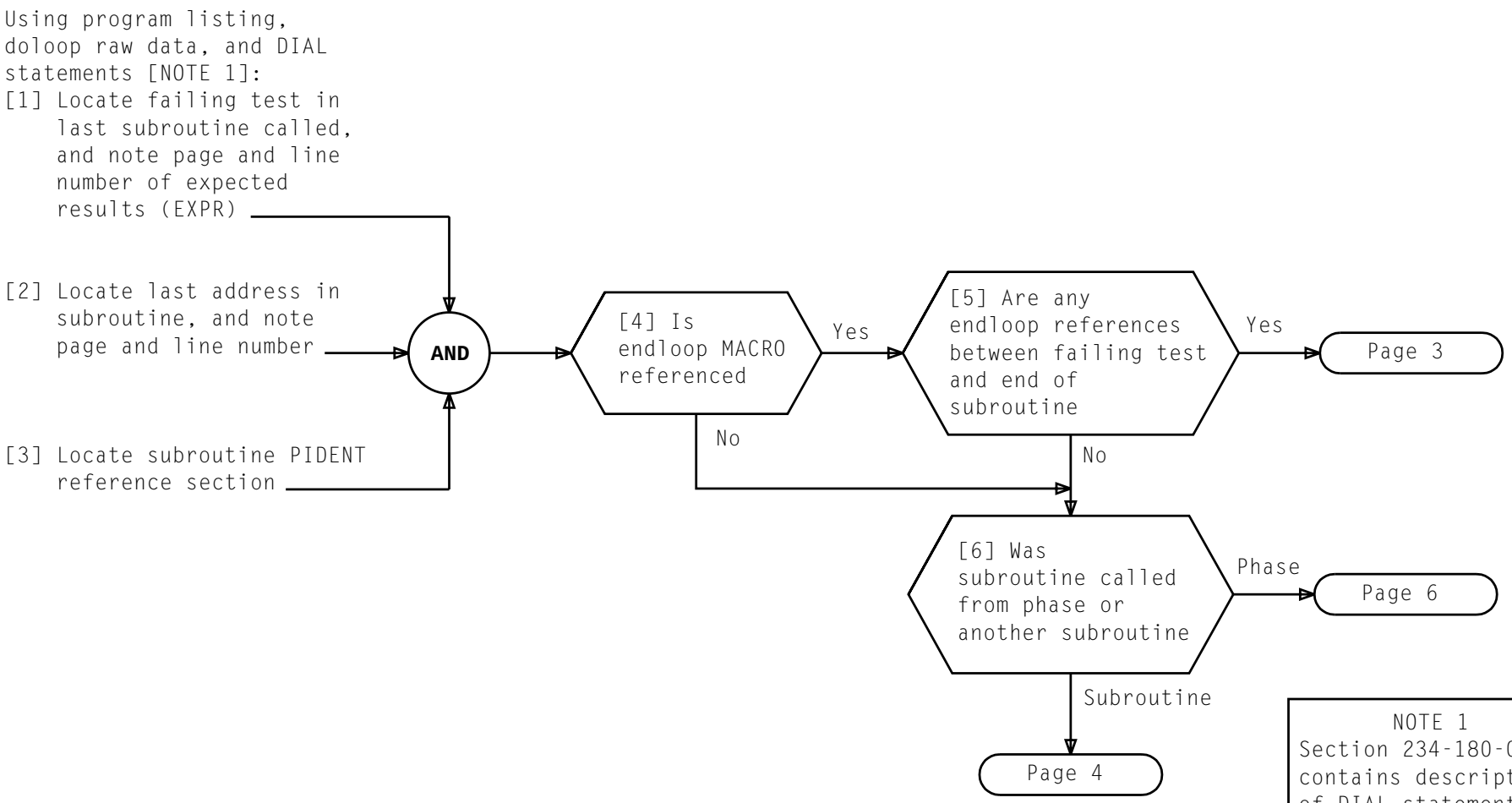


FIG. 1 – Example of Raw Data Doloop Word Relationship to Phase Listing

DETERMINE LOCATION AND FUNCTION OF DOLOOPS, NO SUBROUTINES CALLED

SUMMARY

Using program listing, doloop raw data, and DIAL statements, locate failing test in last subroutine called. Look PAST failing test for endloop statements. For each endloop statement located in subroutine, use endloop label variable to identify location of associated doloop statements. Locate each doloop statement. Obtain doloop index values from raw data printout and determine meaning for each doloop. If endloop statement was not found in subroutine, go to where subroutine was called and look for endloop statements after CALLSUB statement. Continue to look for endloop statements after CALLSUB statements until all doloops indicated on raw data printout for first failing test are located. Read any comments at doloop statements



NOTE 1
Section 234-180-020 contains description of DIAL statements

DETERMINE LOCATION AND FUNCTION OF DOLOOPS, SUBROUTINES CALLED

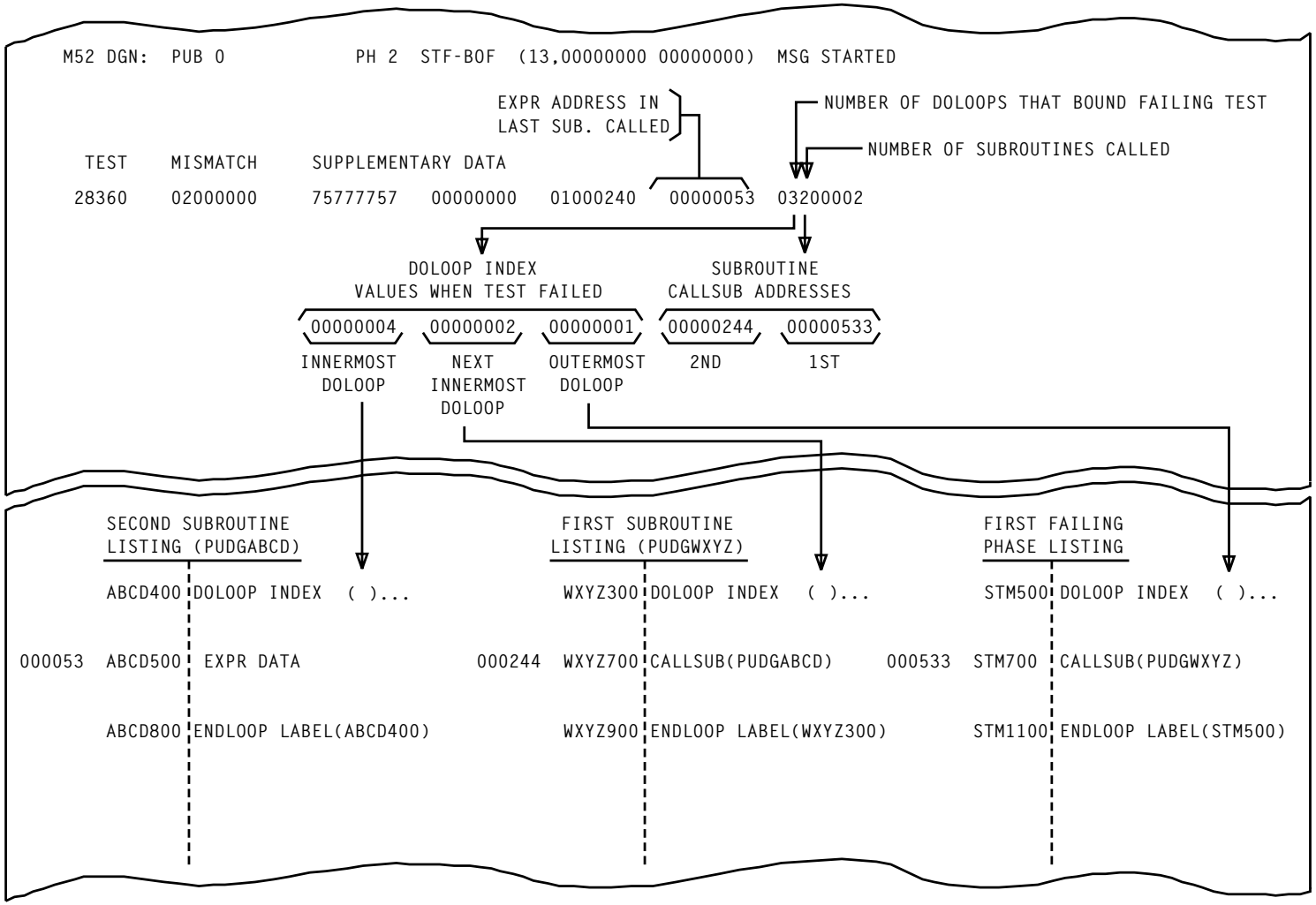
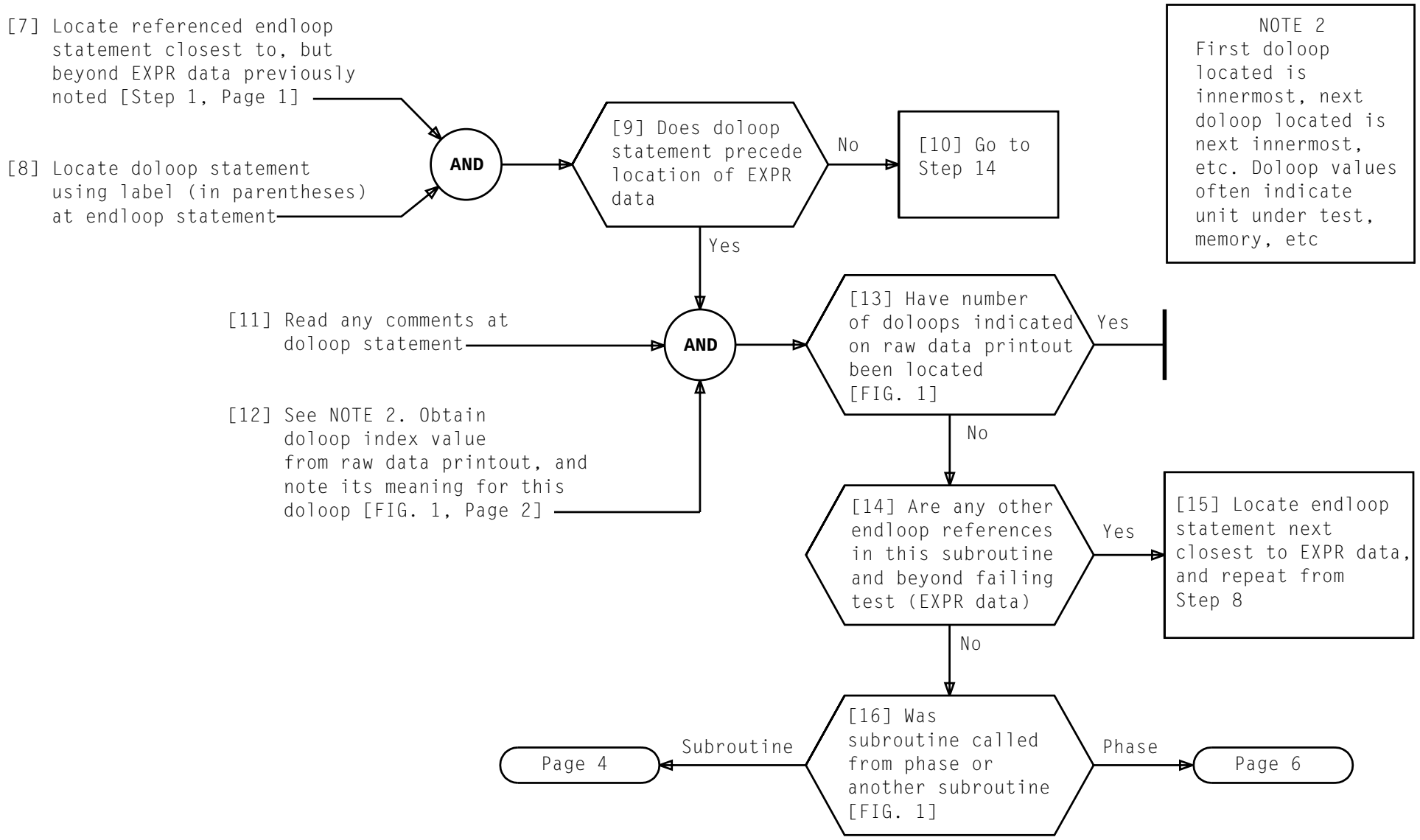
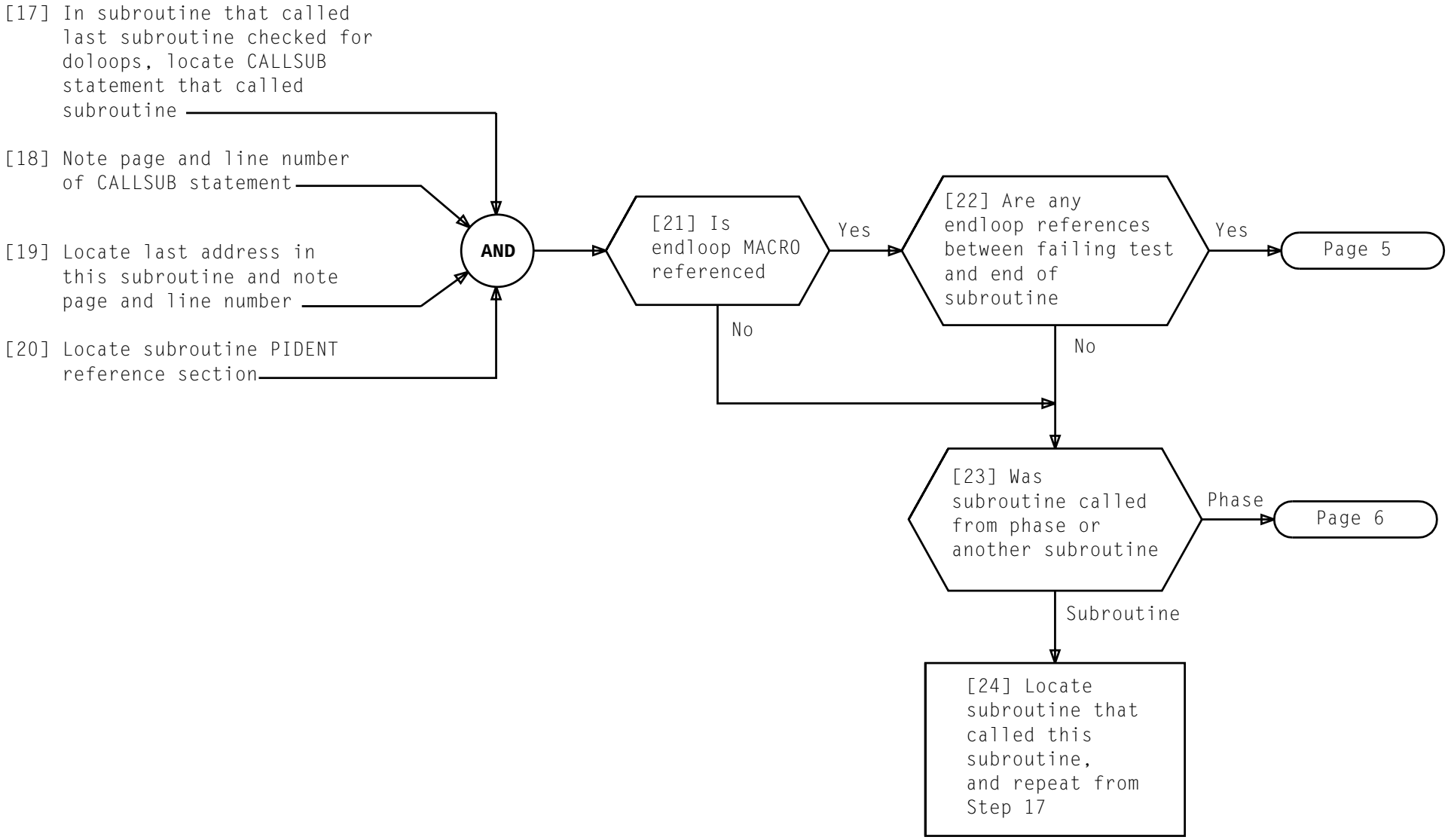


FIG. 1 – Example of Doloop Raw Data Relationship to Listings When Subroutines Called

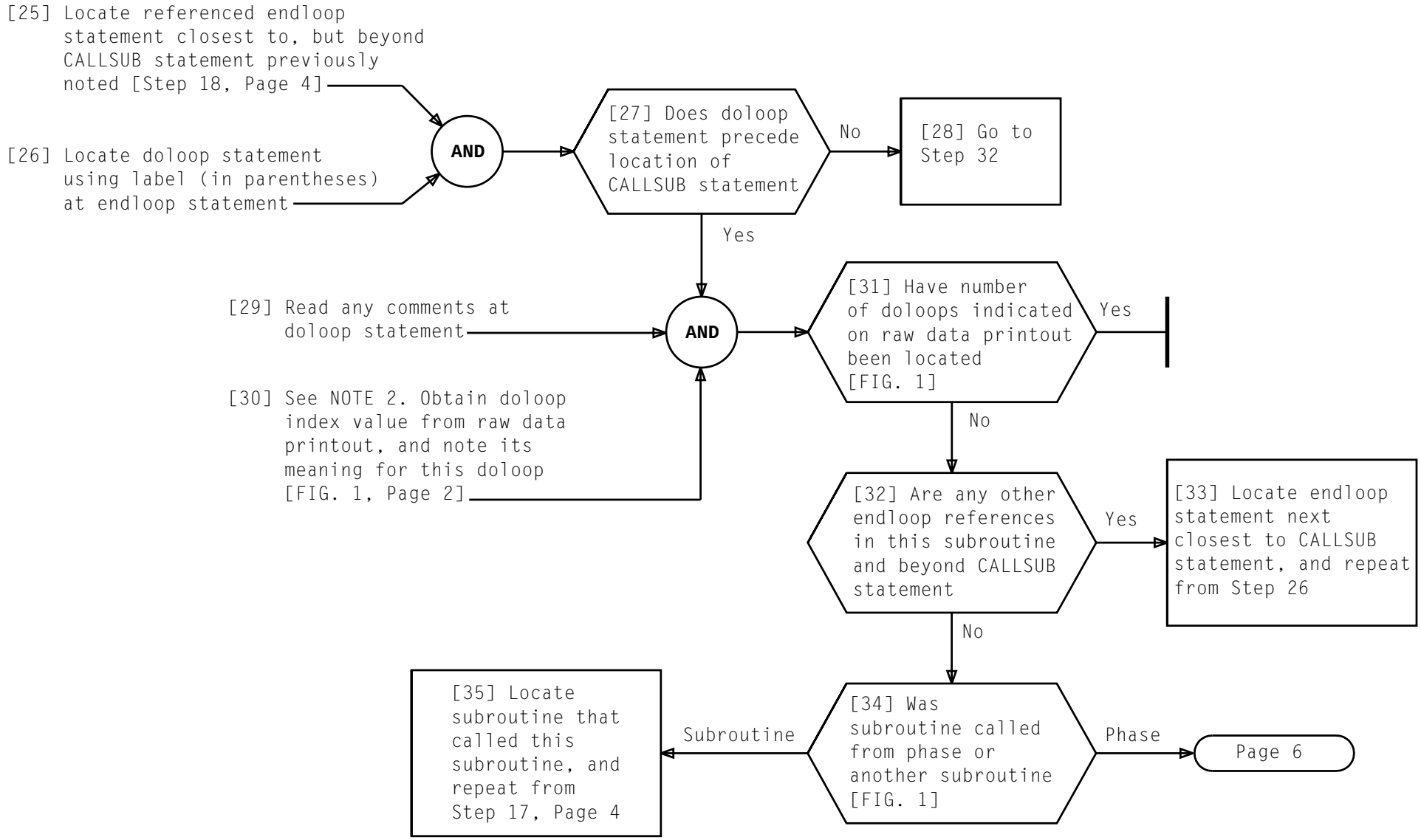
DETERMINE LOCATION AND FUNCTION OF DOLOOPS, SUBROUTINES CALLED



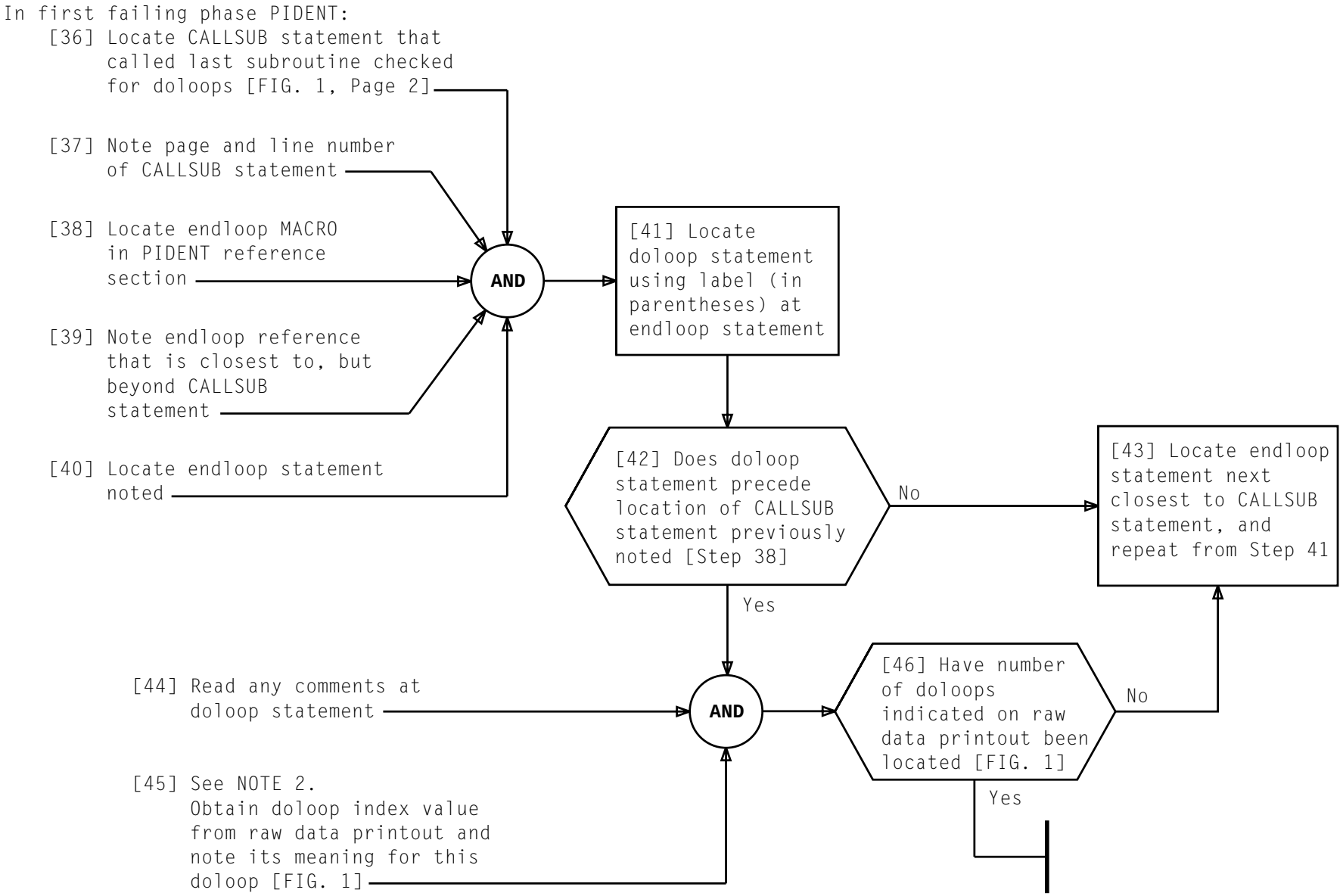
DETERMINE LOCATION AND FUNCTION OF DOLOOPS, SUBROUTINES CALLED



DETERMINE LOCATION AND FUNCTION OF DOLOOPS, SUBROUTINES CALLED



DETERMINE LOCATION AND FUNCTION OF DOLOOPS, SUBROUTINES CALLED



DETERMINE LOCATION AND FUNCTION OF DOLOOPS, SUBROUTINES CALLED

On Summary Data Printout [FIG. 1, Page 2]:

1. Note monitor point address on first CD line under **V1** column

2. Convert octal failing bit in leftmost four octal digits of word under adjacent **V2** column to decimal

   NOTE: Negative addresses for example, 77771510 precede positive addresses in PK. If address is not found, other addresses and bits may be investigated using other V column pairs (first CD line or other CD lines). The PK data for these addresses will be further removed from fault and PR data may be of greater value.

In Test Access PK Document:

3. Find address and failing bit

4. Note pack type and gate name for failing bit

In CPS for Pack Type:

5. Locate component list section

   NOTE: If A or B appears after gate name in test access PK, it indicates A or B half of register (gate)

6. Look in each DESIG column for gate name

7. In adjacent SH LOC column, use location indicated to find gate in CPS

   NOTE: If A or B appears after gate name in test access PK, it indicates A or B half of register (gate)

8. See NOTE 2. At gate, note lead name and terminal leaving gate to outside pack [FIG. 2, Page 2]

In Test Access PK Document:

9. For failing bit, note FS, SD, and symbol name

In SD FS indicated:

10. Locate symbol number having same symbol name as indicated in Test Access PK for failing bit

11. Find lead interconnection section for this symbol

12. Using terminal and lead name noted, find corresponding SD lead name

End of procedure

IDENTIFY LEAD IN PATH OF FAILING BIT USING SUMMARY DATA PRINTOUT AND TEST ACCESS PK DOCUMENT

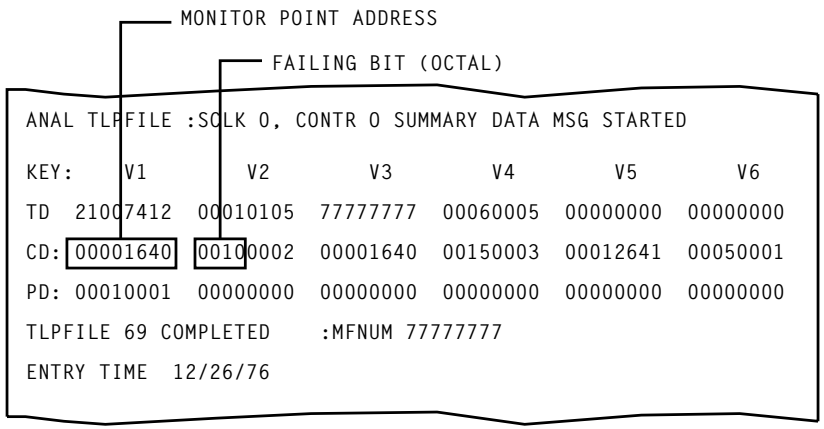


FIG. 1 — Example of Summary Data Printout

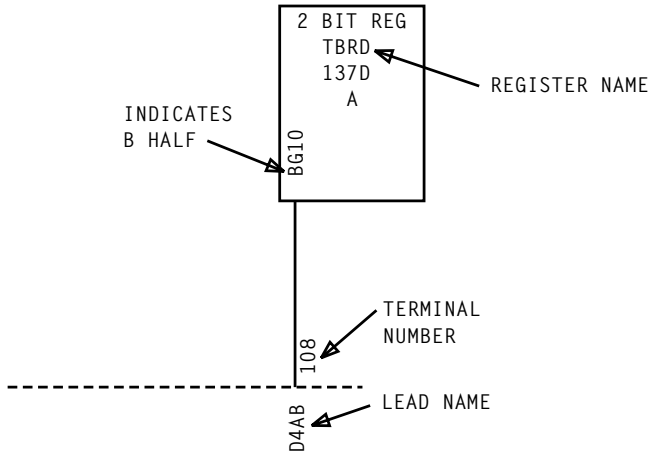


FIG. 2 — Example of Lead Leaving B Half of CPS Register

IDENTIFY LEAD IN PATH OF FAILING BIT USING SUMMARY DATA PRINTOUT AND TEST ACCESS PK DOCUMENT

1. Define error using PMDs [TABLE A]

End of procedure

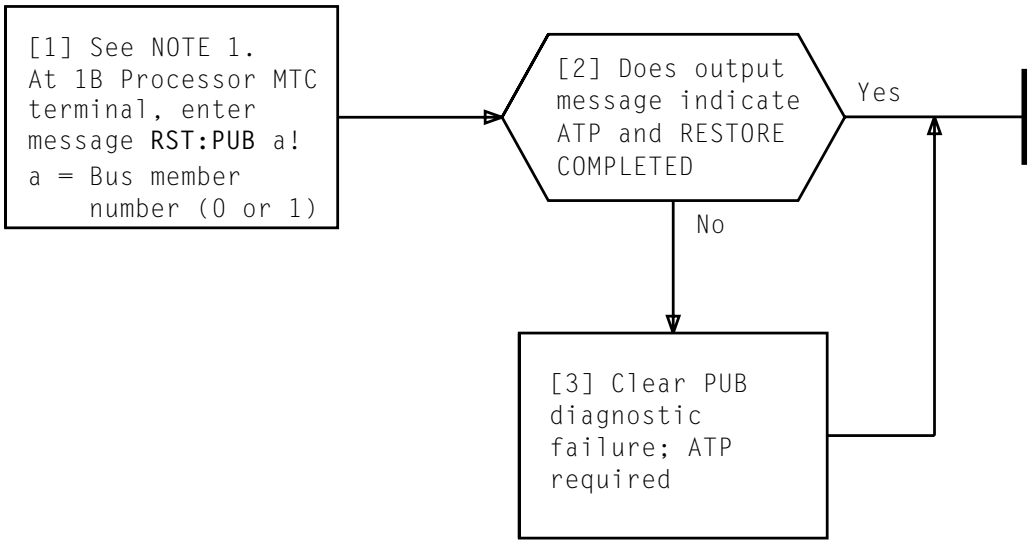
TABLE A

PMD-1	Growth unit
PMD-2	Soft error configuration was duplex controllers
PMD-3	Soft error configuration was simplex controller 0
PMD-4	Soft error configuration was simplex controller 1
PMD-5	Transient error configuration was duplex controllers
PMD-6	Transient error configuration was simplex controller 0
PMD-7	Transient error configuration was simplex controller 1
PMD-10	Bus at unit fault configuration was duplex controllers; duplex bus controller 0 and minor bus (IPUB) 0 suspect
PMD-11	Bus at unit fault configuration was duplex controllers; duplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-12	Bus at unit fault configuration was duplex controllers; duplex bus controller 1 and minor bus (IPUB) 0 suspect
PMD-13	Bus at unit fault configuration was duplex controllers; duplex bus controller 1 and minor bus (IPUB) 1 suspect
PMD-14	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 0 suspect
PMD-15	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-16	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-17	Bus at unit fault configuration was duplex controllers; simplex bus controller 1 and minor bus (IPUB) 0 suspect
PMD-20	Bus at unit fault configuration was simplex controllers; duplex bus controller 0 and minor bus (IPUB) 0 suspect
PMD-21	Bus at unit fault configuration was simplex controllers; duplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-22	Bus at unit fault configuration was simplex controllers; duplex bus controller 1 and minor bus (IPUB) 0 suspect
PMD-23	Bus at unit fault configuration was simplex controllers; duplex bus controller 1 and minor bus (IPUB) 1 suspect
PMD-24	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 0 and minor bus (IPUB) 0 suspect
PMD-25	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 0 and minor bus (IPUB) 1 suspect
PMD-26	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 1 and minor bus (IPUB) 0 suspect
PMD-27	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 1 and minor bus (IPUB) 1 suspect
PMD-30	PUB fault configuration was duplex; bus major bus 0 suspect
PMD-31	PUB fault configuration was duplex; bus major bus 1 suspect
PMD-32	PUB fault configuration was simplex; bus major bus 0 suspect

DEFINE PMD DICTIONARY NODES, PBFR

TABLE A (Contd)

PMD-33	PUB fault configuration was simplex; bus major bus 1 suspect
PMD-34	Controller fault configuration was duplex controllers; controller 0 suspect
PMD-35	Controller fault configuration was duplex controllers; controller 1 suspect
PMD-36	Controller fault configuration was simplex controllers; controller 0 suspect
PMD-37	Controller fault configuration was simplex controllers; controller 1 suspect
PMD-40	Controller fault configuration was simplex controller; bus suspect undetermined
PMD-41	Controller fault configuration was simplex controller; bus suspect undetermined
PMD-42	Controller fault configuration was duplex controllers; controller 0 suspect, but not conclusively. Sequence table will try to remove and diagnose mate controller on subsequent interrupts if they occur
PMD-43	Controller fault configuration was duplex controllers; controller 1 suspect, but not conclusively. Sequence table will try to remove and diagnose mate controller on subsequent interrupts if they occur
PMD-44	CC fault suspect active CC 0
PMD-45	CC fault suspect active CC 1
PMD-46	CC fault suspect stand-by CC 0
PMD-47	CC fault suspect stand-by CC 1
PMD-50	Interrupt from duplex failed unit
PMD-51	No unit found; PBFR could not identify a unit that was responsible for the interrupt or interject
PMD-52	System clock controller fault configuration was simplex system clock controllers; controller 0 suspect
PMD-53	System clock controller fault configuration was simplex system clock controllers; controller 1 suspect
PMD-54	System clock controller fault configuration was simplex system clock controller; and bus suspect undetermined
PMD-55	System clock controller fault configuration was simplex system clock controller; and bus suspect undetermined
PMD-56	System clock soft error configuration was simplex system clock controllers; controller 0 suspect
PMD-57	System clock soft error configuration was simplex system clock controllers; controller 1 suspect
PMD-60	System clock transient error configuration was simplex system clock controllers; controller 0 suspect
PMD-61	System clock transient error configuration was simplex system clock controllers; controller 1 suspect



NOTE 1
Restore message will cause PUB diagnostic to be run. PUB will be restored if ATP

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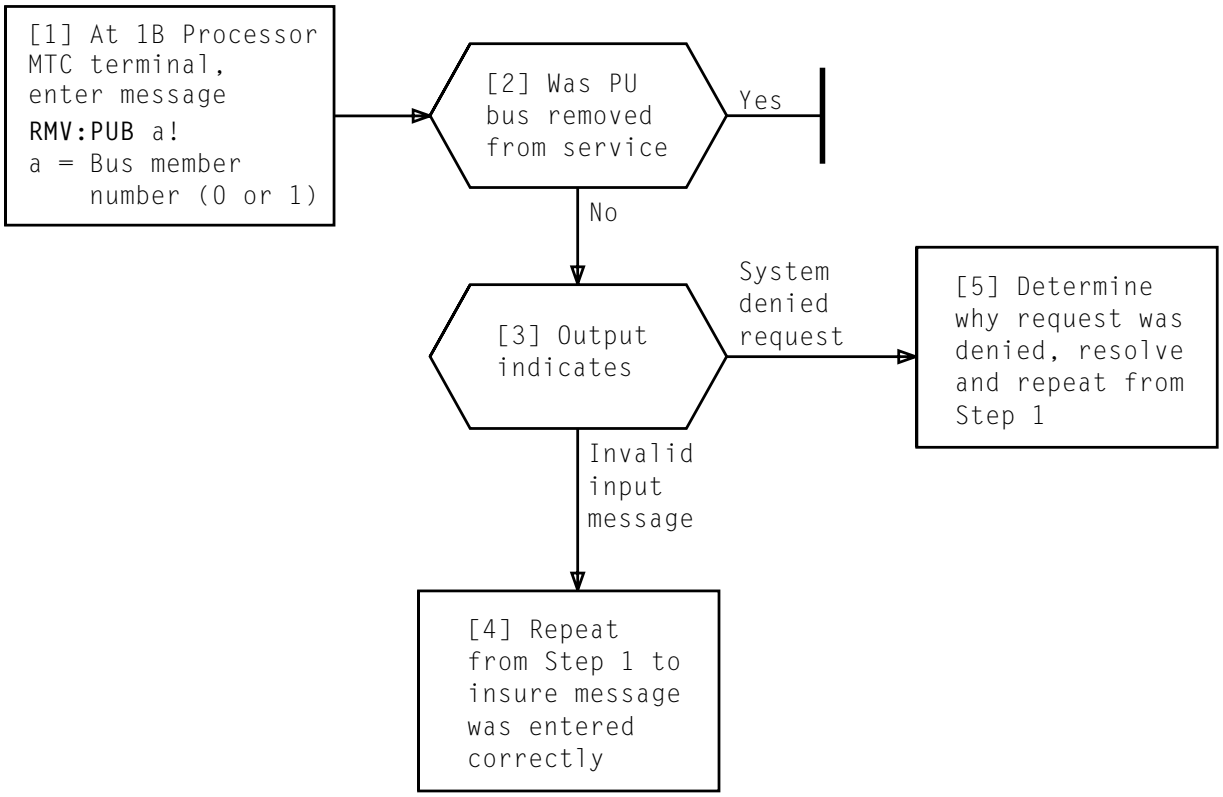
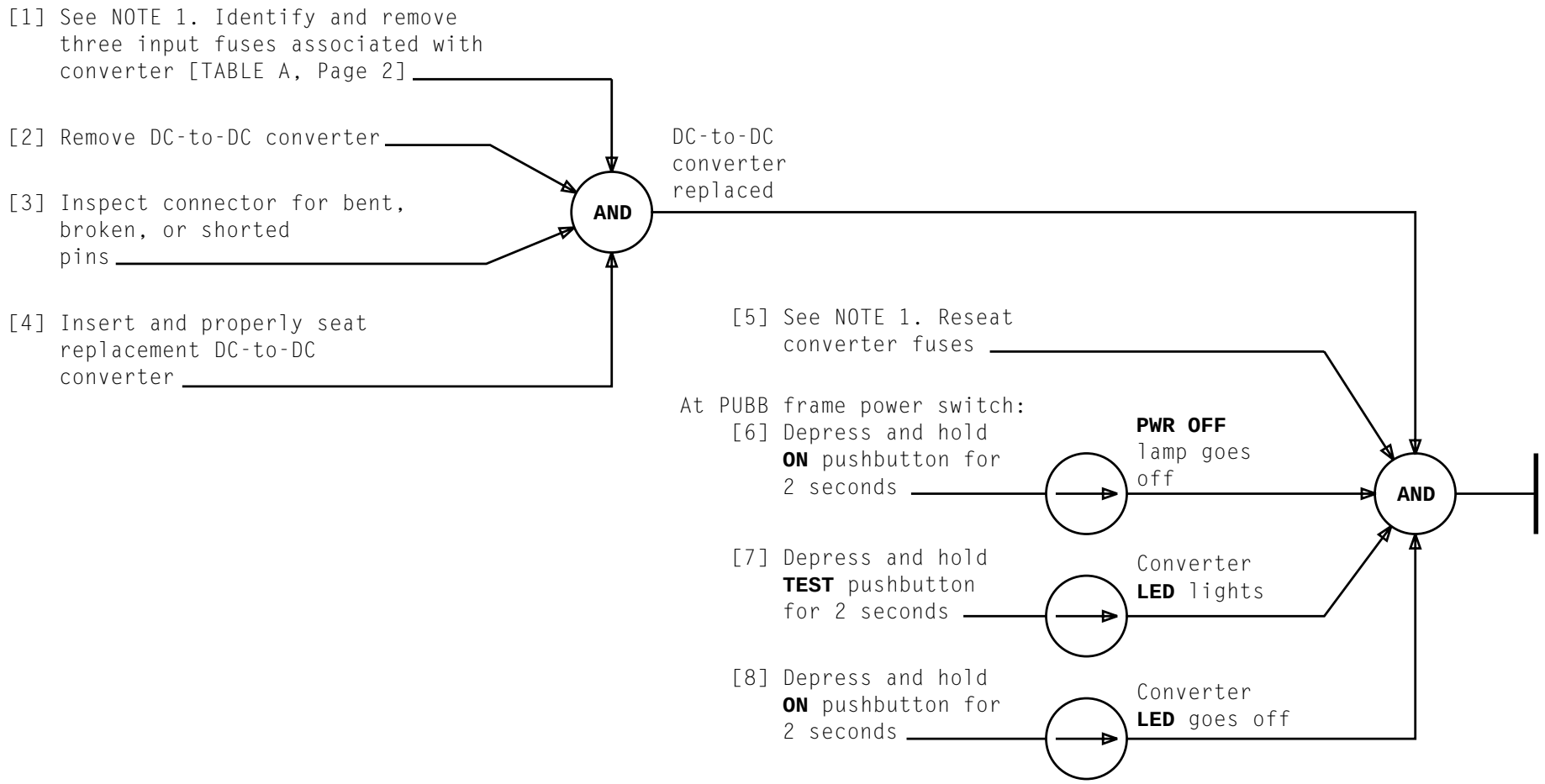
RESTORE PERIPHERAL UNIT BUS TO SERVICE



REMOVE PERIPHERAL UNIT BUS FROM SERVICE

REPLACE DC-TO-DC CONVERTER (J87407A)



NOTE 1
When removing and reseating fuses associated with J87407A converters, remove 140V fuse first, and reseat 140V fuse last

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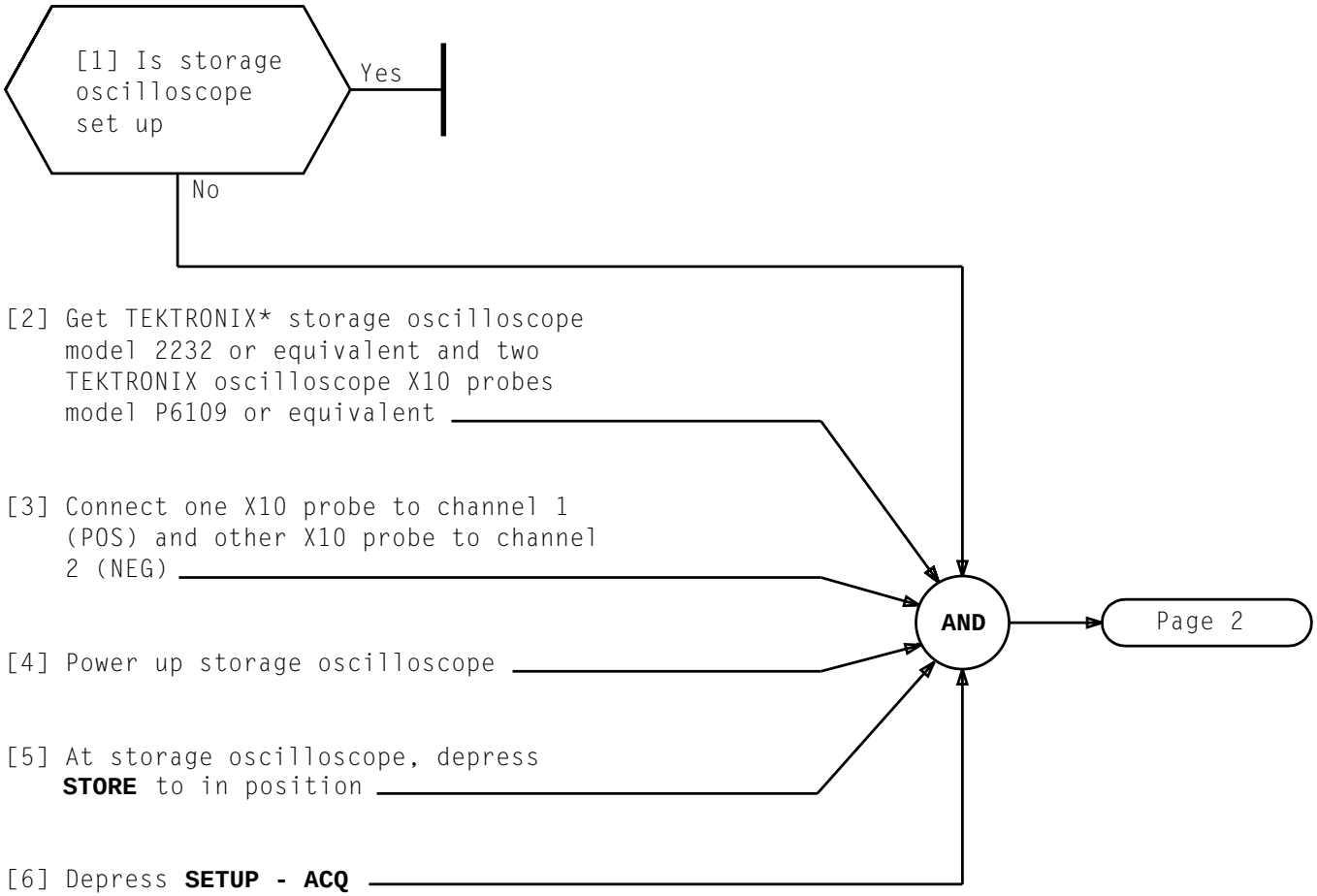
TABLE A				
CONVERTER		FUSES		
LOCATION	DESIGN	140V DESIGN/LOC	+24V DESIGN/LOC	+24V DESIGN/LOC
*17-00	**CV*00**	*AA *07-04 (1 1/3 AMP)	*BA *07-25 (1 1/3 AMP)	*CA *07-25 (3/4 AMP)
*17-03	**CV*01**			
*17-06	**CV*02**			
*12-00	**CV*03**	*AB *07-04 (1 1/3 AMP)		
*12-03	**CV*04**			
*12-06	**CV*05**			
*17-12	**CV*06**	*AC *07-04 (1 1/3 AMP)	*BB *07-25 (1 1/3 AMP)	
*17-15	**CV*07**			
*17-18	**CV*08**			
*12-12	**CV*09**	*AD *07-04 (1 1/3 AMP)		
*12-15	**CV*10**			
*12-18	**CV*11**			
* = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)				

REPLACE DC-TO-DC CONVERTER (J87407A)



* Registered trademark of TEKTRONIX, Inc.

SET UP STORAGE OSCILLOSCOPE FOR PUB LOOPING TEST

[7] Observe storage oscilloscope screen and set ACQ controls per TABLE A by depressing switch associated with control not set correctly

[8] Depress **SETUP** – **DISPLAY**

[9] Observe storage oscilloscope screen and set DISPLAY controls per TABLE B by depressing switch associated with control not set correctly

[10] Depress **SETUP** – **REF**

[11] Observe storage oscilloscope screen and set REF controls per TABLE C by depressing switch associated with control not set correctly

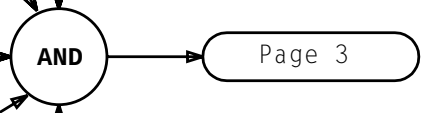


TABLE A

COLUMN	CONTROLS	SWITCH*
1	Peakdet	SAVE REF
2	Scan	1
3	Fast	2
5	Swp Lim: NO LIMIT	4K (for Swp Lim:) and adjust CURSORS to obtain NO LIMIT
5	Trig Pos: 2048/4K	4K (for Trig Pos:), ACQUISITION - 1K/4K (for 4K) and adjust CURSORS to obtain 2048

*Switches under display screen are associated with column that they are under except for Trig Pos: and Swp Lim:

TABLE B

COLUMN	CONTROLS	SWITCH*
1	ΔT	SAVE REF
2	ON	1
3	ON	2

*Switches under display screen are associated with column that they are under

TABLE C

COLUMN	CONTROLS	SWITCH*
1	Format	SAVE REF
2	Ref1	1
3	CH1	2
4	X1	3
5	Vert Gain: 0.2V	4K (for Vert Gain:) and adjust CURSORS to obtain 0.2V

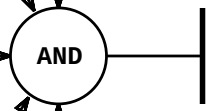
*Switches under display screen are associated with column that they are under

SET UP STORAGE OSCILLOSCOPE FOR PUB LOOPING TEST

[12] Depress **SETUP** – **REF** to return to screen

[13] Determine one location in FIG. 1, Page 5 where bus scoping adapter can be connected

[14] Connect storage scope with bus scoping adapter to connector location determined in Step 13 [see DLP-532 on how to use bus scoping adapter]

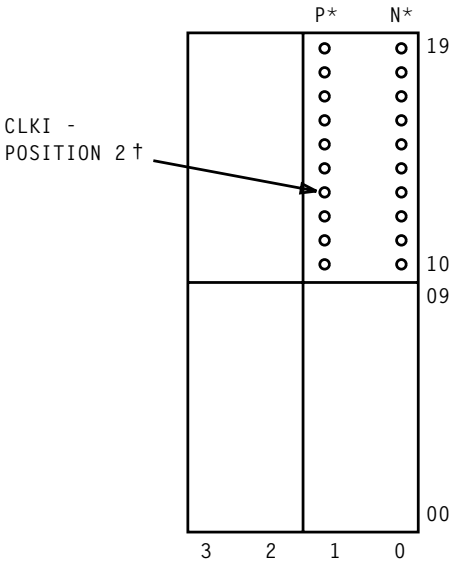


[15] Set bus scoping adapter to position 2

[16] Adjust storage scope per TABLE D, Page 4 for waveform in FIG. 2, Page 5

SET UP STORAGE OSCILLOSCOPE FOR PUB LOOPING TEST

TABLE D OSCILLOSCOPE CONTROL SETTINGS FOR MODEL 2232	
CONTROLS	**POSITION**
SAVE/CONT	Depress until SAVE is not displayed
STORE	Depress (out)
VAR HOLDOFF	Rotate to 1 o'clock position
VERTICAL – POSITION (left)	Rotate to 2 o'clock position
VERTICAL – A/B SWP SEP	Rotate to 12 o'clock position
VERTICAL – POSITION (right)	Rotate to 10 o'clock position
VERTICAL MODE – CH 1 BOTH CH 2	BOTH
VERTICAL MODE – X-Y	Out position
VERTICAL MODE – BW LIMIT	Out position
VERTICAL MODE – ADD ALT CHOP	ADD
VERTICAL – CH 1 VOLTS/DIV	2
VERTICAL – CH 1 VOLTS/DIV – AC GND DC	DC
VERTICAL – INVERT	Depress (in)
VERTICAL – CH 2 VOLTS/DIV	2
VERTICAL – CH 2 VOLTS/DIV – AC GND DC	DC
HORIZONTAL – POSITION	Rotate to 1 o'clock position
HORIZONTAL – MODE	A
HORIZONTAL – A and B SEC/DIV	.2μs
CURSORS	Adjust until ΔT is 0.0 μs on screen
B TRIGGER – SLOPE	Out position
B TRIGGER – LEVEL	Rotate to 8 o'clock position
A TRIGGER – TV FIELD – NORM	Depress (in)
A TRIGGER – SLOPE	Out position
A TRIGGER – LEVEL	Rotate to 12 o'clock position
A TRIGGER – A & B SOURCE	CH 1
A TRIGGER – A COUPL	NORM
A TRIGGER – A EXT COUPL	AC

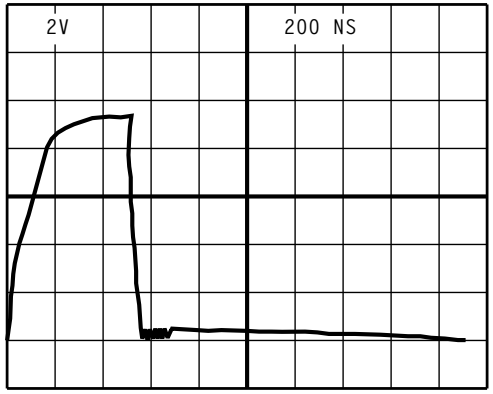


FRAME	
IO	
BUS 0	080-10
BUS 1	080-35
IOP	
BUS 0	080-29
BUS 1	076-29

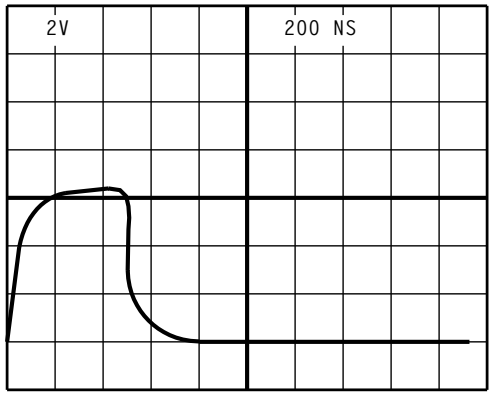
* P FOR POSITIVE LEAD AND
N FOR NEGATIVE LEAD

† POSITION 2 IS ON BUS SCOPING ADAPTER

FIG. 1



NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 2

SET UP STORAGE OSCILLOSCOPE FOR PUB LOOPING TEST

[1] Obtain **PK-4A002** for appropriate 4E generic in office

[2] In the Address Map part of **PK-4A002,** under the **PIDENT, STRIP,** and **SECTION** columns, locate the line that contains **PUDGPBGR, AF,** and **PUDGPBTS**

[3] On the line located in Step 2, under the **ADDR** column, obtain the address listed. Record for use in next step

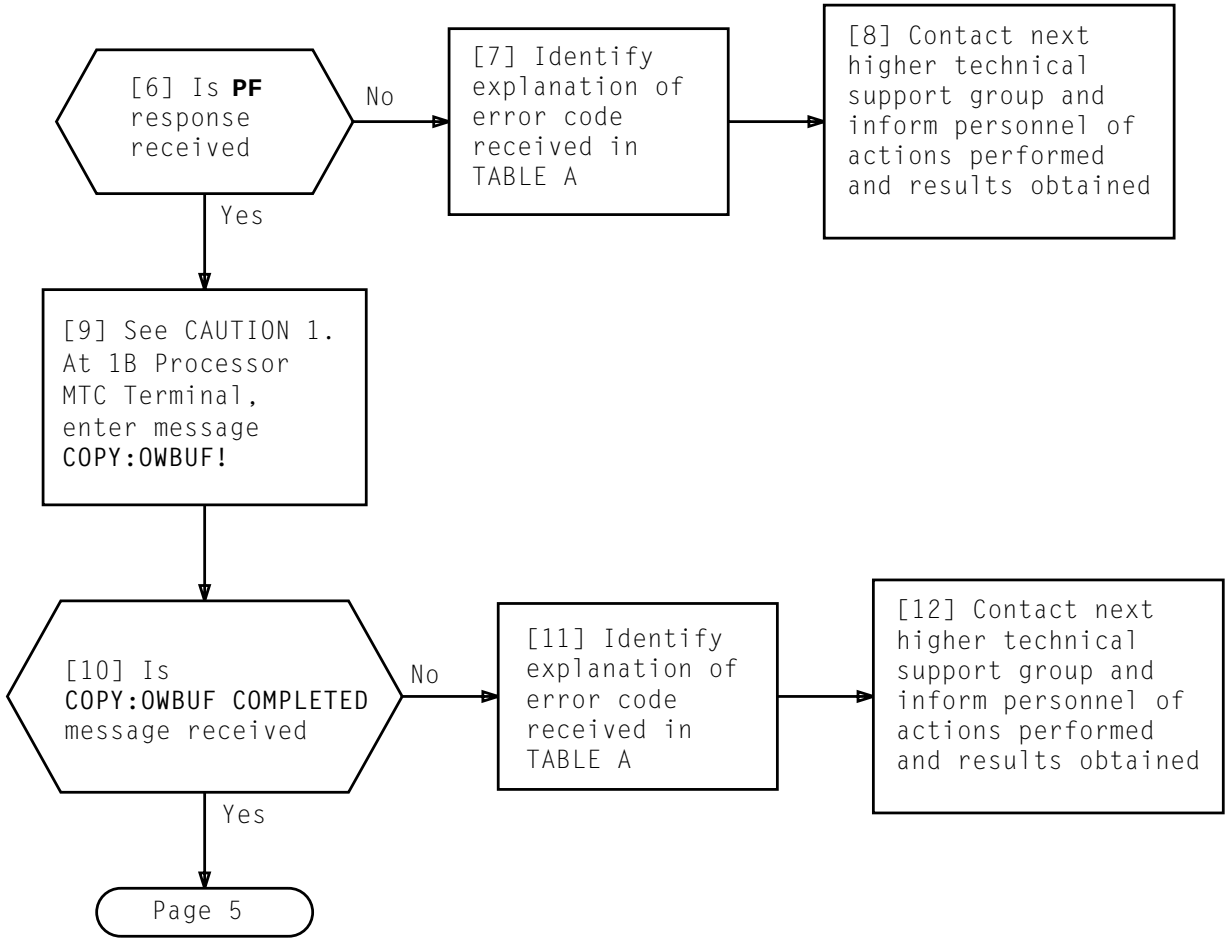
[4] Using the address obtained in Step 3, add 1271 OCTAL to the above address. Save resulting address for use in Step 5

[5] See WARNING 1. At 1B Processor MTC terminal, enter required overwrite (PHPB is first)
IN:OWBUF:FS,ID x,ADR a,DATA b,
OLDDATA 2004010!
Where x = GEN for 4E17, 4E18 &
4E19 Generics
= PGPGM for 4E20 and
Later Generics
a = resulting address from Step 4
b = 01002004 for PHPB
= 01002040 for PDGB
= 01002010 for PLPB
= 01002020 for PSZB

Page 2

WARNING 1
Do not use
UPD:HDATA
message

SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PERIPHERAL FRAME



CAUTION 1
Verify correct output message response of OLD DATA and NEW DATA

SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PERIPHERAL FRAME

TABLE A
OVERWRITE ERROR CODES

ERROR CODE	EXPLANATION
DPLX FAIL	GULP cannot be paged to parse the message because the file stores are duplex failed.
50	Conditional printout may follow. This acknowledgement is used if disk files are duplex failed and GULP is being paged from tape.
100	Invalid syntax. Check input manual to verify that no extra keywords have been input.
101	No argument for keyword ID.
102	No argument for keyword PKG.
103	No argument for keyword FPKG.
104	No argument for keyword ADR.
105	No argument for keyword DATA.
106	Number of arguments of OLDDATA is different from number of arguments of DATA.
110	Overwrites of system merge ID tag cannot be mixed with overwrites of other ID tags.
111	Overwrite overlaps two ID tags.
112	Wrong ID tag specified for a library file store only overwrite.
113	Input address is not in hashed range.
114	Invalid ID tag mnemonic.
115	Incorrect ID tag specified for a file store only overwrite.
120	Part or all non-library main memory overwrite is not backed up on file store.
121	File store backup range is not contiguous. Overwrite must be split on main memory store boundary.
122	PKG, ADR conversion failed. This is due to either invalid or unknown PKG name, relative address larger than size of PKG, or library package not loaded.
123	FPKG, ADR conversion failed. Invalid FPKG name.
124	Library overwrite outside of library Kcode.
131	Overwrite in progress from another channel.
132	Previously input **COPY:OWBUF** request has not yet completed. Enter **STOP:OVRWRT**.
133	Hash mismatch on **COPY:OWBUF**. Enter **STOP:OVRWRT**.
134	Previously input **UPD:HDATA** request has not yet completed. Enter **STOP:OVRWRT**.
135	No overwrite in progress

TABLE A (CONTD)
OVERWRITE ERROR CODES

ERROR CODE	EXPLANATION
136	UPD:HDATA may be input only from the maintenance channel (or its backup if the maintenance channel is out-of-service) or the SCC channel. Before entering message, check for audit printouts or interrupts to assure overwrite is not incorrect.
137	A COPY:OWBUF message must be input.
138	Core only overwrite backed out.
140	Overwrite buffer full.
141	Library program not loaded in PS36 library Kcode.
143	Input overwrite overlaps with overwrite currently in buffer.
144	Old data specified in message does not match data in system.
145	Library system in transition state. Wait a few seconds and reenter the message.
150	Library program is not currently loaded in library Kcode. The overwrite has been bypassed.
152	Hash sum input on COPY:OWBUF does not match computed hash. This indicates that some data in the buffer is different than was expected when input hash was generated. Enter STOP:OVRWRT and check printout.
153	Hash update by SAWS failed. Enter STOP:OVRWRT. Tape audit (SAST) must be run to correct hash errors.
160	File store queue full.
161	DKAD reject — core ADR is out of range. Request technical assistance.
162	DKAD reject — file store address mismatches ID tag.
163	DKAD reject — write request not multiple of 32 or not on sector boundary.
164	DKAD reject — size too big.
165	DKAD reject — file specified is out-of-service.
166	DKAD reject — blocked.
167	DKAD reject — write (trouble) to in-service file.
168	DKAD reject — queue invalid for GULP.
169	DKAD reject — mutilated queue.
170	DKAD reject — no queue specified.
180	Execution of GULP function is in progress.
181	Message processing in progress.
182	Dataset input mode in progress on another channel.
183	Dataset execution is in progress.
184	Message print in progress.
185	Failure to page in GULP or failure to seize general buffer table (GBT).

[13] At 1B Processor MTC Terminal, enter diagnostic looping messages
EX:PUB x**;START!**
EX:PUB x**:PH 2,ENABLE** yyyy**,ADR 1262-1275!**
(yyyy=3195 for CC 0 or 56955 for CC 1)
(x = PUB 0 or 1)

[14] Frame to be scoped is

DIFE

[15] See NOTE 1. Connect scope probes across the BTR locations for bit to be scoped (FIG. 2 and Table B)

SCS or XTSI

[16] See NOTE 1. Connect scope probes across the BTR at locations for bit to be scoped (FIG. 1 and Table B)

[17] Verify the Pollable Bit per waveform (FIG. 3)

[18] At 1B Processor MTC Terminal, enter stop looping and stop overwrite messages **EX:PUB** x**!**
STOP:OVRWRT!

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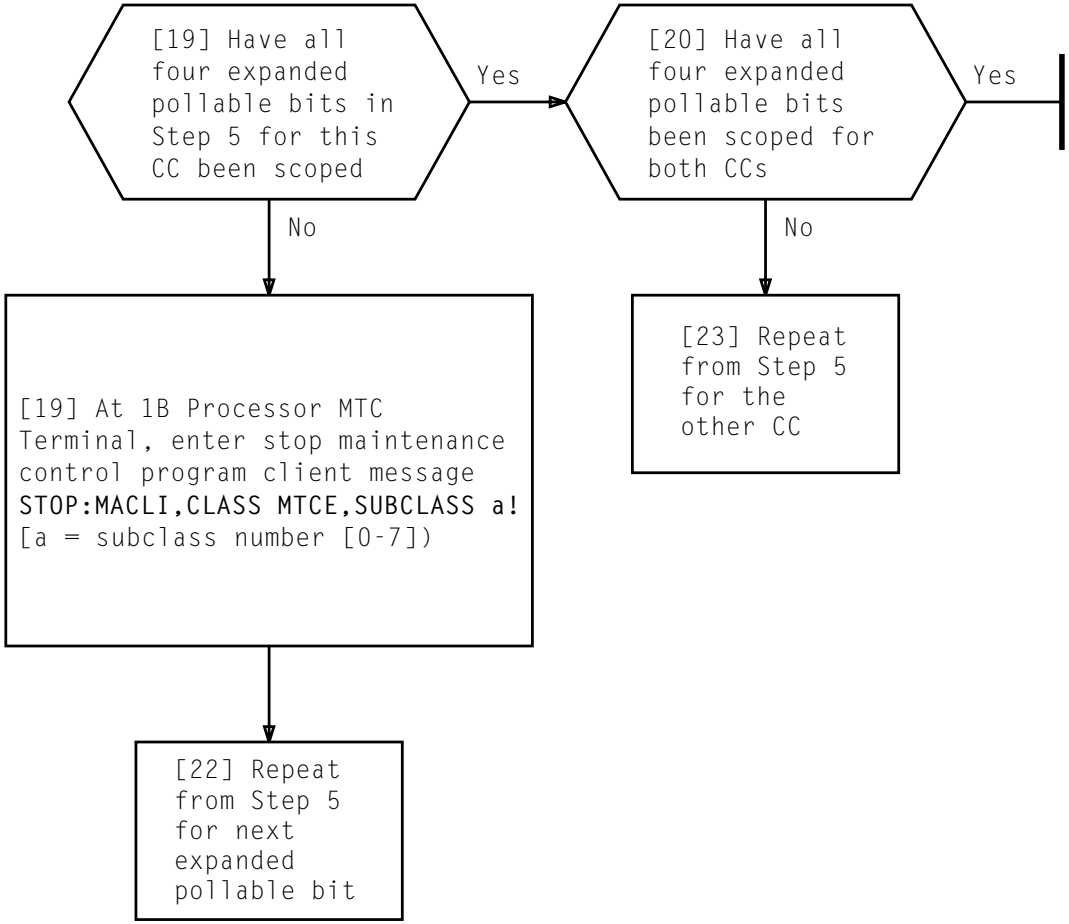
TABLE B

NET NAME	PULSE POINT	DATA
LPP PDGB	(PPU065)	01002040
LPP PSZB	(PPU064)	01002020
LPP PLPB	(PPU063)	01002010
LPP PHPB	(PPU062)	01002004

NOTE 1
Scope probe cables are twisted together. The ground leads of the two cables are connected together, but are not grounded

SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PERIPHERAL FRAME



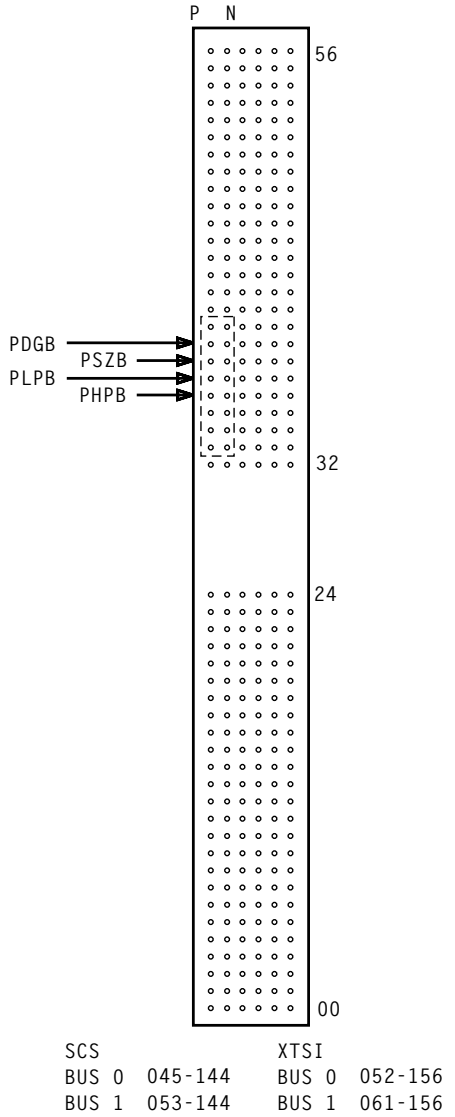
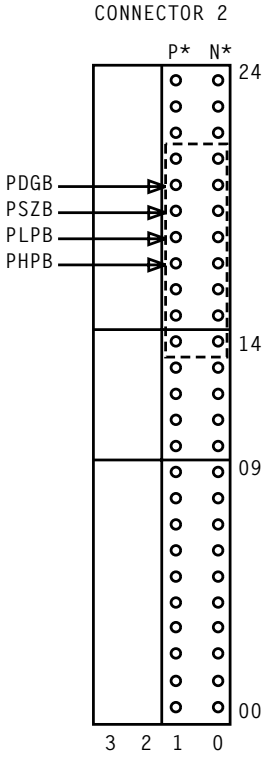


FIG. 1

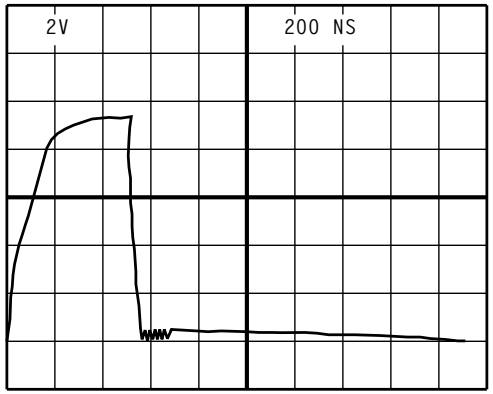
SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PERIPHERAL FRAME



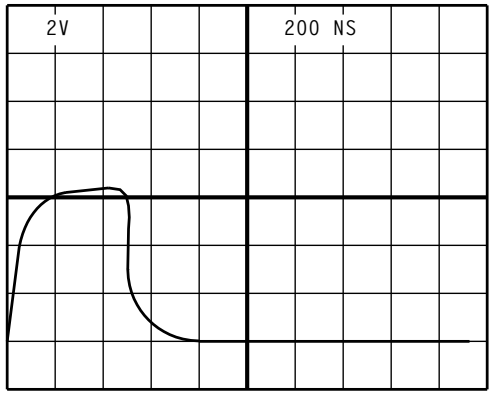
DIF or DIFE	(24-31)
BUS 0	180-067
BUS 1	180-215

* P FOR POSITIVE LEAD AND
  N FOR NEGATIVE LEAD

FIG. 2



NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 3

SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PERIPHERAL FRAME

[1] Obtain **PK-4A002** for appropriate 4E generic in office

[2] In the Address Map part of **PK-4A002**, under the **PIDENT**, **STRIP**, and **SECTION** columns, locate the line that contains **PUDGPBGR**, **AF**, AND **PUDGPBTS**

[3] On the line located in Step 2, under the **ADDR** column, obtain the address listed. Record for use in next step

[4] Using the address obtained in Step 3, add 1271 OCTAL to the above address. Save resulting address for use in Step 5

[5] See WARNING 1. At 1B Processor MTC terminal, enter required overwrite (PHPB is first)
IN:OWBUF:FS,ID x,ADR a,DATA b,
OLDDATA 2004010!
Where x = GEN for 4E17, 4E18 &
4E19 Generics
= PGPGM for 4E20 and
Later Generics
a = resulting address from Step 4
b = 01002004 for PHPB
= 01002040 for PDGB
= 01002010 for PLPB
= 01002020 for PSZB

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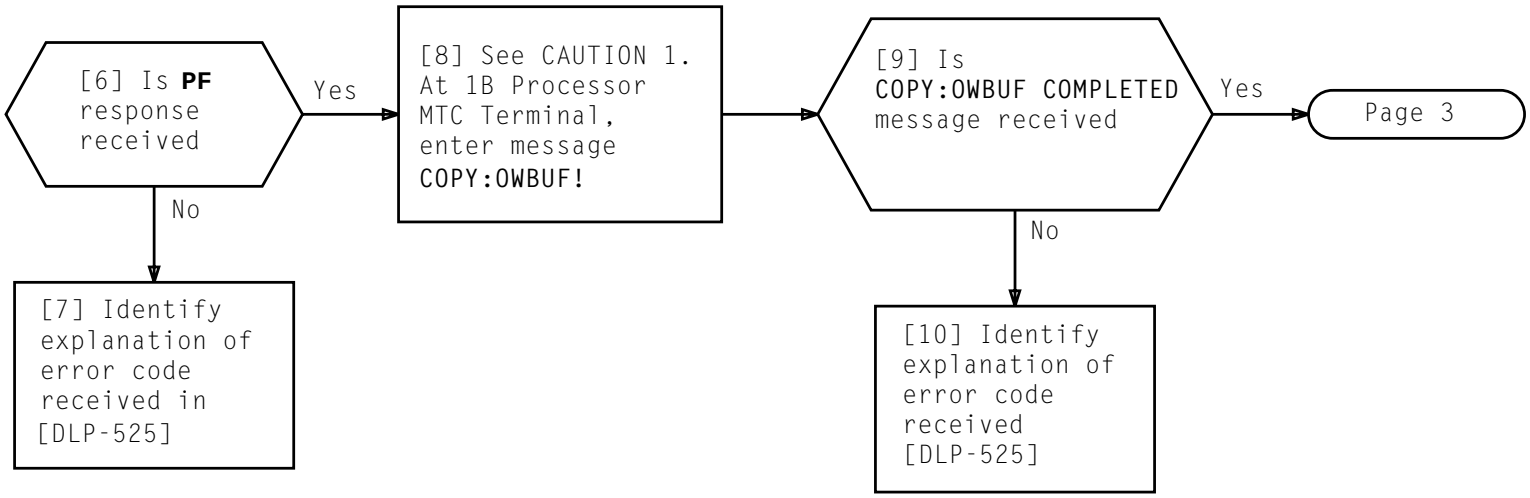
WARNING 1
Do not use
UPD:HDATA
message

SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PUBB FRAME



CAUTION 1
Verify correct output message response of OLD DATA and NEW DATA

SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PUBB FRAME

[11] At 1B Processor MTC Terminal, enter diagnostic looping messages
EX:PUB x;START!
EX:PUB x:PH 2,ENABLE yyyy,ADR 1262-1275!
(yyyy=3195 for CC 0 or 56955 for CC 1)
(x = PUB 0 or 1)

→ [12] See NOTE 1. Connect scope probes across the BTR at locations for bit to be scoped (FIG. 1 and Table A)

→ [13] Verify the Pollable Bit per waveform [FIG. 2]

→ [14] At 1B Processor MTC Terminal, enter stop looping and stop overwrite messages **EX:PUB x! STOP:OVRWRT!**

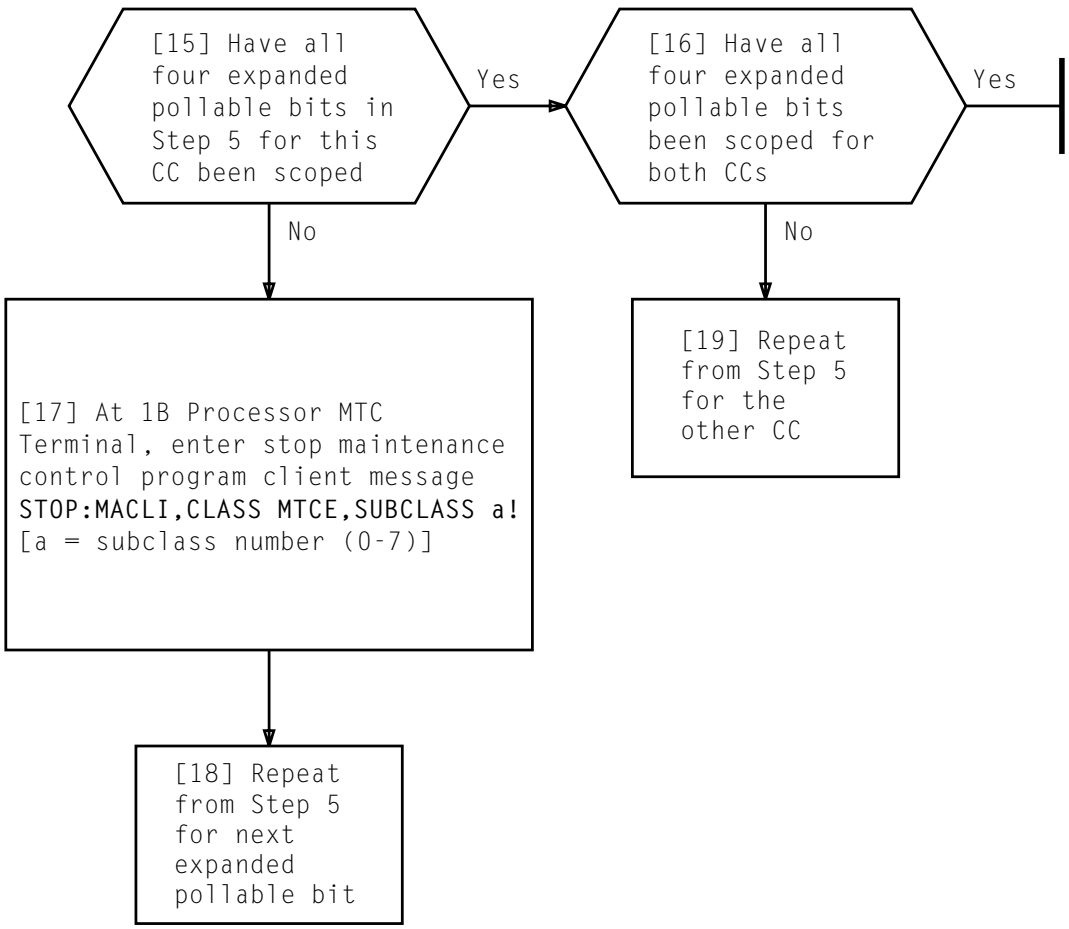
TABLE A

NET NAME	PULSE POINT	DATA	CHANNEL 1*	CHANNEL 2*
LPP PDGB	(PPU065)	01002040	06-28-117	06-28-017
LPP PSZB	(PPU064)	01002020	06-28-115	06-28-015
LPP PLPB	(PPU063)	01002010	06-28-113	06-28-013
LPP PHPB	(PPU062)	01002004	06-28-111	06-28-011

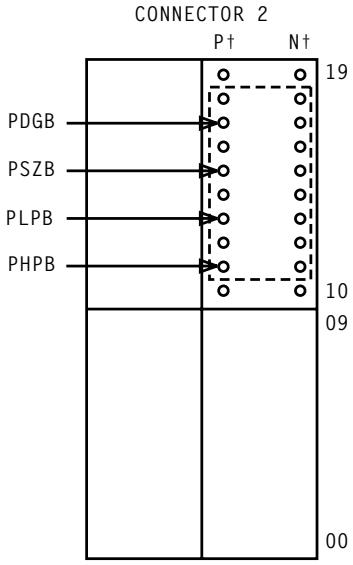
* BTRs for pulse points from CC0 are in Bay 1. BTRs for pulse points from CC1 are in Bay 0. They are wired to the backplane pins at the indicated Channel 1 and Channel 2 locations.

NOTE 1
Scope probe cables are twisted together. The ground leads of the two cables are connected together, but are not grounded

SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PUBB FRAME



SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PUBB FRAME

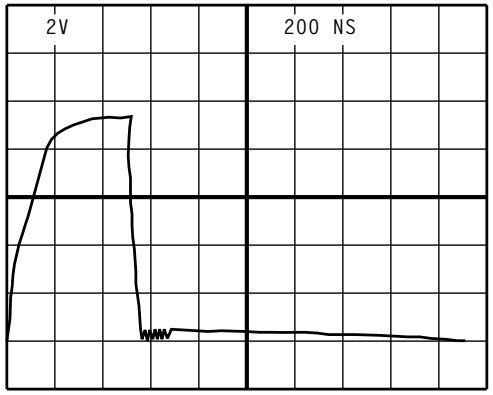


BRANCH A	*76-28
BRANCH B	*76-28
BRANCH C	*76-28
BRANCH D	*76-28
BRANCH E	*64-28
BRANCH F	*64-28
BRANCH G	*64-28
BRANCH H	*64-28
BRANCH K	*48-28
BRANCH L	*48-28
BRANCH M	*48-28
BRANCH R	*48-28
BRANCH T	*36-28
BRANCH V	*36-28
BRANCH W	*36-28
BRANCH X	*36-28

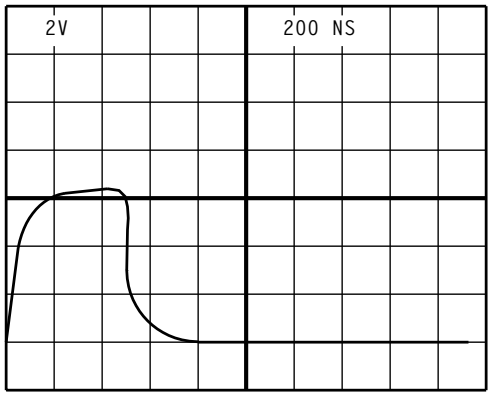
* 0 FOR BUS 0 OR 1 FOR BUS 1

† P FOR POSITIVE LEAD AND N FOR NEGATIVE LEAD

FIG. 1



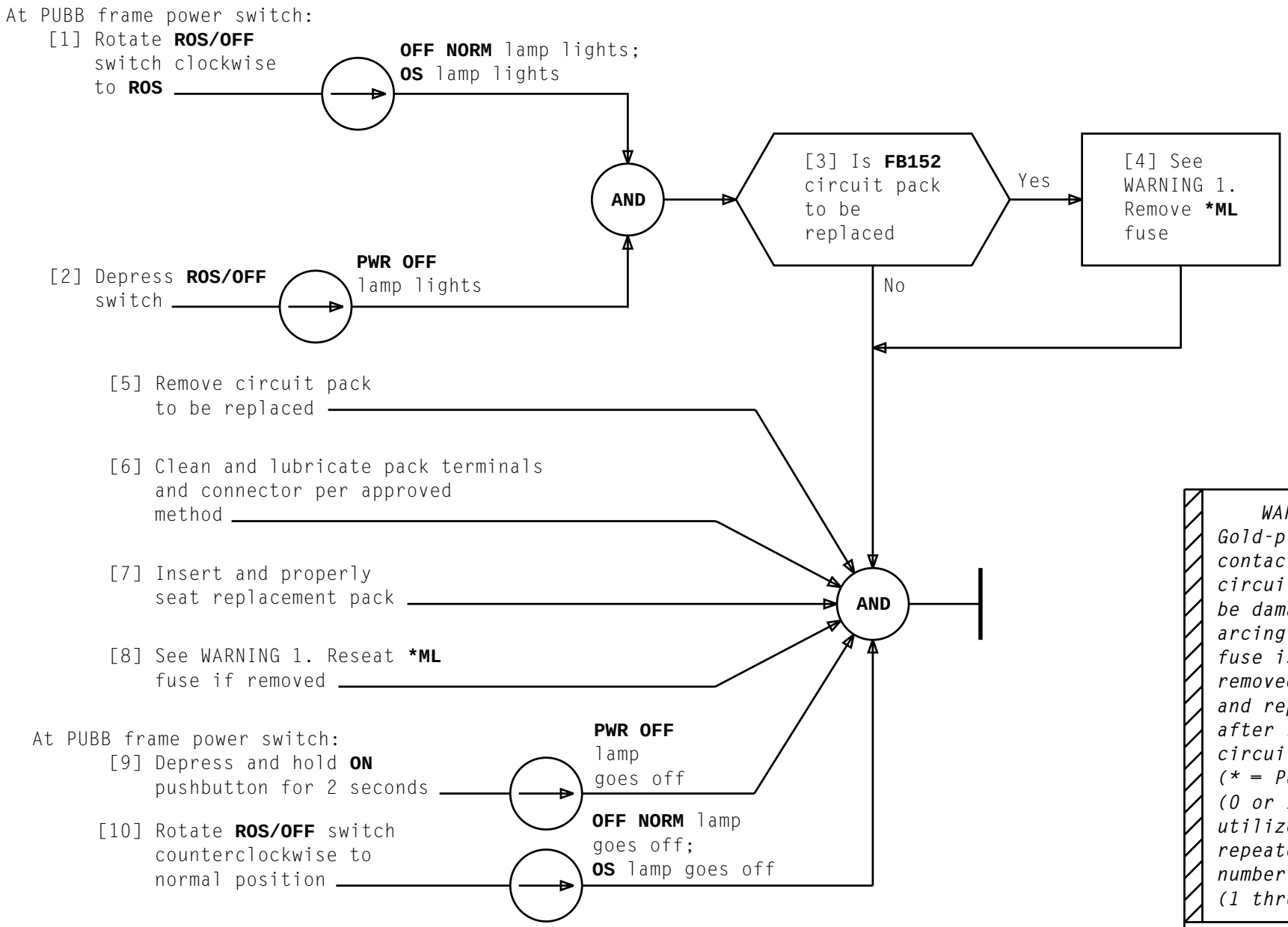
NORMAL PULSE AT DRIVER



NORMAL PULSE 500 FEET FROM DRIVER

FIG. 2

SET UP LOOP TO OBSERVE AND SCOPE EXPANDED POLLABLE BITS AT PUBB FRAME



WARNING 1
*Gold-plated contacts on FB152 circuit pack may be damaged by arcing if *ML fuse is not removed before and replaced after replacing circuit pack (* = PUBB bay (0 or 1) or if utilized, repeater frame number (1 through 4)*

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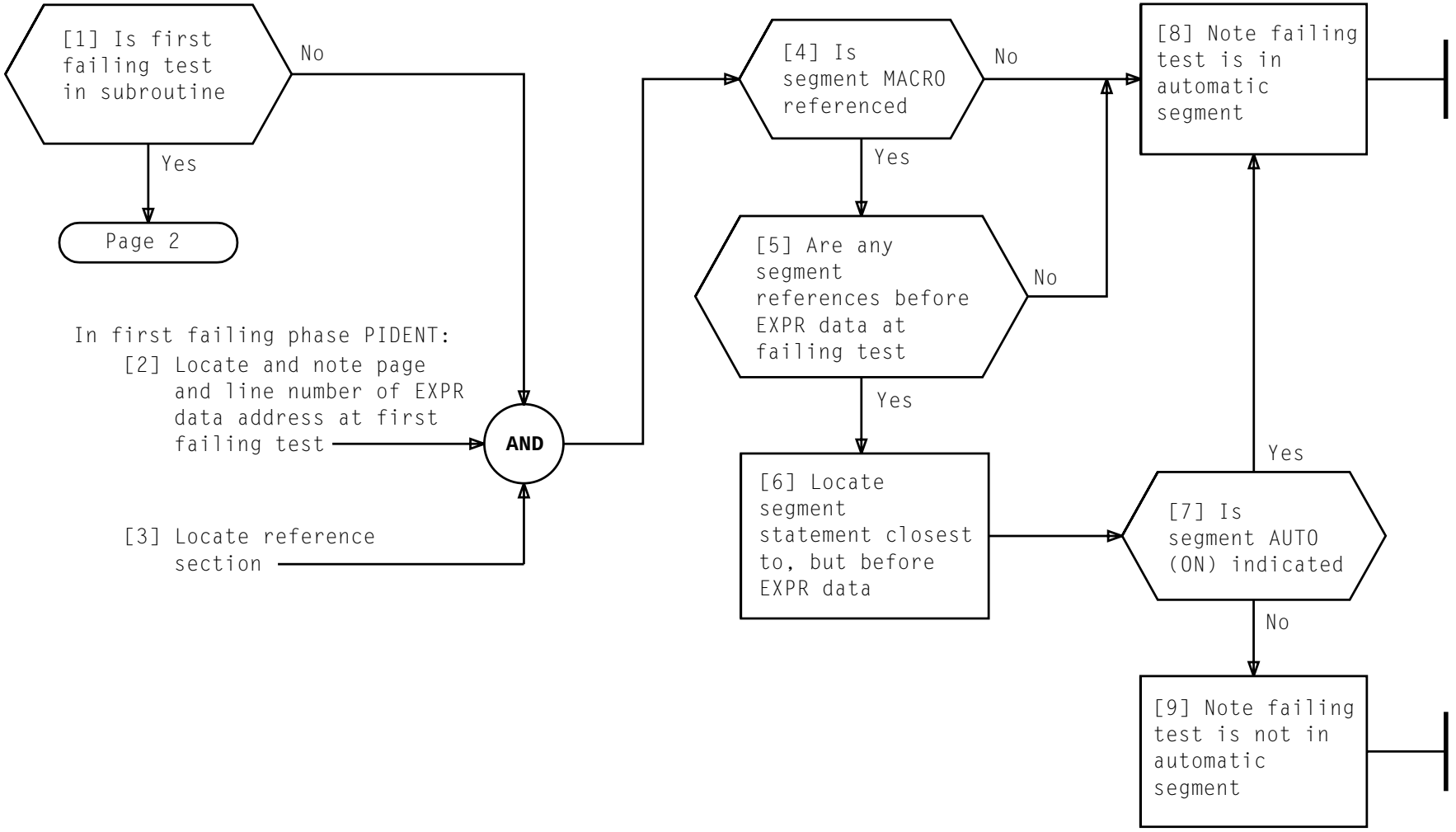
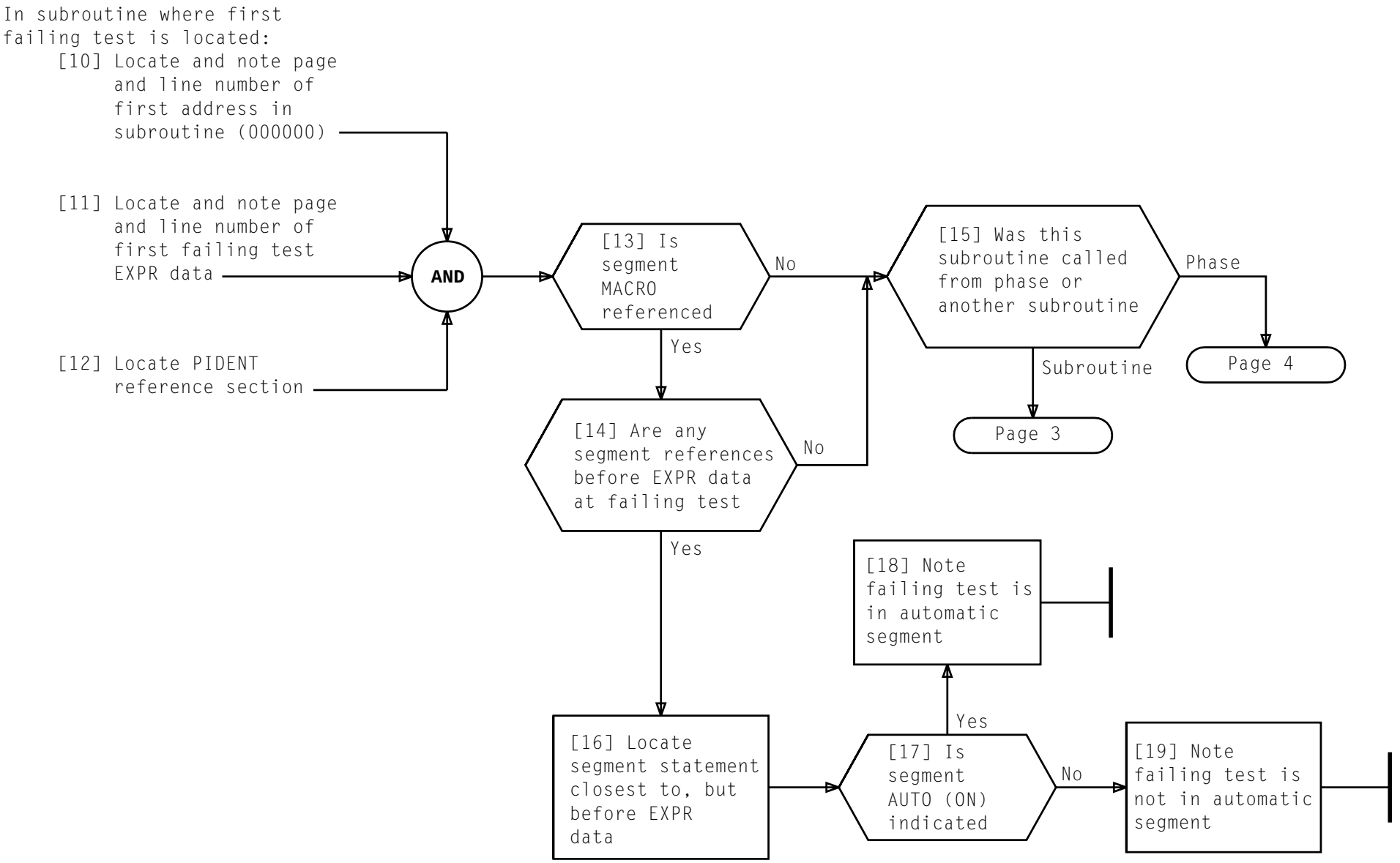
REPLACE CIRCUIT PACK, PUBB FRAME

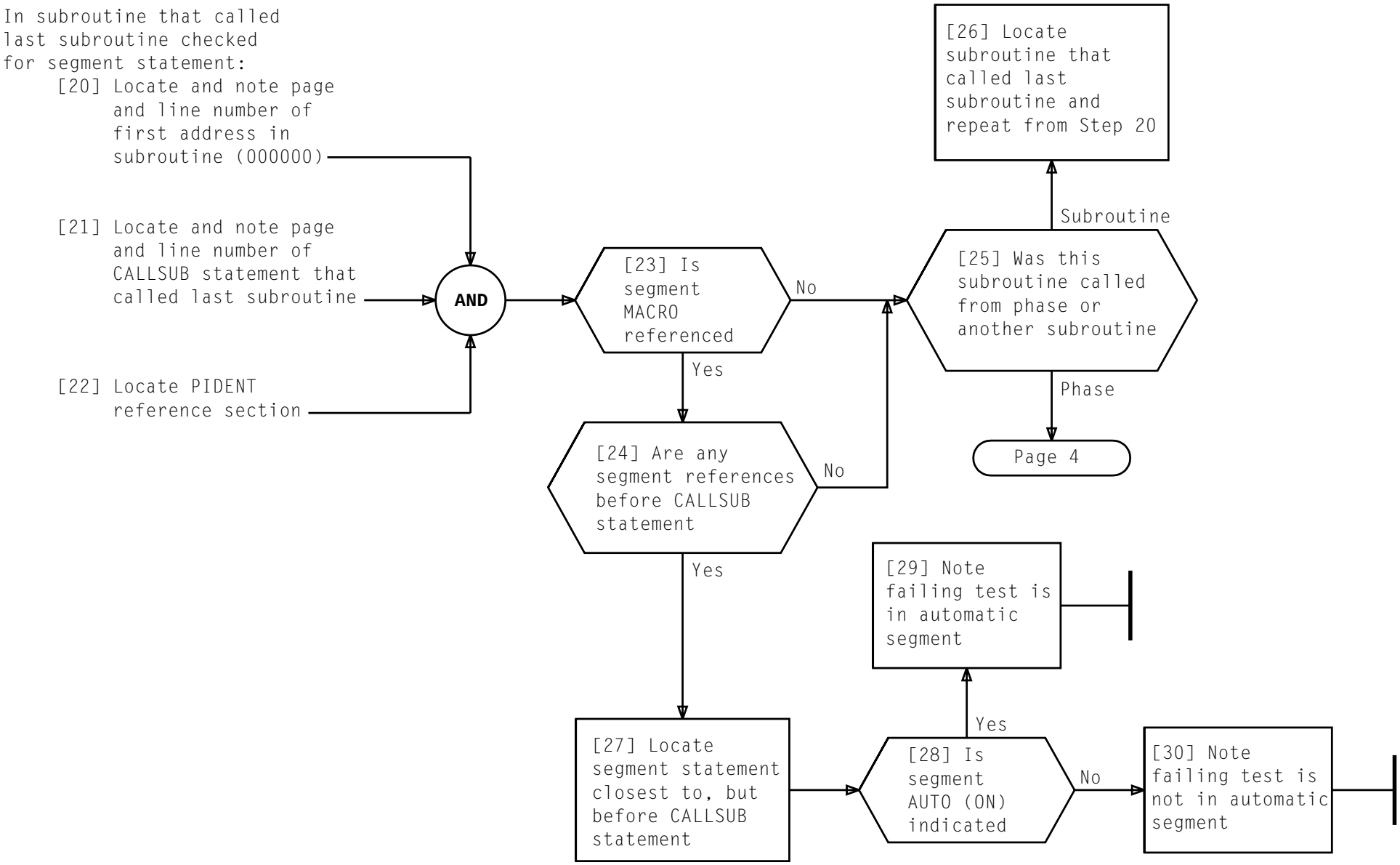
SUMMARY
Locate FIRST segment statement BEFORE first failing test. If segment statement has AUTO (ON) indicated, failing test is in automatic segment. If AUTO (ON) is not indicated, failing test is not in automatic segment. If no segment statement is found before first failing test, failing test is in automatic segment



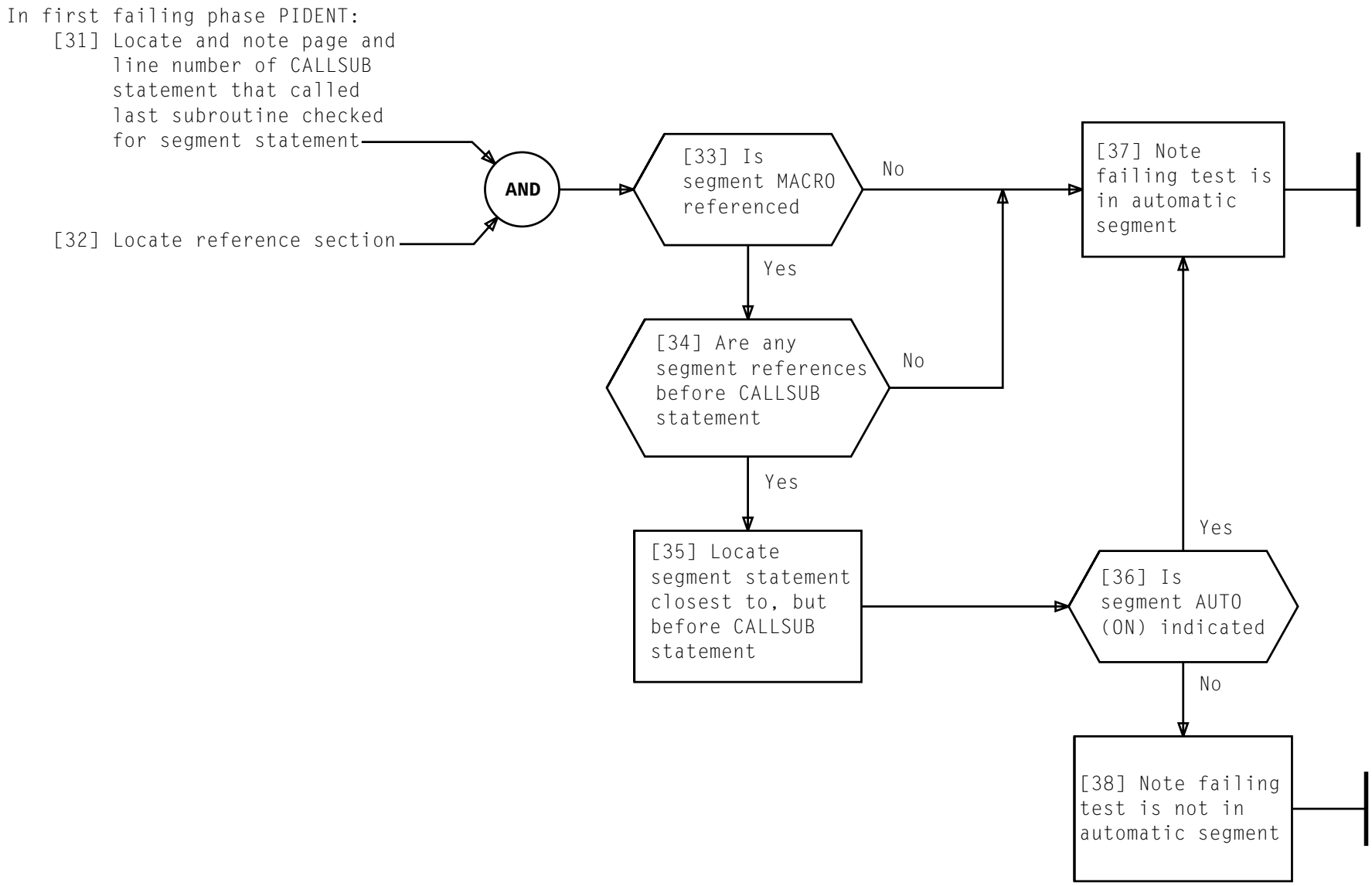
DETERMINE IF FAILING TEST IS IN AUTOMATIC SEGMENT



DETERMINE IF FAILING TEST IS IN AUTOMATIC SEGMENT



DETERMINE IF FAILING TEST IS IN AUTOMATIC SEGMENT



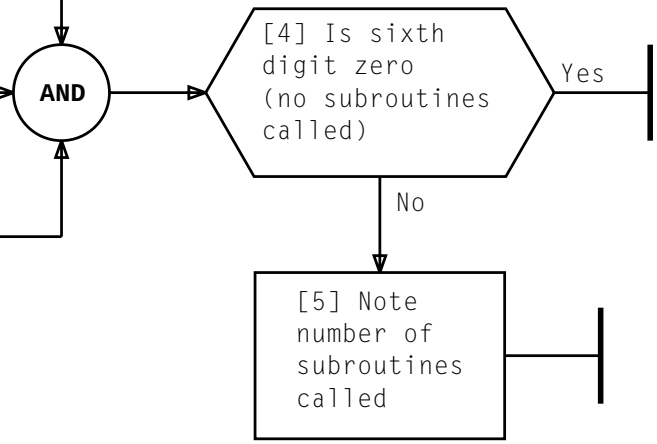
DETERMINE IF FAILING TEST IS IN AUTOMATIC SEGMENT

On raw data printout [FIG. 1, Page 2]:

[1] Locate first failing test raw data

[2] Locate fifth data word following mismatch data

[3] Identify sixth digit of fifth data word



DETERMINE IF SUBROUTINES WERE CALLED

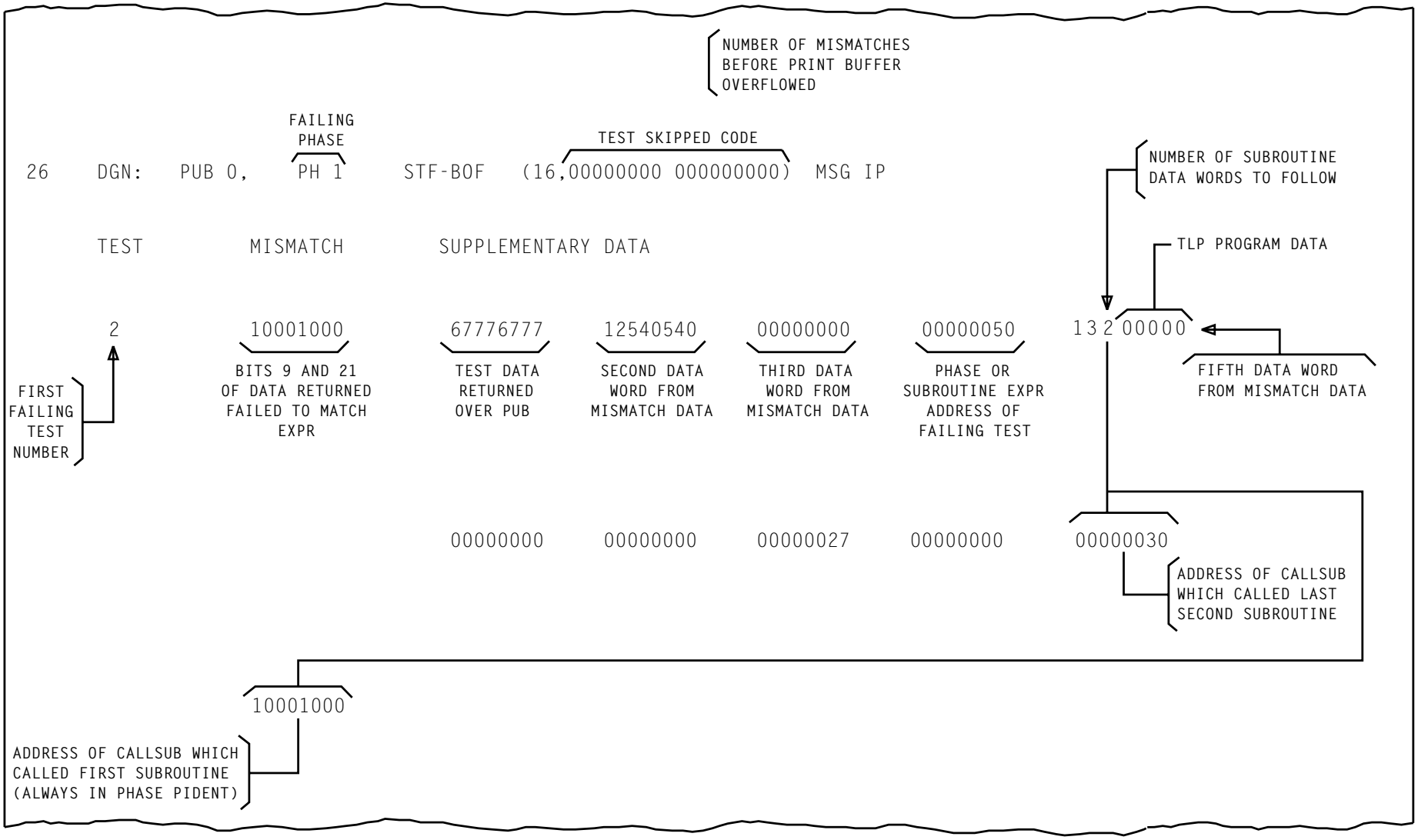


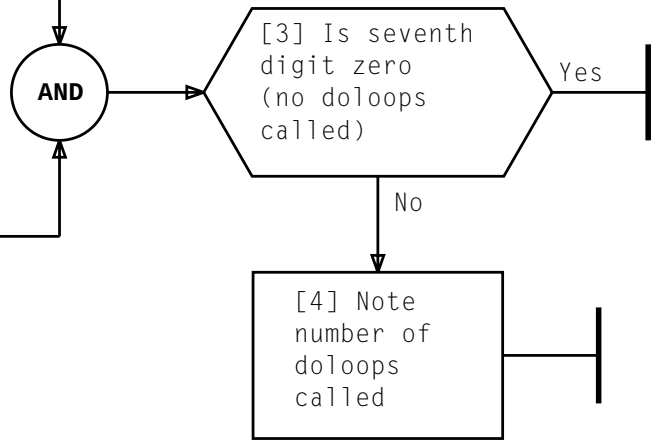
FIG. 1 – Example of PUBB Frame Raw Data Printout

DETERMINE IF SUBROUTINES WERE CALLED

On raw data printout [FIG. 1, Page 2]:

[1] Locate fifth data word following mismatch data

[2] Identify seventh digit of fifth data word



DETERMINE IF DOLOOPS WERE CALLED

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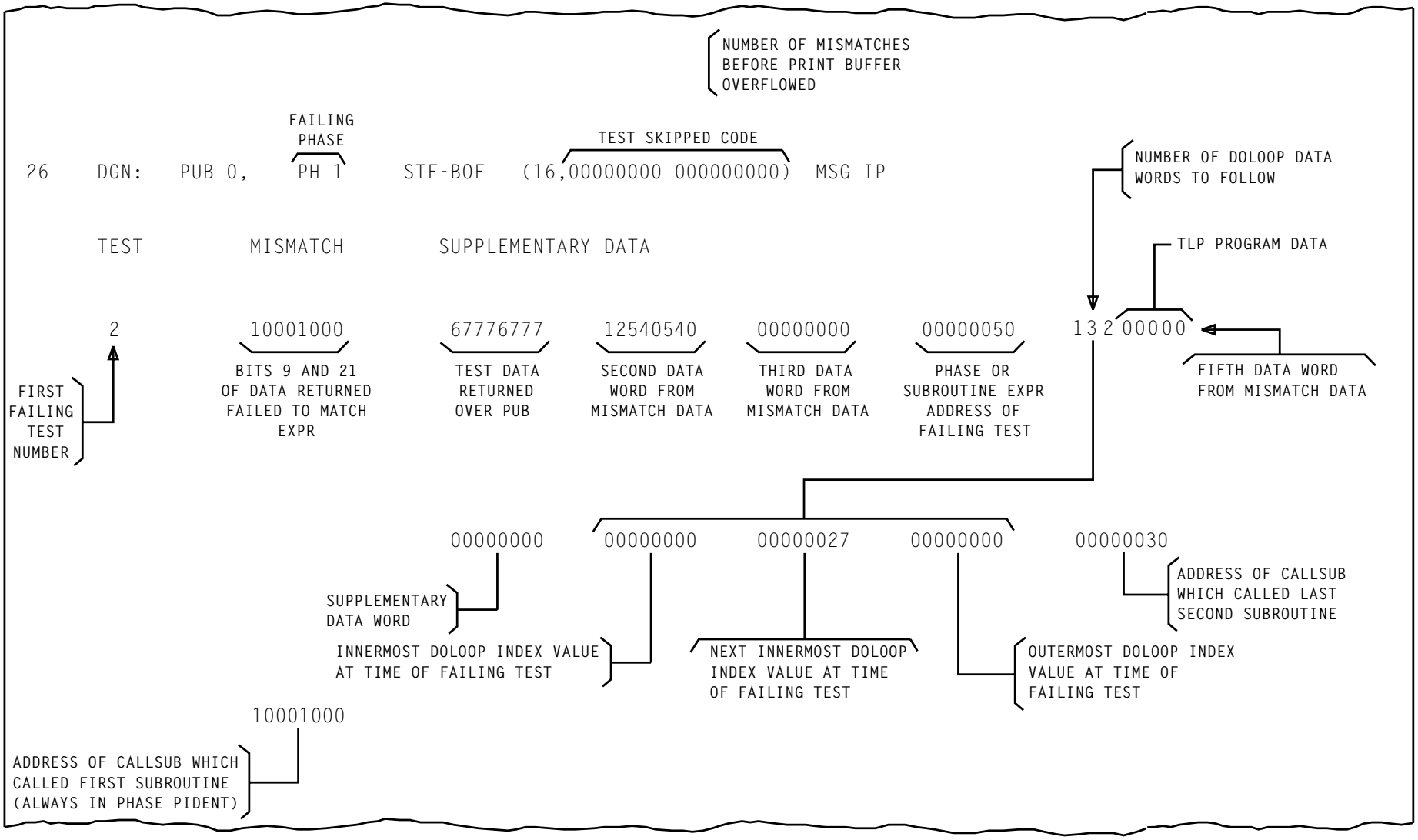

FIG. 1 – Example of PUBB Frame Raw Data Printout

DETERMINE IF DOLOOPS WERE CALLED

1. Locate segment statement that determined failing test was not in automatic segment

2. Note segment statement index word address for later use (loop start address)

3. Locate first segment statement after failing test

4. Note index word address of DIAL statement that follows segment statement located (loop end address)

5. At 1B Processor MTC terminal, enter message
   EX:PUB a;RPT 2:PH b,ADR c-d!
   a = failing PUB (0 or 1)
   b = first failing phase number
   c = loop start address
   d = loop end address

End of procedure

SET UP LOOP OVER FIRST FAILING TEST, WHEN TEST IS IN FORCE SEGMENT

[1] Ensure scope probes from storage scope are wrapped around each other with positive lead connected to Channel 1 and negative lead connected to Channel 2 and ground leads are attached together

[2] See FIG. 1, Page 2. At bus scoping adapter, connect probe from Channel 1 to P connector and Channel 2 to N connector

[3] Connect bus scoping adapter connector to connector at unit/frame to be scoped [FIG. 1, Page 2]

[4] Using bus scoping adapter, starting at position 0, scope each bit, as required through range 0 to 7

[5] If more than one connector is to be scoped, disconnect bus scoping adapter connector and reconnect to another connector to be scoped. Repeat Steps 4 and 5 for each connector to be scoped. See TABLE A for scope adapter position to associated bit

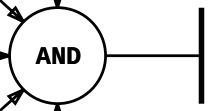

TABLE A

BIT	ASSOCIATED SCOPE ADAPTER POSITION	BIT	ASSOCIATED SCOPE ADAPTER POSITION
0	0	16	0
1	1	17	1
2	2	18	2
3	3	19	3
4	4	20	4
5	5	21	5
6	6	22	6
7	7	23	7
8	0		
9	1		
10	2		
11	3		
12	4		
13	5		
14	6		
15	7		

HOW TO USE BUS SCOPING ADAPTER

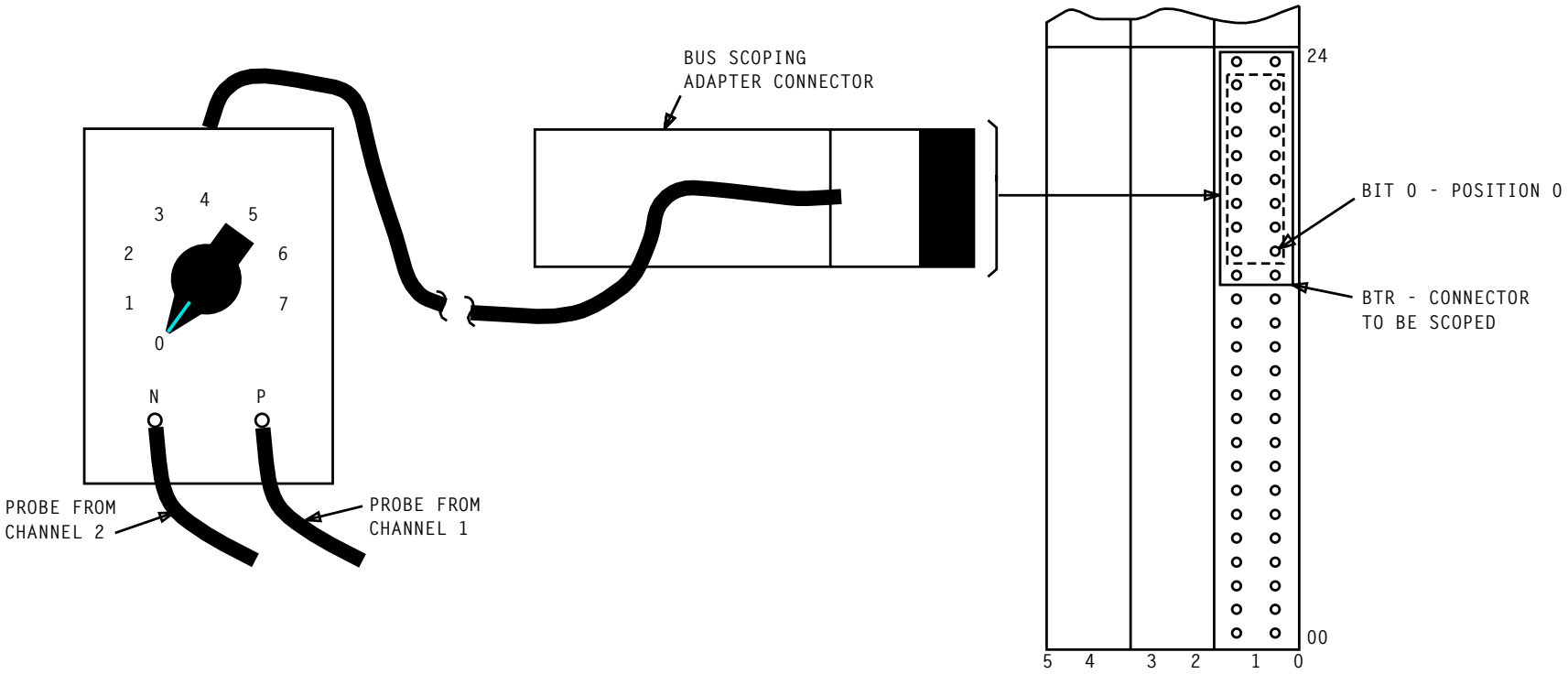

FIG. 1 — Bus Scoping Adapter Connections

HOW TO USE BUS SCOPING ADAPTER

ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE
TPG-000		DLP-516									
IXL-001		DLP-517									
NTP-002		DLP-518									
NTP-003		DLP-519									
NTP-004		DLP-520									
TAD-100		DLP-521									
TAD-101		DLP-522									
TAP-102		DLP-523									
TAP-103		DLP-524									
TAP-104		DLP-525									
TAP-105		DLP-526									
TAP-106		DLP-527									
TAP-107		DLP-528									
TAP-108		DLP-529									
TAP-109		DLP-530									
TAD-110		DLP-531									
TAP-111		DLP-532									
TAP-112		CKL-891									
TAP-113		TNG-893									
DLP-500											
DLP-501											
DLP-502											
DLP-503											
DLP-504											
DLP-505											
DLP-506											
DLP-507											
DLP-508											
DLP-509											
DLP-510											
DLP-511											
DLP-512											
DLP-513											
DLP-514											
DLP-515											

● REVISED OR ADDED ITEM ☐ CANCELED ITEM

CHECKLIST