



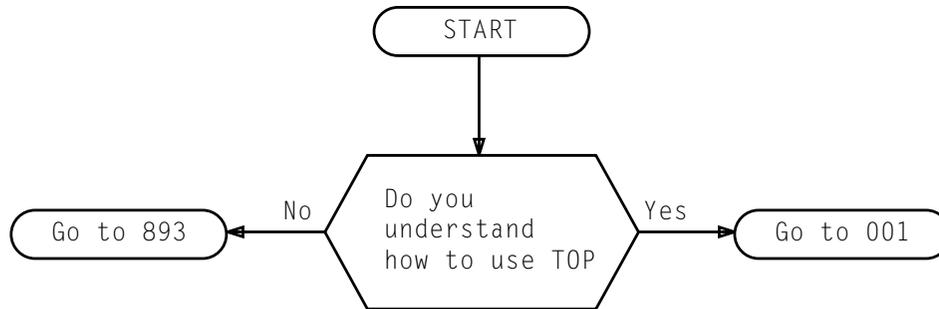
Task Oriented Practice (TOP)

4ESS™ SWITCH

1B Processor

Output Message Analysis

(Audits, Interjects, Interrupts, and BLMs)



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Verify XTSI Files Stored in 3B Computer DLP-536
 Verify D3U Software Version Set to One DLP-537
 Verify New System Files were Copied to XTSI DLP-539

No acceptance test procedures are required

ACCEPTANCE

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MAINTENANCE PHILOSOPHY

General

The output message analysis volume has been developed to extend the trouble-clearing strategy beyond the limits of the Diagnostic (DGN) programs. Output message analysis is performed in response to specific printouts, AUDIT CALL AT, AUDIT AT, and REPT: usually when no DGN: printout has been generated or a DGN: ATP printout has been generated. However, it is possible to perform output message analysis after fault isolation using DGN: has failed if the appropriate output messages are printed. As a result of output message analysis, a suspect pack or unit may be identified, but no directions to replace the suspect packs are within this volume. Circuit pack replacement procedures are provided in the individual frame volumes and can be accessed through the index in that volume. Verification of success in clearing problems may require monitoring the system, subsystem, and frame operation over a lengthy period of time. This is especially true when the problem is sporadic or intermittent. It is assumed that all instructions and decisions are performed correctly. It is also assumed the user has a basic understanding of key interrupt data as provided in this TAD.

Audits

Audits are performed to correct data errors. The occurrence of an audit is not cause for trouble clearing. The TAPs provided for analyzing audits should only be used when the audit is repetitive, indicating a probability of a hardware error or when the AUDIT CALL AT printout is accompanied by a REPT: SYSTEM TROUBLE: AUDIT UNABLE TO CORRECT TROUBLE printout. For this reason, the printout should be checked for all messages related to the audits performed, before determining which TAP to access.

Base Levels, Interjects, and Interrupts

Interjects and interrupts are analyzed utilizing REPT: printouts generated by fault recognition software. These printouts provide several segments of information that should be analyzed. These segments are: Heading Information, Level Data providing the contents of CC Registers, Fault Recognition Results, Error Analysis Recent History Table, and Internal Registers also known as Critical Registers (CREG). Analyzation of this information may follow different approaches. One, a step-by-step approach takes the user (craft) through a bit-by-bit examination of these registers eliminating fault possibilities with each examination until a group of suspect packs are identified. Examples of printouts are provided to aid in location and identification of words (registers) and bits; and tables are used to relate to suspect packs, suspect leads and to provide trouble-clearing tips. In other procedures, analyzation is conducted in a procedural approach which utilizes the Point of Maximum Definition (PMD) to implicate the suspect circuits, packs, and leads. The method used is based upon the sophistication of the PMD relationship to the fault recognition program-generated printout. The level of interject or interrupt is an indication of the equipment involvement. Levels A, B, and C indicate Central Control (CC) or configuration involvement. Level D reflects Call Store (CS) or Interface BUS (IFB, AUI, MUP) involvement and Level E implicates the Program Store (PS). A maintenance interject is a less critical indication of a problem involving the AU BUS, API, DUS or TUC. It should not be ignored because of the of the tendency toward escalation into a more serious problem.

Key register data associated with interrupts and 1B Processor address table follows. For CC internal relationships see SD4A145-03 H sheets.

Tables

Table A lists the Interrupt Source Register (INS) bits. Table B lists the Interrupt Inhibit Register (ONH) bits. Table C lists the Central Control Status Flip-Flops Register (CSC) bits. Table D lists the CC Error Summary Register (CES) bits. Table E lists the IFBC Error Source Register (FES) bits. Table F lists the Peripheral Error Summary Register (PES) bits. Table G lists the Common Level Data (MI1CONT) bits. Table H shows the memory Layout.

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TABLE A – INTERRUPT SOURCE REGISTER (INS) (CONTINUED)

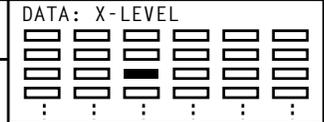
BIT	NAME	DESCRIPTION	BIT	NAME	DESCRIPTION
12	UTAS	Utility A-Level interrupt source. System can recover from this interrupt. This is a soft A (not acted upon until a convenient instruction is being acted upon). This interrupt can occur from GULP or utility functions. If set contact Technical Assistance Center.	16	MCPAS	MCC program (soft) A-Level interrupt source. This is a soft (deferred) interrupt - see bit 12. Poke 2 at MCC terminal. Reason set can be: I/O restore, utility clear, interrupt inhibit, or phase request.
13	ORDS	Out-of-range D-Level interrupt source. Caused by executing invalid instruction options or invalid address range (MMIO address range).	17	MCHA	MCC hard A-Level interrupt source. Select pump configuration or used to hardware switch CCs.
14	INBS	Internal error B-Level interrupt source. Could be BOOTROM parity failure - look at CES register. Also, could be mode parity failure. Automatically pests INH for this bit.	18	PSBS	Pulse source B-Level interrupt source. This should not be seen on a REPT: printout. If set on printout then interrupt source is stuck.
15	PSBSO	Pulse source B-Level has occurred (drives bit PSBS). This is an occurred bit meaning the bit set indicates history not a source of the interrupt. This bit caused by executing a GCP instruction that pulses no GCP or more than one GCP. Has to have the following format: one-out-of-six (bits 0-5), one-out-of-six (6-11), and one-out-of-ten (12-21). If it does not have this format the trouble is software. Unequipped GCPs can cause this interrupt. GCP output but no GCP instruction can also cause this interrupt.	19	PCBS	Processor configuration (PC) B-Level interrupt source. This should not be seen on REPT: printout. If set on printout then interrupt source is stuck.
			20	KL0S	K-Level interrupt source. If set interject was not served within a 10-20 ms time frame. This is a software problem unless running on a simplex CC with an unstable CC.
			21	SWBO	Switch CCs B-Level occurred (GCP PSWCCS) (drives bit PCBS). This is an occurred bit (see bit 15) for switch CC. When set CC has been switched.
			22	RBSO	PROM parity error or ASW failure B-Level occurred (drives bit INBS).
			23	CPBSO	Control parity B-level occurred (drives bit INBS).

TABLE B - INTERRUPT INHIBIT REGISTER (INH) (CONTINUED)

BIT*	NAME	DESCRIPTION	BIT	NAME	DESCRIPTION
22	IASWEPU	A one inhibits the setting of the ASWEPU flip-flop on the CB2 pack (KLW14). PU trouble if set.	23	IAPEPU	A one inhibits the setting of the APEPU flip-flop on the CB2 pack (KLW14). PU trouble if set.

* Bits 4-14, 17, 22, and 23 are under both program and manual control

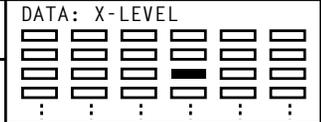
TABLE C – CENTRAL CONTROL STATUS FLIP-FLOPS REGISTER (CSC)



This register contains status bits relating to CC activity and bus usage. Under normal conditions, the contents of CSC are the same in both CCs. All bits are read only via the buffer bus. Most bits are set and cleared by GCPs.

BIT	NAME	DESCRIPTION	BIT	NAME	DESCRIPTION
0	PBO	A one causes the CC to send on both Program Store busses. Bit 13 indicates last software setting of this bit.	10	PUBA	A zero makes coded-enable PU bus 0 active. A one makes coded-enable PU bus 1 active.
1	PBA	A zero indicates Program Store bus 0 is active. A one indicates Program Store bus 1 is active	11	PUBT	A one means the standby CC receives from the active PUB. A zero means the standby CC receives from the standby PUB.
2	PBT	A one means the standby CC receives from the active PSB. A zero means the standby CC receives from the standby PSB.	12	PUBR	A one causes the active CC to send and receive on both coded-enable PU busses, overriding PUBT, PUBA, and PUB0. The standby CC receives on both busses.
3	CBO	A one causes the active CC to send on both Call Store busses. Bit 14 indicates last software setting of this bit.	13	PBOA	This bit indicates the last software setting of bit 0.
4	CBA	A zero indicates Call Store bus 0 is active. A one indicates Call Store bus 1 is active.	14	CBOA	This bit indicates the last software setting of bit 3.
5	CBT	A one means the standby CC receives from the active CSB. A zero means the standby CC receives from the standby CSB.	15	DIVA	This bit indicates the last software setting of bit 8.
6	CCACT	A zero indicates that CC 0 is active. A one indicates CC 1 is active.	16	–	Not used (zero).
7	TCC	A one marks the standby CC as having trouble. This primarily a software state. The only hardware effect of this bit is to block the activity switch that would otherwise occur in the transition from PC state 1 to 2.	17	–	Not used (zero).
			18	–	Not used (zero).
			19	–	Not used (zero).
			20	–	Not used (zero).
			21	–	Not used (zero).
8	DIV	A one places the CCs in "divorced" mode, blocking certain crossover connections and allowing the CCs to run independently. Bit 15 indicates last software setting of this bit.	22	FSTPTP	Freeze-stop or clear-stop indicator. A one indicates the maintenance matcher freeze-stops the standby CC. A zero indicates the standby CC receives a clear-stop instead.
			23	–	Not used (zero).
9	PUB0	A one causes the active CC to send on both coded-enable PU busses.			

TABLE D – CC ERROR SUMMARY REGISTER (CES)



This register provides access to the outputs of various error detectors and some related control signals in the CC. In normal operation its bits are clocked on each cycle, but the occurrence of an interrupt of priority E through B (if not inhibited) freezes the register contents. Bit FREZ in the INH register indicates these bits are frozen. GCP PSFREQ also sets the FREZ bit and freezes these status bits. Buffer Pulse Source (BPS) bit 8 (FREZR) clears FREZ and unfreezes these bits.

BIT	NAME	DESCRIPTION	BIT	NAME	DESCRIPTION
0	–	Not used (zero).	13	PSPER	A one indicates incorrect parity in the right (odd) word read from Program Store.
1	SCWOP	A one indicates a cycle was a write operation using the stack counter.	14	PSPEL	A one indicates incorrect parity in the left (even) word read from Program Store.
2	DPWECS	A one indicates a Call Store detected bad write data parity.	15	CSASWE	A one indicates no ASW response from Call Store.
3	DPWEPS	A one indicates a Program Store detected bad write data parity.	16	CSASWF	A one indicates a Call Store has detected an error.
4	SBRP0	Parity over BR bits 0-7 (byte 0).	17	CSPE	A one indicates incorrect parity in a word read from Call Store.
5	SBRP1	Parity over BR bits 8-15 (byte 1).			
6	SBRP2	Parity over BR bits 16-23 (byte 2).			
7	SBRP3	Parity over BR bits 24-31 (byte 3).			
		On D/E level read-parity as read from the store.	18	RASWE	A one indicates a BOOTROM ASW error - no ASW reply.
8	IFASWE	A one indicates an IFB client did not give an ASW response to an MMIO order.	19	RASWF	A one indicates BOOTROM has detected an error.
9	IFPE	A one indicates a parity error on an MMIO response.	20	RPER	A one indicates incorrect parity in the right (odd) word read from BOOTROM.
10	IFASWF	A one indicates an IFB client has detected an error and is reporting it.	21	RPEL	A one indicates incorrect parity in the left (even) word read from BOOTROM.
11	PSASWE	A one indicates no ASW response from Program Store.	22	MTCCS	A one causes the "m" bit to be set for Call Store data accesses.
12	PSASWF	A one indicates a Program Store has detected an error.	23	MTCPS	A one causes the "m" bit to be set for Program Store data accesses.

TABLE G - COMMON LEVEL DATA (MI1CONT)		DATA: X-LEVEL @ <input type="checkbox"/> MFNUM= <input type="checkbox"/> MICON= <input checked="" type="checkbox"/>	
BIT	DESCRIPTION	BIT	DESCRIPTION
0	MARP return to reference point.	12	An out-of-range Call Store D-Level.
1	MARP return by rolling back to intermediate level.	13	An out-of-range Program Store E-Level.
2	MARP return by rolling ahead to intermediate level.	14	An out-of-range peripheral F-Level.
3	Audit in progress flag.	15	Request hash sum of area indicated in MI1HASHADRS.
4	In restart flag.	16	A maintenance phase record is to be formed by ERAP.
5	CC's have been switched	17	A software error has occurred.
6	A pump of Call Store(s) has been performed.	18	MARP invalid interrupt entry.
7	A pump of Program Store(s) has been performed.	19	SAWS routine has pumped 1 bink on INT Level.
8	Non-backed up area has been zeroed.	20	Call Store duplex failure has occurred.
9	A phase (indicated in MI1PHASEPT) has been requested.	21	Application work flag 2.
10	A pulse source B-Level has occurred.	22	Application work flag 1.
11	An out-of-range pulse source B-Level.	23	Application work flag 0.

TABLE H - MEMORY LAYOUT

30-bit ADDRESS	MCODE	24-BIT ADDRESS (Adr Bits 23-29=ones)	LOCATION	DESCRIPTION
0000000000 - 1777777777	0 - 377		Windowed CS (XS)	XS - Extended Store
2000000000 - 2377777777	400 - 477		Windowed PS	Reserved for future Extended Program Store
2400000000 - 3777777777	500 - 777		Expanded MMIO	Reserved for future Expanded Memory Mapped IO
4000000000 - 5777777777	1000 - 1377		Windowed MMIO (XM)	Reserved for future (XM) (Extended Memory Mapped IO)
6000000000 - 7737777777	1400 - 1767		Expanded MMIO	Reserved for future Expanded Memory Mapped IO
7740000000 - 7747177777	1770 - 1771	00000000 - 07177777	Lower CS	High Usage CS, COMPOOL, ODA Engineered, Utility, and ODA Translation
7747200000 - 7747377777	1771	07200000 - 07377777	Lower CS	Library area
7747400000 - 7747777777	1771	07400000 - 07777777	Lower CS	Common ODA Translators, loader populated programs and tables
7750000000 - 7753777777	1772	10000000 - 13777777	PS	Generic code
7754000000 - 7754237777	1773	14000000 - 14237777	PS	80K Pump area and Vector table start addr- 14000000. Bonded interrupt handlers- 14020000.
7754240000 - 7757777777	1773	14240000 - 17777777	PS	Generic code
7760000000 - 7767777777	1774 - 1775	20000000 - 27777777	Upper CS	Spare Upper CS area, ODA Engineered, COMPOOL, Generic code, and ODA translation

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TABLE H – MEMORY LAYOUT (Cont.)

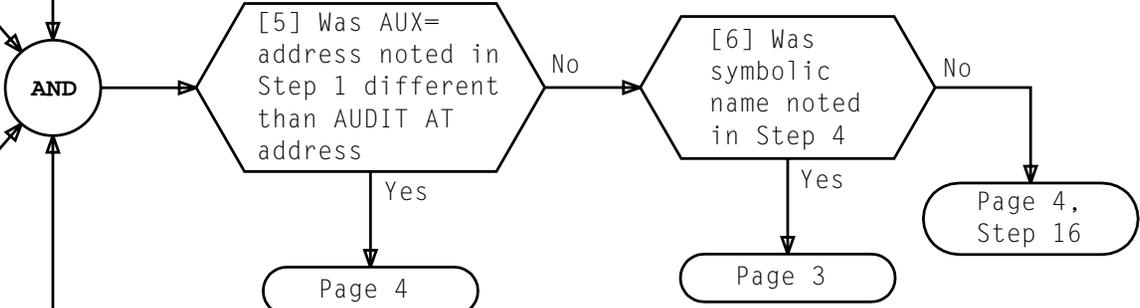
30-bit ADDRESS	MCODE	24-BIT ADDRESS (Adr Bits 23-29=ones)	LOCATION	DESCRIPTION
7770000000 - 7773577777	1776	30000000 - 33577777	Upper CS	ODA translation
7773600000 - 7773617777	1776	33600000 - 33617777	Upper CS	Extended Access (XA) Window 0
7773620000 - 7773637777	1776	33620000 - 33637777	Upper CS	Extended Access (XA) Window 1
7773640000 - 7773657777	1776	33640000 - 33657777	Upper CS	Extended Access (XA) Window 2
7773660000 - 7773677777	1776	33660000 - 33677777	Upper CS	Extended Access (XA) Window 3
7773700000 - 7773717777	1776	33700000 - 33717777	Upper CS	Extended Access (XA) Window 4
7773720000 - 7773737777	1776	33720000 - 33737777	Upper CS	Extended Access (XA) Window 5
7773740000 - 7773757777	1776	33740000 - 33757777	Upper CS	Extended Access (XA) Window 6
7773760000 - 7773777777	1776	33760000 - 33777777	Upper CS	Extended Access (XA) Window 7
7774000000 - 7777577777	1777	34000000 - 37577777	PSE	Program Store Expansion
7777600000 - 7777670377	1777	37600000 - 37670377	MMIO	Fixed MMIO
7777670400 - 7777677777	1777	37670400 - 37677777	MMIO	Fixed MMIO - unused
7777700000 - 7777677777	1777	37700000 - 37767777	ROM	BOOTROM
7777700000 - 7777677777	1777	37770000 - 37775777	Buffer Bus	Unused
7777776000 - 7777776377	1777	37776000 - 37776377	Buffer Bus	Active CC
7777776400 - 7777776777	1777	37776400 - 37776777	Buffer Bus	Standby CC
7777777000 - 7777777377	1777	37777000 - 37777377	Buffer Bus	Invalid Address
7777777400 - 7777777777	1777	37777400 - 37777777	Buffer Bus	Internal CC

SUMMARY

Using AUDIT AT and AUX= addresses, determine PIDENT that called for message print and failure point calling for AUDIT. Using starting address of PIDENT, convert the addresses above to relative addresses. Using

PIDENT, locate relative addresses and scan program listing backward from address points for comments related to AUDIT CALL, data structures passed to AUDITS, and data in CC REGs at time of AUDIT CALL. Decode data structures and CC REGs to determine possible cause of AUDIT AT message

- [1] Using loader map, identify, then obtain PIDENTs containing AUDIT AT and AUX= addresses from printout [Figure 1]
- [2] Convert AUDIT AT and AUX=addresses to relative addresses within PIDENTs [DLP-509]
- [3] In PIDENT containing AUDIT AT address, scan backward from the relative address of AUDIT AT address to entry point of audit call [Figure 2, Page 2]
- [4] Note comments indicating reason for AUDIT CALL, entry point symbolic name (if there is one), CC REGs listed and contents, and data structures passed to AUDITS [Figure 2, Page 2]



```

05  AUDIT CALL AT 16150430 AUX= 16150430 CLIENT= MTC
    MISCELLANEOUS DATA INVALID
    MAC SYSTEM TROUBLE DETECTED
    CC REGS
    L=00000077 F=77767777 G=00140000 J=16140734
    K=00012022 X=00031046 Y=00000002 Z=00000002
    SHADOW REGS
    L=00004172 F=77767777 G=00140000 J=16140734
    K=00012022 X=00000072 Y=00000001 Z=00000071
    DATA:
    16143006 16140736
    12/15/88 08:03:17
    #431
    
```

AUDIT AT AND AUX= ADDRESSES WHEN THEY ARE DIFFERENT: NOTE BOTH

Figure 1 - Sample of the Audit Call at Message

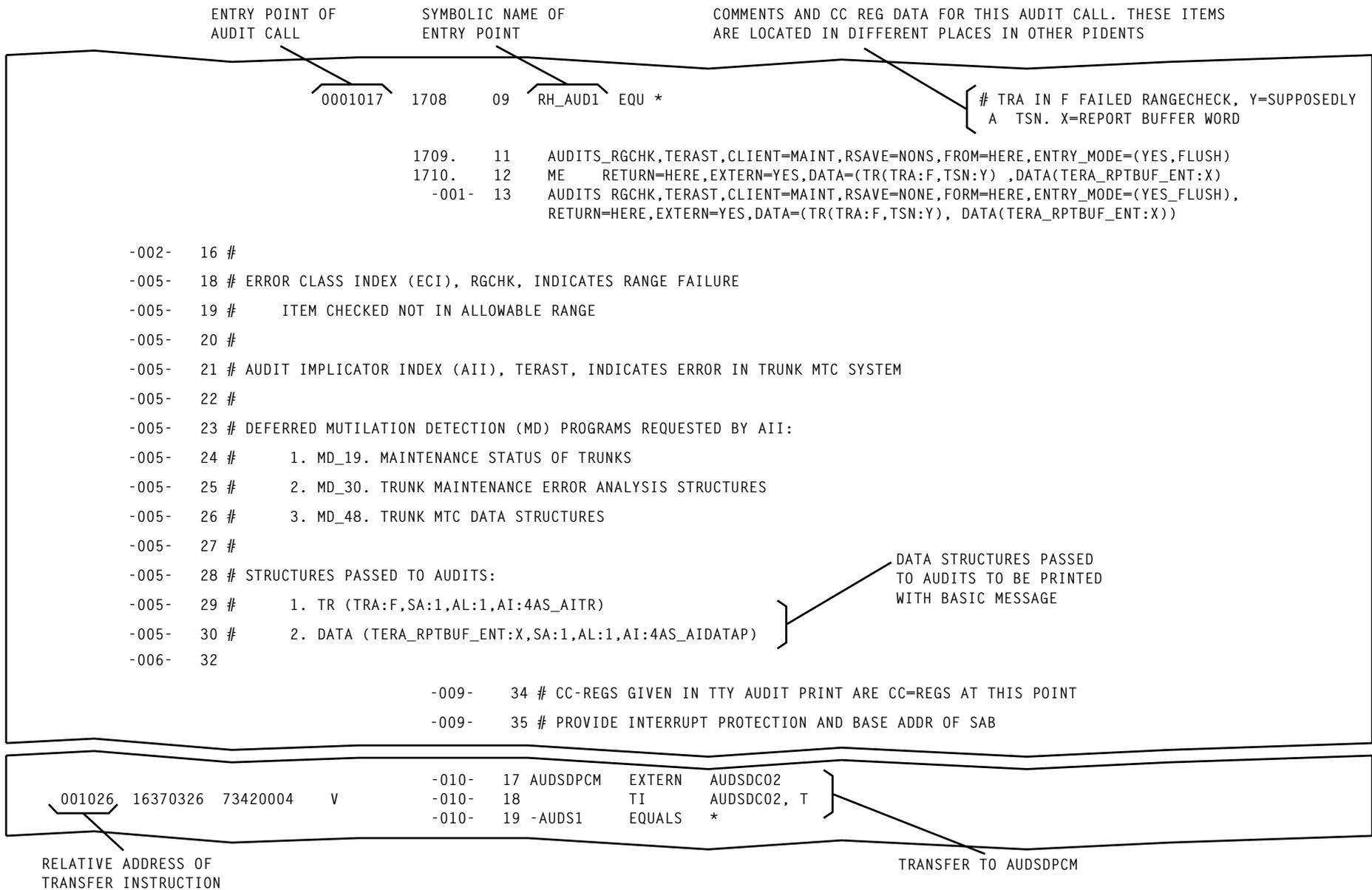


Figure 2 - Sample of PIDENT Audit Call Expansion

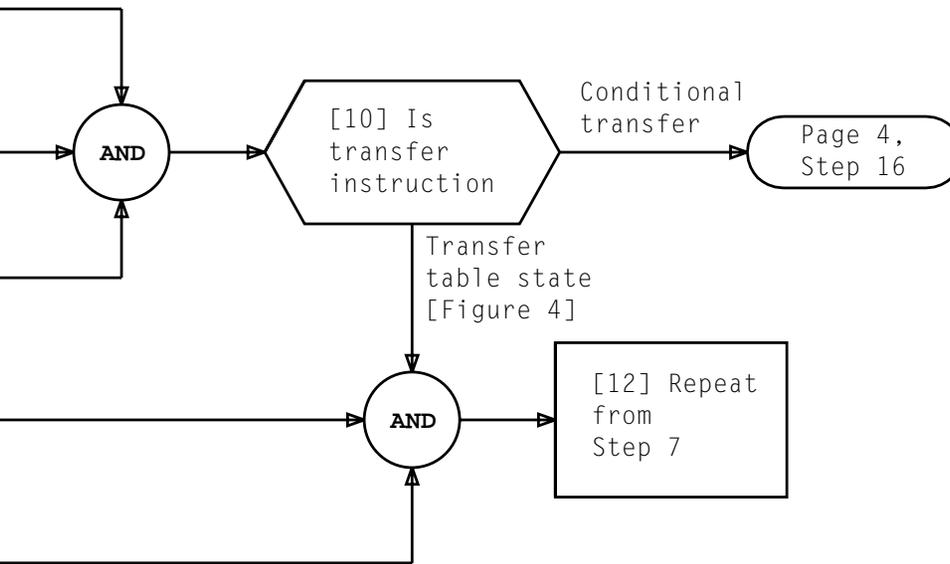
[7] Locate symbolic name in REF/DEF section of PIDENT

[8] Note reference page and line numbers listed for symbolic name [Figure 3]

[9] Locate page and line number in PIDENT

[11] Scan backward through PIDENT to entry point of transfer table

[13] Note symbolic name of entry point



SYMBOLIC NAME	DEF PAGE AND LINE NUMBER	REF PAGE AND LINE NUMBER
1020 L RH_AUDLT	71-39	65-44, 66-14, 102-12, 102-13, 102-14, 102-15
1017 L RH_AUD1	70-06	37-23, 37-25,
766 L RH_BRKCK	68-05	39-07, 39-07, 41-13, 41-22, 43-05, 44-15

Figure 3 - Example From PIDENT REF/DEF Section

007175	15605703	63400200	007375	-003-	22	T	AUDODOT	# STATE 0 IS UNASSIGNED ()
007176	15605704	77400400		-003-	23	T	0(TI)	# STATE 1=4CROGT_AUD1 (AUDIT STATE_IGNORE REPORT
007177	15605705	63400176	007375	-003-	25	T	AUDODOT	# STATE 2 IS UNASSIGNED ()
007200	15605706	63400175	007375	-003-	26	T	AUDODOT	# STATE 3 IS UNASSIGNED ()

Figure 4 - Sample From PIDENT Transfer Table

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[14] In PIDENT containing AUX=
address, locate line of
relative address found in
Step 2

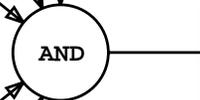
[15] Back up one instruction line
and note transfer instruction
to AUDIT CALL

[16] Scan backward through PIDENT noting
what program was doing when audit
was called [Figure 5, Page 5]

[17] Note data being
checked or compared
and location recorded

[18] Analyze CC REGs
and/or data
structures noted

[19] Determine source
of data in error



ANALYZE AUDIT AT MESSAGE

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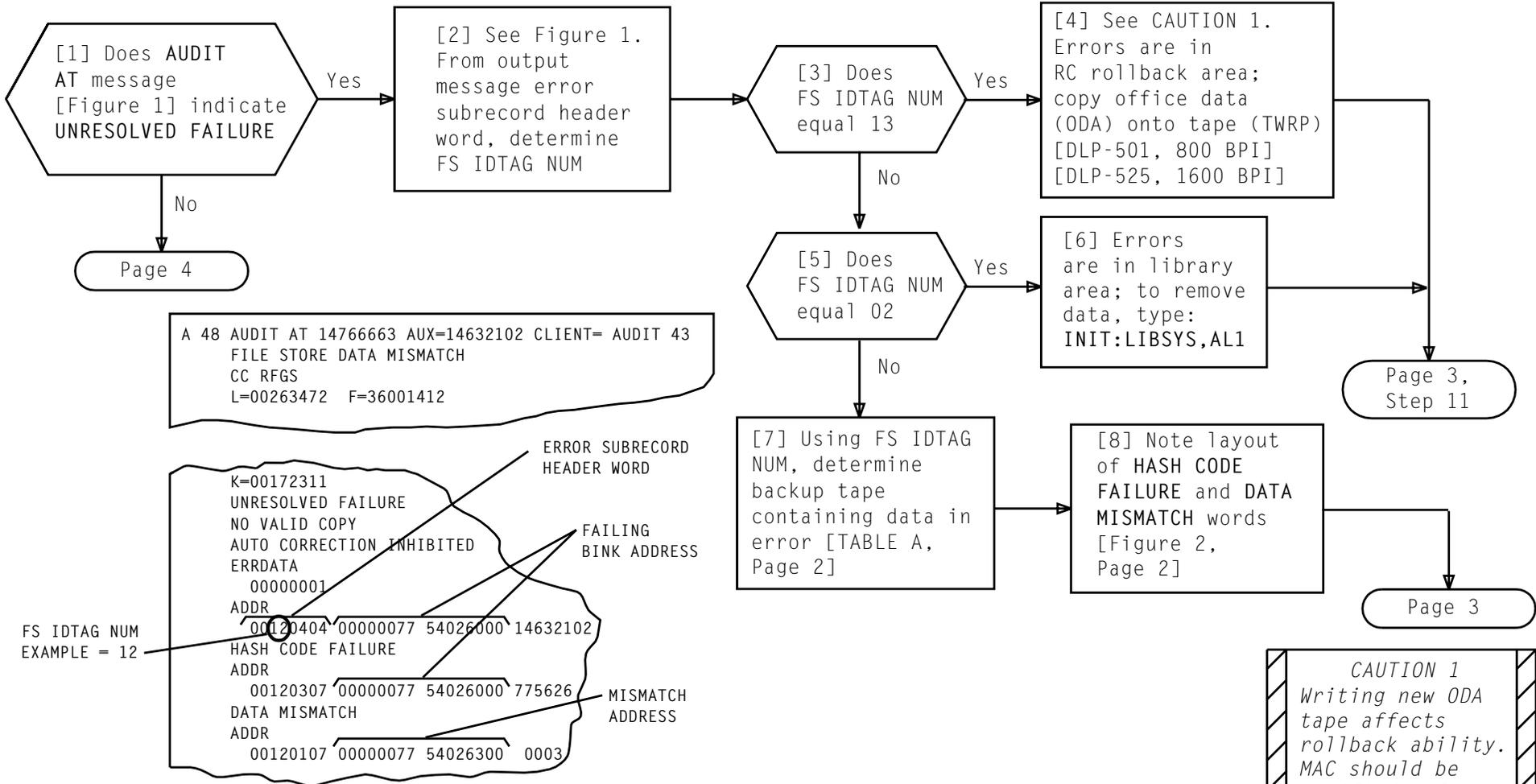
		PAGE LINE NUMBER	
0000024	1024	10	RH_RPT EQU * #1(RH-RPT)
		11	# HAVE A REPORT TO HANDLE: X = FULL WORD FROM REPORT BUFFER
		12	# F = FULL POINTER WORD, UNLOAD SET FOR STORING.
0000024 16367324 3200234 000205146	1027	13	S F,A(TE4BUFPTRS) #1 STORE ALREADY INCREMENTED UNLOAD POINTER
		14	#1 DECODE THE REPORT CODE ITEM IN X REMOVE.TSN.FROM.EA (RHRMVTEA), NEW. TSN. NO. TEST (RHNWNTST),NEW.TSN.TEST.PASSD (RHNTSTPD),RPT.ON.TRUNK.IN.EA(RHRPEATK)
16251000		16	LWA Y(0),0(X),PM (TE4RPTTSN) # REPORTED TSN
		17	CONVERT TSN:Y,TRA:F
3220322500256000		18	AW YF,TR4TR(Y)
		19	RANGECHECK TR(TRA:F),GOTO=FAIL:RH_AUD1 # TEMP.DEFENSIVE CHECK
		21	# RANGECHECK TRUNK REGISTER
3220224000256002		22	CW F,TR4TR+2
43400754 R		23	IF:T C=LT:RH_AUD1
3200224007640240		24	C F,0D4MAXTR
43000751 R		25	IF:T C=GT:RH_AUD1
		26	LWA K(1),0(X),PM(TE4RPTCODE)
		27	T RHRPTCDT(K)

A RANGE CHECK OF THE TRUNK REGISTER IS PERFORMED AT THIS POINT IN THE PROGRAM

A TRANSFER TO AUDIT CALL IS MADE WHEN TR IS FOUND OUT OF RANGE

Figure 5 - Sample of Error Condition Transfer to Audit Call

<p style="text-align: center;">SUMMARY</p> <p>Using AUDIT AT output message, determine FS IDTAG NUM. If message indicates UNRESOLVED FAILURE and FS IDTAG NUM is not 02 or 13, perform TAPE AUDIT (SAST) with appropriate</p>	<p>system backup tape [TABLE A]. If FS IDTAG NUM is 13, copy office data onto tape (TWRP). If FS IDTAG NUM is 02, type INIT:LIBSYS message. If UNRESOLVED FAILURE is not indicated, analyze data and look for possible cause of errors</p>
---	--



```

A 48 AUDIT AT 14766663 AUX=14632102 CLIENT= AUDIT 43
FILE STORE DATA MISMATCH
CC RFGS
L=00263472 F=36001412
  
```

```

K=00172311
UNRESOLVED FAILURE
NO VALID COPY
AUTO CORRECTION INHIBITED
ERRDATA
00000001
ADDR
00120404 00000077 54026000 14632102
HASH CODE FAILURE
ADDR
00120307 00000077 54026000 775626
DATA MISMATCH
ADDR
00120107 00000077 54026300 0003
  
```

Labels in diagram:
 - ERROR SUBRECORD HEADER WORD: points to 'UNRESOLVED FAILURE'
 - FAILING BINK ADDRESS: points to '00120404'
 - MISMATCH ADDRESS: points to '00120307'
 - FS IDTAG NUM EXAMPLE = 12: points to '00120404'

CAUTION 1

Writing new ODA tape affects rollback ability. MAC should be notified before proceeding

Figure 1 - Sample of (Partial) Saws Audit Error Message

ANALYZE AUDIT 43, 44, 45, AND 66 ERRORS

HASH CODE FAILURE

DATA:

aaaaaaaa bbbbbbbb bbbbbbbb cccccccc dddddddd eeeeeeee ffffffff

DATA MISMATCH

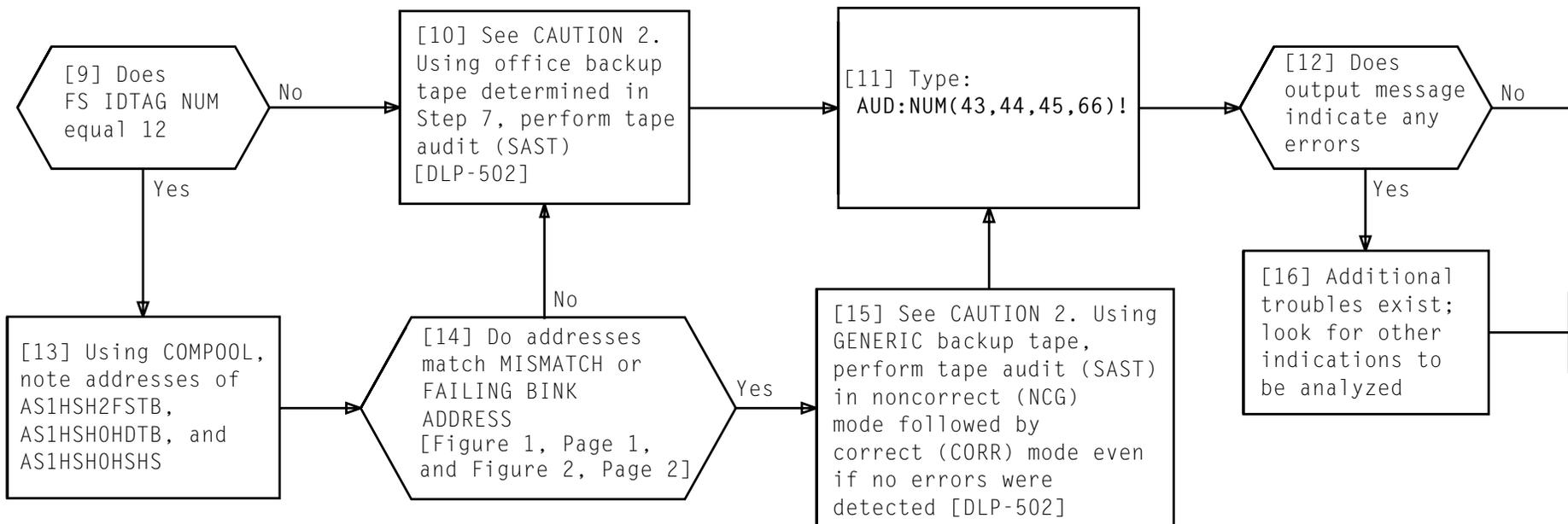
DATA:

aaaaaaaa bbbbbbbb bbbbbbbb cccccccc dddddddd eeeeeeee ffffffff

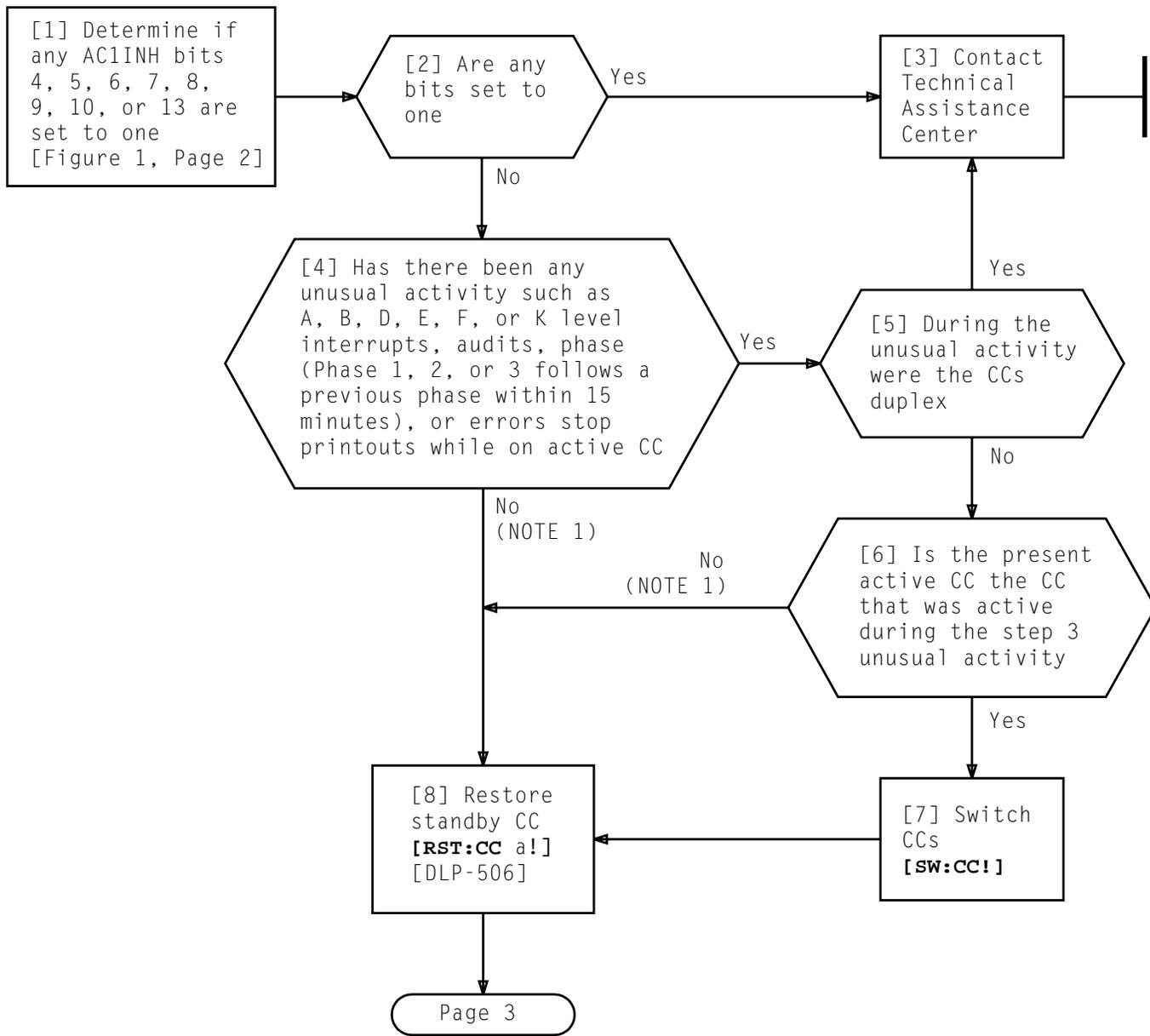
WORD	FOR HASH CODE FAILURE	FOR DATA MISMATCH
a	ERROR SUBRECORD HEADER	ERROR SUBRECORD HEADER
b	FAILING BINK ADDRESS	MISMATCH ADDRESS
c	CORE-RESIDENT STORE HASH SUM	FILE STORE ADDRESS
d	COMPUTED FS 1 HASH SUM	FS 1 DATA
e	COMPUTED FS 0 HASH SUM	FS 0 DATA
f	COMPUTED CORE HASH SUM	CORE DATA

Figure 2 – Layout of Hash Code Failure and Data Mismatch Words

TABLE A		
FS ID TAG NUM	FS AREA NAME	OFFICE BACKUP TAPE TO USE
01	GENERIC PROGRAM	GENERIC
03	OFFICE DATA	ODA
07	NETWORK MANAGEMENT	NTWK MGT
12	MERGE:FOR CORE- DISK AND HASH TBL	GENERIC
14	TRAFFIC/PLANT MEASUREMENT	TR/PLT MEAS
21	PAGED PROGRAM	GENERIC
24	ODA FILE SEGMENT 1	ODA
25	ODA FILE SEGMENT 2	ODA
26	ODA FILE SEGMENT 3	ODA



<i>CAUTION 2</i>	
<i>Software change packages (SCPs), entered since last backup tape was written, is lost at this point and must be reentered</i>	
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NOTE 1	
Because active CC is stable, suspect standby CC.	
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REPT:C-LEVEL @ 14234567 MFNUM=00012345 MICON=00000002 MSG STARTED
 LV=0004 D0=00000000 D1=00000000 D2=00000000 D3=00000000
 CCFR REMOVED CC 1
 DATA: C-LEVEL

	AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR	
	AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASC(H)	AC1ASC(L)	
	AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES	
	AC1ILR	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR	
	<SC+1>	ST1INS	AC1LIT(E)	AC1LPI	AC1ER	AC1PRM	
	AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1ASC(H)	ST1ASC(L)	
	ST1SCA	ST1SDA	ST1BRS(H)	ST1BRS(L)	AC1MEO(H)	AC1MEO(L)	(ADAN)
	ST1LIT	ST1LPI	AC1MSR	AC1MMR	ST1MIO(H)	ST1MIO(L)	
(AFAN)	AC1MIO(H)	AC1MIO(L)	AC1ME1(H)	AC1ME1(L)	AC1MI1(H)	AC1MI1(L)	(DBR)
	ST1MEO(H)	ST1MEO(L)	ST1MI1(H)	ST1MI1(L)	ST1ME1(H)	ST1ME1(L)	
	AC1SAT	AC1TAR	AC1BNCTL				(DADB)

DATA: ACTIVE CC REGISTERS

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1SR	AC1SC	AC1CES	AC1IBR
AC1INS	AC1INJ	AC1ILA	AC1ILR	AC1ITR	AC1INH
AC1CSC	AC1SAT	AC1PCR	AC1MCLK	AC1LIT	AC1DLR
AC1LPA	AC1UPA	AC1ACT	AC1ER	AC1PRM	AC1PRL
AC1LPI	AC1PES	AC1PSC	AC1PSQ	AC1RPO	AC1RP1
AC1PM0	AC1PM1	AC1ABC	AC1SAL	AC1SAR	AC1FIS
AC1EPS	AC1IFR	AC1MMR	AC1MSR	AC1MCO(H)	AC1MCO(L)
AC1MCD(H)	AC1MCD(L)	AC1MCP	AC1CCS(H)	AC1CCS(L)	AC1CUI
AC1FCT	AC1FCE	AC1FES	AC1FEE	AC1FER	AC1FST
AC1FLA(H)	AC1FLA(L)	AC1FLD(H)	AC1FLD(L)	AC1FLT(H)	AC1FLT(L)
AC1FRU(H)	AC1FRU(L)	AC1FRL(H)	AC1FRL(L)	AC1FIP	AC1CLE

DATA: STANDBY CC REGISTERS

ST1FR	ST1GR	ST1JR	ST1KR	ST1LR	ST1XR
ST1YR	ST1ZR	ST1SR	ST1SC	ST1CES	ST1IBR
ST1INS	ST1INJ	ST1ILA	ST1ILR	ST1ITR	ST1INH
ST1CSC	ST1SAT	ST1PCR	ST1MCLK	ST1LIT	ST1DLR
ST1LPA	ST1UPA	ST1ACT	ST1ER	ST1PRM	ST1PRL
ST1LPI	ST1PES	ST1PSC	ST1PSQ	ST1RPO	ST1RP1
ST1PM0	ST1PM1	ST1ABC	ST1SAL	ST1SAR	ST1FIS
ST1EPS	ST1IFR	ST1MMR	ST1MSR	ST1MCO(H)	ST1MCO(L)
ST1MCD(H)	ST1MCD(L)	ST1MCP	ST1CCS(H)	ST1CCS(L)	ST1CUI
ST1FCT	ST1FCE	ST1FES	ST1FEE	ST1FER	ST1FST
ST1FLA(H)	ST1FLA(L)	ST1FLD(H)	ST1FLD(L)	ST1FLT(H)	ST1FLT(L)
ST1FRU(H)	ST1FRU(L)	ST1FRL(H)	ST1FRL(L)	ST1FIP	ST1CLE

Figure 1 - C-Level Interrupt Printout Register Identification

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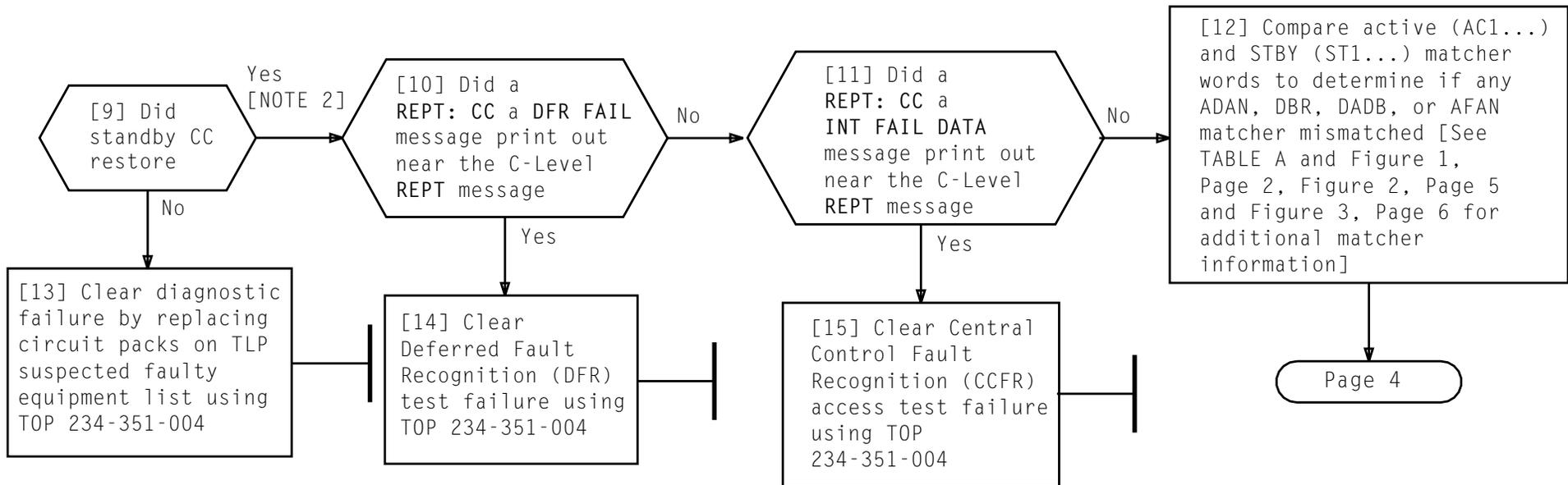
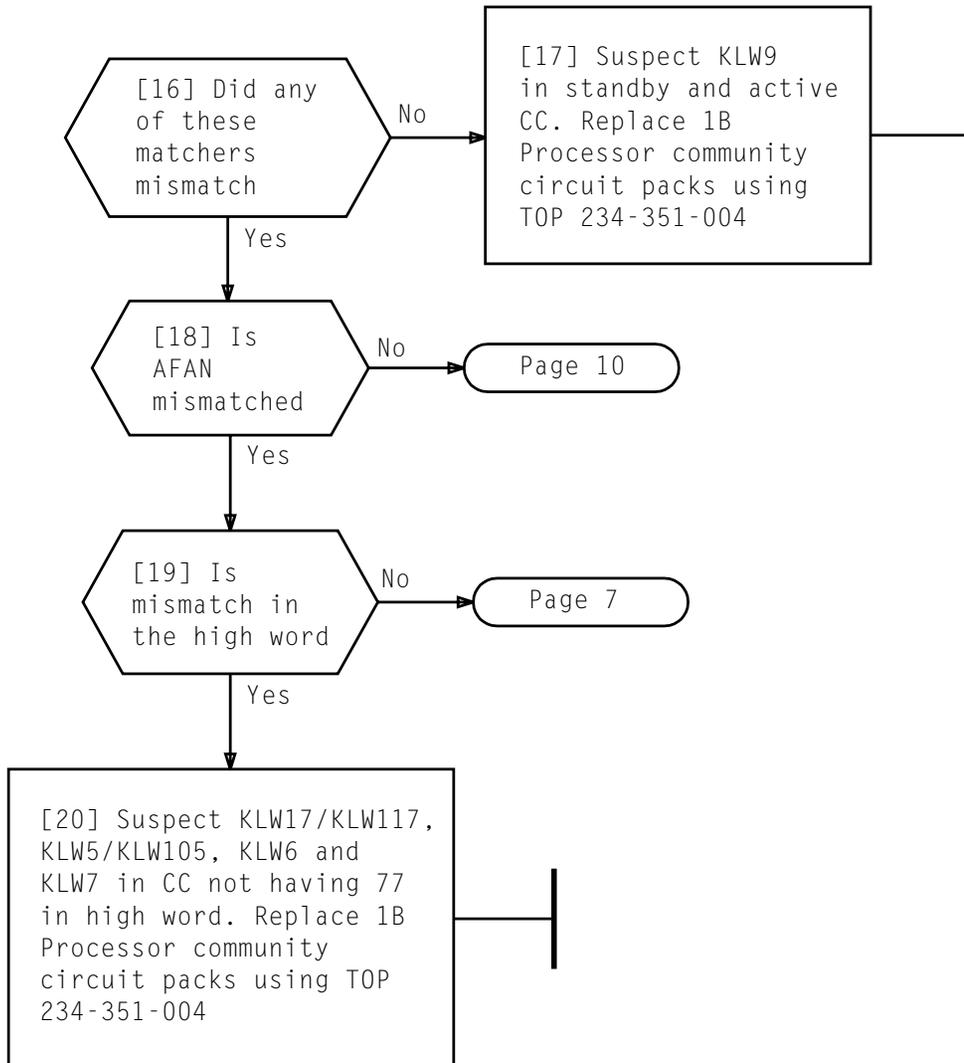


TABLE A - MATCH SUMMARY REGISTER (MSR) LAYOUT			
BIT	HARDWARE NAME	DESCRIPTION	ACCESS
0	MACT	Matcher Active	R
1	MLIERR	Matcher Latched Internal Error	R
2	MLEERR	Matcher Latched External Error	R
10	MOI	Internal Matcher 0 Error Latched Output	R/W
11	MOE	External Matcher 0 Error Latched Output	R/W
12	M1I	Internal Matcher 1 Error Latched Output	R/W
13	M1E	External Matcher 1 Error Latched Output	R/W
16	MAOI	Direct Output Internal Matcher 0 Error	R
17	MINO	Direct Output External Matcher 0 Error	R
18	MA1I	Direct Output Internal Matcher 1 Error	R
19	MIN1	Direct Output External Matcher 1 Error	R

NOTE 2	
Because active CC is stable, suspect standby CC	
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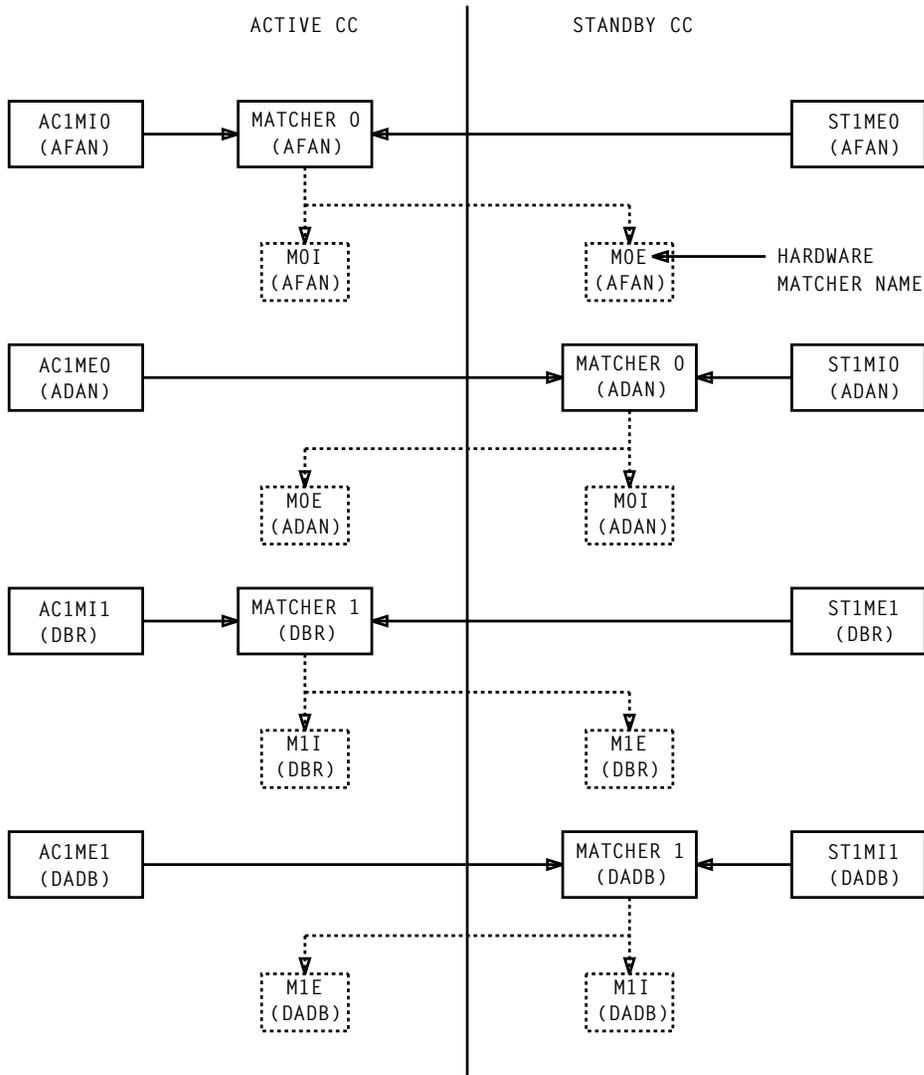


```

REPT: C-LEVEL @54054054 MFNUM=00000221 MICON=00000021 MSG STARTED
LV=0004 D0=01140002 D1=00000000 D2=00000000 D3=00021600
CCFR REMOVED CC 1
DATA: C-LEVEL
00000762 00000370 40000000 00000371 00000770 00000000
00000000 00037022 00000000 00000000 00000277 54054054
54054053 40037026 00000411 00000261 57630003 00000000
00000004 00004000 76000003 04000000 00000003 13530236
12202614 00004000 00000000 52200044 01010000 00001540
00000300 00000000 00000000 40000000 00000177 54054054
54054053 40037022 00000000 00000370 00000077 40037023
22334154 52200044 00004006 00010007 00000077 40037017
00000077 54054054 00000000 00000370 00000000 00000370
00000077 54054054 00000000 00000370 00000000 00000370
00100040 00000177 77777400
DATA: MAC CONTROL MEMORY
66421200 00100020 15102450 15105050 40173000 00064047
02400022 04600010 00000000 00000000 00067000 00007021
00000001 61001700 14450270 00000000 00000244 54044312
00000020 00000000 00000000 00000000 00000000 00000000
00000000 00010000 00000000 00000000 00000000 00000000
DATA: ACTIVE CC REGISTERS
00000762 00000370 40000000 00000371 00000770 00000000
00000000 00037022 13530236 00000003 00000261 14000000
00004000 04000000 00000004 00010004 23420000 76000003
00000411 00100040 00000200 04474602 04452452 00200000
40030000 46460000 00003777 01010000 00001540 00000300
52200044 00060000 00000000 00003000 00000000 00000000
61000000 62000002 00000771 14132041 32002347 00012642
00010001 00000003 00010007 00004006 00000377 40012525
00000000 00040000 00102000 00000205 61742677 76040206
00310030 00006002 00000000 01337333 00000000 57630003
00000000 00000000 00000000 00000000 00000200 02425012
00000000 00000000 00000000 00000000 00000000 00000000
07/05/93 13:56:18
#274

```

Figure 2 - Example of ADAN Mismatch



NAME	BITS	SIGNAL	MATCHER	CC WHERE MATCHED
AFAN	32	FETCH ADDRESS BUS	0	ACTIVE
ADAN	30	DATA ADDRESS BUS	0	STANDBY
DBR	32	BUFFER REGISTER	1	ACTIVE
DADB	32	ALU OUTPUT BUS	1	STANDBY

Figure 3 - CC Matchers (See NOTE 3)

NOTE 3 Dashed lines indicate matcher error sources	
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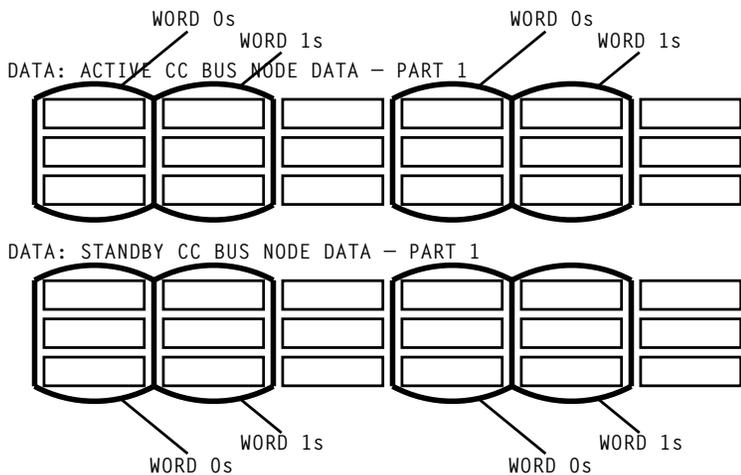
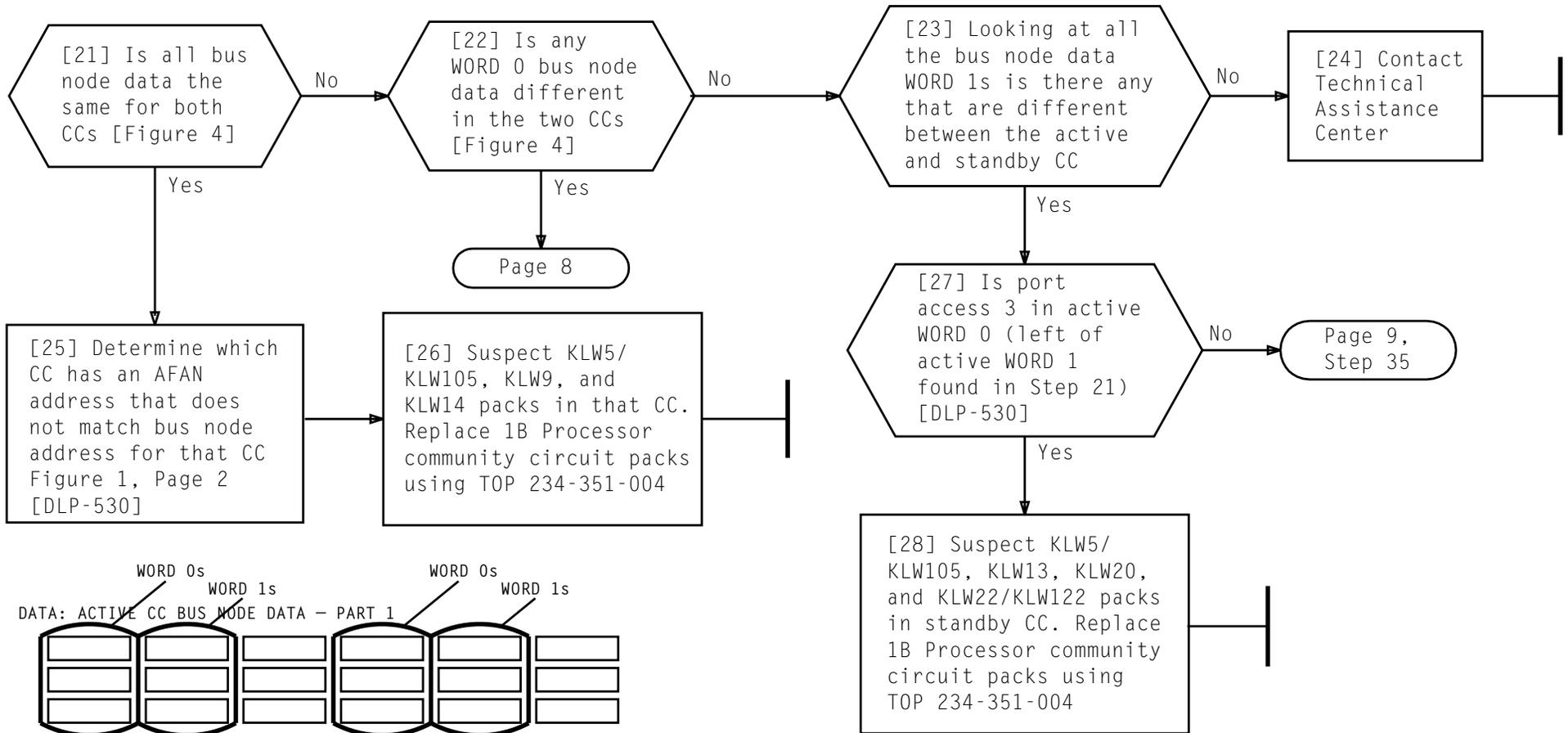


Figure 4 - CC Bus Node Data

[35] Compare active CC pipeline history 4 word combinations (SCA, SDA(H), SDA(L), EPH), to standby CC pipeline history 4 word combinations, from oldest to newest, looking for the first combination that is different [NOTES 5 and 6, and Figure 5, Page 8]

[36] Find 4 WORD combination (SCA, SDA(H), SDA(L) EPH) just before Step 35 4 WORD combination

[37] Find the instruction identified at SCA WORD ADDRESS [DLP-509]

[38] Examine what occurred at this instruction to determine which CC went the wrong way [NOTE 7]

[40] Suspect K LW6, K LW16, and K LW5/ K LW105 pack in CC identified in Step 38. Replace 1B Processor community circuit packs using TOP 234-351-004

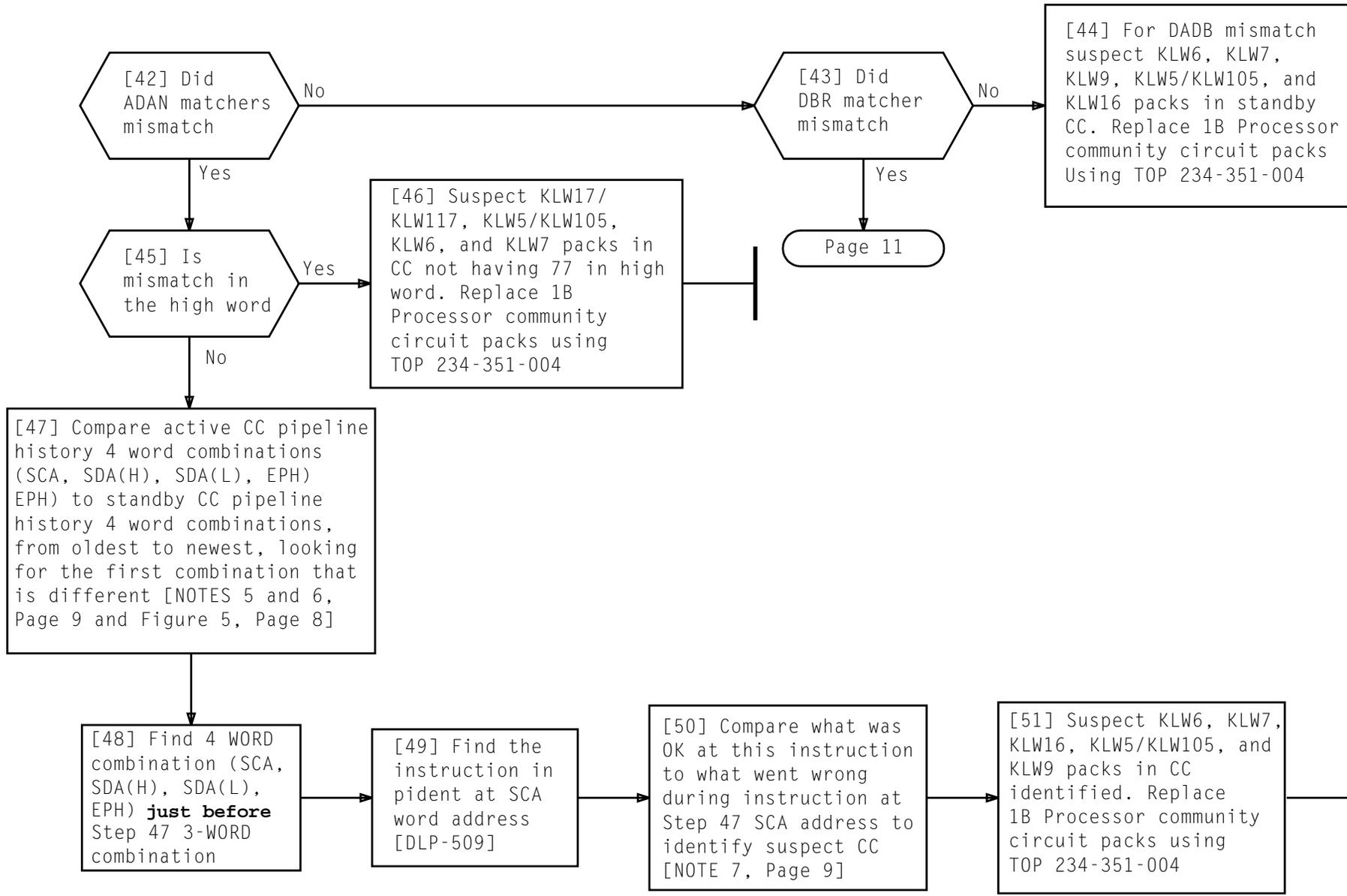
[39] Was this instruction a conditional type of instruction

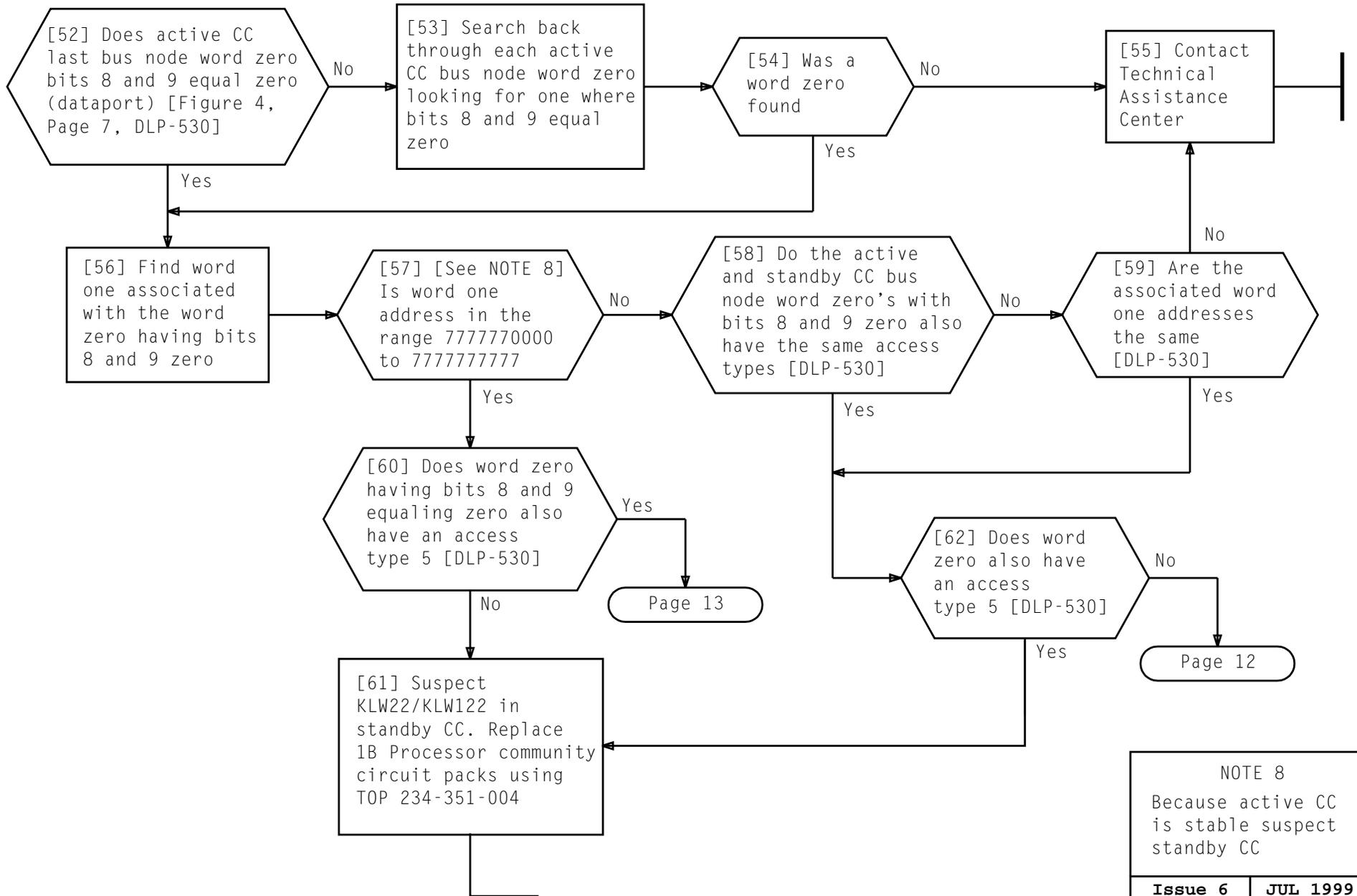
[41] Suspect K LW17, K LW117 pack in CC identified in Step 38. Replace 1B Processor community circuit packs using TOP 234-351-004

NOTES

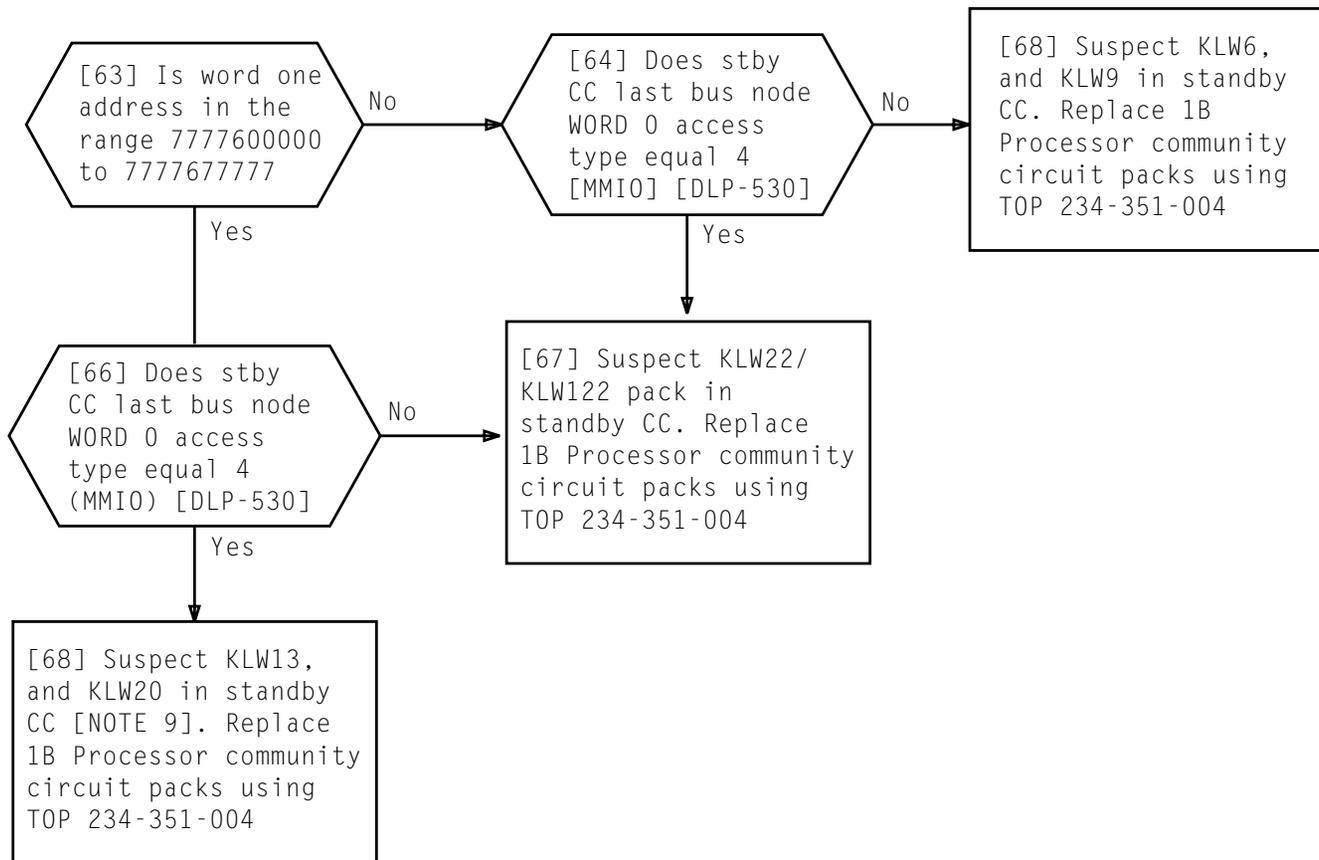
5. Figure 5, Page 8 shows active CC, standby CC has same format.
6. Four word combinations should be read left to right and top to bottom. Oldest is at top left and newest is at bottom right.
7. Listing instruction and CC registers at that point should be examined to determine what the CC should have done. The CC that didn't do that went the wrong way.

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NOTE 8	
Because active CC is stable suspect standby CC	
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NOTE 9	
IFB client addressed could also be source of C-level	
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[69] Word one address is in the range

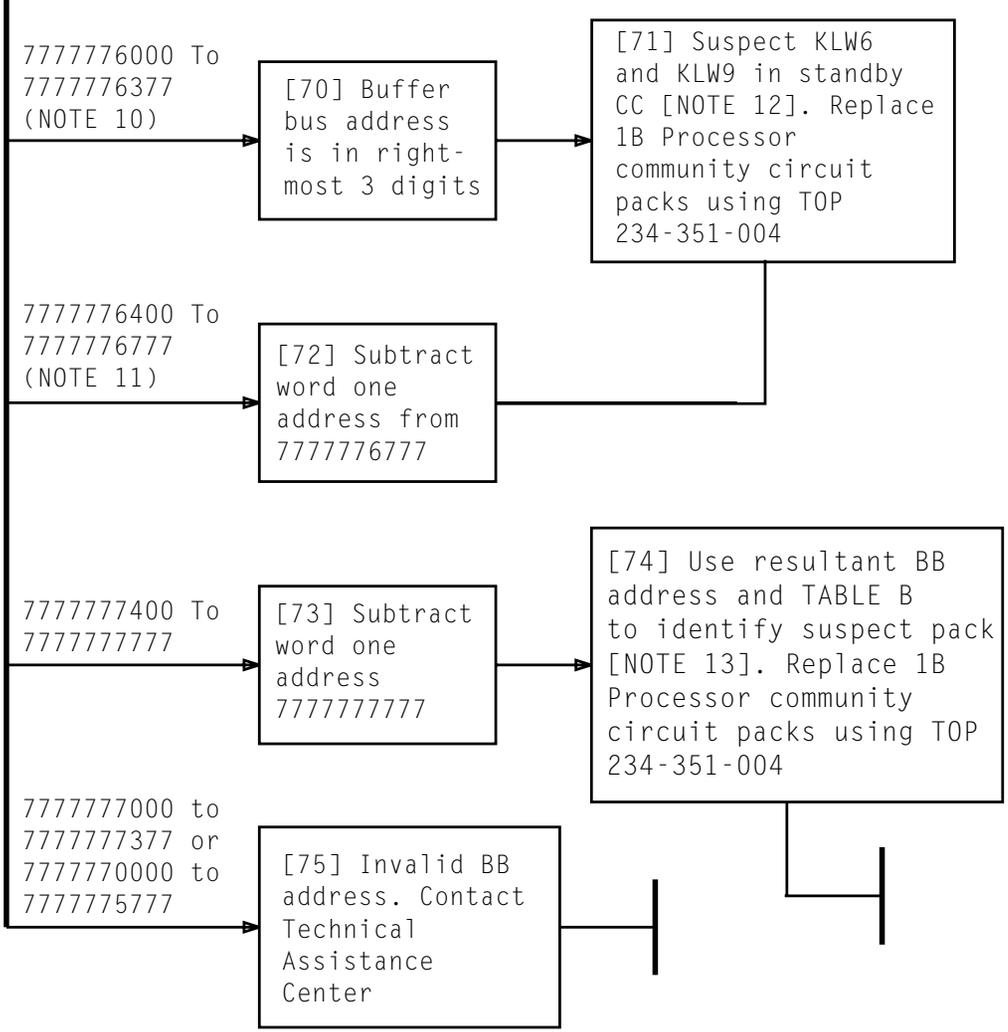


TABLE B - BUFFER BUS PACKS		
BUFFER BUS ADDRESS	PACK	LOCATION
000-002, 010-035	KLW22/KLW122	41-120
200-203	KLW24	41-062
204-206, 274-276	KLW19	41-070
211-215	KLW21	58-046
40, 41, 50-57, 230-257, 270-273, 335	KLW17/ KLW117	41-086
260-267	KLW7	41-078
300-306	KLW14	58-038
310-315, 317, 330-334, 040-041, 050-057	KLW5/ KLW105	41-096
320-326	KLW9	41-038
340-357	KLW8	41-046
360, 361, 370, 371	KLW20	58-062
362-367, 372, 373	KLW13	58-070
374-377	KLW6	41-054

NOTES

- Active CC was addressed at time of interrupt.
- Standby CC was addressed at time of interrupt.
- KLW9 could be suspect in either CC.
- Each CC addressed itself at the time of the interrupt - suspect standby CC.

[1] [NOTE 1] Using contents of AC1JR, AC1SCA, and SR registers reconstruct program in progress at time of interrupt to help isolate faulty hardware or software [Figure 1, Figures 2, and 3, Page 3] [DLP-509]

[2] Did more than one B ENTRY occur

Yes

[3] Locate AC1PCR reg in last PCRV printout and determine STATUS of bits 8, 9, 10 and 11 [Figure 1]

No

[4] Perform B-LEVEL interrupt analysis [TAP-149]

Page 2

PCRV: FAILED

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(L)	AC1FRS	AC1GRS	AC1JRS
AC1KRS	AC1LRS	AC1XRS	AC1YRS	AC1ZRS	AC1SR
AC1SC	PC1HISTORY	PC1OVER-RIDE(H)	PC1OVER-RIDE(L)	PC1FILL_ADD	AC1PCR

PCRV: BENTRY

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASB(H)	AC1ASB(L)
AC1SCA	AC1SDA	AC1CSC	AC1ILA	AC1PCR	AC1SR
AC1MCO	AC1MCP	AC1MCD(H)	AC1MCD(L)	AC1INH	AC1INS

PCRV: FAIL

AC1JR	AC1GR	AC1SR	PC1HISTORY	PC1OVERRIDE(H)	PC1OVERRIDE(L)
PC1FILL_ADDR					

PCRV: B REQ

AC1JR	AC1GR	AC1SCA	AC1CSC	AC1PCR	AC1SR
-------	-------	--------	--------	--------	-------

Figure 1 - B-ENTRY/B-FAILED Printout Register Locations

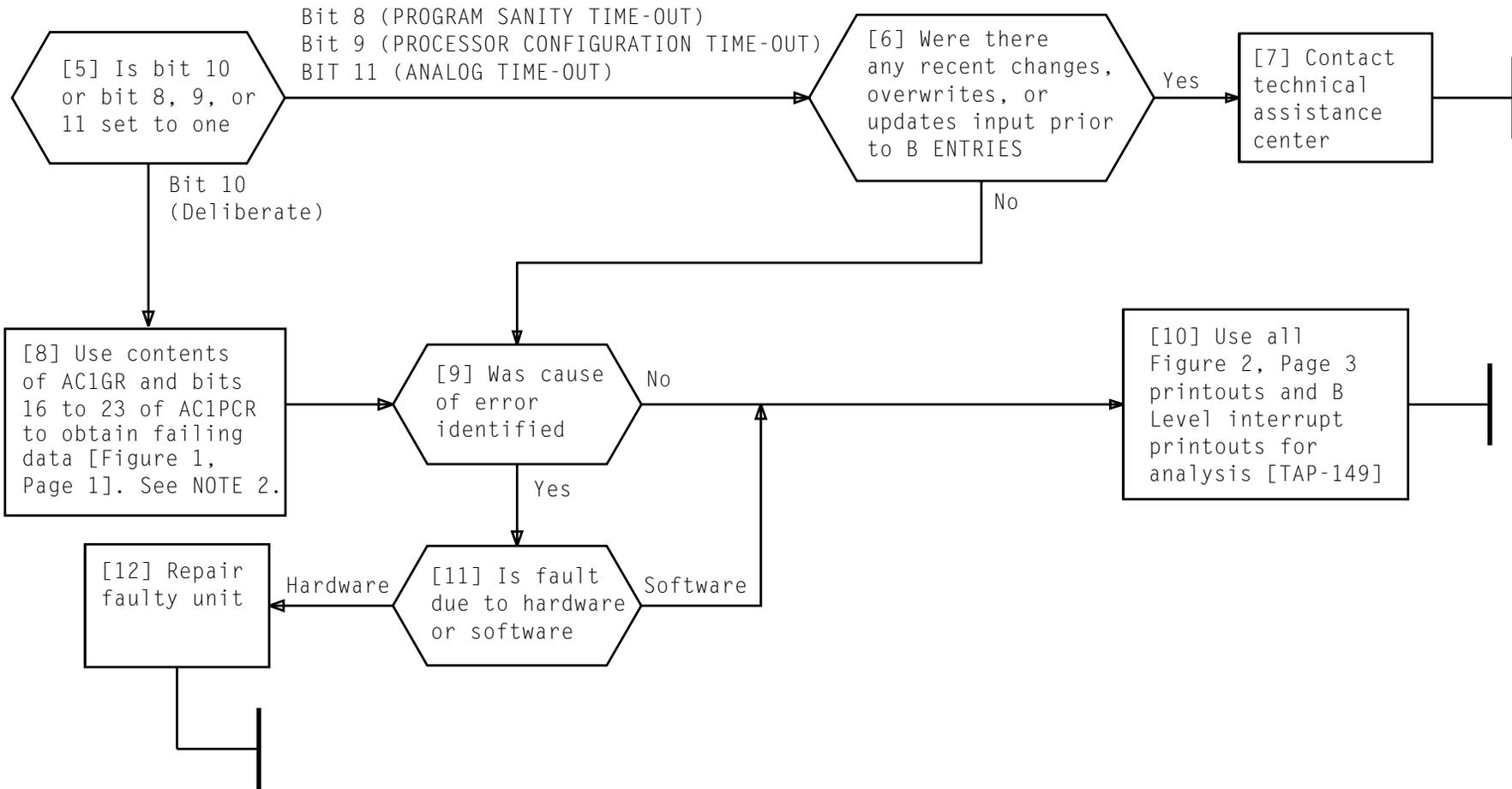
NOTE 1

Look at all three registers. If fault recovery code, use JR; otherwise, use SR. SCA is always valid but not as valuable.

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NOTE 2	
Bits 16-23 of AC1PCR contain the upper byte of failing data, and AC1GR contains the lower 24 bits of failing data	
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```

*C PCRV: FAILED
00024307 00000003 00022003 14037577 00022303 00000077
00000030 00000002 77777631 14032332 00000000 14051755
50000001 00000000 77602000 07403010 33300331 14550642
00000000 02000000 00000000 00000000 00000000 00022307

```

```

*C PCRV: BENTRY
77777777 14226047 50000000 50000000 00000377 77602000
00000377 77777777 00000000 14345240 00000277 77713713
42000043 32004400 00011575 00004002 00022310 00000000
14550642 04025251 60142000 00240400 46477777 40040100

```

Figure 2 - B-Entry/B-Failed Printout (Long)

```

*C PCRV: FAIL
14045743 14000000 14047672 06024300 00000000 14200000
*C PCRV: B REQ
10000000 10000000 77700040 00015455 00024311 14550642

```

Figure 3 - B-Entry/B-Failed Printout (Short)

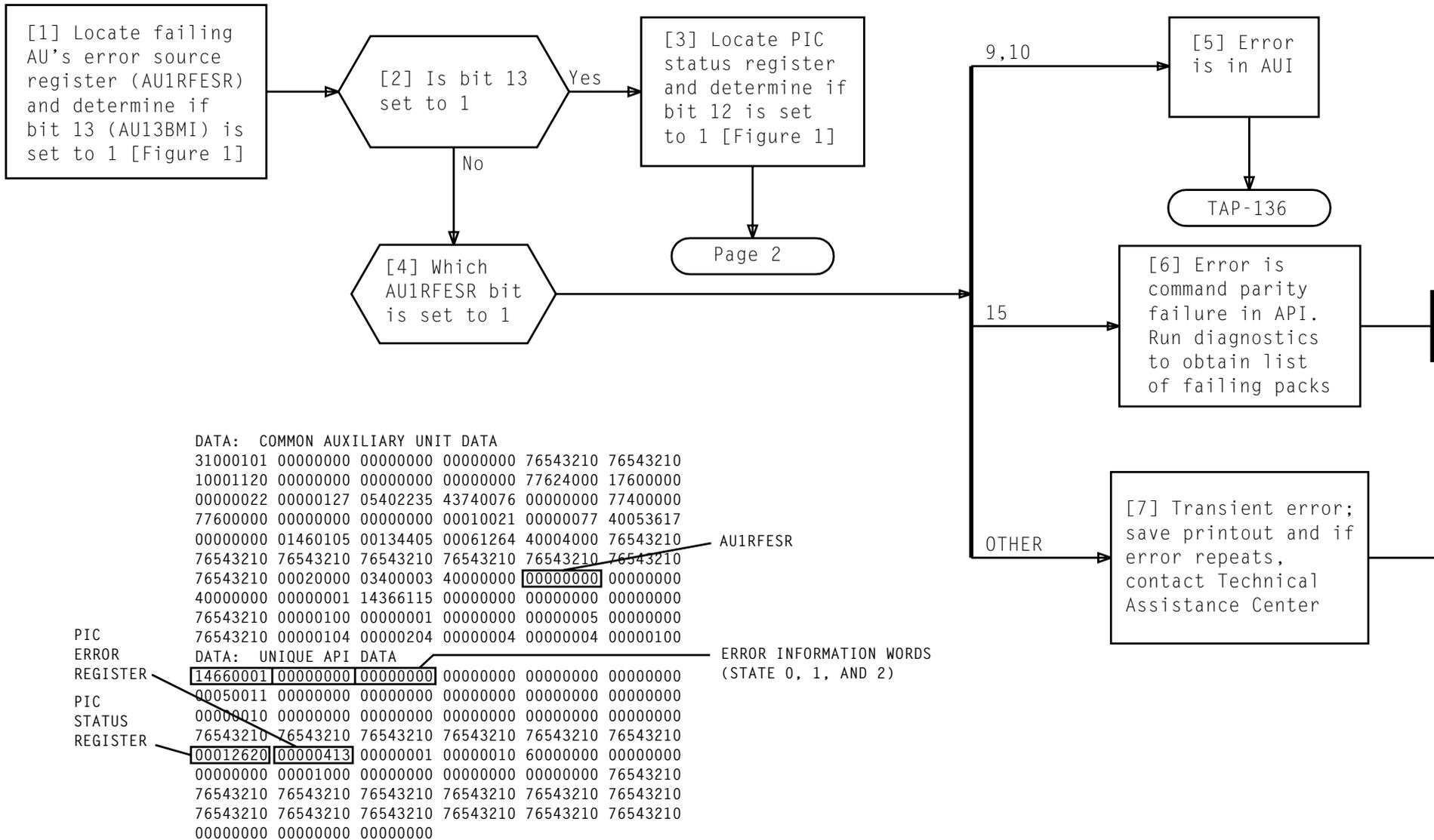


Figure 1 - Part of Interject Printout

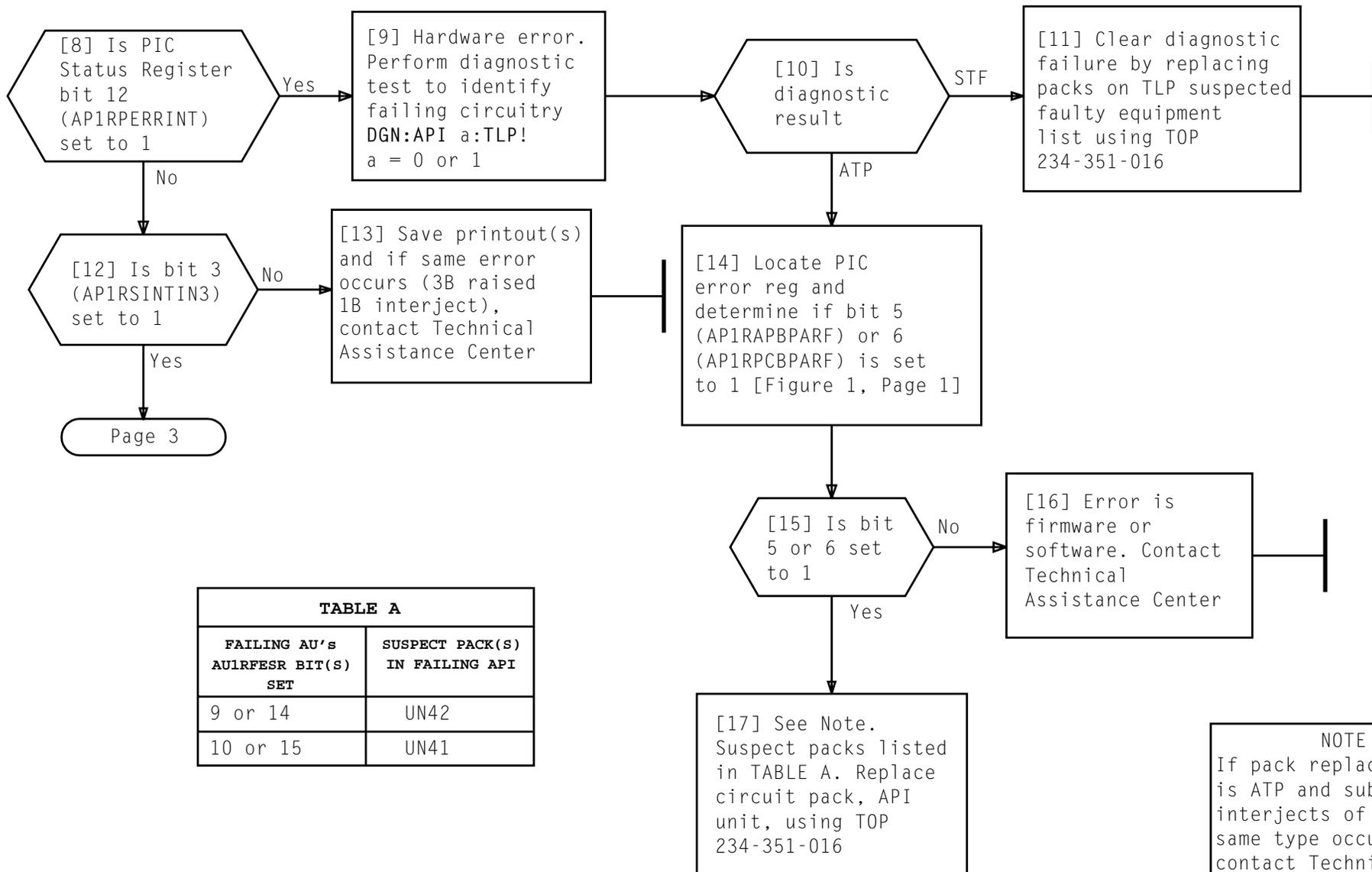
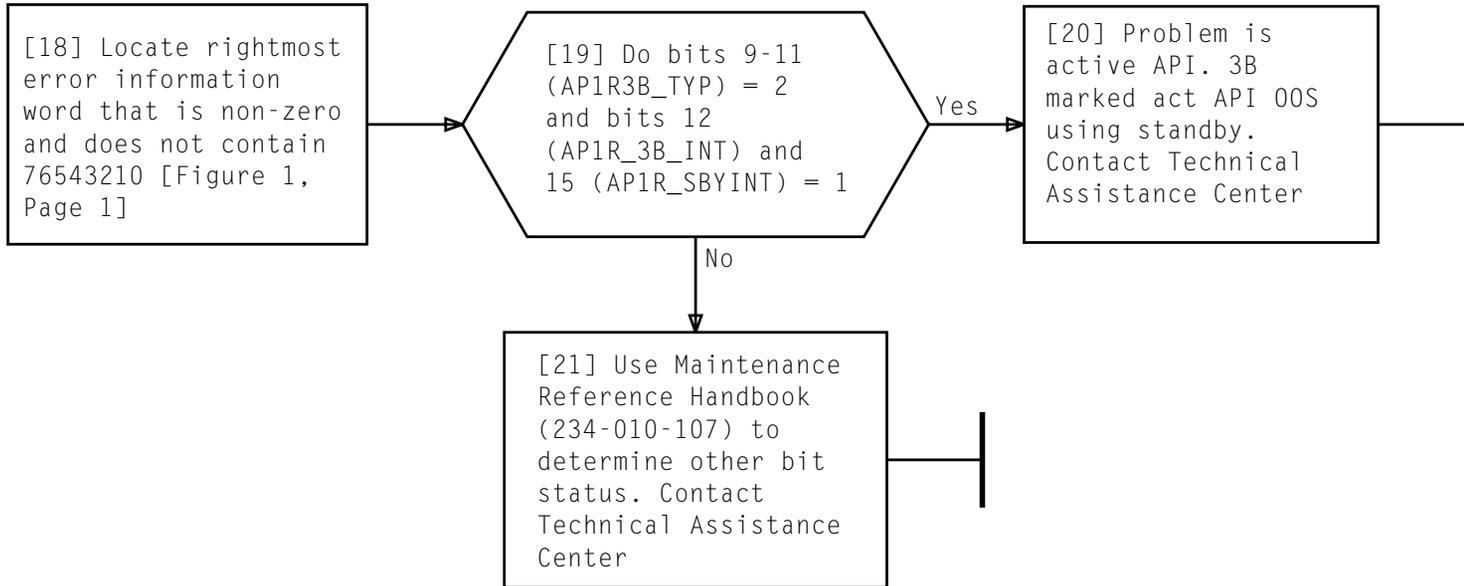
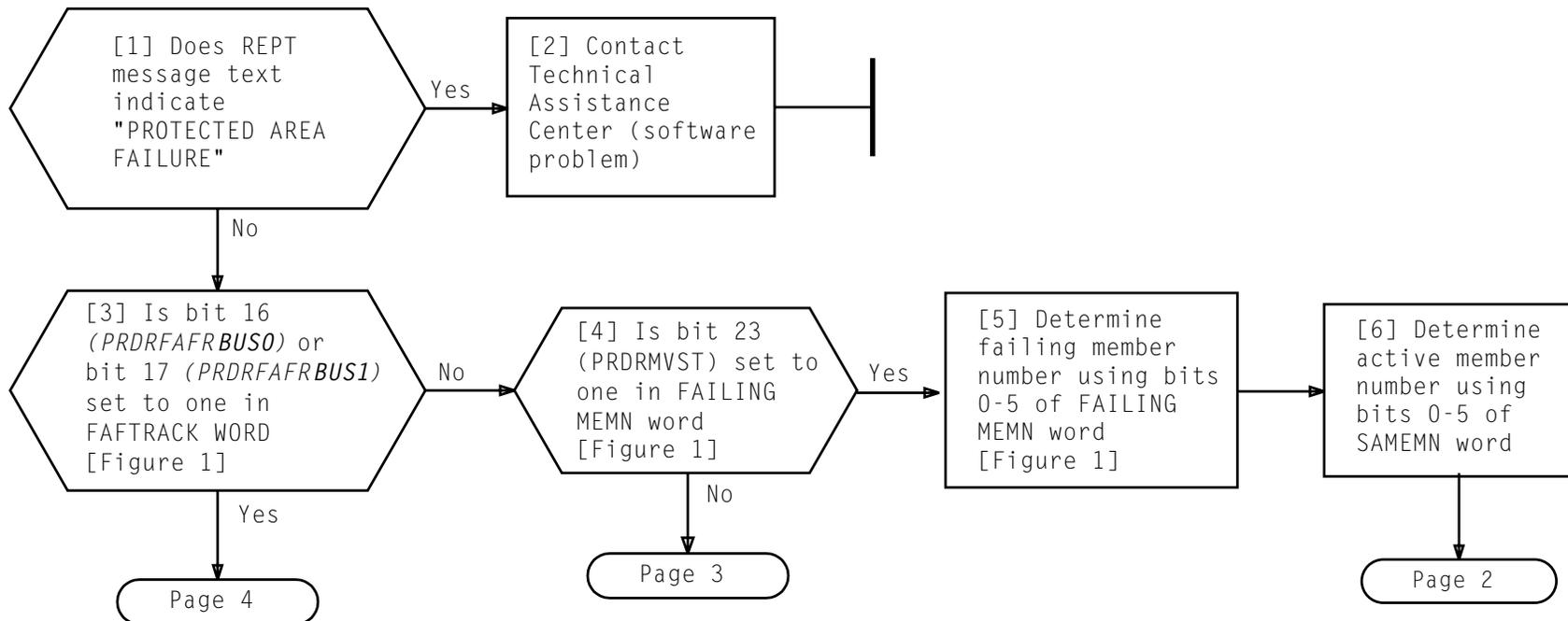


TABLE A	
FAILING AU's AU1RFESR BIT(S) SET	SUSPECT PACK(S) IN FAILING API
9 or 14	UN42
10 or 15	UN41

NOTE
If pack replacement is ATP and subsequent interjects of the same type occur, contact Technical Assistance Center should be contacted

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DATA: CALL STORE IDENTIFICATION DATA (CSFRID)

FAILING_H_ADDR	FAILING_ADDR	RCES	ST1BRS_H	ST1BRS_L	AC1SAL
AC1SAR	ST1SAL	ST1SAR	SCES	FAILING_MEMN	VBOOT
BFAILRT	SYSSTAT	IBUSSTAT	SAMEMN	MNSUSP	BUSBUFFGCPS (CS ONLY) (0 FOR PS)
GCPACT_L	GCPACT_H	CR01ACT	CR10ACT	RESERVE	FLAGS1
GCPSTBY_L	GCPSTBY_H	CR01STBY	CR10STBY	RESERVE	FAFTRACK
CINS	C_ACT_EVEN	C_ACT_ODD	C_STBY_EVEN	C_STBY_ODD	REP_STORE
BUSSTATER	C_H_ACT_EVEN	C_H_ACT_ODD	C_H_STBY_EVEN	C_H_STBY_ODD	ST1ABC
FAILING_MCODE	RESERVE				

Figure 1 - PART OF REPT MESSAGE

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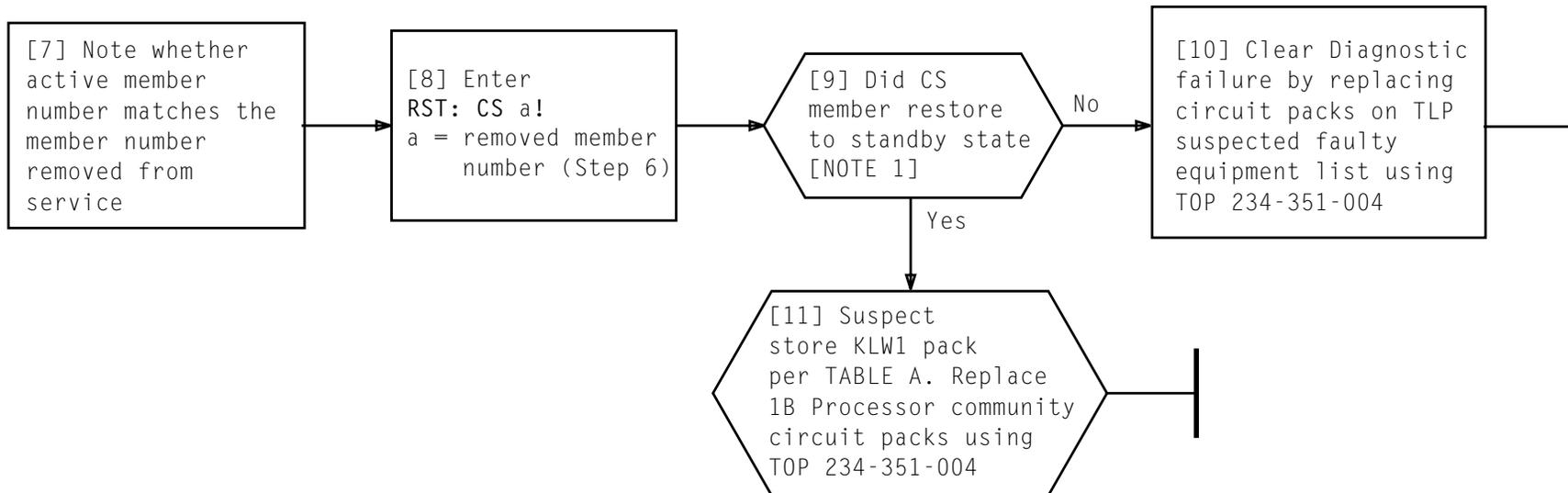
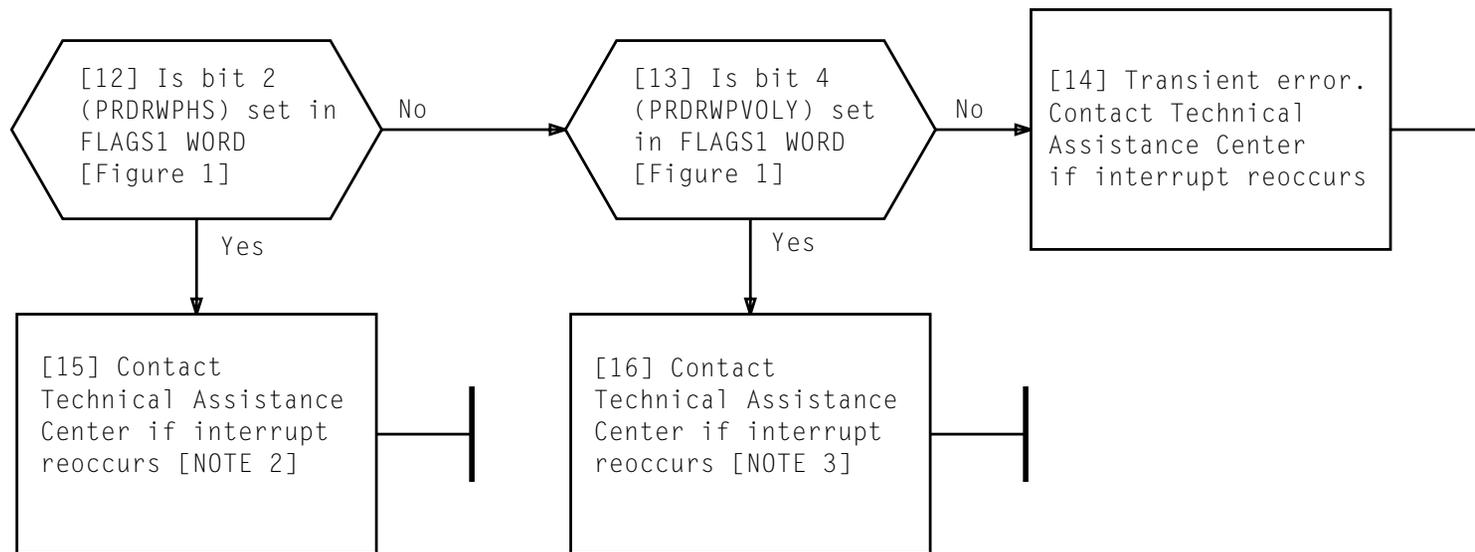


TABLE A							
STORE	LOCATION	STORE	LOCATION	STORE	LOCATION	STORE	LOCATION
0	0-24-006	10	0-24-160	20	0-24-046	30	0-24-120
1	1-24-006	11	0-24-160	21	1-24-046	31	1-24-120
2	0-24-176	12	0-24-030	22	0-24-136	32	0-24-070
3	1-24-176	13	1-24-030	23	1-24-136	33	1-24-070
4	0-24-014	14	0-24-152	24	0-24-054	34	0-24-112
5	1-24-014	15	1-24-152	25	1-24-054	35	1-24-112
6	0-24-168	16	0-24-038	26	0-24-128	36	0-24-078
7	1-24-168	17	1-24-038	27	1-24-128	37	1-24-078
8	0-24-022	18	0-24-144	28	0-24-062	38	0-24-104
9	1-24-022	19	1-24-144	29	1-24-062	39	1-24-104

NOTE 1	
If member number restores and interrupts reoccur, contact Technical Assistance Center	
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NOTES	
2. Software and hardware are inconsistent. Hardware indicated a write protect error while the software indicated the address involved with the violation was not write protected.	
3. A write protect error has been encountered for store member in bits 0-5 of FAILING MEMN word	
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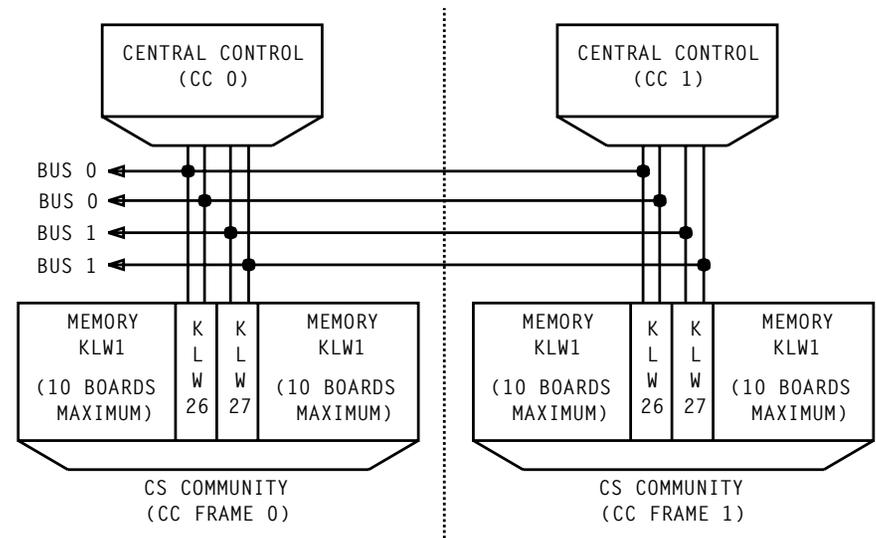
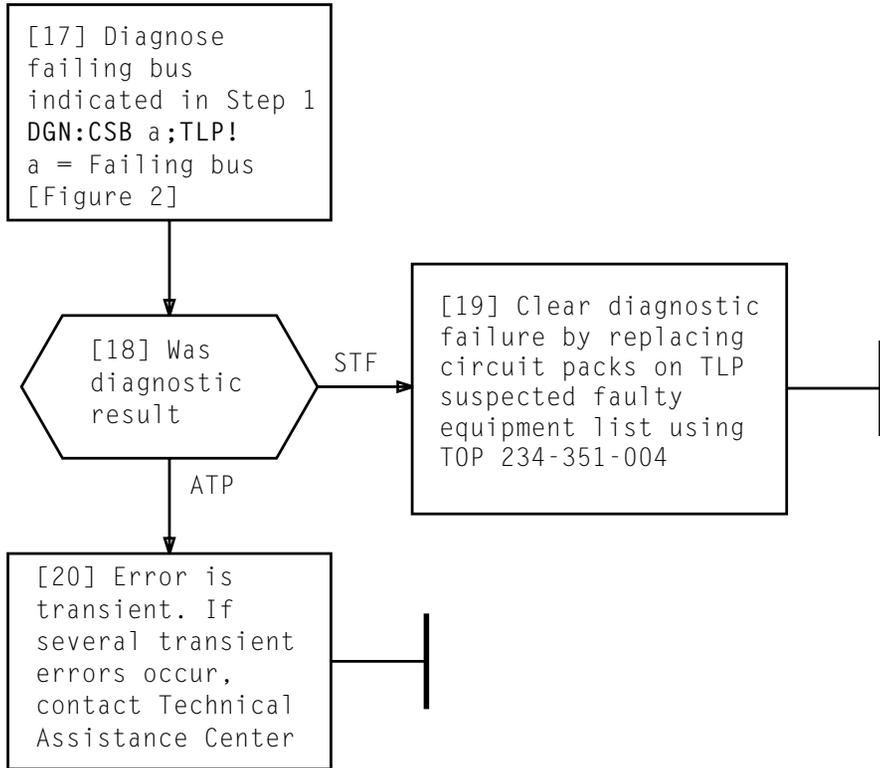
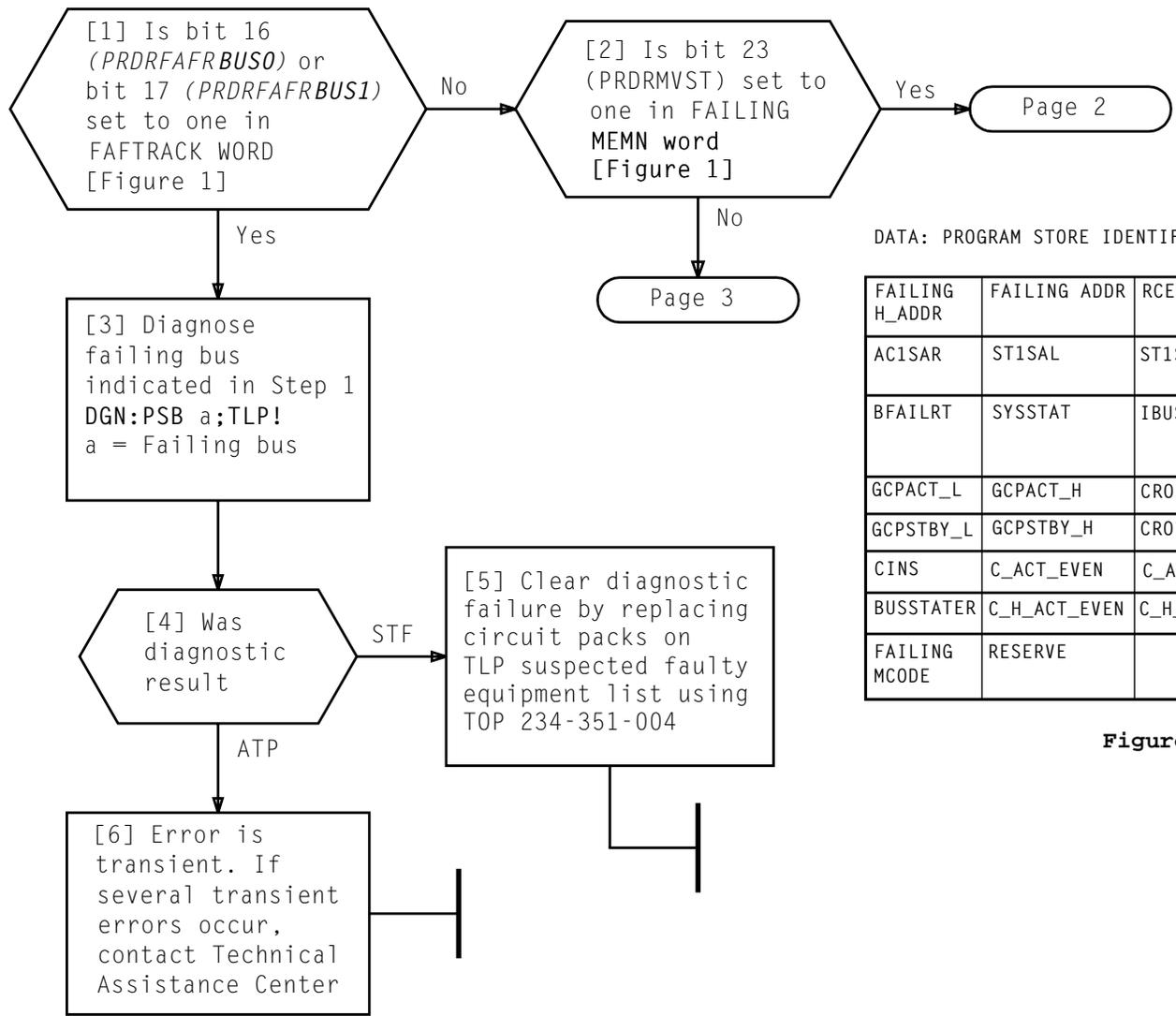


Figure 2 - KLW26/KLW27 - CALL STORE BUFFER BOARDS



DATA: PROGRAM STORE IDENTIFICATION DATA (PSFRID)

FAILING H_ADDR	FAILING ADDR	RCES	ST1BRS_H	ST1BRS_L	ACISAL
AC1SAR	ST1SAL	ST1SAR	SCES	FAILING MEMN	VBOOT
BFILRT	SYSSTAT	IBUSSTAT	SAMEMN	MNSUSP	BUSBUFFGCP (CS ONLY) (0 FOR PS)
GCPACT_L	GCPACT_H	CR01ACT	CR10ACT	RESERVE	FLAGS1
GCPSTBY_L	GCPSTBY_H	CR01STBY	CR10STBY	RESERVE	FAFTRACK
CINS	C_ACT_EVEN	C_ACT_ODD	C_STBY_EVEN	C_STBY_ODD	REP_STORE
BUSSTATER	C_H_ACT_EVEN	C_H_ACT_ODD	C_H_STBY_EVEN	C_H_STBY_ODD	ST1ABC
FAILING MCODE	RESERVE				

Figure 1 - PART OF REPT MESSAGE

[7] Determine failing member number using bits 0-5 of FAILING MEMN word
[Figure 1, Page 1]

[8] Determine active member number using bits 0-5 of SAMEMN word

[9] Note whether active member number matches the member number removed from service

[10] Enter
RST: PS a;TLP!
a = removed member number (Step 6)

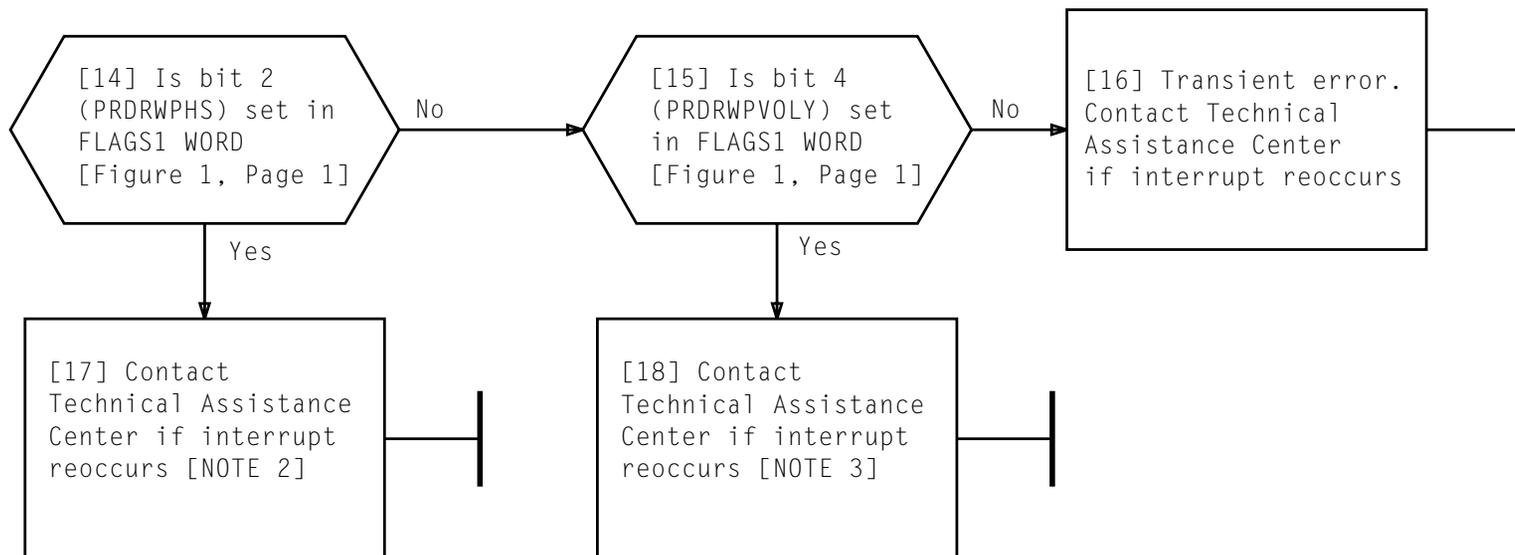
[11] Did PS member restore to standby state
[NOTE 1]

[13] Clear diagnostic failure by replacing circuit packs on TLP suspected faulty equipment list using TOP 234-351-004

[12] Suspect store KIW2 pack per TABLE A. Replace 1B Processor community circuit packs using TOP 234-351-004

TABLE A	
STORE	LOCATION
0	0-41-128
1	1-41-128
2	0-41-136
3	1-41-136
4	0-41-144
5	1-41-144

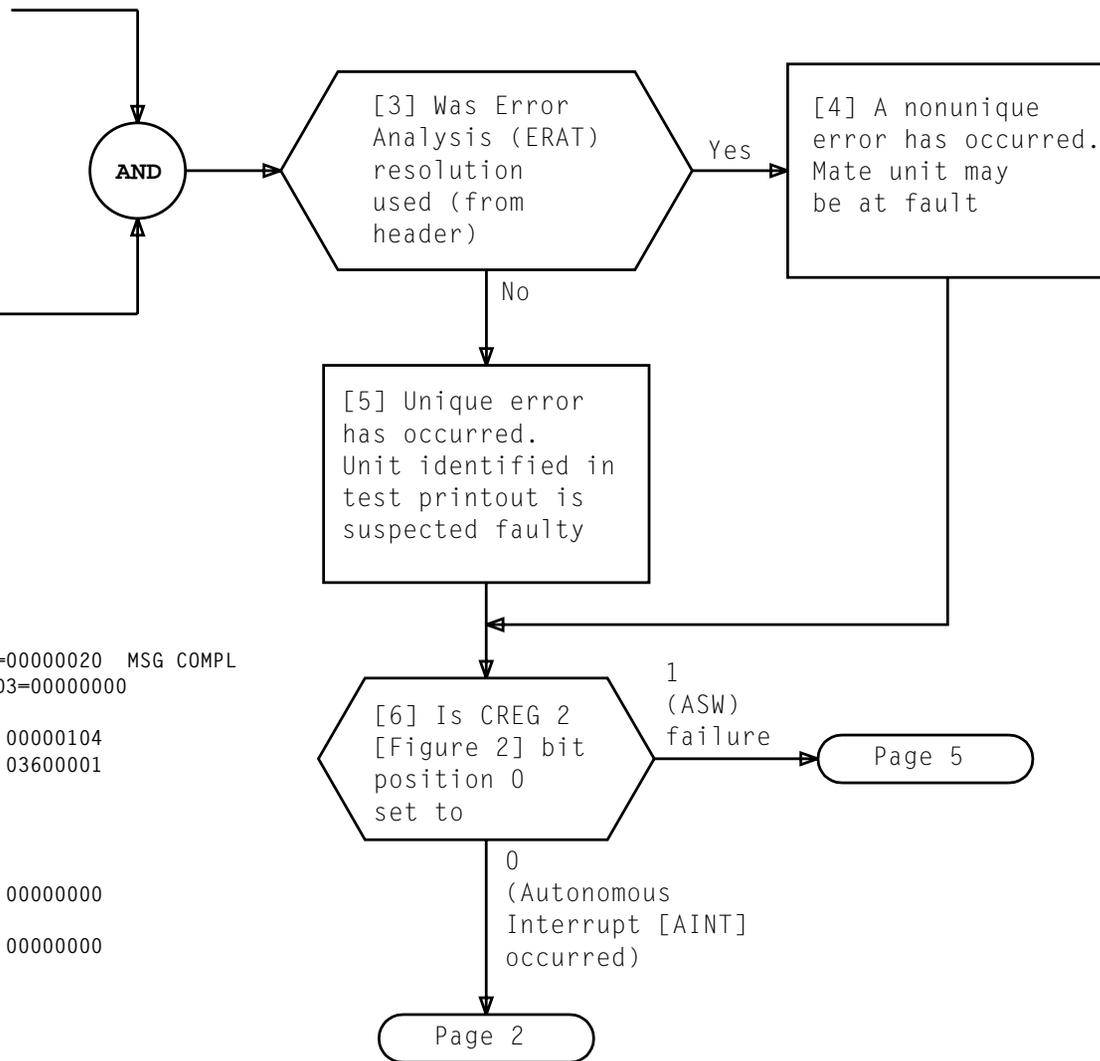
NOTE 1	
If member number restores and interrupts reoccur contact Technical Assistance Center	
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NOTES	
2. Software and hardware are inconsistent. Hardware indicated a write protect error while the software indicated the address involved with the violation was not write protected.	
3. A write protect error has been encountered for store member in bits 0-5 of FAILING MEMN word	
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[1] Using Figure 1, obtain Point of Maximized Definition (PMD) from **FAULT RECOGNITION ISOLATION DATA** word 2 (rightmost three octal digits)

[2] Access PMD dictionary to obtain description of software actions and analysis of this error [DLP-510]



```

A 39 REPT: F-LEVEL 014764301 MFNUM=00004303 MICON=00000020 MSG COMPL
LV=0040 D0=00000000 D1=04000000 D2=00000017 D3=00000000
DATA: PERIPHERAL SYSTEM DATA
03020102 00000000 00000001 00000000 00000000 00000104
00000112 00000004 00000012 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00002400 14130667 03552000 00000020 00002000
DATA: FAULT RECOGNITION ISOLATION DATA
00000020 00002000 00000237 00000000 00000003 00000000
DATA: ERROR ANALYSIS STRATEGY DATA
01664210 00000001 00000001 00000001 00000001 00000000
00000001
04/29/83 11:38:49
#822
  
```

Figure 1 - Part of TNFR Printout

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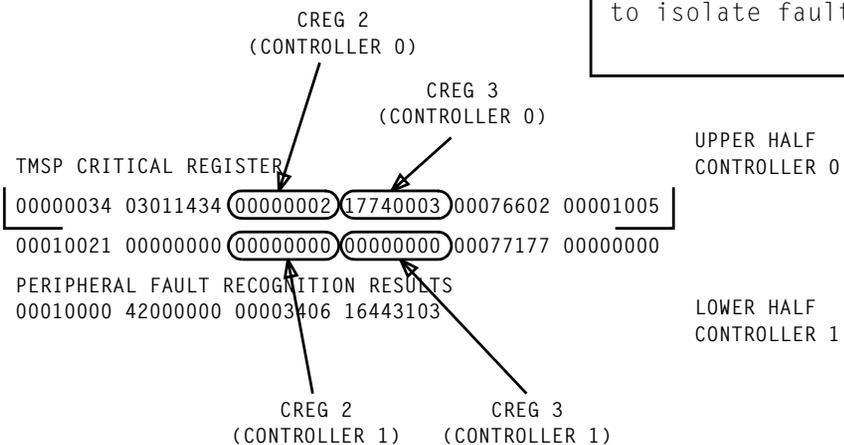
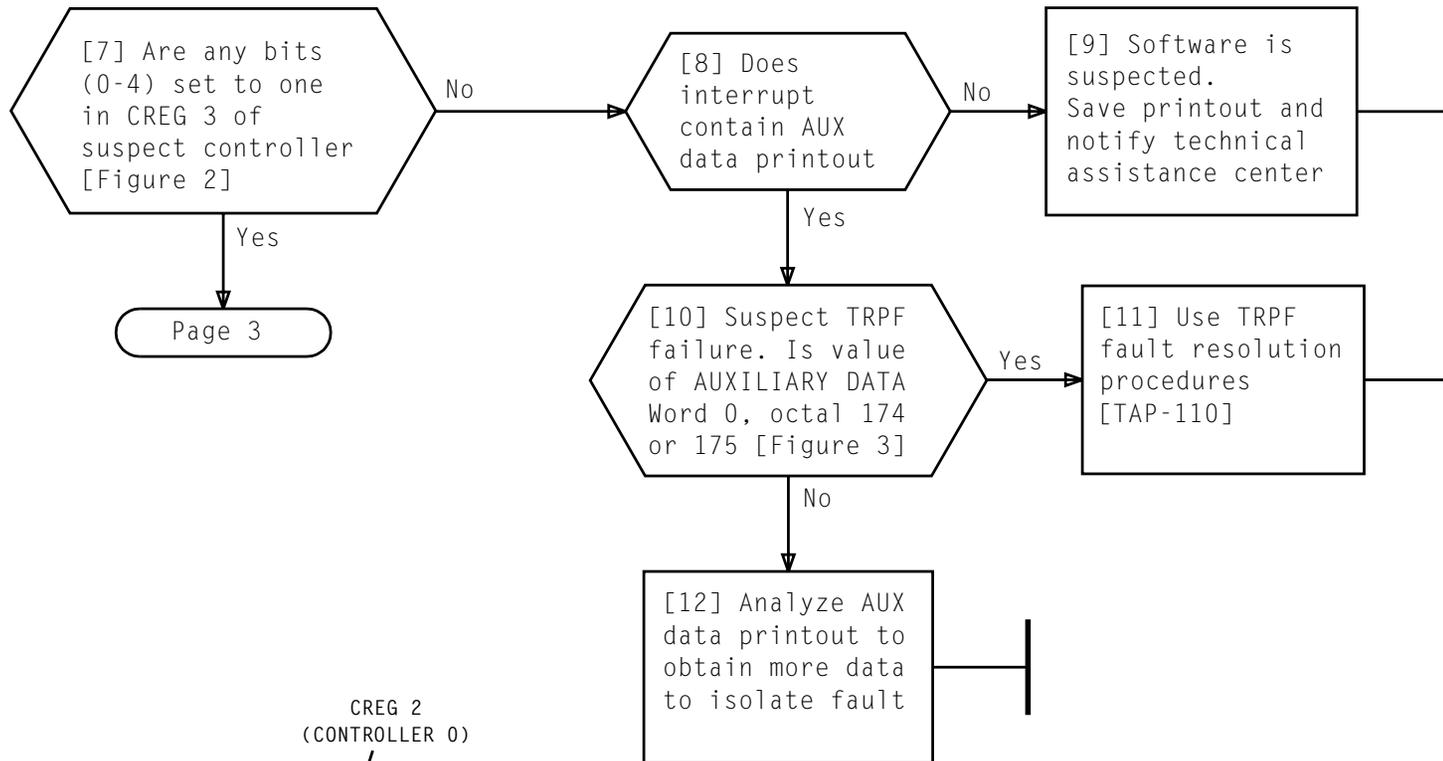


Figure 2 - TMS Critical Registers

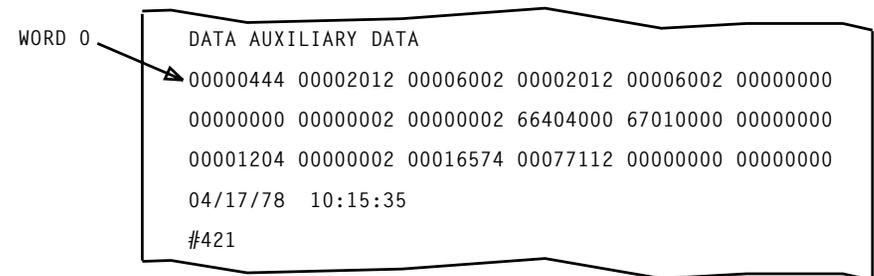


Figure 3 - Auxiliary Data Registers

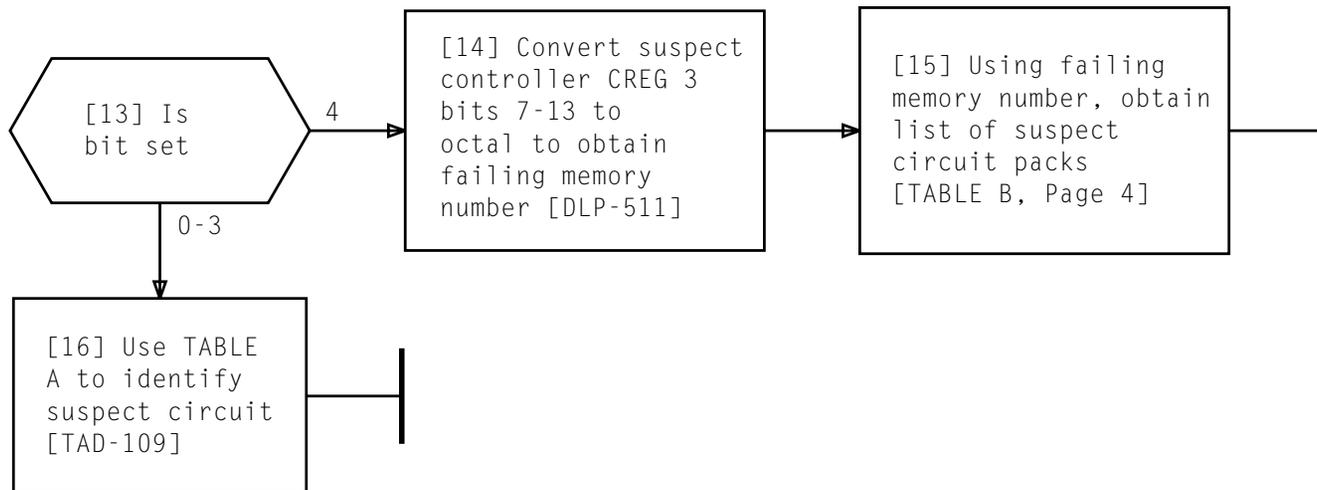


TABLE A TMS-AINT, BITS 0-3							
Significance of bit and reference to SD-4A026 for TMS-A and SD-4A088 for TMS-B appear below. Determine next step for error source bits set							
ESR1 BIT	NAME	LEAD	FS/SYMBOL	IMPLICATION	SUSPECT PACKS	TMS-A	TMS-B
0	CE	ECE0	15/1	Internal clock error. Suspect clock circuit	FA527 FB225	072-21 072-22	(0,1)68-37
1	TSSC	ETSSC0	13/1	Time slot sequence. Check suspect time slot counter circuit	FA532	072-23	(0,1)68-39
2	TSCMM	ETSMM0	14/1	Time slot counter mismatch. Suspect 1) time slot counter 2) match circuit 3) mate controller	FA532 FA527 MATE CONTR	072-23 072-21 -	(0,1)68-39 (0,1)68-37 -
3	CMM	DESB030	15/1	Clock mismatch. Suspect 1) clock match circuit 2) mate controller	FA527 MATE CONTR	072-23	(0,1)68-37

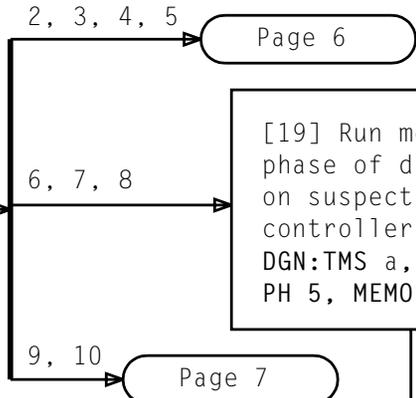
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TABLE B - TMS MEMORY NUMBERS			
HORIZONTAL PACK LOCATION			
FAILING MEMORY NUMBER	TMS-A FA632 MEMORY PACK	TMS-A FA520 MEMORY REGISTER PACK	TMS-B FA1199 MEMORY PACK
0, 20, 40, 60, 100, 120, 140, 160,	-05	-09	-25
1, 21, 41, 61, 101, 121, 141, 161	-06		
2, 22, 42, 62, 102, 122, 142, 162	-07	-10	-27
3, 23, 43, 63, 103, 123, 143, 163	-08		
4, 24, 44, 64, 104, 124, 144, 164	-21		
5, 25, 45, 65, 105, 125, 145, 165	-20	-17	-28
6, 26, 46, 66, 106, 126, 146, 166	-19	-16	-30
7, 27, 47, 67, 107, 127, 147, 167	-18		
10, 30, 50, 70, 110, 130, 150, 170	-24	-28	-46
11, 31, 51, 71, 111, 131, 151, 171	-25		
12, 32, 52, 72, 112, 132, 152, 172	-26	-29	-44
13, 33, 53, 73, 113, 133, 153, 173	-27		
14, 34, 54, 74, 114, 134, 154, 174	-40	-36	-43
15, 35, 55, 75, 115, 135, 155, 175	-39		
16, 36, 56, 76, 116, 136, 156, 176	-38	-35	-41
17, 37, 57, 77, 117, 137, 157, 177	-37		
VERTICAL PACK LOCATION			
0 Through 17	Bay 0, Vertical 36		*24
20 Through 37	Bay 0, Vertical 44		*28
40 Through 57	Bay 0, Vertical 52		*36
60 Through 77	Bay 0, Vertical 60		*40
100 Through 117	Bay 1, Vertical 36		*48
120 Through 137	Bay 1, Vertical 44		*52
140 Through 157	Bay 1, Vertical 52		*60
160 Through 177	Bay 1, Vertical 60		*64
* = Controller 0 or 1			

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[17] Use TABLE C and CREG 2 [Figure 2, Page 2] bits (2-11) set to one to identify suspect circuits

[18] Is CREG 2 bit set to one



[19] Run memory phase of diagnostic on suspect controller
DGN:TMS a, CONTR b:
PH 5, MEMORY,TLP!

[20] Was phase 5 ATP/CATP

[21] Clear diagnostic failure by replacing circuit packs on TLP suspected faulty equipment list using TOP 234-151-011

[22] Check for any recent TMS audits that have been called or indications of software errors

TABLE C ASW ERROR				
ESR1 BIT	NAME	LEAD	FS/SYMBOL	IMPLICATION
0	ASRF	EASRMO	16/11	All seems well failure summary
1	AINT	—	—	Autonomous interrupt failure summary
2	PFE	EPFE0	3/3	Bus parity failure – even bits
3	PFO	EPFB0	3/1	Bus parity failure – odd bits
4	MODE	EMBO0	16/10	Mode failure
5	SEQCK	ESEQCK0	16/11	Suspect output decoder problem in controller
6	MAF	EMAF0	16/9	Suspect a memory problem
7	TSPF	EMPFBO	12/5	Suspect a memory problem
8	AUDIT	EAU00	16/6	Suspect software or a memory problem
9	TSAMM	ETSMM0	14/1	Mismatch error
10	MTMM	EMSH0	10/1	Mismatch error
11	ABORT	EABORT0	16/11	

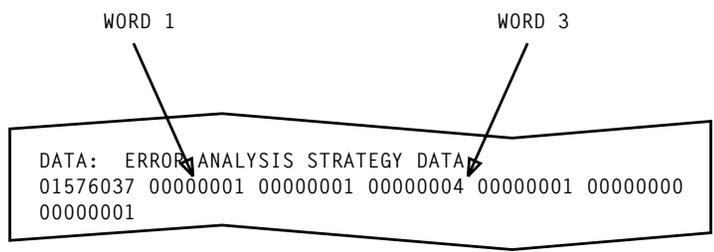
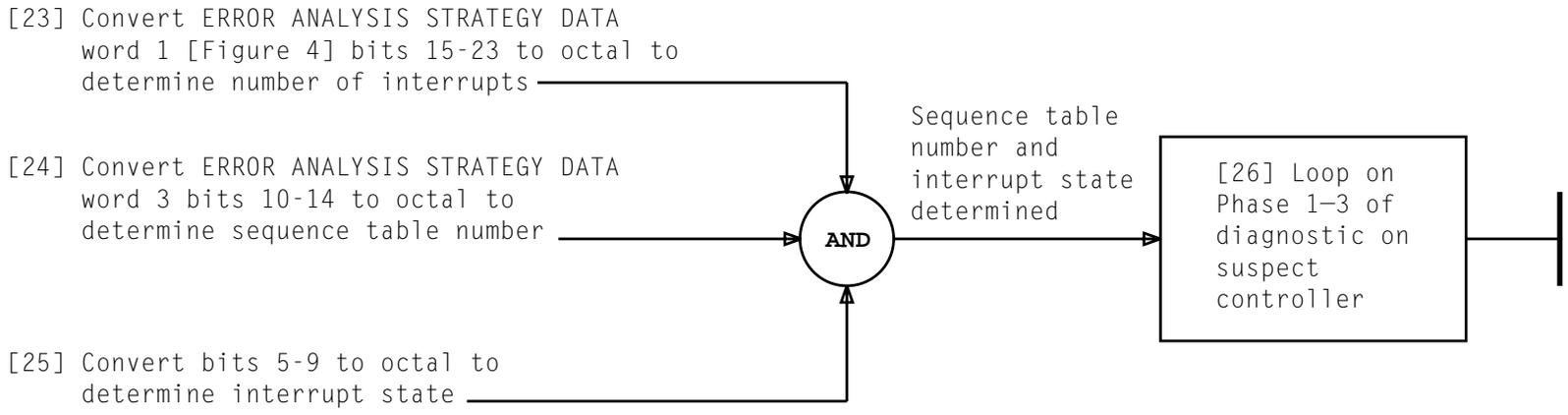
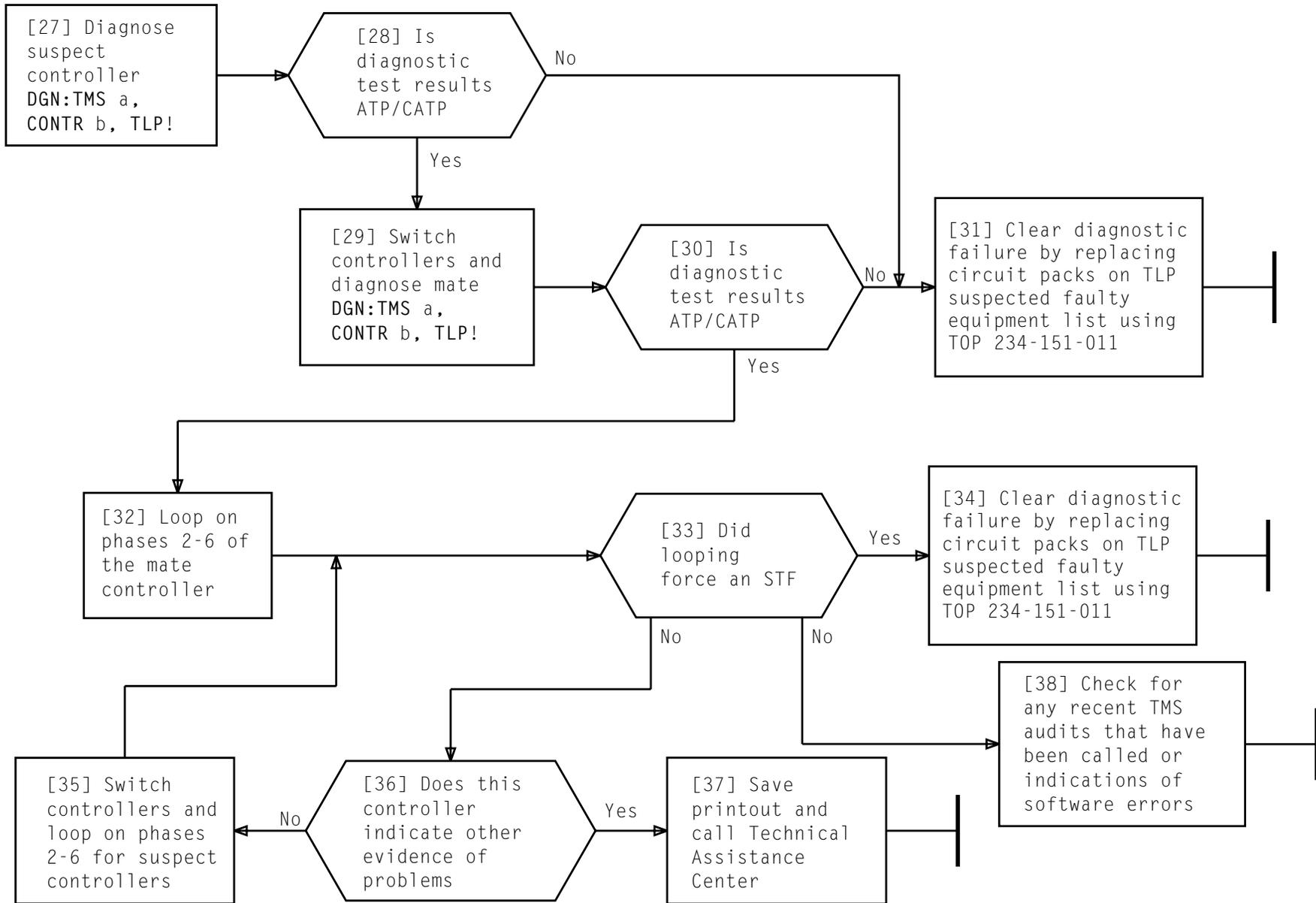
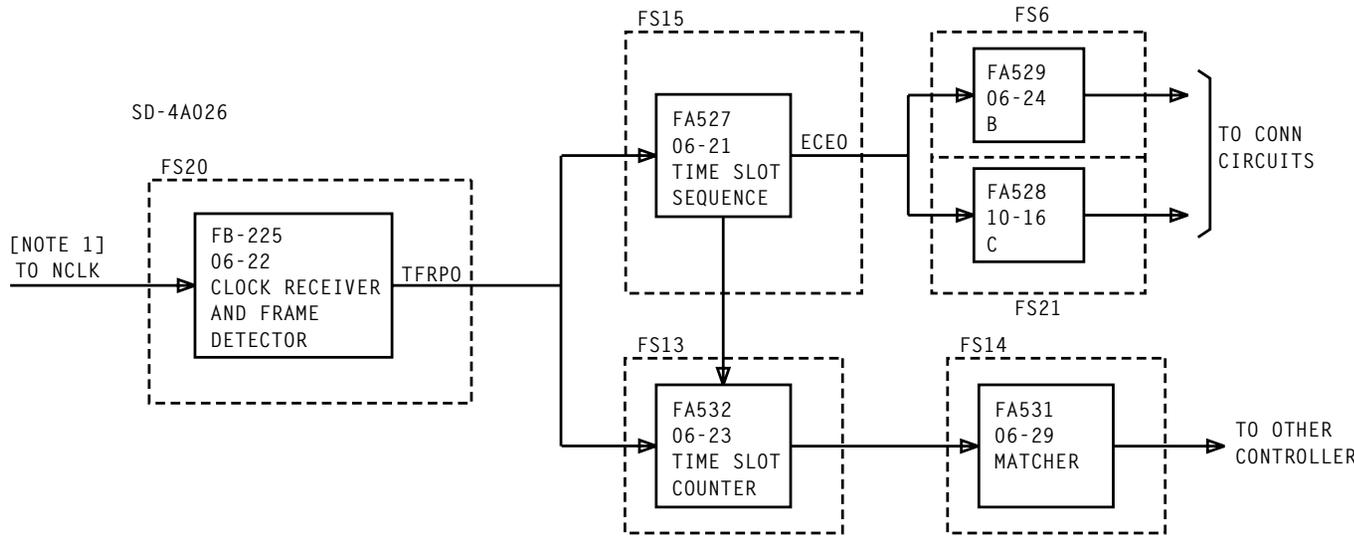


Figure 4 - Error Analysis Strategy Data



A simplified block diagram for AINT bits 0-3 in CREG 3 register is provided as an aid for trouble isolation of clock problems in the TMS frame



NOTE 1	
Verify NCLK frame is providing good clock before checking packs	
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AUTONOMOUS INTERRUPT (AINT) CLOCK BITS 0-3, TIME-MULTIPLEXED SWITCHING

At TCC terminal:

[1] Type F: a;PAT b, (FROM c, TO d,) RDT e!

- a = office code
- b = desired interrupt pattern
- c = month, day, and time filter is to begin
- d = month, day, and time filter is to end
- e = file name interrupt data is to be directed to

[2] Type

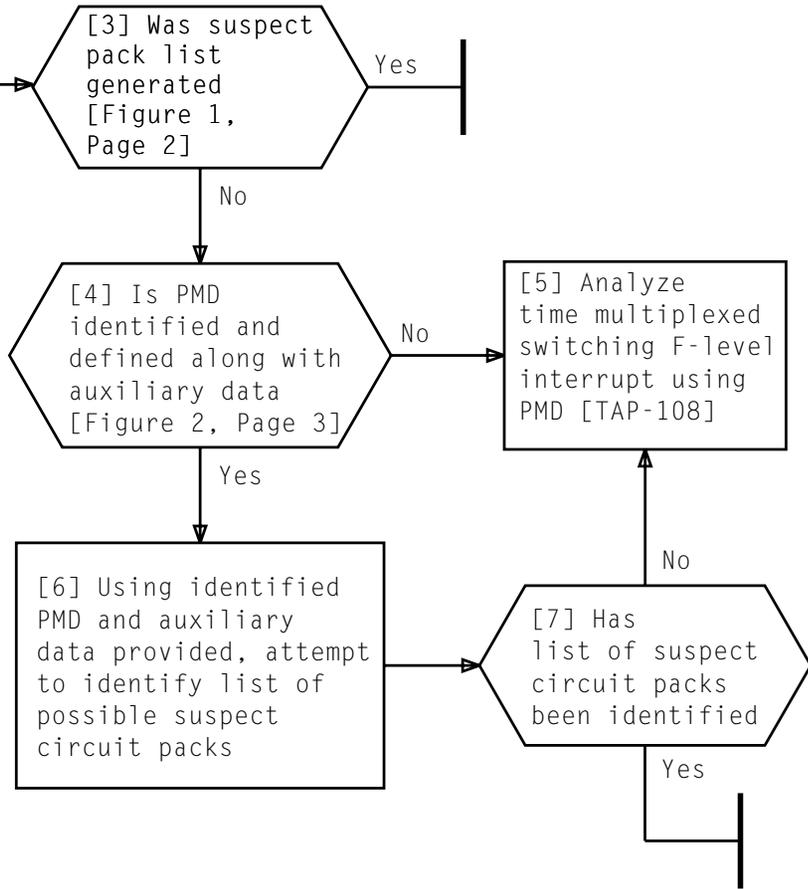
ANAL:TRPF;CHANNEL a;RDT b!

- a = office code
- b = file name interrupt data was directed to

System responds
xx MESSAGES
MATCHED
OUT OF yy

System
responds with
interrupt
message
analysis

AND



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```

-----
: PATH TRACE :
-----
: TTSI :TMS ST2 ST1 : RTS1 : : :
-----
: F C S L P C : F C S A B : S A B : F C S D P C :
: R T P O O H : R T W L L : W L L : R T P S O H :
: A R C D R A : A R T E E : T E E : A R C R R A :
: M L T N : M L V V : V V : M L T N :
-----
: 00-1 2 7 0 017 : 0-0 02 00 14 : 14 00 02 : 02-0 2 0 4 018 :
-----
: CIRCUIT PACKS IN THE PATH :
-----
: TTSI : TMS ST2 : TMS ST1 :RTSI :
-----
: FA1781 052-04 : FA533 028-23 : FA522 064-33 : FA1780 052-58 :
: FA1784 052-07 : FA521 028-31 : FA523 064-34* : FA545 052-47 :
: FA1785 052-14 : FA521 028-32* : FA524 064-21 : FA533B 076-07 :
: FA1808 076-10 : : :
-----
(* OPTIONAL)

```

SUSPECT
CIRCUIT
PACKS →

Figure 1 - Sample Interrupt Message Analysis (Partial)

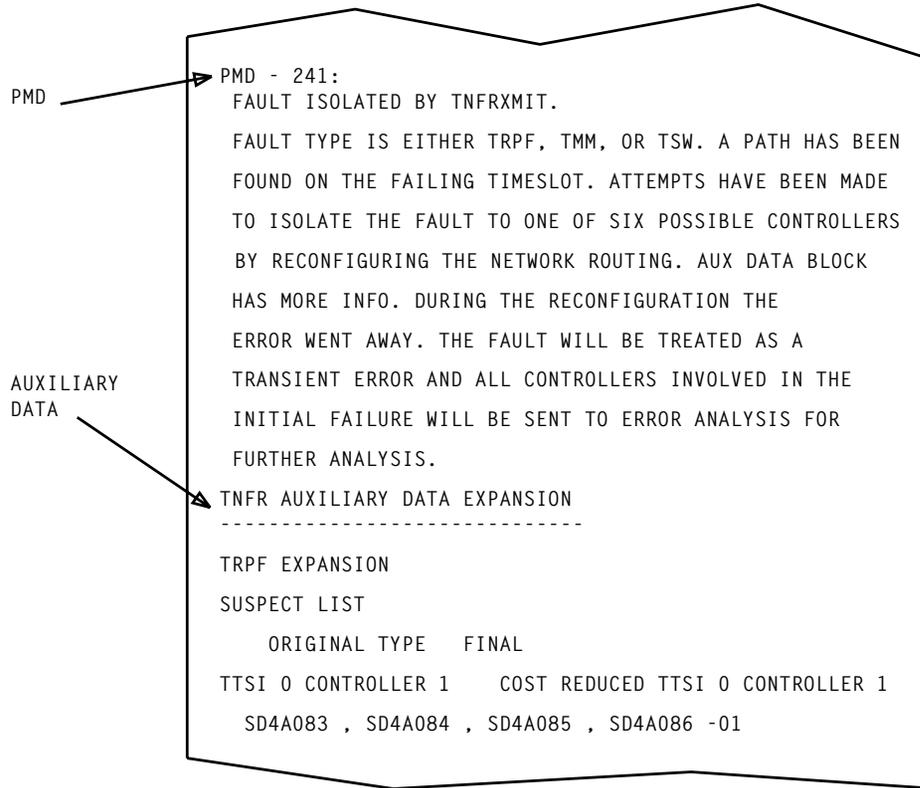
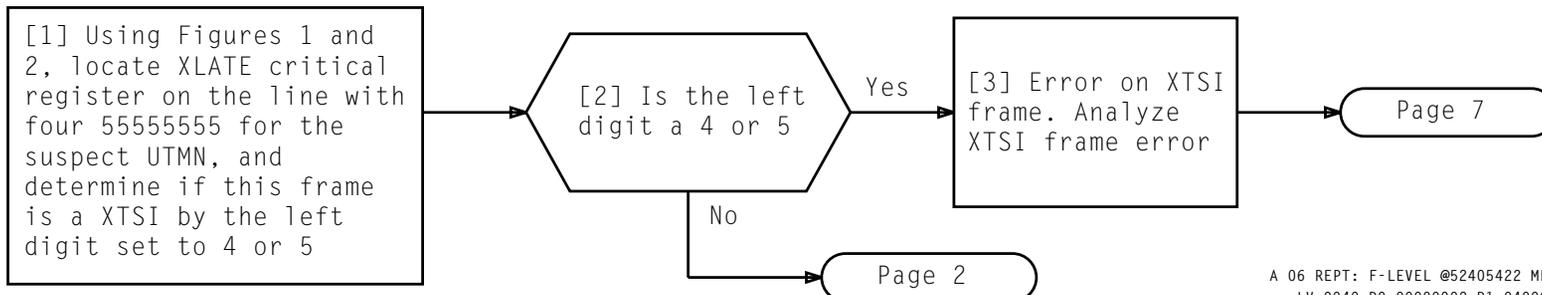


Figure 2 - Sample Interrupt Message Analysis (Partial)



```

A 41 REPT: F-LEVEL @54175146 MFNUM=00000044 MICON=00000020 MSG IP
LV=0040 D0=00000000 D1=04000000 D2=00000037 D3=00000200
DATA: TSI CRITICAL REGISTERS
00000034 42000034 00000002 63400200 00000200 00000060
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00001000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000200 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000171 00000000 00036200
00000016 20637777 55555555 55555555 55555555 55555555
20016020 42004423 00000002 77400200 00020000 00000360
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00074400 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00001000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00020000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000171 00000000 00036200
DATA: PERIPHERAL SYSTEM DATA
00141454 00000001 00000001 00000000 00000000 00000004
00000012 00000004 00000012 03600001 03600001 03400001
03600001
DATA: INTERRUPT SOURCE DATA
00000200 00000000 01330000 00000020 00040000
DATA: FAULT RECOGNITION ISOLATION DATA
00000031 00000003 00000250 00000000 00000003 00000000
DATA: ERROR ANALYSIS STRATEGY DATA
03025431 00000013 00000000 00000031 00000013 00000000
00000001
DATA: AUXILIARY DATA
00001044 00000034 20016020 02000034 02004423 00000000
20637777 00000002 00000002 63400200 77400200 00000000
00001237 00000001 00000000 00000000 00000000 00000000
10/27/98 18:39:52
#929
  
```

TSI XLATE
critical
register

Figure 1 - TSI (Cost Reduced, Vintage or Near Term) Critical Registers

```

A 06 REPT: F-LEVEL @52405422 MFNUM=00000010 MICON=40000020 MSG IP
LV=0040 D0=00000002 D1=04000000 D2=00000037 D3=00000200
DATA: TSI CRITICAL REGISTERS
00002212 00002212 0040213 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000
00000000 00003000 00000022 00000732 23246400 01331111
74177741 00000377 43344334 00004334 77776401 00000020
04000106 00000000 00000000 01000000 00000000 00005100
00020177 10034140 00000000 00000000 00000100 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
00000006 43777777 55555555 55555555 55555555 55555555
00000004 00006004 00040007 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000
00000000 00003000 00000022 00000732 23246400 01531452
74177741 00000377 43344334 00004334 77776401 00000020
04000106 00000000 00000000 01000000 00000000 00005503
00020177 14064140 00000000 00000000 00000000 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
DATA: PERIPHERAL SYSTEM DATA
00103466 00000003 00000000 00000000 00000000 00000012
00000004 00000012 00000004 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00001540 00001020 01010000 00000020 00000100
DATA: FAULT RECOGNITION ISOLATION DATA
00000034 00000000 00000142 00000000 00000005 00000000
01/01/70 14:06:51
#628
  
```

XTSI XLATE
critical
register

Figure 2 - XTSI Critical Registers

ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE

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[4] See NOTE 1. Using Figure 3, locate CREG 2 for suspect controller and determine if bit 0 is set to one [DLP-513]

[5] Is bit 0 set to one

Yes

No

[6] Are any bits 2-13 set to one in CREG 2

Yes

No

[7] See NOTE 2. Are any bits 5-13 set to one in CREG 2

Yes

No

Page 4

Page 3

[8] No error was detected by TSI unit. Analyze CC F LEVEL registers to determine CC, BUS, and unit configurations [TAP-112]

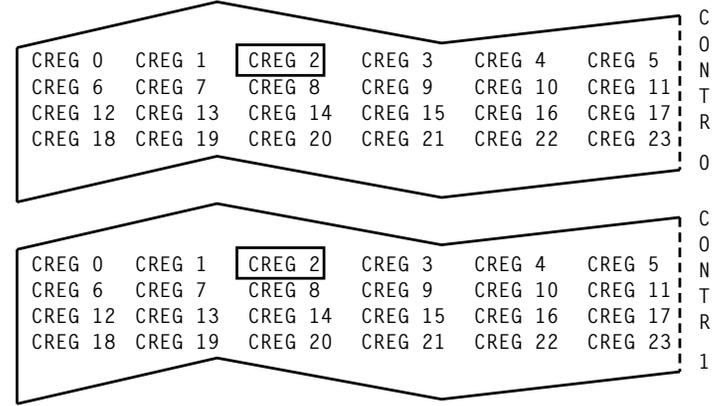


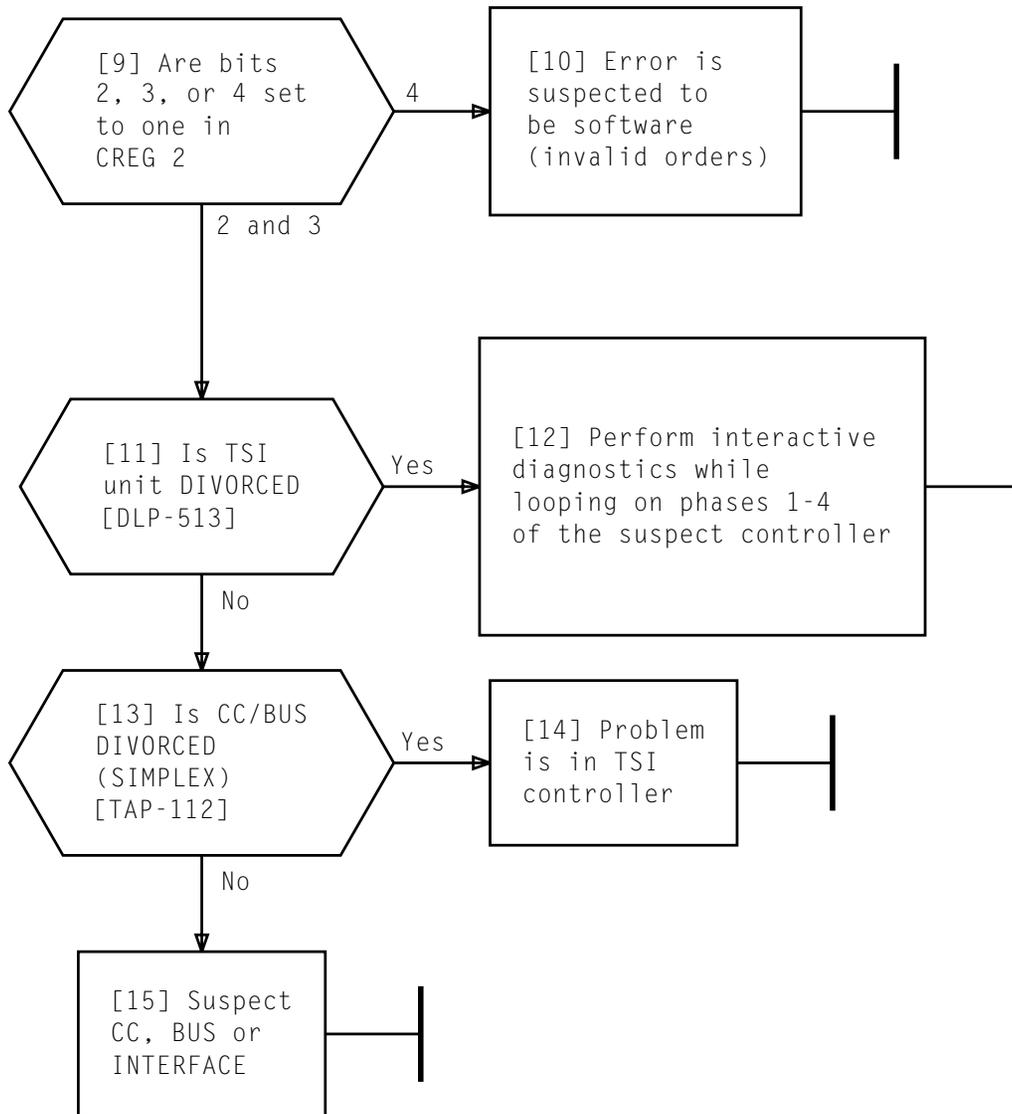
Figure 3 - TSI CREGs

NOTES

1. In-service TSI unit should only be considered.
2. If any bit 5-7 is **only** bit(s) set, then printout should be saved and NESAC should be notified of possible software error

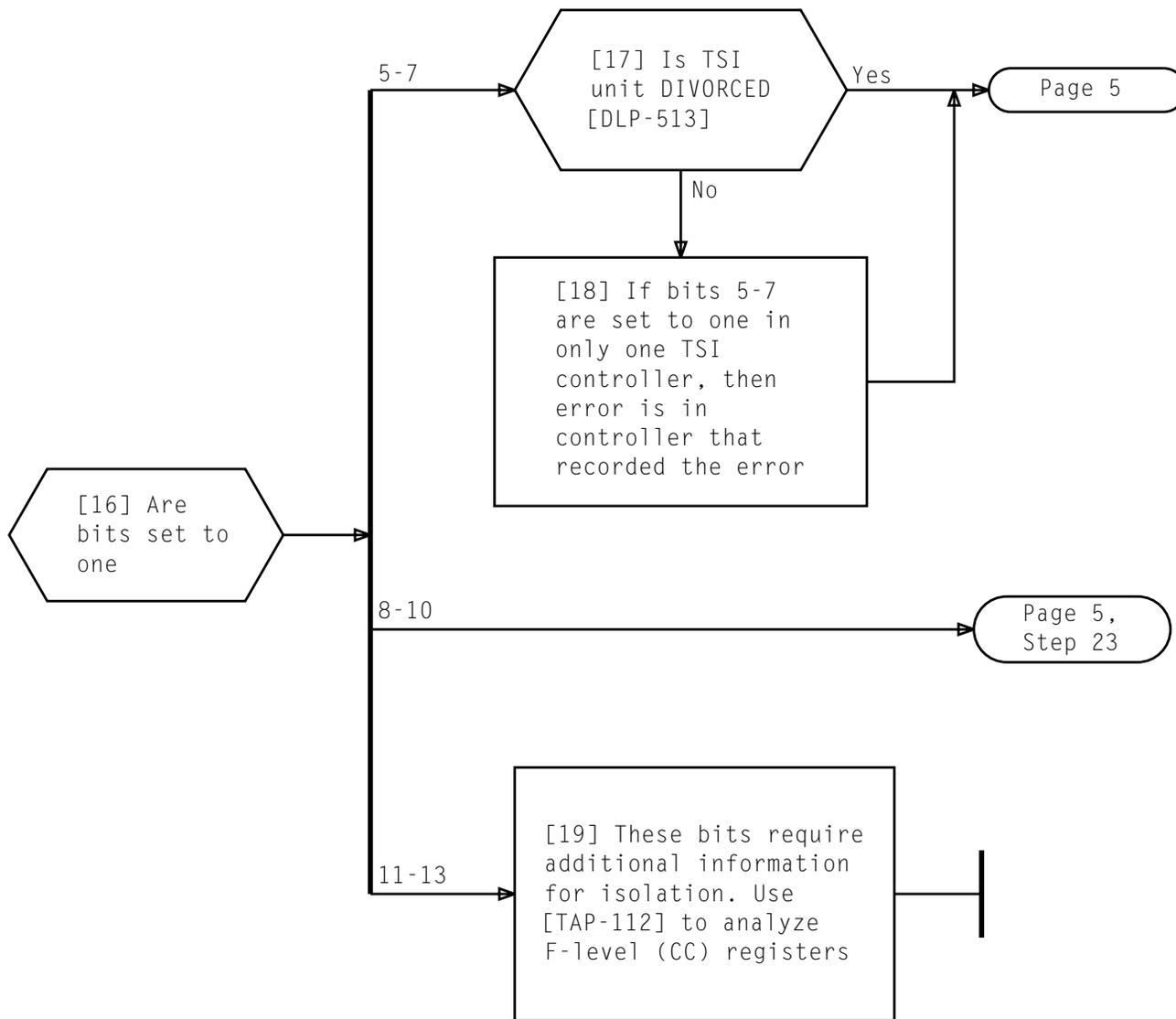
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ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE



ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE

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ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE

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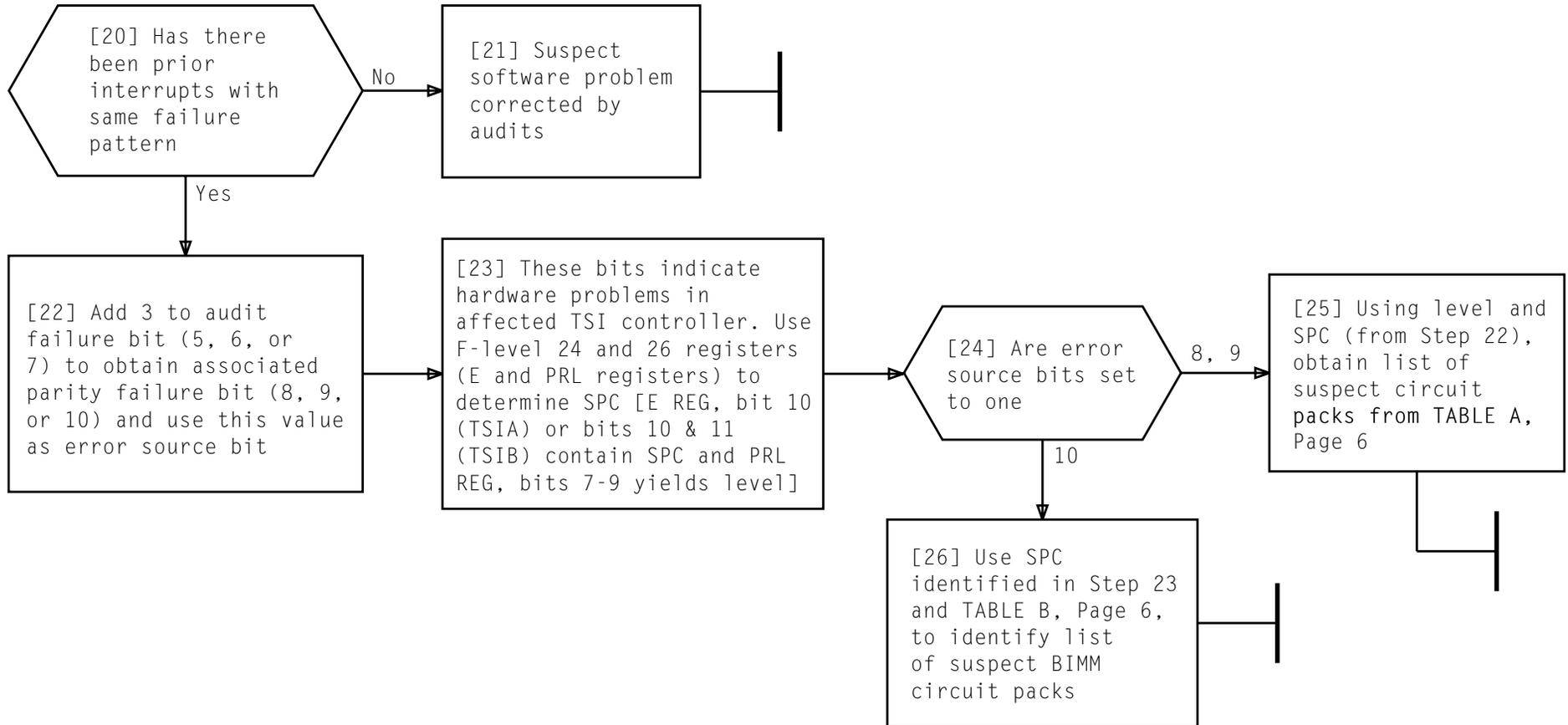
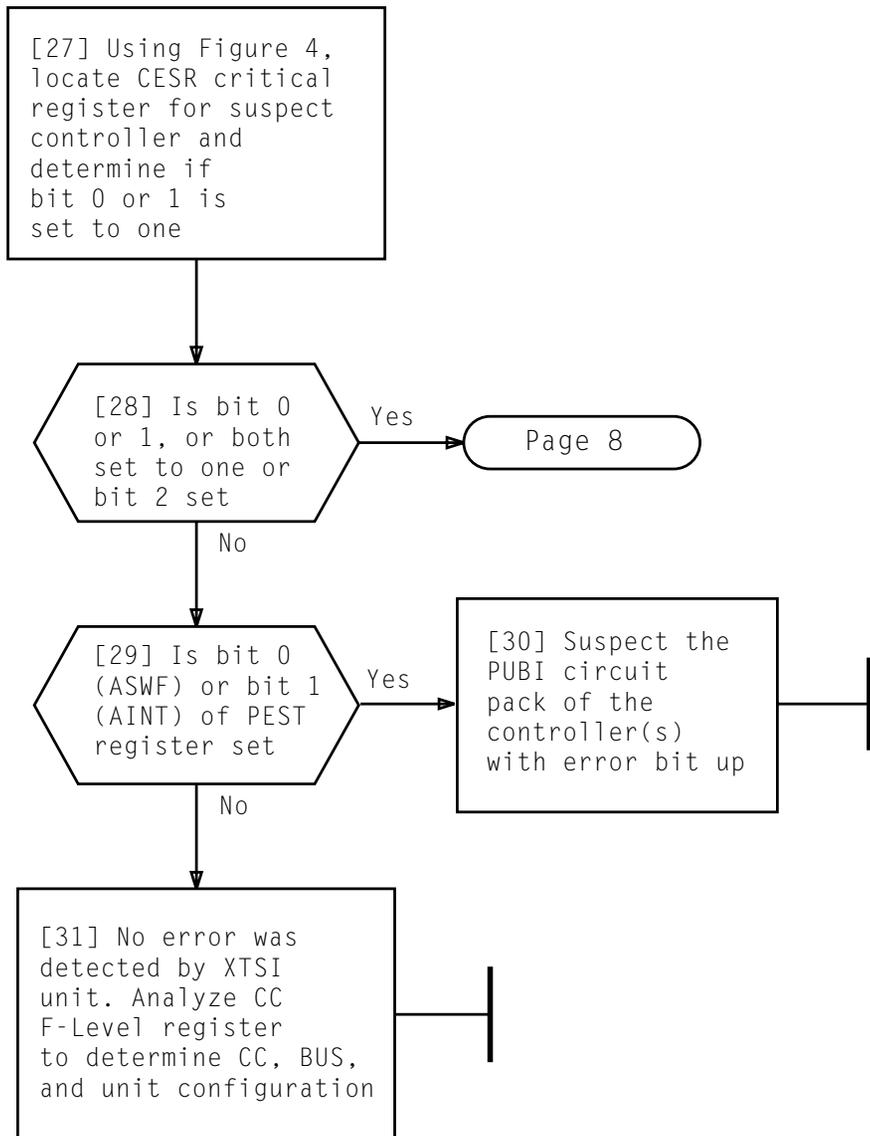


TABLE A SUSPECT TSM MEMORY PACKS SD-4A023-01,02										
SPC	ERROR BIT	CIRCUIT PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	8	FA543	46-26	46-25	46-24	46-23	46-22	46-21	46-20	46-19
	9	FA541	46-44	46-43	46-42	46-41	46-40	46-39	46-38	46-37
1	8	FA543	68-26	68-25	68-24	68-23	68-22	68-21	68-20	68-19
	9	FA541	68-44	68-43	68-42	68-41	68-39	68-38	68-37	68-36
SD-4A083-01										
0	8	FA1780*	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
	9	FA1781†	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
1	8	FA1780*	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
	9	FA1781†	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
2	8	FA1780*	52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
	9	FA1781†	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04
3	8	FA1780*	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37
	9	FA1781†	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
* May be FA1816										
† May be FA1817										

TABLE B BIMM SUSPECT PACKS (SD-4A023-01, 02); (SD-4A083-01)				
CIRCUIT PACK TYPE	SPC 0	SPC 1	SPC 2	SPC 3
FA556	42-52	64-52	NA	NA
FA555	56-38			
FA1783	28-28	40-28	52-28	64-28

ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE

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```

A 06 REPT: F-LEVEL @52405422 MFNUM=00000010 MICON=40000020 MSG IP
LV=0040 DO=00000002 D1=04000000 D2=00000037 D3=00000200
DATA: TSI CRITICAL REGISTERS
00002212 00002212 00040213 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000
00000000 00003000 00000022 00000732 23246400 01331111
74177741 00000377 43344334 00004334 77776401 00000020
04000106 00000000 00000000 01000000 00000000 00005100
00020177 10034140 00000000 00000000 00000100 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
00000006 43777777 55555555 55555555 55555555 55555555
00006004 00006004 00040007 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000
00000000 00003000 00000022 00000732 23246400 01531452
74177741 00000377 43344334 00004334 77776401 00000020
04000106 00000000 00000000 01000000 00000000 00005503
00020177 14064140 00000000 00000000 00000000 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
DATA: PERIPHERAL SYSTEM DATA
00103466 00000003 00000000 00000000 00000000 00000012
00000004 00000012 00000004 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00001540 00001020 01010000 00000020 00000100
DATA: FAULT RECOGNITION ISOLATION DATA
00000034 00000000 00000142 00000000 00000005 00000000
01/01/70 14:06:51
#628
  
```

Figure 4 - XTSI Critical Registers

ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE

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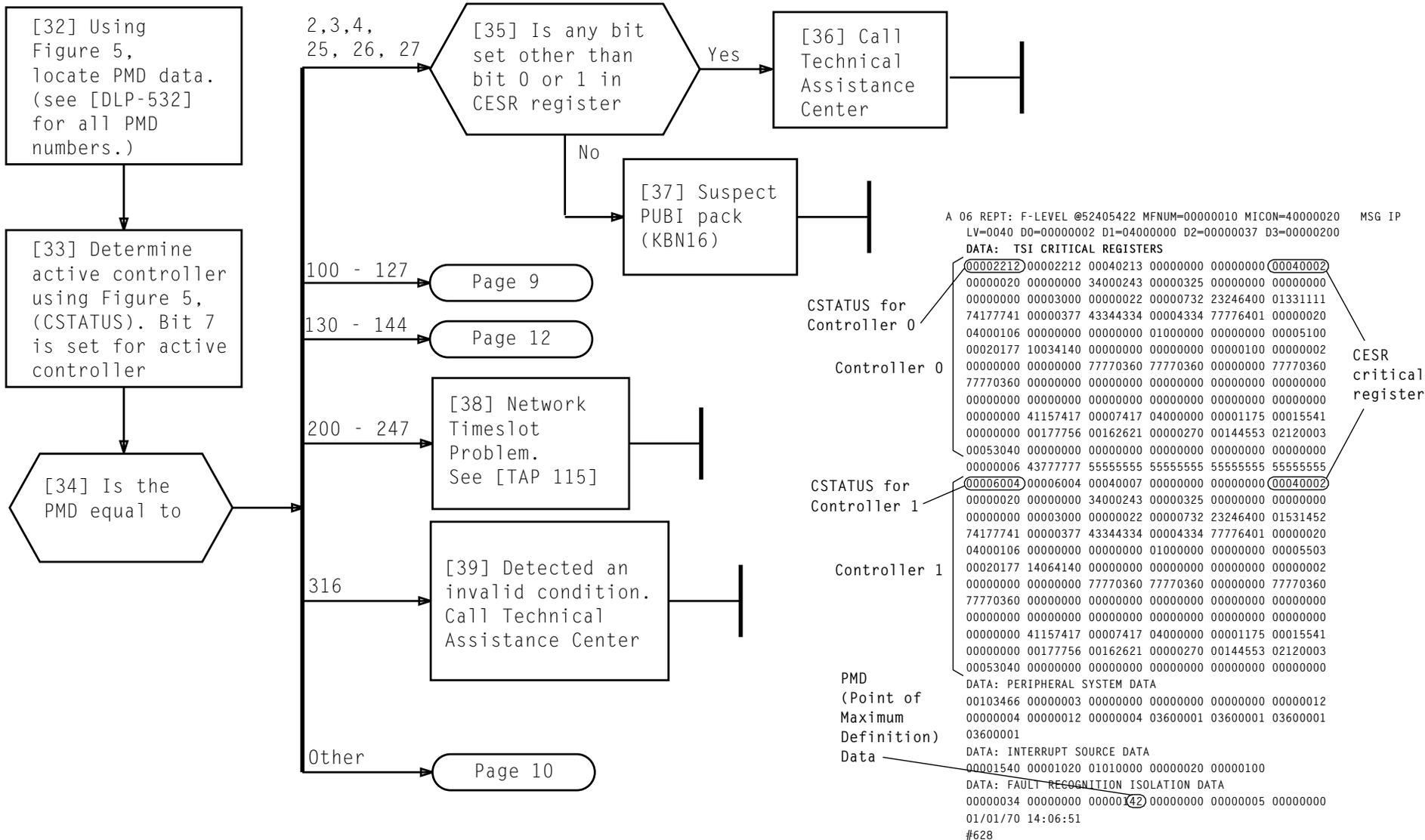
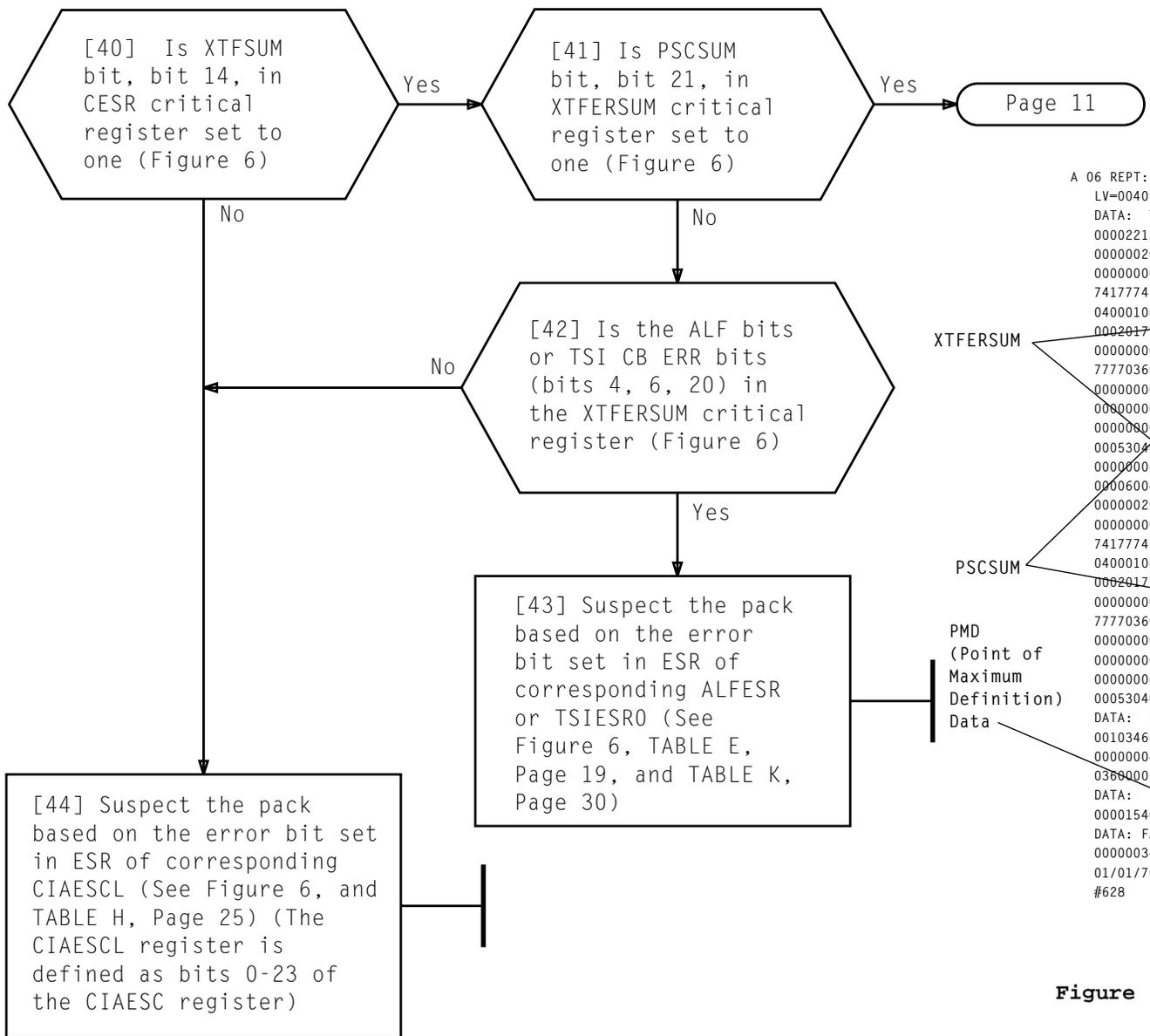


Figure 5 - XTSI Critical Registers

ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE

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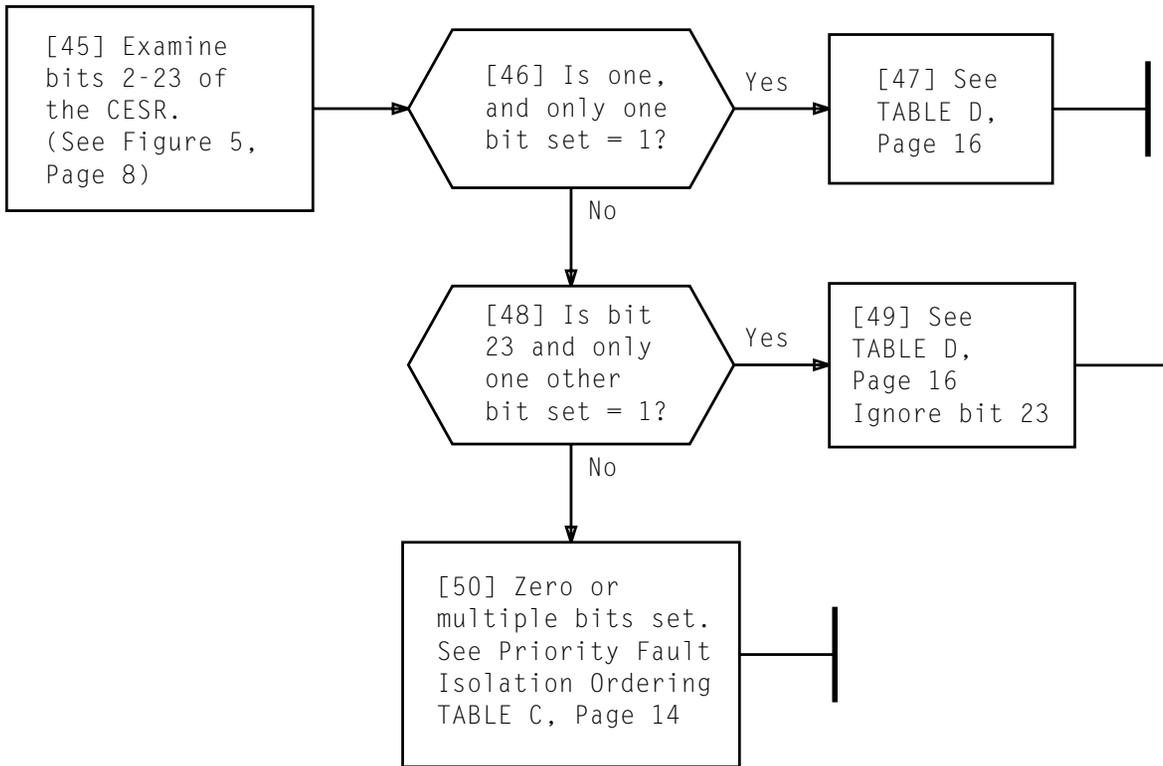
```

A 06 REPT: F-LEVEL @52405422 MFNUM=00000010 MICON=40000020 MSG IP
LV=0040 D0=00000002 D1=04000000 D2=00000037 D3=00000200
DATA: TSI CRITICAL REGISTERS
00002212 00002212 00040213 00000000 00000000 00040002 TSIESRO
00000020 00000000 34000243 00000325 00000000 00000000 TSIESR1
00000000 00003000 00000022 00000732 23246400 01331111 CESR
74177741 00000377 43344334 00004334 77776401 00000020 critical
04000106 00000000 00000000 01000000 00000000 00005100 register
00020177 10034140 00000000 00000000 00000100 00000002
00000000 00000000 07770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
00000006 43777777 55555555 55555555 55555555 55555555
00006004 00006004 00040007 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000 TSIESRO
00000000 00003000 00000022 00000732 23246400 01531452
74177741 00000377 43344334 00004334 77776401 00000020 TSIESR1
04000106 00000000 00000000 01000000 00000000 00005503
00020177 14064140 00000000 00000000 00000000 00000002
00000000 00000000 07770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
DATA: PERIPHERAL SYSTEM DATA
00103466 00000003 00000000 00000000 00000000 00000012
00000004 00000012 00000004 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00001540 00001020 01010000 00000020 00000100
DATA: FAULT RECOGNITION ISOLATION DATA
00000034 00000000 00000142 00000000 00000005 00000000
01/01/70 14:06:51
#628
  
```

Figure 6 - XTSI Critical Registers

ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE

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[51] Perform an EXCLUSIVE OR (or compare) between critical registers PSCSUM and PSCPEST. Any resultant "1s" should indicate a suspect PSC. Replace the pack based on error bits in the corresponding D3UESR. [See the PSCAUX DATA DUMP that accompanied the interrupt. (See Figure 7 and TABLE J, Page 28)]

```

DUMP
SIZE      PUFRR INT   ER CODE_H ER CODE_L  RTN ADR_H  RTN ADR_L
D3UX      D3UX USTAT D3UX STAT  D3UX ESR   D3UX CTL   D3UX EXR
WTT WD1   WTT WD2   WTT WD3   WTT WD4   WTT WD5   WTT WD6
WTT WD7   WTT WD8   WTT WD9   WTT WD10  WTT WD11  WTT WD12
WTT WD13  WTT WD14  WTT WD15  WTT WD16  WTT WD17  WTT WD18
WTT WD19  WTT WD20  WTT WD21  WTT WD22  WTT WD23  WTT WD24
WTT WD25  WTT WD26  WTT WD27  WTT WD28  WTT WD29  WTT WD30
WTT WD31  WTT WD32  WTT WD33  WTT WD34  WTT WD35  WTT WD36
WTT WD37  WTT WD38  WTT WD39  WTT WD40  WTT WD41  WTT WD42
WTT WD43  WTT WD44  WTT WD45  WTT WD46  WTT WD47  WTT WD48
WTT WD49  WTT WD50  WTT WD51  WTT WD52  WTT WD53  WTT WD54
WTT WD55  WTT WD56  WTT WD57  WTT WD58  WTT WD59  WTT WD60
WTT WD61  WTT WD62  WTT WD63  WTT WD64  WTT WD65  WTT WD66
WTT WD67  WTT WD68  TASK_ID   ERR_DATA1  ERR_DATA2  ERR_DATA3
ERR DATA4 ERR DATA5 ERR DATA6 ERR DATA7 ERR DATA8 ERR DATA9
ERR DATA10 ERR DATA11 ERR DATA12 ERR DATA13 ERR DATA14 ERR DATA15
STACK WD1  STACK WD2  STACK WD3  STACK WD4  STACK WD5  STACK WD6
STACK WD7  STACK WD8  STACK WD9  STACK WD10 STACK WD11  STACK WD12
STACK WD13 STACK WD14  STACK WD15 STACK WD16  STACK WD17  STACK WD18

```

Analysis:

Dump Size—Report Type and Block Size

Octal 00010344

PUFR_INT—Development Only.

ER_CODE_H—High 8-bit of a 32-bits Error Code

Bit 0-7 = Contains the software issue number

ER_CODE_L—Low 24-bit of a 32-bits Error Code

Bit 0-11 = Contains the code (See Codes and Class Layout for values.)

12-15 = Contains the error class (See Error Codes and Class Layout for values.)

16-23 = Number of 32 bit error words reported/found in Auxiliary Data Dump.

The remainder is stack information (up to maximum number of error words).

RTN_ADR_H—Pack Type

Bit 0-8 = D3U Pack type = 1

RTN_ADR_L—Low 24-Bits of Failing Address

Bit 0-23 = Failing Address

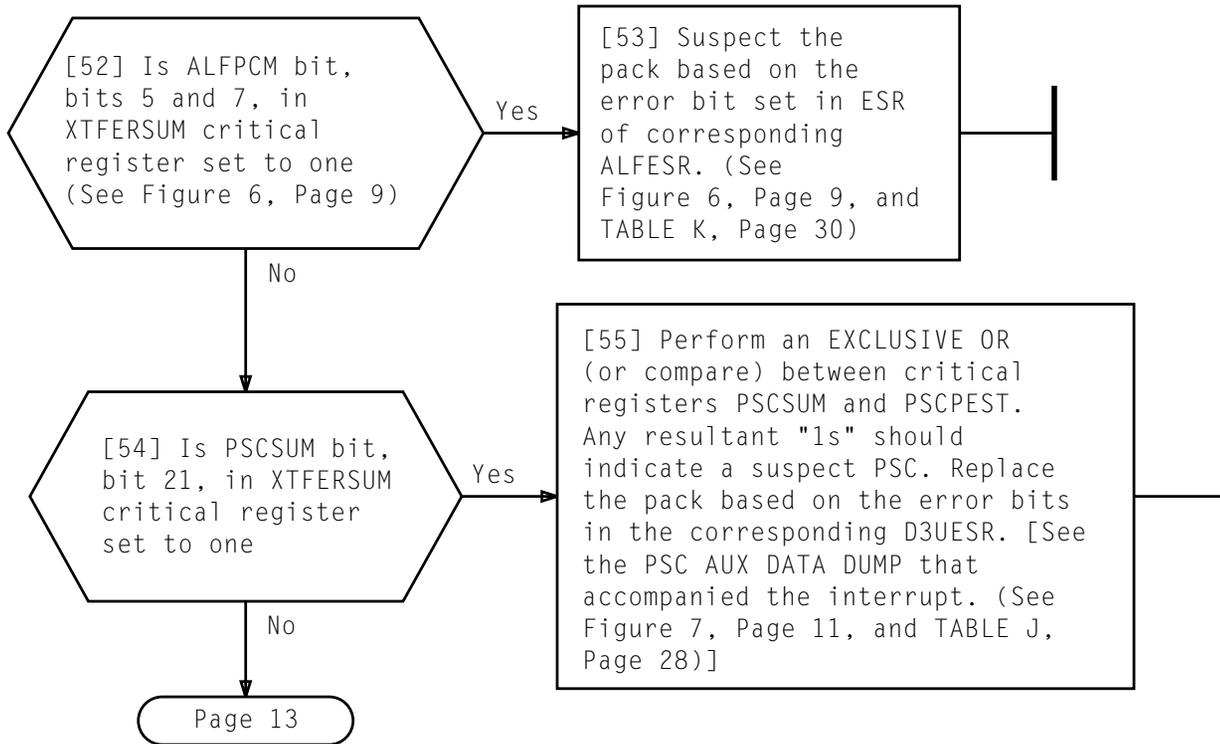
D3UX Subunit - D3U Subunit data

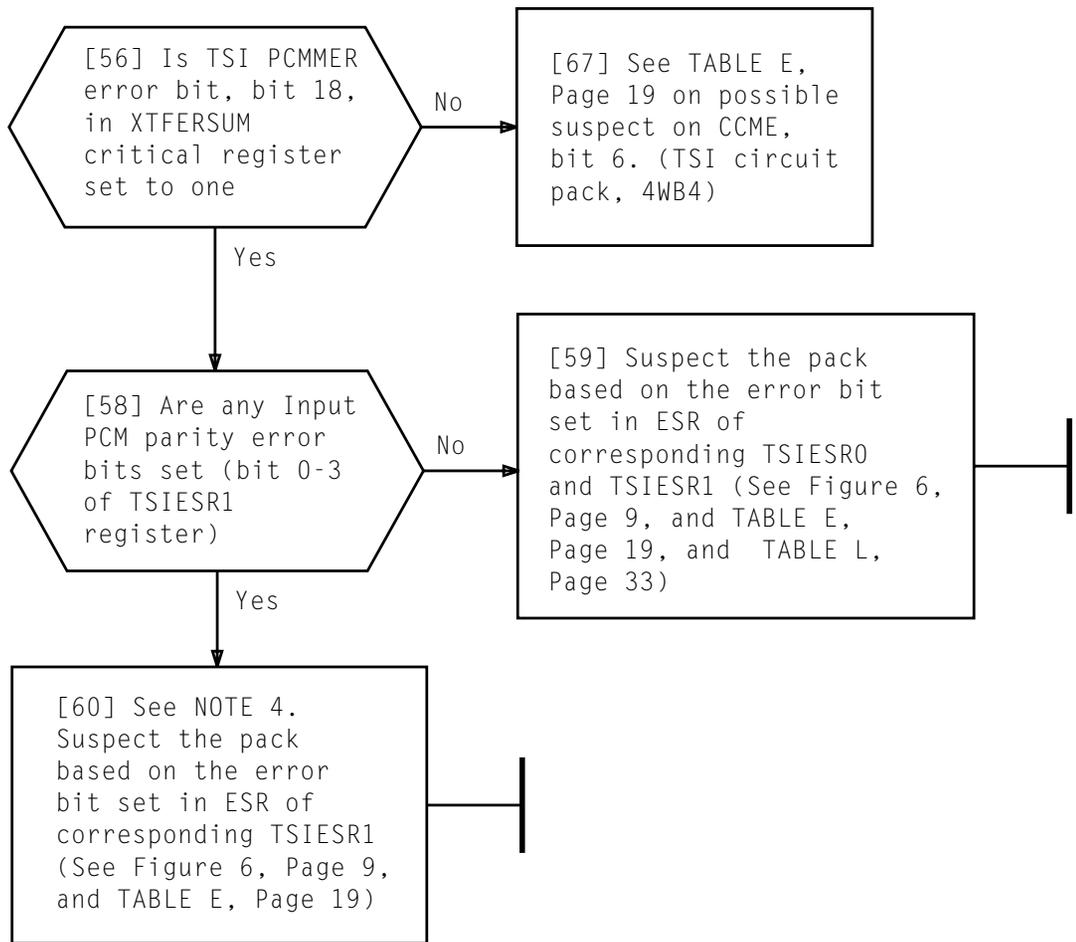
Bit 0-8 = D3U member number (Between 0 and 7) (UTMEM)

9-11 = D3U Unit Type = 0

12-23 Unused

Figure 7 - Example of D3U Shared Memory Auxiliary Data Dump





NOTE 4	
If the error occurs more than once on the same sub-branch (the subunit is the same in the AUX DUMP for all errors), all the circuit packs on the sub-branch should be replaced until the fault disappears	
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TABLE C SUSPECT PRIORITY TABLE AND SUSPECT PACK TABLES				
PRIORITY LEVEL	TYPE OF ERROR	ASSOCIATED ERROR SOURCE REGISTER	SUSPECT BIT(S)	SUSPECT PACK TABLE WITH BIT SET
1	CLOCK ERROR	CESR	15,22	D
		TSIESRO	4,7,8,9	E
2	ACT/STBY ERROR IN HARDWARE	TSIESRO	18	E
		XTFERSUM	22	F
		CESR	10*	D
3	UNRECOVERABLE ERROR	CESR	9	D
4	STACK BOUNDARY ERROR	EXESR	0	G
5	HARD-INIT ERROR	CESR	8	D
6	HARDWARE ERROR	CESR	2,3,6,12,13,19,20,21	D
		CIAESC	1,2,3,4,5,6	H
		GESR	0-3,4-7,8-11,12,13,14	I
		EXESR	2,3,5-12,15	G
7	CONTROL BUS ERROR	CIAESC	7	H
		XTFERSUM	0,1,2,3,4,6,8,16,17	F
8	AUDIT ERROR	CESR	11	D
9	PSC ERROR	CESR	10*	D
		D3UESR	10,11,12,13,14,15,16,17,19	J
* Bit 10 of CESR and GRSVERCODE of 30, 31 or 32 results in ACT/STDY Error in hardware. For other values of GRSVERCODE register, the type of error is PSC error.				

ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME-SLOT INTERCHANGE AND EXPANDED TIME-SLOT INTERCHANGE

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TABLE C (CONTD)				
SUSPECT PRIORITY TABLE AND SUSPECT PACK TABLES				
PRIORITY LEVEL	TYPE OF ERROR	ASSOCIATED ERROR SOURCE REGISTER	SUSPECT BIT(S)	SUSPECT PACK TABLE WITH BIT SET
10	OUTPUT PCM PARITY ERROR	ALFESR	8,9,10,11,12,13	K
		D3UESR	4,5,6,7,8,9	J
11	TSI INPUT PCM PARITY ERROR	TSIESR1	0-3	L
12	TSI PACK ERROR	TSIESR0	4,10-17,19	E
		TSIESR1	4-23	L
13	ALNK ERROR	ALFESR	16	K
14	ALF LOCAL PCM PARITY ERROR	ALFESR	14,15	K
15	ALF BUSY/IDLE & INTERNAL PARITY ERROR	ALFESR	4,18,19,20,21,22	K
16	TRPF ERROR	ALFESR	17	K
17	PSM BUS MISMATCH ERROR	TSIESR0	6	E
18	SOFTWARE ERROR	CESR	7	D
19	SANITY TIMER	EXESR	1	G
20	CONTROLLER MISMATCH ERROR	CESR	23	D

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TABLE D CONTROLLER ERROR SOURCE REGISTER (CESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	ASWF	All Seems Well Failure	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
1	AINT	Autonomous Interrupt	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
2	PUPFE	Peripheral Unit Bus Even Parity Failure	KBN16 UN559 UN559	052-137 052-164 052-180	061-137 061-164 061-180
3	PUPFO	Peripheral Unit Bus Odd Parity Failure	KBN16 UN559 UN559	052-137 052-172 052-156	061-137 061-172 061-156
4	APUT	Autonomous Peripheral Unit Trouble	KBN16 UN547	052-137 052-082	061-137 061-082
5	SEQERR	Error Detected by PUB Sequencers	KBN16 UN548	052-137 052-114	061-137 061-114
6	UNASOP	Invalid/Unassigned OP-Code	KBN16 UN559 UN548	052-137 052-164 052-114	061-137 061-164 061-114
7	SWERRO	Firmware Error Bit 0, Forces Soft Initialization (Restart at point of error)	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082

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TABLE D (CONTD)					
CONTROLLER ERROR SOURCE REGISTER (CESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
8	SWERR1	Firmware Error Bit 1, Forces Hard Initialization (does not clear stable calls)	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
9	SWERR2	Firmware Error Bit 2, Forces Zero Start (clears stable calls)	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
10	SWERR3	Firmware Error Bit 3, PSC Software Detection Error	KBN16 UN548 UN557 UN547 PSCs	052-137 052-114 052-106 052-082 *	061-137 061-114 061-106 061-082 *
11	AUDSUM	Audit Error Source Summary	KBN16 UN548 UN557 UN547 4WB4	052-137 052-114 052-106 052-082 014-098	061-137 061-114 061-106 061-082 031-098
12	MODFL	Mode Failure	KBN16 UN559 UN559	052-137 052-156 052-164	061-137 061-156 061-164
13	PPE	PUB1 Parity Error	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
* See TABLE M for all PSC (D3U) locations.					

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TABLE D (CONTD)					
CONTROLLER ERROR SOURCE REGISTER (CESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
14	XTFSUM	XTSI Fabric Error Source Summary	See TABLE F		
15	LCLKF	Local Clock Failure	KBN16 UN548	052-137 052-114	061-137 061-114
16	LASUM	LAN Access Error Source Summary	KBN16 UN548	052-137 052-114	061-137 061-114
17	SPARESUM	Spare Pack Error Source Summary (Future Expansion)	KBN16 UN548	052-137 052-114	061-137 061-114
18	CIASUM	Control Bus and Image Administration Error Source Summary	See TABLE H		
19	GRAMSUM	Global Ram Local Error Source Summary	UN557 KBN16	052-106 052-137	061-106 061-137
20	EXECSUM	EXEC Local Error Source Summary	UN548 KBN16	052-114 052-137	061-114 061-137
21	BPSUM	Backplane Error Source Summary	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
22	CLKSUM	Clock Error Source Summary	UN548 KBN16 4WB4	052-114 052-137 014-098	061-114 061-137 031-098
23	CCMM	GRAM, EXEC Complex Cross Controller Mismatch	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082

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TABLE E					
TSI ERROR SOURCE REGISTER 0 (TSIESR0)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	CBDPE0	Control Bus Data Write Parity Error for Byte 0	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 031-090 061-082
1	CBDPE1	Control Bus Data Write Parity Error for Byte 1	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 031-090 061-082
2	CBDPE2	Control Bus Data Write Parity Error for Byte 2	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 031-090 061-082
3	CBDPE3	Control Bus Data Write Parity Error for Byte 3	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 031-090 061-082
4	TSCERR	Time-Slot Counter Error. Does Not Match Frame Bit from Network Clock	4WB4	014-098	031-098
5	UNUSED				
6	CCME	Cross-Controller Mismatch Error	4WB4	014-098	031-098
7	NSE	Network Sync Error	4WB4	014-098	031-098
8	PLE	32.768 MHz Phase Lock Error	4WB4	014-098	031-098
9	CSE	32.768 MHz Clock Source Error. 32 MHz Distribution Stuck Low or High	4WB4	014-098	031-098

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TABLE E (CONTD)					
TSI ERROR SOURCE REGISTER 0 (TSIESR0)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
10-13	TSXRMM	Mismatch Error	4WB4	014-098	031-098
14	PCE0	TSXR0 PCM Enable Parity Error	4WB4	014-098	031-098
15	PCE1	TSXR1 PCM Enable Parity Error	4WB4	014-098	031-098
16	PCE2	TSXR2 PCM Enable Parity Error	4WB4	014-098	031-098
17	PCE3	TSXR3 PCM Enable Parity Error	4WB4	014-098	031-098
18	ACTMME	Active/Standby Signal Mismatch Error	4WB4	014-098	031-098
19	BMIMSE	Buffer Memory Input MUX Select Error	4WB4	014-098	031-098
20-23	UNUSED				

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TABLE F XTF FABRIC ERROR SUMMARY REGISTER (XTFERSUM)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	WTPERB0	When Set, Indicates a Byte 0 Parity Error Occurred on an FBI Local CB Write	4WB2 UN547	014-090 052-082	031-090 061-082
1	WTPERB1	When Set, Indicates a Byte 1 Parity Error Occurred on an FBI Local CB Write	4WB2 UN547	014-090 052-082	031-090 061-082
2	WTPERB2	When Set, Indicates a Byte 2 Parity Error Occurred on an FBI Local CB Write	4WB2 UN547	014-090 052-082	031-090 061-082
3	WTPERB3	When Set, Indicates a Byte 3 Parity Error Occurred on an FBI Local CB Write	4WB2 UN547	014-090 052-082	031-090 061-082
4	ALFOCBER	When Set, Indicates Any CB Related Error on ALF0	4WB6 4WB2 UN547	014-082 014-090 052-082	- 031-090 061-082
5	ALFOPCMER	When Set, Indicates PCM Related Error on ALF0. Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB6 4WB4	014-082 014-098	- 031-098
6	ALF1CBER	When Set, Indicates any CB related Error on ALF1	4WB6 4WB2 UN547	014-106 014-090 052-082	- 031-090 061-082
7	ALF1PCMER	When Set, Indicates and PCM Related Error on ALF1. Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB6 4WB4	014-106 014-098	- 031-098
8	ALF2CBER	When Set, Indicates any CB related Error on ALF2	4WB6 4WB2 UN547	- 014-090 052-082	031-082 031-090 061-082
9	ALF2PCMER	When Set, Indicates and PCM Related Error on ALF2. Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB6 4WB4	- 014-098	031-082 031-098

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TABLE F (CONTD)					
XTF FABRIC ERROR SUMMARY REGISTER (XTFERSUM)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
10	ALF3CBER	When Set, Indicates any CB related Error on ALF3	4WB6 4WB2 UN547	- 014-090 052-082	031-106 031-090 061-082
11	ALF3PCMER	When Set, Indicates and PCM Related Error on ALF3. Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB4 4WB6	- 014-098	031-106 031-098
12	SPARECBER	When Set, Indicates any CB Related Error on the SPARE Controller Client	4WB2 UN547	014-099 052-082	031-090 061-082
13	SPAREPCMER	When Set, Indicates any PCM Related Error on the SPARE Controller Client.	4WB4 4WB6 4WB6	014-098 014-082 014-106	031-098 031-082 031-106
14	TERMOCBER	When Set, Indicates any CB Related Error on the TERMO Controller Client	4WB7 4WB2 4WB6 UN547	014-008 014-090 052-082 052-082	031-008 061-090 061-082 061-082
15	TERMOPCMER	When Set, Indicates any PCM Bus Related Error on the TERMO Controller Client	4WB7 4WB4 4WB6	014-008 014-098 014-082	031-008 031-098 031-082
16	TERM1CBER	When Set, Indicates any CB Related Error on the TERM1 Controller Client	PSCs 4WB2 UN547	* 014-090 052-082	* 061-090 061-082
* See TABLE M for all PSC (D3U) locations.					

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TABLE F (CONTD)
XTF FABRIC ERROR SUMMARY REGISTER (XTFERSUM)

BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
17	TERM1PCMER	When Set, Indicates Any PCM Bus Related Error on the TERM1 Controller Client	4WB4 4WB6 4WB6	014-098 014-082 014-106	031-098 031-082 031-106
18	TSIPCMNMR	When Set, Indicates Any TSI Detected PCM, Error, Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB4 4WB6 4WB6 PSCs	014-098 014-082 014-106 *	031-098 031-082 031-106 *
19	TSIPCMMER	When Set, Indicates Any TSI Detected Cross-Controller Mismatch PCM Error	4WB4 4WB6 4WB6	014-098 014-082 014-106	031-098 031-082 031-106
20	TSICBER	When Set, Indicates Any TSI Detected CB Related Error	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 061-090 061-082
21	PSCSUM	When Set, Indicates That a PSC Error Summary Bit is Set in the PSCERSUM Register	PSCs 4WB4 4WB6 4WB6	* 014-098 014-082 014-106	* 031-098 031-082 031-106
22	ASMMER	When Set, Indicates a Mismatch Between the Duplicated Act./Sty. Signals Within the Local Controller or a Mismatch Between the Act./Sty. State of Controller 0 and The Act./Sty. State of Controller 1 (Act./Act. or Sty./Sty.).	4WB2 KBN16	014-090 052-137	031-090 061-137
23	UNUSED	Can not be Written and is Read as 0			

* See TABLE M for all PSC (D3U) locations.

TABLE G EXEC ERROR SOURCE REGISTER (EXESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	STKBND	Stack Bounds Error	UN548	052-114	061-114
1	SANTIMEX	Sanity Timer Expiration	UN548	052-114	061-114
2	ILLOC	Illegal Opcode	UN548	052-114	061-114
3	SRCPERR	Source Parity Error	UN548 UN557 KBN16 UN547 4WB6 4WB6 4WB4 PSCs	052-114 052-106 052-137 052-082 014-082 014-106 014-098 *	061-114 061-106 061-137 061-082 031-082 031-106 031-098 *
4	UNUSED				
5-12	MRPE	MicroRAM Parity Error	UN548	052-114	061-114
13-14	UNUSED				
15	SOFTERR	Software Error (causes EXEC ESR bit to be set in PUBI)	UN548	052-114	061-114
16-23	FPEMW	Force Parity Error in Microword			
* See TABLE M for all PSC (D3U) locations.					

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**TABLE H
CIA ERROR, STATUS AND CONTROL REGISTER (CIAESC)**

BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	FLASHPE	FLASH Write Parity Error (Writing Clears Bit 0-7)	UN547	052-082	061-082
1	SDATPE	Source A Data Parity Error	UN547 UN548 UN557 KBN16 4WB6 4WB6 4WB4 PSCs	052-082 052-114 052-106 052-137 014-082 014-106 014-098 *	061-082 061-114 061-106 061-137 031-082 031-106 031-098 *
2	DDATPE	Destination Data Parity Error	UN547	052-082	061-082
3	SMOPE	Source Mode & Offset Parity Error	UN547	052-082	061-082
4	DMOPE	Destination Mode & Offset Parity Error	UN547	052-082	061-082
5	XTFWPE	XTF Client Write Parity Error	UN547 4WB2 4WB6 4WB6 4WB4 PSCs	052-082 014-090 014-082 014-106 014-098 *	061-082 031-090 031-082 031-106 031-098 *
6	XTFRPE	XTF Client Read Parity Error	UN547 4WB2 4WB6 4WB6 4WB4 PSCs	052-082 014-090 014-082 014-106 014-098 *	061-082 031-090 031-082 031-106 031-098 *
7	ESACK	Client SACK Error	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
* See TABLE M for all PSC (D3U) locations.					

**ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF),
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**TABLE H (CONTD)
CIA ERROR, STATUS AND CONTROL REGISTER (CIAESC)**

BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
8-15	LSACK	Last SACK Received. Gives Value of SACK Received During Last CB Transfer	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
16-23	LSACKEXP	Last SACK Expected. Gives Value of SACK Expected During Last CB Transfer	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
24	FLPTR24	Overflow Bit for Left Shifting of CIA Address Register	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
25	FLPTR25	Overflow Bit for Left Shifting of CIA Address Register	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
26	FLSHRST	Toggle this Bit for Hard Reset of the Flash Card	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
27	NRFLR	Near Flash ready. The FLASH Card on this CIA Circuit Pack is ready for Another Access	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
28	SNCFLR	Sync Flash Ready. The FLASH Card on this CIA Circuit Pack is Ready For Another Access	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
29-31	UNUSED				

* See TABLE M for all PSC (D3U) locations.

TABLE I GRAM ERROR SOURCE REGISTER (GESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0-3	ERAP	RAM Bank A Parity Error	UN557	052-106	061-106
4-7	ERBP	RAM Bank B Parity Error	UN557	052-106	061-106
8-11	EDDP	Destination Bus Address Parity Error	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
12	EDAP	Destination Bus Address Parity Error	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
13	ESAAP	Source Bus A Address Parity Error	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
14	ESBAP	Source Bus B Address Parity Error	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
15	EXUMM	Update Bus Mismatch	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
16	EXSMM	Syndrome Mismatch	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
17-23	UNUSED	All zero			

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TABLE J
D3U ERROR SOURCE REGISTER (D3UESR)

BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	CBDPE0	Control Bus Data Parity Error, Byte 0	PSCs 4WB2 UN547	* 014-090 052-082	* 031-090 061-082
1	CBDPE1	Control Bus Data Parity Error, Byte 1	PSCs 4WB2 UN547	* 014-090 052-082	* 031-090 061-082
2	CBDPE2	Control Bus Data Parity Error, Byte 2	PSCs 4WB2 UN547	* 014-090 052-082	* 031-090 061-082
3	CBDPE3	Control Bus Data Parity Error, Byte 3	PSCs 4WB2 UN547	* 014-090 052-082	* 031-090 061-082
4	TSCPEE	Time-Slot Count Even Bits Parity Error	PSCs 4WB4	* 014-098	* 031-098
5	TSCPEO	Time-Slot Count Odd Bits Parity Error	PSCs 4WB4	* 014-098	* 031-098
6	PCMBIE0	PCM Out Bus 0 (2) Busy/Idle Error. (PCM Bus Busy/Idle Bits Don't Agree)	PSCs 4WB4	* 014-098	* 031-098
7	PCMBIE1	PCM Out Bus 1 (3) Busy/Idle Error. (PCM Bus Busy/Idle Bits Don't Agree)	PSCs 4WB4	* 014-098	* 031-098
8	PCMOPE0	PCM Out Bus 0 (2) Parity Error	PSCs 4WB4	* 014-098	* 031-098
* See TABLE M for all PSC (D3U) locations.					

TABLE J (CONTD)					
D3U ERROR SOURCE REGISTER (D3UESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
9	PCMOPE1	PCM Out Bus 1 (3) Parity Error	PSCs 4WB4	* 014-098	* 031-098
10	PCMOSEQ	PCM Out Sequence Error	PSCs 4WB4	* 014-098	* 031-098
11	PCMISEQ	PCM In Sequence Error	PSCs 4WB4	* 014-098	* 031-098
12	PCMTCLE	PCM Control-Interface Error (TSC State machine Error)	PSCs 4WB4	* 014-098	* 031-098
13	DS1CLKPE	DS1 Clock Phase Error	PSCs 4WB4	* 014-098	* 031-098
14	CLKPE	33 MHz Clock Phase Error	PSCs 4WB4	* 014-098	* 031-098
15	PHALT	D3U Processor Halt	PSCs 4WB4	* 014-098	* 031-098
16	PBUSE	D3U Processor Bus Error	PSCs 4WB4	* 014-098	* 031-098
17	PPARE	D3U Processor Parity Error	PSCs 4WB4	* 014-098	* 031-098
18	D3USWERR	Software Error. D3U Processor has the Ability to Set this Bit	PSCs 4WB4	* 014-098	* 031-098
19-31	UNUSED	—	—	—	—
* See TABLE M for all PSC (D3U) locations.					

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TABLE K ALF ERROR REGISTER (ALFESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	CBDPE0	Indicates a Parity Error was Detected on Data From the CB Byte 0	4WB6 4WB6 4WB2 UN547	014-082 014-106 014-090 052-082	031-082 031-106 031-090 061-082
1	CBDPE1	Indicates a Parity Error was Detected on Data From the CB Byte 1	4WB6 4WB6 4WB2 UN547	014-082 014-106 014-090 052-082	031-082 031-106 031-090 061-082
2	CBDPE2	Indicates a Parity Error was Detected on Data From the CB Byte 2	4WB6 4WB6 4WB2 UN547	014-082 014-106 014-090 052-082	031-082 031-106 031-090 061-082
3	CBDPE3	Indicates a Parity Error was Detected on Data From the CB Byte 3	4WB6 4WB6 4WB2 UN547	014-082 014-106 014-090 052-082	031-082 031-106 031-090 061-082
4	ERIDLWR	Wrote ALFIDLE0 or ALFIDLE1 Without Having the Corresponding Enable Bit Set in ALFCTL	4WB6 4WB6	014-082 014-106	031-082 031-106
5-7	UNUSED				
8	ALFTSCPEE	Indicates a Parity Error was Detected on the TSC Even Bits	4WB6 4WB6 4WB4	014-082 014-106 014-098	031-082 031-106 031-098
9	ALFTSCPEO	Indicates a Parity Error was Detected on the TSC Odd Bits	4WB6 4WB6 4WB4	014-082 014-106 014-098	031-082 031-106 031-098
10	ALFPCMBIE0	Indicates a Parity Error was Detected on PCM Bus Busy/Idle 0	4WB6 4WB6 4WB4	014-082 014-106 014-098	031-082 031-106 031-098

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TABLE K (CONTD)					
ALF ERROR REGISTER (ALFESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
11	ALFPCMBIE1	Indicates a Parity Error was Detected on PCM Bus Busy/Idle 1	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
12	ALFPCMOPE0	Indicates a Parity Error was Detected on Data from PCM Output Bus 0	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
13	ALFPCMOPE1	Indicates a Parity Error was Detected on Data from PCM Output Bus 1	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
14	ALFPCMIPE0	Indicates a Parity Error was Detected on Data from PCM Input Bus 0	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
15	ALFPCMIPE1	Indicates a Parity Error was Detected on Data from PCM Input Bus 1	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
16	ALNKSUM	Indicates a Parity Error was Detected in One or More of the 16 A'Link Circuits. ALF Register ALNKPER indicates Which Circuit Detected the Error	4WB6	014-082	031-082
			4WB6	014-106	031-106
			UN546	052-026	061-026
			UN545	052-014	061-014

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TABLE K (CONTD)					
ALF ERROR REGISTER (ALFESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
17	TRPFSUM	Indicates that a Transmission parity Error (TRPF) was Detected in One or More of the 16 A'Link Circuits. ALF Register TRPFPER Indicates Which Circuit Detected the Error	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
18	BITMAPER0	Indicates a Parity Error was Detected on Data from the Busy/Idle Memory Circuit 0	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
19	BITMAPER1	Indicates a Parity Error was Detected on Data from the Busy/Idle Memory Circuit 1	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
20	BUFOPER	Indicates a Parity Error was Detected on Leading-Ones Detector Buffer Memory 0 Read Address	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
21	BUF1PER	Indicates a Parity Error was Detected on Leading-Ones Detector Buffer Memory 1 Read Address	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
22	DBISUM	Indicates that an Internal Matching Error in the LOD Delayed Busy/Idle Circuit Was Detected (Summary Bit for the DBIER Register)	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
23	NONE	This Bit Always Reads Zero. A Write to the ALFESR with Bit 23 Causes a 60 NS Pulse That Clears BUF (0/1) Per in the ALFESR	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014

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TABLE L TSI ERROR SOURCE REGISTER 1 (TSIESR1)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	0PCMIPER	PCM 0 Input Parity Error (from Clients)	4WB4 4WB6 PSCs	014-098 014-082 *	031-098 031-082 *
1	1PCMIPER	PCM 1 Input Parity Error (from Clients)	4WB4 4WB6 PSCs	014-098 014-082 *	031-098 031-082 *
2	2PCMIPER	PCM 2 Input Parity Error (from Clients)	4WB4 4WB6 PSCs	014-098 014-106 *	031-098 031-106 *
3	3PCMIPER	PCM 3 Input Parity Error (from Clients)	4WB4 4WB6 PSCs	014-098 014-106 *	031-098 031-106 *
4	TSM0MM	Time-Slot Memory 0 Mismatch Error	4WB4	014-098	031-098
5	TSM1MM	Time-Slot Memory 1 Mismatch Error	4WB4	014-098	031-098
6	TSM2MM	Time-Slot Memory 2 Mismatch Error	4WB4	014-098	031-098
7	TSM3MM	Time-Slot Memory 3 Mismatch Error	4WB4	014-098	031-098
8	PCA0	Time-Slot Memory 0 Address Parity Error	4WB4	014-098	031-098
9	PCA1	Time-Slot Memory 1 Address Parity Error	4WB4	014-098	031-098
10	PCA2	Time-Slot Memory 2 Address Parity Error	4WB4	014-098	031-098
11	PCA3	Time-Slot Memory 3 Address Parity Error	4WB4	014-098	031-098
12	PCD0	Time-Slot Memory 0 Data Parity Error	4WB4	014-098	031-098
* See TABLE M for all PSC (D3U) locations.					

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TABLE L (CONTD)					
TSI ERROR SOURCE REGISTER 1 (TSIESR1)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
13	PCD1	Time Slot Memory 1 Data Parity Error	4WB4	014-098	031-098
14	PCD2	Time Slot Memory 2 Data Parity Error	4WB4	014-098	031-098
15	PCD3	Time Slot Memory 2 Data Parity Error	4WB4	014-098	031-098
16	PCB0	Time Slot Memory 0 Busy/Idle Parity Error	4WB4	014-098	031-098
17	PCB1	Time Slot Memory 1 Busy/Idle Parity Error	4WB4	014-098	031-098
18	PCB2	Time Slot Memory 2 Busy/Idle Parity Error	4WB4	014-098	031-098
19	PCB3	Time Slot Memory 3 Busy/Idle Parity Error	4WB4	014-098	031-098
20	BM00PE	Buffer Memory 0 Output Parity Error	4WB4	014-098	031-098
21	BM10PE	Buffer Memory 1 Output Parity Error	4WB4	014-098	031-098
22	BM20PE	Buffer Memory 2 Output Parity Error	4WB4	014-098	031-098
23	BM30PE	Buffer Memory 3 Output Parity Error	4WB4	014-098	031-098

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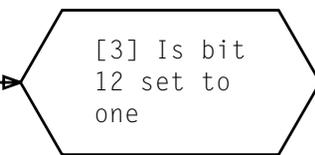
TABLE M PSC CIRCUIT PACK (D3U) LOCATIONS			
CIRCUIT PACK		LOCATION (Note)	
PSC circuit packs*	D3U Type: 4WB3	014-016 (PSC Number 00) 014-024 (PSC Number 01) 014-032 (PSC Number 02) 014-040 (PSC Number 03)	014-156 (PSC Number 08) 014-164 (PSC Number 09) 014-172 (PSC Number 10) 014-180 (PSC Number 11)
Note: Refer to Header Data for appropriate PSC Number * These circuit packs should be replaced one at a time until the trouble is cleared.			

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[1] Locate AC1CSC register [Figure 1] and determine state of bit positions 6-12

[2] Determine ACTIVE CC from status of bit 6 (CCACT), (if 0, CC 0 is active; if set to one, CC 1 is active)



[4] Contact Technical Assistance Center. Active CC is sending and receiving on bus 0 and 1. The standby CC is receiving on both buses.

[5] Use TABLE A and B to determine bus and CC status (SIMPLEXED or or DUPLEXED)

Page 2

BIT 8 (DIV)	BIT 7 (TCC)	CC STATUS
0	0	Duplex CC
1	0	Simplex CC
1	1	

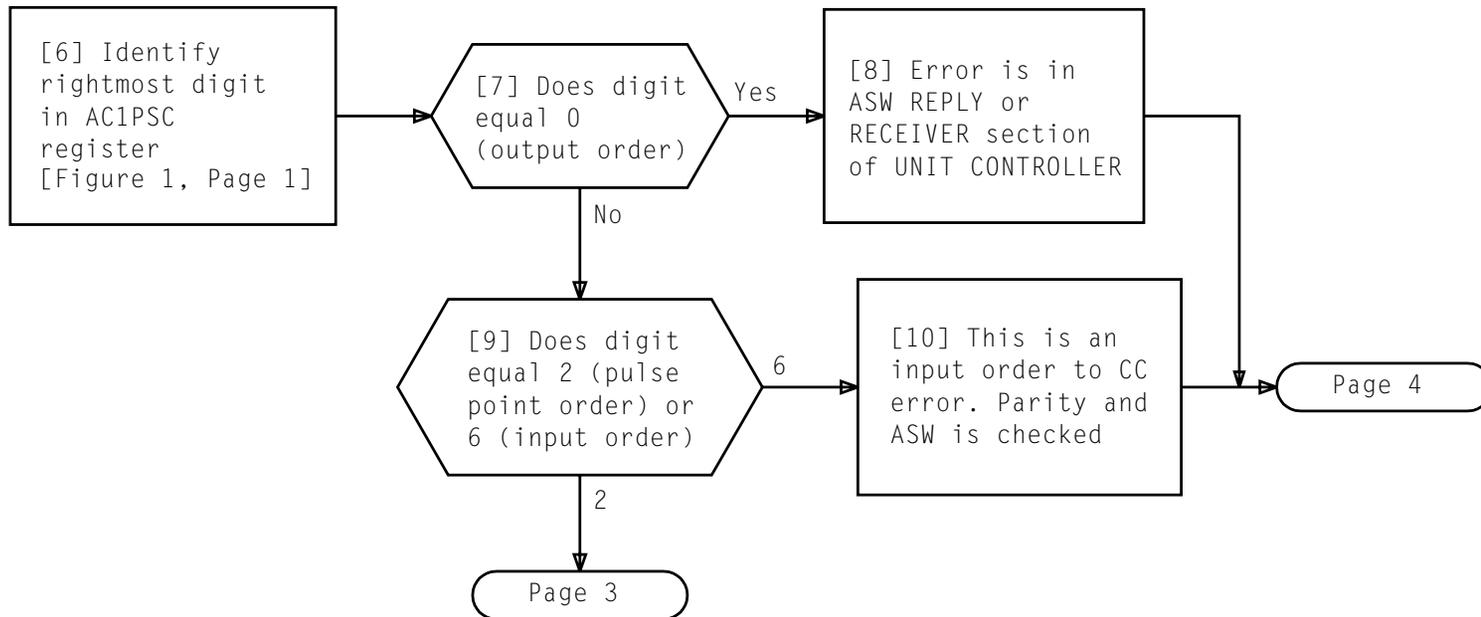
F-LEVEL					
AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASF(H)	AC1ASF(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1LR	
AC1PSQ	AC1ULR	AC1PES	ST1PES	ST1ER	ST1PRM
ST1PRL	ST1PSC	AC1RPO	AC1RPI	ST1RPO	ST1RPI
ST1CSC	ST1INH	PU1RFLC00	PU1RFLC01	PU1RFLC02	PU1RFLC03
PU1RFLC04	PU1RFLC05	PU1RFLC06	PU1RFLC07		
PU1RFLC00		CONTROLLER 0 PULSE POINT REPLY			
01		1 " " "			
02		0 STATUS REGISTER			
03		1 " "			
04		0 ERROR SOURCE REGISTER			
05		1 " " "			
06		FAIL TEST			
07		FAIL DATA			
AC1 - ACTIVE CC REGISTER					
ST1 - STANDBY CC REGISTER					

BIT VALUE				ACTIVE CC		STANDBY CC	
PUBR 12	PUBT 11	PUBA 10	PUBO 09	ENABLE/ WRITE	REPLY (RECEIVE)	ENABLE/ WRITE	REPLY (RECEIVE)
0	0	0	0	0	0	1	1
0	0	1	0	1	1	0	0
0	1	0	0	0	0	X	0
0	1	1	0	1	1	X	1
0	0	0	1	0&1	0	X	1
0	0	1	1	0&1	1	X	0
0	1	0	1	0&1	0	X	0
0	1	1	1	0&1	1	X	1
1	DC	DC	DC	0&1	0&1	X	0&1

X = Idle, bus receives only. DC = Don't care

Figure 1 - CC Register Layout

ANALYZE F-LEVEL INTERRUPT, (CC) REGISTER ANALYSIS



[11] Locate AC1LPI register address instruction in PR Listing [Figure 1, Page 1] [DLP-509]

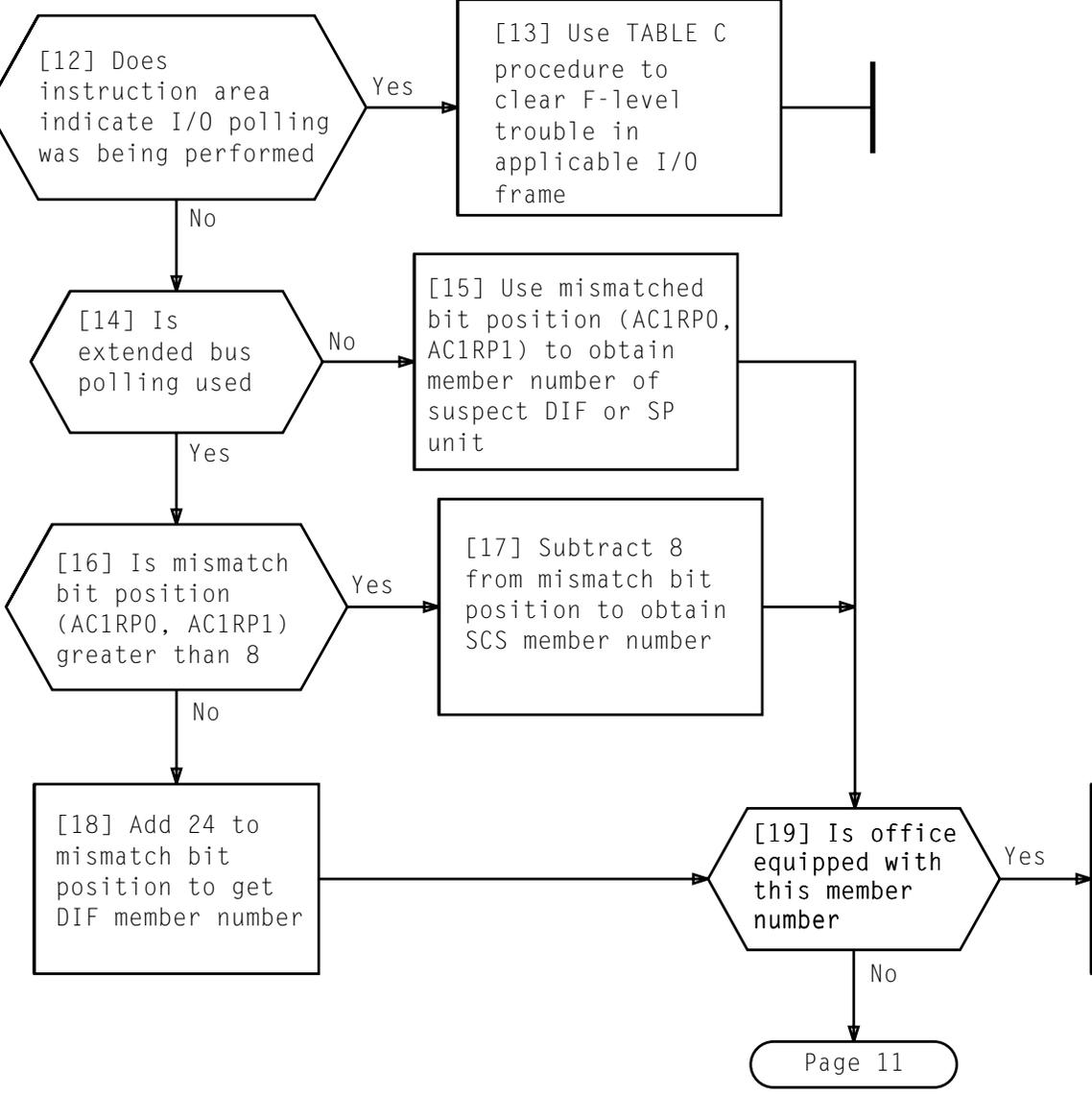
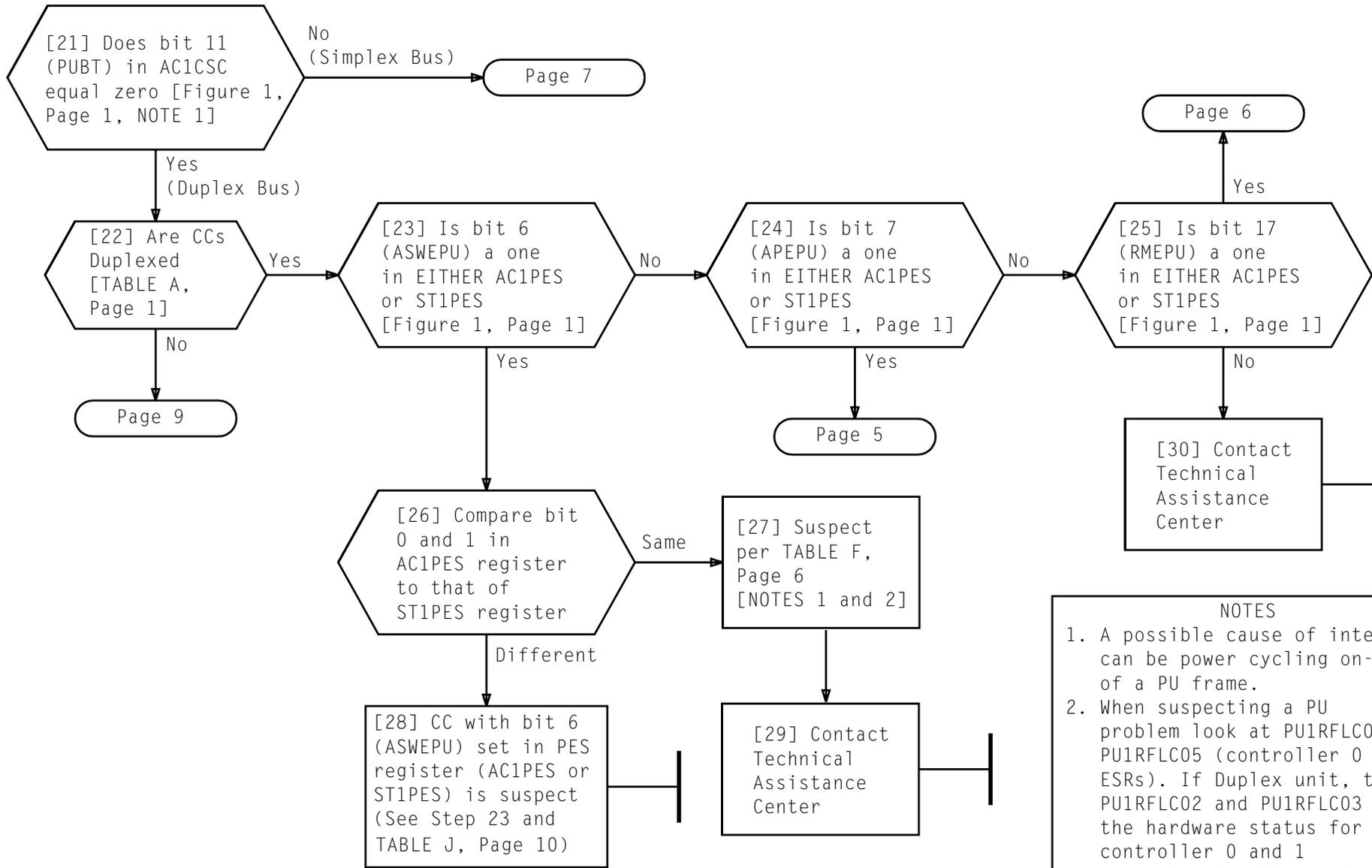


TABLE C	
I/O FRAME	PROCEDURE
J5A006A	TAP-166
J5A006C	TAP-160
J5A006D	TAP-161

TABLE D	
FRAME	DOCUMENTATION
SP1	234-151-031
SP2	234-151-032
DIF	234-151-055
SCS	234-151-077

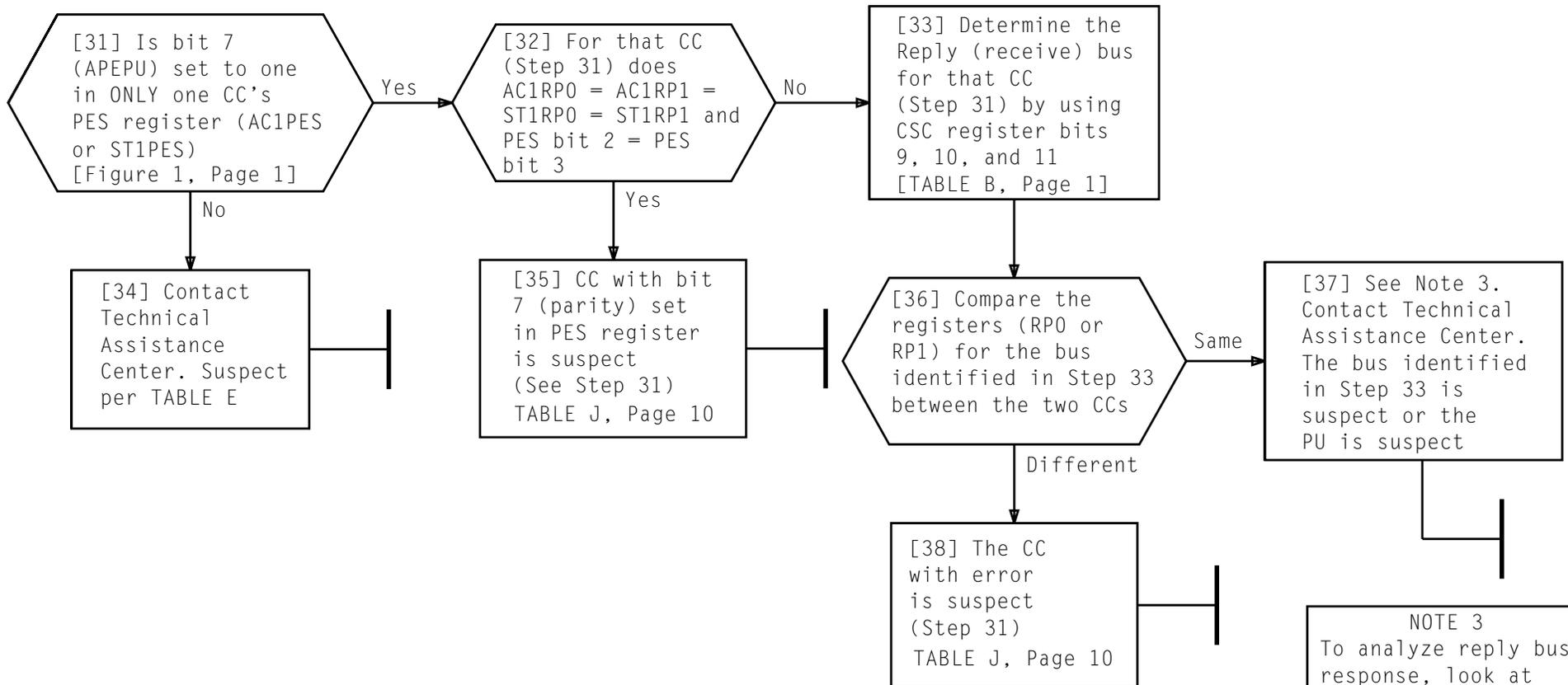
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NOTES

1. A possible cause of interrupt can be power cycling on-off of a PU frame.
2. When suspecting a PU problem look at PU1RFLC04 and PU1RFLC05 (controller 0 and 1 ESRs). If Duplex unit, the PU1RFLC02 and PU1RFLC03 are the hardware status for controller 0 and 1 respectively. [See TABLES G, H, and I on Page 9]

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NOTE 3
 To analyze reply bus response, look at PUB SDs and Unit SDs for hardware in this category. Figure out the layout and connections for that unit to bus. From difference between responses, determine what cable, cable driver, or piece of controller is suspect.

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TABLE E - PES REGISTER [NOTE 3]		
BIT 3 - AP1PU	BIT 2 - APOPU	SUSPECT
0	0	Check BUS Reply Registers 24 bits, if even parity then error condition.
0	1	If even parity on Bus Reply Register + Parity then error condition.
1	0	
1	1	Check Bus Reply Register 24 bits, if odd parity then error condition.

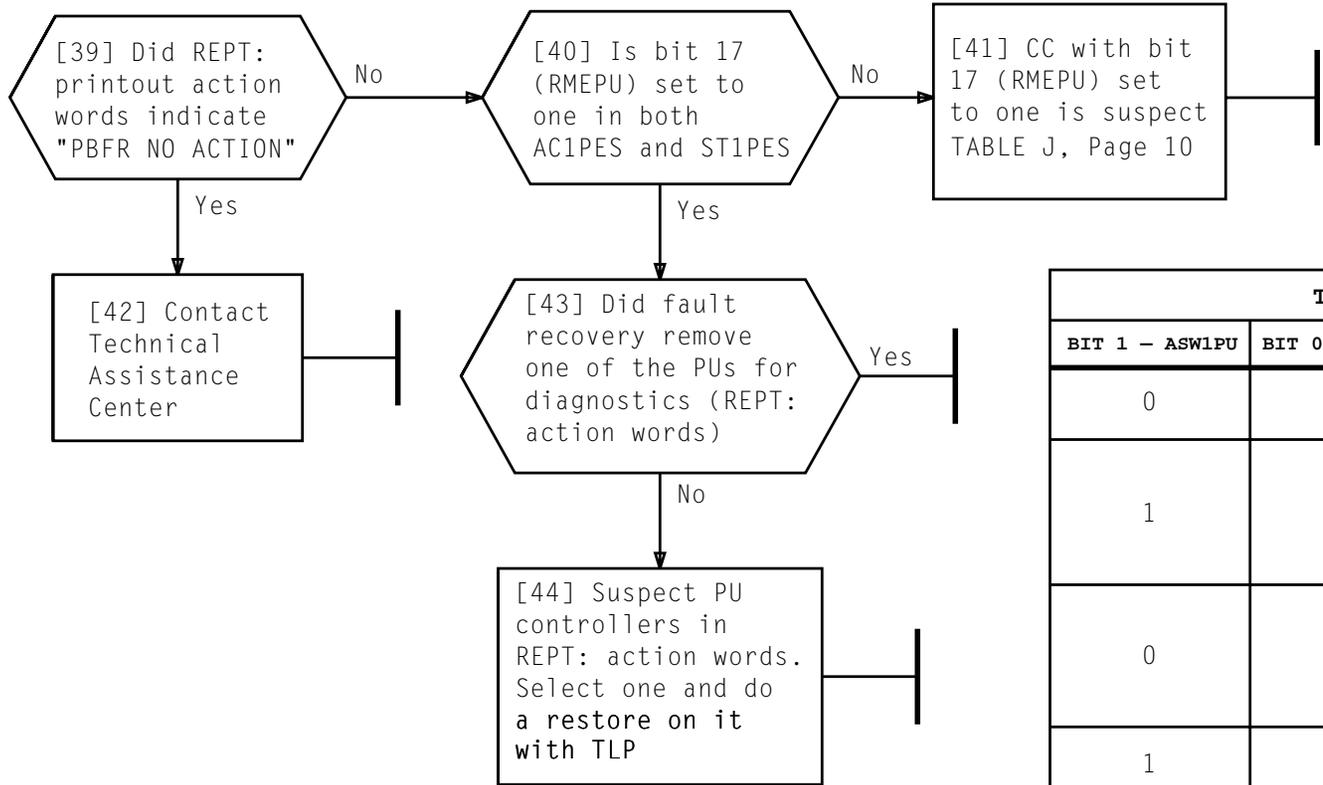
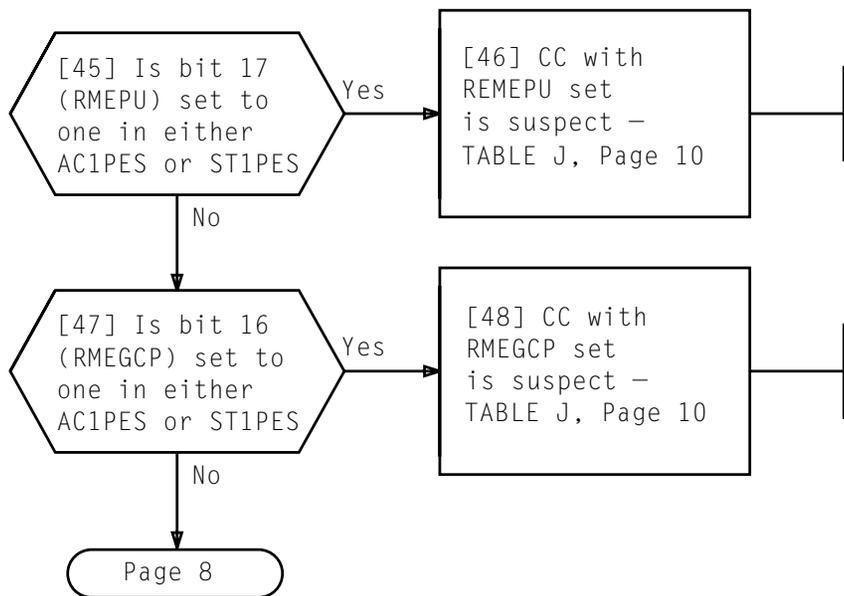
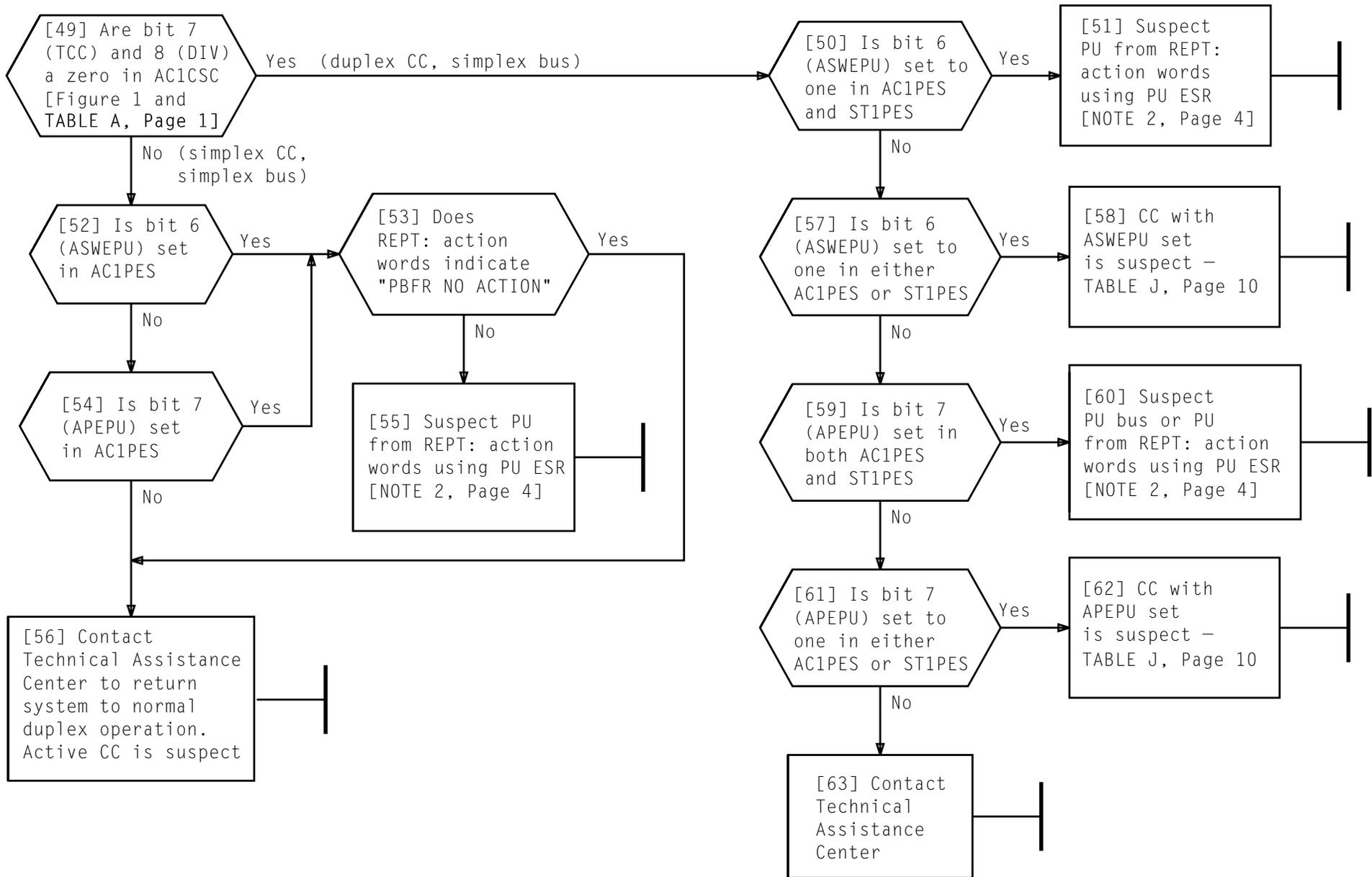
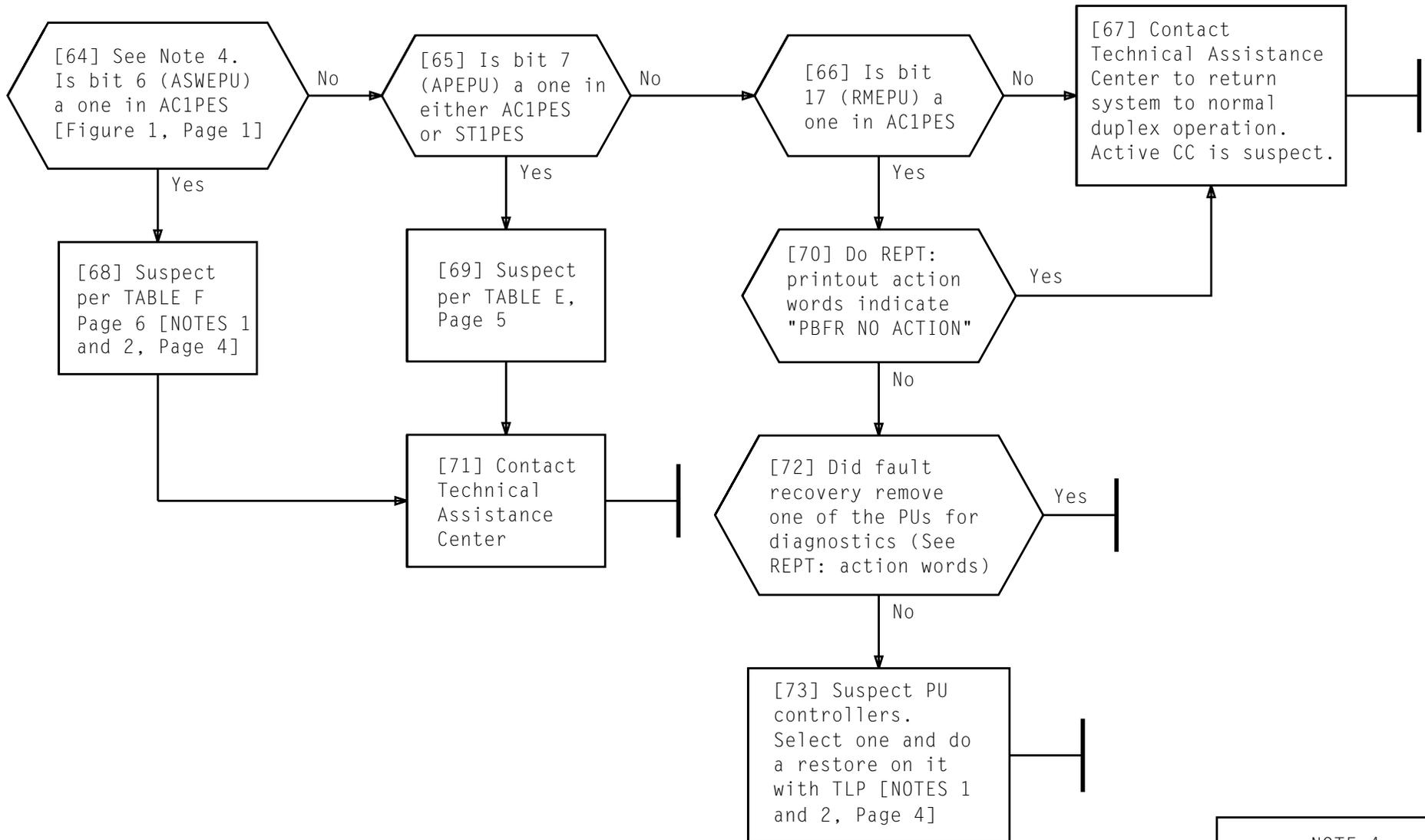


TABLE F - PES REGISTER		
BIT 1 - ASW1PU	BIT 0 - ASW0PU	SUSPECT
0	0	PU PROBLEM, look at PU ESR. Possible software problem
1	0	BUS 0 or IPUB 0 Controller suspect. Determine which controller from hardware and software STATUS WORDS
0	1	BUS 1 or IPUB 1 Controller suspect. Determine which controller from hardware and software STATUS WORDS
1	1	CC with Bit 6 (ASW6PU) set to one is suspect (AC1PES or ST1PES). Suspect packs in that CC using TABLE J, Page 10 packs





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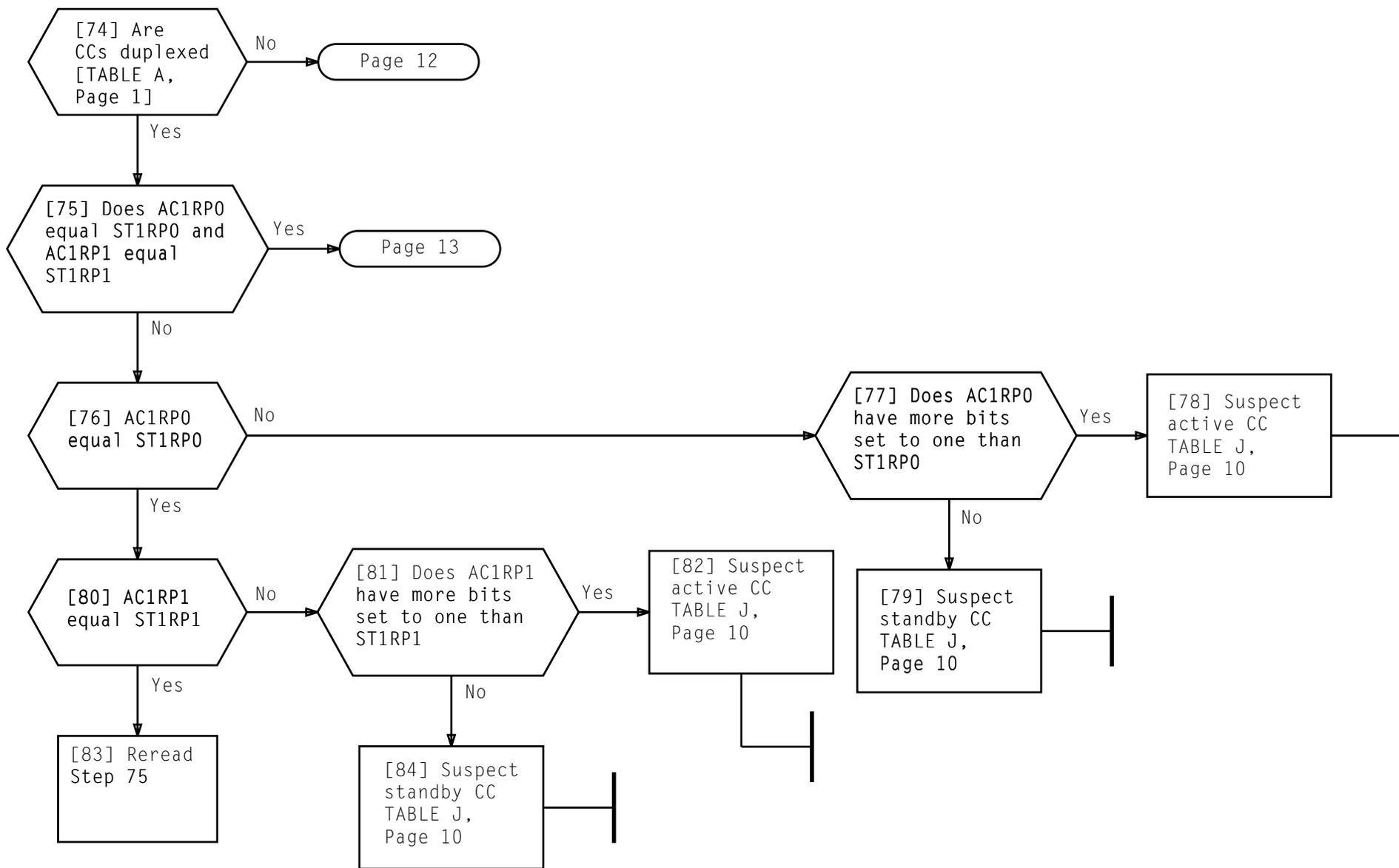
NOTE 4 This page is for simplex CC and duplex bus	
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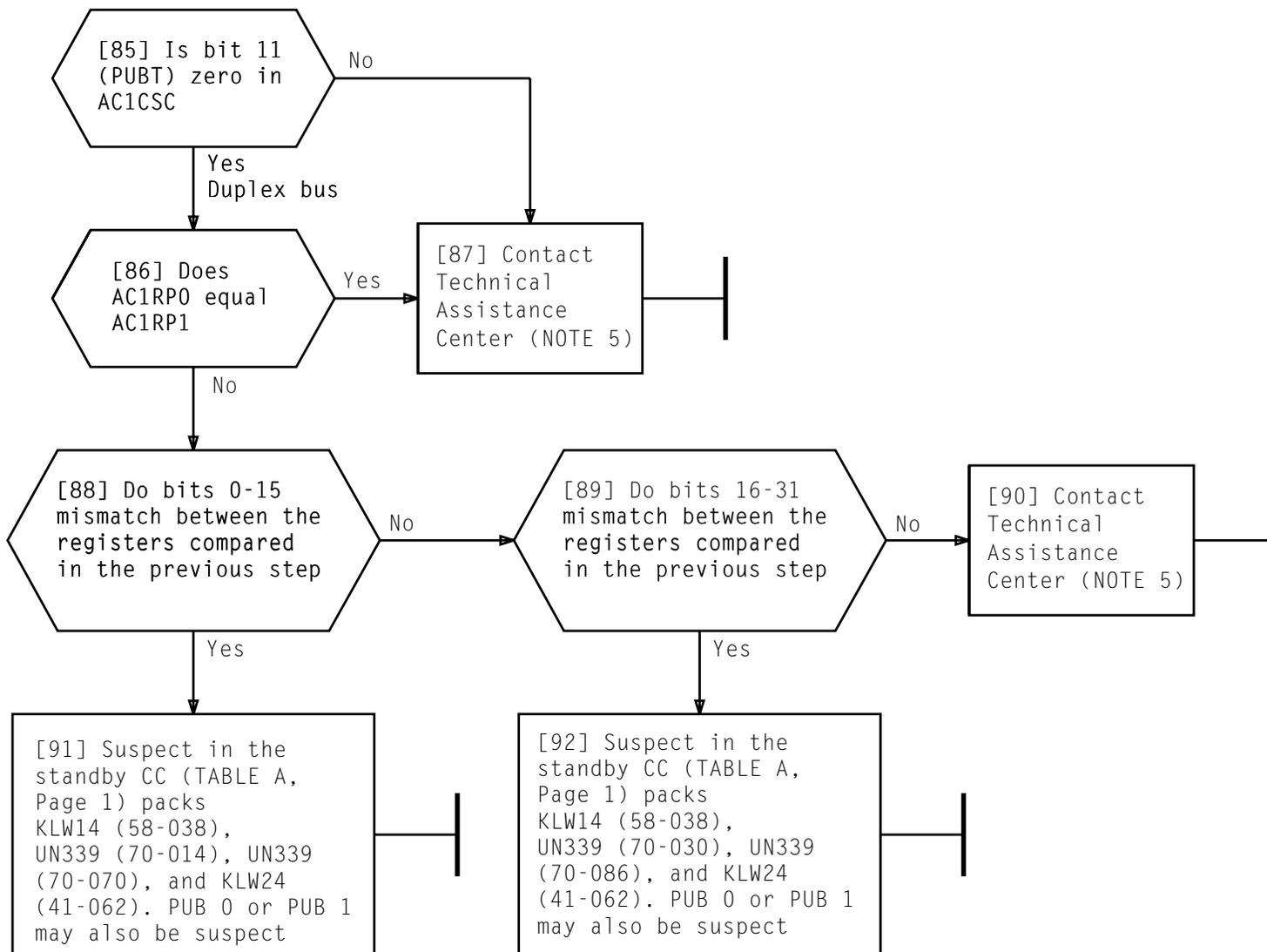
TABLE G - E-REGISTER LAYOUTS												
BITS →	21	20	19	18	17	16	15	14	13	12	11	10
MCC	0	0	0	0	1	1	1	1	0	1	1	0
SP/DIF	0	0	0	1	0	Member number				MTX		
SCLK	0	0	0	1	1	Member number						
TMS	0	0	1	0	0					MEM NO		
TSI	0	0	1	0	1	Member number				SPC		
TGR	0	0	1	1	0	Member number						
IOUS	0	0	1	1	1	Member number			IOUC			
EST	0	1	0	0	1	Member number						
SCS	0	1	0	1	1	Member number			SCU NUMBER			
BITS →	21	20	19	18	17	16	15	14	13	12	11	10

TABLE H - I/O F LEVELS	
REGISTER	DESCRIPTION
PUIRFLC00	PLSRPLY (MA PULSE REPLY)
PUIRFLC01	USOFT-STAT (UNIT SOFT STATUS)
PUIRFLC02	UHARD-STAT (UNIT HARD STATUS)
PUIRFLC03	SU-STAT (SUBUNIT STATUS)
PUIRFLC04	ESR (ERROR SUMMARY)
PUIRFLC05	ACTION (RECOVERY ACTION)
PUIRFLC06	CSR (CHANNEL STATUS REGISTER)
PUIRFLC07	TSTRSLT (TEST RESULT FLAGS)

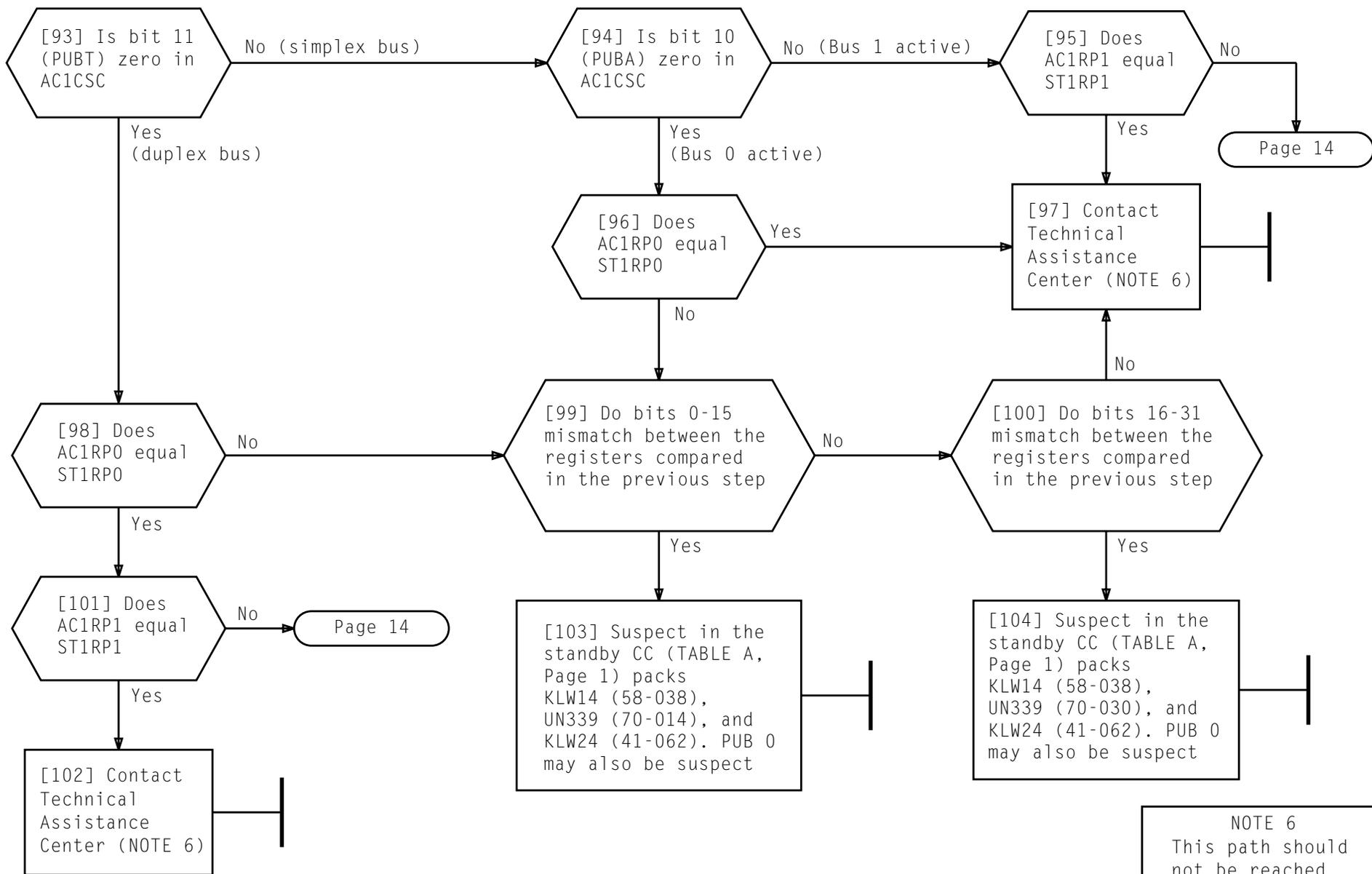
TABLE I - CRITICAL REGISTERS		
UNIT TYPE	PUIRFLC04 (CONTR 0)	PUIRFLC05 (CONTR1)
DIF	CESR	CESR
EST	CESR1	CESR1
TMS	TG4ESR+0	TG4ESR+0
TSI	ASESR (ESR0)	ASESR (ESR0)
SP	SP4ESR1	SP4ESR1
SCLK	HESR	HESR
CCIS	ESR	ESR
SCS	CESR	CESR

TABLE J - SUSPECT PACKS IN SUSPECT CC	
PACK	LOCATION
KLW14	58-038
UN339	DLP-531
KLW24	41-062

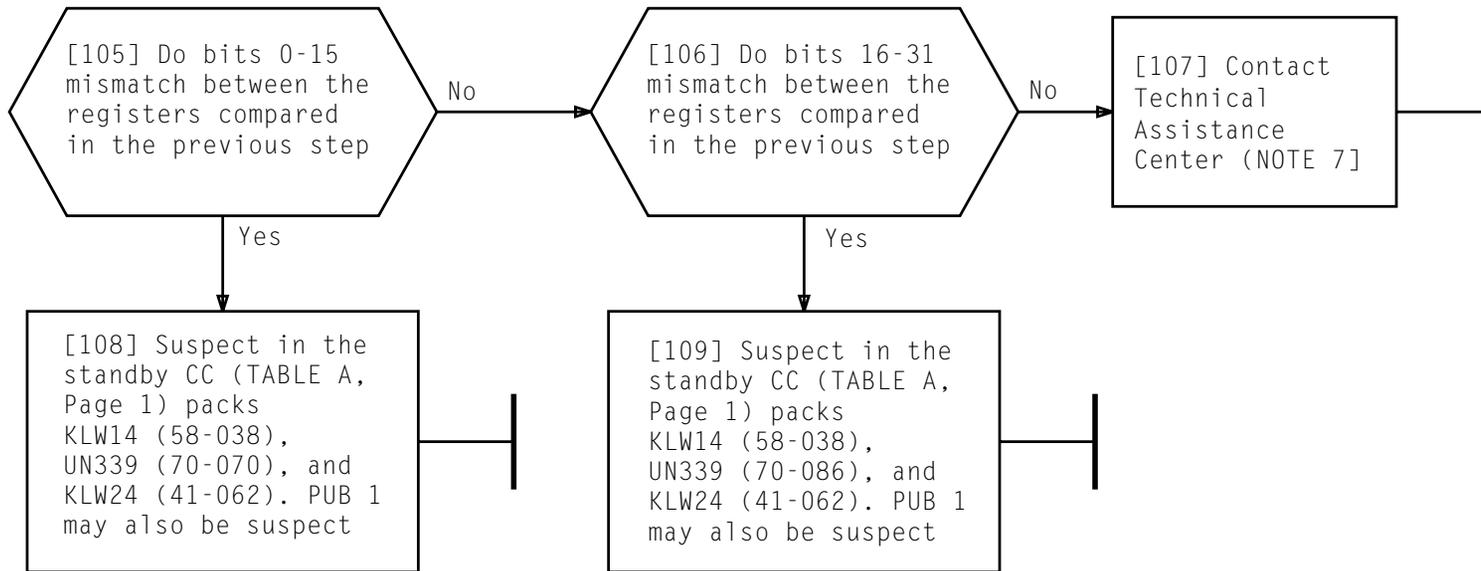




NOTE 5	
This path should not be reached	
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NOTE 6	
This path should not be reached	
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NOTE 7	
This path should not be reached	
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This data formulates the strategy to be used when multiple bits are set in bit positions 4 through 14 of TSI controller error source registers (ESR+1)

1. Use ERAP data and attempt to locate a repeating pattern or common unit
 2. Check prior printouts for audit activities that may have been involved with an interrupt
 3. Investigate clock problems external to TSI frame
 4. Use Figure 1 to check bits 4-7 (implicate cable/bus as suspect) in PERIPHERAL SYSTEM DATA WORD 1
 5. Analyze F-level Registers
 6. Check SDs and attempt to locate a common circuit pack
- End of procedure

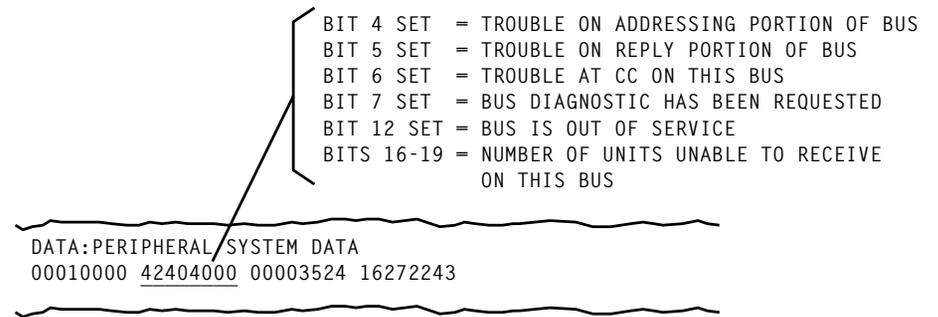


Figure 1 - Cable/Bus Implication

CAUTION: Maintenance on a simplexed unit is complicated by the system's inability to reconfigure and could cause a directed phase one.

The following stratagems are provided as general guidelines for analyzing faults in a simplexed TSI.

1. Check to see if maintenance activities may have caused problem (that is, powering down or up of mate unit)
 2. Analyze bits 4, 5, 6 in CREG 3 register as one bit (starting with bit 4) and try to resolve error using duplex path
 3. Analyze bits 7, 8, 12 (starting with bit 12) as in Step 2 except that resolution internal or external to the unit cannot be made (suspect clock problems in attached unit, power sequencer, etc)
 4. Resolution of a TSWF (bit 11) to the determination of which side contains the error should not be attempted
 5. Try to determine why unit is simplexed and if error is related to simplexed condition
 6. Use ERAP data to determine if a pattern exists
 7. Use TABLE A (TSI-A), Page 2 or TABLE B (TSI-B), page 3 for additional information (bits set to one in CREG 3)
- End of procedure

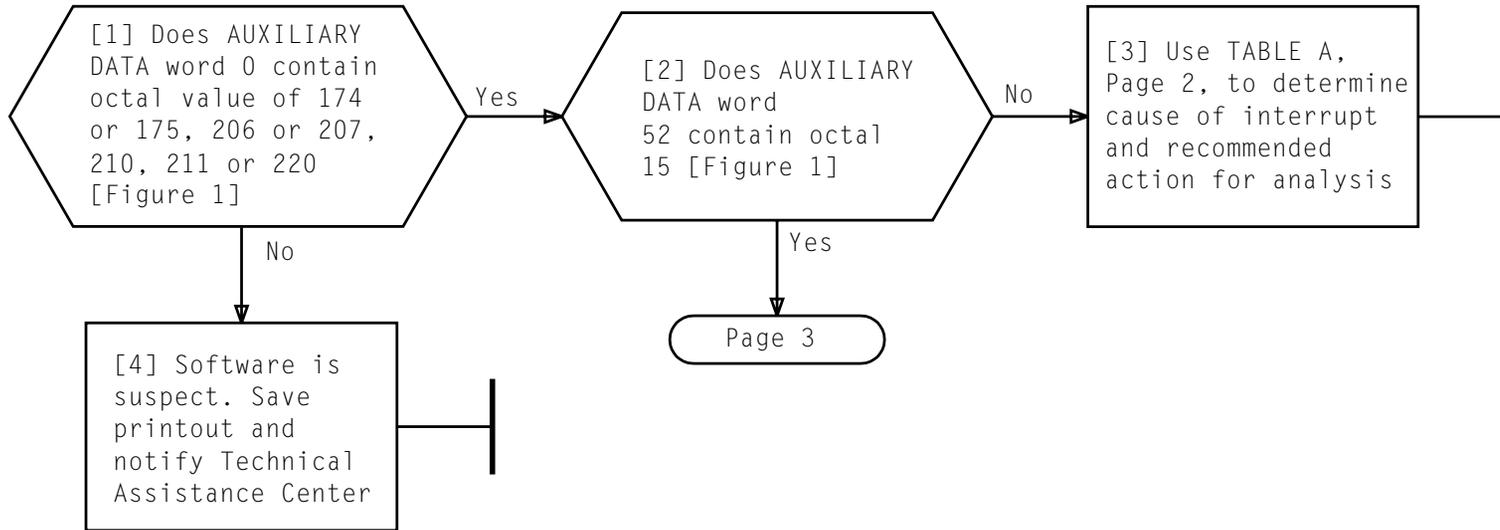
TABLE A
TSI A BIT IDENTIFICATION APUF, CREG 3)

BIT	NAME	LEAD(S)	SD	FS/SYMBOL	IMPLICATION	BIT	NAME	LEAD(S)	SD	FS/SYMBOL	IMPLICATION
0	CE	CCESTRCO	4A023	4/1	Internal clock error. Suspect clock circuit	9	—	—	—	—	Not used
1	TSSC	ERESTSCO	4A023	5/3	Time slot sequence check. Suspect time slot counter circuit	10	TRPF	0EPL00 7EPL00	4A024	20/1 20/8	Transmission parity failure
2	TSCMM	METRCMMO	4A023	4/1	Time slot counter mismatch	11	TSWF	0EBTO 1EBTO 2EBTO 3EBTO 4EBTO 5EBTO 6EBTO	4A024	25/5 25/5 25/6 25/6 25/7 25/7 25/8	Transmit seems well failure
3	CMM	ETRCMMO	4A023	4/1	Clock mismatch. Suspect clock match circuit or mate controller	12	RSWF	0ERBO 6ERBO	4A024	1/1 1/7	Receive seems well failure. Suspect VIU/ DTU failure or receive box failure
4	RTMP	0EPRRO 7EPRRO	4A024	11/1 11/8	Receive time slot memory (TSM) parity failure	13	RMM	0ECOLO 4ECOLO	4A024	6/1 6/5	Receive mismatch. Suspect: 1. decorrelator or buffer A 2. mismatch circuit 3. mate controller
5	TTMP	0ERTPO 7ERTPO	4A024	17/1 17/8	Transmit TSM parity failure	14	TMM	0ECRO 4ECRO	4A024	24/1 24/5	Transmit mismatch. Suspect: 1. decorrelate circuit 2. match circuit 3. mate controller
6	BIMP	ERMPO	4A024	23/5	Busy idle map memory (BIMM) parity failure	15	SSWF	ECLK0	4A023	9/1	Suspect clock circuit
7	BMAPF	0ERPHAO 1ERPHAO 2ERPHAO 3ERPHAO 4ERPHAO 5ERPHAO 6ERPHAO 7ERPHAO	4A024	5/1 5/1 5/2 5/2 5/4 5/4 5/5 5/5	Buffer memory A parity failure						
8	BMBPF	0ERSPO 7ERSPO	4A024	8/1 8/8	Buffer memory B parity failure						

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TABLE B
TSI B BIT IDENTIFICATION (APUF, CREG 3)

BIT	NAME	LEAD(S)	SD	FS/SYMBOL	IMPLICATION	BIT	NAME	LEAD(S)	SD	FS/SYMBOL	IMPLICATION
0	CE	(Internal)	4A085	16/1	Twisted Ring Counter Error.	9	—	—	—	—	Not Used.
1	TSSC	ETSCPTY0	4A085	17/1	Time slot sequence check. Suspect time slot counter circuit.	10	TRPF	ETRPFO	4A084	5/1-4	Leading one detector parity failure.
2	—	—	—	—	Not Used	11	TSWF	ETSWFO	4A084	14/1-8	Transmit seems well failure.
3	TRCMM	TTRCOM TTRCIM (From mate)	4A085	16/1	Twisted ring counter mismatch. Suspect clock match circuit or mate controller.	12	RSWF	ERSWO	4A084	11/1,3, 5,6,9, 11,13,15	Receive seems well failure. Suspect VIU/DTU failure or receive box failure.
4	RTSMPF	ERMEMPO	4A084	2/1-8	Receive time slot memory (TSM) parity failure.	13	RMM	EBMMTCHO	4A084	2/1-8	Receive mismatch. Suspect: 1. Decorrelator buffer A and same port receiver. 2. Mismatch circuit and receiver. 3. Mate controller.
5	TTSMPF	ETMEMPO	4A084	6/1-8	Transmit TSM parity failure.	14	TMM	ETMMO	4A084	8/1	Transmit mismatch. Suspect: 1. Decorrelator circuit. 2. Match circuit. 3. Mate controller.
6	BIMMF	EBIMMO	4A084	7/1	Busy/Idle map memory parity failure.	15	—	—	—	—	Not Used
7	BMAPF	ODSBMAO 7DSBMAO	4A084	12/1-8	Buffer memory A parity failure.						
8	BMBPF	ERBMPO	4A084	2/1-8	Buffer memory B parity failure.						



WORD 0 WORD 52

DATA: AUXILIARY DATA					
00000220	40032163	00001336	00000163	00000336	04610261
00000001	00000000	00070400	00000000	00002261	02041110
00000000	00000012	00000004	03011012	03011004	02100004
00000070	00000070	40404064	40404040	40404040	00000000
40404064	40404040	40404040	00000000	00000000	60006135
00000000	00001012	00001004	02001012	02001004	00000000
00000000	00000000	00000000	63400000	02000000	00000000
23306015	27326531	33343133	77377535	23306015	27326531
33343133	77377535	00000000	00000046	00000015	00000004
43777777	10637477	12637777	00001246	00001002	00001200
00000000	00000000	00000000	00000000	00000000	00000000
00000000	00000000				
06/23/96	17:11:01				
#750					

Figure 1 - AUXILIARY DATA Registers

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TABLE A – PATH RESULTS		
AUX DATA WORD 52 VALUE	ERROR DESCRIPTION	RECOMMENDED ACTION
0	T-TSI routing failure	Run diagnostics on suspect TSI – should result in STF; if not, notify Technical Assistance Center
1	TTSI no data	Suspect Leading One Detector or TTSM register associated with the failing level
3	T-TSI data mismatch	Contact Technical Assistance Center
5	TMS mismatch failure	
6	TMS software	
7	R-TSI duplex failure	
12	R-TSI data mismatch	
13	R-TSI software error	
14	R-TSI network mismatch	
	R-XTSI routing mismatch	Run diagnostic on suspect unit
4	TMS access failure	Run diagnostic on suspect unit; should result in STF. This TRPF is first indication that a unit has stopped working
10	R-TSI access failure	
11	R-TSI routing failure	Same as for value 0 above
16	TMS duplex failure	Contact Technical Assistance Center

**ANALYZE TNFR F-LEVEL INTERRUPT TRPF FAILURE,
TIME-SLOT INTERCHANGE/TIME-MULTIPLEXED SWITCH**

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[5] Use word 54 for TTSI. If the most significant digit is 4 or 5, the frame is XTSI; else, it is a regular TSI

[6] Use word 56 for XTSI. If the most significant digit is 4 or 5, the frame is XTSI; else, it is a regular TSI

See NOTE 1.

[7] Use AUXILIARY DATA words 5, 11, 17, 29 [Figure 2, page 4] and TABLE B, to determine the TRPF path data

[8] Use TABLE C, page 4 and AUXILIARY DATA word 51 to identify controllers involved in TRPF path

[9] Use ISDs, SDs, or ERAP to isolate TRPF and identify suspect circuit packs

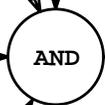


TABLE B TRPF PATH DATA							
AUX DATA REGISTER	HARDWARE PATH						
05 T-TSI	CHANNEL	SPU	LEVEL	SPC	MEMN	TERMINATING SWITCH LEVEL	
	Bits 0-6		Bits 9-11	Bit 12	Bits 13-18	Bits 21-23	ISD-130
T-XTSI	Bits 0-9	Bits 10	Bits 12-14	Bit 15	Bits 16-21		
11 TMS ST2	B-LINK		A-LINK		SWITCH	TMSP	
	Bits 0-3		Bits 6-9		Bits 12-15	Bits 19,18	
17 TMS ST1	Bit layout is same as ST2SW						
29 R-TSI	CHANNEL	SPU	LEVEL	SPC	MEMN	ORIGINATING SWITCH LEVEL	
	Bits 0-6		Bits 9-11	Bit 12	Bits 13-18	Bits 21-23	ISD-131
R-XTSI	Bits 0-9	Bits 10	Bits 12-14	Bit 15	Bits 16-21		

NOTE 1 ISD applies to TSI-B only	
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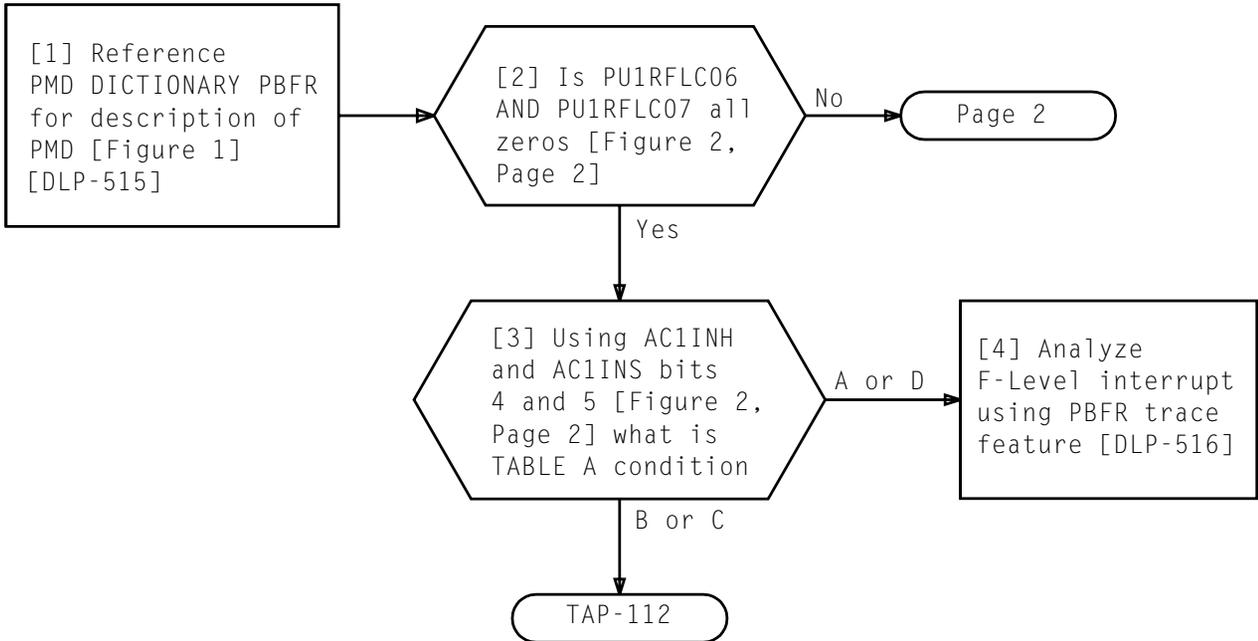
A 14 REPT: F-LEVEL @1420/4313 MFNUM=00135364 MICON=00000020
LV=0040 D0=00000000 D1=04000000 D2=00000037 D3=00000003
DATA: INTERRUPT SOURCE DATA
00002640 00000000 01402000 00000020 00000020
DATA: FAULT RECOGNITION ISOLATION DATA
00000030 00000000 10000241 00000001 00000014 00000000
DATA: ERROR ANALYSIS STRATEGY DATA
04026344 00000004 00000004 00000030 00000004 00000000
00000000
DATA: AUXILIARY DATA
00000220 40032163 00001336 00000163 00000336 04610261 5
00000001 00000000 00070400 00000000 00002261 02041110 11
00000000 00000012 00000004 03011012 03011004 02100004 17
00000070 00000070 40404064 40404040 40404040 00000000
40404064 40404040 40404040 00000000 00000000 60006135 29
00000000 00001012 00001004 02001012 02001004 00000000
00000000 00000000 00000000 63400000 02000000 00000000
23306015 27326531 33343133 77377535 23306015 27326531
33343133 77377535 00000000 00000046 00000015 00000004
43777777 10637477 12637777 00001246 00001002 00001200
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000
06/23/96 17:11:01 51
#750

```

AUX
DATA
WORDS

Figure 2 - Auxiliary Data Registers

TABLE C AUX DATA 51			
	T-TSI	TMS	R-TSI
BITS SET TO ONE			
CONTR 0	Bit 0	Bit 2	Bit 4
CONTR 1	Bit 1	Bit 3	Bit 5



```

    ERROR ANALYSIS RECENT HISTORY TABLE
    00241030 10401630 00000000 00000000 00000000 00000000
    00000003 00000001 00010000 77777776 00000000 00000001
    30602040 00000000 40001604 00000002 00000003 00000000
    00000000 00000044 00000052 00000004 00000012 00241030
    00402040 00000000 00000000 00000000 00076010 20000201
    00025673 00025673 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 00000000
    00100001 00011702 00000101 00000000 00000000 00000000
    00000000 00000000 03471371 00000000 00000001 00000000
    04000151 00000000 10000252 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 20637777
    12/30/88 02:02:33
    #247
  
```

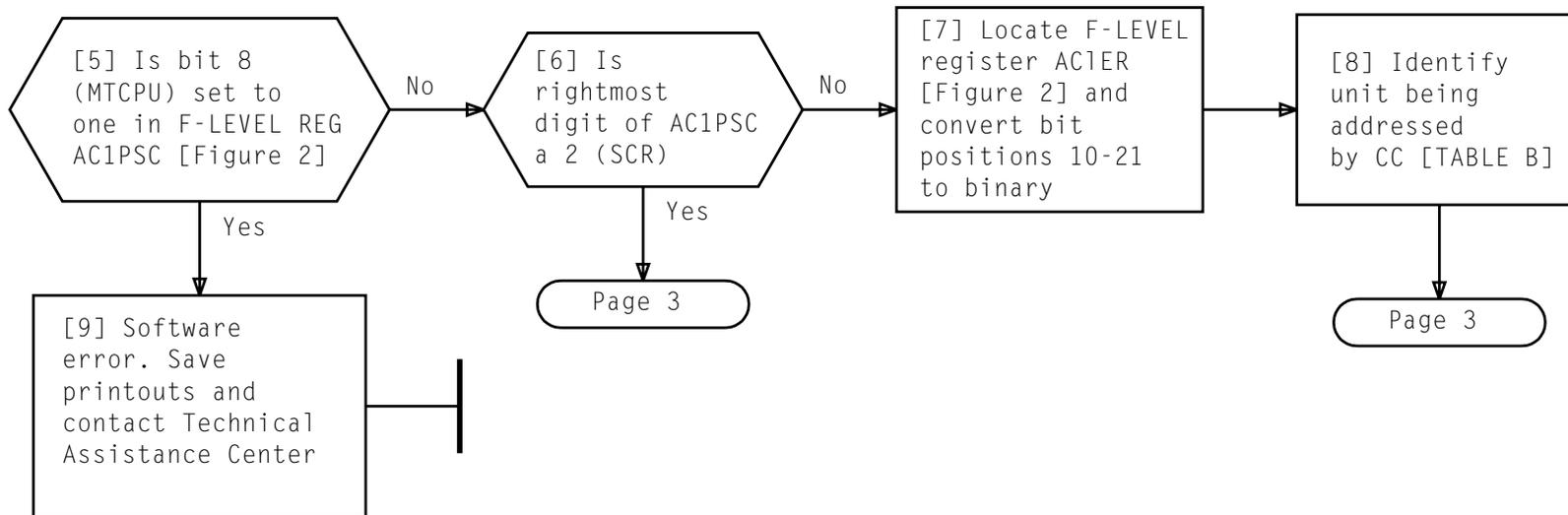
PMD NUMBER

Figure 1 - RCNT Register Printout

TABLE A				
AC1INH		AC1INS		CONDITION
BIT 5 (IPUFS)	BIT 4 (IAPUFS)	BIT 5 (PUFS)	BIT 4 (APUFS)	
DC	0	0	1	A
0	0	1	DC	B
0	1	1	DC	C
1	0	DC	1	D

DC = Don't Care

ANALYZE PBFR F-LEVEL INTERRUPT



DATA: F-LEVEL (FLEV)

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASF(H)	AC1ASF(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1LR	
AC1PSQ	AC1ULR	AC1PES	ST1PES	ST1ER	ST1PRM
ST1PRL	ST1PSC	AC1RPO	AC1RP1	ST1RPO	ST1RP1
ST1CSC	ST1INH	PU1RFLC00	PU1RFLC01	PU1RFLC02	PU1RFLC03
PU1RFLC04	PU1RFLC05	PU1RFLC06	PU1RFLC07		
PU1RFLC00		CONTROLLER	0 PULSE POINT REPLY		
01			1 " " "		
02			0 STATUS REGISTER		
03			1 " " "		
04			0 ERROR SOURCE REGISTER		
05			1 " " "		
06			FAIL TEST		
07			FAIL DATA		

AC1 - ACTIVE CC REGISTER
ST1 - STANDBY CC REGISTER

Figure 2 - CC Register Layout

TABLE B
E-REGISTER LAYOUTS

BITS →	21	20	19	18	17	16	15	14	13	12	11	10
MCC	0	0	0	0	1	1	1	1	0	1	1	0
SP/DIF	0	0	0	1	0	Member number					MTX	
SCLK	0	0	0	1	1	Member number						
TMS	0	0	1	0	0						MEM NO	
TSI	0	0	1	0	1	Member number					SPC	
TGR	0	0	1	1	0	Member number						
IOUS	0	0	1	1	1	Member number				IOUC		
EST	0	1	0	0	1	Member number						
SCS	0	1	0	1	1	Member number				SCU number		
BITS →	21	20	19	18	17	16	15	14	13	12	11	10

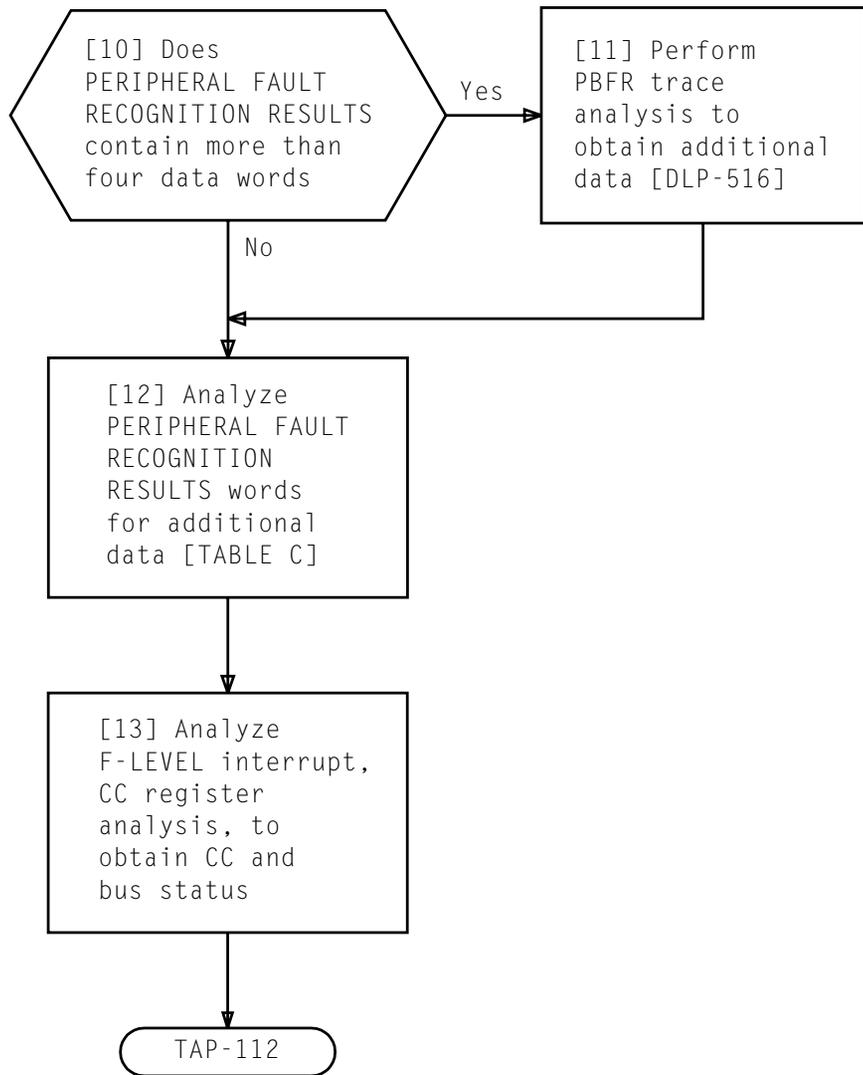


TABLE C PERIPHERAL FAULT RECOGNITION RESULTS			
IDENTIFICATION OF REGISTERS IN RESULTS			
TABLE OF F-LEVEL MESSAGES			
PU4RESULT	PU4UTMNO	PU4FRPMD	PU4FRJRG
PU4RESULT	-----NMLKJIHGFEDCBA		
BIT	0	A = CC0 found faulty	
	1	B = CC1 found faulty	
	2	C = Controller 0 found faulty	
	3	D = Controller 1 found faulty	
	4	E = PU bus 0 found faulty	
	5	F = PU bus 1 found faulty	
	6	G = PU bus 0 at unit found faulty	
	7	H = PU bus 1 at unit found faulty	
	8	I = Faulty unit or subunit to be removed and diagnosed	
	9	J = Faulty unit or subunit to be removed	
	10	K = Fault recognition was unable to find the fault	
	11	L = Fault recognition found that a software error caused the F-level	
	12	M = Fault recognition found that a transient caused the F-level	
	13	N = Signal processor matrix found faulty	
PU4UTMNO	DDDDDDCCCCCBBAAAAAA--		
BIT	2-8	A = Submember found faulty (if any)	
	9	B = Set if submember found faulty	
	10-16	C = Member number found faulty	
	17-23	D = Unit type found faulty	
PU4FRPMD	--CCCCCBBBBBBBAAAAAA		
BIT	0-7	A = Point of Maximum Definition MACRO number relative to an FR program	
	8-14	B = Fault recognition decision code	
	15-21	C = Error analysis action code	
PU4FRJRG = FR program address where error was located			

ANALYZE PBFR F-LEVEL INTERRUPT

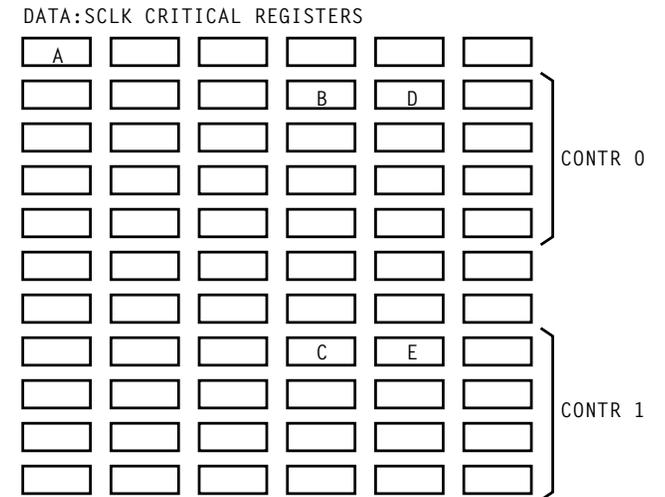
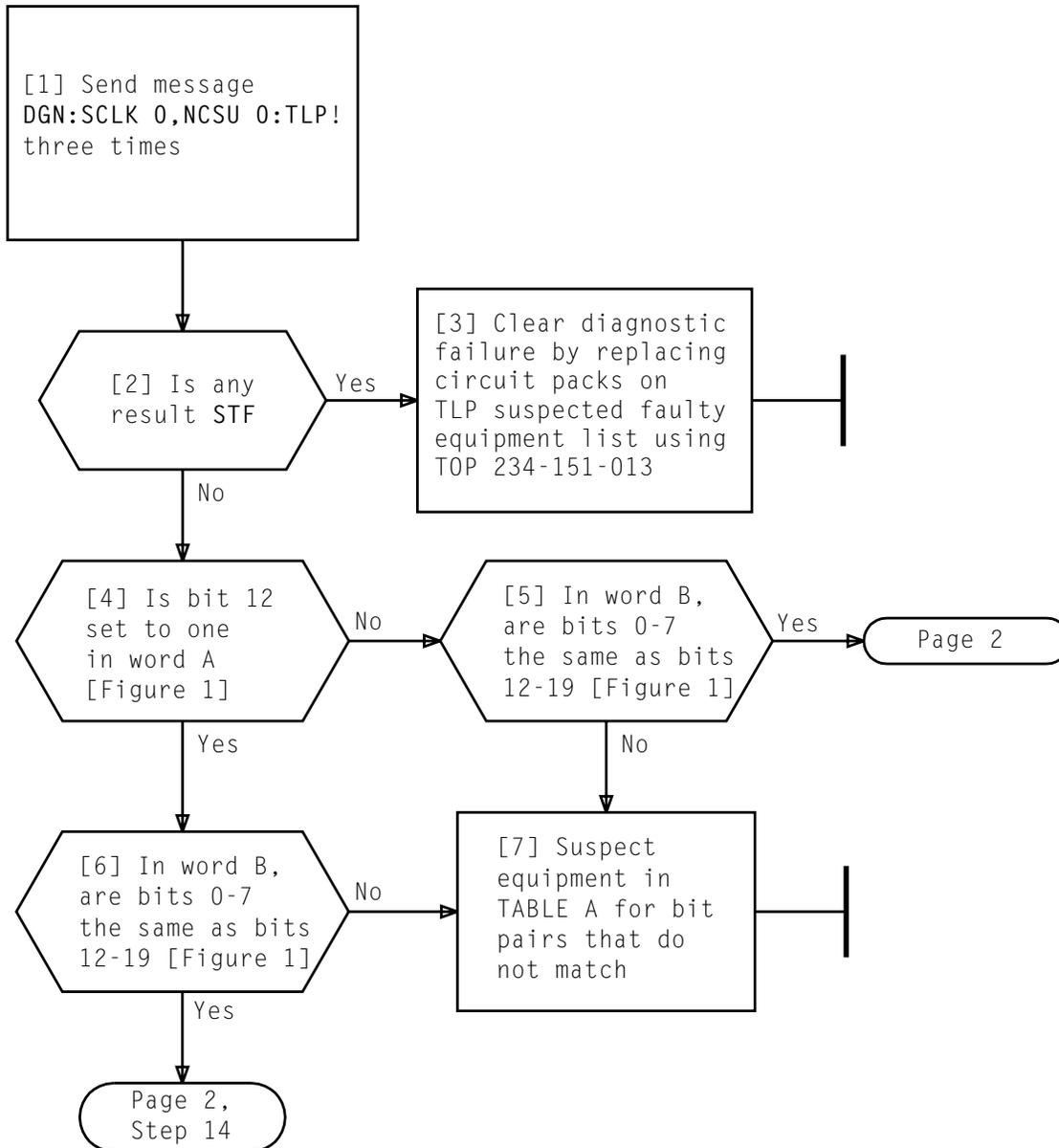
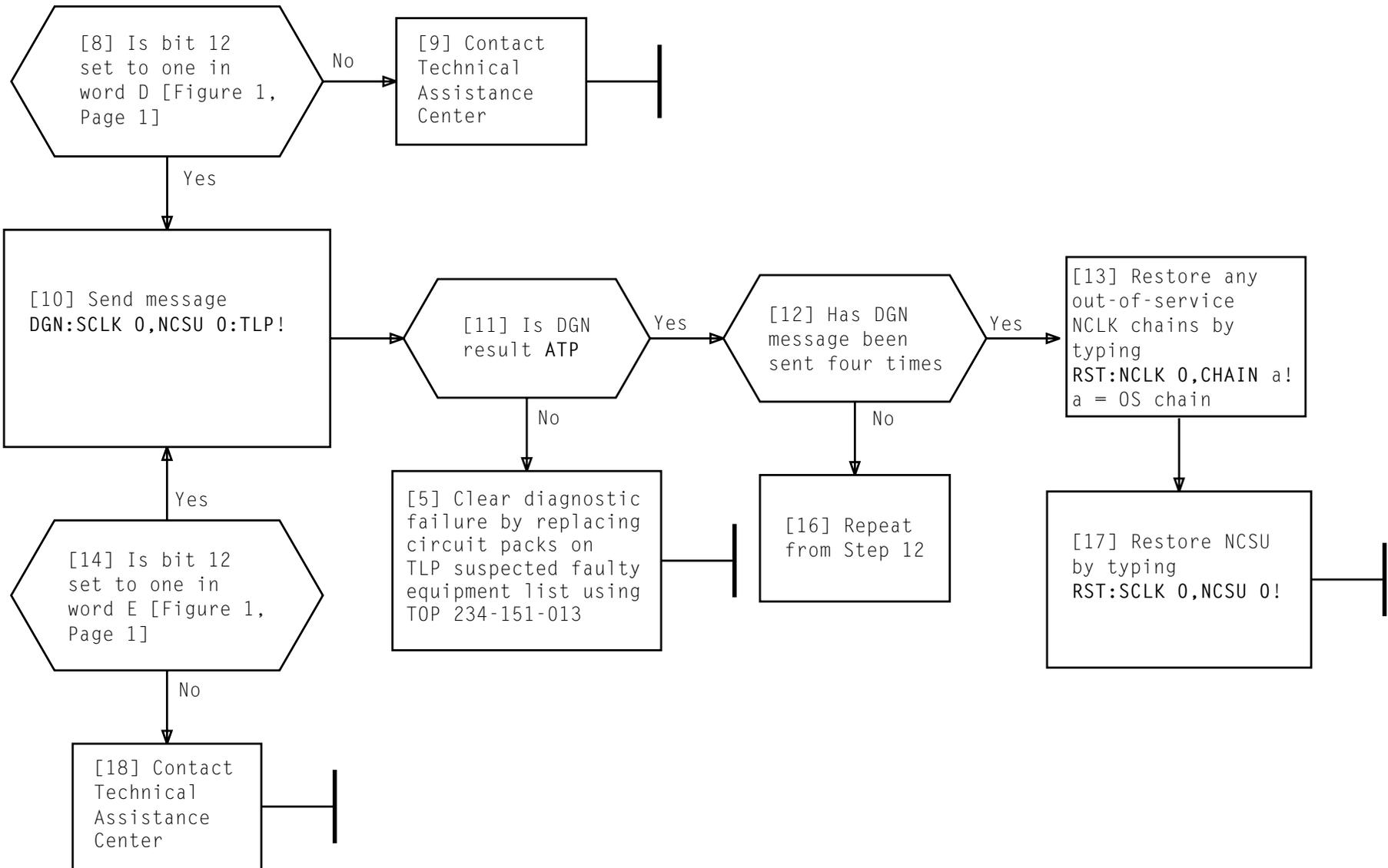


Figure 1 - Part of Base Level Printout

TABLE A BASE 0 ESR (WORD B)		
BIT PAIR	BIT DESCRIPTION	SUSPECT EQUIPMENT
0,12	Oscillator out of range	Suspect NCLK oscillator indicated. Clear phase error using TOP 234-151-013. If more than one oscillator indicated, suspect lower numbered oscillator first
1,13	Oscillator 0	
2,14	Oscillator 1	
2,15	Oscillator 2	
4,16	Oscillator 3	Office timing reference outage
5,17	BSRF outage	
6,18	DS1A outage	
7,19	DS1B outage	

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- [1] Using Figure 1, identify suspect controller from TEXT HEADER
- [2] Using Figure 1, obtain Point of Maximum Definition (PMD) from DATA:ERROR ANALYSIS RECENT HISTORY TABLE, Word 29
- [3] Define PMD dictionary nodes to obtain description of software analysis and action taken [DLP-517]
- [4] Using Figure 1 and TABLE A, determine frame mode of operation, that is, SIMPLEX, DUPLEX

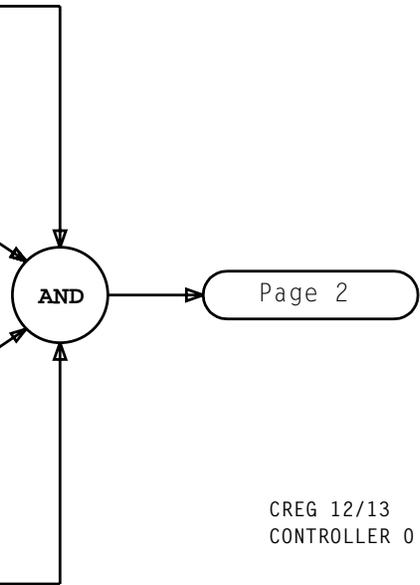


TABLE A			
	CREG 0	CREG 1	MODE OF OPERATION
State of bit 12	0	0	FRAME is DUPLEXed
	0	1	Controller 1 is OOS
	1	0	Controller 0 is OOS
	1	1	DUPLEX FAILURE

```

A 12 REPT: F-LEVEL @14703410 MFNUM=00001336 MICON=00000020 COMPLETED
LV=0040 D0=00000000 D1=60020000 D2=00000000 D3=00000000
VCFR RESTORED VIF 1 VIU 3 ← SUSPECT UNIT
DATA: F-LEVEL
00100025 07210003 14450162 45710325 00000300 00000040
00000012 14703410 03270062 14703410 00000040 14450216
00004012 14703410 02026102 00000020 07210003 00000000
16305272 04001000 00010000 00000000 60000000 00000000
01402000 00002700 00000000 00000300 00010000 00000000
60000000 00000000 01402000 00002700 00000000 00000020
02025102 07210003 00000300 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
DATA: VIF CRITICAL REGISTERS
CREG 0 → 00210047 00206004 00000000 00000000 00000000 00000000
CREG 12/13 CONTROLLER 0 → 00000000 00000007 00100010 00177777 00004000 00003503
CREG 1 → 00000000 00000000 00000000 00000000 00000000 00000000
CREG 12/13 CONTROLLER 1 → 00000000 00006007 00000411 00000000 00004000 00003746
DATA: PERIPHERAL FAULT RECOGNITION RESULTS
00000000 00000204 00000400 00000150 00000000 00000000
DATA: ERROR ANALYSIS RECENT HISTORY TABLE
04605403 27000601 00000000 00000000 00000000 00000000
00006103 00000400 00000002 00000300 00040004 50050406
20444140 00000000 00001604 00000000 00000000 00002204
00000000 00000411 00000000 00206004 00210047 04505403
00044140 00000000 00000000 00000000 00110010 20000023 ← PMD
00001336 00001336 00000003 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00002403 00000000
00100004 00010002 00000101 00000000 00000000 00000010
00000000 00000000 35363321 00000000 00000001 00000000
VIU ERROR SOURCE REGISTERS → 00000000 00000000 00000000 20000000 00000000 00000000
00000000 00000000 00031520 00000000
07/14/79 08:11:51
#514
  
```

Figure 1 - VIF Interrupt Printout

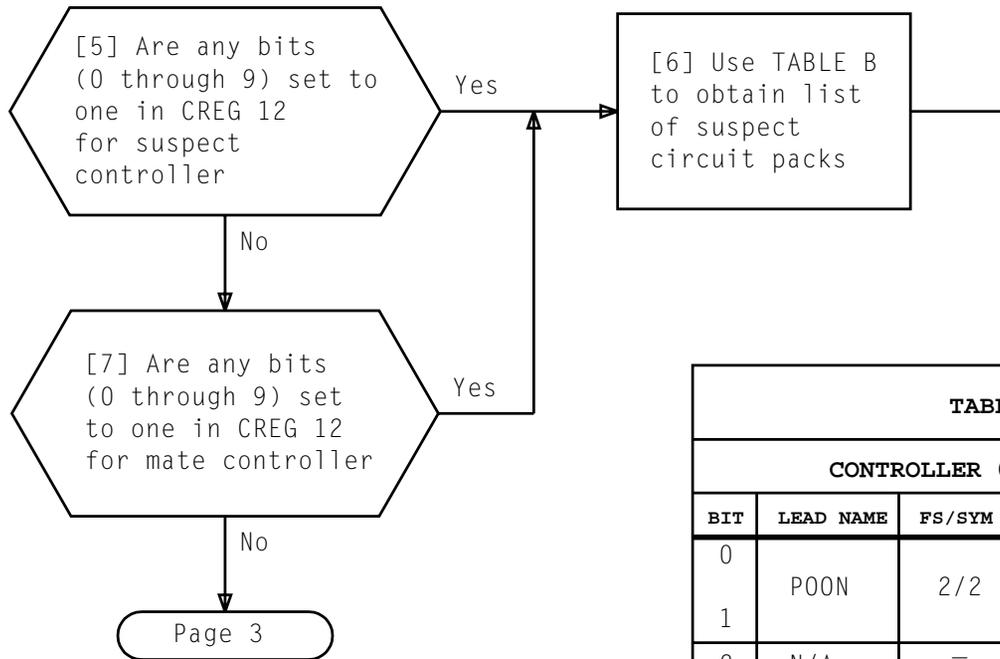


TABLE B - CREG 12 CIRCUIT PACKS - (SD56158-01)							
CONTROLLER 0, ESR BITS				CONTROLLER 1, ESR BITS			
BIT	LEAD NAME	FS/SYM	SUSPECT PACK/LOC	BIT	LEAD NAME	FS/SYM	SUSPECT PACK/LOC
0	POON	2/2	FA741 @ 148-11	0	PO1N	2/5	FA741 @ 148-26
1			FA740 @ 148-12	1			FA740 @ 148-25
			FA742 @ 148-05				FA742 @ 148-32
2	N/A	-		2	N/A	-	
3	00FNO	8/2	FA747 @ 144-08	3	00FN1	8/6	FA747 @ 144-29
			FB481 @ 144-07				FB481 @ 144-31
8	CC0N0		FA748 @ 144-09	8	CC0N0		FA748 @ 144-28
4	TC0N	12/1	FA754 @ 156-12	4	TC0N	12/1	FA754 @ 156-12
5	TC1N	12/2	FA754 @ 156-13	5	TC1N	12/2	FA754 @ 156-13
6	TC2N	12/3	FA754 @ 156-14	6	TC2N	12/3	FA754 @ 156-14
7	TC3N	12/4	FA754 @ 156-15	7	TC3N	12/4	FA754 @ 156-15
9	CC1N0	8/4	FA748 @ 144-09	9	CC1N1	8/8	FA748 @ 144-28
			FA747 @ 144-08				FA747 @ 144-29
			FA481 @ 144-07				FA481 @ 144-31

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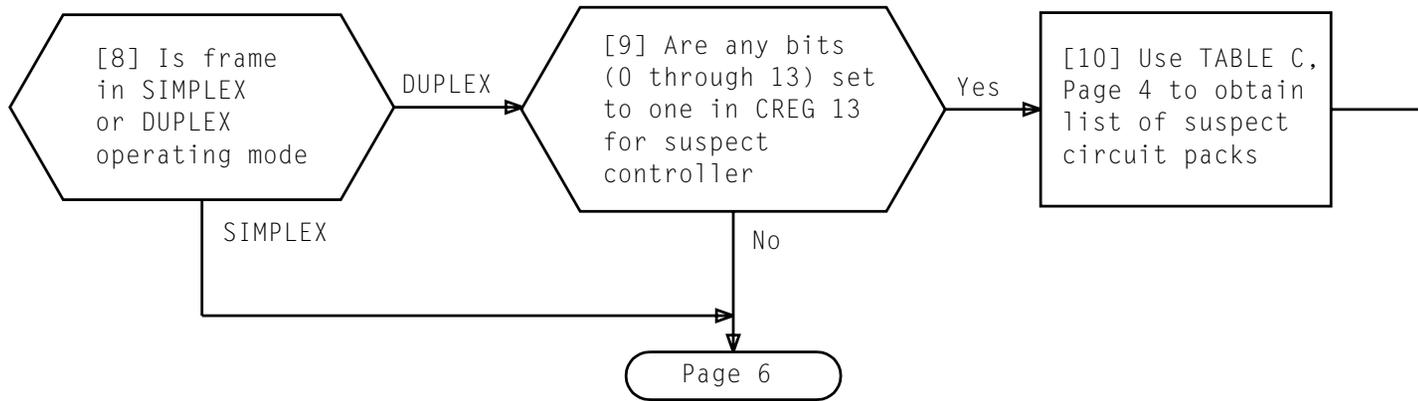


TABLE C
CREG 13 CIRCUIT PACKS - (SD-5G158-01)

CONTROLLER 0, ESR BITS					CONTROLLER 0, ESR BITS (Contd)				
BIT	LEAD NAME	FS/SYM	ERROR IDENTIFICATION	SUSPECT PACK/LOC	BIT	LEAD NAME	FS/SYM	ERROR IDENTIFICATION	SUSPECT PACK/LOC
0	MMICFNO	8/3	INDICATOR CHECK FRAME MISMATCH	FA749 @ 144-10 FA748 @ 144-09 FA747 @ 144-08	8	MMDSGNO	9/3	DIGITAL SIGNAL GENERATOR MISMATCH	FA750 @ 144-12 *FA750 @ 144-25 FA748 @ 144-09 FA749 @ 144-10
1	MMESMNO	2/2	MISMATCH ENABLE SELECT MODE ON INPUT REGISTER	FA741 @ 148-11 FA740 @ 148-12					9
2	MMREPNO	6/1	INPUT TO REPLY REGISTER MISMATCH	FA760 @ 152-18 FS 2, 3, 13 PACKS	10	MM11BNO	6/1	ERROR SOURCE REGISTER MISMATCH	FA760 @ 152-18 FA743 @ 148-07 FS 3 PACKS
3	MMMUXNO	11/5	INDICATOR MULTIPLEXER MISMATCH	FA757 @ 144-14 FA756 @ 144-17 FA756 @ 144-18 FA756 @ 148-17 FA756 @ 148-18					11
4	MMSMNO	11/5	STATUS MEMORY MISMATCH	FA757 @ 144-14 FA758 @ 144-16 *FA758 @ 144-21 FS 3 PACKS	12	CCONO	8/2	REMOTE TIMING RECEIVER CODE VIOLATION	FA747 @ 144-08 FA481 @ 144-07 FA748 @ 144-09 FA741 @ 144-11
5	MMP10	10/2	VIU CONTROL BUFFER PARITY VIOLATION 1, VIOLATION 2	FA753 @ 148-03 *FA753 @ 148-34 FA747 @ 144-08					13
6	MMP20			7	MMPSLNO	6/1	PROTECTION SWITCH LOGIC FUNCTION CODE MISMATCH	FA760 @ 152-18 FA755 @ 148-06 *FA755 @ 148-31	

* This pack is in Controller 1

TABLE C
CREG 13 CIRCUIT PACKS - (SD-5G158-01) (Contd)

CONTROLLER 1, CREG 13 ESR BITS					CONTROLLER 1, CREG 13 ESR BITS (Contd)				
BIT	LEAD NAME	FS/SYM	ERROR IDENTIFICATION	SUSPECT PACK/LOC	BIT	LEAD NAME	FS/SYM	ERROR IDENTIFICATION	SUSPECT PACK/LOC
0	MMICFN1	8/7	INDICATOR CHECK FRAME MISMATCH	FA749 @ 144-27 FA748 @ 144-28 FA747 @ 144-29	8	MMDSGN1	9/6	DIGITAL SIGNAL GENERATOR MISMATCH	FA750 @ 144-25 *FA750 @ 144-12 FA748 @ 144-28 FA749 @ 144-27
1	MMESMN1	2/5	MISMATCH ENABLE SELECT MODE ON INPUT REGISTER	FA741 @ 148-26 FA740 @ 148-25					
2	MMREPN1	6/2	INPUT TO REPLY REGISTER MISMATCH	FA760 @ 152-19 FS 2, 3, 13 PACKS	10	MM11BN1	6/2	ERROR SOURCE REGISTER MISMATCH	FA760 @ 152-19 FA743 @ 148-30 FS 3 PACKS
3	MMMUXN1	11/13	INDICATOR MULTIPLEXER MISMATCH	FA757 @ 144-23 FA756 @ 144-19 FA756 @ 144-20 FA756 @ 148-19 FA756 @ 148-20					
4	MMSMN1	11/13	STATUS MEMORY MISMATCH	FA757 @ 144-23 FA758 @ 144-21 *FA758 @ 144-16 FS 3 PACKS	12	CCON1	8/6	REMOTE TIMING RECEIVER CODE VIOLATION	FA747 @ 144-29 FA481 @ 144-31 FA748 @ 144-28 FA741 @ 741-26
5	MMP11	10/4	VIU CONTROL BUFFER PARITY VIOLATION 1, VIOLATION 2	FA753 @ 148-34 *FA753 @ 148-03 FA747 @ 144-08					
6	MMP21			13	CC1N1	8/8	REMOTE FRAME COUNTER VIOLATION	FA748 @ 144-28 FA747 @ 144-29 FA749 @ 144-27	
7	MMPSLN1	6/2	PROTECTION SWITCH LOGIC FUNCTION CODE MISMATCH	FA760 @ 152-19 FA755 @ 148-31 *FA755 @ 148-06					

* This pack is in Controller 0

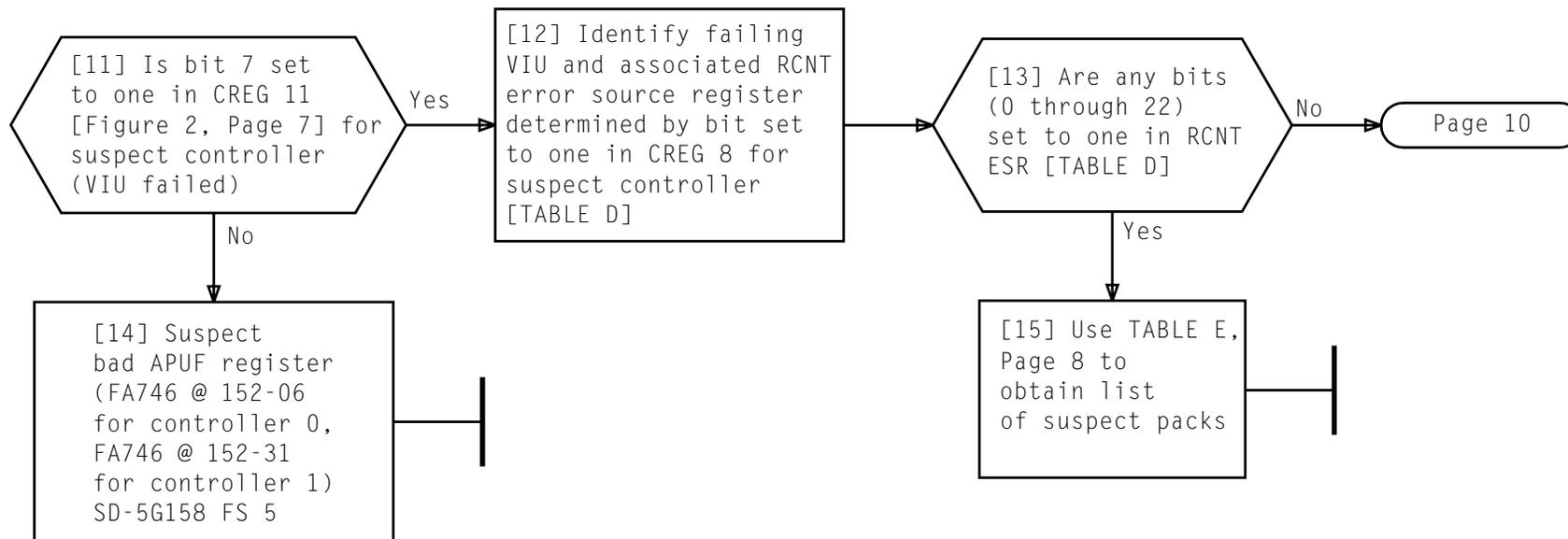


TABLE D		
CREG 8 SET BIT	FAILING VIU	ASSOCIATED ERROR SOURCE REGISTER
0	0	RCNT+54
1	1	RCNT+55
2	2	RCNT+56
3	3	RCNT+57
4	4	RCNT+58
5	5	RCNT+59
6	6	RCNT+60
7	7	RCNT+61

```

A 12 REPT: F-LEVEL @14703410 MFNUM=00001336 MICON=00000020   COMPLETED
LV=0040 D0=00000000 D1=60020000 D2=00000000 D3=00000000
VCFR RESTORED VIF 1 VIU 3 ← SUSPECT UNIT
DATA: F-LEVEL
00100025 07210003 14450162 45710325 00000300 00000040
00000012 14703410 03270062 14703410 00000040 14450216
00004012 14703410 02026102 00000020 07210003 00000000
16305272 04001000 00010000 00000000 60000000 00000000
01402000 00002700 00000000 00000300 00010000 00000000
60000000 00000000 01402000 00002700 00000000 00000020
02025102 07210003 00000300 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000
CREG 8/9
CONTROLLER 0
DATA: VIF CRITICAL REGISTERS
00210047 00206004 00000000 00000000 00000000 00000000
00000000 00000007 00100010 00177777 00004000 00003503 ← CREG 10/11
00000000 00000000 00000000 00000000 00000000 00000000
CONTROLLER 0
00000000 00006007 00000411 00000000 00004000 00003746 ← CREG 10/11
00000000 00000204 00000400 00000150 00000000 00000000
CONTROLLER 1
DATA: PERIPHERAL FAULT RECOGNITION RESULTS
00000000 00000000 00000023 10121656
CREG 8/9
DATA: ERROR ANALYSIS RECENT HISTORY TABLE
CONTROLLER 1
04605403 27000601 00000000 00000000 00000000 00000000
00006103 00000400 00000002 00000300 00040004 50050406
20444140 00000000 00001604 00000000 00000000 00002204
00000000 00000411 00000000 00206004 00210047 04505403
00044140 00000000 00000000 00000000 00110010 20000023
00001336 00001336 00000003 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00002403 00000000
00100004 00010002 00000101 00000000 00000000 00000010
00000000 00000000 35363321 00000000 00000001 00000000
RCNT 54 ← 00000000 00000000 00000000 20000000 00000000 00000000 ← RCNT 54
00000000 00000000 00031520 00000000
07/14/79 08:11:51
#514

```

Figure 2 - VIF Interrupt Printout

TABLE E
RCNT+54 THROUGH RCNT+61 (SD-5G157)

SET BIT	LEAD NAME	FS/SYM	ERROR INDICATION	SUSPECT PACK/LOC	SET BIT	LEAD NAME	FS/SYM	ERROR INDICATION	SUSPECT PACK/LOC
0	S3	7/2	SIGNAL ALARM IN BLOCK CONTAINING TRUNK 125	JA3 @ 09-02	4	P2	5/5	DECODER I/P PROCESSOR PARITY FAIL ALARM	FA726 @ 03-18
				JA6 @ 09-03					FA728 @ 03-16
1	S2	7/1	SIGNAL ALARM IN BLOCK CONTAINING TRUNK 127	JA7 @ 09-25	5	P1	4/12	PARITY OVER DATA PASSED BETWEEN PACKS FA727, FA571, FB220	FA729 @ 15-19
				JA5 @ 09-26					FA730 @ 15-17
2	S1	7/2	SIGNAL ALARM IN BLOCK CONTAINING TRUNK 126	JA4 @ 09-30	6	D3	7/2	HIGH DISTORTION IN BLOCK CONTAINING TRUNK 125	FA731 @ 03-11
				FA724 @ 03-19					FA731 @ 09-11
3	S0	7/1	SIGNAL ALARM IN BLOCK CONTAINING	JA3 @ 09-04	7	D2	7/1	HIGH DISTORTION IN BLOCK CONTAINING TRUNK 127	JA3 @ 09-02
				JA6 @ 09-05					JA6 @ 09-03
3	S0	7/1	SIGNAL ALARM IN BLOCK CONTAINING	JA7 @ 09-27	8	D1	7/2	HIGH DISTORTION IN BLOCK CONTAINING TRUNK 126	JA7 @ 09-25
				JA5 @ 09-28					JA5 @ 09-26
3	S0	7/1	SIGNAL ALARM IN BLOCK CONTAINING	JA4 @ 09-30	9	D0	7/1	HIGH DISTORTION IN BLOCK CONTAINING TRUNK 0	JA5 @ 09-28
				FA724 @ 03-20					JA3 @ 09-04
3	S0	7/1	SIGNAL ALARM IN BLOCK CONTAINING	FA723 @ 15-13	10	P4	6/2	CONTROL ACCESS PARITY M/M	FA732 @ 03-13
				FA731 @ 09-11					FA731 @ 03-11

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ANALYZE VCFR, F-LEVEL INTERRUPT

TABLE E (Contd)
RCNT+54 THROUGH RCNT+61 (SD-5G157)

SET BIT	LEAD NAME	FS/SYM	ERROR INDICATION	SUSPECT PACK/LOC	SET BIT	LEAD NAME	FS/SYM	ERROR INDICATION	SUSPECT PACK/LOC
11	P3	5/5	DECODER I/P PROCESSOR PARITY FAIL	SAME AS BIT 4	17	P5	5/3	PARITY ERROR IN SERIAL/ RETIMING	FA733 @ 03-16 FA730 @ 03-17 FB480 @ 03-15
12	TRU	2/4	OUTPUT CLOCK ERROR ALARM	FA721 @ 15-22 FA729 @ 15-19 FA731 @ 03-11	18	PWR	8/1	80A OR 81A PWR SUPPLY FAILURE	80A @ 09-08 81A @ 09-23
13	TRL	2/5	OUTPUT CLOCK ERROR ALARM	FA721 @ 03-22 FA729 @ 15-19 FA731 @ 03-11	19	CST	2/1	STATE OF VIU CLOCK	NOT USED
14	TTU	2/2	OUTPUT CLOCK ERROR ALARM	FA721 @ 15-09 FA729 @ 15-19 FA731 @ 03-11	20	CSO	2/1	ALARMS WHEN CLOCK SELECT AND BUFFER SWITCH FROM CONTR 0 TO 1 OR 1 TO 0	FA729 @ 15-19 FA731 @ 03-11 SD-5G156-01
15	TTL	2/3	OUTPUT CLOCK ERROR ALARM	FA721 @ 03-09 FA729 @ 15-19 FA731 @ 03-11	21			NOT USED	
16	P6	6/1	PARITY VIOLATION (CONTROL)	FA731 @ 03-11 SD-5G156-01	22	REF	5/2	FAILURE TO FRAME ON PCM DATA	FA733 @ 03-16 FB480 @ 03-15 FA730 @ 03-17 TSI PROBLEM, COAX PROBLEM

ANALYZE VCFR, F-LEVEL INTERRUPT

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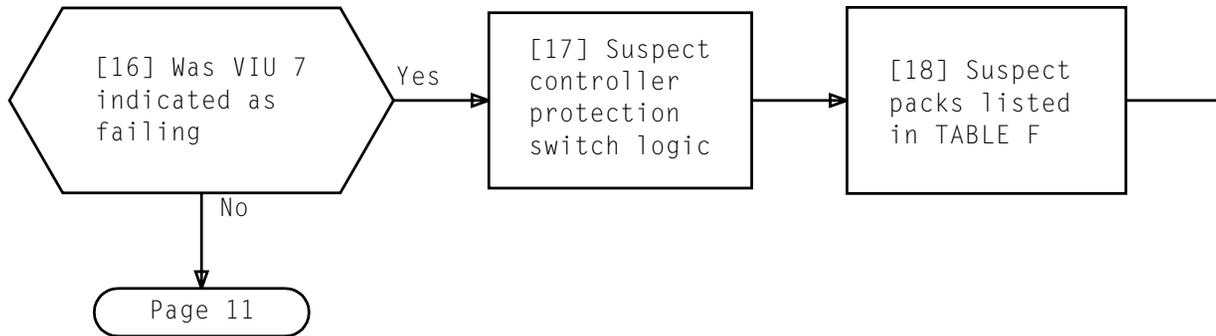


TABLE F	
CIRCUIT PACK	LOCATION
FA 755	148-06
FA 755	148-31
FC 195	156-21
FC 195	156-24

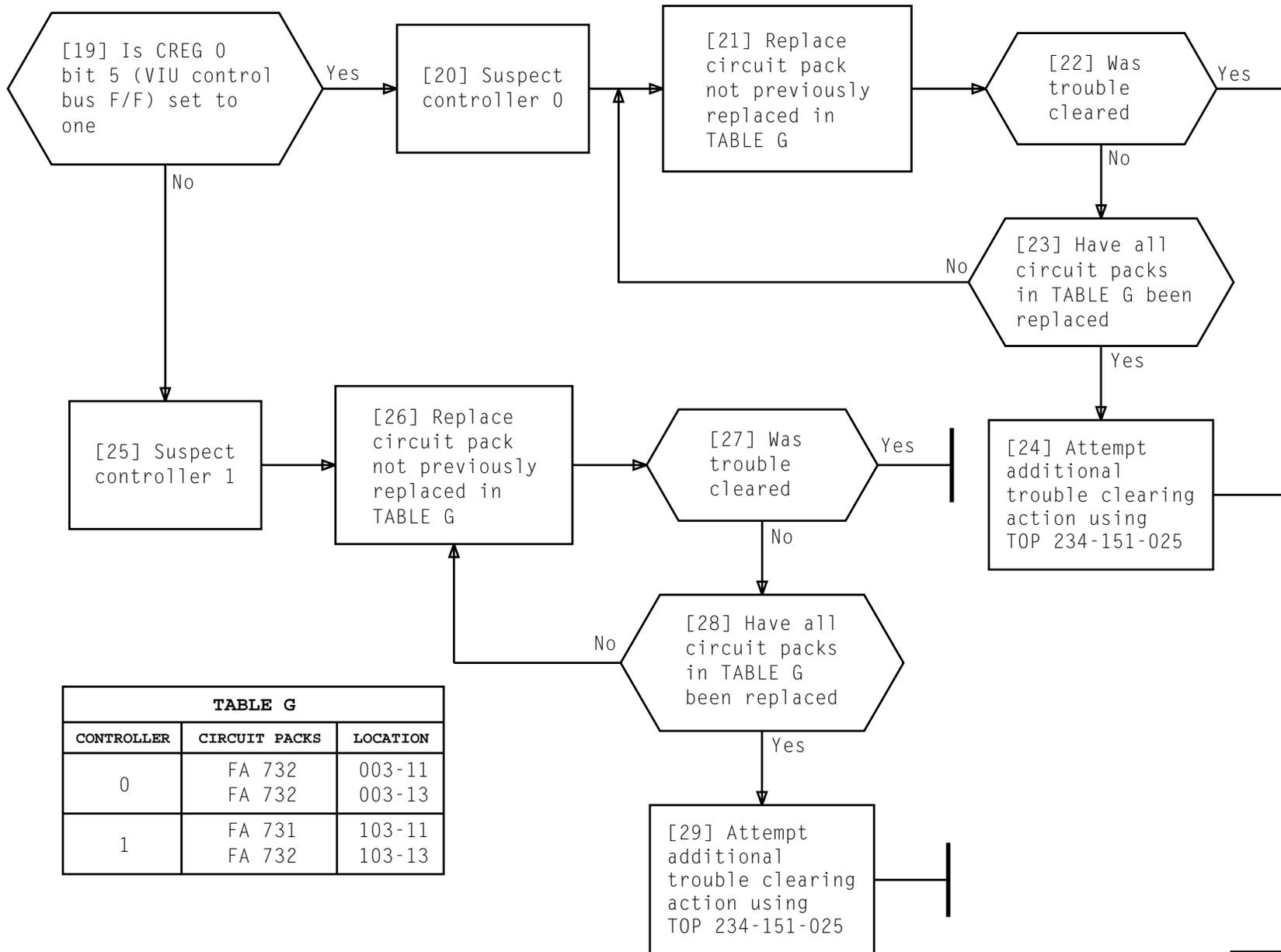


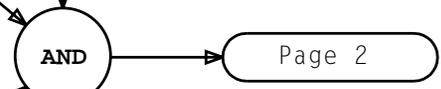
TABLE G		
CONTROLLER	CIRCUIT PACKS	LOCATION
0	FA 732	003-11
	FA 732	003-13
1	FA 731	103-11
	FA 732	103-13

See Figure 1:

- [1] Identify VIU where error was detected
- [2] Locate and note contents of register associated with VIU where error was detected

See Figure 2:

- [3] Convert contents of associated VIU register from octal to binary
- [4] Determine rightmost set bit



A 39 REPT: INTERJECT @14207170 MFNUM=00001321 MICON=00000000 COMPLETED
 LVDATA=0400 SRDATA=00000000 FRDATA=60000000

VCFR RESTORED VIF 12 VIU 4

INTERJECT
06020000

PERIPHERAL FAULT RECOGNITION RESULTS
00000000 00000000 00000036 16465532

ERROR ANALYSIS RECENT HISTORY TABLE

04645430	00000000	00000000	20000000	00000400	00000000
00002003	00000400	00010000	20000000	00000000	00000000
04146040	00000000	00001604	00000000	00000000	00000000
00000000	00010020	00000000	00002000	00004160	04645430
00046040	00000000	00000000	00000000	00076210	20000036
04641321	00001321	00000024	00000000	00000000	00000000
00000000	00000000	00000000	00000000	00000000	00000000
00100004	00012001	00000101	00000000	00000200	00000000
00000000	00000000	74416516	00000000	00000001	00000000

VIU WHERE
ERROR WAS
DETECTED

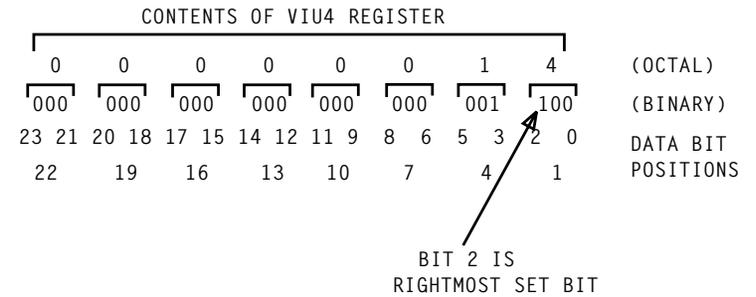


Figure 2 - Example of Rightmost Set Bit

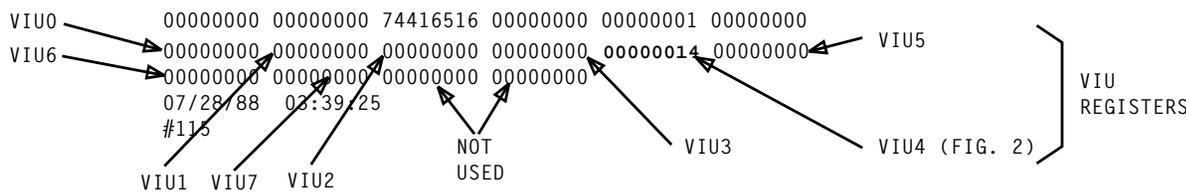


Figure 1 - VCFR Interject Printout

ANALYZE VCFR INTERJECT

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[5] Determine type of error associated with rightmost set bit [TABLE A]

[6] Locate type of error in TABLE B, Page 3. Identify and list all associated suspect circuit packs [NOTES 1 and 2]

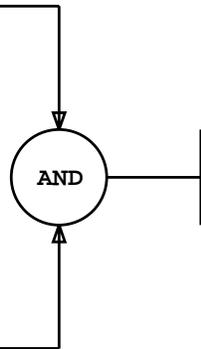


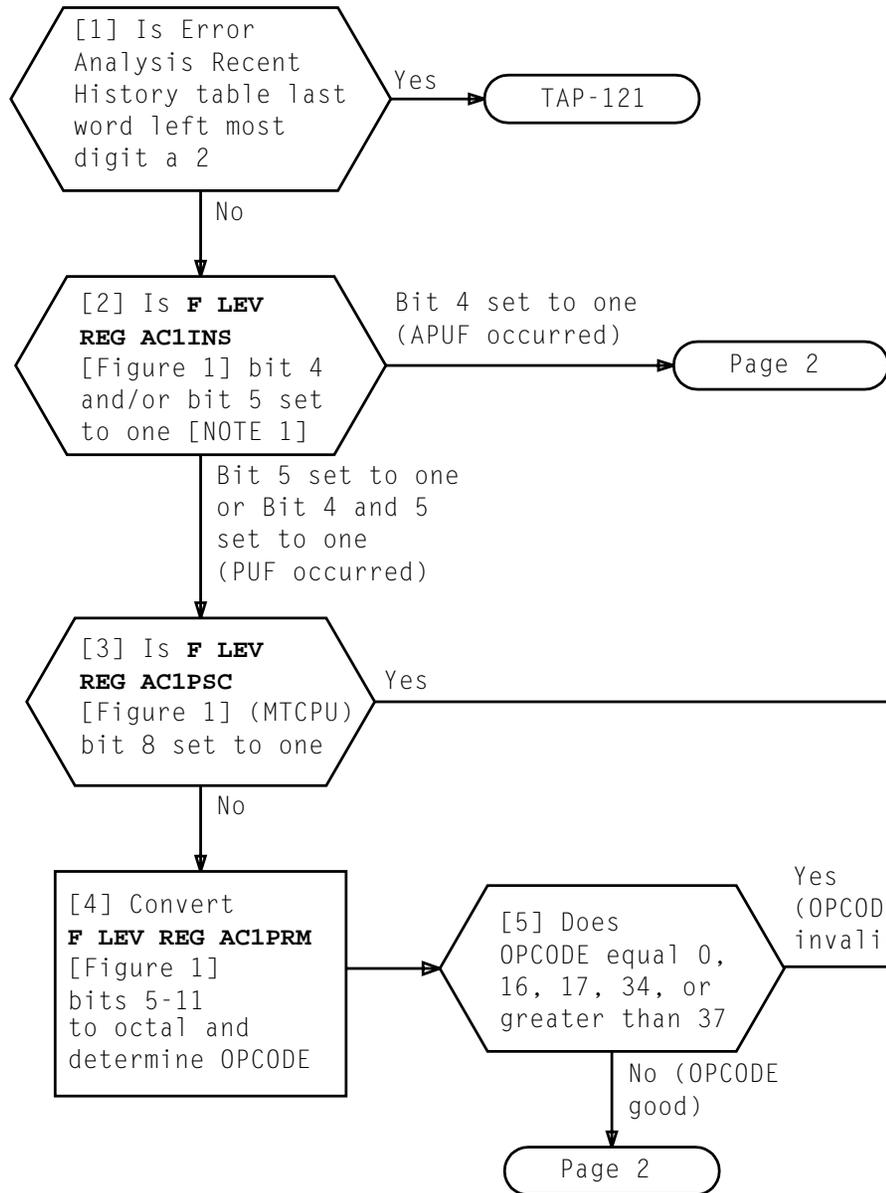
TABLE A																								
TYPE OF ERROR PER BIT POSITION																								
DATA BITS	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TYPE OF ERROR		R E F		C S O	C S T	P W R	P 5	P 6	T L	T U	T L	T U	P 3	P 4	D 0	D 1	D 2	D 3	P 1	P 2	S 0	S 1	S 2	S 3

NOTES	
1. All possibilities of troubles are not covered in TABLE B, Page 3. Any troubles found that are not listed should be added to TABLE B, Page 3	
2. Numbers in parenthesis are circuit pack locations	
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**TABLE B
SUSPECT CIRCUIT PACKS ASSOCIATED WITH TYPE OF ERROR**

SUSPECT CIRCUIT PACKS	TYPE OF ERROR																				REF				
	S3	S2	S1	S0	P2	P1	D3	D2	D1	D0	P4	P3	TRU	TRL	TTU	TTL	P6	P5	PWR	CST		CSO			
JA 3 (09-02)	X	X					X	X																	
JA 6 (09-03)	X	X					X	X																	
JA 3 (09-04)			X	X					X	X															
JA 6 (09-05)			X	X					X	X															
JA 7 (09-25)	X	X					X	X																	
JA 5 (09-26)	X	X					X	X																	
JA 7 (09-27)			X	X					X	X															
JA 5 (09-28)			X	X					X	X															
JA 4 (09-29)	X		X																						
JA 4 (09-30)		X		X																					
FA724(03-19)	X	X																							
FA724(03-20)			X	X																					
FA723(15-11)		X	X																						
FA723(15-13)	X	X																							
FA571(15-17)							X																		
FA733(03-16)																									X
FB480(03-15)																									X
FA730(03-17)																									X
FA731(03-11)	X	X	X	X																					
FA732												X													
FB220(15-21)							X																		

ANALYZE VCFR INTERJECT



SPFR RESTORED SP 12 CONTR 1

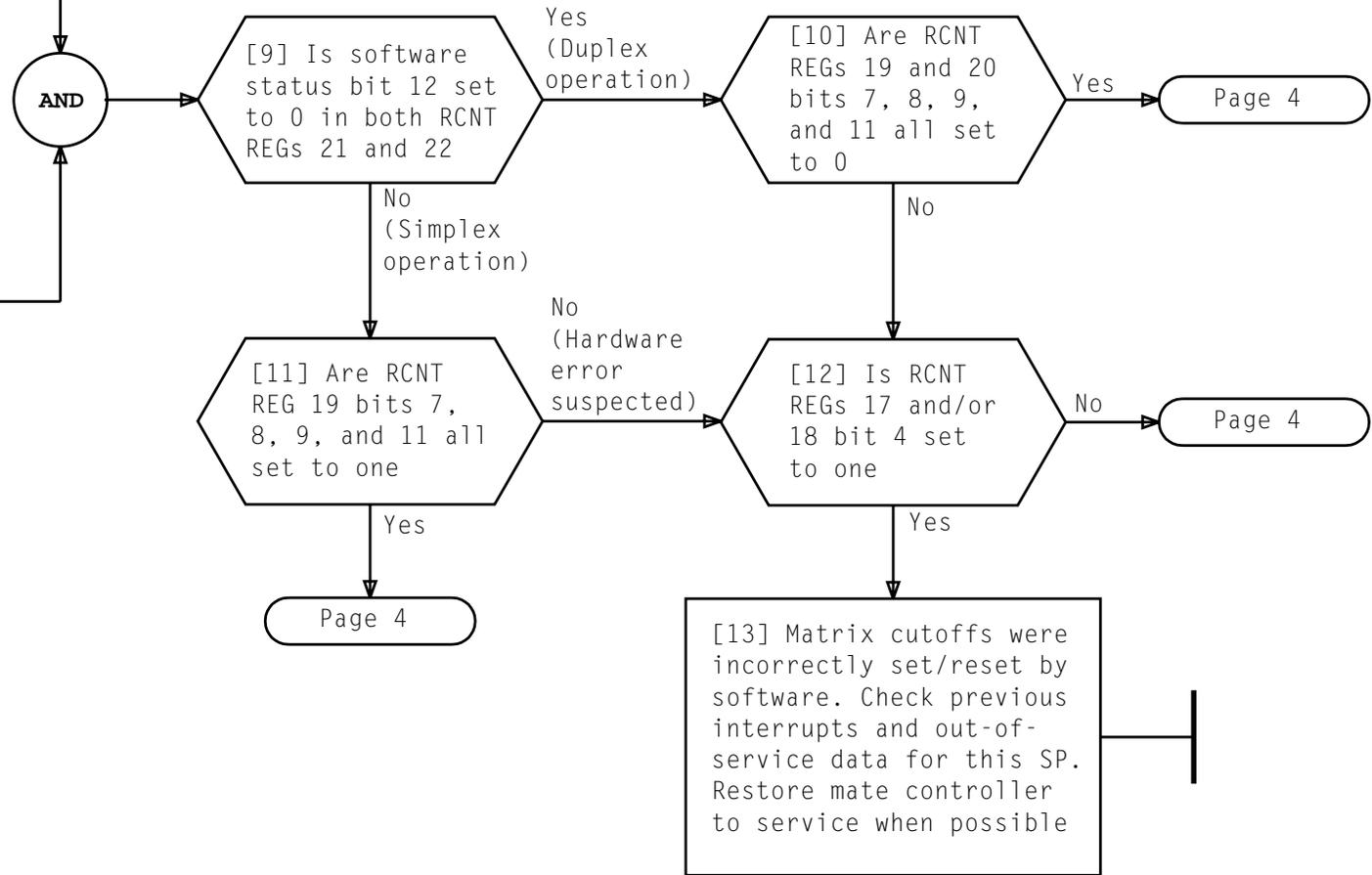
F-LEVEL					
AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASF(H)	AC1ASF(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1LR	
AC1PSQ	AC1ULR	AC1PES	ST1PES	ST1ER	ST1PRM
ST1PRL	ST1PSC	AC1RP0/	AC1RP1	ST1RP0	ST1RP1
ST1CSC	ST1INH	PUIRFLC00/	PUIRFLC01	PUIRFLC02	PUIRFLC03
PUIRFLC04	PUIRFLC05	PUIRFLC06	PUIRFLC07		

Figure 1 - F-Level Register Printout

NOTE 1	
If both bits are set, then use PUF path	
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[7] Determine which controller is suspect. RCNT REG 0 [Figure 2, Page 3] bit 0 indicates which controller is suspect

[8] Determine hardware and software status as indicated by RCNT 19-22 register bits 0-6 [Figure 2 and TABLE A, Page 3]



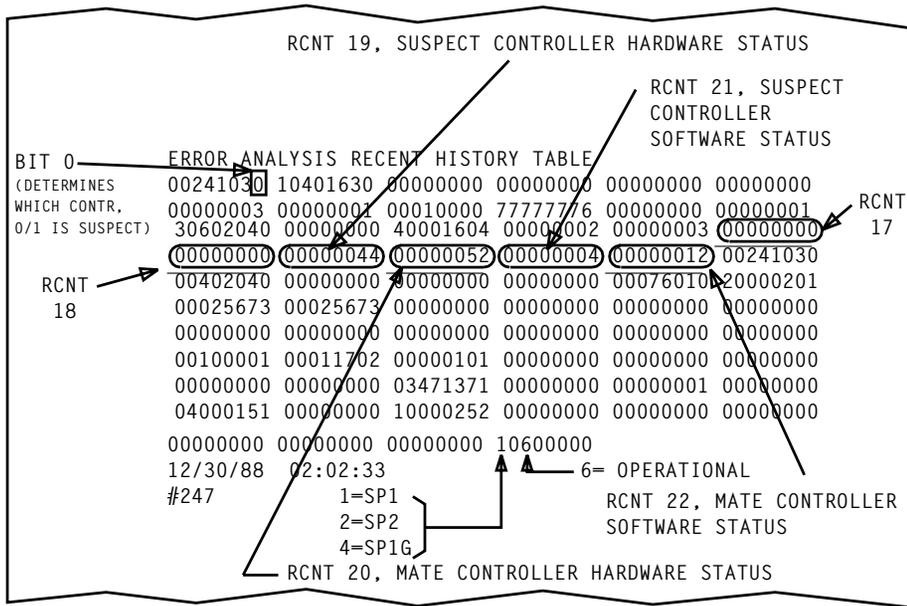
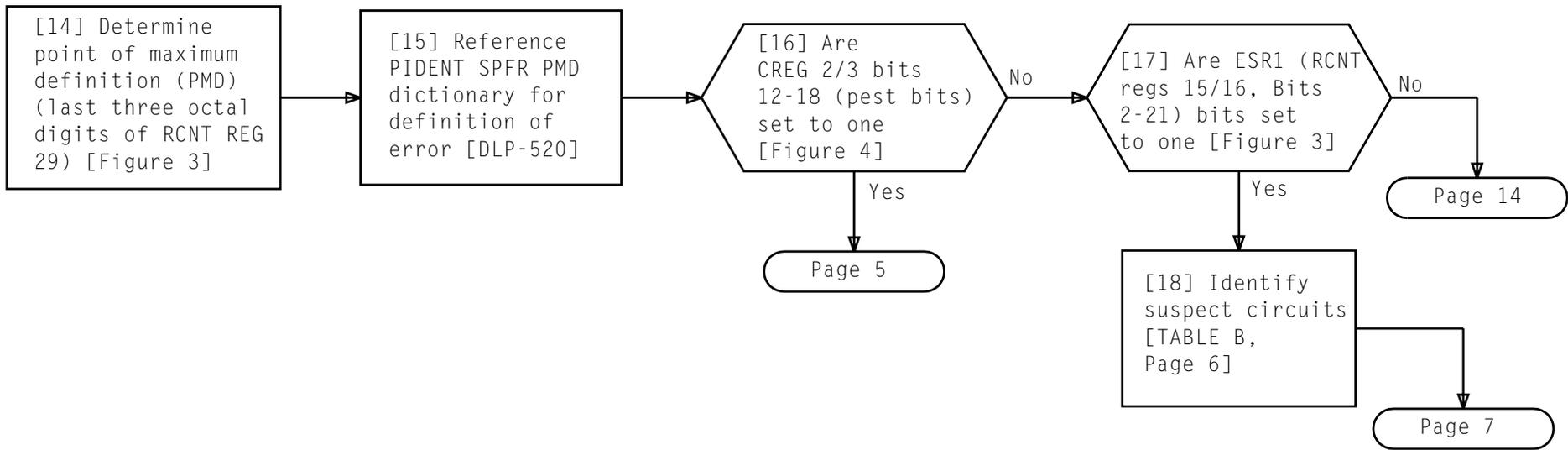


Figure 2 - RCNT Register Printout

TABLE A RCNT 19-22, HARDWARE/SOFTWARE STATUS			
BIT	NAME	STATE	IMPLICATION
0	MA	0	Operational mode
		1	Maintenance mode
1	R0	0	Receiving on Bus 0
		1	Receiving on Bus 1
2	S0	0	Not sending on Bus 0
		1	Sending on Bus 0
3	S1	0	Not sending on Bus 1
		1	Sending on Bus 1
4	DIV	0	DUPLEX
		1	SIMPLEX - should be set in both controllers
*5	STOP	0	SP not stopped
		1	Stopped for out-of-service or interrupt (only set in out-of-service controller in hardware status)
6	CA	0	Using clock from controller 0
		1	Using clock from controller 1 Both controllers should be using the same clock. If the frame is SIMPLEX, it should be the in-service controller

*Bit 5 (RCNT REGs 19 and 20) is always set on an F-level interrupt printout



RCNT 15 ESR 1 REG SUSPECT	RCNT 16 ESR 1 REG MATE	PMD NUMBER	
ERROR ANALYSIS RECENT HISTORY TABLE			
00241030	10401630	00000000	00000000
00000003	00000001	00010000	77777776
30602040	00000000	40001604	00000002
00402040	00000000	00000000	00000003
00025673	00025673	00000000	00000004
00000000	00000000	00000000	00000012
00100001	00011702	00000101	00000000
00000000	00000000	03471371	00000001
04000151	00000000	10000252	00000000
00000000	00000000	00000000	10600000
12/30/88	02:02:33		
#247			

Figure 3 - RCNT Register Printout

CREG 2	CREG 3	CREG 10	CREG 11	CREG 76	CREG 77
SP INTERNAL REGISTERS					
00000000	00000000	00000000	00000000	00000000	00002640
00000000	05620243	00000000	00002377	00000000	00000517
00000000	00000000	00000000	00000000	00000000	00000000
00000000	77777777	00000000	77770000	00000000	42424242
00000000	00000000	00000000	50027704	00000000	50027704
00000000	60406000	00000000	00000000	00000000	60406000
00000000	46200000	00000000	46200000	00000000	00054406
00000000	00070007	00000000	00002525	00000000	37523752
37403740	37403740	37133703	37133703	34003400	34003400
00000000	37473747	00000000	32443244	00000000	77777777
00000000	00000000	00000000	25252525	00000000	52525252
00000000	00000000	00000000	00000000	00000000	00000000
00000000	77777777	00000000	77777777	00000000	00000001
00000000	00006067	00000000	00007740	00000000	02500200
00000000	01246033	00000000	00200000	00000000	01404043
00000000	35160400	00000000	00000000	00000000	34200252
00000000	13600000				

Figure 4 - SP Internal Register Printout

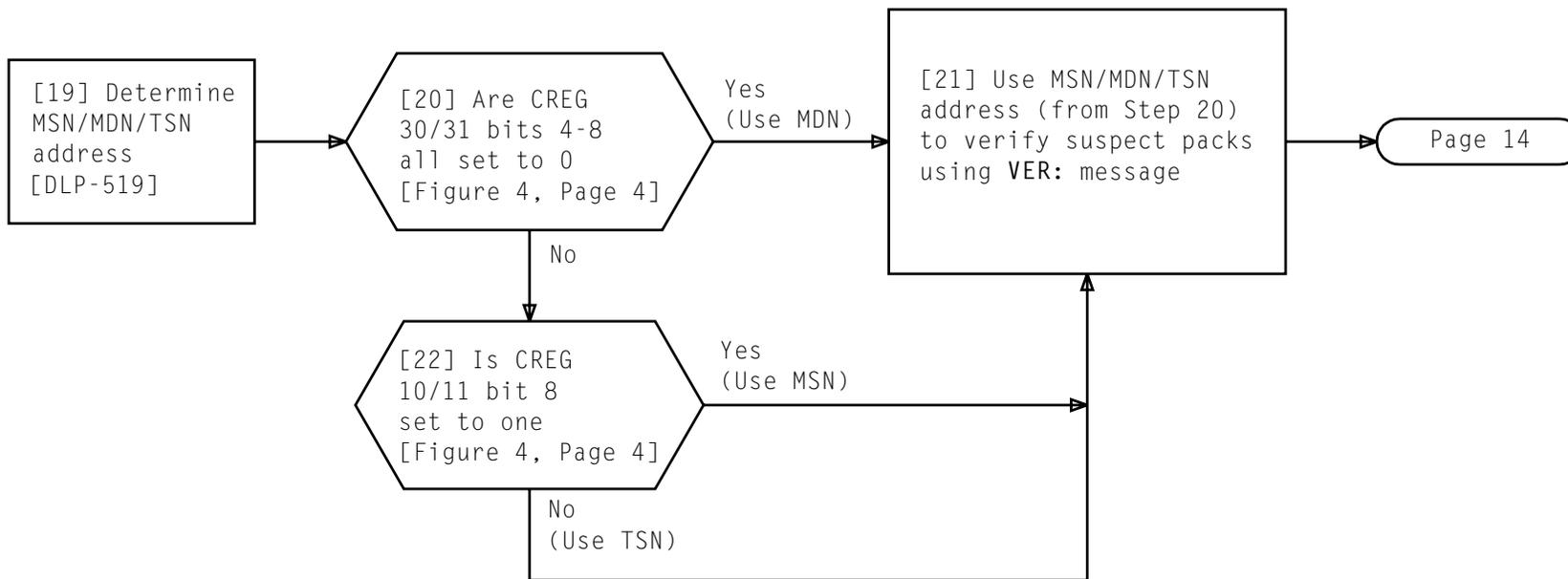
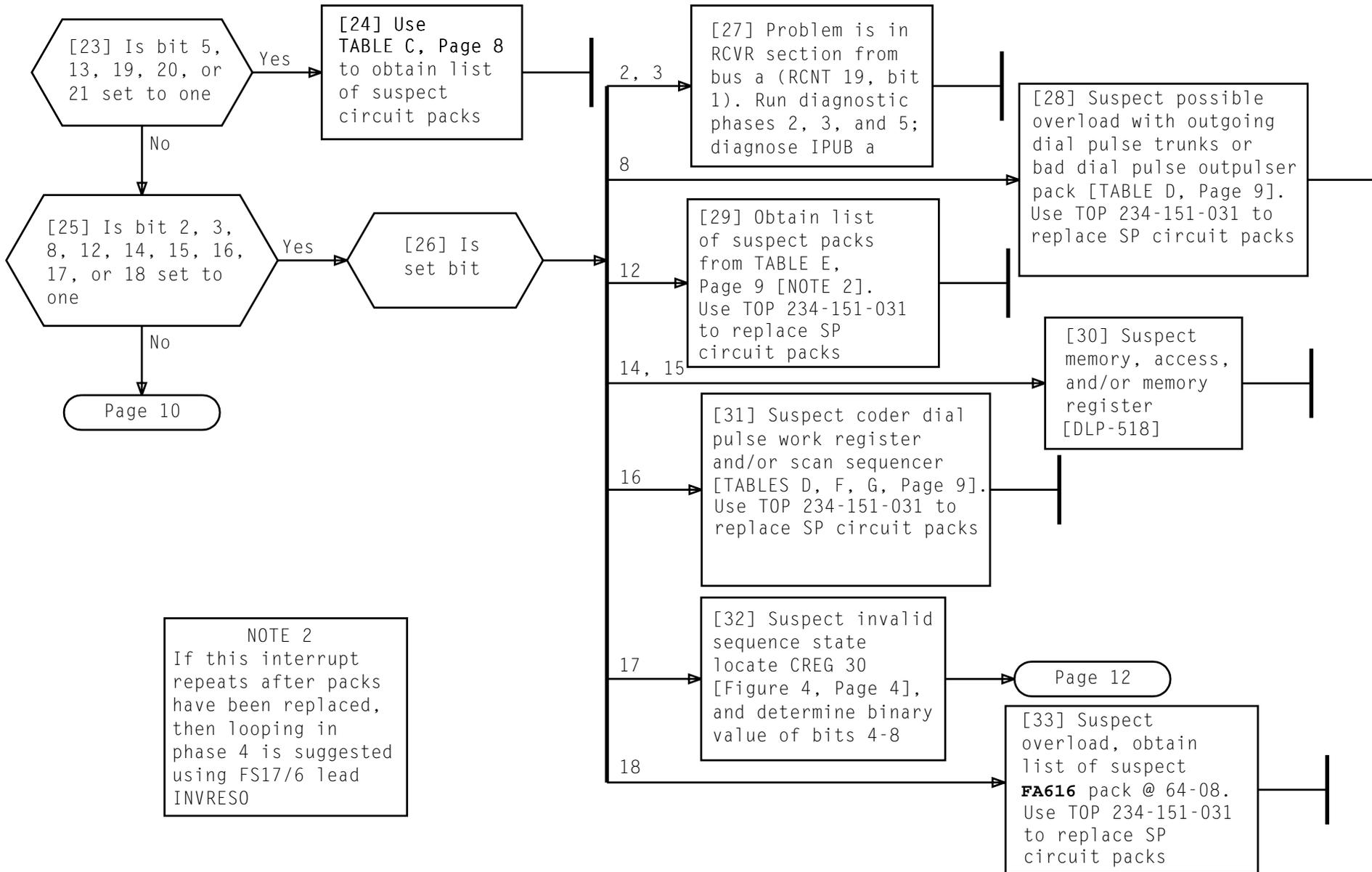


TABLE B			
ESR 1 (RCNT 15 AND 16)			
PACKS IMPLICATED BY ESR BITS CAN BE FOUND IN SD-4A013			
ESR1 BIT	NET NAME	SOURCE FS/SYMBOL	COMMENTS
0	SASWF0	19/10	Directed order failure
1	SATNT0	19/10	Autonomous failure
2	PARE1	1/9	PU bus input parity fail
3	PAR01	1/11	PU bus input parity fail
4	INTJOA	19/24	Interject
5	TROUT0	20/3	Analog timer time-out
6	MXTADRM0	10/14	Matrix address register mismatch
7	RBRMM0	2/9	Reply bus register mismatch
8	DPOLF0	16/3	DP out worklist overflow
9	-	-	-
10	SEQMM0	10/1	Autonomous sequencer mismatch
11	MRMM0	8/11	Memory register mismatch
12	INVRES0	17/6	Invalid OPCODE
13	DETOUT1 CCERRO	20/3 20/6	Level detector error Clock error
14	MRP1ER0	8/3	Memory parity 1
15	MRP2ER0	8/4	Memory parity 2
16	GTH0	14/5	Coder greater than DPWR
17	SQINVS0	10/1	Sequencer invalid state
18	SANTT00	18/2	Executive sequencer sanity error
19	XMCLER0	20/12	Extended MS clock error
20	CLKMM0	20/9	Ring counters mismatch
21	DPRWER0	12/10	Missing DP in end-of-list flag
22	-	-	-
23	-	-	-



NOTE 2
 If this interrupt repeats after packs have been replaced, then looping in phase 4 is suggested using FS17/6 lead INVRESO

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TABLE C ESR1 SUSPECT PACKS/ACTION			
ESR BIT	SP-1 COMBINED MATRIX		COMMENTS/RECOMMENDED PROCEDURE
	PACK TYPE	LOCATION	
2,3	—	—	Problem in RCVR section from BUS a (RCNT 19, bit 1); run DGN phases 2, 3, and 5/DGN:IPUB a
5	FB002 FB001 FA668	60-04 56-04 60-06	
8	—	—	Possible overloaded outgoing dial pulse trunks or bad FS14 circuit pack
12	—	—	Check lead INVRES0 (FS17/6) if pack replacement does not solve problem
13, *20	FB001 FA663 FB002 FB003 FA664	56-04 56-06 60-04 56-05 56-07	
14,15	—	—	Perform memory pack procedure [DLP-518]
16	—	—	Suspect coder (FS13) dial pulse work reg (FS14) and/or scan sequencer (FS12)
17	—	—	Check for invalid sequencer state
18	—	—	Possible SP overload (not serving offered load) suspect executive sequencer circuit packs (FS18)
19	FA575	68-06	
21	FA577 FA588	64-20,21,22 64-25	Also, suspect scan sequencer circuit packs (FS12)
* Bad pack could be in either controller			

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TABLE D FS14 CIRCUIT PACKS	
SP-1 COMBINED MATRIX	
PACK TYPE	LOCATION
FA577	60-16
FA576	60-14, 13, 12
FA621	60-11
FA620	60-10
FA588	64-23

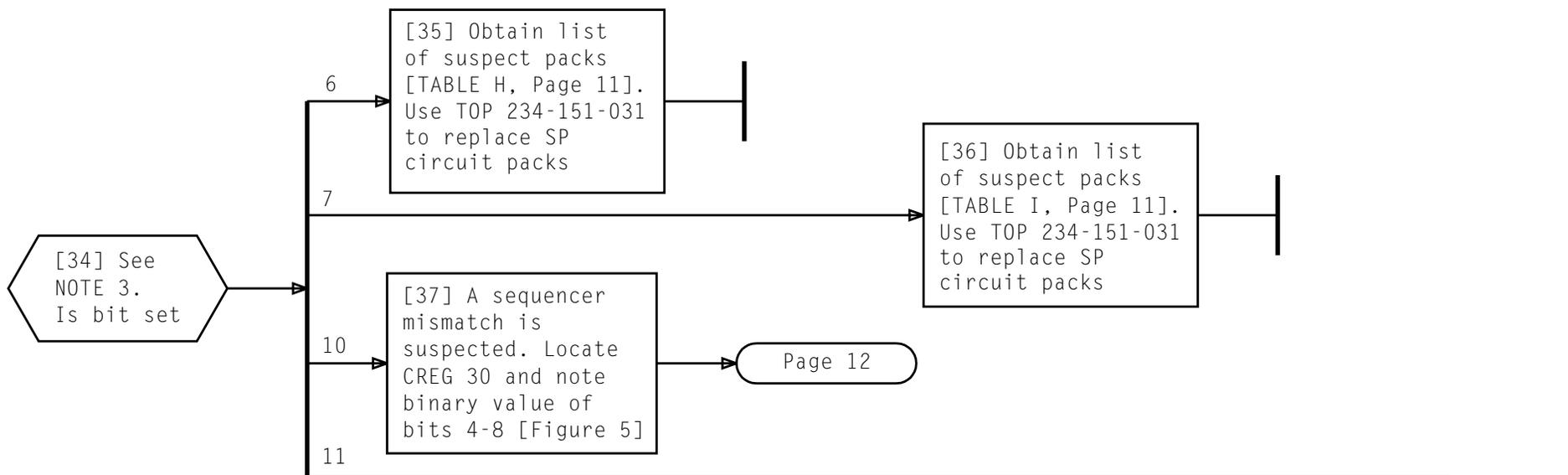
TABLE F FS12 CIRCUIT PACKS	
SP-1 COMBINED MATRIX	
PACK TYPE	LOCATION
FA592	64-16
FA593	64-17
FA589	64-18
FA591	64-19
FA600	64-11
FA598	64-10
FA602	64-14
FA613	64-12
FA621	60-11
FA601	64-13

TABLE E FS17 CIRCUIT PACKS			
SP-1		COMBINED MATRIX	
PACK TYPE	LOCATION	PACK TYPE	LOCATION
FA618	72-23	FA1243	72-23
FA619	72-24	FA1242	72-24
FA604	72-20	FA525	72-20
FA583	72-21	FA583	72-21
FA525	72-22	FA603	72-22
FA603	72-25	FA619	72-25
FA599	56-26	FA599	56-26

TABLE G FS13 CIRCUIT PACKS	
PACK TYPE	SP-1/COMBINED MATRIX LOCATION
FA576	60-12, 13, 14

ANALYZE SP F-LEVEL INTERRUPT

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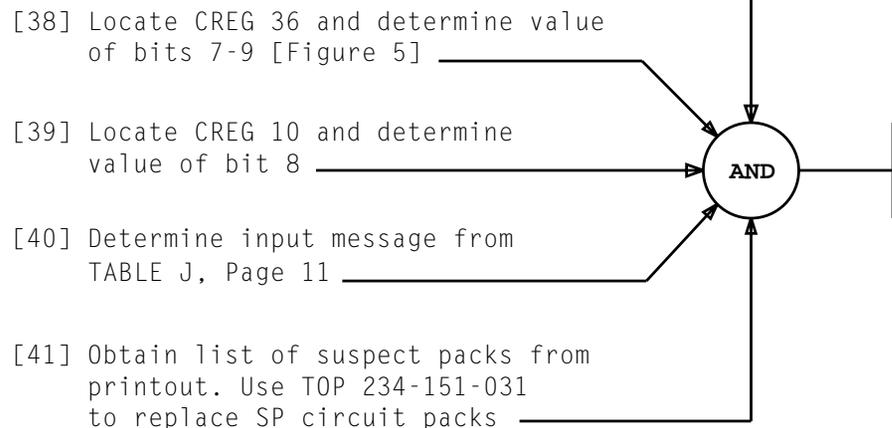


CREG 10

SP INTERNAL REGISTERS				
00000000	00000000	00000000	00000000	00002640
00000000	05620243	00000000	00002377	00000517
00000000	00000000	00000000	00000000	00000000
00000000	77777777	00000000	77770000	00000000
00000000	00000000	00000000	50027704	00000000
00000000	60406000	00000000	00000000	00000000
00000000	46200000	00000000	46200000	00054406
00000000	00070007	00000000	00002525	00000000
37403740	37403740	37133703	37133703	34003400
00000000	37473747	00000000	32443244	00000000
00000000	00000000	00000000	25252525	00000000
00000000	00000000	00000000	00000000	00000000
00000000	77777777	00000000	77777777	00000000
00000000	00006067	00000000	00007740	00000000
00000000	01246033	00000000	00200000	00000000
00000000	35160400	00000000	00000000	00000000
00000000	13600000			

CREG 30 points to the 6th column.
CREG 36 points to the 7th column.

Figure 5 - SP Critical Register (CREG) Printout



NOTE 3 Bad pack could be in either controller	
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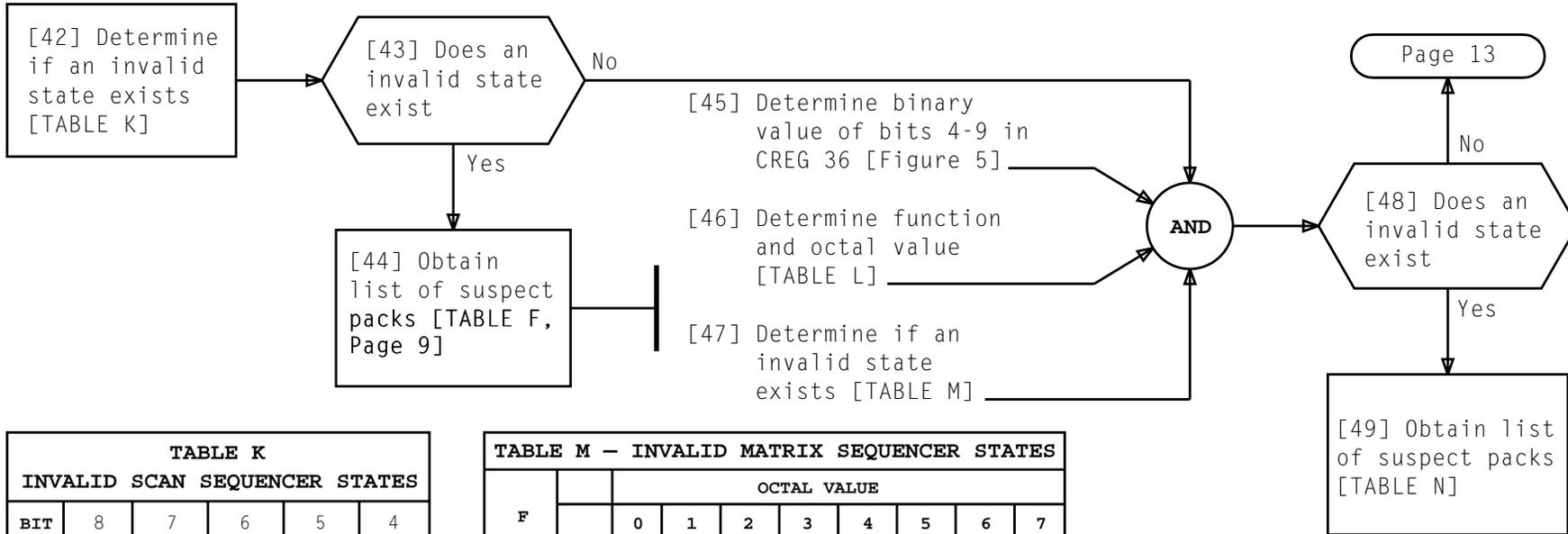
TABLE H FS10 CIRCUIT PACKS			
SP-1		COMBINED MATRIX	
PACK TYPE	LOCATION	PACK TYPE	LOCATION
FA590	56-19,20,21,22	FA1239	56-19,20,21,22
FA587	56-11	FA1238	56-11
FA597	56-13	FA1241	56-13
FA596	56-12	FA1240	56-12
FA584	56-18,17,16,14	FA584	56-18,17,16,14
FA599	56-26,25,24	FA599	56-26,25,24

TABLE I FS 2 CIRCUIT PACKS	
PACK TYPE	SP-1/COMBINED MATRIX LOCATION
FA531	72-09,10
FA534	72-08
FA528	72-04,05,06,07 72-11,12,13,14

TABLE J VERIFY MESSAGES		
CREG 36 BITS 7-9 VALUE	CREG 10 BIT 8 VALUE	USE VERIFY MESSAGE
0	0	VER:SPMTXPK:SCP,TSN o'a!
0	1	VER:SPMTXPK:SCP,MSN o'a!
≠ 0	0	VER:SPMTXPK:SDM,TDN o'a!
≠ 0	1	VER:SPMTXPK:SDM,MDN o'a!
a = TSN, MSN, TDN, or MDN octal number		

ANALYZE SP F-LEVEL INTERRUPT

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BIT	8	7	6	5	4		
V A L U E	1	0	0	1	0	0	
			0	1	0	0	
		1	0	1	1	0	0
			0	1	0	1	0
	1	1	0	1	0	1	
			1	0	0	1	

F U N C T I O N	OCTAL VALUE							
	0	1	2	3	4	5	6	7
A				*	*	*		
B				*	*	*		
C					*			
D					*			
E			*	*	*			
F	*	*	*	*	*	*	*	*
G					*			
H			*	*	*			

PACK TYPE		LOCATION
SP-1	COMBINED MATRIX	
FA587	FA1238	56-11
FA597	FA1241	56-13
FA596	FA1240	56-12
FA599		56-26,25,24
FA616		64-08

BIT		FUNCTION	BIT		OCTAL VALUE	BIT		FUNCTION	BIT		OCTAL VALUE	
9	8	7	6	5	4	9	8	7	6	5	4	
0	0	0	A	0	0	0	0	0	E	0	0	4
		1	B		1	1		1	5			
	1	0	C	1	0	2	1	0	G	1	0	6
		1	D		1	3		1	7			

[50] Determine binary value of bits 15-18 in CREG 36 [Figure 5, Page 10]

[51] Determine if an invalid state exists [TABLE O]

[54] Determine binary value of bits 11-14 in CREG 36 [Figure 5, Page 10]

[55] Determine if an invalid state exists [TABLE Q]

[52] Does an invalid state exist

[53] Obtain list of suspect packs [TABLE P]. Use TOP 234-151-031 to replace SP circuit packs

[56] Does an invalid state exist

[57] Obtain list of suspect packs [TABLE R]. Use TOP 234-151-031 to replace SP circuit packs

[58] See NOTE 4. Replace FA616 pack [TABLE R]. Use TOP 234-151-031 to replace SP circuit packs

TABLE O INVALID DIAL PULSE SEQUENCER STATES				
BITS				STATE
18	17	16	15	INVALID STATE
1	1	0	0	
			1	
		1	0	
			1	

TABLE P FS14 CIRCUIT PACKS	
PACK TYPE	LOCATION
	SP-1 COMBINED MATRIX
FA577	60-16
FA576	60-14,13,12
FA621	60-11
FA602	60-10
FA588	64-23
FA616	64-08

TABLE Q INVALID MF OUT SEQUENCER STATES				
BIT				STATE
14	13	12	11	INVALID STATE
1	1	0	1	
		0	0	
		1	1	
		1	0	
			1	

TABLE R MF OUT SEQUENCER SP-1/COMBINED MATRIX PACKS	
PACK TYPE	LOCATION
FA615	64-04
FA614	64-05
FA588	64-23
FA577	64-06
FA581	64-07
FA616	64-08

NOTE 4
If trouble does not clear, mate sequencers should be checked for invalid state

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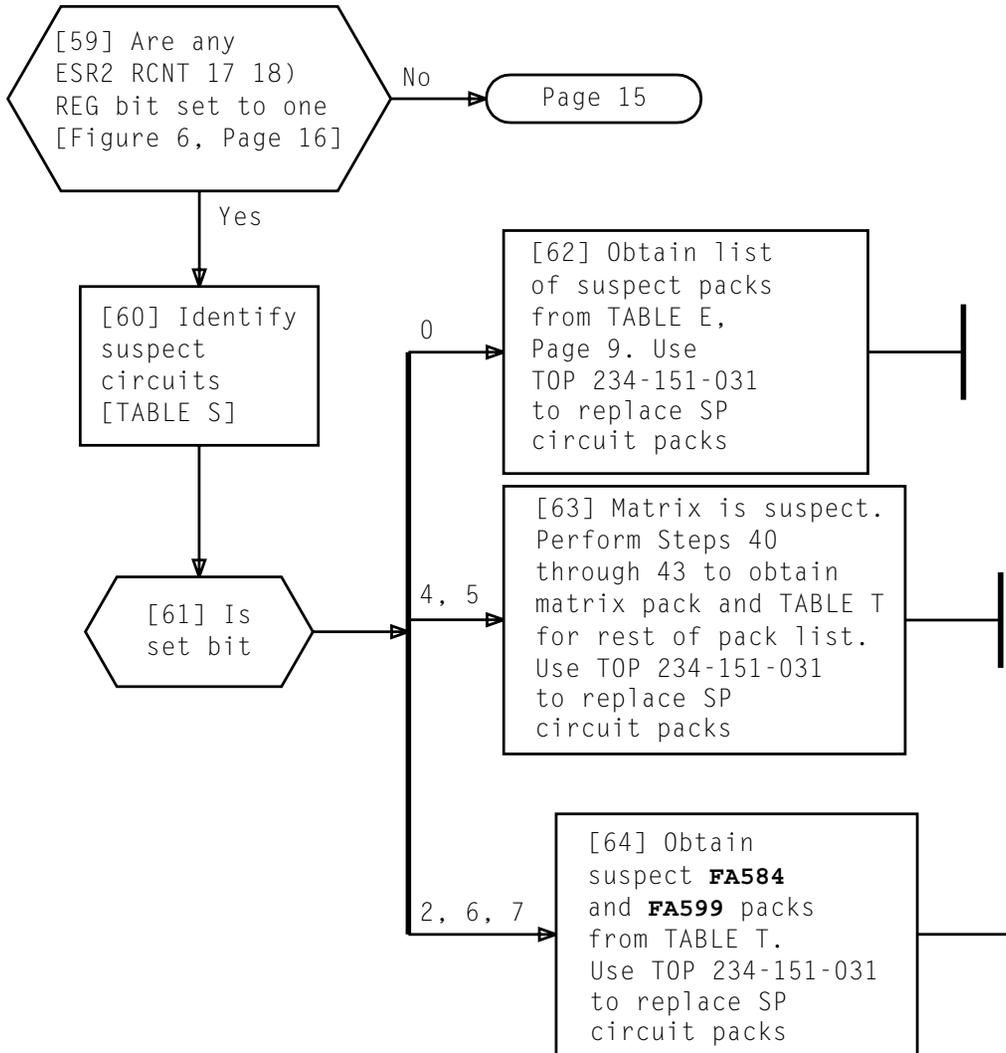
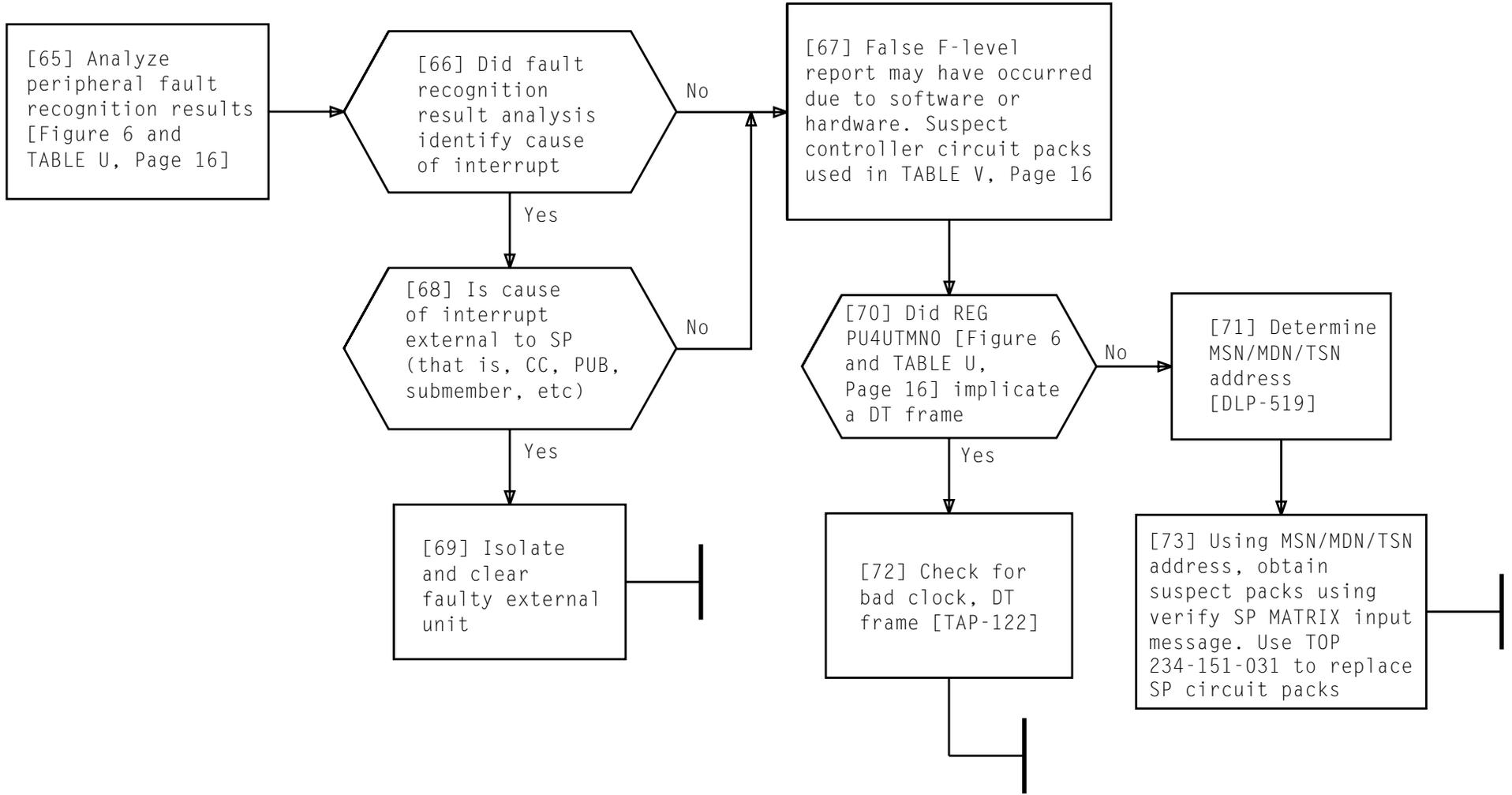


TABLE S			
USING INFORMATION FROM TABLE D, RELATIONSHIP TO CIRCUIT WHICH CAUSED ESR BIT TO BE SET CAN BE FOUND IN SD-4A013 USING CHART BELOW			
ESR2 BIT	NET NAME	SOURCE FS/SYMBOL	COMMENTS
0	PUSOT00	17/8	PU sequencer time-out
1	-	-	-
2	WNEWIO	10/3	Matrix work-work register mismatch
3	-	-	-
4	MXTASWFO	10/26	Matrix ASW failure
5	MXTHOM00	10/27	Matrix homogeneity failure
6	HNEHEO	10/3	Matrix hold-hold register mismatch
7	MXWNCHO	10/10	Matrix work-hold register mismatch
8	-	-	-

TABLE T			
BIT 4, 5 SUSPECT PACK LIST			
SP-1		COMBINED MATRIX	
PACK TYPE	LOCATION	PACK TYPE	LOCATION
FA584	56-18, 17, 16, 14	FA584	56-18, 17, 16, 14
FA599	56-26, 25, 24	FA599	56-26, 25, 24
FA590	56-19, 20, 21, 22	FA1239	56-19, 20, 21, 22
FA587	56-11	FA1238	56-11
FA597	56-13	FA1241	56-13
FA596	56-12	FA1240	56-12

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**TABLE U
PERIPHERAL FAULT RECOGNITION RESULTS**

IDENTIFICATION OF REGISTERS IN RESULTS
TABLE OF F-LEVEL MESSAGE

```

PU4RESULT  PU4UTMNO  PU4FRPMD  PU4FRJRG
PU4RESULT  -----NMLKJIHGFEDCBA
Bit    0   A = CCO found faulty
       1   B = CC1 found faulty
       2   C = Controller 0 found faulty
       3   D = Controller 1 found faulty
       4   E = PU bus 0 found faulty
       5   F = PU bus 1 found faulty
       6   G = PU bus 0 at unit found faulty
       7   H = PU bus 1 at unit found faulty
       8   I = Faulty unit or subunit to be removed and
           diagnosed
       9   J = Faulty unit or subunit to be removed
      10   K = Fault recognition was unable to find the fault
      11   L = Fault recognition found that a software error
           caused the F-level
      12   M = Fault recognition found that a transient
           caused the F-level
      13   N = Signal processor matrix found faulty

PU4UTMNO   DDDDDDDCCCCCBBAAAAAA--
Bits  2-8  A = Submember found faulty (if any)
       9   B = Set if submember found faulty
      10-16 C = Member number found faulty
      17-23 D = Unit type found faulty

PU4FRPMD   --CCCCCBBBBBBBAAAAAAA
Bits  0-7  A = Point of maximum definition MACRO number
           relative to an FR program
       8-14 B = Fault recognition decision code
      15-21 C = Error analysis action code

PU4FRJRG = FR program address where error was located
    
```

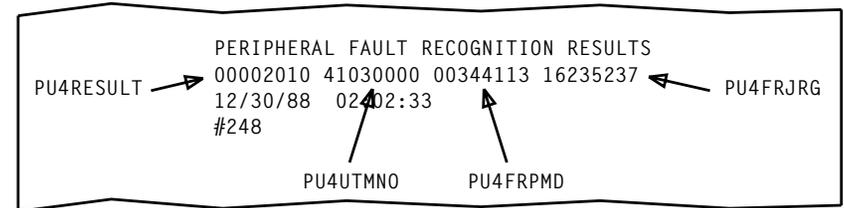
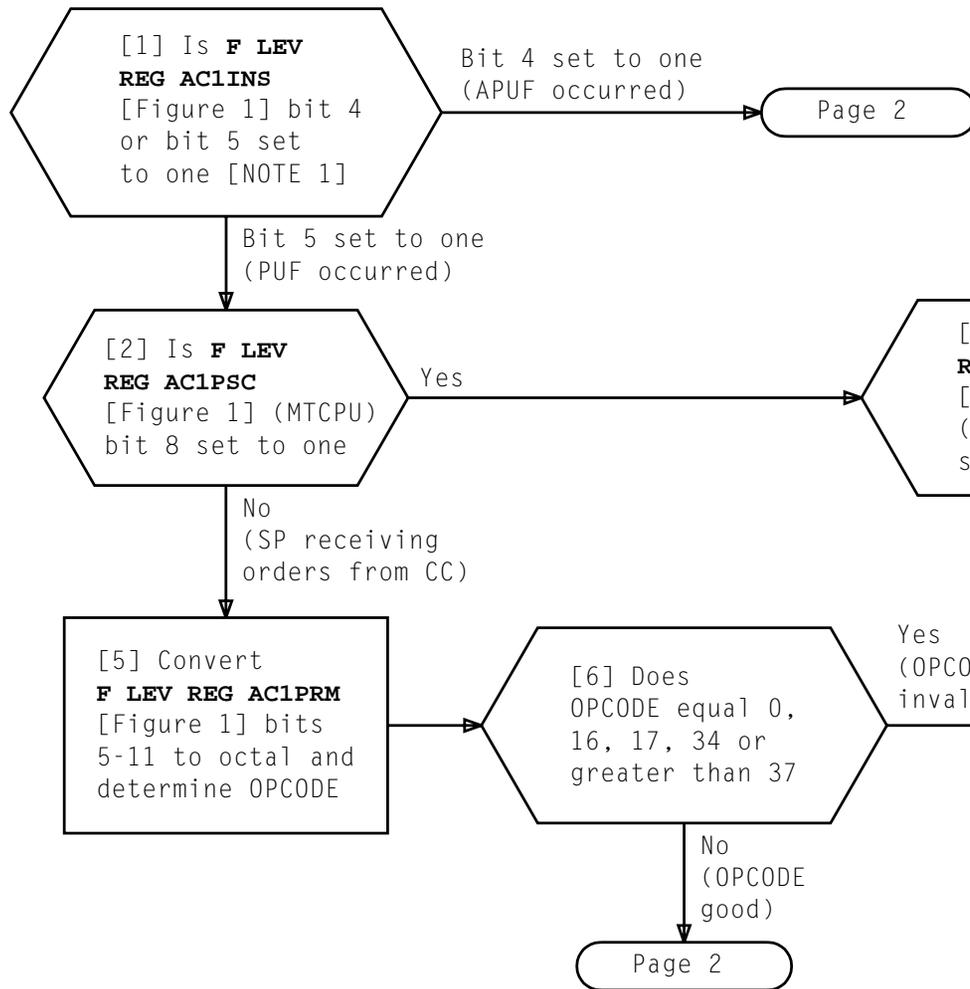


Figure 6 - Peripheral Fault Recognition Results Printout

TABLE V SP CONTROLLER PACKS		
	PACK	LOCATION
4A013 (FS19)	FA617	68-07
	FA529	72-26



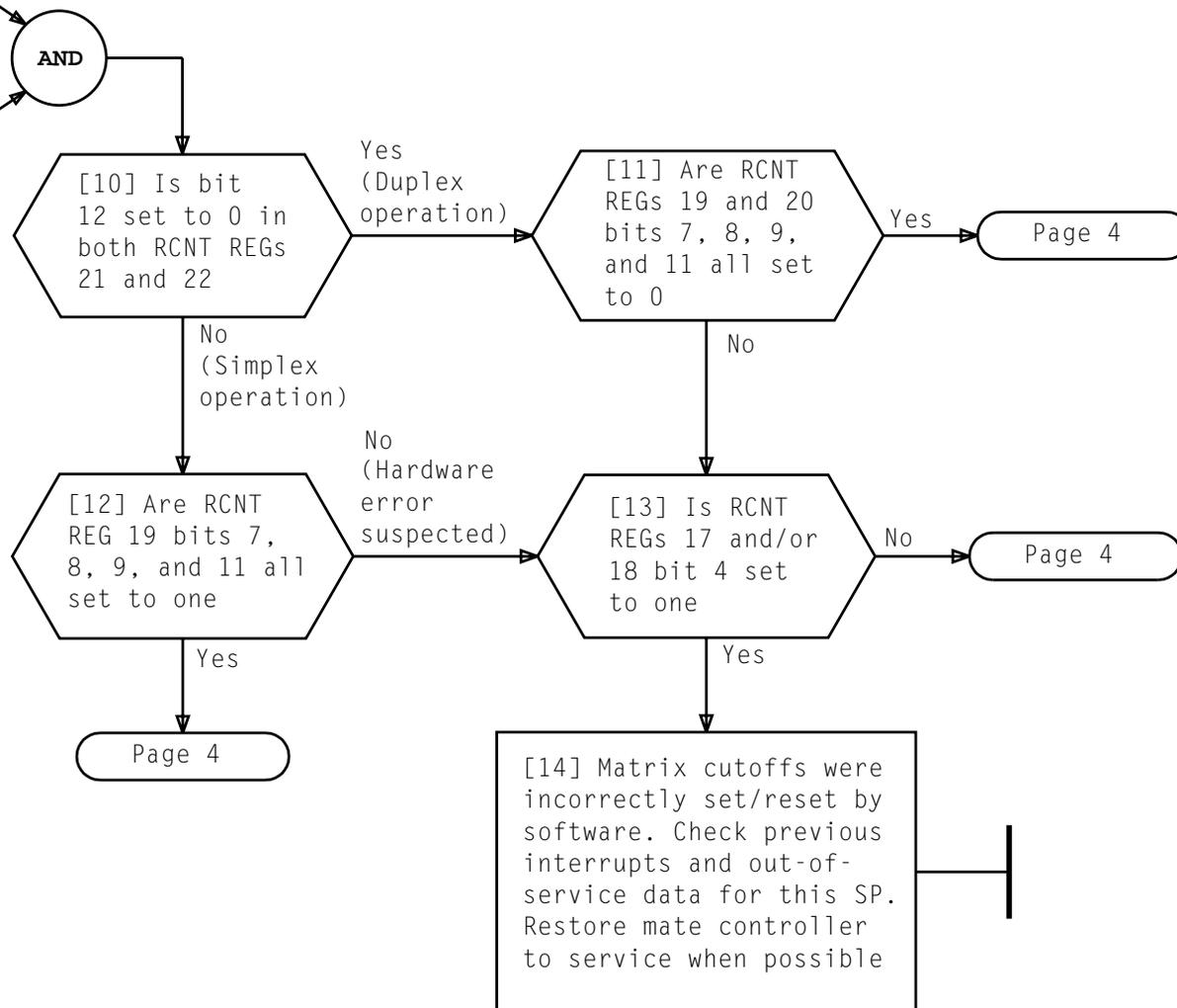
SPFR RESTORED SP 12 CONTR 1					
F-LEVEL					
AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASF(H)	AC1ASF(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1LR	
AC1PSQ	AC1ULR	AC1PES	ST1PES	ST1ER	ST1PRM
ST1PRL	ST1PSC	AC1RP0/	AC1RP1	ST1RP0	ST1RP1
ST1CSC	ST1INH	PU1RFLC00/	PU1RFLC01	PU1RFLC02	PU1RFLC03
PU1RFLC04	PU1RFLC05	PU1RFLC06	PU1RFLC07		

Figure 1 - F-Level Register Printout

NOTES	
1. If both bits are set, PUF path should be used	
2. If this interrupt repeats, software should be suspect and Technical Assistance Center notified	
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[8] Determine which controller is suspect. RCNT REG 0 [Figure 2, Page 3] bit 0 indicates which controller is suspect

[9] Determine hardware and software status as indicated by RCNT 19-22 register bits 0-6 [Figure 2, and TABLE A, Page 3]



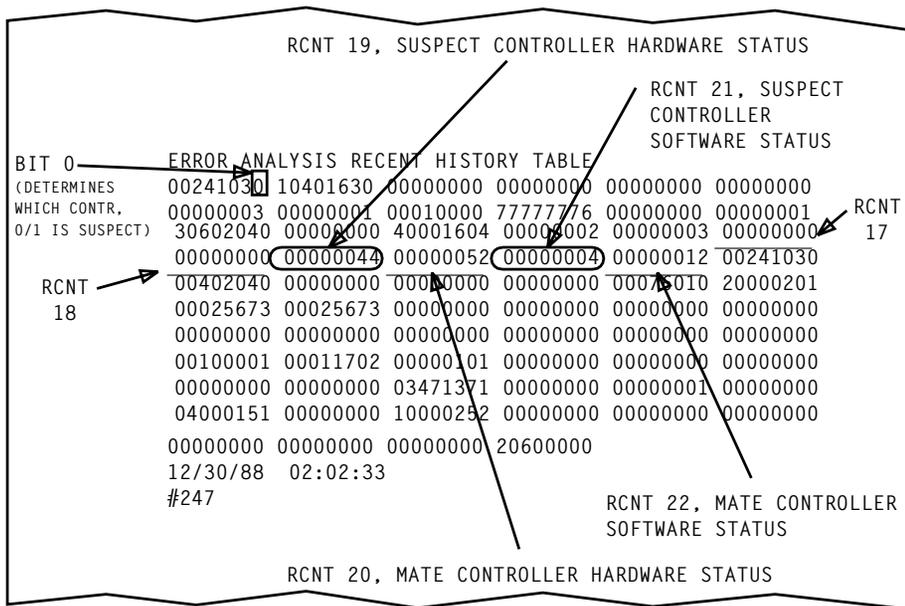
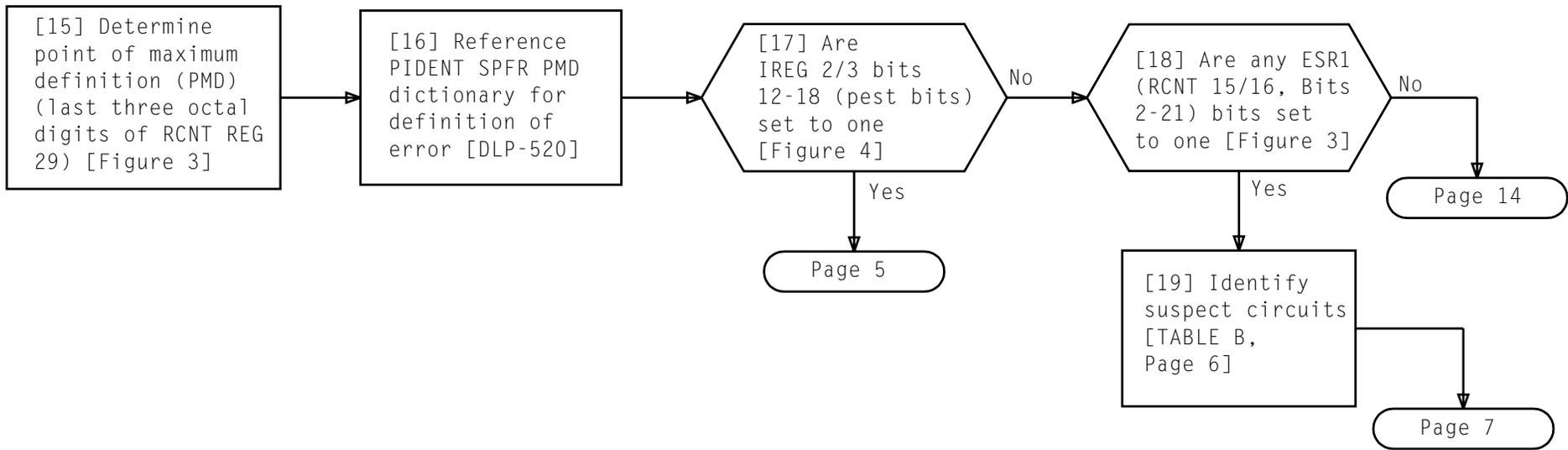


Figure 2 - RCNT Register Printout

TABLE A RCNT 19-22, HARDWARE/SOFTWARE STATUS			
BIT	NAME	STATE	IMPLICATION
0	MA	0	Operational mode
		1	Maintenance mode
1	R0	0	Receiving on Bus 0
		1	Receiving on Bus 1
2	S0	0	Not sending on Bus 0
		1	Sending on Bus 0
3	S1	0	Not sending on Bus 1
		1	Sending on Bus 1
4	DIV	0	DUPLEX
		1	SIMPLEX - should be set in both controllers
*5	STOP	0	SP not stopped
		1	Stopped for out-of-service or interrupt (only set in out-of-service controller in hardware status)
6	CA	0	Using clock from controller 0
		1	Using clock from controller 1 Both controllers should be using the same clock. If the frame is SIMPLEX, it should be the in-service controller

*Bit 5 (RCNT REGs 19 and 20) is always set on an F-level interrupt printout

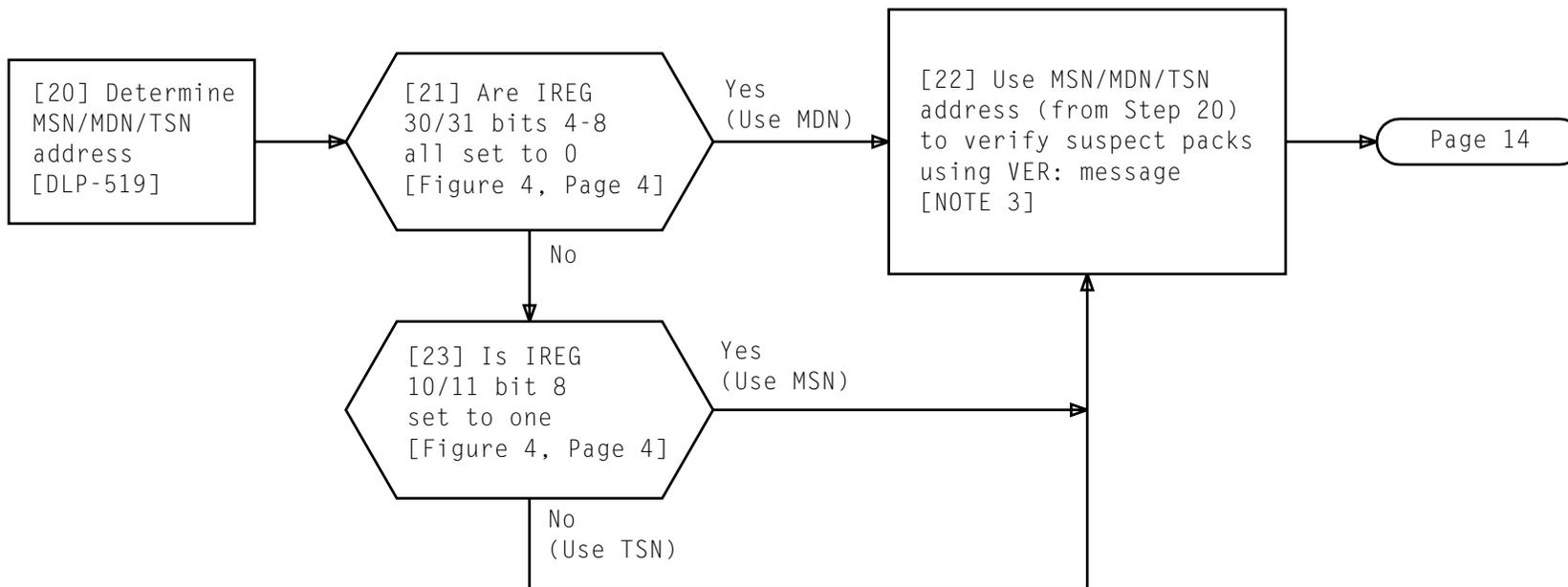


RCNT 15 ESR 1 REG SUSPECT	RCNT 16 ESR 1 REG MATE	PMD NUMBER	
ERROR ANALYSIS RECENT HISTORY TABLE			
00241030	10401630	00000000	00000000
00000003	00000001	00010000	77777776
30602040	00000000	40001604	00000004
00402040	00000044	00000052	00000000
00422040	00000000	00000000	00076010
00025673	00025673	00000000	00000000
00000000	00000000	00000000	00000000
00100001	00011702	00000101	00000000
00000000	00000000	03471371	00000001
04000151	00000000	10000252	00000000
00000000	00000000	00000000	20600000
12/30/88	02:02:33		
#247			

Figure 3 - RCNT Register Printout

IREG 2	IREG 3	IREG 10	IREG 11
SP INTERNAL REGISTERS			
00000000	00000000	00000000	00002640
00000000	05620243	00000000	00002377
00000000	00000000	00000000	00000000
00000000	77777777	00000000	77770000
00000000	00000000	00000000	42424242
00000000	60406000	00000000	50027704
00000000	60406000	00000000	00000000
00000000	46200000	00000000	60406000
00000000	00070007	00000000	00054406
00000000	00000000	00002525	00000000
37403740	37403740	37133703	37133703
00000000	37473747	00000000	34003400
00000000	00000000	00000000	32443244
00000000	00000000	00000000	25252525
00000000	00000000	00000000	00000000
00000000	77777777	00000000	77777777
00000000	00006067	00000000	00000001
00000000	01246033	00000000	00007740
00000000	00000000	00000000	00000000
00000000	35160400	00000000	00000000
00000000	13600000	00000000	01404043
			02500200
			34200252

Figure 4 - SP Internal Register (IREG) Printout

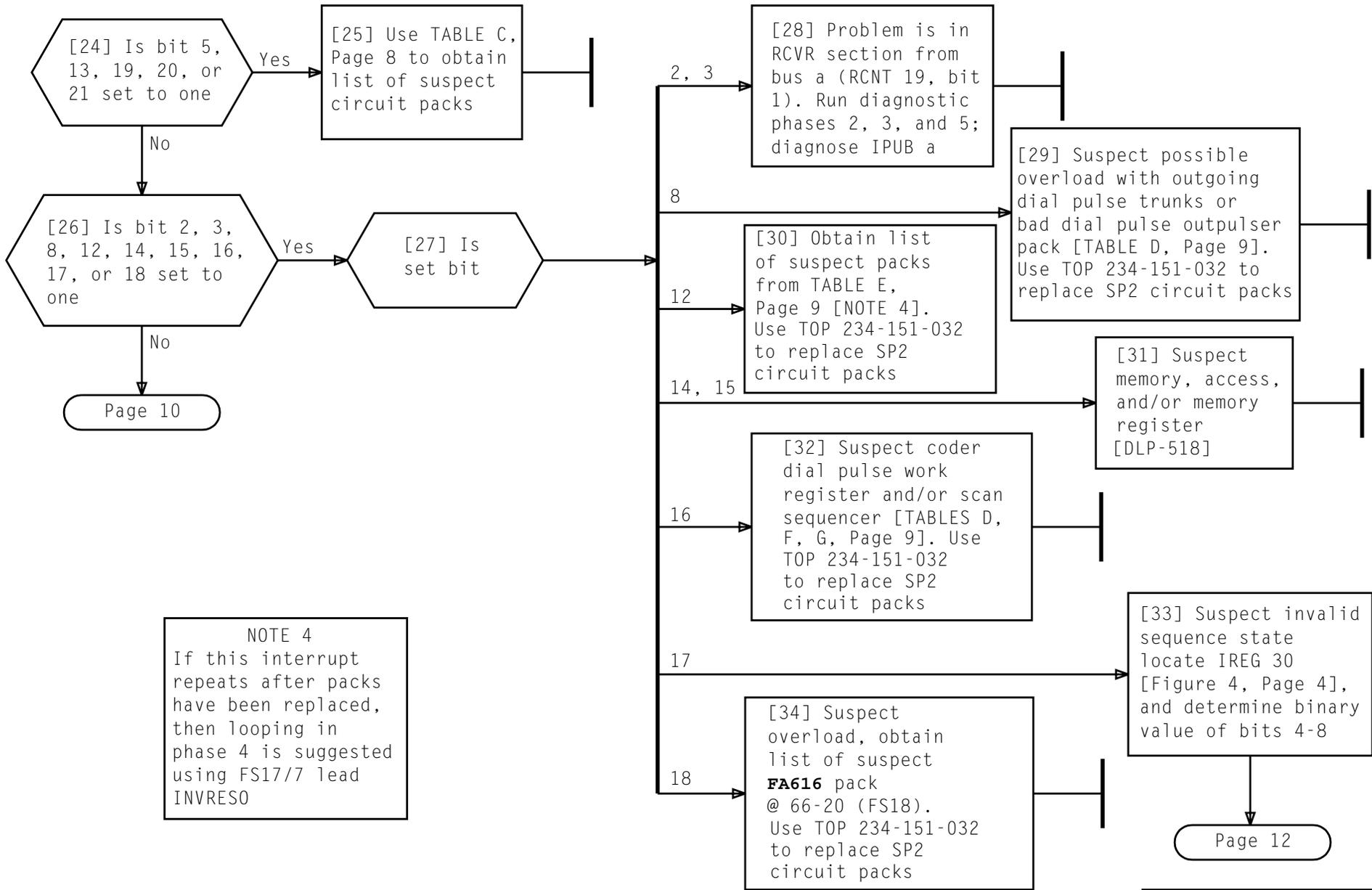


NOTE 3	
An SP-2 may have an associated pack not identified by verify message	
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TABLE B			
ESR 1 (RCNT 15 AND 16)			
PACKS IMPLICATED BY ESR BITS CAN BE FOUND IN SD-4A067 USING CHART BELOW			
ESR1 BIT	NET NAME	SOURCE FS/SYMBOL	COMMENTS
0	SASWF0	19/10	Directed order failure
1	SATNT0	19/10	Autonomous failure
2	PARE1	1/9	PU bus input parity fail
3	PAR01	1/11	PU bus input parity fail
4	INTJOA	19/24	Interject
5	TROUT0	20/3	Analog timer time-out
6	MXTADRM0	10/14	Matrix address register mismatch
7	RBRMM0	2/9	Reply bus register mismatch
8	DPOLF0	16/3	DP out worklist overflow
9	-	-	-
10	SEQMM0	10/1	Autonomous sequencer mismatch
11	MRMM0	8/11	Memory register mismatch
12	INVRES0	17/6	Invalid OPCODE
13	DETOUT1 CCERRO	20/3 20/6	Level detector error Clock error
14	MRP1ER0	8/3	Memory parity 1
15	MRP2ER0	8/4	Memory parity 2
16	GTH0	14/5	Coder greater than DPWR
17	SQINVS0	10/1	Sequencer invalid state
18	SANTT00	18/2	Executive sequencer sanity error
19	XMCLER0	20/12	Extended MS clock error
20	CLKMM0	20/9	Ring counters mismatch
21	DPRWER0	12/10	Missing DP in end-of-list flag
22	-	-	-
23	-	-	-

ANALYZE SP2 F-LEVEL INTERRUPT

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NOTE 4
 If this interrupt repeats after packs have been replaced, then looping in phase 4 is suggested using FS17/7 lead INVRESO

ANALYZE SP2 F-LEVEL INTERRUPT

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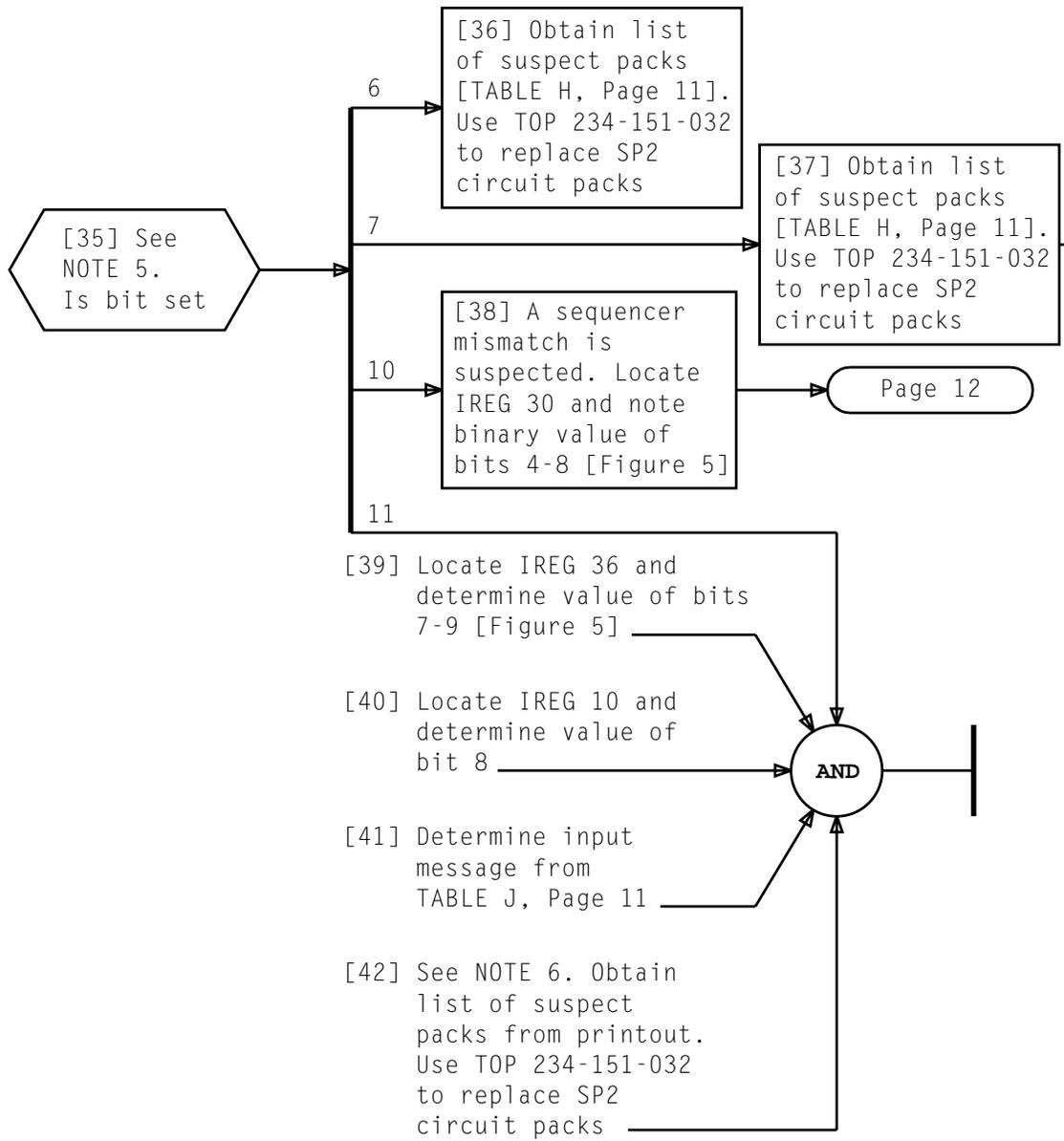
TABLE C			
ESR1 SUSPECT PACKS/ACTION			
ESR BIT	SP-2		COMMENTS/RECOMMENDED PROCEDURE
	PACK TYPE	LOCATION	
2,3	-	-	Problem in RCVR section from BUS a (RCNT 19, bit 1); run DGN phases 2, 3, and 5/DGN:IPUB a
5	FB002 FB001 FA668	62-12 62-11 66-14	
8	-	-	Possible overloaded outgoing dial pulse trunks or bad FS14 circuit pack
12	-	-	Check lead INVRES0 (FS17/7) if pack replacement does not solve problem
13, *20	FA663 FB002 FB003 FA664 FB001	66-12 62-12 66-10 66-11 62-11	
14,15	-	-	Perform memory pack procedure [DLP-518]
16	-	-	Suspect coder (FS13) dial pulse work reg (FS14) and/or scan sequencer (FS12)
17	-	-	Check for invalid sequencer state
18	-	-	Possible SP overload (not serving offered load) suspect executive sequencer circuit packs (FS18)
19	FA575	58-34	
21	FA577 FA588	66-32,34,31 66-41	Also, suspect scan sequencer circuit packs (FS12)
* Bad pack could be in either controller			

TABLE D FS14 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA577	62-14
FA576	62-20, 21, 23
FA621	62-22
FA620	62-19
FA588	66-40

TABLE E FS17 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA1195	74-26
FA619	74-29
FA618	74-31
FA604	74-32
FA583	74-38
FA525	74-43
FA603	74-37
FA599	74-13
FA1194	74-25

TABLE F FS12 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA1245	62-16
FA602	62-22
FA591	66-24
FA600	66-18
FA613	66-21
FA589	66-16
FA1246	62-15
FA598	62-17
FA601	66-15
FA621	66-22

TABLE G FS13 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA576	62-20, 21, 23



IREG 10

SP INTERNAL REGISTERS					
00000000	00000000	00000000	00000000	00000000	00002640
00000000	05620243	00000000	00002377	00000000	00000517
00000000	00000000	00000000	00000000	00000000	00000000
00000000	77777777	00000000	77770000	00000000	42424242
00000000	00000000	00000000	50027704	00000000	50027704
00000000	60406000	00000000	00000000	00000000	60406000
00000000	46200000	00000000	46200000	00000000	00054406
00000000	00070007	00000000	00002525	00000000	37523752
37403740	37403740	37133703	37133703	34003400	34003400
00000000	37473747	00000000	32443244	00000000	77777777
00000000	00000000	00000000	25252525	00000000	52525252
00000000	00000000	00000000	00000000	00000000	00000000
00000000	77777777	00000000	77777777	00000000	00000001
00000000	00006067	00000000	00007740	00000000	02500200
00000000	01246033	00000000	00200000	00000000	01404043
00000000	35160400	00000000	00000000	00000000	34200252
00000000	13600000				

IREG 30 points to the 4th column of the table.
IREG 36 points to the 2nd column of the table.

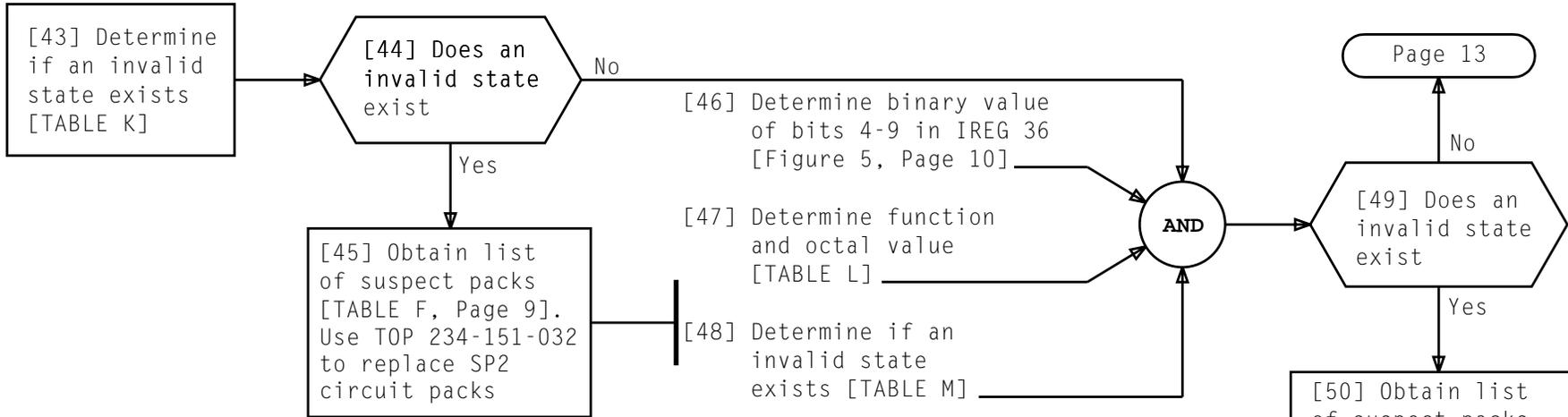
Figure 5 - SP Internal Register (IREG) Printout

NOTES	
5. Bad pack could be in either controller	
6. An SP-2 may have an associated pack not identified by verify message	
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TABLE H FS10 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA590	66-06,07,08,09
FA1191	70-14
FA1192	70-13
FA1193	70-12
FA584	70-08,09,10,11
FA599	70-06,07

TABLE I FS 2 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA531	74-14,15
FA534	74-16
FA528	74-27,24,22,23 74-19,21,17,20

TABLE J VERIFY MESSAGES		
CREG 36 BITS 7-9 VALUE	CREG 10 BIT 8 VALUE	USE VERIFY MESSAGE
0	0	VER:SPMTXPK:SCP,TSN o'0!
0	1	VER:SPMTXPK:SCP,MSN o'0!
≠ 0	0	VER:SPMTXPK:SDM,TDN o'0!
≠ 0	1	VER:SPMTXPK:SDM,MDN o'0!



BIT	8	7	6	5	4
V A L U E	1	0	0	0	0
			1	0	0
		1	0	1	0
			1	1	1
	1	0	1	0	0
				1	1
		1	0	1	0
			1	0	1

F U N C T I O N	OCTAL VALUE							
	0	1	2	3	4	5	6	7
A				†	†	†		
B				†	†	†		
C								
D								
E			†	†				
F	†	†	†	†	†	†	†	†
G								
H			†	†				

BIT		FUNCTION	BIT		OCTAL VALUE	BIT		FUNCTION	BIT		OCTAL VALUE	
9	8	7	6	5	4	9	8	7	6	5	4	
0	0	0	A	0	0	0	1	0	E	1	0	4
		1	B		0	1		1	5			
	1	0	C	1	0	2	1	0	G	1	0	6
		1	D		1	3		1	7			

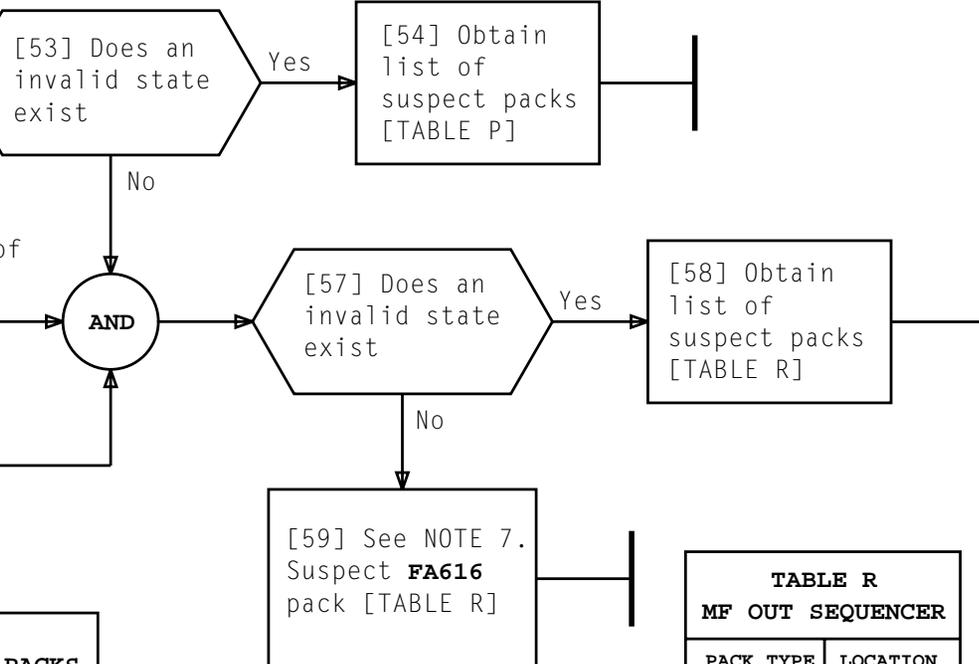
PACK TYPE	LOCATION
FA1191	70-14
FA1192	70-13
FA1193	70-12
FA599	70-06, 07
FA599	74-13
FA616	66-20

[51] Determine binary value of bits 15-18 in IREG 36 [Figure 5, Page 10]

[52] Determine if an invalid state exists [TABLE O]

[55] Determine binary value of bits 11-14 in IREG 36 [Figure 5, Page 10]

[56] Determine if an invalid state exists [TABLE Q]



BITS				STATE
18	17	16	15	
1	1	0	0	I
			1	N
		1	0	V
			1	A
				L
				I
				D

PACK TYPE	LOCATION
FA577	62-14
FA576	62-20,21,23
FA621	62-22
FA602	62-19
FA588	66-40
FA616	66-20

BIT				STATE
14	13	12	11	
1	0	1	1	I N V A L I D
			0	
	1	0	1	
			0	
			1	

PACK TYPE	LOCATION
FA666	66-23
FA615	66-19
FA588	66-40
FA577	66-33
FA581	66-30
FA616	66-20

NOTE 7
If trouble does not clear, mate sequencers should be checked for invalid state

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[60] Are any ESR2 (IREG 0/1) REG bit set to one [Figure 6, Page 15]

No

Page 15

Yes

[61] Identify suspect circuits [TABLE S]

[62] Is set bit

0

[63] Obtain list of suspect packs from TABLE E, Page 9. Use TOP 234-151-032 to replace SP2 circuit packs

4, 5

[64] Matrix is suspect. Perform Steps 40 through 43 to obtain matrix pack and TABLE T for rest of pack list. Use TOP 234-151-032 to replace SP2 circuit packs

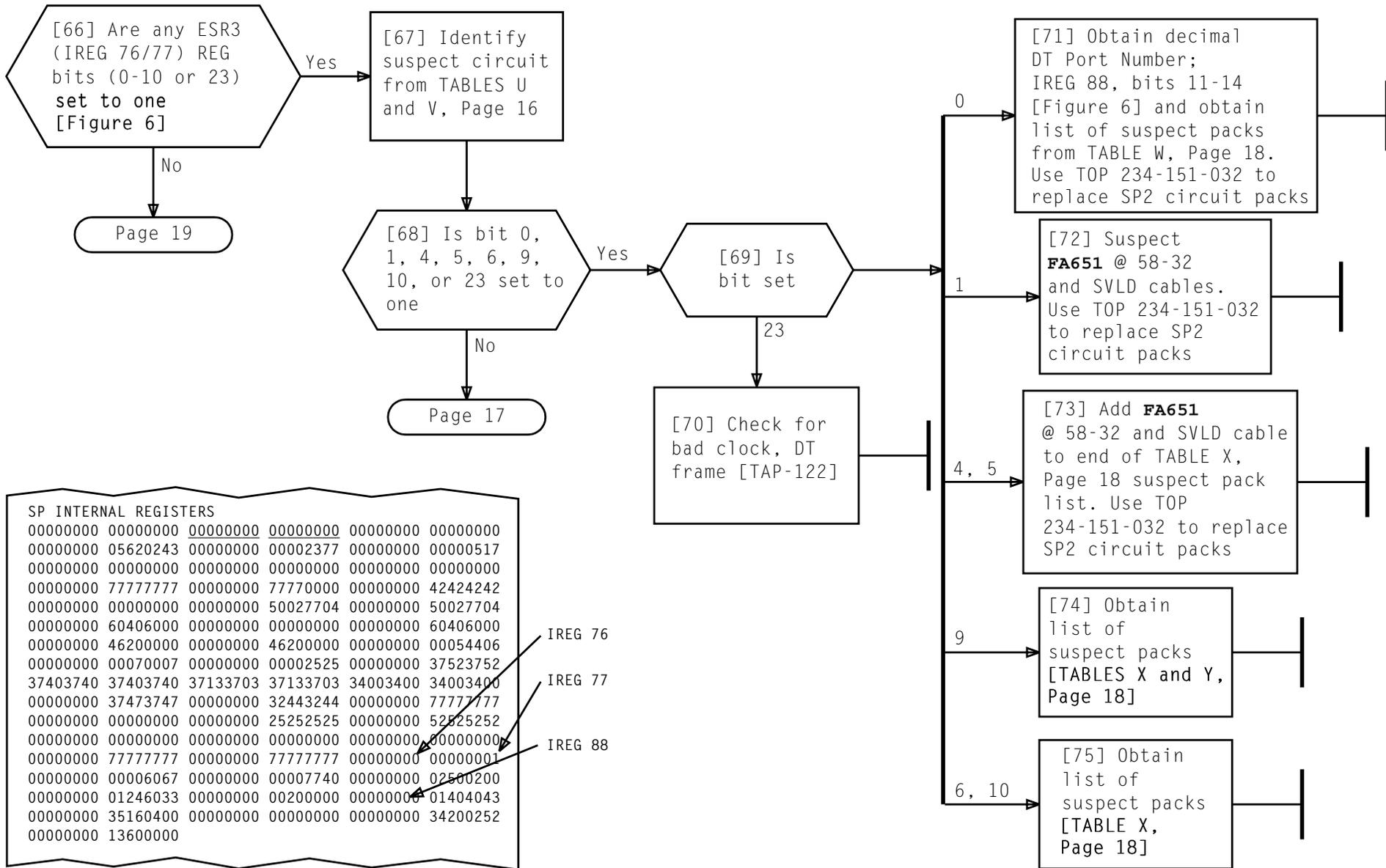
2, 6, 7

[65] Obtain suspect **FA584** and **FA599** packs from TABLE T. Use TOP 234-151-032 to replace SP2 circuit packs

TABLE S			
USING INFORMATION FROM TABLE D, RELATIONSHIP TO CIRCUIT WHICH CAUSED ESR BIT TO BE SET CAN BE FOUND IN SD-4A067 USING CHART BELOW			
ESR2 BIT	NET NAME	SOURCE FS/SYMBOL	COMMENTS
0	PUSOT00	17/8	PU sequencer time-out
1	-	-	-
2	WNEWIO	10/3	Matrix work-work register mismatch
3	-	-	-
4	MXTASWFO	10/26	Matrix ASW failure
5	MXTHOM00	10/27	Matrix homogeneity failure
6	HNEHEO	10/3	Matrix hold-hold register mismatch
7	MXWNCHO	10/10	Matrix work-hold register mismatch
8	-	-	-

TABLE T	
BIT 4, 5 SUSPECT PACK LIST	
PACK TYPE	LOCATION
FA584	70-08, 09, 10, 11
FA599	70-06, 07, 13
FA1191	70-14
FA1192	70-13
FA1193	70-12
FA590	66-06, 07, 08, 09

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SP INTERNAL REGISTERS

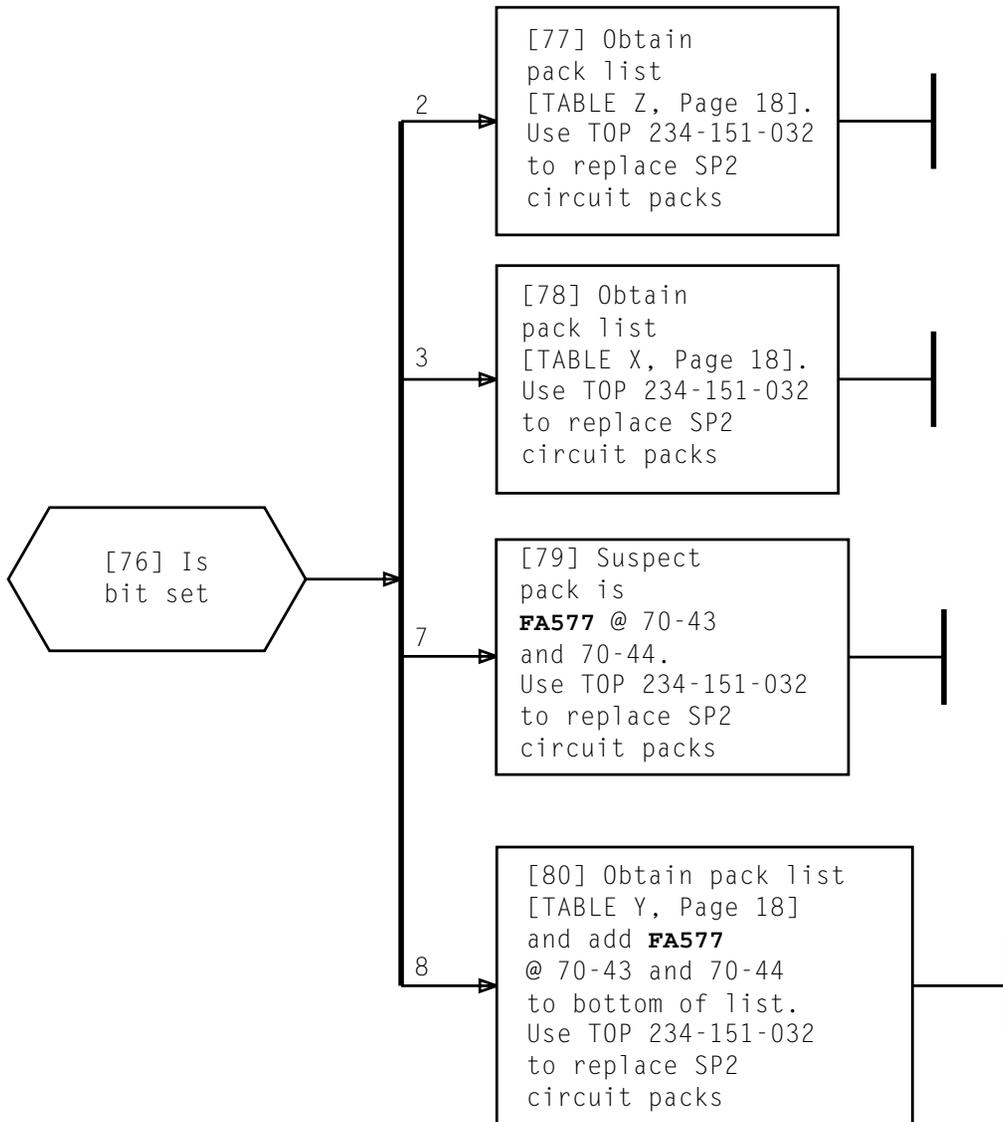
00000000	00000000	00000000	00000000	00000000	00000000
00000000	05620243	00000000	00002377	00000000	00000517
00000000	00000000	00000000	00000000	00000000	00000000
00000000	77777777	00000000	77770000	00000000	42424242
00000000	00000000	00000000	50027704	00000000	50027704
00000000	60406000	00000000	00000000	00000000	60406000
00000000	46200000	00000000	46200000	00000000	00054406
00000000	00070007	00000000	00002525	00000000	37523752
37403740	37403740	37133703	37133703	34003400	34003400
00000000	37473747	00000000	32443244	00000000	77777777
00000000	00000000	00000000	25252525	00000000	52525252
00000000	00000000	00000000	00000000	00000000	00000000
00000000	77777777	00000000	77777777	00000000	00000001
00000000	00006067	00000000	00007740	00000000	02500200
00000000	01246033	00000000	00200000	00000000	01404043
00000000	35160400	00000000	00000000	00000000	34200252
00000000	13600000				

IREG 76
IREG 77
IREG 88

Figure 6 - SP Internal Register (IREG) Printout

TABLE U ESR3 - (SP-2 ONLY) IREG 76 AND 77		
BIT	NAME	IMPLICATION
0	TOK	The DT that this SP-2 was linked to had a transmitter failure
1	DTOCER	The DT the SP-2 was linked to sent an invalid OP CODE
2	MSGSEQMM	Message sequencers mismatched. Suspect the message sequencer circuit
3	DTPSEQMM	The I/O sequencers mismatched. Suspect I/O sequencer circuit
4	DTBITER	Lost a bit timing from this DT
5	DTRMER	Lost frame timing from DT
6	DTSAN	SP-2 did not process all DTs in time. Suspect loss of timing from DT
7	DTSERMM	Outgoing (to DT) data reclock registers mismatched. Suspect bad shift register.
8	DTSRMM	The shift registers between controllers mismatched. Suspect shift register or memory path
9	PARER	Parity error on incoming DT data
10	DTPCST	I/O sequencer in an invalid state

TABLE V USING INFORMATION FROM TABLE F, RELATIONSHIP TO CIRCUIT WHICH CAUSED ESR BIT TO BE SET CAN BE FOUND IN SD-4A067 USING CHART BELOW			
ESR3 BIT	NAME	FS/SYMBOL	COMMENTS
2	MSGSEQMM	25/4	Message storage sequencer mismatch
3	DTPSEQMM	23/1-4 22/9 20/8	I/O sequencer mismatch
7	DTSERMM	23/15 23/13	Serial reclock register mismatch
8	DTSRMM	23/15 24/1-16,20-29	Shift register mismatch
10	DTPCST	23/1.2	I/O sequencer in invalid state



ANALYZE SP2 F-LEVEL INTERRUPT

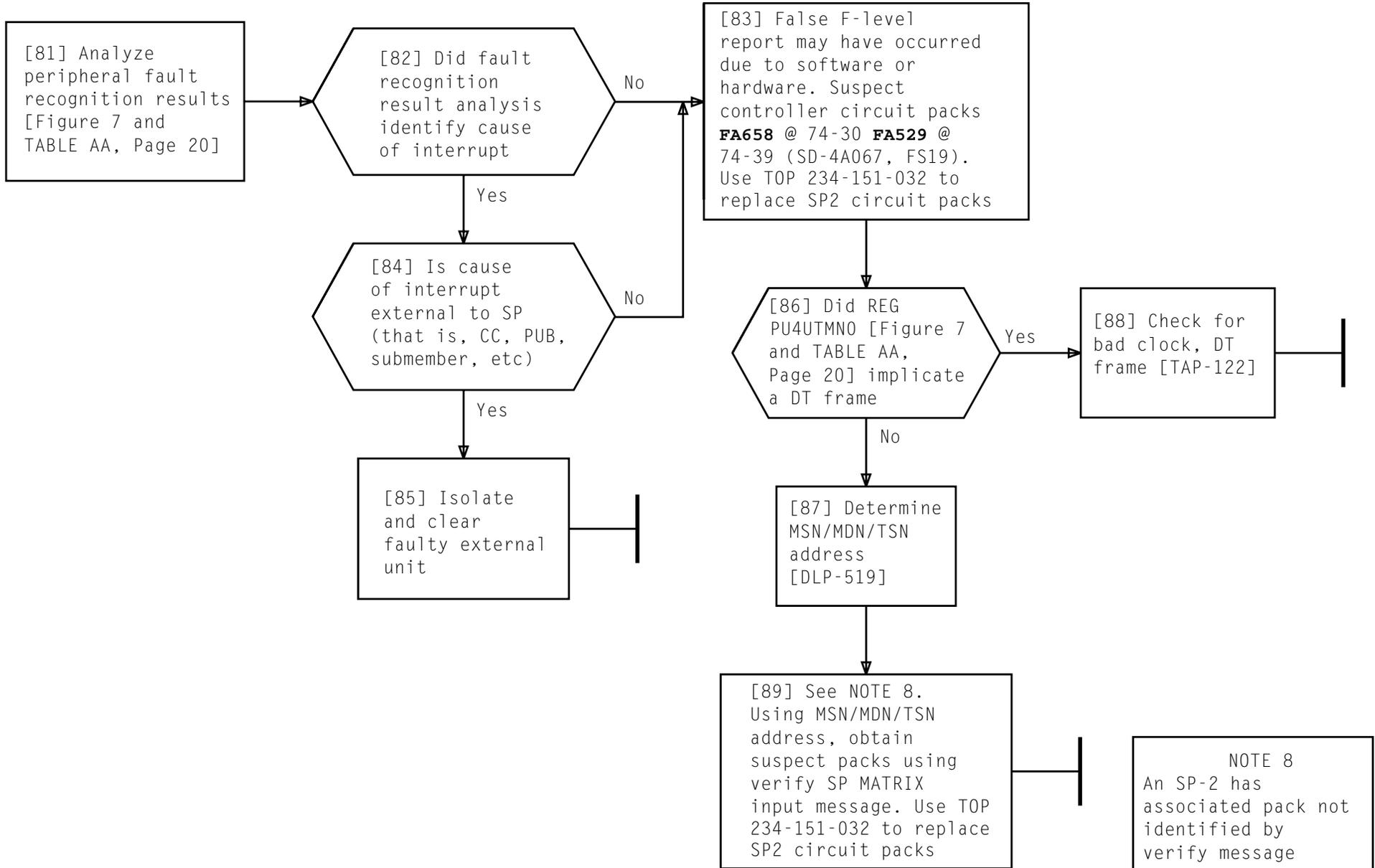
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TABLE W FS22 CIRCUIT PACKS																
PORTS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PACK TYPE	LOCATIONS*															
FA524	13	12	11	10	22	21	20	19	49	48	47	46	60	59	58	57
FA533	16 (C1 DRIVER) 15 (C0 DRIVER)				25 (C1 DRIVER) 24 (C0 DRIVER)				52 (C1 DRIVER) 51 (C0 DRIVER)				63 (C1 DRIVER) 62 (C0 DRIVER)			
FA649	14 (SWITCH DRIVER)				23 (SWITCH DRIVER)				50 (SWITCH DRIVER)				61 (SWITCH DRIVER)			
* All packs in vertical location 58																

TABLE X FS23 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA654	58-28
FA650	62-41
FA656	58-31
FA657	58-27
FA577	70-43,44

TABLE Y FS24 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA1196	66-50,49,43,42
FA650	62-41
FA531	66-51
FA531	62-44

TABLE Z FS25 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA652	58-29
FA655	58-26
FA653	58-30
FA651	58-32



ANALYZE SP2 F-LEVEL INTERRUPT

NOTE 8	
An SP-2 has associated pack not identified by verify message	
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**TABLE AA
PERIPHERAL FAULT RECOGNITION RESULTS**

**IDENTIFICATION OF REGISTERS IN RESULTS
TABLE OF F-LEVEL MESSAGE**

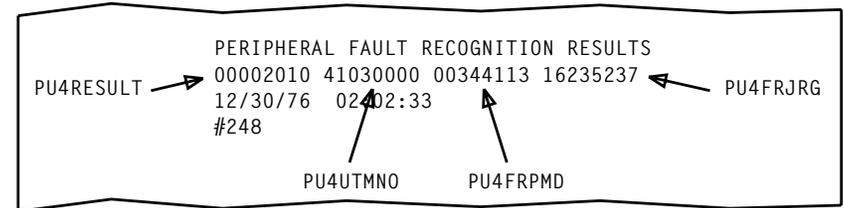
```

PU4RESULT  PU4UTMNO  PU4FRPMD  PU4FRJRG
PU4RESULT  -----NMLKJIHGFEDCBA
Bit   0   A = CCO found faulty
      1   B = CC1 found faulty
      2   C = Controller 0 found faulty
      3   D = Controller 1 found faulty
      4   E = PU bus 0 found faulty
      5   F = PU bus 1 found faulty
      6   G = PU bus 0 at unit found faulty
      7   H = PU bus 1 at unit found faulty
      8   I = Faulty unit or subunit to be removed and
           diagnosed
      9   J = Faulty unit or subunit to be removed
     10   K = Fault recognition was unable to find the fault
     11   L = Fault recognition found that a software error
           caused the F-level
     12   M = Fault recognition found that a transient
           caused the F-level
     13   N = Signal processor matrix found faulty

PU4UTMNO   DDDDDDDCCCCCBBAAAAAA--
Bits  2-8  A = Submember found faulty (if any)
      9    B = Set if submember found faulty
     10-16 C = Member number found faulty
     17-23 D = Unit type found faulty

PU4FRPMD   --CCCCCBBBBBBBAAAAAAA
Bits  0-7  A = Point of maximum definition MACRO number
           relative to an FR program
      8-14 B = Fault recognition decision code
     15-21 C = Error analysis action code

PU4FRJRG = FR program address where error was located
    
```



**Figure 7 - Peripheral Fault Recognition
Results Printout**

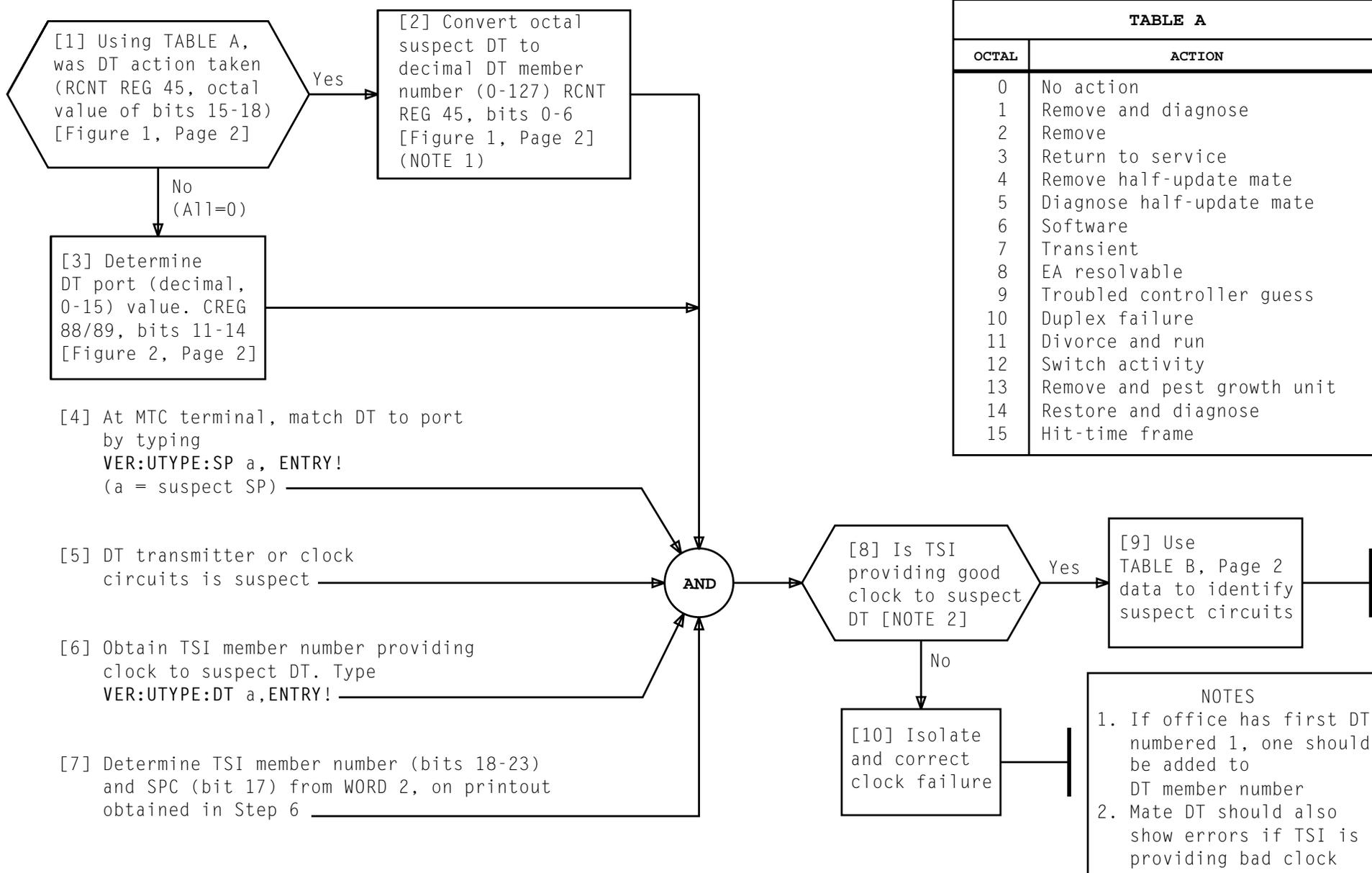


TABLE A	
OCTAL	ACTION
0	No action
1	Remove and diagnose
2	Remove
3	Return to service
4	Remove half-update mate
5	Diagnose half-update mate
6	Software
7	Transient
8	EA resolvable
9	Troubled controller guess
10	Duplex failure
11	Divorce and run
12	Switch activity
13	Remove and pest growth unit
14	Restore and diagnose
15	Hit-time frame

NOTES

1. If office has first DT numbered 1, one should be added to DT member number
2. Mate DT should also show errors if TSI is providing bad clock

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RCNT 1

```

ERROR ANALYSIS RECENT HISTORY TABLE
00241030 10401630 00000000 00000000 00000000 00000000
00000003 00000001 00010000 77777776 00000000 00000001
30602040 00000000 40001604 00000002 00000003 00000000
00000000 00000044 00000052 00000004 00000012 00241030
00402040 00000000 00000000 00000000 00076010 20000201
00025673 00025673 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00100001 00011702 00000101 00000000 00000000 00000000
00000000 00000000 03471371 00000000 00000001 00000000
04000151 00000000 10000252 00000000 00000000 00000000
00000000 00000000 00000000 20600000
12/30/88 02:02:33
#247

```

RCNT 45

Figure 1 - RCNT Register Printout

```

SP INTERNAL REGISTERS
00000000 00000000 00000000 00000000 00002640
00000000 05620243 00000000 00002377 00000000 00000517
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 77777777 00000000 77770000 00000000 42424242
00000000 00000000 00000000 50027704 00000000 50027704
00000000 60406000 00000000 00000000 00000000 60406000
00000000 46200000 00000000 46200000 00000000 00054406
00000000 00070007 00000000 00002525 00000000 37523752
00000000 37473747 00000000 32443244 00000000 77777777
00000000 00000000 00000000 25252525 00000000 52525252
00000000 00000000 00000000 00000000 00000000 00000000
00000000 77777777 00000000 77777777 00000000 00000001
00000000 00006067 00000000 00007740 00000000 02500206
00000000 01246033 00000000 00200000 00000000 01404043
00000000 35160400 00000000 00000000 00000000 34200252
00000000 13600000

```

CREG 88

CREG 89

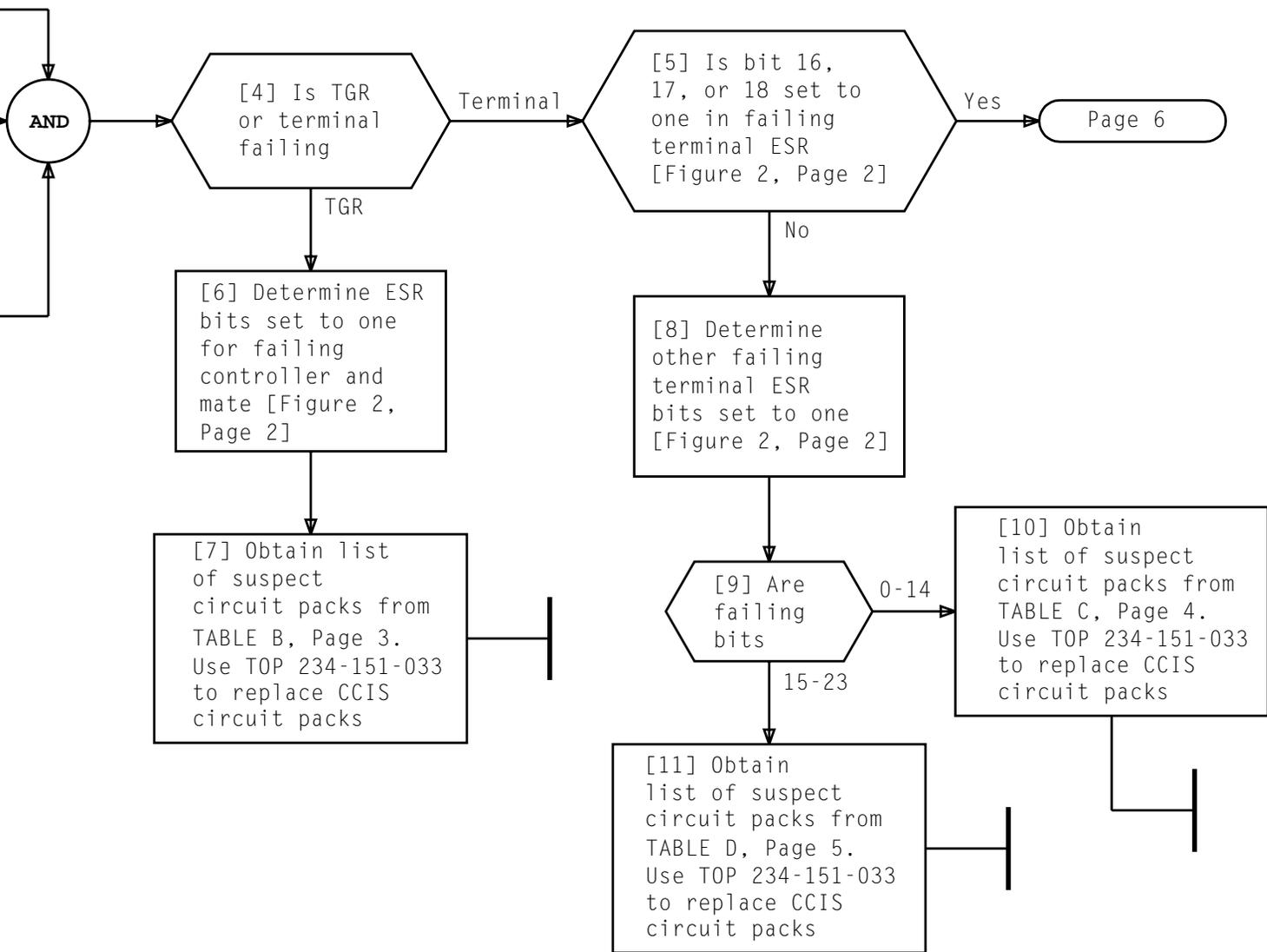
Figure 2 - SP Critical Register (CREG) Printout

TABLE B DT SUSPECT CIRCUITS				
USING ESR3 INFORMATION IMPLICATING DT, SUSPECT CIRCUIT CAN BE FOUND				
ESR3 BIT	LEAD NAME	DT SD-6G114 FS/SYMBOL	SP2 SD-4A067 FS/SYMBOL	COMMENT
0	TOKO	FS 17 FS 18	22/9,18,27,36	Transmitter OK error
*1	DTOCER	FS 17	25/3	Invalid OPCODE
*4	DTBITER	FS 17	23/15 22/9,18,27,36	DT lost bit timing
*5	DTFRMER	FS 17	23/15 22/9,18,27,36	DT lost frame timing
*6	DTSAN	FS 17	23/3,15	SP-2 did not finish processing DTs in time
*7	DTPARER	FS 17	24/19 22/9	Incoming DT parity error
* If TOK is not up, there is only one CKT pack (FA1188) on FS 17 which can cause bit 1,4,5,6, or 7 to come up				

[1] Identify PMD number in rightmost three octal digits of RCNT29
[Figure 1, Page 2]

[2] Read PMD description in TABLE A, Page 2

[3] Determine from interrupt printout text and Figure 2, Page 2 if TGR or term indicated as failing _____



ANALYZE CCISFR F-LEVEL INTERRUPT, COMMON CHANNEL INTEROFFICE SIGNALING FRAME

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DATA: ERROR ANALYSIS RECENT HISTORY TABLE

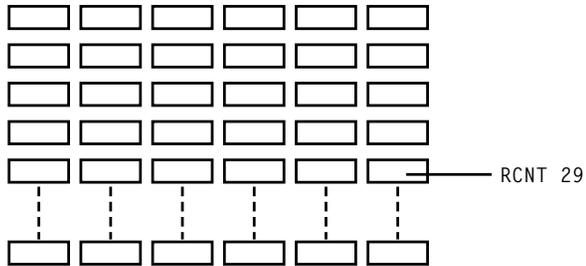


Figure 1 - Recent History Data

DATA: CCIS CRITICAL REGISTERS

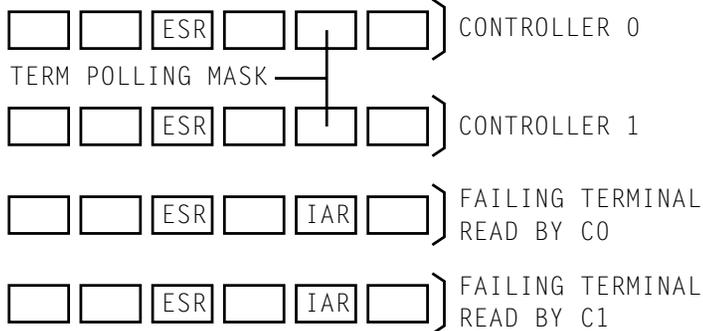


Figure 2 - CCIS Critical Registers

TABLE A PMD DESCRIPTIONS			
PMD*	DESCRIPTION	PMD*	DESCRIPTION
1, 2	MTCE OPCODE failure (OPCODE ≥ 100)	17, 20	Terminal stopped. Terminal hardware error
3, 4	Invalid TGR OPCODE		
5, 6	Order to unequipped terminal	21, 22	Terminal retry passed through original controller - transient error
7, 10	Retry of TAC order passed - transient error		
11, 12	TAC order retry failed - hard fault in controller	23, 24	Terminal retry passed through mate. Problem in original controller
13, 14	Quarantine bit not set in active controller - configuration problem		
15, 16	Terminal accessed was out of service. Check terminal polling mask	25, 26	Terminal retry failed through both controllers. Terminal hardware suspect
* Odd PMDs - Both controllers in service before interrupt Even PMDs - Only even controller in service before interrupt			

TABLE B CONTROLLER ESR					
BIT	NAME	FUNCTION	PACK TYPE	SUSPECT PACK LOCATION	ASSOCIATED FS*
0	ASWF	All seems well failure	FA824	02-19	8
1	-	Unassigned			
2	PFE	Parity failure - even	FA534 FA534	06-22 06-23	4
3	PFO	Parity failure - odd	FA534 FA534	06-22 06-23	4
4	TDPF	Terminal data parity failure	FA824	02-19	6
5	NTASW	No terminal all seems well			6
6	EASW	Erroneous all seems well	FA822	02-18	6
7	QUAR	Quarantine	-	-	-
8	OPDF	OPCOPE decoder failure	FA820 FA821 FA825	02-20 02-21 06-20	5
9	DIF	Data transfer failure	FA534	06-23	4
10	VOC	Valid OPCODE	FA822	02-18	6
11	-	Unassigned	-	-	-
* SD-4A057-01					

ANALYZE CCISFR F-LEVEL INTERRUPT, COMMON CHANNEL INTEROFFICE SIGNALING FRAME

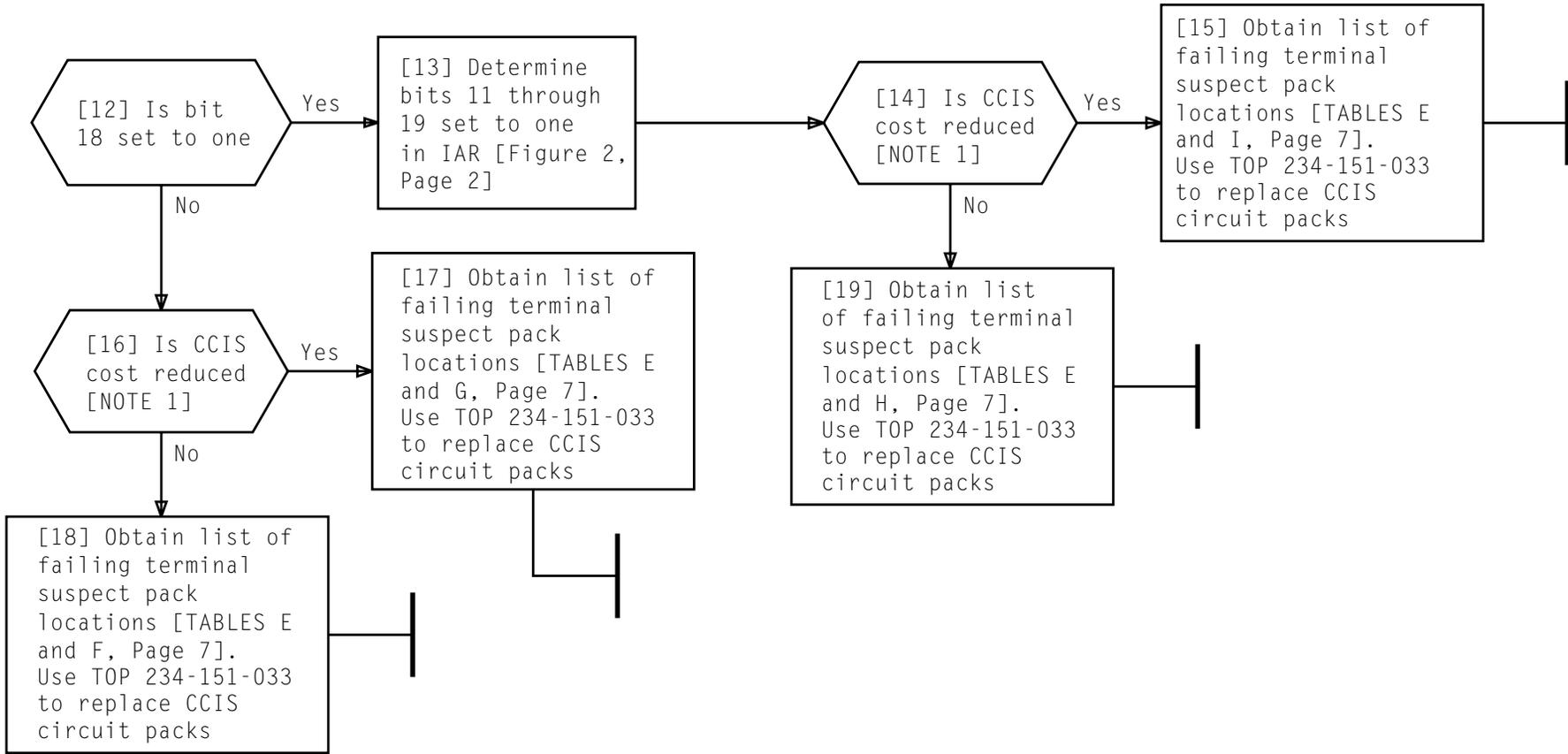
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TABLE C TERMINAL ESR BITS 0-14					
BIT	NAME	FUNCTION	PACK TYPE	SUSPECT PACK LOCATION	ASSOCIATED FS†
0-5	—	Unassigned	—	—	—
6	DSR	Data set ready	*	04-39	1
7	SDATA	Transmitter data	FA795	02-12	1
8	RDATA	Receive data	*	04-39	1
9	PESUMB	Partial error summary B (12, 13, 15, 17)	FA792	02-14	4
			FA790	02-13	4
			FA791	06-14	4
			FA788	02-17	4
			FA789	02-16	4
10	PESUMA	Partial error summary A (14, 16, 18, 20)	FA792	02-14	4
			FA790	02-13	4
			FA791	06-14	4
			FA788	02-17	4
			FA789	02-16	4
11	ESUM	Error summary (A & B)	FA792	02-14	4
			FA790	02-13	
			FA791	06-14	
			FA788	02-17	
			FA789	02-16	
12	LLA	Link list address error	FA791	06-14	4
13	LLD	Link list data failure	—	—	4
14	TBDOF	Transmit bit overflow	FA795	02-12	1
* Office-dependent † SD-94833-01					

TABLE D TERMINAL ESR BITS 15-23					
BIT	NAME	FUNCTION	PACK TYPE	SUSPECT PACK LOCATION	ASSOCIATED FS*
15	RBOF	Receive bid overflow	FA795	02-12	1
16	DCP	Data memory C parity	FA791	06-14	4
17	DABP	Data memory AB parity			4
18	PMP	Program memory parity			2
19	LNRP	I/O list number error			4
20	IODEC	I/O decoder error			4
21	IOPBOF	I/O put buffer overflow			1
22	IODP	I/O data parity			1
23	I00CP	I/O OPCODE parity	FA794	02-06	1
* SD-94833-01					

ANALYZE CCISFR F-LEVEL INTERRUPT, COMMON CHANNEL INTEROFFICE SIGNALING FRAME

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NOTE 1	
Cost reduced frame does not have packs in terminal locations 02-26, 27 and 06-28, 29	
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ANALYZE CCISFR F-LEVEL INTERRUPT, COMMON CHANNEL INTEROFFICE SIGNALING FRAME

TABLE E		
TERM.	BAY	STARTS AT VERTICAL
0	0	33
1		41
2		56
3	1	33
4		41
5		56
6		25
7		33
8		41
9	Left supl.	56
10		66
11	Right supl.	25
12		33
13		41
14		56
15		66

TABLE F	
NON-COST REDUCED TERMINAL SUSPECT PACK LOCATIONS	
ESR BIT 16	ESR BIT 17
06-12*	02-09
06-13	02-10
	02-11*
	02-12*
	06-09
	06-10
	06-11*
	06-12*
	06-13*
*Optional pack	

TABLE G	
COST REDUCED TERMINAL SUSPECT PACK LOCATIONS	
ESR BIT 16	ESR BIT 17
06-12	02-09
	02-10
	06-09
	06-10
	06-12

TABLE H		
NON-COST REDUCED TERMINAL SUSPECT PACK LOCATIONS		
ESR BITS 12-19	ESR BIT 11=0	ESR BIT 11=1
Bit 12 = 1	02-22	06-22
Bit 13 = 1	02-23	06-23
Bit 14 = 1	02-24	06-24
Bit 15 = 1	02-25	06-25
Bit 16 = 1	02-26	06-26
Bit 17 = 1	02-27	06-27
Bit 18 = 1	02-28	06-28
Bit 19 = 1	02-29*	-
*Optional pack		

TABLE I		
COST REDUCED TERMINAL SUSPECT PACK LOCATIONS		
ESR BITS 12-19	ESR BIT 11=0	ESR BIT 11=1
Bit 12 = 1	02-22	06-22
Bit 13 = 1		
Bit 14 = 1	02-23	06-23
Bit 15 = 1		
Bit 16 = 1	02-24	06-24
Bit 17 = 1		
Bit 18 = 1	02-25	06-25
Bit 19 = 1		

[1] Determine octal PMD number from rightmost three digits of the RCNT+29 register and record [Figure 1, Page 2]

In TABLE A, Page 5:

[2] Identify row for location of PMD number that was determined in Step 1

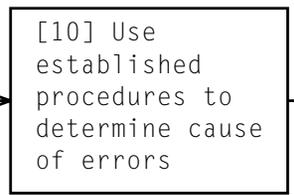
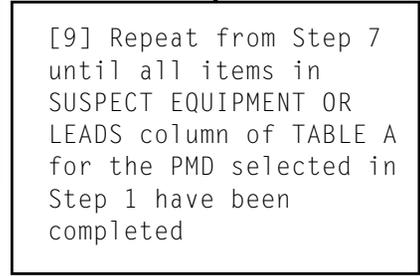
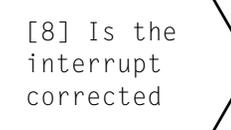
[3] Identify the active or mate controller as required from bit 7 of the STATR register [Figure 2, Page 3] and record

[4] Identify ESU reporting errors by using position of set bit in the USR (unit error summary) register [Figure 2, Page 3] and record

[5] Determine the bits or conditions to be inhibited using the position of bits in UPR (unit pest register) [Figure 2, Page 3] and record

[6] Locate and identify the bits in the last look memory [Figure 3, Page 4] that are set to one and record

[7] Perform activities listed in the SUSPECT EQUIPMENT/LEADS column by doing one at a time starting with the first item listed in TABLE A, Page 5. Use TOP 234-151-050 to replace ES circuit packs



DATA: ERROR ANALYSIS RECENT HISTORY TABLE					
06143403	00000000	00000000	20000000	00000400	00000000
00005603	00200000	00000002	00000000	00000000	00000000
30666240	00000000	40001604	00000020	00000020	00000000
00000000	00002312	00002004	00001112	00000004	04343403
40165200	00000000	00000000	00000000	00105210	4000027
00012261	00012261	00000016	00000000	00000000	00000000
00000000	00000000	00000000	00000000	00042407	00000075
00100012	00013502	00000101	00000014	00000000	00040000
00000000	00000000	00555361	00000000		

DATA: ERROR ANALYSIS HISTORY TABLE					
RCNT+0	RCNT+1	RCNT+2	RCNT+3	RCNT+4	RCNT+5
RCNT+6	RCNT+7	RCNT+8	RCNT+9	RCNT+10	RCNT+11
RCNT+12	RCNT+13	RCNT+14	RCNT+15	RCNT+16	RCNT+17
RCNT+18	RCNT+19	RCNT+20	RCNT+21	RCNT+22	RCNT+23
RCNT+24	RCNT+25	RCNT+26	RCNT+27	RCNT+28	RCNT+29
RCNT+30	RCNT+31	RCNT+32	RCNT+33	RCNT+34	RCNT+35
RCNT+36	RCNT+37	RCNT+38	RCNT+39	RCNT+40	RCNT+41
RCNT+42	RCNT+43	RCNT+44	RCNT+45	RCNT+46	RCNT+47
RCNT+48	RCNT+49	RCNT+50	RCNT+51	RCNT+52	RCNT+53
RCNT+54	RCNT+55	RCNT+56	RCNT+57	RCNT+58	RCNT+59
RCNT+60	RCNT+61	RCNT+62	RCNT+63		

Figure 1 - Third Part of EST Interject Printout

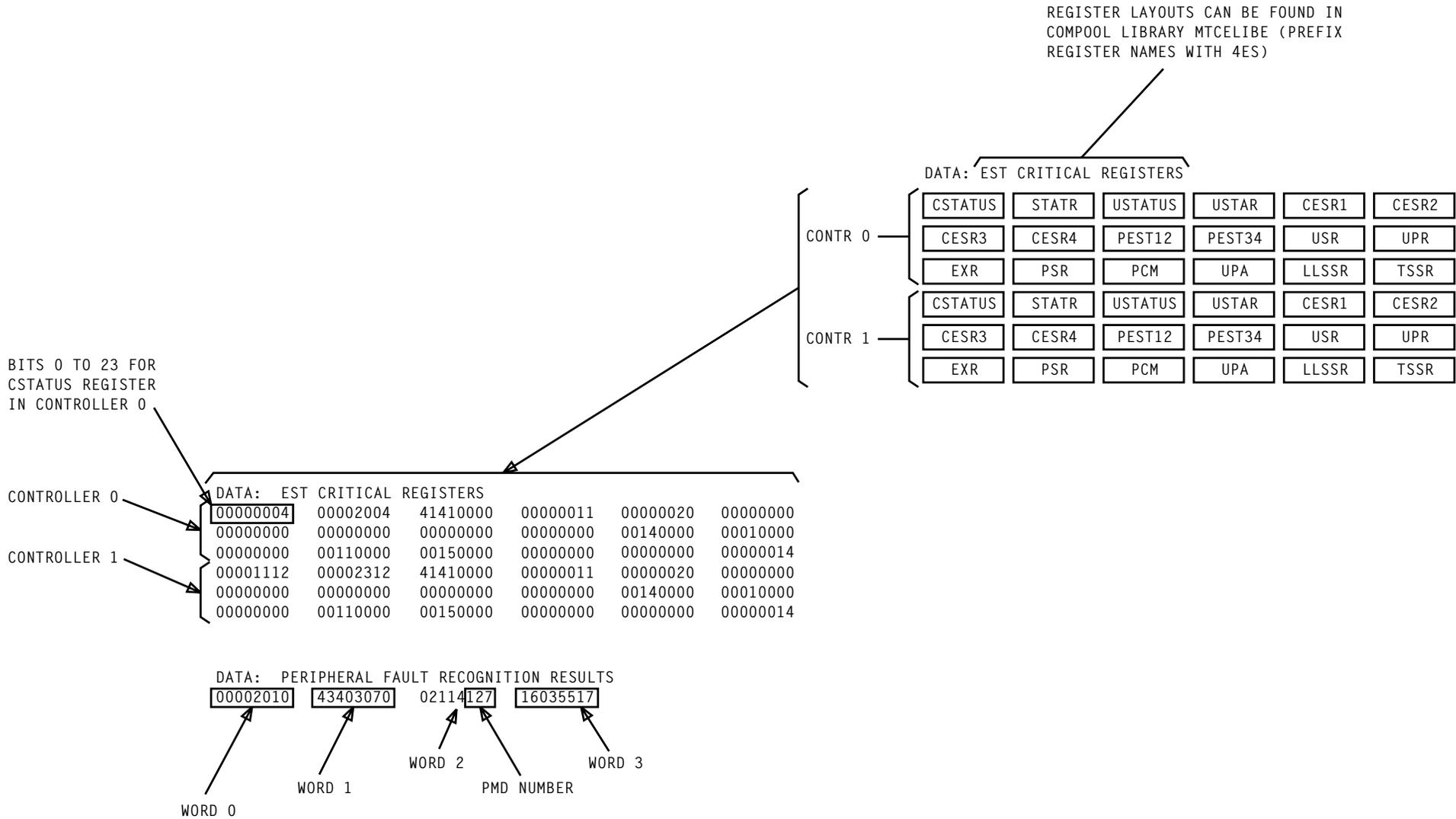


Figure 2 - Second Part of EST Interject Printout

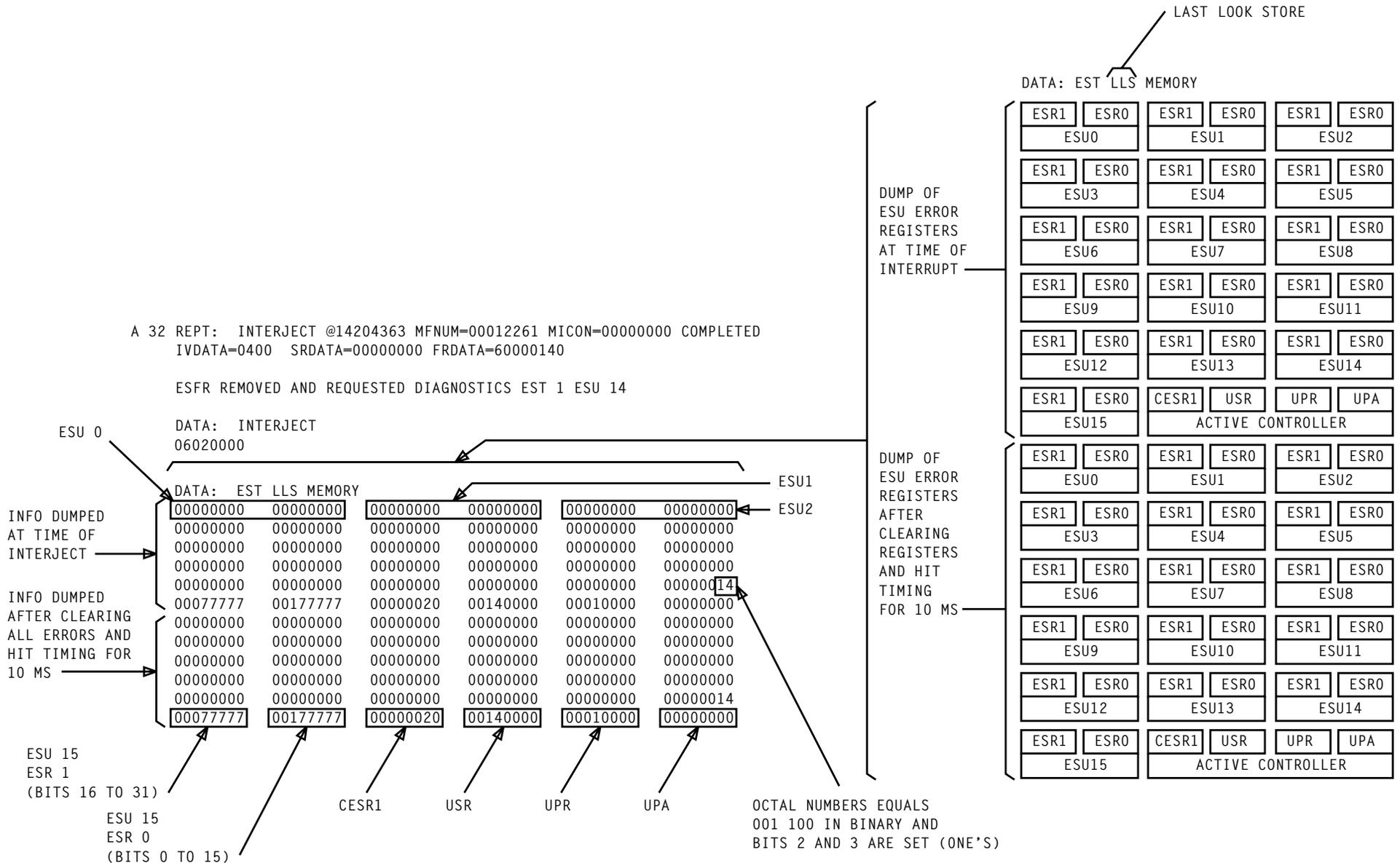


Figure 3 - First Part of EST Interject Printout

ANALYZE ESFR INTERJECT

TABLE A							
PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIGURE 2	USR FIGURE 2	UPR FIGURE 2	ESR FIGURE 3	
120	Both controllers in service. APUT set in active and not set in mate	Mate controller	Bit 7 equals zero in mate controller	-	-	-	<ol style="list-style-type: none"> 1. Suspect circuit packs in mate controller that are listed in TABLE B, Page 13 2. Use established office procedures to determine cause of errors in circuitry associated with a INAPUTN LEAD (a = mate controller)
121	Both controllers in service. APUT set in mate and not set in active. Mate USR have bits set	Active controller	Bit 7 equals one in active controller	-	-	-	<ol style="list-style-type: none"> 1. Suspect circuit packs in active controller that are listed in TABLE B, Page 13 2. Use established office procedures to determine cause of errors in circuitry associated with a INAPUTN LEAD (a = active controller)

TABLE A (Contd)

PMD		SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS	
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIGURE 2	USR FIGURE 2	UPR FIGURE 2		ESR FIGURE 3
122	APUT set in active controller. Same bits set in active USR at interrupt and after 10 ms hit timing delay	ESUs that are alarming	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	-	<ol style="list-style-type: none"> 1. Check cabling between shelf of ESU reporting errors and controller packs of active controller 2. Check backplane wiring from ESU packs reporting to shelf connector 3. Suspect circuit packs in active controller that are listed in TABLE C, Page 13
123	APUT set in active controller. Active USR had bits set. All bits not set at interrupt and after 10 ms hit delay timing	ESUs that are alarming	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	-	<ol style="list-style-type: none"> 1. Check cabling between shelf of ESU reporting errors and controller packs of active controller 2. Check backplane wiring from ESU packs reporting to shelf connector 3. Suspect circuit packs in active controller that are listed in TABLE C, Page 13

TABLE A (Contd)

PMD		SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS	
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIGURE 2	USR FIGURE 2	UPR FIGURE 2		ESR FIGURE 3
124	APUT set in active controller. Active USR had one bit set. Bit was set at interrupt and not set after 10 ms hit timing delay	ESU that is alarming	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	Identify ESR bits set to one at the time of interrupt for ESU reporting errors and interpret meaning	<ol style="list-style-type: none"> 1. Suspect in ESU that are listed in TABLE D, Page 13, and have error bits set to one 2. Check leads and associated circuitry that are listed in TABLE E, Page 14, and have corresponding bits in the ESR register set to one
125	APUT set in active controller. Active found unpested, unequipped, growth, or special growth ESUs reporting errors	Active controller	Bit 7 equals one in active controller	-	If bits equal one in positions that represent growth or special growth ESUs do nothing (program pested ESUs). If bits that are equal to one represent other equipped ESUs, replace packs in suspect Equipment/Leads column	-	Suspect NH27 and NH32 circuit packs at locations called out in TABLE C, Page 13

TABLE A (Contd)

PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIGURE 2	USR FIGURE 2	UPR FIGURE 2	ESR FIGURE 3	
126	APUT set in active controller. No ESU errors reported through active controller when interrupt occurred	Active controller	Bit 7 equals one in active controller	-	-	-	Suspect NH26 and NH27 circuit packs at locations called out in TABLE C, Page 13
127	APUT set in active controller. One ESU reporting errors through active controller. Same errors reported when interrupt occurred and after 10 ms hit delay timing	ESU that is alarming	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	Identify ESR bits set to one at time of interrupt and also after 10 ms hit delay timing and interpret meaning	<ol style="list-style-type: none"> 1. Suspect packs in ESU that are listed in TABLE D, Page 13, and have error bits set to one and ESU reporting errors 2. Check leads and associated circuitry that are listed in TABLE E, Page 14, and have corresponding bits in the ESR register set to one

TABLE A (Contd)

PMD		SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS	
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIGURE 2	USR FIGURE 2	UPR FIGURE 2		ESR FIGURE 3
130	A PUT set in active controller. One ESU reporting errors through active controller. Same errors reported when interrupt occurred and after 10 ms hit delay timing. (ESR0 bits 4-7)	TSI DS120 line or ESU circuitry on TSI side	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	Identify ESR bits set to one at time of interrupt and also 10 ms hit delay timing and interpret meaning	<ol style="list-style-type: none"> 1. Suspect packs in ESU that are listed in TABLE D, Page 13, and have error bits set to one and ESU reporting errors 2. Check leads and associated circuitry that are listed in TABLE E, Page 14, and have corresponding bits in the ESR register set to one 3. Check DS120 line between TSI and ESU reporting errors

TABLE A (Contd)

PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIGURE 2	USR FIGURE 2	UPR FIGURE 2	ESR FIGURE 3	
131	APUT set in active controller. One ESU reporting errors through active controller. Same errors reported when interrupt occurred and after 10 ms hit delay timing	VIF/DF/DIF DS120 line or ESU circuitry on VIF/DT/DIF side	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	Identify ESR bits set to one at time of interrupt and also 10 ms hit delay timing and interpret meaning	<ol style="list-style-type: none"> 1. Suspect packs in ESU that are listed in TABLE D, Page 13, and have error bits set to one and ESU reporting errors 2. Check leads and associated circuitry that are listed in TABLE E, Page 14, and have corresponding bits in the ESR register set to one
132	APUT set in active controller. One ESU reporting errors as indicated by active controller USR bit set. No error bits set in ESR thru active controller	Active controller	Bit 7 equals one in active controller	If both controllers are in service prior to interrupt, ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	-	<ol style="list-style-type: none"> 1. If one controller is out of service prior to interrupt, suspect NH32 circuit pack in active controller at location called in TABLE C, Page 13 2. If both controllers are in service perform the following: <ol style="list-style-type: none"> a. Check cabling between ESU shelf and controller packs or backplane wiring from ESU packs to shelf connector

TABLE A (Contd)

PMD		SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS	
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIGURE 2	USR FIGURE 2	UPR FIGURE 2		ESR FIGURE 3
132 (Contd)							2. Suspect NH31 and NH32 circuit packs in controller that was active prior to interrupt at locations called out in TABLE C, Page 13
133	APUT set in active and mate controller. No USR bits set in mate controller	Mate controller	-	-	-	-	1. Suspect NH26 and NH27 circuit packs in both controllers at locations called out in TABLE C, Page 13 2. Check for multiple hardware faults in mate controller
134	APUT not set in active or mate controller	Mate controller	-	-	-	-	Request technical assistance per local office practice
135	APUT not set in active and mate is out of service	Active controller					Request technical assistance per local office practice

TABLE A (Contd)

PMD		SIGNIFICANT REGISTER INDICATIONS					SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIGURE 2	USR FIGURE 2	UPR FIGURE 2	ESR FIGURE 3	
136	APUT set in mate and not set in active controller. No USR bits set in mate controller	Mate controller	Bit 7 equals one in mate controller	-	-	-	Suspect NH26 and NH27 circuit packs in mate controller at locations called out in TABLE C, Page 13

TABLE B		
PACK	CONTR 0	CONTR 1
NH32	064-09	064-14
NH33	055-11	055-12
NH31	064-08	064-15
NH27	073-09	073-14

TABLE C		
PACK	CONTR 0	CONTR 1
NH33	055-11	055-12
NH32	064-09	064-14
NH31	064-08	064-15
NH27	073-09	073-14
NH26	073-07	073-16

TABLE D ESU SUSPECT PACK LOCATIONS ASSOCIATED WITH ESR BITS									
ESR →	ESR0						ESR1		
BITS →	0-3	4-7	8,9	10-12	13	14,15, 0	1-3	4-8	9-10
PACK ESU ↙	NH2 LOCATION	NH3 LOCATION	NH1 LOCATION	NH4 LOCATION	NH6 LOCATION	NH5 LOCATION	NH5 LOCATION	NH8 LOCATION	NH7 LOCATION
0	028-07	028-09	028-08	028-06	028-01	028-04	028-02	028-10	028-11
1	028-16	028-14	028-15	028-17	028-22	028-19	028-21	028-13	028-12
2	037-07	037-09	037-08	037-06	037-01	037-04	037-02	037-10	037-11
3	037-16	037-14	037-15	037-17	037-22	037-19	037-21	037-13	037-12
4	046-07	046-09	046-08	046-06	046-01	046-04	046-02	046-10	046-11
5	046-16	046-14	046-15	046-17	046-22	046-19	046-21	046-13	046-12
6	128-07	128-09	128-08	128-06	128-01	128-04	128-02	128-10	128-11
7	128-16	128-14	128-15	128-17	128-22	128-19	128-21	128-13	128-12
8	137-07	137-09	137-08	137-06	137-01	137-04	137-02	137-10	137-11
9	137-16	137-14	137-15	137-17	137-22	137-19	137-21	137-13	137-12
10	146-07	146-09	146-08	146-06	146-01	146-04	146-02	146-10	146-11
11	146-16	146-14	146-15	146-17	146-22	146-19	146-21	146-13	146-12
12	155-07	155-09	155-08	155-06	155-01	155-04	155-02	155-10	155-11
13	155-16	155-14	155-15	155-17	155-22	155-19	155-21	155-13	155-12
14	164-16	164-14	164-15	164-17	164-22	164-19	164-21	164-13	164-12

ANALYZE ESR INTERJECT

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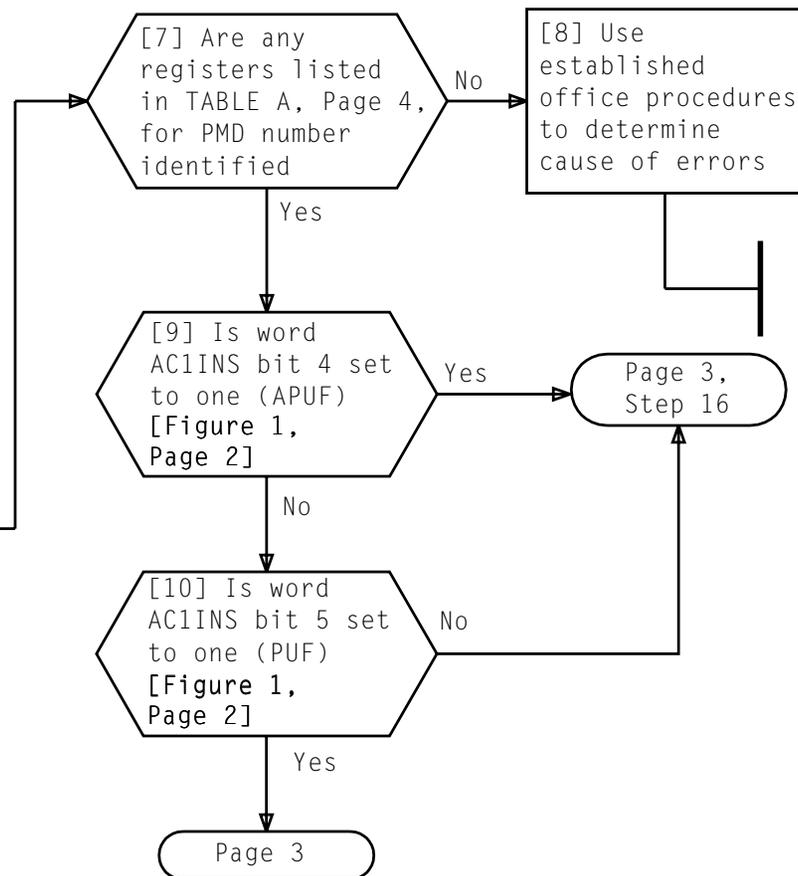
TABLE E				
ESU (LLS MEMORY) ERROR SOURCE REGISTER BITS				
ESR	BIT	LEAD	FUNCTION MONITORED	SIGNAL MONITORED
0	0	UESB0	VIF/DT/DIF	GBC3
	1	UESB1	input framing	1MHz clock (PHX)
	2	UESB2	VIF/DT/DIF output parity	Serial data parity
	3	UESB3	VIF/DT/DIF output parity	Serial data parity
	4	UESB4	TSI input framing	GBC3
	5	UESB5		1MHz clock (RCK1)
	6	UESB6	TSI output parity	Serial data parity
	7	UESB7	TSI output parity	Serial data parity
	8	UESB8	RCV line driver out	ROUT
	9	UESB9	XMT line driver out	TOUT
	10	UESB10	Each error source bit observes 8 monitor points through an 8-bit parity generator. Odd parity across 8 monitor points is compared with a reference bit from controller	PYUCC at TS 124
	11	UESB11		PYUCB at TS 124
	12	UESB12		PYUCA at TS 124
	13	UESB13		PYTDA at TS 124
	14	UESB14		PFSCA at TS 124
	15	UESB15		PFSCB at TS 124
0	UESB16	PFSCC at TS 124		
1	UESB17	PSSCA at TS 124		
2	UESB18	PSSCB at TS 124		
3	UESB19	PSSCC at TS 124		
1	4	UESB20	TRK status store E/D	TRK status TS 123
	5	UESB21	TRK status store S/F	TRK status TS 123
	6	UESB22	GGC counter SYNC	GGC SYNC
	7	UESB23	EST initialize	INITO
	8	UESB24	Good INTVL CNTR INIT	IGICO
	9	UESB25	GWC counter SYNC	GWCSYNC
	10	UESB26	Controller select	OASP, 1ASP

SUMMARY

Determine active controller and suspect controller. Locate and read PMD description in PR4A348. If no registers are identified which are listed in TABLE A, Page 4, suspect software problem and use established office procedures to determine cause of errors. Otherwise, determine if APUF or PUF source by using AC1INH and AC1INS registers. If APUF source, locate leads in SD5G168-01 for TABLE A PMD register bits set to one

using TABLE C and SD lead index. If PUF source, identify OPCODE in AC1PRM register, and use TABLE B, Page 4, to determine read or write order. Locate leads in SD5G168 for TABLE A PMD register bits set to one using SD information, note 312, part B, write or read order information and SD lead index. For APUF or PUF source, suspect packs and leads that could cause lead names located to go active [NOTE 3, Page 3].

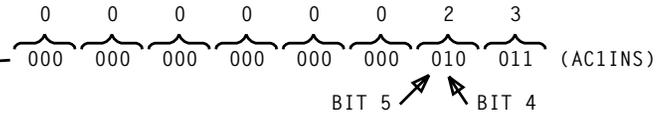
- [1] Determine active controller(CACT) and mate controller (CMATE) by noting which controller has bit 7 set to one in STATR register (CACT), and which controller has it set to zero (CMATE) [Figure 1, Page 2 (EST critical registers)] and record results
- [2] Determine suspect controller using bits 2 (CONTR 0) and 3 (CONTR 1) of PU4RESULT word [Figure 1, Page 2]
- [3] Identify and record octal PMD number [Figure 1, Page 2]
- [4] Locate "PMDabc" in PIDENT ESRMAIN (PR4A348) cross reference section (abc = is octal PMD number) and record
- [5] Note page and line number listed in DEF/REF column for PMDabc (abc = octal PMD number) and record
- [6] Go to referenced page and line number, and read PMDabc comments (abc = octal PMD number)



ANALYZE ESFR F-LEVEL INTERRUPT

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A 05 REPT: F-LEVEL =14424210 MFNUM=00000554 MICON=00000022 COMPLETED
 LVDATA=0040 SRDATA=00000002 FRDATA=60000100



ESFR RESTORED EST 1 CONTR 1

DATA: F-LEVEL

00047400	00000001	00047447	00041617	20000000	20001320
14363055	00000000	14363055	14424210	00000040	14424207
00041617	14424212	22007666	00000023	07210017	00000004
14423722	04021000	00011000	00000002	60000000	00000000
00000000	00000000	00160012	00000000	00000017	00000000
60000000	00000000	00000002	00000000	00000000	00000000
00007666	77637777	20000000	00123413	00123717	00006012
00002302	00001022	00001022	00000000	00000000	

F-LEVEL

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASF(H)	AC1ASF(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1LR	
AC1PSQ	AC1ULR	AC1PES	ST1PES	ST1ER	ST1PRM
ST1PRL	ST1PSC	AC1RPO	AC1RP1	ST1RPO	ST1RP1
ST1CSC	ST1INH	PU1RFLC00	PU1RFLC01	PU1RFLC02	PU1RFLC03
PU1RFLC04	PU1RFLC05	PU1RFLC06	PU1RFLC07		

AC1PRM

DATA: MAC CONTROL MEMORY

60221200	00000000	14264364	14267360	47161601	00064000
15200062	04200040	00000000	20000000	00047400	00000000
00000000	20001320	14363055	00000000	00047447	54047336
00000600	00000000				

DATA: EST CRITICAL REGISTERS

STATR CONTR 0	00600012	00006012	01600004	00000011	00001022	00000000
	00000000	00000000	00000000	00000000	00177777	00037367
	00000000	00000000	00140000	00000000	00000000	00000016
STATR CONTR 1	00601102	00002302	01600004	00000011	00001322	00002000
	00000000	00000000	00000000	00000000	00177777	00037367
	00000000	00000000	00140000	00000000	00000000	00000016

DATA: PERIPHERAL FAULT RECOGNITION RESULTS

00010010 43402000 00303455 16044051

DATA: ERROR ANALYSIS RECENT HISTORY TABLE

01643403	00000000	00160012	00000000	00000000	00000000
00007603	00200000	00000002	20000000	00000001	00200007
04706100	00000000	00001604	00001022	00001022	00000000
00000000	00002302	00006012	00601102	00600012	00643403
40026040	00000000	00000000	00000000	00106110	20000055
00000554	00000554	00000000	00000000	00000000	00000000
00000000	00000000	00000000	00000000	00000000	00000000
00100001	00010610	00001010	00000000	00000000	00000000
00000000	00000000	00035740	00000000	00000001	00000000
00000000	00000000	00000000	00000000	00000000	00000000
00000000	00000000	00000000	00000000		

PMD

DATA: EST CRITICAL REGISTERS

C0	CSTATUS	STATR	USTATUS	USTAR	CESR1	CESR2
	CESR3	CESR4	PEST12	PEST34	USR	UPR
C1	EXR	PSR	PCM	UPA	LLSSR	TSSSR
	CSTATUS	STATR	USTATUS	USTAR	CESR1	CESR2
	CESR3	CESR4	PEST12	PEST34	USR	UPR
	EXR	PSR	PCM	UPA	LLSSR	TSSSR

ALL WORDS PREFIXED BY 4ES AND LAYOUTS MAY BE FOUND IN COMPOOL LIBRARY MTCLIBE

DATA: PERIPHERAL FAULT RECOGNITION RESULTS

PU4RESULT PU4UTMND PU4FRPMD PU4FRJRG

Figure 1 - Interrupt Printout

ANALYZE ESFR F-LEVEL INTERRUPT

[11] Determine OPCODE (octal) in bits 5-11 of word AC1PRM
 [Figure 1, Page 2]

[12] See NOTE 1. Use TABLE B, Page 4, to determine if OPCODE
 was a read or write order

[13] Determine TABLE A, Page 4, PMD register bits
 set to one for suspect controller identified
 in Step 2 [Figure 1, Page 2]

[14] Using information note 312, part B in SD5G168-01
 (Sheets D9 and D10), identify write lead name (write
 order) or read lead name (read order) associated with
 register bits in TABLE A, Page 4 set to one

[15] See NOTE 2. Use SD lead index to locate each
 write or read lead name in an FS

[16] Determine PMD register bits from TABLE A, Page 4, set
 to one for suspect controller identified in Step 2
 [Figure 1, Page 2]

[17] Using TABLE C, Page 4, locate SD5G168-01
 information notes associated with suspect controller
 PMD registers having bits set to one

[18] See NOTE 2. For each suspect controller register
 bit set to one, note its net name and function

[19] See NOTE 2. Use SD lead index located at front of SDs
 to locate each net name lead in an FS

AND

AND

[20] See NOTE 3.
 Suspect packs and
 leads that could
 cause net name
 leads located to
 go active

[21] Is
 problem
 corrected

[22] Use
 established
 office procedures
 to determine
 cause of errors

- NOTES
1. OPCODE actions described in SD5G168-01 information notes 325 and 326
 2. Prefix lead names with suspect controller (0 or 1)
 3. Lead names ending in P go high when active. Lead names ending in N go low when active

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ANALYZE ESRF F-LEVEL INTERRUPT

TABLE A					
PMD	REGISTER	BITS	PMD	REGISTER	BITS
001	*	-	035		
002	{ MADATA CESR1 CESR4	19,20	036		
004			037		
005			040		
007			041		
010			042		
014			043		
016			044		
020			045		
003	{ MADATA CESR1 CESR4	20,19,6	046		
006			047		
011			050		
012			051		
013			052		
015			053		
017			054		
017			055		
021	†	-	056		
022			057		
023	{ CESR1 CESR2 CESR3 CESR4	0-15 0-11 0-15 0-11	060		
024			061		
025			062		
026			070		
027			071		
030			072		
031			066	††	-
032			067		
033			073	†	-
* Duplex failure † Suspect software †† No errors found					

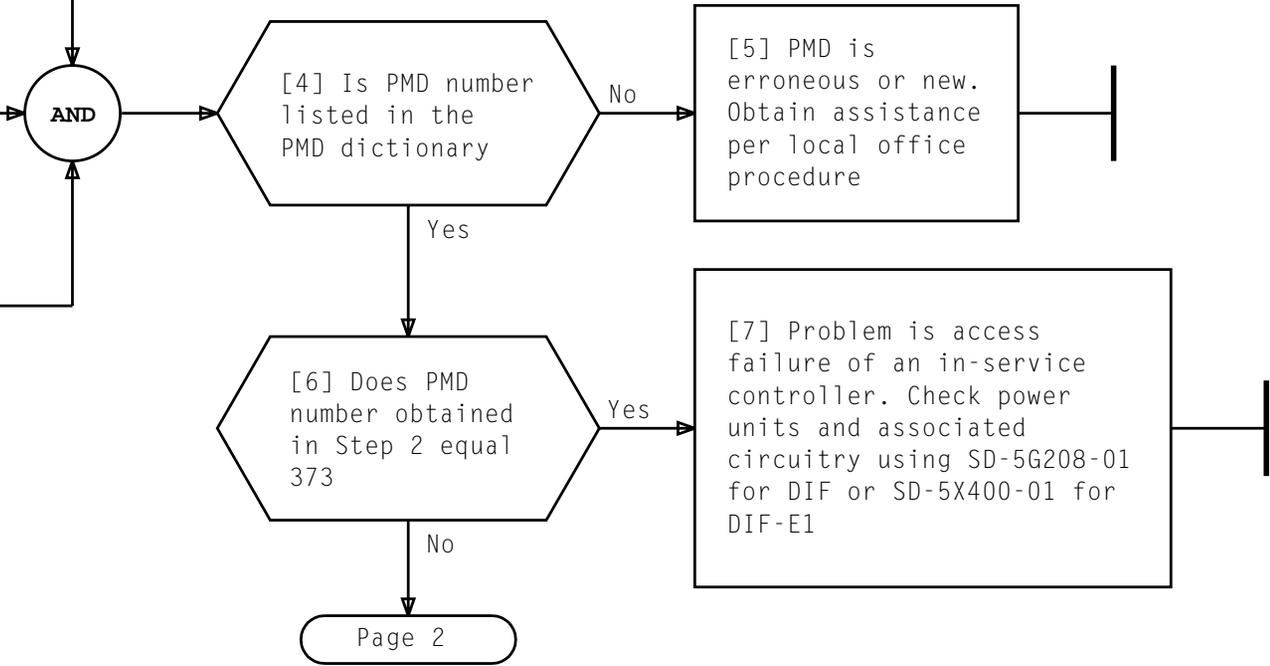
TABLE B		
OPCODE	READ	WRITE
003		√
027	√	
044		√
047	√	
105		√
106		√
111		√
112	√	
114		√
117		√
120	√	
141	√	
142		√
160	√	
170	√	
171	√	
172	√	
173	√	
174		√
175		√

TABLE C		
REGISTER	INFO. NOTE	SHEET
MADATA	331	D16
CESR1	346	D17
CESR2	347	D18
CESR3	348	
CESR4	349	

[1] Using Figure 1, identify suspect DIF or DIF-E1 controller and type of F-level interrupt such as PUF or APUF

[2] Using Figure 2, Page 6, obtain PMD number from FAULT RECOGNITION ISOLATION DATA field

[3] Access PMD dictionary [DLP-521] to obtain a description of the error analysis results



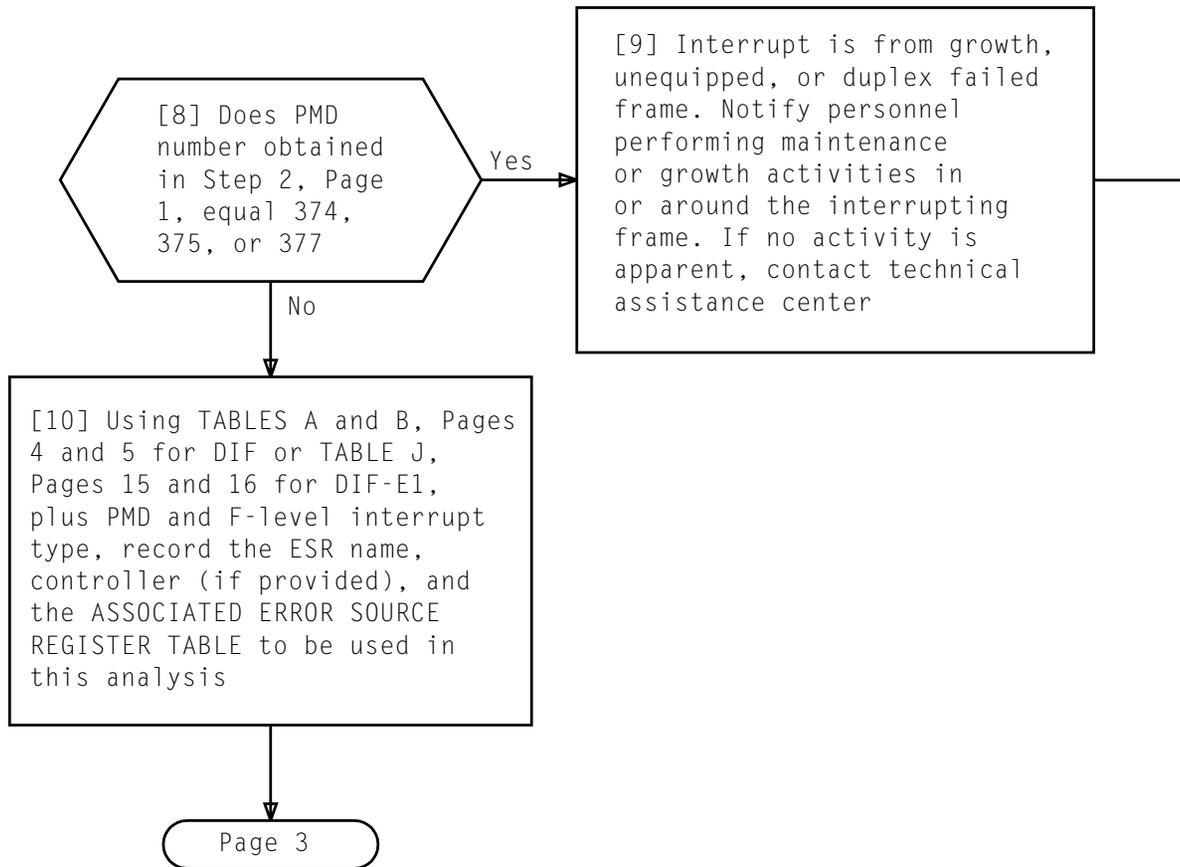
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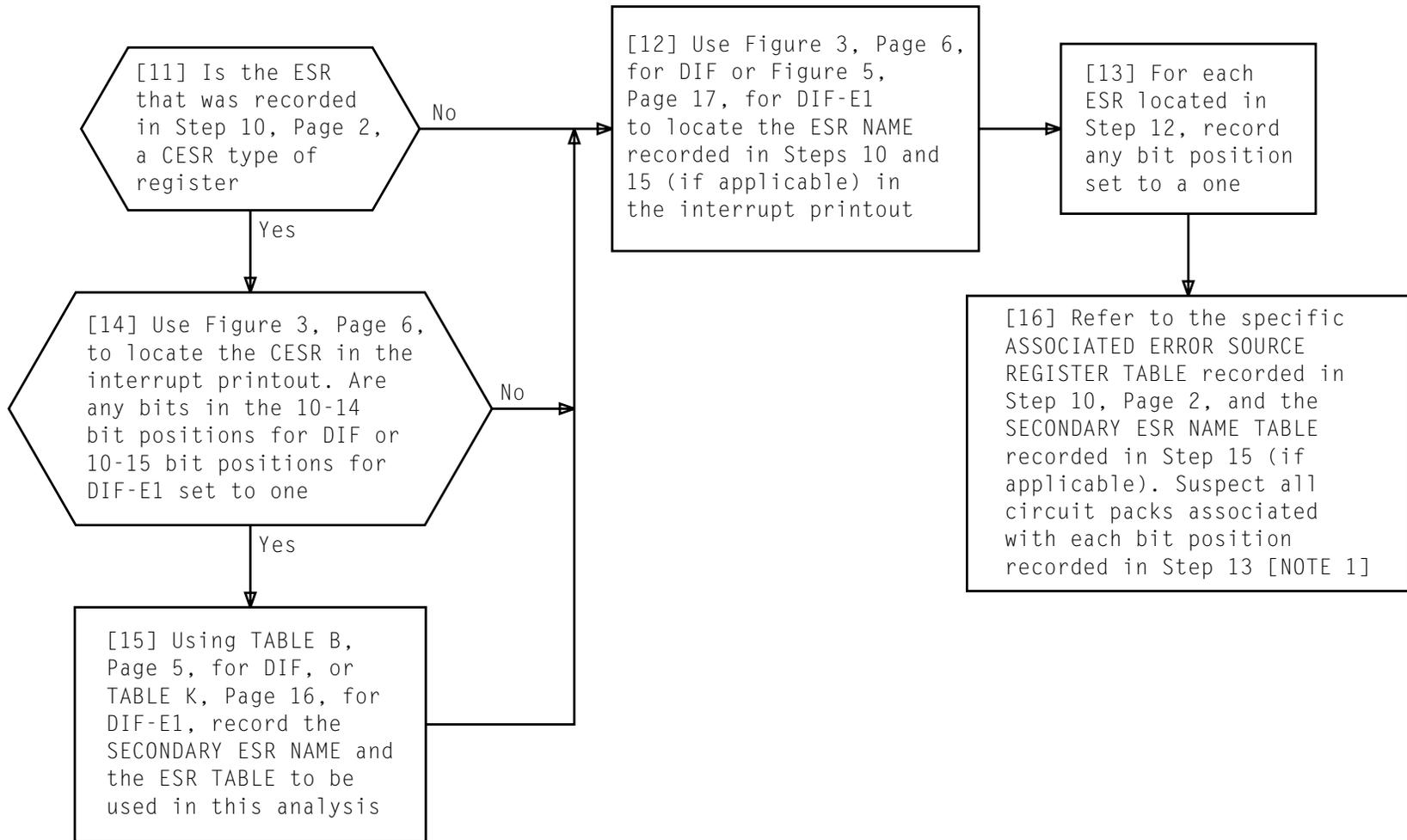
A 39 REPT:F-LEVEL 15004417 MFNUM=00000345 MICON=00000022 MSG STARTED
LV=0040 D0=00000000 D1=00000000 D2=00000057 D3=00000000
APUFS INTERRUPT DIF 21
DIFR RESOLVED ERROR DIF 21 CONTR 0
DIFR RECOMMENDED REMOVAL LOM DIF 21 CONTR 0
DIFR RECOMMENDED DIAGNOSTICS DIF 21 CONTR 0
FERA REQUESTED REMOVAL LOM DIF 21 CONTR 0
FERA REQUESTED DIAGNOSTICS DIF 21 CONTR 0
  
```

Figure 1 - Text Header Portion of DIFR Printout

ANALYZE DIFR F-LEVEL INTERRUPT

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NOTE 1	
The same CP may be contained in the CP list more than once. Duplicate entries should be ignored.	
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TABLE A			
DIF REFERENCE			
PMD	ESR NAME	ASSOCIATED ERROR SOURCE REGISTER TABLE	
		FOR APUF	FOR PUF
11,12,14,15,17,21,25,26,141,142	CLKESR (Clock error)	C, Page 7	C, Page 7
30-37,40-43,47,50,51,117,125,150,151,153,176	CESR for controller with bit 0 (ASWF) and/or bit 1 (AINT) set	D, Page 8	D, Page 8
154,156,160,161,162,164,165,166	MPESRH and/or MPESRF for active controller only**	F, Page 10; G, Page 11	F, Page 10; G, Page 11; H*, Page 12
54,56,60,61,62,64,65,66	MPESRH and/or MPESRF for both controllers	F, Page 10; G, Page 11	F, Page 10; G, Page 11; H*, Page 12
222	MPRS RH (bit 10)	F, Page 10	F, Page 10
70,71,72,75,76,77,100,101,102,120,170,171,172,177	CESR		D, Page 8; H*, Page 12
73,74,121	CESR for standby controller**		D, Page 8; H*, Page 12
173,174,175	CESR for active controller		D, Page 8; H*, Page 12
103-107,110-116,122,123,124	CESR for active controller**		D, Page 8; H*, Page 12
130, 131, 132, 1, 2, 3, 4, 5	CESR	D, Page 8	D, Page 8
* = Use TABLE H to expand "E" and "P" registers for PUFs only ** = Controller is active when CSTATUS bit 7 = 1 (bit 7 = 0 for standby)			

TABLE B		
DIF REFERENCE		
CESR BIT	SECONDARY ESR NAME	ESR TABLE [NOTE]
10, 11	IBIR	E, Page 9
12	MPESRH	F, Page 10
13	SPESR	I, Page 14
14	CLKESR	C, Page 7
<p>NOTE: Packs associated with circuitry recommended in ESR TABLE should be checked per SD-5G208-01 for other possible problems</p>		

ANALYZE DIFR F-LEVEL INTERRUPT

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A 39 REPT:F-LEVEL 01476430/1 MFNUM=0 0004303 MICON=00000020 MSG COMPL
LV=0040 D0=00000000 D1=04000 000 D2=00000017 D3=00000000
DATA:PERIPHERAL SYSTEM DATA
03020102 00000000 00000001 00000000 0 00000000 00000100
00000112 00000004 00000012 03600001 03600001 03600000
03600000
DATA:INTERRUPT SOURCE DATA
00002400 14130667 03552127 00 000020 00002000
DATA:FAULT RECOGNITION ISOLATION DATA
00000020 00002000 00000PMD 00000000 00000003 00000000
DATA:ERROR ANALYSIS STRATEGY DATA
01664210 00000001 00000001 00000001 00000001 00000000
00000000
04/29/79 11:38:37
*825

```

Figure 2 - Part of DIFR Printout

CSTATUS	HWSTATUS	MADATA	FSTATUS	DIU0D0	DIU0S1	} C O N T R 0	
CESR	PEST	(1) MPESRH	(2) MPESRF	DIUSUM0	DIUSUM1		(1) MPESR-DIFE1
CLKESR	SPEER	IBIR	EXR	PSRL	PSRH		(2) MPRETE-DIFE1
PSVL	PSVH	(3) 0...0	(4) 0...0	(5) 0...0	TRKCNTN		(3) MAPESR-DIFE1
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS		(4) EXCFESR-DIFE1
SPSTATR	(6) LUSPDO	(7) LUSPD1	(8) LUSPP0	(9) LUSPP1	MPBSTAT		(5) EXCMASK-DIFE1
URD1	URD2	URD3	URD4	URD5	URD6		(6) MAPCNTRS-DIFE1
URD7	URD8	URD9	URD10	URD11	URD12		ESCNCNTL-DIFE1 MF/DTMF 4ST
CCPST0	CCPST1	MPIES	MPRTIS	(10) MPMBSF	0...0		(7) MAPREGS-DIFE1
DACPST0	DACPST1	DRFPST0	DRFPST1	PSSSL	PSSSH		(8) MPSTKPTR-DIFE1
CALOW	CAHIGH	INTJ	0...0	0...0	0...0	(9) MPPMCNT-DIFE1	
MEMN	XLATE	FIRMVERS	5...5	5...5	5...5	(10) EXECSMW-DIFE1	
CSTATUS	HWSTATUS	MADATA	FSTATUS	DIU0D0	DIU0S1	} C O N T R 1	
CESR	PEST	MPESR	MPRETE	DIUSUM0	DIUSUM1		
CLKESR	SPEER	IBIR	EXR	PSRL	PSRH		
PSVL	PSVH	MAPESR	EXCESR	EXCMASK	TRKCNTN		
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS		
SPSTATR	MAPCNTRS	MAPREGS	MPSTKPTR	MPPMCNT	MPBSTAT		
URD1	URD2	URD3	URD4	URD5	URD6		
URD7	URD8	URD9	URD10	URD11	URD12		
CCPST0	CCPST1	MPIES	MPRTIS	MPMBSF	0...0		
DACPST0	DACPST1	DRFPST0	DRFPST1	PSSSL	PSSSH		
CALOW	CAHIGH	INTJ	0...0	0...0	0...0		

Figure 3 - DIF CREG Layout

TABLE C
CLOCK ERROR SOURCE REGISTER (CLKESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1	BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	ERACK160	1B/D8	CK16 energy detector for controller to unit (link A)	TM21(162-067,219) TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)	9	ERBCCSY0	1C/B8	(B) clock SYNC pulse ESR bit	TM21(152-055,231) TM24(162-085,201)
					10	ERLFMM0	1D/E7	Combined GGCSY and 10-msec waveform ESR bit	TM24(162-085,201)
1	ERAFSY0	1C/C8	Frame SYNC energy detector for controller to unit (link A)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)	11	XSFPCSY0	1D/E7	Super frame pattern (SFP) SYNC ESR bit	TM24(162-085,201)
					12	ASAMMO	6/G7	Active standby ESR for link A	TM47(162-073,213)
2	ERBCK160	1B/D8	CK16 energy detector for controller to unit (link B)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)	13	ASBMM0	6/G7	Active standby ESR for link B	TM47(162-073,213)
3	ERBFSY0	1B/E8	Frame SYNC energy detector for controller to unit (link B)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)	14	AERSFPS0	B1D/C5	Combined super frame pattern (SFP) SYNC and waveform ESR bit for link A	TM20(144-115,171) TM24(162-085,201)
4	ERAGGCP0	1B/D8	Combined GGC 32PY and 32SY ESR bit for controller to unit (link A)	TM22(162-103,183) TM21(162-067,219) TM24(162-085,201)	15	BERSFPS0	1D/E7	Combined super frame pattern (SFP) SYNC and waveform ESR bit for link B	TM20(144-115,171) TM24(162-085,201)
5	ERBGGCP0	1B/D8	Combined GGC 32PY and 32SY ESR bit for controller to unit (link B)	TM22(162-103,183) TM21(152-055,231) TM24(162-085,201)	16	ERGCCW0	1B/E7	Controller GGC and GWC distribution ESR bit	TM22(162-103,183) TM20(144-115,171) TM24(162-085,201)
					17	ERCK6GW0	1B/F7	T1 smooth sequence signal and T1 frame SYNC signal ESR bit	TM20(144-115,171) TM24(162-085,201)
6	ERGCBO	1B/C8	Controller GBC distribution ESR bit	TM22(162-103,183) TM21(152-055,231) TM24(162-085,201)	18	ER15FSA0	18/F7	T1 clock and T1 frame SYNC ESR bit from link A	TM20(144-115,171) TM24(162-085,201)
7	ERMMF0	1B/C8	Framing signal minor misframe ESR bit	TM22(162-103,183) TM24(162-085,201)	19	ER15FSB0	18/F7	T1 clock and T1 frame SYNC ESR bit from link B	TM20(144-115,171) TM24(162-085,201)
8	ERACCSY0	1C/B4	(A) clock SYNC pulse ESR bit	TM21(162-067,219) TM24(162-085,201)					

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**TABLE D
CONTROLLER ERROR SOURCE REGISTER (CESR)**

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT PACK - CONTR 0, CONTR 1	BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT PACK - CONTR 0, CONTR 1
0	ASWFPSO	7/C5	All seems well failure	TM46(162-079,207)	12	MMESRUM0	8F/F7	MP local ESR summary	TM41(152-091,195) TM46(162-079,207)
1	AINTPSO	7/L5	Autonomous interrupt	TM46(162-079,207)	13	ERLUSSPO	17G/G7	SP local ESR summary	TM30(144-067,219) TM46(162-079,207)
2	ERPUBEPY0	2A/G8	Peripheral unit bus even parity failure	TM32(170-025,261) TM46(162-079,207)	14	ERCKSUM0	1D/B7	Summary of clock ESR alarms	TM24(162-085,201) TM46(162-079,207)
3	ERPUBOPY0	2A/G8	Peripheral unit bus odd parity failure	TM32(170-025,261) TM46(162-079,207)	15	EXSUM3	4G/E4	Extended IBUS summary (future)	TM58(162-109,177) TM46(162-079,207)
4	INAPUT	8G/F9	Internal APUT	TM40(152-085,201) TM46(162-079,207)	16	T1LMM0	1D/E7	Cross-controller M/M SFP ESR alarm	TM24(162-085,201) TM46(162-079,207)
5			APUB (not used)	TM46(162-079,207)	17	ERIBMM0	4B/A7	Internal bus M/M	TM56(170-085,201) TM46(162-079,207)
6			Unassigned OPCODE firmware writable	TM46(162-079,207)	18	RRPYMM0	2B/E5	PUB reply register M/M	TM34(170-007,279) TM46(162-079,207)
7	ERPUBMOD0	2A/G8	Mode failure	TM32(170-025,261) TM46(162-079,207)	19	PUSEQMM0	2B/E5	PUB sequencer M/M (cross-controller)	TM34(170-007,279) TM46(162-079,207)
8	ERMFERMO	1B/B8	Out-of-frame	TM22(162-103,183) TM46(162-079,207)	20	BPSEQMM0	2B/D5	PUB buffer poll sequencer M/M (cross-controller)	TM34(170-007,279) TM46(162-079,207)
9	ERCK160	1A/C4	Absence of Intracontroller 16.384 MHz clock alarm	TM23(162-097,195)	21			Unassigned	
10	ERECSUM0	4B/G7	EXEC local ESR summary	TM56(170-085,201) TM46(162-079,207)	22	ERLFMM0	1D/E7	Low frequency clock (10 msec) M/M (cross-controller)	TM24(162-085,201) TM46(162-079,207)
11	ERIBSUM0	4B/G7	Internal bus local ESR summary	TM56(170-085,201) TM46(162-079,207)	23			Unassigned	

TABLE E INTERNAL BUS I REGISTER (IBIR)				
BITS (0-9)				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	IBMIXAMMO	4C/H5	Internal bus return M/M (bits 0-4)	TM48(170-091,195)
1	IBMIXBMMO	4D/E3	Internal bus return M/M (bits 5-9)	TM48(170-097,189)
2	IBMIXCMMO	4D/E7	Internal bus return M/M (bits 10-4)	TM48(170-103,183)
3	IBMIXDMMO	4E/E7	Internal bus return M/M (bits 15-19)	TM48(170-109,177)
4	IBMIXEMMO	4E/E3	Internal bus return M/M (bits 20-23) and parity	TM48(170-115,171)
5	ERIBMXPYO	4A/F7	Receive IB parity error	TM55(170-079,207) TM56(170-085,201)
6	ERIBAKDESO	4A/H7	IB destination and acknowledgment	TM55(170-079,207) TM56(170-085,201)
7	ERIBSOLPO	4A/A7	IB source, destination and OP CODE loop error	TM55(170-079,207) TM56(170-085,201)
8	ERIBAKSORO	4A/H7	Source acknowledgment error	TM55(170-079,207) TM56(170-085,201)
9	Unassigned			

TABLE E (Contd) INTERNAL BUS I REGISTER (IBIR)				
BITS (10-15)				
EXECUTIVE ESR				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
10	ERECIALUO	3D/C3	ALU mismatch	TM54(170-073,213) TM56(170-085,201)
11	SPORDYERR	4B/G4	PUC firmware detected error (firmware writable)	TM56(170-085,201)
12	UNMPOP	4B/G4	Unassigned MP OPCODE (firmware writable)	TM56(170-085,201)
13	MPDRDYERR	4B/G4	MP data ready error (firmware writable)	TM56(170-085,201)
14	ERECMSEQO	3B/C3	EXEC sequencer mismatch	TM53(170-043,243) TM56(170-085,201)
15	ERECPTO	3E/D5	EXEC ROM parity error	TM61(170-055,231) TM62(170-049,237) TM56(170-085,201)
16	ERIBSUMO	4B/G7	IB ESR summary	TM56(170-085,201)
17	ERECSUMO	4B/G7	IB EXEC summary	TM56(170-085,201)
18	PEST1A	4B/F3	Pest for ESR Bits (0-15)	TM56(170-085,201)
19	ERCHK1	4B/F3	ROM check ENABLE	TM56(170-085,201)
20	RCHKST1	4B/F3	ROM check STOP	TM56(170-085,201)
Data bits 21-23 are not used at this time				

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TABLE F MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESRH) FOR HARDWARE ERRORS				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	HCPYERRO	8C/D8	Hardcore parity M/M	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
1	TRAPERRO	8C/B8	CPU trap	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
2	HLDERRO	8C/D8	DMA request hardware time-out	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
3	RDPYERRO	8C/G8	External bus read parity error	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
4	PTFLERRO	8C/C8	IB reply function failure	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
5	CCPYERR1	8F/C6	Incoming CC port parity error	TM41(152-091,195) TM52(152-115,171) TM40(152-085,201) TM42(152-103,183)
6	CNPYERR1	8F/D6	Incoming CN port parity error	TM41(152-091,195) TM52(152-115,171) TM40(152-085,201) TM42(152-103,183)
7	PSTRERRO	8E/D7	Program store parity error	TM37(152-079,207) TM64(152-067,213) TM41(152-091,195)
8	ERLUMBO	20/D8	Unit maintenance bus error	TM41(152-091,195) TM38(144-097,189) TM64(152-067,213) TM37(152-079,207)

TABLE F (Contd) MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESRH) FOR HARDWARE ERRORS				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
9	ERPST0	20/F9	Unit scanner pest error	TM38(144-097,189) TM41(152-091,195)
10			Unassigned	
11	ERUSCN10	19/F8	Unit scan error 1	TM43(144-109,177) TM64(152-067,213)
12	ERUSCN20	19/F8	Unit scan error 2	TM37(152-079,207) TM41(152-091,195)
13	PSTSERR0	8E/C7	Secondary program store parity error	TM64(152-067,213) TM37(152-079,207) TM41(152-091,195)

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**TABLE G (DIF)
MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESRF)**

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING			SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
			VALUE OF BITS 0-7 (OCTAL)	ERROR NAME	MEANING	
0-7	ESR0-ESR7	8G/D6	0	NO ERRORS	No errors	TM40 (152-085, 201) TM42 (152-103, 182) TM52 (152-115, 171) TM41 (152-091, 195) TM38 TM43
			1	MEMOVFL	OS8 memory overload	
			2	INVOP	Invalid MACRO OPCODE	
			3	EXECTO	EXEC MP service T/O	
			4	REPLYF	Compelled response NA	
			5	OUTPUTF	Invalid output request	
			6	SANITYTO	Sanity Time-out (T/O)	
			7	MBUFOVEL	Maintenance buffer overflow T/O	
			10	UNUSEDINT	Unassigned interrupt error	
			12	UNITF	Excessive number of units alarming	
			14	UMBF	UMB failure pattern for ESR	
			15	SCANF	ESR pattern for scanner failure	
			16	ICOUNTFAIL	MP ESR CODE for wrong ICOUNT	
			Undefined	OTHER	Unknown error type	

TABLE H E & P REGISTER EXPANSION*		
(F-LEVEL AC1ER, AC1PRM, AND AC1PRL)		
E REGISTER BITS 21-17 (DECIMAL)		BITS 16-12 (DECIMAL)
VALUE	UNIT TYPE	MEMN
0	Undefined	-
1	MCC/PPI	0
2	SP/DIF	Bits 16-12
3	SCLK	0
4	TMS	Bits 11, 10
5	TSI	Bits 16-11
6	TGR	Bits 16-10
7	IOUS	Bits 16-14
8	Undefined	-
9	EST	Bits 16-12
10	Undefined	-
11	SCS	Bits 16-14
12-31	Undefined	-

* See Figure 4, Page 13. For all PUF type F-Level interrupts from the DIF, a log should be maintained of the contents of the E, P(upper), and P(lower) registers from the interrupt printout. These registers contain the KCODE and instruction sent by the 1B Processor CC over the PU Bus. This table can then be used to break down the contents of these registers and log the results. Obtain assistance per local office procedures if bits 21-17 of the E register indicate some other frame than the SP/DIF or if there is a repeating pattern of OPCODE and Extended OPCODE in recurring interrupts.

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A 26 REPT: F-LEVEL @50250076 MFNUM= 00004667 MICON=00000026 MSG STARTED
LV=0040 D0=01000000 D1=20000000 D2=00000057 D3=00000000
PBFR POSSIBLE SP PULSE POINT TROUBLE
PUFS INTERRUPT DIF 2
PBFR RESOLVED ERROR DIF 2 CONTR 1
PBFR RECOMMENDED REMOVAL LOM DIF 2 CONTR 1
PBFR RECOMMENDED DIAGNOSTICS DIF 2 CONTR 1
PBFR RECOMMENDED RETRY ON DIF 2
FERA REMOVED LOM DIF 2 CONTR 1
FERA SCHED DGN DIF 2 CONTR 1
FERA RETRY PASSED DIF 2
DATA: F-LEVEL
00000020 00000002 00020000 00002525 00005125 00000023
00000000 00015654 00000000 00000023 00000077 50250076
50250076 40260052 00007144 00000341 57630041 00000000
AC1PRL 00000040 00000060 10000003 04000000 00000002 13236172 AC1PRM
50137406 02000417 00000171 50250074 01020000 00000500
00000000 00000006 00000000 00000023 60000000 00000060
00002270 00005125 00002110 00002110 01020000 00000500
00000000 00000006 00000000 00005125 00000000 00005125
00007144 10000003 00000000 00000000 00001052 00407343
03400001 02407402 00401002 00000001
AC1ER

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Figure 4 - Part of F-Level Interrupt Printout

**TABLE I (DIF)
SIGNAL PROCESSOR ERROR SOURCE REGISTER (SPESR)**

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1	BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	LRDEYPO	17D/A9	Parity error on read of ST ROM bits 2-7	TM26(144-085,201) TM30(144-067,219) TM28(144-073,213)	11	LBISERRO	17F/B8	M/M on loopback of IS data-B distribution	TM31(144-049,237) TM30(144-067,219) TM27(144-055,231)
1	URDPYEO	17D/B9	Parity error on read of ST ROM bits 10-15	TM26(144-085,201) TM25(144-067,219) TM28(144-073,213)	12	ESCNERRO	17E/G7	M/M at output of duplicated E scanners	TM29(144-081,195) TM30(144-067,219) TM28(144-073,213)
2	LARPYEO	17D/B9	ST ROM address parity error on read of bits 2-7	TM26(144-085,201) TM25(144-079,207) TM28(144-073,213)	13	EAERRORO	17B/F9	E store/trunk status store address parity error	TM27(144-055,231) TM25(144-079,207) TM30(144-067,219)
3	URAPYEO	17D/B9	ST ROM address parity error on read of bits 8-15	TM26(144-085,201) TM25(144-079,207) TM28(144-073,213)	14	MAERRORO	17B/F9	M store trunk status store address parity error	TM27(144-055,231) TM25(144-079,207) TM30(144-067,219)
4	CCESPYEO		Parity error on cross-controller trunk state loopback	TM26(144-085,201) TM25(144-079,207) TM28(144-073,213)	15	SPARE00		Unused	
5	TSSOPYEO	17D/G9	Parity error on trunk status store output	TM26(144-085,201) TM25(144-079,207) TM28(144-073,213)	16	MDERRORO	17B/F9	M/M on output of duplicated M store	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
6	LABMERRO	17F/B3	M/M on loopback of M signal blocking control-A distribution	TM31(144-049,237) TM30(144-067,219) TM28(144-073,213)	17	ISERRORO	17B/F9	M/M on output of duplicated IS store	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
7	LBBMERRO	17F/B8	M/M on loopback of M signal blocking control-B distribution	TM31(144-049,237) TM30(144-067,219) TM28(144-073,213)	18	XCMDLEO	17B/G9	M/M of duplicated cross-controller loopback of M data	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
8	LAMERRO	17F/A8	M/M on loopback of M data-A distribution	TM31(144-049,237) TM30(144-067,219) TM27(144-055,231)	19	XCISLEO	17B/F9	M/M of duplicated cross-controller loopback of IS data	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
9	LBMERRO	17F/A8	M/M on loopback of M data-A distribution	TM31(144-049,237) TM30(144-067,219) TM27(144-055,231)	20	IBPYEO		Parity error on data loaded from internal bus	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
10	LAISEURO	17F/B3	M/M on loopback of M data-A distribution	TM31(144-049,237) TM30(144-067,219) TM27(144-055,231)	21	EDERRORO	17B/F9	M/M at output of duplicated E store	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
					22	SPARE10		Unused	
					23	SPARE20		Unused	

TABLE J
DIF-E1 REFERENCE

PMD	ESR NAME	ASSOCIATED ERROR SOURCE REGISTER TABLE	
		FOR APUF	FOR PUF
		11,12,14,15,17,21, 25,26,141,142	CLKESR (Clock error)
30-37,40-43,47,50, 51,117,125,150, 151,153,176	CESR for controller with bit 0(ASWF) and/or bit 1(AINT) set	M, Page 19	M, Page 19
154,156,160,161, 162,164,165,166	MPESR for active controller only**	O, Page 21; P, Page 22	O, Page 21; Q, Page 23
54,56,60,61, 62,64,65,66	MPESR for both controllers	O, Page 21; P, Page 22	O, Page 21; P, Page 22 Q*, Page 23
44,45,46,152	CESR(Mismatch error)	M, Page 19	M, Page 19
70,71,72 75,76,77 100,101,102,120 170,171,172,177	CESR		M, Page 19; Q*, Page 23
73,74,121	CESR for standby controller**		M, Page 19; Q*, Page 23
173,174,175	CESR for active controller		M, Page 19; Q*, Page 23
103-107 110-116, 122,123,124	CESR for active controller**		M, Page 19; Q*, Page 23
Table J continued on next page.			

TABLE J (Contd)			
DIF-E1 REFERENCE			
PMD	ESR NAME	ASSOCIATED ERROR SOURCE REGISTER TABLE	
		FOR APUF	FOR PUF
130, 131, 132, 1, 2, 3, 4, 5	No action required		
330, 331 340, 341	CESR	M, Page 19	M, Page 19 Q*, Page 23
350, 360	CESR (active ** controller)		M, Page 19 Q*, Page 23
* = Use TABLE Q to expand "E" and "P" registers for PUFs only ** = Controller is active when CSTATUS bit 7 = 1 (bit 7 = 0 for standby)			

TABLE K		
DIF-E1 REFERENCE (NOTE)		
CESR BIT	SECONDARY ESR NAME	ESR TABLE
10, 11	IBIR	N, Page 20
12	MPESR	O, Page 21
13	SPESR	R, Page 25
14	CLKESR	L, Page 18
15	MAPESR	S, Page 26
NOTE: Packs associated with circuitry recommended in ESR TABLE should be checked per SD-5X400-01 for other possible problems		

CSTATUS	HWSTATUS	MADATA	FSTATUS	DIU0D0	DIU0S1	} C O N T R 0	
CESR	PEST	MPESR	MPRETE	DIUSUM0	DIUSUM1		
CLKESR	SPESR	IBIR	EXR	PSRL	PSRH		
PSVL	PSVH	MAPESR	EXCFESR	EXCMASK	TRKCNTR		
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS		
SPSTATR	MAPCNTRS	MAPREGS	MPSTKPTR	MPPMCNT	MPBSTAT		
URD1	URD2	URD3	URD4	URD5	URD6		
URD7	URD8	URD9	URD10	URD11	URD12		
CCPST0	CCPST1	MPIES	MPRTIS	EXECSMW	0...0		
DACPST0	DACPST1	DRFPST0	DRFPST1	PSSSL	PSSSH		
CALOW	CAHIGH	INTJ	0...0	0...0	0...0		
MEMN	XLATE	FIRMVERS	5...5	5...5	5...5		
CSTATUS	HWSTATUS	MADATA	FSTATUS	DIU0D0	DIU0S1		} C O N T R 1
CESR	PEST	MPESR	MPRETE	DIUSUM0	DIUSUM1		
CLKESR	SPESR	IBIR	EXR	PSRL	PSRH		
PSVL	PSVH	MAPESR	EXCFESR	EXCMASK	TRKCNTR		
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS		
SPSTATR	MAPCNTRS	MAPREGS	MPSTKPTR	MPPMCNT	MPBSTAT		
URD1	URD2	URD3	URD4	URD5	URD6		
URD7	URD8	URD9	URD10	URD11	URD12		
CCPST0	CCPST1	MPIES	MPRTIS	EXECSMW	0...0		
DACPST0	DACPST1	DRFPST0	DRFPST1	PSSSL	PSSSH		
CALOW	CAHIGH	INTJ	0...0	0...0	0...0		

Figure 5 - DIF-E1 CREG Layout

TABLE L
CLOCK ERROR SOURCE REGISTER (CLKESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1	BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	ERACK160	7B23	CK16 energy detector for controller to unit (link A)	TM1(162-067,219) TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)	9	ERBCCSY0	7B25 G0	Clock chain link B Sync pulse error	TM1(162-067,219) TM24(162-085,201)
		D8			10	ERLFMM0	7B25 E7	GGCSY and 10 MSEC clock error	TM24(162-085,201)
1	ERAFSY0	7B23	Frame SYNC energy detector for controller to unit (link A)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)	11	XSFPCSY0	7B25 E8	Super frame Sync error	TM24(162-085,201)
		D8			12	ASAMMO	9B27 G7	Active/standby link A error	TM364(162-073,213)
2	ERBCK160	7B23 E8	CK16 energy detector for controller to unit (link B)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)	13	ASBMM0	9B27 G7	Active/standby link B error	TM364(162-073,213)
3	ERBFSY0	7B23 E8	Frame SYNC energy detector for controller to unit (link B)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)	14	AERSFPS0	7B25 C5	Super frame pattern and SFSY link A error	TM20(144-115,171) TM24(162-085,201)
4	ERAGGCP0	7B23 D8	Combined GGC 32PY and 32SY ESR bit for controller to unit (link A)	TM22(162-103,183) TM1(162-067,219) TM24(162-085,201)	15	BERSFPS0	7B25 C5	Super frame pattern and SFSY link B error	TM20(144-115,171) TM24(162-085,201)
5	ERBGGCP0	7B23 E8	Combined GGC 32PY and 32SY ESR bit for controller to unit (link B)	TM22(162-103,183) TM1(162-067,219) TM24(162-085,201)	16	ERGCCW0	7B25 D5	Clock chain A GGCPY and GWCPY error	TM22(162-103,183) TM20(144-115,171) TM24(162-085,201)
6	ERGCBO	7B23 B8	GBC Parity error	TM22(162-103,183) TM1(162-067,219) TM24(162-085,201)	17	ERCK6GW0	18B58 D7	Clock chain and SFSY ESR	TM20(144-115,171) TM24(162-085,201)
7	ERMMFO	7B23 C9	Minor framing error	TM22(162-103,183) TM24(162-085,201)	18	ER15FSA0	18B58 F7	1.5 MHZ and T1FSY link A error	TM20(144-115,171) TM24(162-085,201)
8	ERACCSY0	7B25 G0	Clock chain link A Sync pulse error	TM1(162-067,219) TM24(162-085,201)	19	ER15FSB0	18B58 F7	1.5 MHZ and T1FSY link B error	TM20(144-115,171) TM24(162-085,201)
					20-23	UNASSIGNED			

**TABLE M
CONTROLLER ERROR SOURCE REGISTER (CESR)**

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT PACK - CONTR 0, CONTR 1	BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT PACK - CONTR 0, CONTR 1
0	ASWFPSO	8B26 B5	All seems well failure - F LEVEL	TM363(162-079,207)	12	MMESRSUM0	12B36 F8	MP ESR summary	TM68(152-091,195) TM363(162-079,207)
1	AINTPSO	8B26 C5	Autonomous interrupt - F LEVEL	TM363(162-079,207)	13	ERLUSPO	15B49 B8	SP ESR summary	TM18(144-055,231) TM363(162-079,207)
2	ERPUBEPY0	3B7 G8	Peripheral unit bus even parity failure	TM6(170-115,171) TM363(162-079,207)	14	ERCKSUM0	7B25 B7	Clock ESR Summary	TM24(162-085,201) TM363(162-079,207)
3	ERPUBOPY0	3B7 G8	Peripheral unit bus odd parity failure	TM6(170-115,171) TM363(162-079,207)	15	EXSUM3	8B26	MAP ESR Summary or Frogger error (MF only)	TM363(162-079,207)
4	INAPUT	12B37 F9	Internal APUT INTERJECT	TM40(152-85,201) TM363(162-079,207)	16	T1LMM0	7B25 E7	T1 line mismatch	TM24(162-085-201) TM363(162-079,207)
5		8B26	APUB	TM363(162-079,207)	17	ERIBMM0	4B15 B6	Internal bus mismatch	TM363(162-079,207)
6		8B26	Unassigned OPCODE received	TM363(162-079,207)	18	RRPYMM0	3B9 E5	PUB reply register mismatch	TM7*(170-097,189) TM363(162-079,207)
7	ERPUBMOD0	3B7 G8	Mode failure	TM6(170-115,171) TM363(162-079,207)	19	PUSEQMM0	3B9 E5	PUB sequencer mismatch	TM7*(170-097,189) TM363(162-079,207)
8	ERMFERMO	7B23 C8	Out-of-frame error	TM22(162-103,183) TM363(162-079,207)	20	SEQMM0	3B9 D4	SP M-Bit mismatch	TM7*(170-097,189) TM363(162-079,207)
9	ERCK160	7B24 C4	16 MBIT clock error	TM23(162-097,195)	21			Unassigned	
10	ERECSUM0	4B15 G6	EXEC ESR summary	TM11(170-043,243) TM363(162-079,207)	22	ERLFMM0	7B25 E8	Low frequency clock mismatch	TM24(162-085,201) TM363(162-079,207)
11	ERIBSUM0	4B15 G6	Internal bus ESR summary	TM11(170-043,243) TM363(162-079,207)	23			Unassigned	

* May be TM371

TABLE N INTERNAL BUS I REGISTER (IBIR)				
BITS (0-9)				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	IBMXAMMO	4B10 H5	IB Multiplexer A – Return mismatch	TM365(170-091,195)
1	IBMXBMMO	4B11 E3	IB Multiplexer B – Return mismatch	TM365(170-085,201)
2	IBMXCMMO	4B11 E7	IB Multiplexer C – Return mismatch	TM365(170-079,207)
3	IBMXDMMO	4B12 F3	IB Multiplexer D – Return mismatch	TM365(170-073,213)
4	IBXEMMO	4B12 C7	IB Multiplexer E – Return mismatch	TM365(170-067,219)
5	ERIBMXPYO	4B13 F7	Receive IB parity error	TM10*(170-055,231) TM11(170-043,243)
6	ERIBAKDESO	4B13 H7	Destination Ack error	TM10*(170-055,231) TM11(170-043,243)
7	ERIBSDLPO	4B13 A7	Source/Dest/opcode loop mismatch	TM10*(170-055,231) TM11(170-043,243)
8	ERIBAKSORO	4B15 G0	Source Ack error	TM10*(170-055,231) TM11(170-043,243)
9	N.A	4B15	Firmware error maintenance buffer	TM11(170-043,243)
10	ERECALUO	5B17 C3	ALU mismatch	TM9(170-031,255) TM11(170-043,243)
* May be TM10B				

TABLE N (Contd) INTERNAL BUS I REGISTER (IBIR)				
BITS (10-15)				
EXECUTIVE ESR				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
11	N. A.	4B15	Firmware error – SP	TM11(170-043,243) TM17(144-067,219)
12	N. A.	4B15	Firmware error – Exec	TM11(170-043,243) TM8(170-019, 267) TM6(170-115, 171)
13	N. A.	4B15	Firmware error – MP	TM11(170-043,243) TM368(152-097,189)
14	ERECMSEQO	4B15 H0	Exec Sequencer Mismatch	TM8(170-019,267) TM11(170-043,243)
15	ERECPYO	5B18	Exec PROM parity error	TM370(170-025,261) TM11(170-043,243)
16	ERIBSUMO	4B15 G5	IB ESR Summary	TM11(170-043,243)
17	ERECSUMO	4B15 G5	Exec ESR Summary	TM11(170-043,243)
18	PEST1A	4B15 F3	Pest for ESR Bits (0-17, 22)	TM11(170-043,243)
19	ERCHK1	4B15 F3	ROM check enable	TM11(170-043,243)
20	RCHKST1	4B15 F3	ROM check stop	TM11(170-043,243)
21	UNASSIGNED			
22	ECERZZO	4B15 H0	Buffer RAM address parity check error	TM11(170-043,243)
23	UNASSIGNED			

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TABLE O MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESR)				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0-7	ESR0-ESR7	12B37 D5	Firmware writable [TABLE P, Page 22]	TM40(152-085,201) TM366*(152-103,183)
8	HCPYERRO	12B34 D8	Hardcore parity M/M	TM366*(152-103,183) TM68(152-091,195)
9	TRAPERRO	12B34 B8	CPU trap error	TM366*(152-103,183) TM68(152-091,195) TM368(152-097,189) TM368(152-109,177) TM366*(152-115,171)
10	HLDERRO	12B34 D8	DMA request hardware time-out	TM366*(152-103,183) TM68(152-091,195)
11	RDPYERRO	12B34 G8	External bus read parity error	TM366*(152-103,183) TM68(152-091,195)
12	PTFLERRO	12B34 C3	Firmware ESR Bit failure	TM366*(152-103,183) TM68(152-091,195)
13	CCPYERR1	12B36 C6	Incoming CC port parity error	TM68(152-091,195) TM40(152-085,201) TM366*(152-103,183)
14	CNPYERR1	12B36 D6	Incoming CN port parity error	TM68(152-091,195) TM40(152-085,201) TM366*(152-103,183)
15	PSTRERRO	12B38 D8	Main program store parity error	TM366*(152-103,183) TM67(152-067,219) TM67(152-073,213) TM57(152-079,207) TM37
* May be TM375				

TABLE O (Contd) MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESR)				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
16	ERLUMBO	16B56 E8	Unit maintenance bus error	TM38(144-103,183) TM68(152-091,195)
17	ERPSTO	16B56 F8	Unit scanner pest error	TM38(144-103,183) TM68(152-091,195)
18			Unit maintenance bus shift register alarm	
19	ERUSCN10	17B57 F8	Unit Scan error 1	TM19(144-109,177) TM67(152-067,219) (152-073,213 079,207) TM68(152-091,195)
20	ERUSCN20	17B57 F8	Unit Scan error 2	
21			Unassigned	
22	HALTERO	12B36 F5	MP halt error	TM68(152-091,195) TM366*(152-103,183)
23	HLPST1	12B36 F4	Pest bit for MP halt error	TM68(152-091,195)
* May be TM375				

ANALYZE DIFR F-LEVEL INTERRUPT

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**TABLE P
FIRMWARE ERROR SOURCE REGISTER**

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING			SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
			VALUE OF BITS 0-7 (OCTAL)	ERROR NAME	BIT MEANING	
0-7	ESR0-ESR7	12B37 D5	0	NOERRORS	No errors	TM40(152-085,201) TM366*(152-103,183) TM365(170-067,219)
			1	MEMOVFL	OS8 memory overload	
			2	INVOP	Invalid MACRO OPCODE	
			3	EXECTO	EXEC MP service T/O	
			4	REPLYF	Compelled response NA	
			5	OUTPUTF	Invalid output request	
			6	SANITYTO	Sanity time-out (T/O)	
			7	MBUFOVEL	Maintenance buffer overflow T/O	
			10		Unassigned (interrupt error)	
			11		Unassigned	
			12	UNITF	Unit failure code ESR	
			13	DGF	DG failure code ESR	
			14	UMBF	UMB failure pattern for ESR	
			15	SCANF	ESR pattern for scanner failure	
			16	ICOUNTFAIL	MP ESR CODE for wrong ICOUNT	
			17	FIRMF	Micro DCON Firmware Failure	
			20	MPAUDITERROR	MP PROG. Store Audit Failure	
			21	SPAUDITERROR	SP PROG. Store Audit Failure	

* May be TM375

TABLE Q E & P REGISTER EXPANSION*		
(F-LEVEL AC1ER, AC1PRM, AND AC1PRL)		
E REGISTER BITS 21-17 (DECIMAL)		BITS 16-12 (DECIMAL)
VALUE	UNIT TYPE	MEMN
0	Undefined	—
1	MCC/PPI	0
2	SP/DIF	Bits 16-12
3	SCLK	0
4	TMS	Bits 11, 10
5	TSI	Bits 16-11
6	TGR	Bits 16-10
7	IOUS	Bits 16-14
8	Undefined	—
9	EST	Bits 16-12
10	Undefined	—
11-31	Undefined	—

* See Figure 6, Page 24. For all PUF type F-Level interrupts from the DIF-E1, a log should be maintained of the contents of the E, P(upper), and P(lower) registers from the interrupt printout. These registers contain the KCODE and instruction sent by the 1B Processor CC over the PU Bus. This table can then be used to break down the contents of these registers and log the results.

Obtain assistance per local office procedures if bits 21-17 of the E register indicate some other frame than the SP/DIF-E1 or if there is a repeating pattern of OPCODE and Extended OPCODE in recurring interrupts.

```

A 26 REPT: F-LEVEL @50250076 MFNUM= 00004667 MICON=00000026 MSG STARTED
LV=0040 D0=01000000 D1=20000000 D2=00000057 D3=00000000
PBFR POSSIBLE SP PULSE POINT TROUBLE
PUFS INTERRUPT DIF 2
PBFR RESOLVED ERROR DIF 2 CONTR 1
PBFR RECOMMENDED REMOVAL LOM DIF 2 CONTR 1
PBFR RECOMMENDED DIAGNOSTICS DIF 2 CONTR 1
PBFR RECOMMENDED RETRY ON DIF 2
FERA REMOVED LOM DIF 2 CONTR 1
FERA SCHED DGN DIF 2 CONTR 1
FERA RETRY PASSED DIF 2
DATA: F-LEVEL
00000020 00000002 00020000 00002525 00005125 00000023
00000000 00015654 00000000 00000023 00000077 50250076
50250076 40260052 00007144 00000341 57630041 00000000
AC1PRL 00000040 00000060 10000003 04000000 00000002 13236172 AC1PRM
50137406 02000417 00000171 50250074 01020000 00000500
00000000 00000006 00000000 00000023 60000000 00000060
00002270 00005125 00002110 00002110 01020000 00000500
00000000 00000006 00000000 00005125 00000000 00005125
00007144 10000003 00000000 00000000 00001052 00407343
03400001 02407402 00401002 00000001
AC1ER

```

Figure 6 - Part of F-Level Interrupt Printout

**TABLE R
SIGNAL PROCESSOR ERROR SOURCE REGISTER (SPESR)**

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1	BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	NTSPYER0	15B53 B9	State translator parity error	TM682(144-085,201) TM17(144-067,219)	11			Unassigned	
1	CTSPYER0	15B53 F8	Current trunk state parity error	TM682(144-085,201) TM4(144-079,207)	12	ESCNERRO	15B55 G7	E Bit Scanner mismatch	TM362 (144-097,189) TM5 (144-043,243) TM17 (144-067,219)
2	LTJMPMM0	15B53 E8	Looped jump control mismatch	TM682(144-085,201) TM17(144-067,219)	13	EADERO	15B48 F9	E Bit store – address error	TM16* (144-049,237) TM17 (144-067,219)
3	LRFMM0	15B53 E8	Looped RPTFLG control mismatch	TM682(144-085,201) TM17(144-067,219)	14	MADERO	15B48 F9	M Bit store – address parity error	TM16* (144-049,237) TM17 (144-067,219)
4	LAESERO	15B47 B8	Block of M Bit distribution update mismatch (0-15, 32)	TM5(144-043,243)	15	EDERO	15B48 F9	Duplicated E Bit store mismatch	TM16* (144-049,237) TM17 (144-067,219)
5	LBESERO	15B47 B8	Block of M Bit distribution update mismatch (16-31, 33)	TM5(144-043,243)	16	MDERO	15B48 F9	Duplicated M Bit store mismatch	TM16* (144-049,237) TM17 (144-067,219)
6	LAMERO	15B47 A8	M BIT distribution loop mismatch (0-15, 32)	TM5(144-043,243) TM16*(144-049,237)	17	ISERO	15B48 G9	Duplicated PCIS store mismatch	TM16* (144-049,237) TM17 (144-067,219)
7	LBMERO	15B47 A8	M BIT distribution loop mismatch (16-31, 33)	TM5(144-043,243) TM16*(144-049,237)	18	XCMDLEO	15B48 F9	Looped cross controller M Bit data mismatch	TM16* (144-049,237) TM17 (144-067,219)
8	LAISERO	15B47 B8	Loop PCIS distribution mismatch (0-15, 32)	TM5(144-043,243) TM16*(144-049,237)	19	XCISLEO	15B48 G9	Looped cross controller PCIS data mismatch	TM16* (144-049,237) TM17 (144-067,219)
9	LBISERO	15B47 B8	Loop PCIS distribution mismatch (16-31, 33)	TM5(144-043,243) TM16*(144-049,237)	20	IBPYER0	15B48 A9	Internal bus data error	TM16* (144-049,237) TM17 (144-067,219)
10	CCTSPYE0	15B52 C9	Cross controller trunk state mismatch	TM4(144-079,207)	21	TSSADPYE1	15B51 E8	TSS address parity error	TM15 (144-073,213) TM365 (170-091,195)
* May be TM372 or TM684					22	CTSEBERO	15B53 E9	Current trunk state E bit mismatch	TM682 (144-085,201) TM16* (144-049,237)
					23			Unassigned	

TABLE S
MESSAGE ACCOUNTING PROCESSOR ESR BITS 0-9 AND STATUS REGISTER BITS 21-23 (MAPESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	EXR BITS	SUSPECT CIRCUIT PACKS CONT 0, CONTR 1
0	EIBDO	14B41/F0	Parity error over Rcvd IB Data	1,2	TM303* (152-037,249) TM302† (152-043,243)
1	EPTSS0	14B41/F0	Parity error when PTSS is read	1,2	TM303* (152-037,249) TM304 (152-031,255)
2	EPTSRPS0	14B41/F0	Parity error when PTRSRS is read	1,2	TM303* (152-037,249) TM305 (152-019,267)
3	ETRKCTRO	14B41/F0	Read and write trunk counters are out of step	1,2	TM303* (152-037,249) TM304 (152-031,255)
4	EXCLO	14B41/F0	X-CONT UPDATE data link faulty	1,2	TM303* (152-037,249) TM307 (152-025,261)
5	EPPMO	14B41/F0	P-bit link to SP faulty	1,2	TM303* (152-037,249) TM304 (152-031,255)
6	EMUX0	14B41/F0	PTSS Multiplex data fails parity	1,2	TM303* (152-037,249) TM305 (152-019,267)
7	EBPIO	14B41/F0	Data link between PROC and PTSS fails parity	1,2	TM303* (152-037,249) TM307 (152-025,261)
8	EPSADO	14B41/F0	Parity error over P store address	1,2	TM303* (152-037,249) TM304 (152-031,255)
9	EGB3CLK0	14B41/F0	Pipeline CLK to PROC and PTSS memory pack failed loop check	1,2,3	TM303* (152-037,249) TM304 (152-031,255)
21	STOP1A	14B41/A0	Reclocked STOP status bit	-	TM303* (152-037,249) TM1 (152-067,219)
22	UPDAT1	14B41/A0	Reclocked UPDATE status bit	-	TM303* (152-037,249) TM1 (152-067,219)
23	WPEST0	14B41/E1	Pest for all ESR bits (0-9)	-	TM303* (152-037,249) TM304 (152-031,255)
* May be TM374					
† May be TM373					

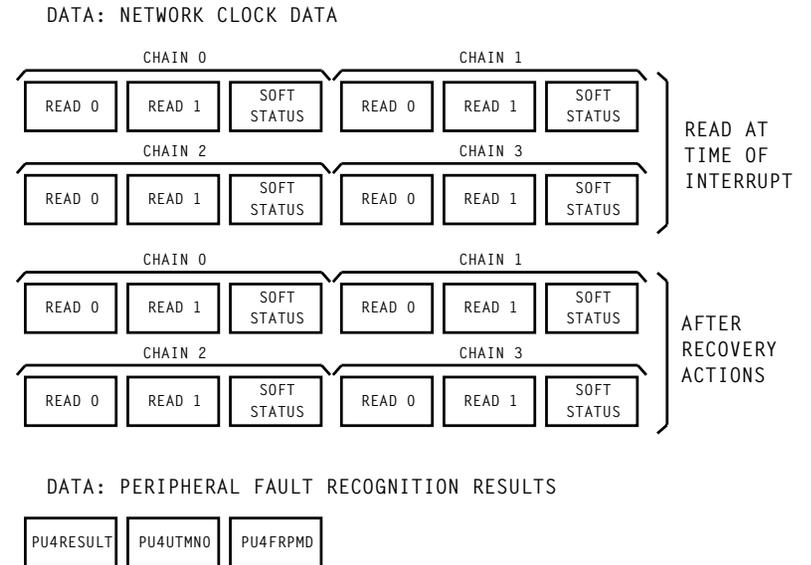
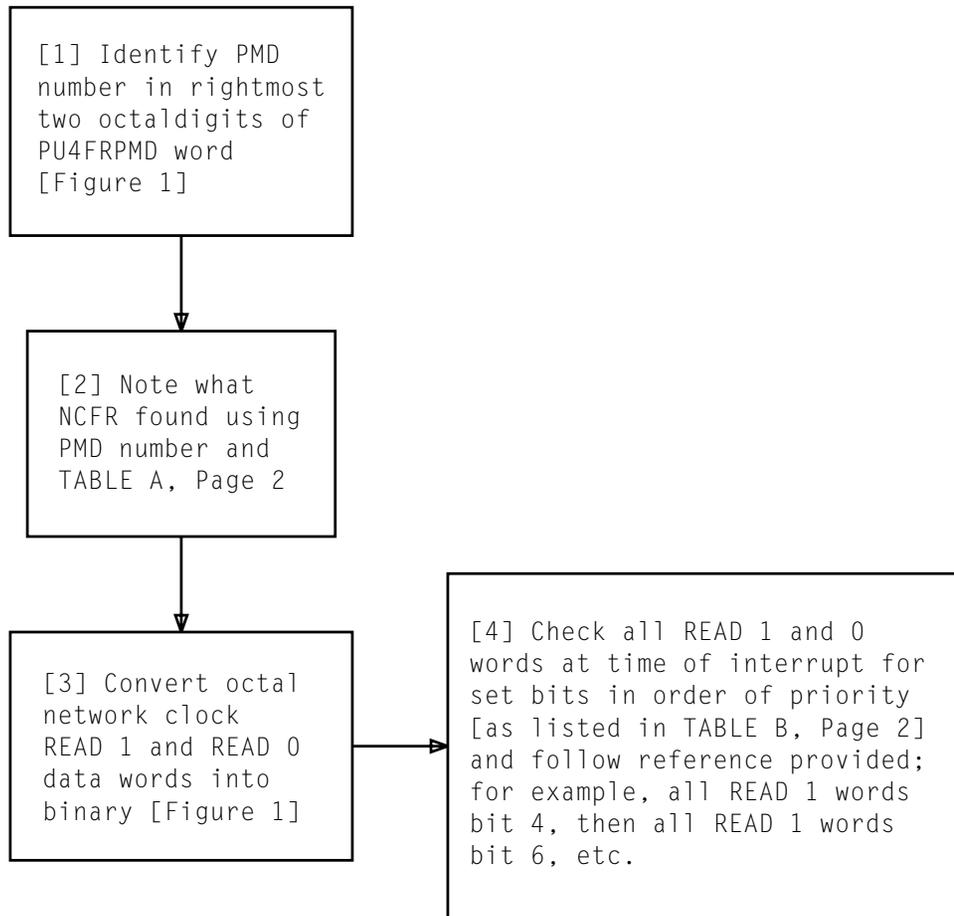


Figure 1 - Check Register Layout

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

TABLE A PMD DESCRIPTION					
PMD*	NCFR FOUND	PMD*	NCFR FOUND	PMD*	NCFR FOUND
1	Fanout level detector	12	No errors found	26	Chain 10 counter failed
2	Master oscillator level detector	13	Phase lock oven control is out of range	27	Chain 11 counter failed
3	Oscillator level detector fault	14	Error summary circuits failed	30	Chain 00 matcher failed
4	Chain is being removed at random because two matchers were indicated, which is invalid combination except for double faults	15	Phase Fault-transient	31	Chain 01 matcher failed
		16	Unassigned	32	Chain 10 matcher failed
		17	Output disconnect fault	33	Chain 11 matcher failed
		20	Single MSL (Master Select Level) error	34	Chain failed access test
		21	Master oscillator fault		
5	Matcher 00	22	Phase fault – hard	35	Master select failure
6	Matcher 01	23	Fanout level detector	36	Frame pulse detector
7	Matcher 10	24	Chain 00 counter failed	37	Output Disconnect fault
10	Matcher 11				
11	Two chains 00S and matchers up	25	Chain 01 counter failed		
* PMDs 1-17 are transient errors; PMDs 20-37 are hard faults					

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

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**TABLE B
READ 0 AND 1 WORDS – BIT PRIORITIES* AND RELATED FAULT CONDITIONS**

WORD*	BITS*	BIT DESCRIPTION	CONDITIONS	REFERENCE
1	4	Oscillator level detector	Suspect packs and leads in chain with bit 4 set	TABLE C – Page 5
1	6	Master select level detector	Suspect packs and leads in chain with bit 6 set	TABLE D – Page 5
1	12	Phase lock oven monitor	Suspect packs and leads in chain with bit 12 set	TABLE E – Page 6
1	5	Oscillator phase detector	A. Bit 5 set in more than one chain; clear phase error	234-351-013
			B. Bit 5 set in one chain; check phase meter in chain with bit 5 set a. If PHASE meter reads greater than plus or minus 3 degrees from zero, clear phase error b. If PHASE meter reads plus or minus 3 degrees or less from zero, suspect packs and leads in this chain	234-351-013
				TABLE F – Page 6
1	7	Phase unlock detector	A. Bit 7 set in one chain; suspect packs and leads in that chain	TABLE G – Page 6
			B. Bit 7 set in more than one chain; clear phase error	234-351-013
0	2 thru 11	Fanout level detector – BRANCH A through Fanout level detector – BRANCH J	A. More than one bit (2-11) set; suspect packs and leads for chain with bit set	TABLE H – Page 7
			B. Single bit (2-11) set; suspect packs and leads for chain with bit set	TABLE I – Page 8
1	10	Error summary	A. Bit 10 set in one chain; bit 0 set in all four chains; no Read 0 bits set; and no other Read 1 bits set; suspect packs and leads in chain with bit 10 set	TABLE J – Page 9
			B. Bit 10 set in one chain and bit 1, 2, or 3 set in same chain; suspect packs and leads in this chain	TABLE K – Page 9

* Words and bits are listed in order of priority

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

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TABLE B (Contd)				
READ 0 AND 1 WORDS – BIT PRIORITIES* AND RELATED FAULT CONDITIONS				
WORD*	BITS*	BIT DESCRIPTION	CONDITIONS	REFERENCE
0	0	Frame matcher	A. Bit 0 set in one chain and bit 1 not set in any chain, suspect packs and leads in chain having bit 0 set	TABLE L – Page 9
			B. Bit 0 set in three chains and bit 1 not set in any chain, determine common chain [TABLE M] and suspect packs and leads in common chain [TABLE N]	TABLE M – Page 10 TABLE N – Page 10
			C. Bit 0 and bit 1 set in same chain, suspect pack in that chain	TABLE O – Page 10
			D. Bit 0 and bit 1 set in three chains, determine common chain [TABLE M] and suspect packs and leads in common chain (TABLE P)	TABLE M – Page 10 TABLE P – Page 10
			E. Bit 0 set in two chains and bit 1 set in three chains, determine common chain [TABLE M] and suspect packs and leads in common chain [TABLE Q]	TABLE M – Page 10 TABLE Q – Page 11
0	1	Counter matcher	Bit 1 set in one chain, suspect packs and leads for that chain	TABLE R – Page 11
All other READ 0 and 1 word bits are DON'T CARE				
* Words and bits are listed in order of priority				

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

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TABLE C OSCILLATOR/MASTER SELECT LEVEL ERROR				
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-34	00SCA	1	24
	070-31	00SCLE1	1	5
	070-29	00SCLEPO	1	1
	070-23	0SOSCLEO	12	4
		0SOSCLDO		
	044-35	*OSCILLATOR		
1	070-37	10SCA	2	24
	070-40	10SCLE1	2	5
	070-42	10SCLEPO	2	1
	070-48	1SOSCLEO	13	4
		1SOSCLDO		
	033-35	*OSCILLATOR		
2	170-34	00SCA	1	24
	170-31	00SCLE1	1	5
	170-29	00SCLEPO	1	1
	170-23	0SOSCLEO	12	4
		0SOSCLDO		
	144-35	*OSCILLATOR		
3	170-37	10SCA	2	24
	170-40	10SCLE1	2	5
	170-42	10SCLEPO	2	1
	170-48	1SOSCLEO	13	4
		1SOSCLDO		
	133-35	*OSCILLATOR		

*If pack replacement does not clear trouble, check oscillator (level) before replacing oscillator

TABLE D MASTER SELECT LEVEL ERROR WITH OR WITHOUT PHASE ERROR									
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01			CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM			LEAD	FS	SYM
0	070-32	0MOSCS	1	2	2	170-32	0MOSCS	1	2
	070-31	0MSLE1	1	4		170-31	0MSLE1	1	4
	070-29	0MSLEPO	1	1		170-29	0MSLEPO	1	1
	070-23	0SMSLDO	12	4		170-23	0SMSLDO	12	4
	070-34	OUTPUT*	1	24		070-34	OUTPUT*	1	24
1	070-39	1MOSCS	2	2	3	170-39	1MOSCS	2	2
	070-40	1MSLE1	2	4		170-40	1MSLE1	2	4
	070-42	1MSLEPO	2	1		170-42	1MSLEPO	2	1
	070-48	1SMSLDO	13	4		170-48	1SMSLDO	13	4
	070-34	OUTPUT*	1	24		070-34	OUTPUT*	1	24

*Clock distribution driver output leads to master oscillator selector

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TABLE E PHASE LOCK OVEN ERROR				
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	078-20	0PLOMPO	1	11
	070-23	0SPLOM1	12	4
	066-33	0TCBCTL	1	9
	066-31	0TEMCTLP	1	12
	066-34	0TEMCTLP	1	13
	Check PHASE LOCK OVEN TEMP meter [DLP-524]			
1	078-52	1PLOMPO	2	11
	170-48	1SPLOM1	13	4
	066-39	1TCBCTL	2	9
	066-40	1TEMCTLP	2	12
	066-37	1TEMCTLP	2	13
	Check PHASE LOCK OVEN TEMP meter [DLP-524]			
2	178-20	0PLOMPO	1	11
	070-23	0SPLOM1	12	4
	166-33	0TCBCTL	1	9
	166-31	0TEMCTLP	1	12
	166-34	0TEMCTLP	1	13
	Check PHASE LOCK OVEN TEMP meter [DLP-524]			
3	178-52	1PLOMPO	2	11
	170-48	1SPLOM1	13	4
	166-39	1TCBCTL	2	9
	166-40	1TEMCTLP	2	12
	166-37	1TEMCTLP	2	13
	Check PHASE LOCK OVEN TEMP meter [DLP-524]			

TABLE F PHASE LOCK ERROR AND PHASE METER EQUAL TO OR LESS THAN 3 DEGREES				
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-29	0PLEPO	1	1
	070-23	0SPLLEO	12	4
1	070-42	1PLEPO	2	1
	070-48	1SPLLEO	13	4
2	170-29	0PLEPO	1	1
	170-23	0SPLLEO	12	4
3	170-42	1PLEPO	2	1
	170-48	1SPLLEO	13	4

TABLE G PHASE UNLOCK ERROR IN ONE CHAIN				
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-29	0PULEPO	1	1
	070-23	0SPUEDLO	12	4
		0SPUEDMO		
	Clear phase error 234-351-013			
1	070-42	1PULEPO	2	1
	070-48	1SPUEDLO	13	4
		1SPUEDMO		
	Clear phase error 234-351-013			
2	170-29	0PULEPO	1	1
	170-23	0SPUEDLO	12	4
		0SPUEDMO		
	Clear phase error 234-351-013			
3	170-42	1PULEPO	2	1
	170-48	1SPUEDLO	13	4
		1SPUEDMO		
	Clear phase error 234-351-013			

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**TABLE H
MULTIPLE FANOUT LEVEL ERRORS**

READ 0 BITS 2 THRU 11 SET					READ 0 BITS 2 THRU 6 SET			READ 0 BITS 7 THRU 11 SET				
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01			SUSPECT PACK LOCATION	SD-4A036-01			SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM		LEAD	FS	SYM		LEAD	FS	SYM
0	070-26	OCLFODR	5	1	074-27	OCLFODR	5	2	074-26	OCLFODR	5	3
1	070-45	1CLFODR	6	1	074-44	1CLFODR	6	2	074-45	1CLFODR	6	3
2	170-26	OCLFODR	5	1	174-27	OCLODR	5	2	174-26	OCLFODR	5	3
3	170-45	1CLFODR	6	1	174-44	1CLFODR	6	2	174-45	1CLFODR	6	3

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**TABLE I
SINGLE FANOUT LEVEL ERROR**

TABLE I SINGLE FANOUT LEVEL ERROR																
CHAIN 0					CHAIN 1				CHAIN 2				CHAIN 3			
BIT	SUSPECT PACK LOCATION	SD-4A036-01														
		LEAD	FS	SYM												
2	070-25	0FOMPOA	10	1	070-46	1FOMPOA	11	1	170-25	0FOMPOA	10	1	170-46	1FOMPOA	11	1
	074-27	0CLFOD1A	5	2	074-44	1CLFOD1A	6	2	174-27	0CLFOD1A	5	2	174-44	1CLFOD1A	6	2
3	070-25	0FOMPOB	10	1	070-46	1FOMPOB	11	1	170-25	0FOMPOB	10	1	170-46	1FOMPOB	11	1
	074-27	0CLFOD1B	5	2	074-44	1CLFOD1B	6	2	174-27	0CLFOD1B	5	2	174-44	1CLFOD1B	6	2
4	070-25	0FOMPOC	10	1	070-46	1FOMPOC	11	1	170-25	0FOMPOC	10	1	170-46	1FOMPOC	11	1
	074-27	0CLFOD1C	5	2	074-44	1CLFOD1C	6	2	174-27	0CLFOD1C	5	2	174-44	1CLFOD1C	6	2
5	070-25	0FOMPOD	10	1	070-46	1FOMPOD	11	1	170-25	0FOMPOD	10	1	170-46	1FOMPOD	11	1
	074-27	0CLFOD1D	5	2	074-44	1CLFOD1D	6	2	174-27	0CLFOD1D	5	2	174-44	1CLFOD1D	6	2
6	070-25	0FOMPOE	10	1	070-46	1FOMPOE	11	1	170-25	0FOMPOE	10	1	170-46	1FOMPOE	11	1
	074-27	0CLFOD1E	5	2	074-44	1CLFOD1E	6	2	174-27	0CLFOD1E	5	2	174-44	1CLFOD1E	6	2
7	070-25	0FOMPOF	10	1	070-46	1FOMPOF	11	1	170-25	0FOMPOF	10	1	170-46	1FOMPOF	11	1
	074-26	0CLFOD1F	5	3	074-45	1CLFOD1F	6	3	174-26	0CLFOD1F	5	3	174-45	1CLFOD1F	6	3
8	070-25	0FOMPOG	10	1	070-46	1FOMPOG	11	1	170-25	0FOMPOG	10	1	170-46	1FOMPOG	11	1
	074-26	0CLFOD1G	5	3	074-45	1CLFOD1G	6	3	174-26	0CLFOD1G	5	3	174-45	1CLFOD1G	6	3
9	070-25	0FOMPOH	10	1	070-46	1FOMPOH	11	1	170-25	0FOMPOH	10	1	170-46	1FOMPOH	11	1
	074-26	0CLFOD1H	5	3	074-45	1CLFOD1H	6	3	174-26	0CLFOD1H	5	3	174-45	1CLFOD1H	6	3
10	070-25	0FOMPOI	10	1	070-46	1FOMPOI	11	1	170-25	0FOMPOI	10	1	170-46	1FOMPOI	11	1
	074-26	0CLFOD1I	5	3	074-45	1CLFOD1I	6	3	174-26	0CLFOD1I	5	3	174-45	1CLFOD1I	6	3
11	070-25	0FOMPOJ	10	1	070-46	1FOMPOJ	11	1	170-25	0FOMPOJ	10	1	170-46	1FOMPOJ	11	1
	074-26	0CLFOD1J	5	3	074-45	1CLFOD1J	6	3	174-26	0CLFOD1J	5	3	174-45	1CLFOD1J	6	3

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TABLE J MASTER SELECT 0 IN ALL CHAINS AND ERROR SUMMARY IN ONE CHAIN				
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-21	0ESPO	14	4
	070-29	00SCES	1	1
	070-23	0I00MSE1	12	4
	074-28	0MES1	8	1
	070-25	0F0MES1	10	1
	078-20	0P0LES1	1	11
	1	070-50	1ESPO	15
070-42		10SCES	2	1
070-48		1I00MSE1	13	4
074-43		1MES1	9	1
070-46		1F0MES1	11	1
078-52		1P0LES1	2	11
2	170-21	0ESPO	14	4
	170-29	00SCES	1	1
	170-23	0I00MSE1	12	4
	174-28	0MES1	8	1
	170-25	0F0MES1	10	1
	178-20	0P0LES1	1	11
3	170-50	1ESPO	15	4
	170-42	10SCES	2	1
	170-48	1I00MSE1	13	4
	174-43	1MES1	9	1
	170-46	1F0MES1	11	1
	178-52	1P0LES1	2	11

TABLE K MASTER SELECT 1, 2, OR 3 WITH ERROR SUMMARY IN ONE CHAIN				
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEADS	FS	SYM
0	070-29	Master select control input- output leads	1	1
1	070-42		2	1
2	170-29		1	1
3	170-42		2	1

TABLE L FRAME MATCH ERROR IN ONE CHAIN				
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	074-28	0FMPO	8	1
	070-27	0FRSO	3	2
	074-27	0CLFOMA	5	2
	074-44	1CLFOMB	6	2
	174-45	1CLFOMOC	6	3
1	074-43	1FMPO	9	1
	070-44	1FRSO	4	2
	074-44	1CLFOMA	6	2
	074-27	0CLFOMB	5	2
2	174-26	0CLFOMOC	5	3
	174-28	0FMPO	8	1
	170-27	0FRSO	3	2
	174-27	0CLFOMA	5	2
3	174-44	1CLFOMB	6	2
	074-26	0CLFOMOC	5	3
	174-43	1FMPO	9	1
	170-44	1FRSO	4	2
3	174-44	1CLFOMA	6	2
	174-27	0CLFOMB	5	2
	074-45	1CLFOMOC	6	3

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TABLE M DETERMINE COMMON CHAIN	
THREE CHAINS WITH READ 0 BIT 0 OR 1 SET	COMMON CHAIN
0, 1, 2	0
0, 1, 3	1
1, 2, 3	2
0, 2, 3	3

TABLE O FRAME MATCH AND COUNTER MATCH ERROR IN ONE CHAIN			
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01	
		FS	SYM
0	074-28	8	1
1	074-43	9	1
2	174-28	8	1
3	174-43	9	1

TABLE P FRAME MATCH ERROR AND COUNTER MATCH ERROR IN THREE CHAINS				
COMMON CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-27	0FRM1A 0FRM1B 0FRM1C 0FRCS0	3	2
	070-28	0CLCM	3	1
1	070-44	1FRM1A 1FRM1B 1FRM1C 1FRCS0	4	2
	070-43	1CLCM	4	1
2	170-27	0FRM1A 0FRM1B 0FRM1C 0FRCS0	3	2
	170-28	0CLCM	3	1
3	170-44	1FRM1A 1FRM1B 1FRM1C 1FRCS0	4	2
	170-43	1CLCM	4	1

TABLE N FRAME MATCHER ERROR IN THREE CHAINS AND NO COUNTER MATCH ERROR				
COMMON CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-26	0CLFODR	5	1
	070-27	0FRCS0	3	2
1	070-45	1CLFODR	6	1
	070-44	1FRCS0	4	2
2	170-26	0CLFODR	5	1
	170-27	0FRCS0	3	2
3	170-45	1CLFODR	6	1
	170-44	1FRCS0	4	2

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TABLE Q FRAME MATCHER ERROR IN TWO CHAINS AND COUNTER MATCH ERROR IN THREE CHAINS				
COMMON CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-27	0FRCS0	3	2
	070-23	0STCPST1	12	4
1	070-44	1FRCS0	4	2
	070-48	1STCPST1	13	4
2	170-27	0FRCS0	3	2
	170-23	0STCPST1	12	4
3	170-44	1FRCS0	4	2
	170-48	1STCPST1	13	4

TABLE R COUNTER MATCH ERROR ONLY (ONE CHAIN)									
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01			CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM			LEAD	FS	SYM
0	074-28	0CMPO	8	1	2	174-28	0CMPO	8	1
		0FRM1A					0FRM1A		
		1FRM1B					1FRM1B		
		0FRMI1C					0FRMI1C		
0	070-27	0FRM1A	3	2	2	170-27	0FRM1A	3	2
	070-44	1FRM1B	4	2		170-44	1FRM1B	4	2
	170-44	1FRM01C	4	2		070-27	0FRM01C	3	2
1	074-43	1CMPO	9	1	3	174-43	1CMPO	9	1
		1FRM1A					1FRM1A		
		0FRM1B					0FRM1B		
		1FRMI1C					1FRMI1C		
1	070-44	1FRM1A	4	2	3	170-44	1FRM1A	4	2
	070-27	0FRM1B	3	2		170-27	0FRM1B	3	2
	170-27	0FRM01C	3	2		070-44	1FRM01C	4	2

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[1] Using SCLK F-level printout, identify PMD number in rightmost two octal digits of PU4FRPMD word [Figure 1]

[2] Is PMD number 11, 12, or 16 through 21

[3] Analyze NCFR F-level interrupt [TAP-127]

[4] Is PMD any number 70 through 74

[5] Read PMD description in TABLE A, Page 2

[6] Note PMD description in TABLE A, Page 2

AND

[8] Is any bit 0 through 6 set to one in RCNT+15 or RCNT+16 word [Figure 2]

[7] Identify suspect controller from F-level printout header text _____

DATA: PERIPHERAL FAULT RECOGNITION RESULTS

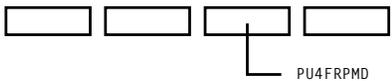


Figure 1

ERROR ANALYSIS HISTORY TABLE

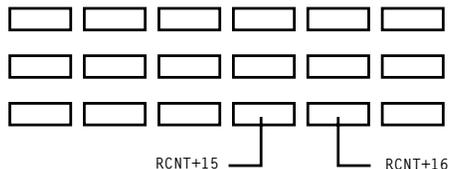


Figure 2

[12] Use TABLE C, Page 3, to identify suspect packs and leads in suspect CONTR. Use TOP 234-351-013 to replace SCLK circuit pack

[9] Is bit 7 set to one in RGNT+15 or RGNT+16

[10] Is AC1LR register all zeros [Figure 3]

[11] Use TABLE B, Page 3, to identify suspect packs and leads in suspect CONTR. Use TOP 234-351-013 to replace SCLK circuit pack



Figure 3

ANALYZE SCFR F-LEVEL INTERRUPT, SYSTEM CLOCK

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TABLE A
PMD DESCRIPTIONS

PMD	SCFR FOUND	PMD	SCFR FOUND	PMD	SCFR FOUND	PMD	SCFR FOUND	PMD	SCFR FOUND
1	Neither controller had errors	13	Duplex CONFIG; counter mismatch not resolved	23	Error not resolved	35	Simplex, enable not set, controller 0 in service	45	Simplex, M bit not set, controller 0 in service
2	Both controllers found to be OS	14	System clock has counter fault and controller 0 is in service	24	Duplex CONFIG; controller 0 had error	36	Simplex, enable not set; controller 1 in service	46	Simplex, M bit not set, controller 1 in service
3	Both controllers are in service and controller 1 had ASWF			25	Duplex CONFIG; controller 1 had error			47	Both controllers in service but only controller 0 recorded mode failure incorrectly
4	Both controllers are in service and controller 0 had ASWF	15	System clock has counter fault and controller 1 is in service	26	Reply register mismatch; only controller 0 had error	37	Both controllers recorded invalid OPCODE erroneously	50	Both controllers in service but only controller 1 recorded mode failure incorrectly
5	Controller 0 had ASWF by itself			27	Reply register mismatch; only controller 1 had error	40	Only controller 0 on line recorded invalid OPCODE erroneously		
6	Controller 1 had ASWF by itself	16	Network clock bay 1 is in trouble and system clock controller 0 is in service	30	Reply register mismatch; error not resolved	41	Only controller 1 on line recorded invalid OPCODE erroneously	51	Both controllers recorded mode failure incorrectly
7	Both controllers are in service and controller 0 had counter mismatch			31	Duplex, failing OPCODE			52	Only controller 0 in service and it recorded mode failure erroneously
10	Both controllers are in service and controller 1 had counter mismatch	17	Network clock bay 1 is in trouble and system clock controller 1 is in service	32	Simplex, failing OPCODE, controller 0 in service	42	Controllers are duplexed and only controller 0 recorded invalid OPCODE incorrectly	53	Only controller 1 in service and it recorded mode failure erroneously
11	Network clock bay 0 is faulty			33	Simplex, failing OPCODE, controller 1 in service			54	Could not find any parity errors
12	Network clock bay 1 is faulty	20	Network clock bay 0 is in trouble and system clock controller 1 is in service	34	Duplex, enable not set	43	Controllers are duplexed and only controller 1 recorded invalid OPCODE incorrectly	54	Could not find any parity errors
				21	Network clock bay 0 is in trouble and system clock controller 1 is in service				
		22	Error not resolved						

TABLE A (Contd) PMD DESCRIPTIONS	
PMD	SCFR FOUND
55	Even parity in simplex controller 0 controller 0
56	Odd parity in simplex
57	Even parity in simplex controller 1
60	Odd parity in simplex controller 1
61	Even, odd, or mixed parities in duplex controllers
62	Even parity in duplex controller 0
63	Even parity in duplex controller 1
64	Odd parity in duplex controller 0
65	Odd parity in duplex controller 1
66	Even parity in duplex controllers 0 and 1
67	Odd parity in duplex controllers 0 and 1
70	SYSClk duplexed with NCSU ASWF in only one controller's ESR
71	SCLK duplex with NCSU ASWF error bit set in controller 1
72	SCLK simplex with NCSU ASWF error bit set in in-service SCLK controller
73	SCLK duplex with NCSU ASWF error bit set in both SCLK controllers
74	SYNC Unit caused reply register mismatch in duplex SCLK controllers

TABLE B AC1LR REGISTER ALL ZEROS						
UNIT	SUSPECT PACK		LEAD†	FS‡	SYM‡	COMMENT
	TYPE	LOCATION				
SCLU IPUB	FA1237	060-32	*0BCLMP1	2	31	
		160-32	*1BCLMP1	3	31	
	OPSC2 RELAY	055-59	0BSEL	12	30	Contact 2M (SCLK CONTR 0)
	1PSC2 RELAY	155-59	1BSEL	13	30	Contact 2M (SCLK CONTR 1)
SCLK	FC12	†56-44	\$MABB	8	1	

* SCLK CONTR
† SCLK Suspect pack bay location – SCLK controller number
‡ SCLK – SD-4A037-02, NCLK – SD-4A014-02
\$ BUS

TABLE C AC1LR REGISTER NOT ZEROED						
UNIT	SUSPECT PACK		LEAD†	FS‡	SYM‡	COMMENT
	TYPE	LOCATION†				
SCLK	FA1807	†56-41	RPASW0	9	2	
	FA641	†56-42	*ASW0	9	1	
SCLU IPUB	FA1237	060-31	0ASW	2	32	BUS 0
		160-31	1ASW	3	32	BUS 1
	FC13	060-27	0PUASWP/NI	2	12	BUS 0
		160-27	1PUASWP/NI	3	12	BUS 1

* BUS
† SCLK Suspect bay location – SCLK controller number
‡ SCLK – SD-4A037-02, NCLK – SD-4A014-02

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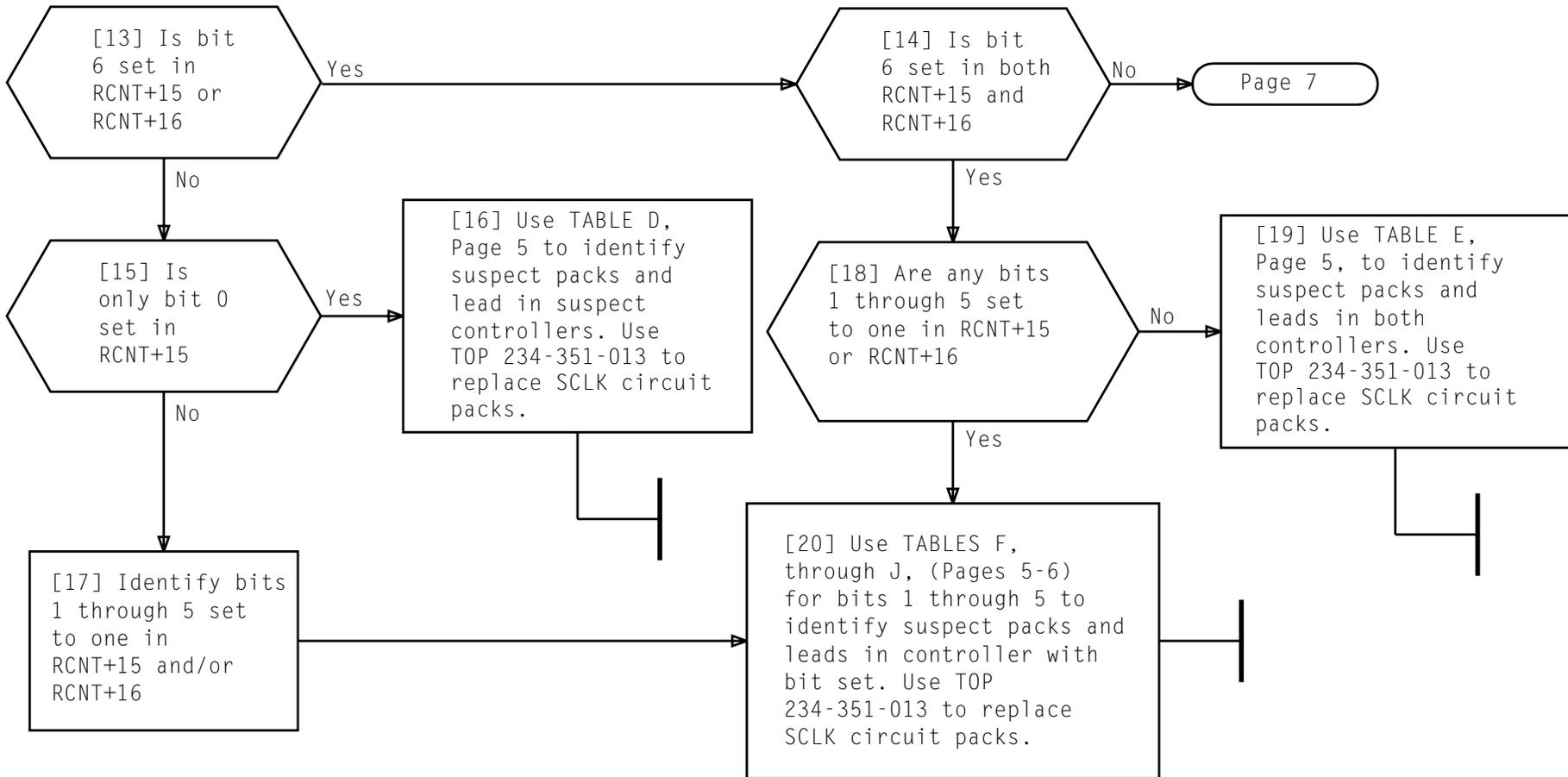


TABLE D BIT 0 (ONLY)				
SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION*	LEAD	FS	SYM
FA529	56-39	ESASW	5	2
FA529	56-40	ERRSUM	5	7
FA1807	56-41	ESRG	9	2

* Suspect pack bay location - SCLK controller number

TABLE E BIT 6 (BOTH CONTROLLERS)				
SUSPECT PACK*		SD-4A037-02		
TYPE	LOCATION†	LEAD	FS	SYM
FA531	56-34	RPBMAT1	4	4,5
	56-33	RPBMA01	4	1,2,3
FA528	56-23	MORB0,1,2	1	2
	56-20	MORB3,4,5	1	5
	56-24	MORB6,7,8	1	8
	56-25	MORB9,10,11	1	11
	56-22	MORB12,13,14	1	14
	56-21	MORB15,16,17	1	17
	56-31	MORB18,19,20	1	20
56-32	MORB21,22,23	1	23	
FA1807	56-41	STRMF	9	2
FB232	56-06	16CLAP	12	1

* Suspect pack list applies to both SCLK controllers
† Suspect pack bay location - SCLK controller number

TABLE F BIT 1					
UNIT	SUSPECT PACK LOCATION	LEAD ‡	FS ‡	SYM ‡	COMMENT
SCLK	+56-39	CNTRMM	5	2	FA529
	+56-13	MATO	11	1	FA640
	+56-41	ESRG	9	2	FA1807
	+56-07	MATCH	13	5-7	FA531
	+56-08	MATCH (0,1)	13	1-4	FA636
	+56-10	STOA-ST6A	14	1,2	FA636
	+56-12	STOB-ST6B	14	3,4	FA637
	+56-11	ST7A-ST28A	15	1	FA637
	+56-09	ST7B-ST28B	15	2	FA637
	+56-06	8KCAP, 8KCBP, WINAP	12	1	FB232
NCLK	078-21*	OCLK00	1	1	If SCLK CONTR 0 suspect
	078-22*	OCLK01	1	1	If SCLK CONTR 1 suspect
	178-21*	1CLK00	1	2	If SCLK CONTR 1 suspect
	178-22*	1CLK01	1	2	If SCLK CONTR 0 suspect
	Cables carrying 16 mHz signal from NCLK (FB211) to SCLK (FB232) are also suspect				

* These FB211 packs require special replacement procedures. See [234-151-013]
† SCLK suspect pack bay location - SCLK controller number
‡ SCLK - SD-4A037-02;NCLK - SD-4A014-02

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TABLE G BIT 2									
SUSPECT PACK		SD-4A037-02			SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION *	LEAD	FS	SYM	TYPE	LOCATION *	LEAD	FS	SYM
FA529	56-39	ESPFE	5	2	FA528	56-23	WRPEV0	1	1
FA534	56-27	PEVCHK	2	1,3		56-20	WRPEV1	1	4
FA551	56-38	STRPTF	7	1		56-24	WRPEV2	1	7
FA1807	56-41	STERRA0	9	2		56-25	WRPEV3	1	10
FA641	56-42	TANIO	9	1		56-22	WRPEV4	1	13
						56-21	PRTEV	1	16
						56-31	WRPEV6	1	19
						56-32	EA00	1	22

* Suspect pack bay location – SCLK controller number

TABLE I BIT 4				
SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION *	LEAD	FS	SYM
FA529	56-40	ESIVOP	5	7
FA639	56-43	IVOPC	10	1
FA528	56-23	WB29	1	1
	56-24	WB31	1	7
		WB33		
		WB35		
	56-25	WB30 WB32 WB34	1	10
56-32	EA00	1	22	
	56-31	EA01	1	19
FA551	56-38	STIVOP	7	1
FA1807	56-41	STERRA0	9	2
FA641	56-42	TANIO	9	1

* Suspect pack bay location – SCLK controller number

TABLE J BIT 5				
SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION *	LEAD	FS	SYM
FA529	56-40	ESMODF	5	7
FA639	56-43	MODF	10	1
FA528	56-24	WB35	1	7
	56-32	MBIT	1	22
FA529	56-39	SRMAS	5	2
FA551	56-38	STIVOP	7	1
FA1807	56-41	STERRA0	9	2
FA641	56-42	TANIO	9	1

* Suspect pack bay location – SCLK controller number

TABLE H BIT 3				
SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION *	LEAD	FS	SYM
FA529	56-39	ESPFO	5	2
FA534	56-27	PODCHK	2	2,4
FA551	56-38	STRPTF	7	1
FA1807	56-41	STERRA0	9	2
FA641	56-42	TANIO	9	1
FA528	56-23	WRPOD0	1	1
	56-20	WRPOD1	1	4
	56-24	WRPOD2	1	7
	56-25	WRPOD3	1	10
	56-22	PRT0D	1	13
	56-21	WRPOD5	1	16
	56-31	EA01	1	19
	56-32	WRPOD7	1	22

* Suspect pack bay location – SCLK controller number

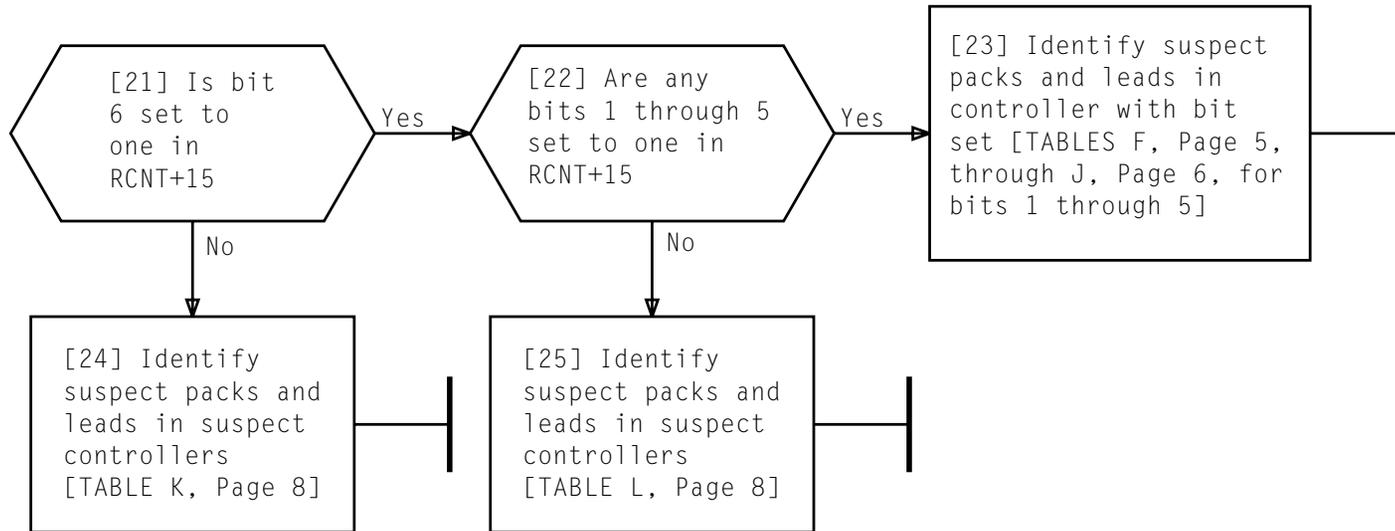
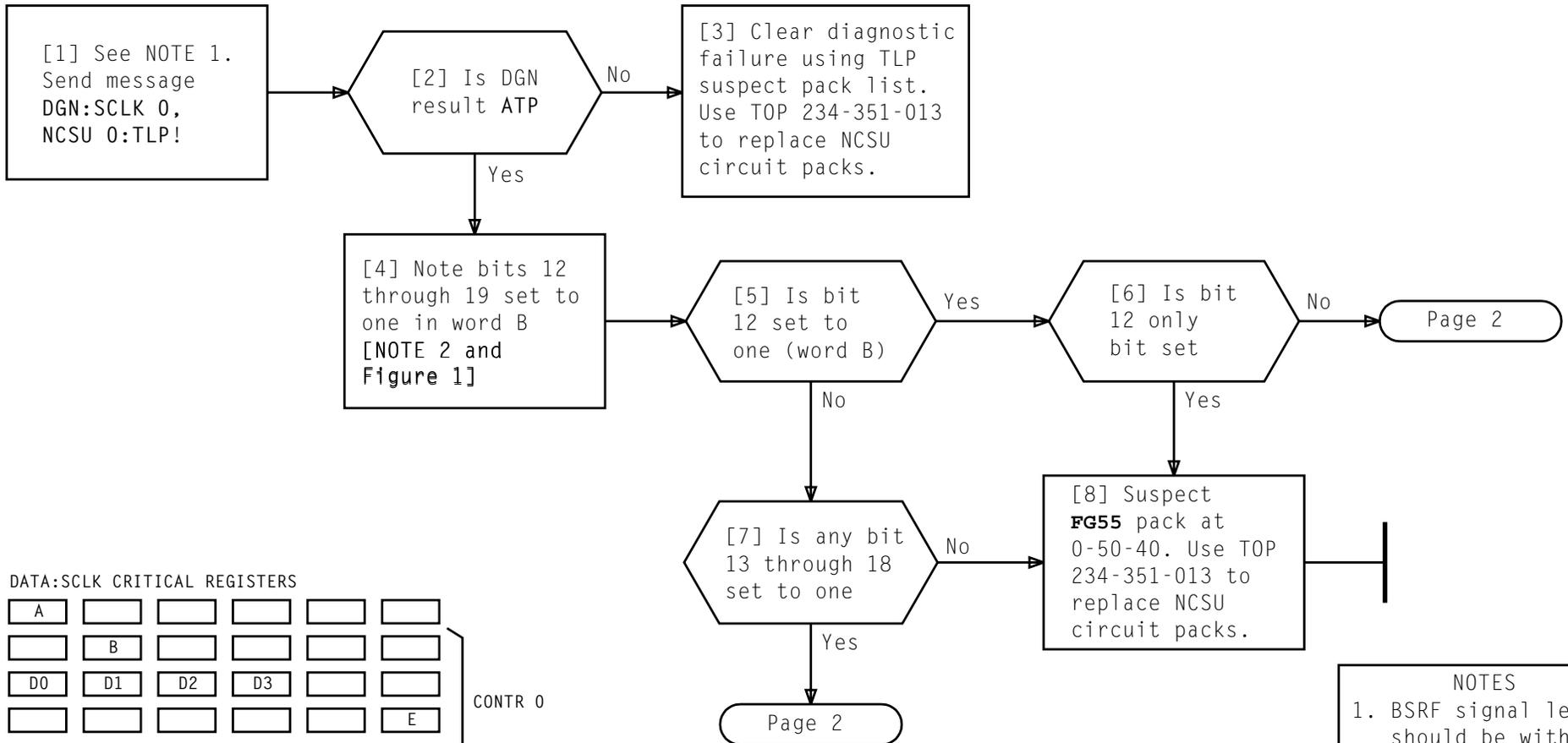


TABLE K RCNT+16 REGISTER BIT 6 SET						
UNIT	SUSPECT PACK		LEAD*	FS†	SYM†	
	TYPE	LOCATION*				
SCLK	FA1807	56-41	RPASW0	9	2	
	FA641	56-42	CLOUT	9	1	
	FB232	56-06	16CLAP	12	1	
	FA639	56-43	ACOPC	10	1	
	FA531	56-26	KMATCH1	3	2	
	FA528		56-22	EA3, EA5	1	13
			56-21	EA2, EA4, EA6	1	16
			56-31	EA7, EA9, EA11	1	19
			56-32	EA8, EA10	1	22
	SCLK IPUB	FC12	060-34	OSYCO	2	7
160-34			ISYCO	3	7	

*SCLK suspect pack bay location – SCLK controller number
†SCLK – SD-4A037-02, NCLK – SD-4A014-02

TABLE L RCNT+15 REGISTER BIT 6 SET				
SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION*	LEAD	FS	SYM
FA529	56-40	ESRMF	5	7
FA531	56-34	RPBMAT1	4	4,5
	56-33	RPBMA01	4	1,2,3
FA1807	56-41	STRMF	9	2
FB232	56-06	16CLAP	12	1

*Suspect pack bay location – SCLK controller number



DATA:SCLK CRITICAL REGISTERS

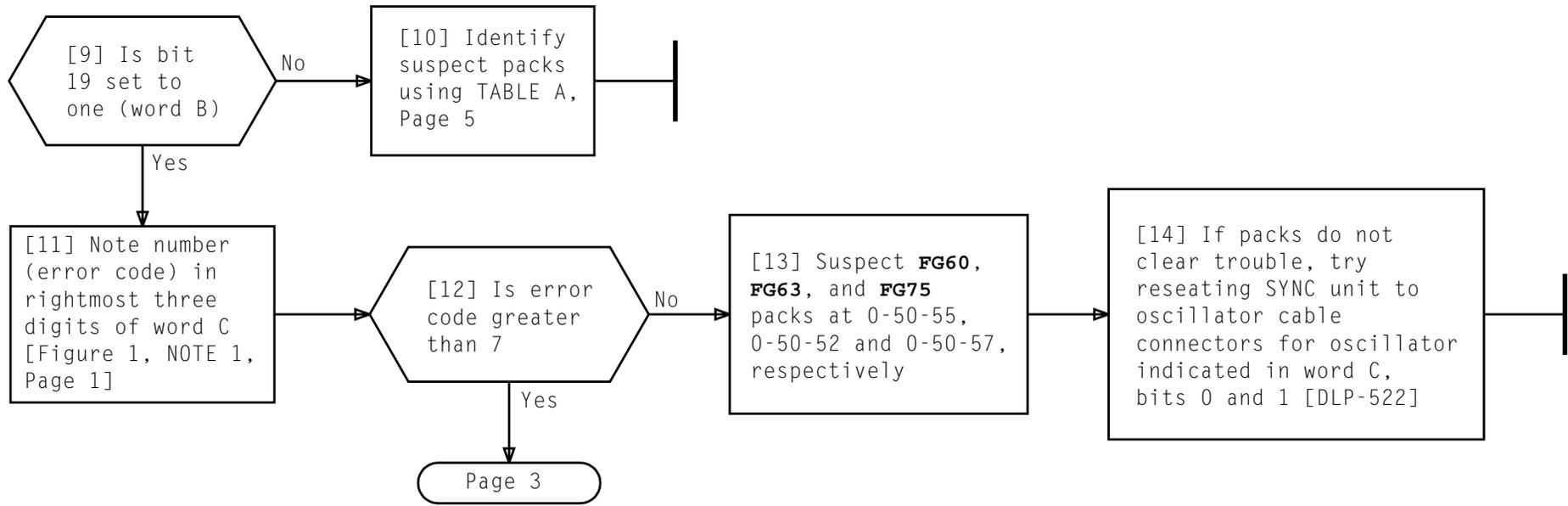
A						CONTR 0
	B					
D0	D1	D2	D3			
					E	
	C					
A						CONTR 1
	B					
D0	D1	D2	D3			
					E	
	C					

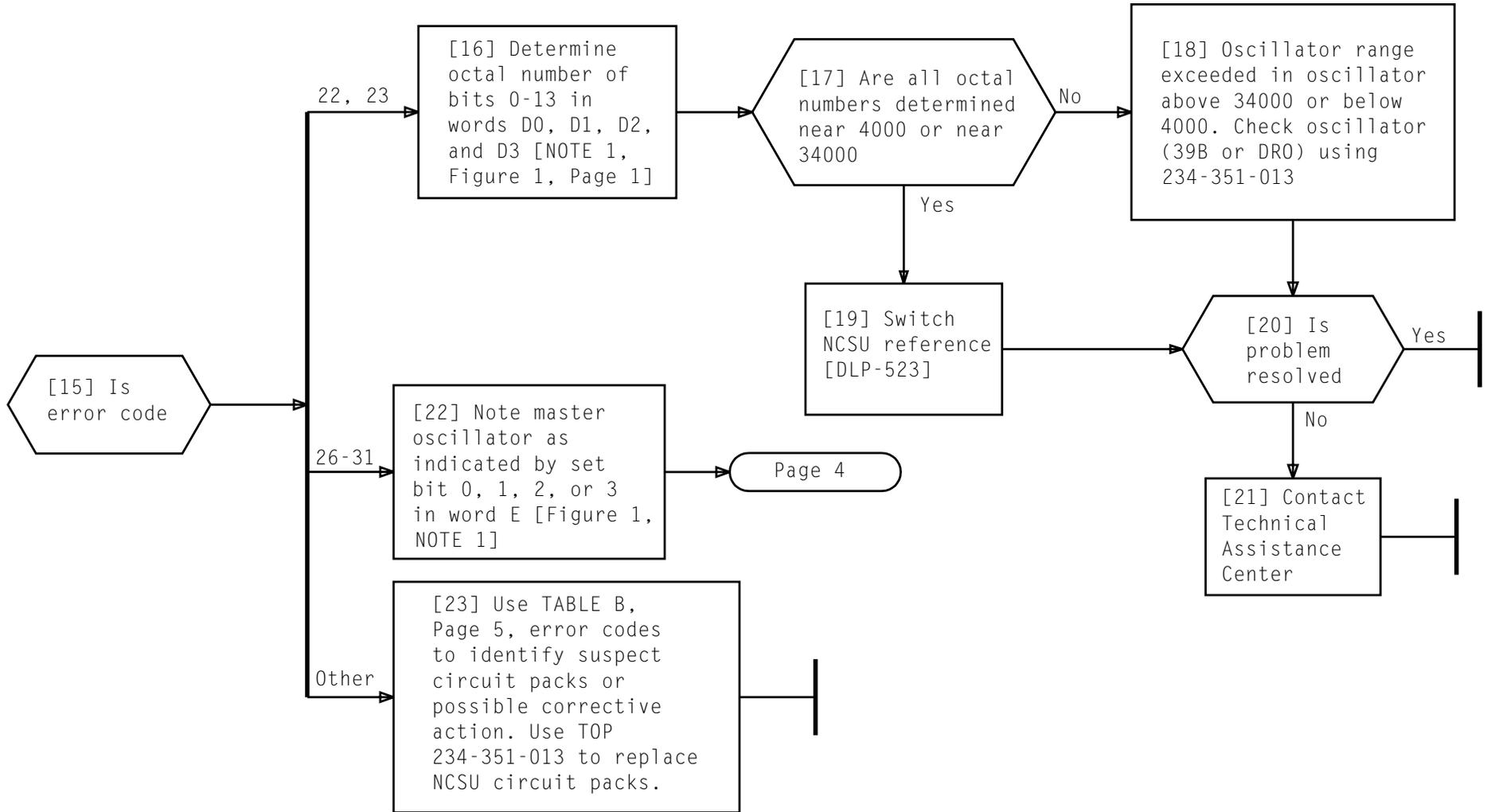
Figure 1 - SCLK Critical Registers

NOTES

- BSRF signal level should be within specifications if used by NCSU
- If bit 12 of word A equals 0, CONTR 0 words in Figure 1 should be used. If it equals 1, CONTR 1 words should be used

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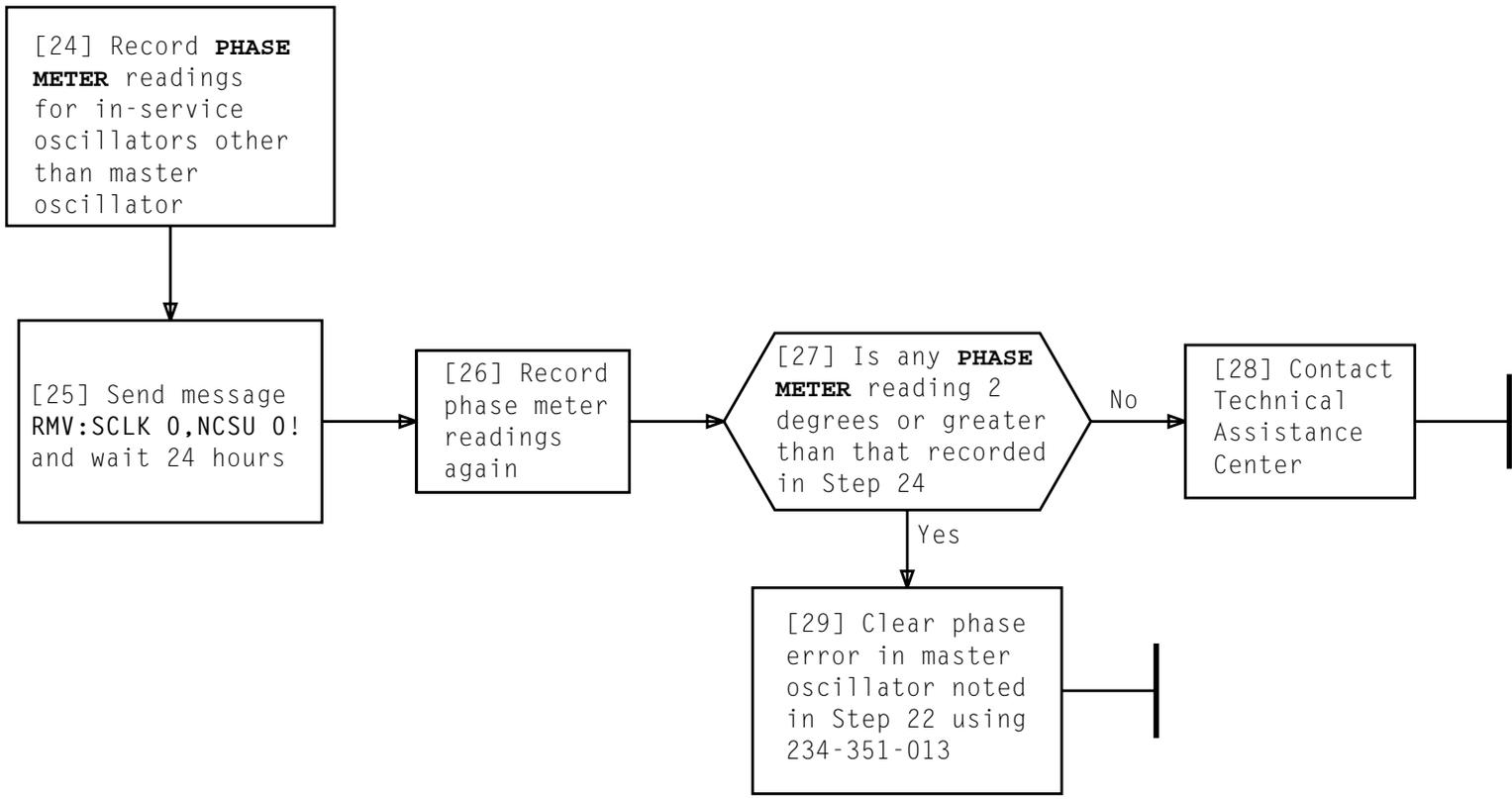
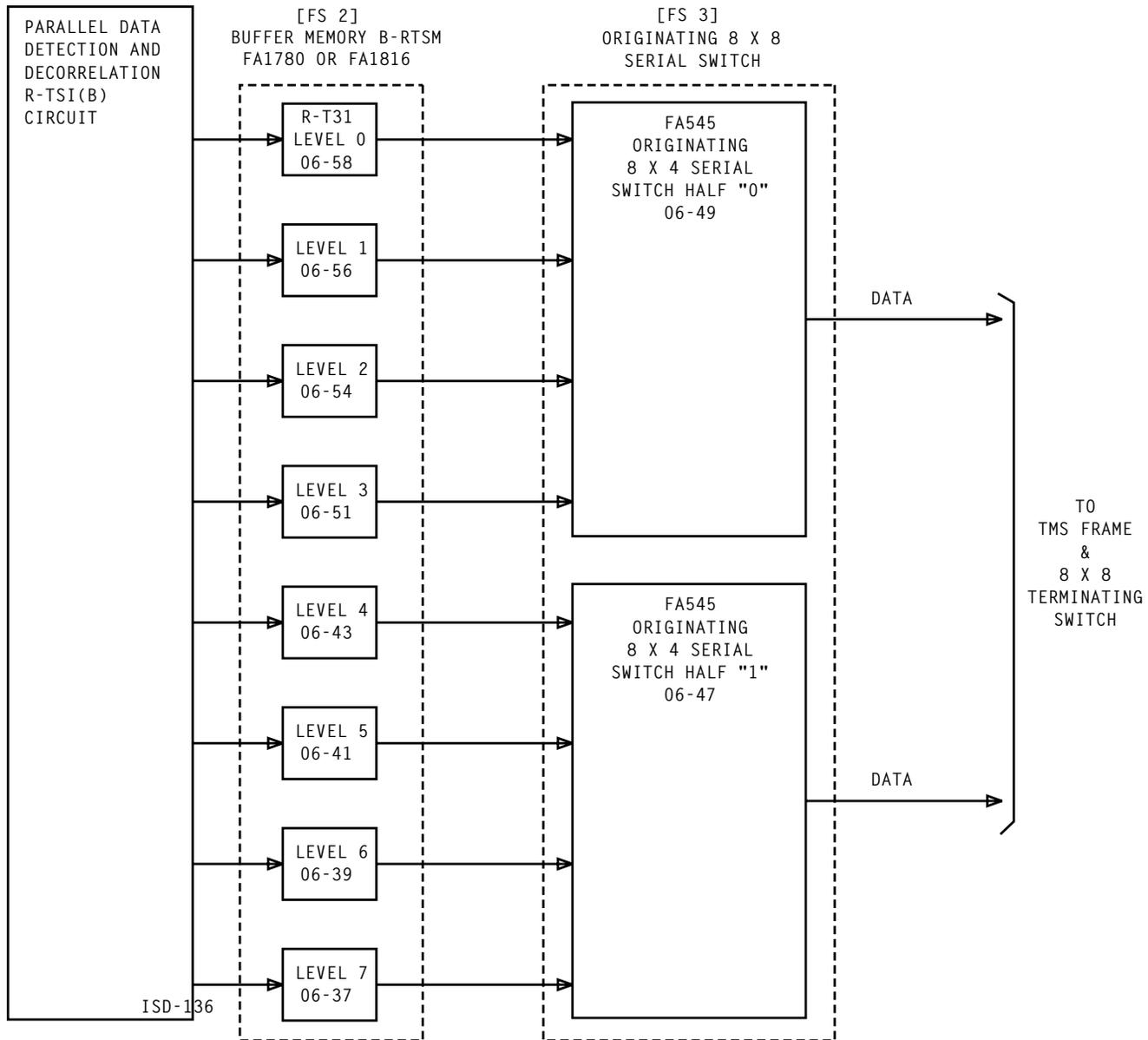


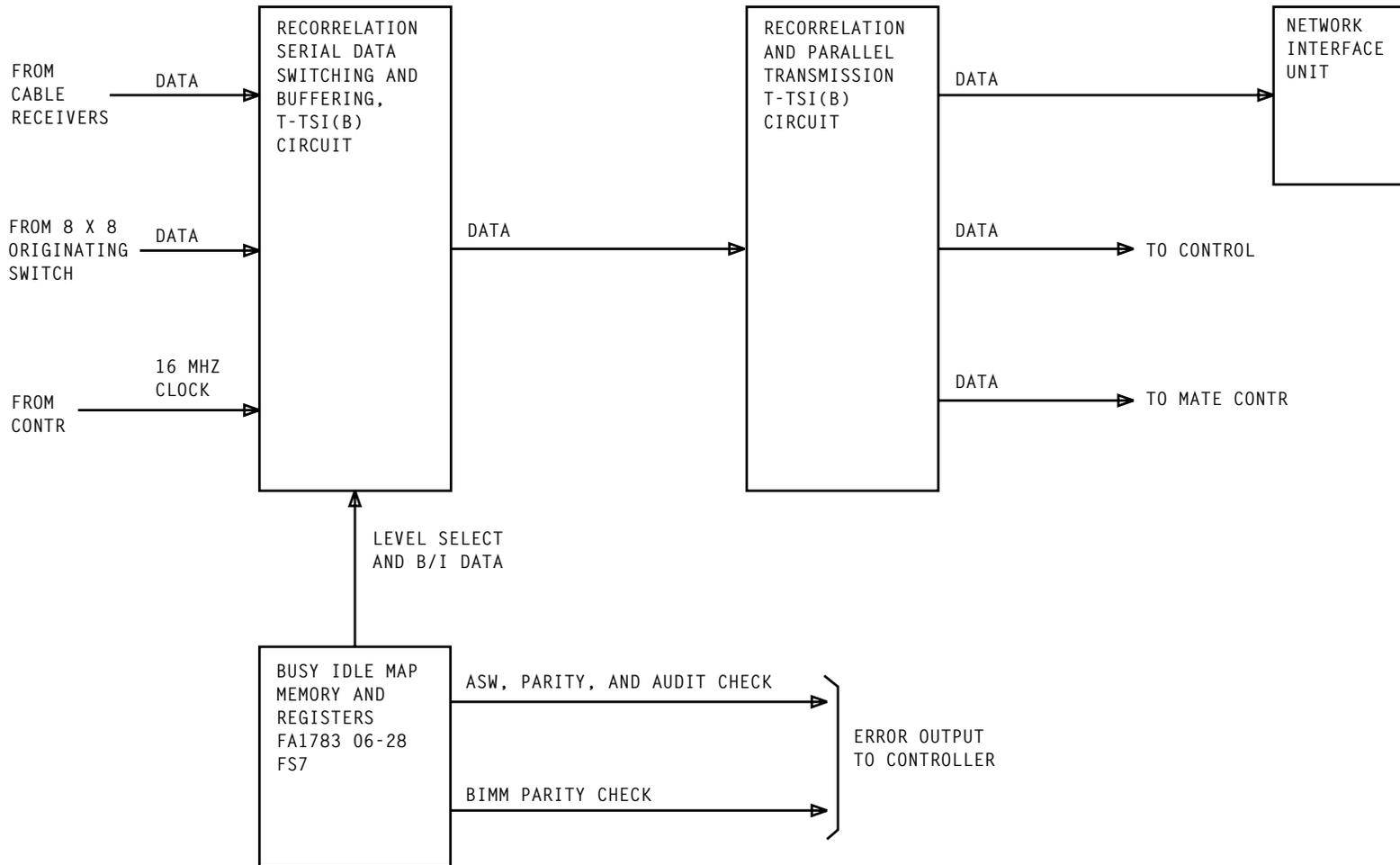
TABLE A ALL SEEMS WELL ERROR SOURCE REGISTER (ASWESR)				
BIT	BIT DESCRIPTION	PACK	LOCATION	COMMENTS
13	Clock parity error	FG56	0-50-36	SD-4A105, FS2, SYM 1, leads B1-B40
14	Clock error	FG55 FG63 FG56	0-50-40 0-50-52 0-50-36	
15	Microprocessor match failure	FG57 FG63 FG58	0-50-42 0-50-52 0-50-44	FG92 for DRO OSC.
16	Microprocessor sanity	FG63 FG62	0-50-52 0-50-59	
17	Invalid OPCODE	FG56 FG53 FA1806	0-50-36 *-56-43	System clock
18	Microprocessor trap	FG63 FG58 FG59	0-50-52 0-50-44 0-50-46	FG92 for DRO OSC.
* If Figure 1, Page 1, word A, bit 1 set, * = 1; if not set, * = 0				

TABLE B ERROR CODES (WORD C)†							
CODE	PACK	LOCATION	COMMENTS	CODE	PACK	LOCATION	COMMENTS
10	FG61	0-50-63		24	Switch NCSU reference [DLP-523]		
	FG62	0-50-59		32	Same as code 21		
	Clear phase error – 234-351-013			33	Same as code 40		
11	Same as code 40			34	FG61	0-50-63	Chain 0 Chain 1 Chain 2 Chain 3
13	FG63	0-50-52			FA628	0-70-29	
	FG64	0-50-65			FA628	0-70-42	
	FG59	0-50-46			FA628	1-70-29	
Clear phase error – 234-351-013			35	FA628	1-70-42		
14	Same as code 10			36	Same as code 10 (for 39B OSC.)		
15	Same as code 40				Check for major alarm on a DRO OSC.		
17	FG64	0-50-65		37	FG64	0-50-65	SCLK
	FG63	0-50-52			FB232	*-56-96	
	FG59	0-50-46			FG61	0-50-63	
21	Switch NCSU reference [DLP-523]			40	Contact Technical Assistance Center		
	FG65	0-50-67		42	Check for DRO OSC. power failure		
	FG64	0-50-65					
* If Figure 1, Page 1, word A, bit 1 set, * = 1; if not set, * = 0							
† Partial list – other error codes within this TAP							



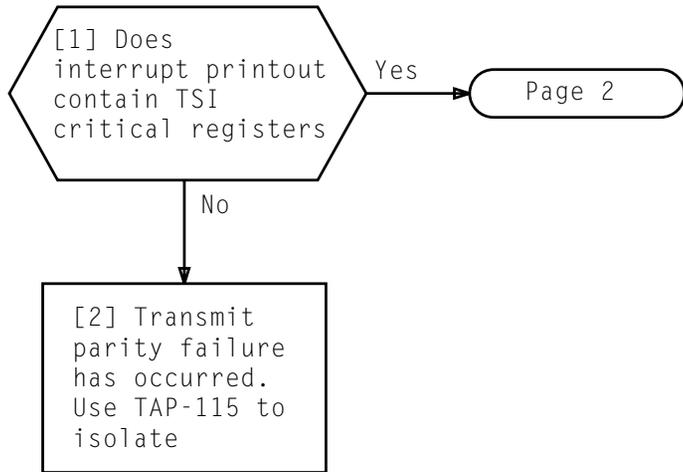
BUFFER MEMORY B AND ORIGINATING R-TSI(B) CIRCUIT

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TRANSMIT TSI, TSI-B SWITCHING AND PERMUTING CIRCUIT

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[3] Obtain point of maximized definition (PMD) from **FAULT RECOGNITION ISOLATION DATA** word 2 [Figure 1]

[4] Access PMD dictionary to obtain description of software actions and analysis of error [DLP-510]

[5] Determine frames mode of operation, DIVORCED (SIMPLEX) or NOT DIVORCED (DUPLEX), and type of error (PUF, APUF, TRPF) [DLP-513]

Mode of operation and error type identified

AND

[6] Is type of error PUF or APUF [DLP-513]

PUF

[7] Clear PUF problem [TAP-111]

APUF

[8] Is error a TRPF [DLP-513]

Yes

[9] Clear TRPF problem [TAP-115]

No

[10] Was frame SIMPLEX (DIVORCED) or DUPLEXED at time of interrupt [DLP-513]

SIMPLEXED

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DUPLEX

Page 3

PMD NUMBER

```
A 39 REPT: F-LEVEL 014764301 MFNUM=00004303 MICON=00000020 MSG COMPL
LV=0040 D0=00000000 D1=04000000 D2=00000017 D3=00000000
DATA: PERIPHERAL SYSTEM DATA
03020102 00000000 00000001 00000000 00000000 00000104
00000112 00000004 00000012 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00002400 14130667 03552000 00000020 00002000
DATA: FAULT RECOGNITION ISOLATION DATA
00000020 00002000 0000237 00000000 00000003 00000000
DATA: ERROR ANALYSIS STRATEGY DATA
01664210 00000001 00000001 00000001 00000001 00000000
00000001
```

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Figure 1 - Part of TNFR Printout

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[15] Use TABLE B to obtain suspect pack list for set bits 0, 1, 3, or 15, use [TAD-114] for general strategy, and use Figure 3, and Example 1 for frame type

TABLE B CLOCK BITS			
FRAME TYPE	SET BIT	PACK TYPE	LOCATION
TSI-A1 [SD-4A023-01]	0,1,3	FA562	56-36
		FB225	56-35
		FB224	56-37
		FA552	56-30
		FA553	56-33
	FA554	56-34	
	15	FB220	56-39
		FB225	56-35
TSI-A2 [SD-4A023-02]	0,1,3	FA562	56-36
		FC463	56-35
		FA552	56-30
		FA553	56-33
		FA554	56-34
TSI-B [SD-4A083-01]	0,1,3	FA1798	72-29
		FA1233	72-31
		FA1234	72-30
		FC464	72-27

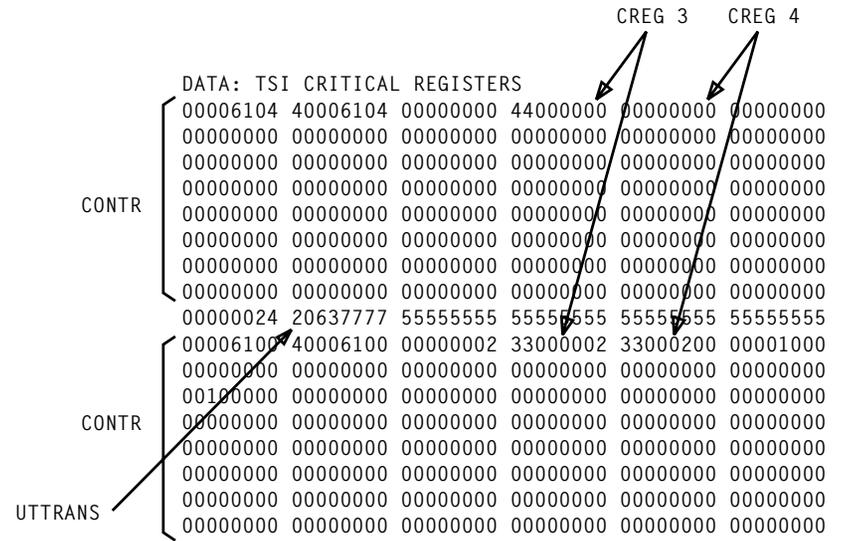
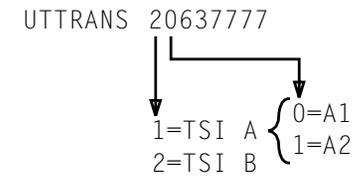


Figure 3 - TSI CREGs



EXAMPLE 1

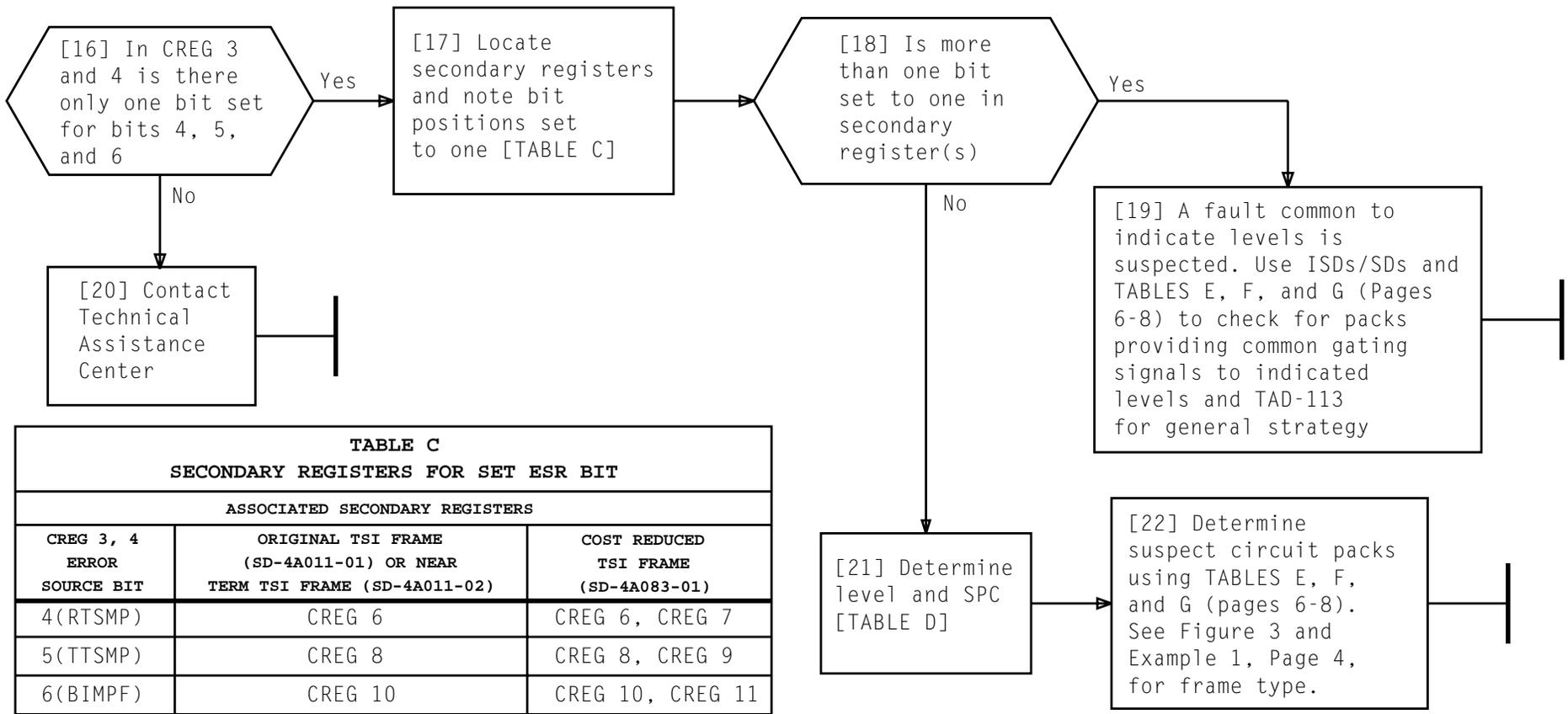


TABLE C
SECONDARY REGISTERS FOR SET ESR BIT

ASSOCIATED SECONDARY REGISTERS		
CREG 3, 4 ERROR SOURCE BIT	ORIGINAL TSI FRAME (SD-4A011-01) OR NEAR TERM TSI FRAME (SD-4A011-02)	COST REDUCED TSI FRAME (SD-4A083-01)
4(RTSMP)	CREG 6	CREG 6, CREG 7
5(TTSMP)	CREG 8	CREG 8, CREG 9
6(BIMPF)	CREG 10	CREG 10, CREG 11

TABLE D
SPC AND LEVEL

CREG	SPC								SPC							
6,8,10	1								0							
7,9,11	3								2							
BIT	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LEVEL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

TABLE E – SUSPECT PACK LIST FOR ESR BIT 4										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA632(B)	42-29	42-28	42-27	42-26	42-24	42-23	42-22	42-21
		FA543	46-26	46-25	46-24	46-23	46-22	46-21	46-20	46-19
	TSI-A2 SD4A011-02	FA632B	42-29	42-28	42-27	42-26	42-24	42-23	42-22	42-21
		FA543	46-26	46-25	46-24	46-23	46-22	46-21	46-20	46-19
TSI-B SD4A083-01	FA1780*	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37	
1	TSI-A1 SD4A011-01	FA632(B)	64-29	64-28	64-27	64-26	64-24	64-23	64-22	64-21
		FA543	68-26	68-25	68-24	68-23	68-22	68-21	68-20	68-19
	TSI-A2 SD4A011-02	FA632B	64-29	64-28	64-27	64-26	64-24	64-23	64-22	64-21
		FA543	68-26	68-25	68-24	68-23	68-22	68-21	68-20	68-19
TSI-B SD4A083-01	FA1780*	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37	
2	TSI-B SD4A083-01	FA1780*	52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
3	TSI-B SD4A083-01	FA1780*	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37
* FA1780 or FA1816 (wide band option on SPC – all levels)										

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TABLE F – SUSPECT PACK LIST FOR ESR BIT 5										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA632(B)	42-44	42-43	42-42	42-41	42-39	42-38	42-37	42-36
		FA541	46-44	46-43	46-42	46-41	46-40	46-39	46-38	46-37
	TSI-A2 SD4A011-02	FA632B	42-44	42-43	42-42	42-41	42-39	42-38	42-37	42-36
		FA541	46-44	46-43	46-42	46-41	46-40	46-39	46-38	46-37
	TSI-B SD4A083-01	FA1781*	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
	1	TSI-A1 SD4A011-01	FA632(B)	64-44	64-43	64-42	64-41	64-39	64-38	64-37
FA541			68-44	68-43	68-42	68-41	68-40	68-39	68-38	68-37
TSI-A2 SD4A011-02		FA632B	64-44	64-43	64-42	64-41	64-39	64-38	64-37	64-36
		FA541	68-44	68-43	68-42	68-41	68-40	68-39	68-38	68-37
TSI-B SD4A083-01		FA1781*	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
2		TSI-B SD4A083-01	FA1781*	52-24	52-23	52-19	52-17	52-10	52-09	52-05
3	TSI-B SD4A083-01	FA1781*	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
* FA1780 or FA1816 (wide band option on SPC – all levels)										

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ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE (TSI)

TABLE G – SUSPECT PACK LIST FOR ESR BIT 6										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6*	7*
0 or 1	TSI-A1 SD4A011-01	FA633(B)	N/A	N/A	N/A	N/A	N/A	N/A	42-53	64-53
		FA556							42-52	64-52
		FA555							56-38	56-38
	TSI-A2 SD4A011-02	FA633B	N/A	N/A	N/A	N/A	N/A	N/A	42-53	64-53
		FA556							42-52	64-52
		FA555							56-38	56-38
0	TSI-B SD4A083-01	FA1783	28-28	28-28	28-28	28-28	28-28	28-28	28-28	28-28
1	TSI-B SD4A083-01	FA1783	40-28	40-28	40-28	40-28	40-28	40-28	40-28	40-28
2	TSI-B SD4A083-01	FA1783	52-28	52-28	52-28	52-28	52-28	52-28	52-28	52-28
3	TSI-B SD4A083-01	FA1783	64-28	64-28	64-28	64-28	64-28	64-28	64-28	64-28
* For TSI-A1 and TSI-A2 this column is bit 6 and 7 not level 6 and 7										

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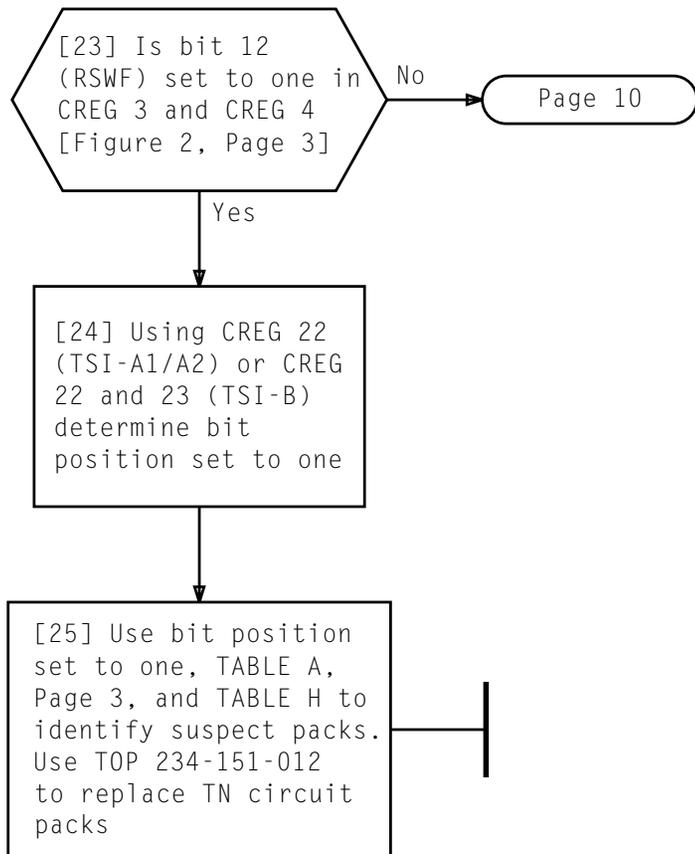
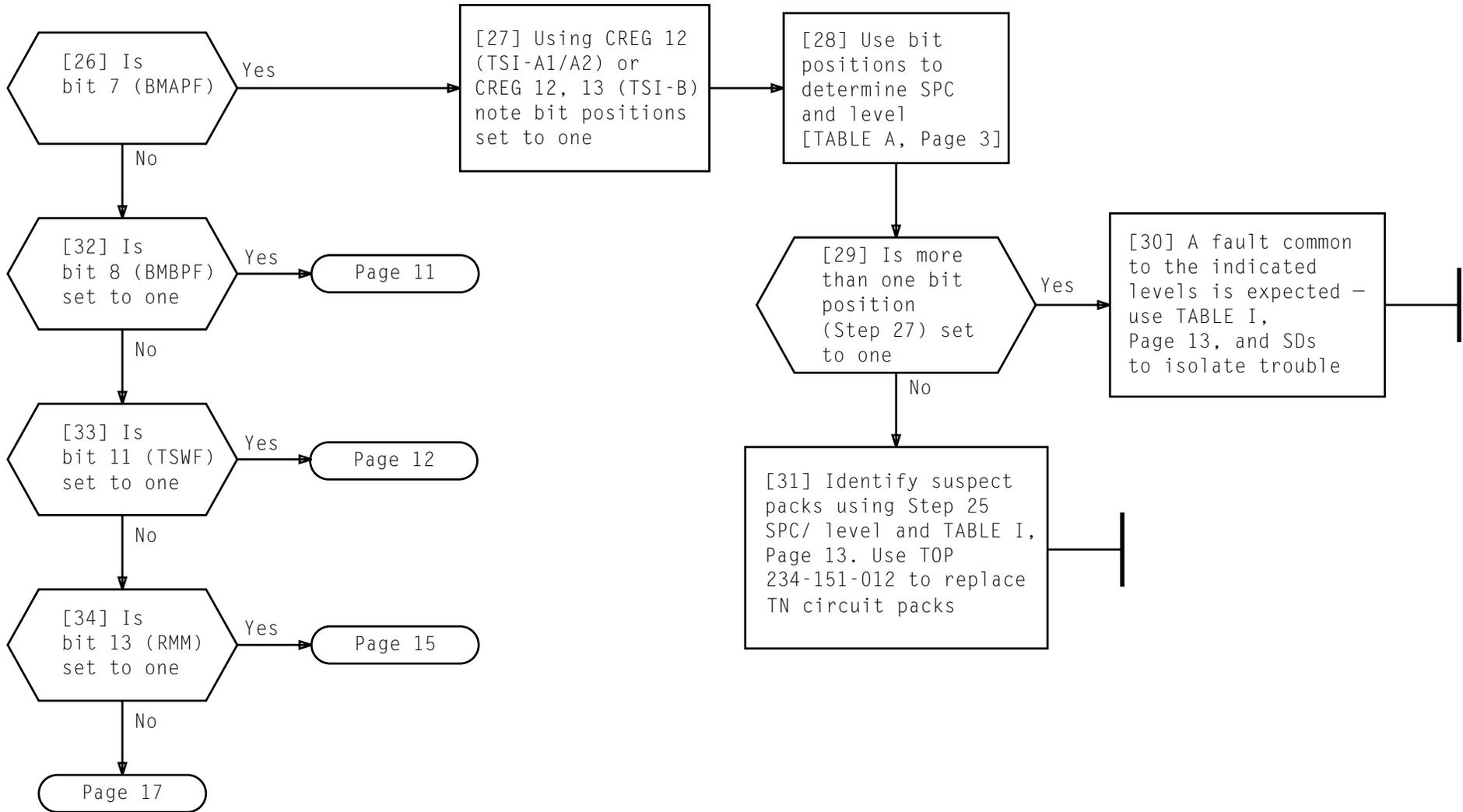


TABLE H SUSPECT PACKS FOR CREG 3/4 BIT 12								
TSI (SD-4A011-01, 02)				TSI (SD-4A083-01)				
LEVEL	CIRCUIT PACK TYPE	SPC 0	SPC 1	CIRCUIT PACK TYPE	SPC 0	SPC 1	SPC 2	SPC 3
0	FB221(B)	38-23	60-23	FB221B	*24-69	*36-69	*48-69	*60-69
	FA567	38-19	60-19	FA1791	*24-68	*36-68	*48-68	*60-68
	FA569	38-11	60-11	FA1782	*24-66	*36-66	*48-66	*60-66
1	FB221(B)	38-23	60-23	FB221B	*24-69	*36-69	*48-69	*60-69
	FA567	38-18	60-18	FA1791	*24-65	*36-68	*48-68	*60-68
	FA569	38-10	60-10	FA1782	*24-63	*36-63	*48-63	*60-63
2	FB221(B)	38-22	60-22	FB221B	*24-61	*36-61	*48-61	*60-61
	FA567	38-17	60-17	FA1791	*24-60	*36-60	*48-60	*60-60
	FA569	38-09	60-09	FA1782	*24-58	*36-58	*48-58	*60-58
3	FB221(B)	38-22	60-22	FB221B	*24-61	*36-61	*48-61	*60-61
	FA567	38-15	60-15	FA1791	*24-56	*36-56	*48-56	*60-56
	FA569	38-08	60-08	FA1782	*24-54	*36-54	*48-54	*60-54
4	FB221(B)	38-21	60-21	FB221B	*24-52	*36-52	*48-52	*60-52
	FA567	38-14	60-14	FA1791	*24-51	*36-51	*48-51	*60-51
	FA569	38-07	60-07	FA1782	*24-49	*36-49	*48-49	*60-49
5	FB221(B)	38-21	60-21	FB221B	*24-52	*36-52	*48-52	*60-52
	FA567	38-13	60-13	FA1791	*24-47	*36-47	*48-47	*60-47
	FA569	38-06	60-06	FA1782	*24-45	*36-45	*48-45	*60-45
6	FB221(B)	38-20	60-20	FB221B	*24-43	*36-43	*48-43	*60-43
	FA567	38-12	60-12	FA1791	*24-41	*36-41	*48-41	*60-41
	FA569	38-05	60-05	FA1782	*24-39	*36-39	*48-39	*60-39
7				FB221B	*24-43	*36-43	*48-43	*60-43
				FA1791	*24-38	*36-38	*48-38	*60-38
				FA1782	*24-37	*36-37	*48-37	*60-37

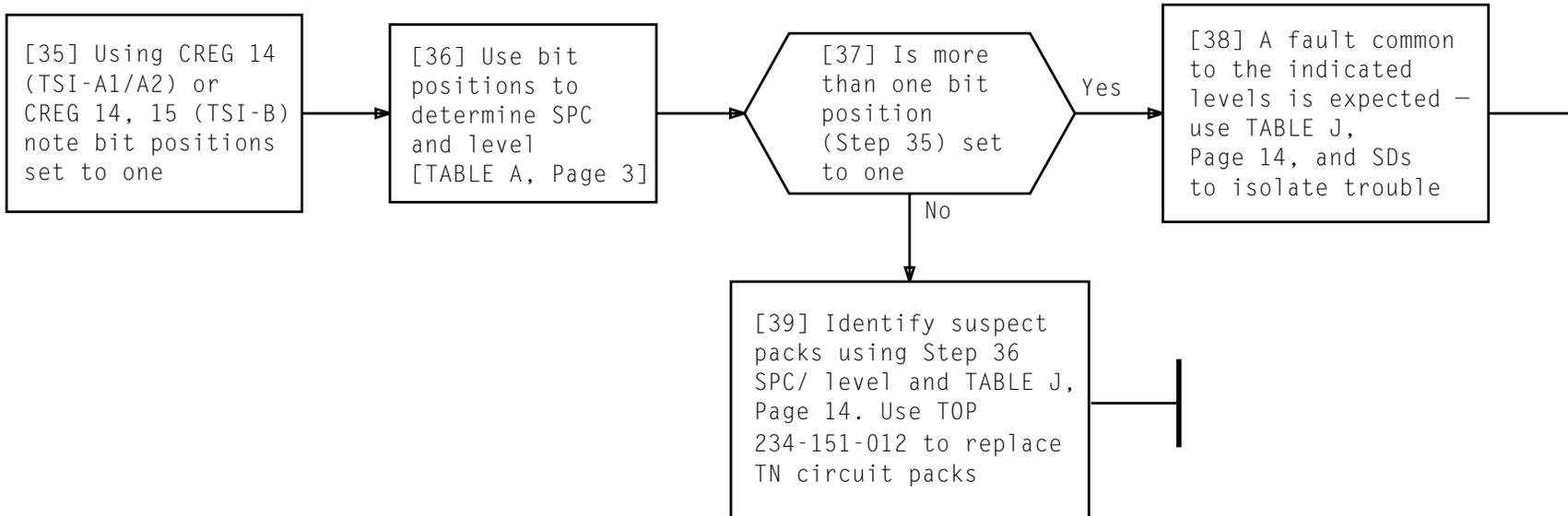
* Bay 0 or 1 same as suspect controller

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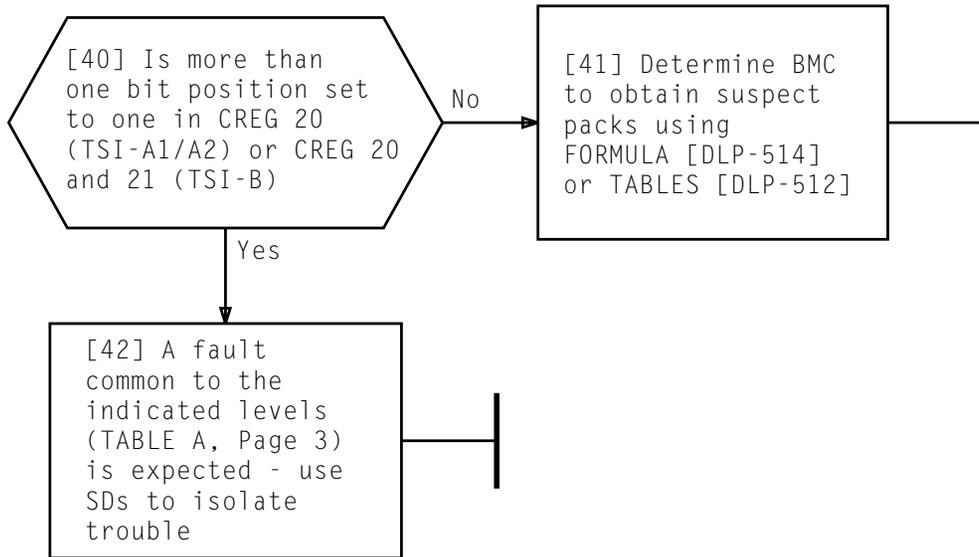


TABLE I - SUSPECT PACK LIST FOR ESR BIT 7										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA633(B)	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04
		FA542	(46-09, 46-08, 46-07)				(46-06, 46-05, 46-04)			
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	N/A
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	N/A
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04
		FA542	(46-09, 46-08, 46-07)				(46-06, 46-05, 46-04)			
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	N/A
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	N/A
		FA540	42-15, 42-14 (Address Select)				42-13, 42-12 (Address Select)			
	TSI-B SD4A083-01	FA1791	24-68	24-65	24-60	24-56	24-51	24-47	24-41	N/A
FA1782		24-66	24-63	24-58	24-54	24-49	24-45	24-39	N/A	
1	TSI-A1 SD4A011-01	FA633(B)	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
		FA542	(68-09, 68-08, 68-07)				(68-06, 68-05, 68-04)			
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	N/A
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	N/A
		FA540	64-15, 64-14 (Address Select)				64-13, 64-12 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
		FA542	(68-09, 68-08, 68-07)				(68-06, 68-05, 68-04)			
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	N/A
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	N/A
		FA540	64-15, 64-14 (Address Select)				64-13, 64-12 (Address Select)			
	TSI-B SD4A083-01	FA1791	36-68	36-65	36-60	36-56	36-51	36-47	36-41	36-38
FA1782		36-66	36-63	36-58	36-54	36-49	36-45	36-39	36-37	
2	TSI-B SD4A083-01	FA1791	48-68	48-65	48-60	48-56	48-51	48-47	48-41	48-38
		FA1782	48-66	48-63	48-58	48-54	48-49	48-45	48-39	48-37
3	TSI-B SD4A083-01	FA1791	60-68	60-65	60-60	60-56	60-51	60-47	60-41	60-38
		FA1782	60-66	60-63	60-58	60-54	60-49	60-45	60-39	60-37

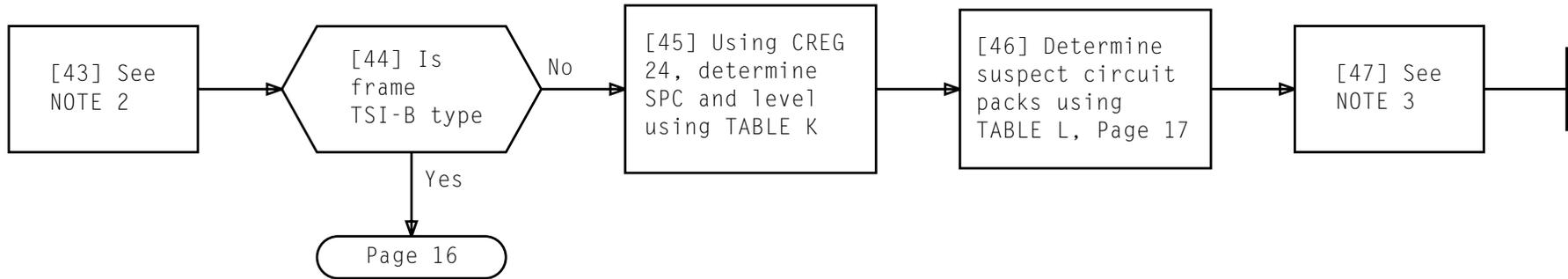
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ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE (TSI)

TABLE J – SUSPECT PACK LIST FOR ESR BIT 8										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA633(B)	50-18	50-17	50-15	50-14	50-13	50-12	50-11	50-10
		FA544	50-26	50-25	50-24	50-23	50-22	50-21	50-20	50-19
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	50-18	50-17	50-15	50-14	50-13	50-12	50-11	50-10
		FA1198	50-26		50-24		50-22		50-20	
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-B SD4A083-01	FA1786	28-45	28-45	28-45	28-45	28-45	28-45	28-45	28-45
		FA1780*	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
	1	TSI-A1 SD4A011-01	FA633(B)	72-18	72-17	72-15	72-14	72-13	72-12	72-11
FA544			72-26	72-25	72-24	72-23	72-22	72-21	72-20	72-19
FA540			68-18, 68-17 (Address Select)				68-15, 68-14 (Address Select)			
TSI-A2 SD4A011-02		FA633B	72-18	72-17	72-15	72-14	72-13	72-12	72-11	72-10
		FA1198	72-26		72-24		72-22		72-20	
		FA540	68-18, 68-17 (Address Select)				68-15, 68-14 (Address Select)			
TSI-B SD4A083-01		FA1786	40-45	40-45	40-45	40-45	40-45	40-45	40-45	40-45
		FA1780*	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
2		TSI-B SD4A083-01	FA1786	52-45	52-45	52-45	52-45	52-45	52-45	52-45
	FA1780*		52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
3	TSI-B SD4A083-01	FA1786	64-45	64-45	64-45	64-45	64-45	64-45	64-45	64-45
		FA1780*	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37
* FA1780 or FA1816 (wide band option on SPC - all levels)										

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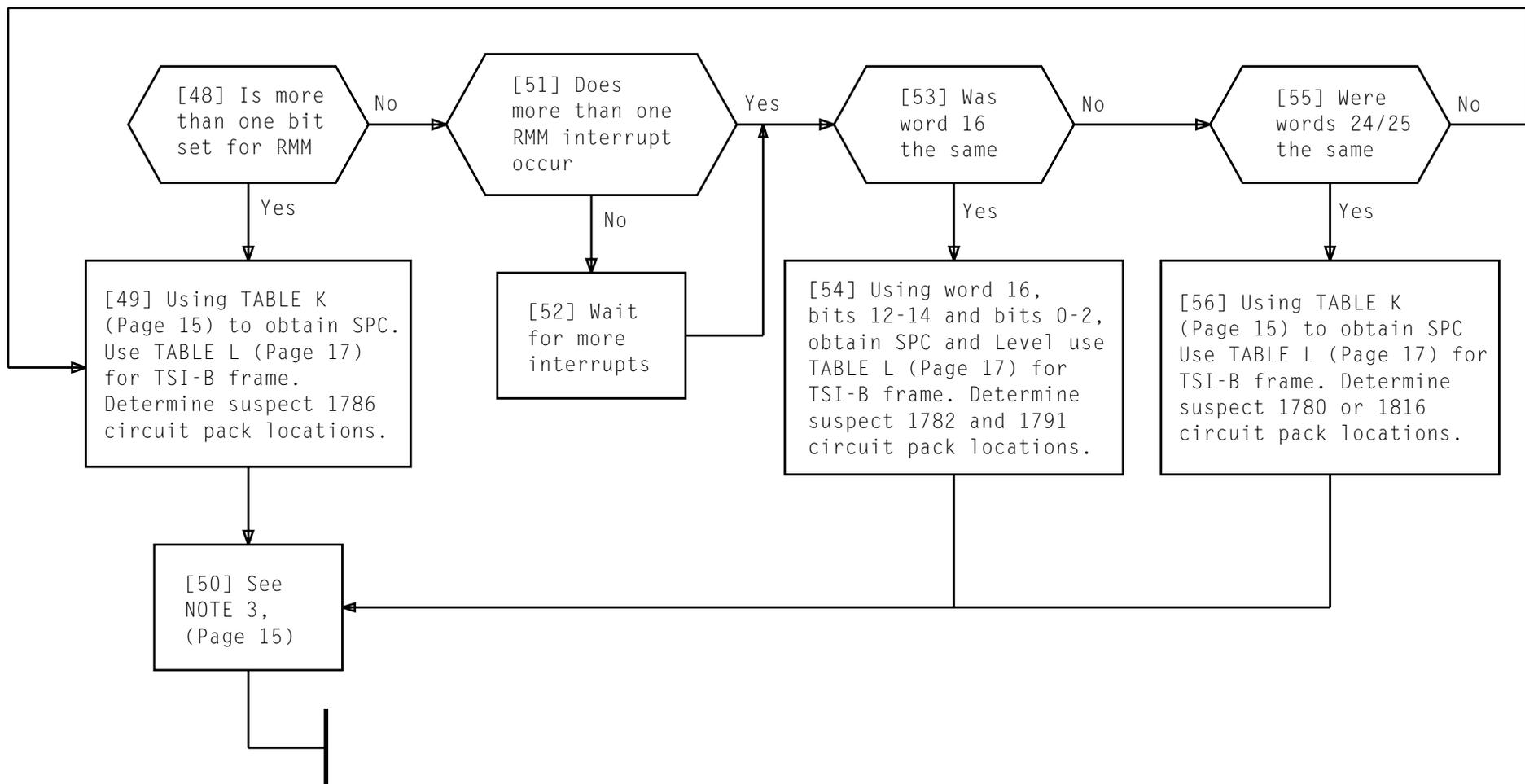
**TABLE K
LEVEL AND SPC**

CREGs		SPC								SPC							
RMM	TMM	1								0							
24	26	3								2							
25	27																
BIT		15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LEVEL		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

NOTE 2

2. If other interrupts occur with unique error (not RMM or TMM) then analyze these interrupts first
3. When a RMM mismatch has occurred, either controller may be suspect. If changing suspect circuit packs in one controller does not fix problem, change suspect circuit packs in other controller

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TABLE L SUSPECT RMM – CIRCUIT PACKS FOR ESR BIT 13										
FRAME TYPE	SPC	CIRCUIT PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 (SD-4A011-01) or TSI-A2 (SD-4A011-02)	0	FA542	46-09	46-07	46-08	46-06	46-04	46-05		
		FA633*	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	
		FA539	–	–	–	–	–	–	–	–
	1	FA542	68-09	68-07	68-08	68-06	68-04	68-05		
		FA633*	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	
		FA539	–	–	–	–	–	–	–	–
* TSI-A2 (SD4A011-02) has FA633B pack, TSI-A1 (SD4A011-01) could have FA633B pack.										

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TABLE L (Contd)										
SUSPECT TMM – CIRCUIT PACKS FOR ESR BIT 13										
FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-B 1786 Circuit Pack	0	FA1786	←————— 28-45 —————→							
	1	FA1786	←————— 28-45 —————→							
	2	FA1786	←————— 28-45 —————→							
	3	FA1786	←————— 28-45 —————→							
TSI-B 1782 and 1791 Circuit Pack	0	FA1782	24-66	24-63	24-60	24-56	24-51	24-47	24-04	—
		FA1791	24-68	24-65	24-58	24-54	24-49	24-45	24-03	—
	1	FA1782	36-66	36-63	36-60	36-56	36-51	36-47	36-04	—
		FA1791	36-68	36-65	36-58	36-54	36-49	36-45	36-03	—
	2	FA1782	48-66	48-63	48-60	48-56	48-51	48-47	48-04	—
		FA1791	48-68	48-65	48-58	48-54	48-49	48-45	48-03	—
3	FA1782	60-66	60-63	60-60	60-56	60-51	60-47	60-04	—	
	FA1791	60-68	60-65	60-58	60-54	60-49	60-45	60-03	—	
TSI-B 1780 or 1816 Circuit Pack	0	FA1780/ FA1816	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
	1	FA1780/ FA1816	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
	2	FA1780/ FA1816	52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
	3	FA1780/ FA1816	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37

[57] See NOTE 4. Using CREG 26/27 and TABLE K, (Page 15) determine SPC and level

[58] Determine suspect packs using TABLE M. Use TOP 234-151-012 to replace TN circuit packs

TABLE M SUSPECT TMM-CIRCUIT PACKS FOR ESR BIT 14											
FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL								
			0	1	2	3	4	5	6	7	
TSI-A1 [SD-4A023-01] or TSI-A2 [SD-4A023-02]	0	FA539	38-56	38-55	38-54	38-53	38-52				
		FA633*	46-57	46-56	46-55	46-54	46-53	46-52	46-51	46-50	
		FA542	42-59	42-59	42-59	42-59	42-56	42-56	42-56	42-56	
		FA542	42-58	42-58	42-58	42-58	42-55	42-55	42-55	42-55	
		FA542	42-57	42-57	42-57	42-57	42-54	42-54	42-54	42-54	
	1	FA539	60-56	60-55	60-54	60-53	60-52				
		FA633*	68-57	68-56	68-55	68-54	68-53	68-52	68-51	68-50	
		FA542	64-59	64-59	64-59	64-59	64-56	64-56	64-56	64-56	
		FA542	64-58	64-58	64-58	64-58	64-55	64-55	64-55	64-55	
		FA542	64-57	64-57	64-57	64-57	64-54	64-54	64-54	64-54	
TSI-B [SD-4A083-01]	0	FA1781	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04	
		FA1787	← 28-29 →								
	1	FA1781	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04	
		FA1787	← 40-29 →								
	2	FA1781	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04	
		FA1787	← 52-29 →								
	3	FA1781	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04	
		FA1787	← 64-29 →								

* TSI-A2 has FA633B pack, TSI-A1 could have FA633B pack.

NOTE 3
Bit 14 is set indicating a TMM mismatch has occurred. Either controller may be suspect. Other interrupts with unique errors should be used to select suspect

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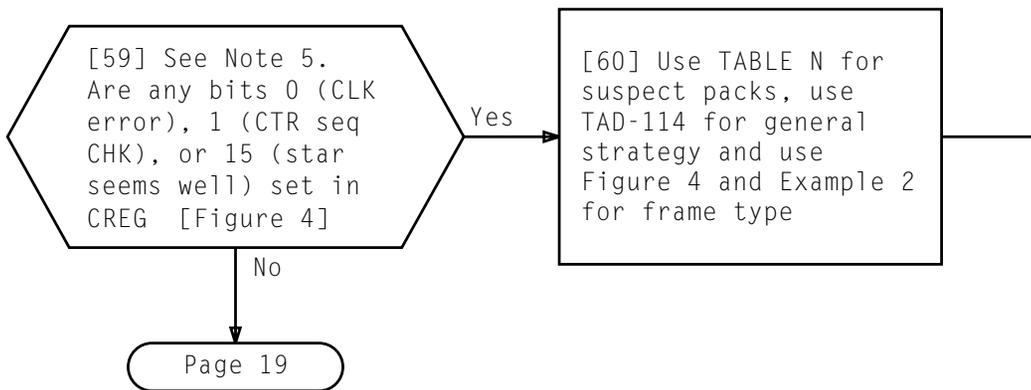
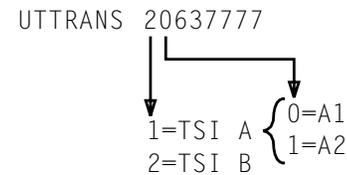


TABLE N CLOCK BITS			
FRAME TYPE	SET BIT	PACK TYPE	LOCATION
TSI-A1 [SD-4A023-01]	0,1,3	FA562 FB225 FB224 FA552 FA553 FA554	56-36 56-35 56-37 56-30 56-33 56-34
	15	FB220 FB225	56-39 56-35
TSI-A2 [SD-4A023-02]	0,1,3	FA562 FC463 FA552 FA553 FA554	56-36 56-35 56-30 56-33 56-34
TSI-B [SD-4A083-01]	0,1,3	FA1798 FA1233 FA1234 FC464	72-29 72-31 72-30 72-27

```

    DATA: TSI CRITICAL REGISTERS
    CREG 3 CREG 4
    CONTROLLER 0 04016521 00000000 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 20017600 00000000
    00000024 20637777 55555555 55555555 55555555 55555555
    CONTROLLER 1 00007134 42007134 00000002 41402000 00062000 00001000
    00000000 00000000 00000000 00000000 00000000 00000000
    00000000 00000000 00000000 00000000 00000000 00000000
    00000077 00000000 00000000 00000000 00000000 00000000
    00017037 00000000 00013026 00000000 00000000 00000000
    03670263 03770377 03770377 03730336 00100172 00000000
    03770377 03770377 03770377 03770377 03770377 00000000
    UTTRANS 00000000 00000077 00000000 00000000 20017600 00000000
    04/23/89 02:58:33
    #822
  
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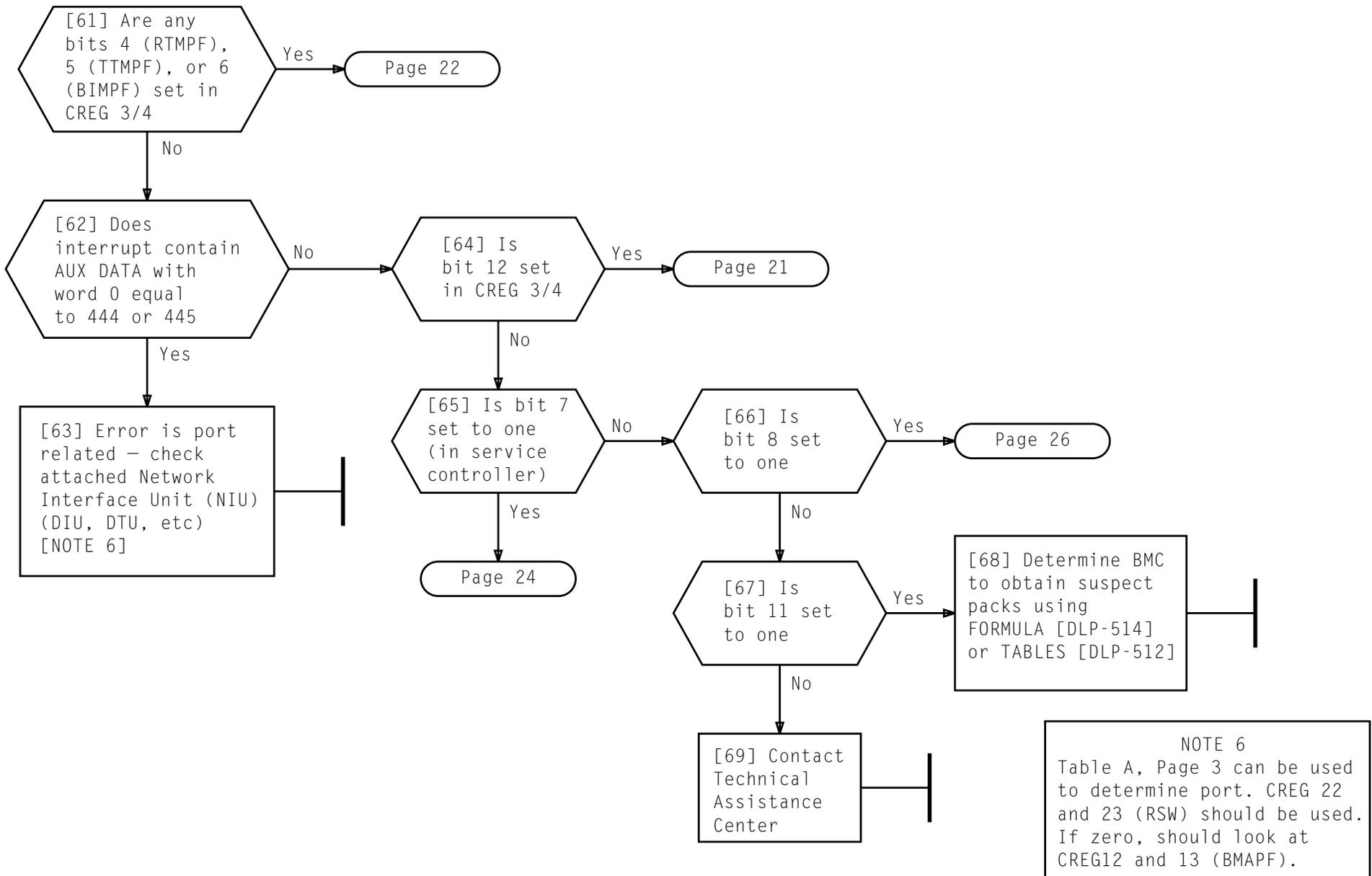
Figure 4 - TSI CREGs



EXAMPLE 2

NOTE 5
Analysis is for a simplex unit interrupt. Information is less conclusive than a duplex unit interrupt

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NOTE 6
 Table A, Page 3 can be used to determine port. CREG 22 and 23 (RSW) should be used. If zero, should look at CREG12 and 13 (BMAPF).

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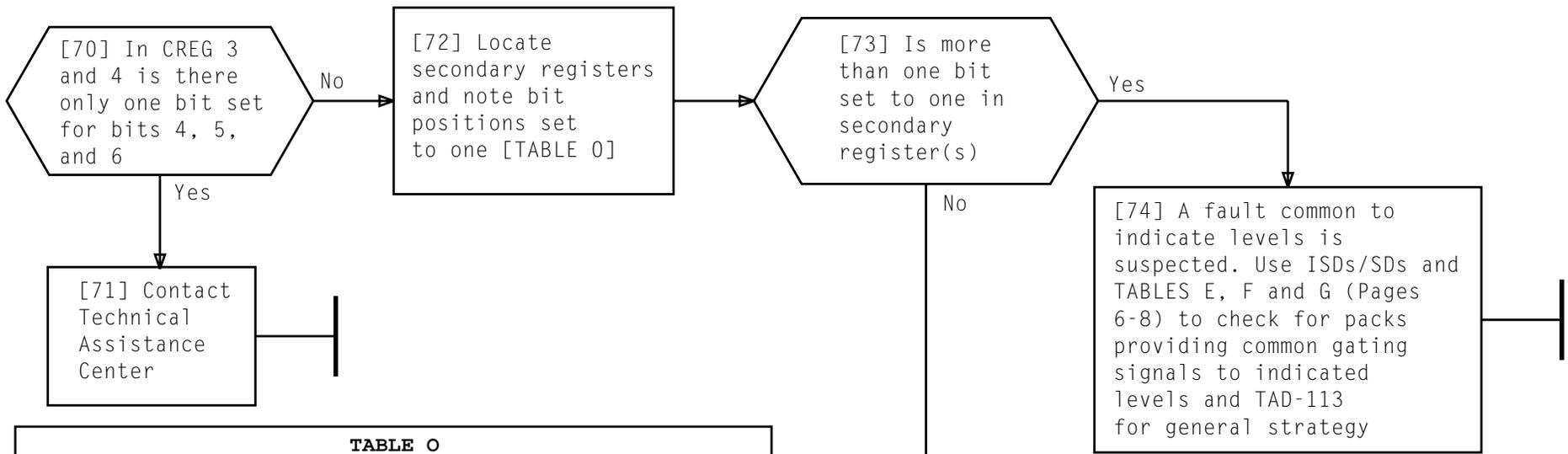


TABLE O SECONDARY REGISTERS FOR SET ESR BIT		
ASSOCIATED SECONDARY REGISTERS		
CREG 3, 4 ERROR SOURCE BIT	ORIGINAL TSI FRAME (SD-4A011-01) OR NEAR TERM TSI FRAME (SD-4A011-02)	COST REDUCED TSI FRAME (SD-4A083-01)
4(RTSMP)	CREG 6	CREG 6, CREG 7
5(TTSMP)	CREG 8	CREG 8, CREG 9
6(BIMPF)	CREG 10	CREG 10, CREG 11

TABLE P SPC AND LEVEL																
CREG	SPC								SPC							
6,8,10	1								0							
7,9,11	3								2							
BIT	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LEVEL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

[77] Using CREG 22 (TSI-A1/A2) or CREG 22 and 23 (TSI-B) determine bit position set to one [See Figure 4 and Example 2, Page 20, for frame type]

[78] Use bit position set to one and TABLE Q, then TABLE R to identify suspect packs. Use TOP 234-151-012 to replace TN circuit packs.

TABLE Q																
IDENTIFICATION OF SPC AND LEVEL																
(EVEN NUMBERED SECONDARIES)																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT POSITION
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	LEVEL
1							0							SPC		
* (ODD NUMBERED SECONDARIES)																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT POSITION
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	LEVEL
3							2							SPC		
* For TSI-B																

TABLE R								
SUSPECT PACKS FOR CREG 3/4 BIT 12								
TSI (SD-4A011-01, 02)				TSI (SD-4A083-01)				
LEVEL	CIRCUIT PACK TYPE	SPC 0	SPC 1	CIRCUIT PACK TYPE	SPC 0	SPC 1	SPC 2	SPC 3
0	FB221	38-23	60-23	FB221B	*24-69	*36-69	*48-69	*60-69
	FA567	38-19	60-19	FA1791	*24-68	*36-68	*48-68	*60-68
	FA569	38-11	60-11	FA1782	*24-66	*36-66	*48-66	*60-66
1	FB221	38-23	60-23	FB221B	*24-69	*36-69	*48-69	*60-69
	FA567	38-18	60-18	FA1791	*24-65	*36-68	*48-68	*60-68
	FA569	38-10	60-10	FA1782	*24-63	*36-63	*48-63	*60-63
2	FB221	38-22	60-22	FB221B	*24-61	*36-61	*48-61	*60-61
	FA567	38-17	60-17	FA1791	*24-60	*36-60	*48-60	*60-60
	FA569	38-09	60-09	FA1782	*24-58	*36-58	*48-58	*60-58
3	FB221	38-22	60-22	FB221B	*24-61	*36-61	*48-61	*60-61
	FA567	38-15	60-15	FA1791	*24-56	*36-56	*48-56	*60-56
	FA569	38-08	60-08	FA1782	*24-54	*36-54	*48-54	*60-54
4	FB221	38-21	60-21	FB221B	*24-52	*36-52	*48-52	*60-52
	FA567	38-14	60-14	FA1791	*24-51	*36-51	*48-51	*60-51
	FA569	38-07	60-07	FA1782	*24-49	*36-49	*48-49	*60-49
5	FB221	38-21	60-21	FB221B	*24-52	*36-52	*48-52	*60-52
	FA567	38-13	60-13	FA1791	*24-47	*36-47	*48-47	*60-47
	FA569	38-06	60-06	FA1782	*24-45	*36-45	*48-45	*60-45
6	FB221	38-20	60-20	FB221B	*24-43	*36-43	*48-43	*60-43
	FA567	38-12	60-12	FA1791	*24-41	*36-41	*48-41	*60-41
	FA569	38-05	60-05	FA1782	*24-39	*36-39	*48-39	*60-39
7				FB221B	*24-43	*36-43	*48-43	*60-43
			N/A	FA1791	*24-38	*36-38	*48-38	*60-38
			N/A	FA1782	*24-37	*36-37	*48-37	*60-37
* Bay 0 or 1 same as suspect controller								

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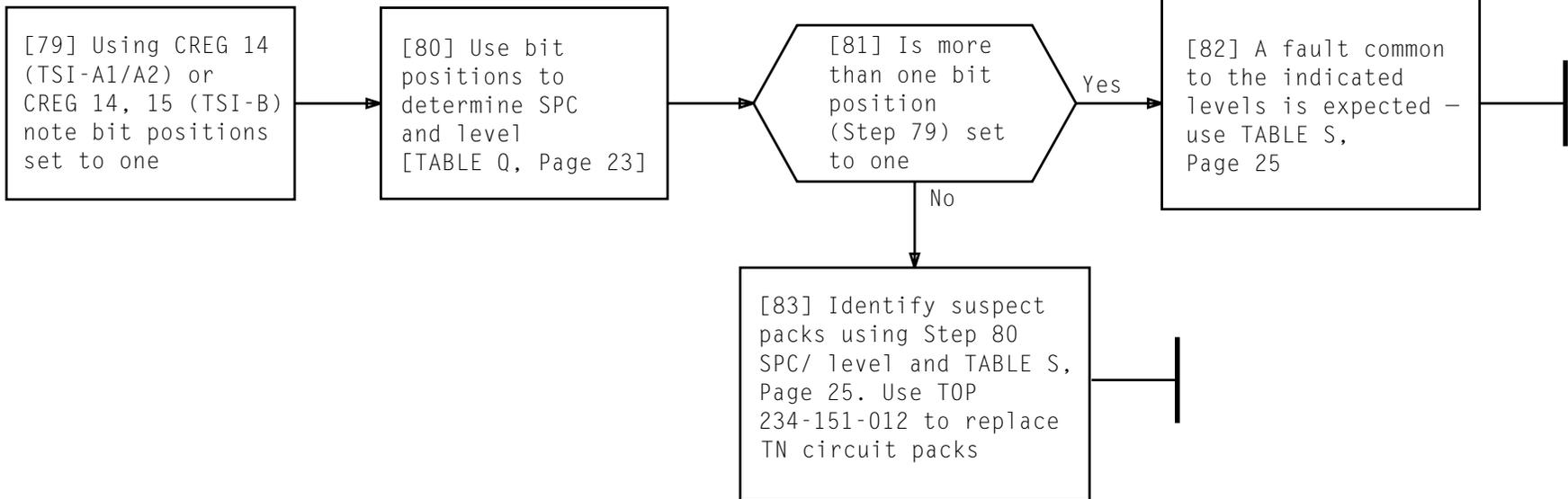


TABLE S - SUSPECT PACK LIST FOR ESR BIT 7											
SPC	FRAME TYPE	PACK TYPE	LEVEL								
			0	1	2	3	4	5	6	7	
0	TSI-A1 SD4A011-01	FA633	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04	
		FA542	(46-09, 46-08, 46-07)				(46-06, 46-05, 46-04)				
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	N/A	
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	N/A	
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)				
	TSI-A2 SD4A011-02	FA633B	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04	
		FA542	(46-09, 46-08, 46-07)				(46-06, 46-05, 46-04)				
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	N/A	
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	N/A	
		FA540	42-15, 42-14 (Address Select)				42-13, 42-12 (Address Select)				
	TSI-B SD4A083-01	FA1791	24-68	24-65	24-60	24-56	24-51	24-47	24-41	N/A	
		FA1782	24-66	24-63	24-58	24-54	24-49	24-45	24-39	N/A	
	1	TSI-A1 SD4A011-01	FA633	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
			FA542	(68-09, 68-08, 68-07)				(68-06, 68-05, 68-04)			
FA569			60-11	60-10	60-09	60-08	60-07	60-06	60-05	N/A	
FA567			60-19	60-18	60-17	60-15	60-14	60-13	60-12	N/A	
FA540			64-15, 64-14 (Address Select)				64-13, 64-12 (Address Select)				
TSI-A2 SD4A011-02		FA633B	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04	
		FA542	(68-09, 68-08, 68-07)				(68-06, 68-05, 68-04)				
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	N/A	
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	N/A	
		FA540	64-15, 64-14 (Address Select)				64-13, 64-12 (Address Select)				
TSI-B SD4A083-01		FA1791	36-68	36-65	36-60	36-56	36-51	36-47	36-41	36-38	
		FA1782	36-66	36-63	36-58	36-54	36-49	36-45	36-39	36-37	
2		TSI-B SD4A083-01	FA1791	48-68	48-65	48-60	48-56	48-51	48-47	48-41	48-38
			FA1782	48-66	48-63	48-58	48-54	48-49	48-45	48-39	48-37
3	TSI-B SD4A083-01	FA1791	60-68	60-65	60-60	60-56	60-51	60-47	60-41	60-38	
		FA1782	60-66	60-63	60-58	60-54	60-49	60-45	60-39	60-37	

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ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE (TSI)

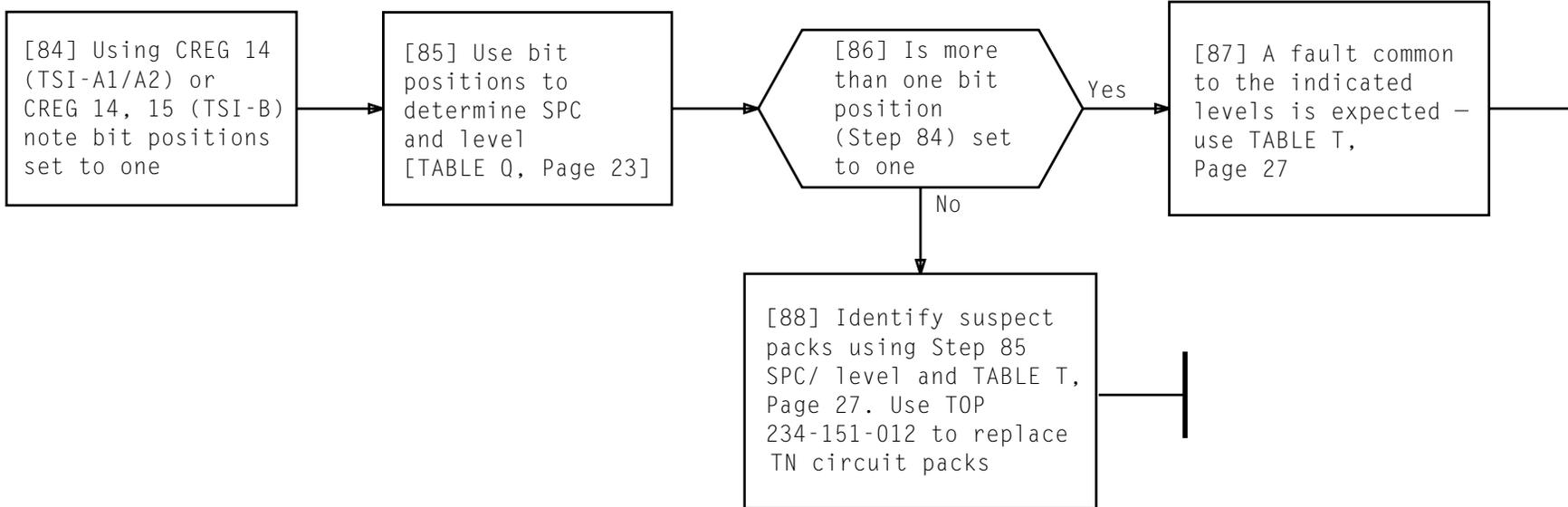
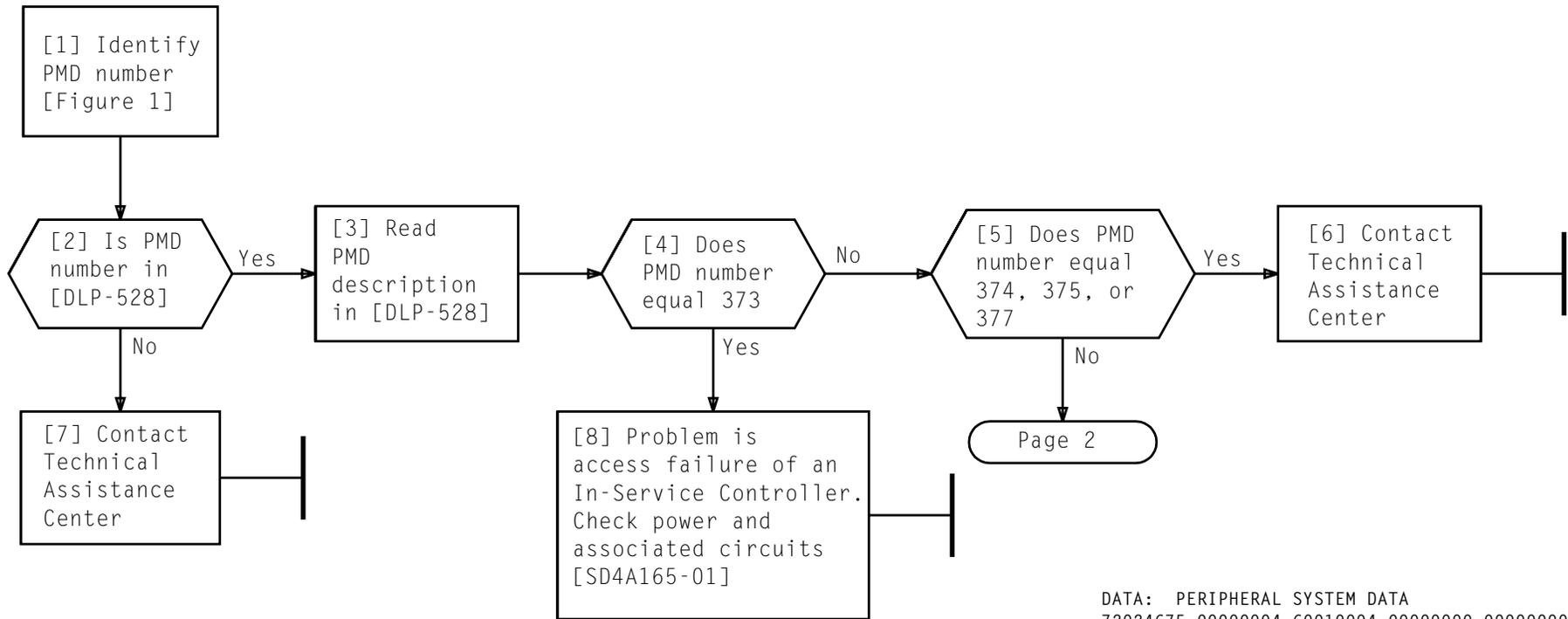


TABLE T – SUSPECT PACK LIST FOR ESR BIT 8										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6*	7*
0	TSI-A1 SD4A011-01	FA633	50-18	50-17	50-15	50-14	50-13	50-12	50-11	50-10
		FA544	50-26	50-25	50-24	50-23	50-22	50-21	50-20	50-19
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	50-18	50-17	50-15	50-14	50-13	50-12	50-11	50-10
		FA1198	50-26		50-24		50-22		50-20	
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-B SD4A083-01	FA1786	28-45	28-45	28-45	28-45	28-45	28-45	28-45	28-45
		FA1780*	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
	1	TSI-A1 SD4A011-01	FA633	72-18	72-17	72-15	72-14	72-13	72-12	72-11
FA544			72-26	72-25	72-24	72-23	72-22	72-21	72-20	72-19
FA540			68-18, 68-17 (Address Select)				68-15, 68-14 (Address Select)			
TSI-A2 SD4A011-02		FA633B	72-18	72-17	72-15	72-14	72-13	72-12	72-11	72-10
		FA1198	72-26		72-24		72-22		72-20	
		FA540	68-18, 68-17 (Address Select)				68-15, 68-14 (Address Select)			
TSI-B SD4A083-01		FA1786	40-45	40-45	40-45	40-45	40-45	40-45	40-45	40-45
		FA1780*	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
2		TSI-B SD4A083-01	FA1786	52-45	52-45	52-45	52-45	52-45	52-45	52-45
	FA1780*		52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
3	TSI-B SD4A083-01	FA1786	64-45	64-45	64-45	64-45	64-45	64-45	64-45	64-45
		FA1780*	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37
* FA1780 or FA1816 (wide band option on SPC - all levels)										

ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE (TSI)

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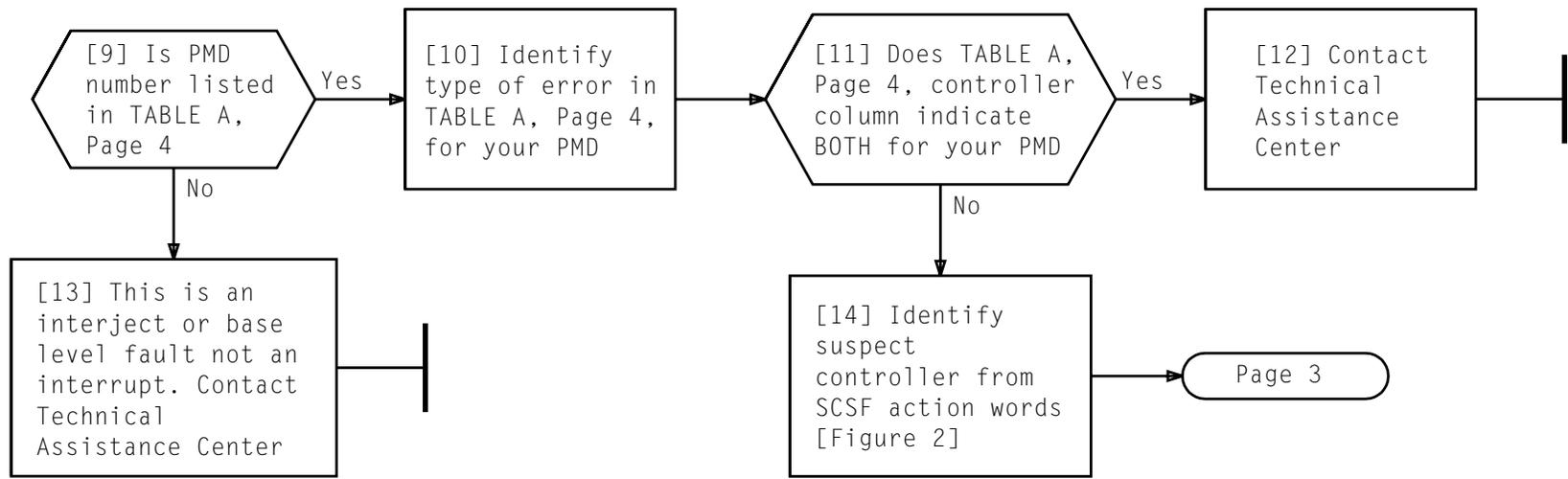
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DATA: PERIPHERAL SYSTEM DATA
72024675 00000004 60010004 00000000 00000000 00000004
00000000 00000004 00000000 01600001 01600041 60070041
01600041
DATA: INTERRUPT SOURCE DATA
00004401 77777766 00754000 02000000 00000001
DATA: FAULT RECOGNITION ISOLATION DATA
00000001 00000000 00000051 00000000 00000003 00000000
DATA: ERROR ANALYSIS STRATEGY DATA
00112000 00037200 00200100 00000022 00012000 01000101
00000000 00040000 00003051 01000000 62000000 01000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 12330204
12326240 14401152 00433106 00000034 00000000 00000001
00000000 00001604
POINT OF MAXIMUM DEFINITION (PMD)
04/21/92 10:00:52
#469
  
```

Figure 1 - Part of SCSF F-Level Printout

ANALYZE SCSF, F-LEVEL INTERRUPT

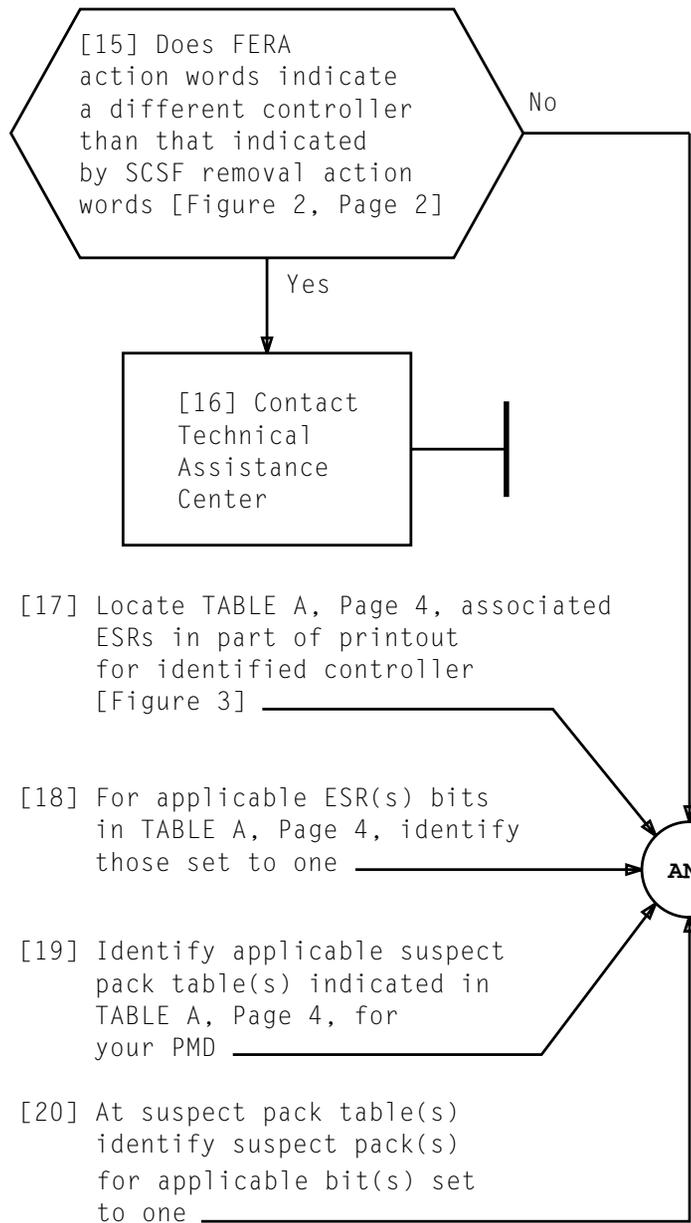
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```

A 00 REPT: F-LEVEL @15742476 MFNUM=00000034 MICON=00000020 MSG STARTED
LV=0040 D0=00000000 D1=00000000 D2=00000217 D3=00000000
APUFS INTERRUPT SCS 0
SCSF RESOLVED ERROR SCS 0 CONTR 0
SCSF RECOMMENDED NORMAL REMOVAL SCS 0 CONTR 0
SCSF RECOMMENDED DIAGNOSTICS SCS 0 CONTR 0
FERA REMOVED SCS 0 CONTR 0
FERA SCHED DGN SCS 0 CONTR 0
DATA: F-LEVEL
  
```

Figure 2 – Part of F-Level Interrupt Printout



CSTATUS	HWSTATR	MADATA	FSTATUS	SCUOS	CESR	C O N T R O
PEST	CONTROL	EBLKSTATL	EBLKSTATH	EBLKADR	GRESR	
GRCNTR	GADRO	GADRI	EXESR	EXCSTATL	EXCSTATH	
EXFPR	EXPC	EXANTIM	EXSTKBL	EXSTKBH	EXSTRPTR	
EXINTR	RLBPTR	WLPBPTR	RDBPTR	WDBPTR	MBPTRS	
SHMBPTR	MBSTAT	SCU0ESR	SCU1ESR	SCU2ESR	SCU3ESR	
SCU4ESR	SCU5ESR	SCU6ESR	SCU7ESR	SCU8ESR	SCU9ESR	
SCU10ESR	SCU11ESR	SCU12ESR	SCU13ESR	SCU14ESR	SCU15ESR	
FWERRBUF0	FWERRBUF1	FWERRBUF2	FWERRBUF3	FWERRBUF4	FWERRBUF5	
FWERRBUF6	FWERRBUF7	FWERRBUF8	FWERRBUF9	EBMEMRST	EBLNKADR	
EBLNKSTATL	EBLNKSTATH	0.....0	0.....0	0.....0	0.....0	
MEMN	XLATE	5.....5	5.....5	5.....5	5.....5	
CSTATUS	HWSTATR	MADATA	FSTATUS	SCUOS	CESR	C O N T R 1
PEST	CONTROL	EBLKSTATL	EBLKSTATH	EBLKADR	GRESR	
GRCNTR	GADRO	GADRI	EXESR	EXCSTATL	EXCSTATH	
EXFPR	EXPC	EXSANTIM	EXSTKBL	EXTKBH	EXSTRPTR	
EXINTR	RLBPTR	WLPBPTR	RDBPTR	WDBPTR	MAPTAS	
SHMPTA	MBSTAT	SCU0ESR	SCU1ESR	SCU2ESR	SCU3ESR	
SCU4ESR	SCU5ESR	SCU6ESR	SCU7ESR	SCU8ESR	SCU9ESR	
SCU10ESR	SCU11ESR	SCU12ESR	SCU13ESR	SCU14ESR	SCU15ESR	
FWERRBUF0	FWERRBUF1	FWERRBUF2	FWERRBUF3	FWERRBUR4	FWERRBUF5	
FWERRBUF6	FWERRBUF7	FWERRBUR8	FWERRBUF9	EBMEMRST	EBLNKADR	
EBLNKSTATL	EBLNKSTATH	0.....0	0.....0	0.....0	0.....0	

Figure 3 - SCS Critical Register (CREG) Layout [Part of REPT Message]

TABLE A					
PMD NUMBER	CONTROLLER	TYPE OF ERROR	ASSOCIATED ERROR SOURCE REGISTER	APPLICABLE ESR BIT(S)	ESR SUSPECT PACK TABLE
331,340,350,360	ACTIVE	RAM ERROR	GRESR	0,1,2,3,4,5,6,7	E
330,341	STANDBY		EXESR	3,5,6,7,8,9,10,11,12	F
57	BOTH	SANITY/STACK BOUNDARY	EXESR	0,1	F
56,75,155,173	ACTIVE				
55,76	STANDBY				
332	BOTH	FATAL FIRMWARE	CESR	8	B
333,343,353,363	ACTIVE				
334,344	STANDBY				
47	BOTH	FIRMWARE (NO PPE)	CESR	7,9,10,11	B
50,117,153,176	ACTIVE				
51,125	STANDBY				
52	BOTH	FIRMWARE (WITH PPE)	CESR	7,9,10,11,13	B
53,126,154,174	ACTIVE				
54,127	STANDBY				
46,62,113,114,115,116,124	BOTH	MISMATCH	CESR	22,23	B
44,60,103,104,105,106,122,152,175	ACTIVE				
45,61,107,110,111,112,123	STANDBY				
262,272	BOTH	IAS	EBLKSTATL	0,1,2,4,7	C
261,271	ACTIVE		EBLKSTATH	0,1,4	D
260,270	STANDBY				
40,41,42,43	BOTH	HARDWARE	CESR	6,12,13,14,15,16,17,18,19,20,21	B
30,31,32,33,71,72,120,150,151,171,172,177	ACTIVE				
34,35,36,37,73,74,121	STANDBY				
1,4,5,70	BOTH	NO ERROR SOURCE	CESR	0,1	B
2,130,131,132,170	ACTIVE				
3	STANDBY				

**TABLE B
CONTROLLER ERROR SOURCE REGISTER (CESR)**

BIT NUMBER	REGISTER BITNAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING†	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0	ASWF	ODPUR260	B11/G7	1DPUR260	B24/H7	All-Seems-Well Failure (An ASWF asserts the Peripheral Unit Failure (PUF) flag)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
1	AINT	ODPUR260	B11/G7	1DPUR260	B24/H7	Autonomous Interrupt (An AINT asserts the Autonomous Peripheral Unit Failure (APUF) flag)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
2	PUPFE	ODPUW390	B11/B8	1DPUW390	B24/B8	Peripheral unit bus even parity failure (This error asserts an ASWF)	UN350 UN349 UN349 UN349	045-112 045-152 045-160 045-168	053-112 053-152 053-160 053-168
3	PUPFO	ODPUW380	B11/B8	1DPUW380	B24/B8	Peripheral unit bus odd parity failure (This error asserts an ASWF)	UN350 UN349 UN349 UN349	045-112 045-152 045-160 045-168	053-112 053-152 053-160 053-168
4	APUT	ODPUR270	B11/G7	1DPUR270	B24/H7	Autonomous Peripheral Unit Trouble (interject level) – (Indicates a Service Circuit Unit (SCU) detected error or a digit buffer overflow)	SCU x UN350 KCN3 KCN3	* 045-112 045-048 045-056	* 053-112 053-048 053-056
5	APUB	ODPUR280	B11/G7	1DPUR280	B24/H7	Autonomous Peripheral Unit Base level (NOT CURRENTLY USED BY THE SCS)	UN350 UN351	045-112 045-072	053-112 053-072
6	UNASOP	None		None		Invalid/unassigned op-code (This error asserts an ASWF)	UN350 UN349 UN349 UN351	045-112 045-152 045-160 045-072	053-112 053-152 053-160 053-072

**TABLE B (Contd)
CONTROLLER ERROR SOURCE REGISTER (CESR)**

BIT NUMBER	REGISTER BITNAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING†	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
7	SWERR0	None		None		Firmware error bit 0 (This error asserts an AINT/ASWFt)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
8	SWERR1	None		None		Firmware error bit 1 (This error asserts an AINT/ASWFt)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
9	SWERR2	None		None		Firmware error bit 2 (This error asserts an AINT/ASWFt)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
10	SWERR3	None		None		Firmware error bit 3 (This error asserts an AINT/ASWFt)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
11	SWERR4	None		None		Firmware error bit 4 (This error asserts an AINT/ASWFt)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
12	MODFL	None		None		PUBI [UN350] Mode Failure (This error asserts an ASWF)	UN350 UN349 UN349	045-112 045-144 045-152	053-112 053-144 053-152

**TABLE B (Contd)
CONTROLLER ERROR SOURCE REGISTER (CESR)**

BIT NUMBER	REGISTER BITNAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING†	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
13	PPE	None		None		PUBI [UN350] Parity Error (This error asserts an AINT/ASWFt)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
14	SPARE14	None		None		Spare bit (NOT ASSIGNED) (This bit asserts an AINT/ASWFt)	UN350 UN351	045-112 045-072	053-112 053-072
15	LCLKF	None		None		PUBI [UN350] local clock failure (This error asserts an AINT/ASWFt)	UN350 UN351	045-112 045-072	053-112 053-072
16	HWSPARE0	None		None		Hardware spare 0 (NOT ASSIGNED) (This bit asserts an AINT/ASWFt)	UN350 UN351	045-112 045-072	053-112 053-072
17	HWSPARE1	None		None		Hardware spare 1 (NOT ASSIGNED) (This bit asserts an AINT/ASWFt)	UN350 UN351	045-112 045-072	053-112 053-072
18	EBSUM	0EEBSUM0	B11/B3	1EEBSUM0	B24/B3	Extended Bus interface [KCN3] error summary (This error asserts an AINT/ASWFt)	KCN3 UN350	045-048 045-112	053-048 053-112
19	GRAMSUM	0EGRSUM0	B10/F8	1EGRSUM0	B23/F8	Global RAM [UN352] memory data parity error summary (This error asserts an AINT/ASWFt)	UN352 UN350	045-088 045-112	053-088 053-112
20	EXECSUM	0EEXSUM0	B10/C5	1EEXSUM0	B23/C5	EXEC [UN351] error source summary for bits 0-15 in the EXEC error source register (This error asserts an AINT/ASWFt)	UN351 UN350	045-072 045-112	053-072 053-112
21	BPSUM	0EBPSUM0	B10/F8	1EBPSUM0	B23/F8	Backplane error summary (Detected on the GRAM [UN352] circuit pack) (This error asserts an AINT/ASWFt)	UN350 UN351 UN352 KCN3 KCN3 UN357 UN357	045-112 045-072 045-088 045-048 045-056 045-024 045-120	053-112 053-072 053-088 053-048 053-056 053-024 053-120
22	CPMM	0ECPMM0	B10/C5	1ECPMM0	B23/C5	EXEC [UN351] clock phase error (This error asserts an AINT/ASWFt)	UN351 UN350	045-072 045-112	053-072 053-112

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TABLE B (Contd)									
CONTROLLER ERROR SOURCE REGISTER (CESR)									
BIT NUMBER	REGISTER BITNAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING †	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
23	CCMM	0ECCMM0	B10/F8	1ECCMM0	B23/F8	Cross-controller mismatch (Detected on the GRAM [UN352] circuit pack) (This error asserts an AINT/ASWF†; a fault on the mate controller can also trigger this error)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
<p>* SCU x is the Service Circuit Unit in which the fault was detected; where x is the value of the content 0145 Extended Bus Address Register. A TSI fault can also trigger this error. The KCN3 in position 48 interfaces with SCUs 0 - 7; whereas, the KCN3 in position 56 interfaces with SCUs 8 - 15.</p> <p>† AINT/ASWF - AINT (Autonomous Interrupt) is generated by the error if no peripheral unit order is being processed; whereas, ASWF (All-Seems-Well Failure) occurs if the error is triggered during order processing.</p>									

ANALYZE SCSF, F-LEVEL INTERRUPT

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TABLE C
EXTENDED BUS LINK STATUS REGISTER LOW (EBLKSTATL)
(32 bit register – upper 8 bits are listed in EBLKSTATH)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION*	CONTR 1 LOCATION*
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0	ICRSCU	None		None		Illegal command received by the SCU	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
1	RPESCU	None		None		SCU receive link parity error	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
2	RFESCU	None		None		SCU receive link frame error	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
3	SPARE3	None		None		Spare bit (NOT USED)			
4	RFFSCU	None		None		SCU receive FIFO full (NO ERROR)			
5	RFHFSCU	None		None		SCU receive FIFO half full (NO ERROR)			
6	TFNESCU	None		None		SCU transmit FIFO not empty (NO ERROR)			
7	ERRSUM	None		None		SCU error summary bit	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
8	TSA	None		None		Transmit sequencer active (NO ERROR)			
9-14	TSEQS	None		None		Transmit sequencer state (NO ERROR)			
15	STATLSSRB	None		None		This bit reflects the state of the Set Status Register Bit (bit 17) of the EBI control register (NO ERROR)			
16	RSA	None		None		Receive sequencer active (NO ERROR)			
17-21	RSEQS	None		None		Receive sequencer state (NO ERROR)			
22	NOC	None		None		Near operation complete (NO ERROR)			
23	EBIOC	None		None		Operation complete sync (NO ERROR)			

* SCU n is the Service Circuit Unit in which the KCN4 is located; where n is the value of the contents of the Extended Bus Address Register. The KCN3 in position 48 interfaces with SCUs 0 – 7; whereas, the KCN3 in position 56 interfaces with SCUs 8 – 15.

TABLE D
EXTENDED BUS LINK STATUS REGISTER HIGH (EBLKSTATH)
(32 bit register – lower 24 bits are listed in EBLKSTATL)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION*	CONTR 1 LOCATION*
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0	ICRSCC	None		None		Illegal command received by the controller	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
1	RLVSCC	None		None		Receive link violation by the controller	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
2	STATHSSRB	None		None		This bit reflects the state of the Set Status Register Bit (bit 17) of the EBI control register (NO ERROR)			
3	DDATPE	None		None		Controller destination data parity error (This error asserts the EBSUM flag in the UN350 CESR register)	KCN4 KCN3 UN350 UN351 UN352	045-048 045-056 045-112 045-072 045-088	053-048 053-056 053-112 053-072 053-088
4	RPE	None		None		Receiver parity error from an EB link	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
5	SPE	None		None		Controller source address parity error (This error asserts the EBSUM flag in the UN350 CESR register)	KCN4 KCN3 UN350 UN351 UN352	045-048 045-056 045-112 045-072 045-088	053-048 053-056 053-112 053-072 053-088
6	DPE	None		None		Controller destination address parity error (This error asserts the EBSUM flag in the UN350 CESR register)	KCN4 KCN3 UN350 UN351 UN352	045-048 045-056 045-112 045-072 045-088	053-048 053-056 053-112 053-072 053-088

TABLE D (Contd)
EXTENDED BUS LINK STATUS REGISTER HIGH (EBLKSTATH)
(32 bit register – lower 24 bits are listed in EBLKSTATL)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
7	TPE	None		None		Transmit parity error to an EB link (This error asserts the EBSUM flag in the UN350 CESR register)	KCN3 KCN3	045-048 045-056	053-048 053-056

* SCU n is the Service Circuit Unit in which the KCN4 is located; where n is the value of the contents of the Extended Bus Address Register. The KCN3 in position 48 interfaces with SCUs 0 – 7; whereas, the KCN3 in position 56 interfaces with SCUs 8 – 15.

TABLE E
GLOBAL RAM ERROR SOURCE REGISTER (GRESR)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0-3	ERAP	None		None		Ram bank A data parity error bits (These errors assert the GRAMSUM flag in the UN350 CESR register)	UN352	045-088	053-088
4-7	ERBP	None		None		Ram bank B data parity error bits (These errors assert the GRAMSUM flag in the UN350 CESR register)	UN352	045-088	053-088
8-11	EDDP	None		None		Destination bus data parity error bits (These errors assert the BPSUM flag in the UN350 CESR register)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056
12	EDAP	None		None		Destination bus address parity error (These errors assert the BPSUM flag in the UN350 CESR register)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056
13	ESAAP	None		None		Source bus A address parity error (This error asserts the BPSUM flag in the UN350 CESR register)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056
14	ESBAP	None		None		Source bus B address parity error (This error asserts the BPSUM flag in the UN350 CESR register)	UN352 UN351	045-088 045-072	053-088 053-072
15	EXUMM	None		None		Cross-connect update bus mismatch (This error asserts the CCMM flag in the UN350 CESR register; it may be generated due to a mate controller fault)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056

TABLE E (Contd)
GLOBAL RAM ERROR SOURCE REGISTER (GRESR)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
16	EXSMM	None		None		Cross-connect syndrome bus mismatch (This error asserts a CCMM flag in the UN350 CESR register; it may be generated due to a mate controller fault)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056
17	SPARE17	None		None		(NOT USED)			
18	SPARE18	None		None		(NOT USED)			
19	SPARE19	None		None		(NOT USED)			
20	SPARE20	None		None		(NOT USED)			
21	SPARE21	None		None		(NOT USED)			
22	SPARE22	None		None		(NOT USED)			
23	SPARE23	None		None		(NOT USED)			

TABLE F
EXEC ERROR SOURCE REGISTER (EXESR)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0	STKBNDERR	None		None		EXEC stack bounds error (This error asserts the EXEC SUM flag in the UN352 CESR register. A firmware bug may cause this error)	UN351	045-072	053-072
1	SANITYTMR	None		None		Sanity timer elapsed (This error asserts the EXEC SUM flag in the UN352 CESR register. A firmware bug may cause this error)	UN351	045-072	053-072
2	ALUMM	None		None		ALU mismatch*	UN351	045-072	053-072
3	MALUPERR	None		None		Source A or B data parity error*	UN351 UN352 UN350 KCN3 KCN3	045-072 045-088 045-112 045-048 045-056	053-072 053-088 053-112 053-048 053-056
4	SPARE4	None		None		(NOT USED)			
5	MPERR0	None		None		Microword parity error (byte 0)*	UN351	045-072	053-072
6	MPERR1	None		None		Microword parity error (byte 1)*	UN351	045-072	053-072
7	MPERR2	None		None		Microword parity error (byte 2)*	UN351	045-072	053-072
8	MPERR3	None		None		Microword parity error (byte 3)*	UN351	045-072	053-072
9	MPERR4	None		None		Microword parity error (byte 4)*	UN351	045-072	053-072
10	MPERR5	None		None		Microword parity error (byte 5)*	UN351	045-072	053-072
11	MPERR6	None		None		Microword parity error (byte 6)*	UN351	045-072	053-072
12	MPERR7	None		None		Microword parity error (byte 7)*	UN351	045-072	053-072
13	SPARE13	None		None		(NOT USED)			
14	SPARE14	None		None		(NOT USED)			
15	SOFTERR	None		None		Software defined error (This error is normally set by software and asserts the EXEC SUM flag in the UN352 CESR register)	UN351	045-072	053-072

TABLE F (Contd)
EXEC ERROR SOURCE REGISTER (EXESR)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
16	CFPEMW0	None		None		Force microword parity error - byte 0 (NO ERROR)			
17	CFPEMW1	None		None		Force microword parity error - byte 1 (NO ERROR)			
18	CFPEMW2	None		None		Force microword parity error - byte 2 (NO ERROR)			
19	CFPEMW3	None		None		Force microword parity error - byte 3 (NO ERROR)			
20	CFPEMW4	None		None		Force microword parity error - byte 4 (NO ERROR)			
21	CFPEMW5	None		None		Force microword parity error - byte 5 (NO ERROR)			
22	CFPEMW6	None		None		Force microword parity error - byte 6 (NO ERROR)			
23	CFPEMW7	None		None		Force microword parity error - byte 7 (NO ERROR)			

* These errors assert the EXEC SUM flag in the UN352 CESR register.

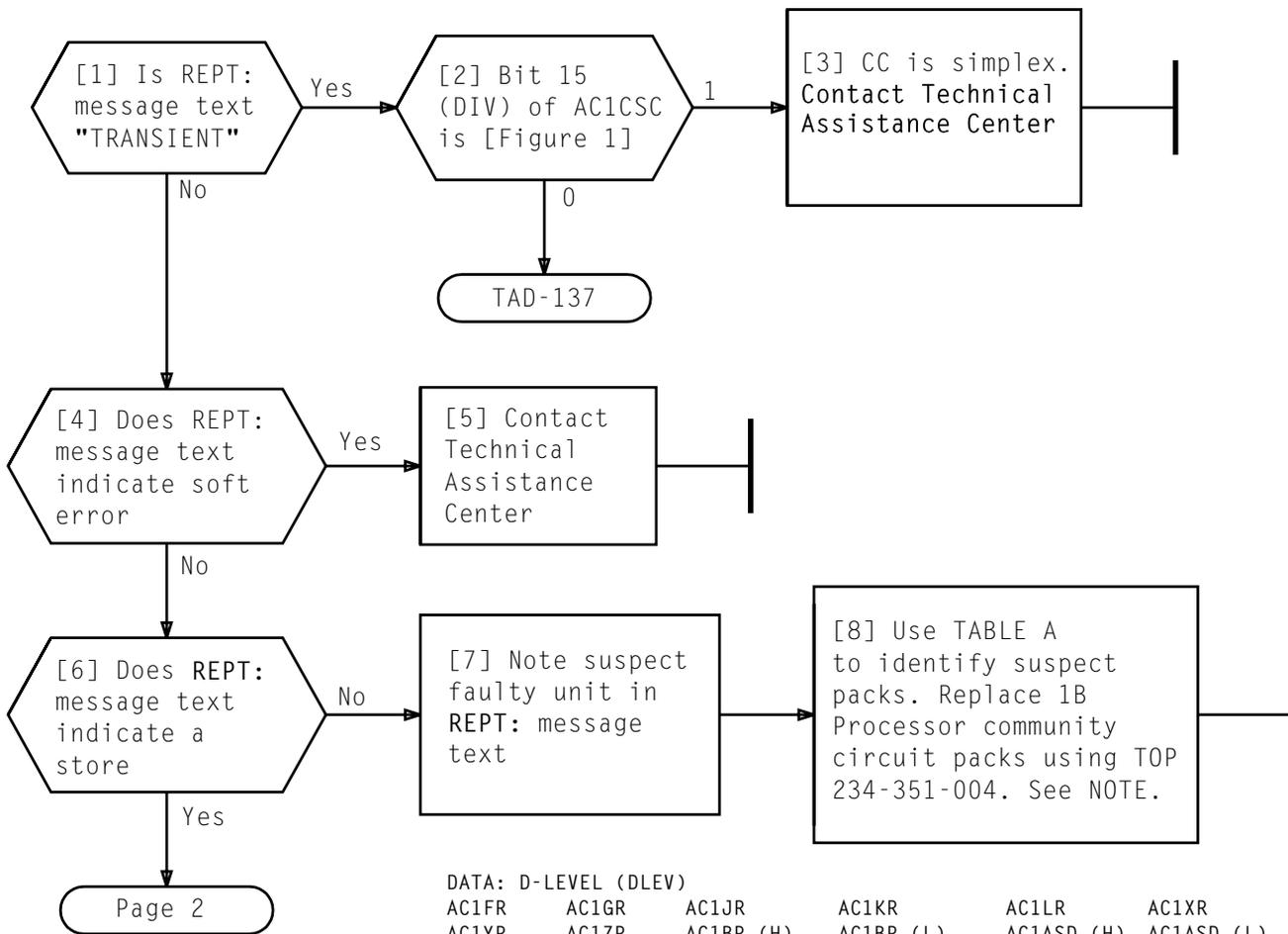


TABLE A		
SUSPECT UNIT	SUSPECT PACK(S)	PACK LOCATION
CC	KLW 3	41-104
	KLW 4	41-112
	KLW 17/KLW117	41-078
	KLW 6	41-054
	KLW 22	41-120
IFBC	KLW 13	58-070
	KLW 20	58-062
MUP	KLW 16/KLW116	58-078
AUI	KLW 18	58-120
SSD	KLW 15	58-168

DATA: D-LEVEL (DLEV)

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR (H)	AC1BR (L)	AC1ASD (H)	AC1ASD (L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS (H)	AC1BRS (L)	ST1CES	ST1ILA
AC1AP	AC1ABC	AC1IBR	ST1IBR	AC1TAR	AC1BNCTL

Figure 1 - Part of D-Level REPT message

NOTE	
Suspect units numbered 0 are in bay 0 and suspect units numbered 1 are in bay 1.	
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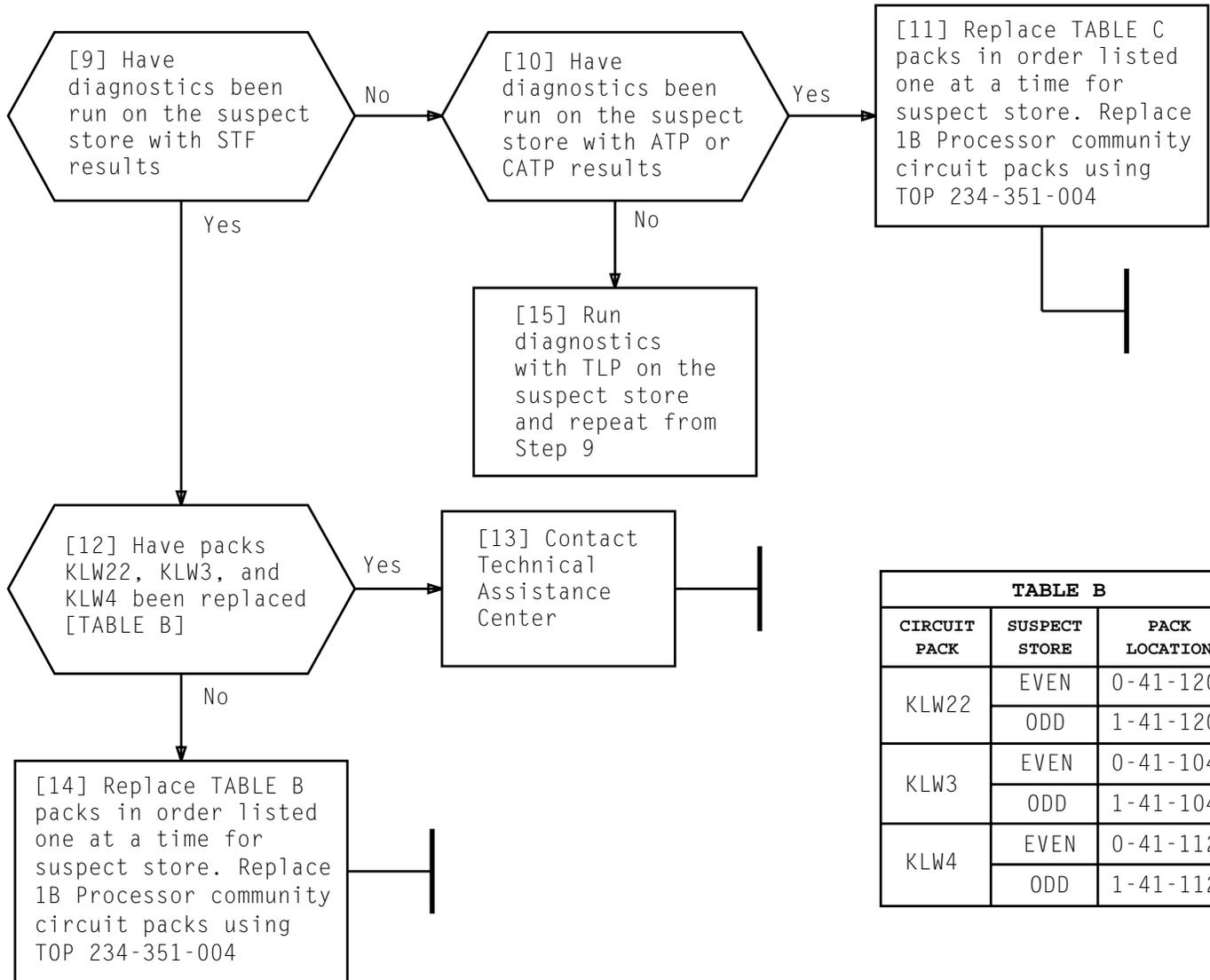


TABLE C		
CIRCUIT PACK	SUSPECT STORE	PACK LOCATION
KLV1	CS0	0-24-006
	CS1	1-24-006
	CS2	0-24-176
	CS3	1-24-176
	CS4	0-24-014
	CS5	1-24-014
	CS6	0-24-168
	CS7	1-24-168
	CS8	0-24-022
CS9	1-24-022	
KLV2	PS0	0-41-128
	PS1	1-41-128
	PS2	0-41-136
KLV22	EVEN	0-41-120
	ODD	1-41-120
KLV3	EVEN	0-41-104
	ODD	1-41-104
KLV4	EVEN	0-41-112
	ODD	1-41-112
KLV13	EVEN	0-58-070
	ODD	1-58-070
KLV20	EVEN	0-58-062
	ODD	1-58-062
KLV18	EVEN	0-58-120
	ODD	1-58-120
KLV16/ KLV116	EVEN	0-58-078
	ODD	1-58-078
KLV26	EVEN	0-24-086
	ODD	1-24-086
KLV27	EVEN	0-27-096
	ODD	1-27-096

TABLE B		
CIRCUIT PACK	SUSPECT STORE	PACK LOCATION
KLV22	EVEN	0-41-120
	ODD	1-41-120
KLV3	EVEN	0-41-104
	ODD	1-41-104
KLV4	EVEN	0-41-112
	ODD	1-41-112

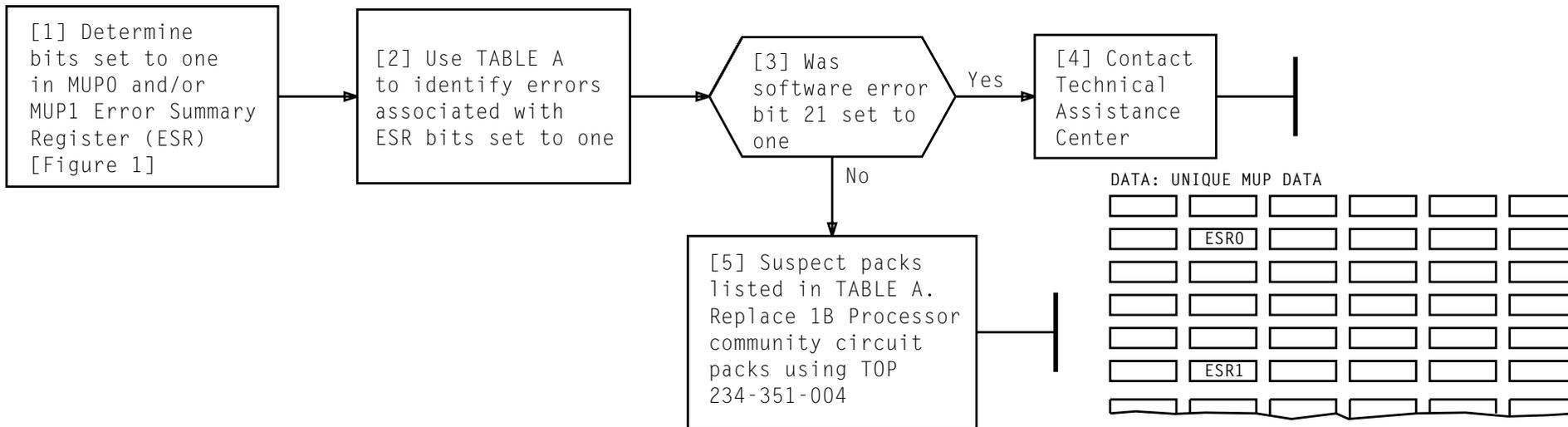


Figure 1 - Part of REPT Message

TABLE A - MUP ESR0/1							
BIT SET TO ONE	ERROR	SUSPECT PACKS*	PACK LOCATION	BIT SET TO ONE	ERROR	SUSPECT PACKS*	PACK LOCATION
2	DETECTED NO ALL SEEMS WELL	ALL ERRORS KLV16/ KLV116	58-078†	11	IFB ERROR- MTCE INTERRUPT	ALL ERRORS KLV16/ KLV116	58-078†
3	DETECTED ALL SEEMS WELL FAILURE			16	SANITY TIMEOUT		
4	MASTER DETECTED DATA PARITY ERROR			17	68010 BUS ERROR		
5	MUP DETECTED DATA PARITY ERROR			18	DRAM ERROR		
6	MUP DETECTED CONTROL ERROR			19	MEMORY ACCESS ERROR		
7	MUP DETECTED UNUSED ADDRESS ERROR			20	BOTH MUPs ACTIVE		
8	MUP DETECTED ADDRESS PARITY ERROR			21	SOFTWARE DETECTED ERROR		
9	SENT ALL SEEMS WELL FAILURE			22	MUP FORCED IN HARDWARE		
10	CLIENT ERROR- MTCE INTERJECT			23	USER DEFINED OPERATIONAL INTERJECT		

* A possible, though unlikely, suspect pack is KLV25 at 58-086.
 † MUPO pack location is 058-078, MUP1 is 158-078

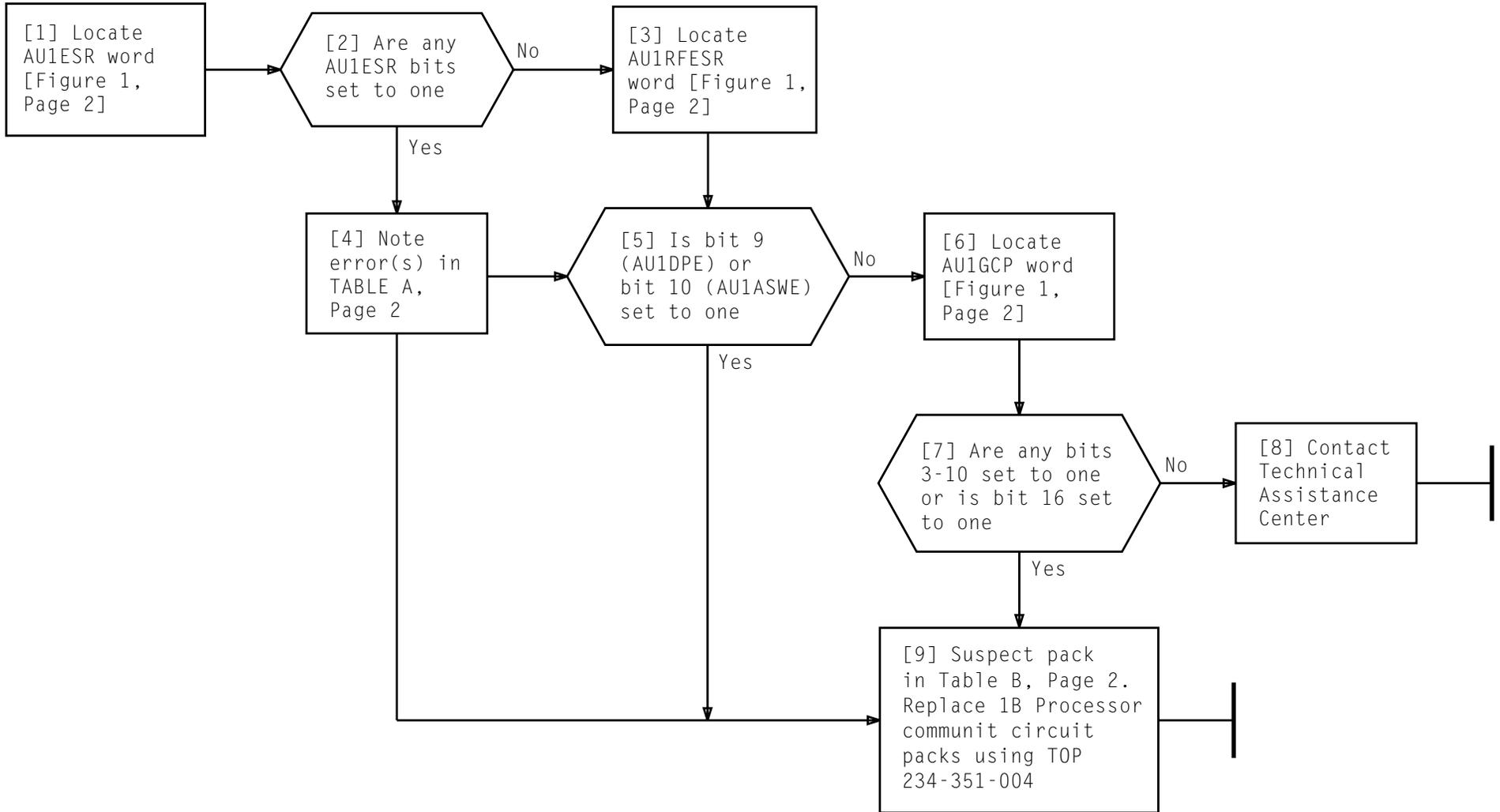


TABLE A - AUIESR			
BIT SET TO ONE	ERROR	BIT SET TO ONE	ERROR
0	DMA LOWER LIMIT EXCEEDED	9	SENT ALL-SEEMS-WELL FAILURE
1	DMA UPPER LIMIT EXCEEDED	10	AU BUS DETECTED ERROR
2	DETECTED NO ALL SEEMS WELL	11	IFB ERROR MTCE INTERRUPT
3	DETECTED ALL SEEMS WELL FAILURE	16	COMMAND OVERWRITE ERROR
4	MASTER DETECTED DATA PARITY ERROR	17	AU VERIFY MISMATCH ERROR
5	SLAVE DETECTED DATA PARITY ERROR	18	AU SAP VERIFY MISMATCH ERROR
6	SLAVE DETECTED COMMAND ERROR	19	AU STORE ADDRESS BUS PARITY ERROR
7	SLAVE DETECTED INVALID ADDRESS ERROR	20	AU REPLY BUS PARITY ERROR
8	SLAVE DETECTED ADDRESS PARITY ERROR		

DATA: COMMON AUXILIARY UNIT DATA



Figure 1 - Part of REPT Message

TABLE B	
PACK	LOCATION
KLW18	58-118
UN338	70-094*
UN338	70-110*
UN338	70-126*
UN338	70-142†
UN338	70-158†
UN338	70-174†

* BUS 0 locations (See NOTE, [Figure 1])
 † BUS 1 locations (See NOTE, [Figure 1])

NOTE	
AUIAUB register bit 8 (AUIAUOMIJ) set to one indicates bus 0 used and bit 9 (AUIAU1MIJ) set to one indicates bus 1 used	
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Recommendations to Eliminate Faulty/Noisy Client/IFB

These steps are needed because excessive transient errors have occurred and the faulty/noisy unit could not be identified and removed by fault recovery.

These steps attempt to eliminate the possible source of the error/fault. Each step is taken until the transient error disappears or technical assistance is requested. The community involved is one IFB with its clients (assuming both CCs have reported the same error on a client).

- 1) Normally the D-LEV IFFR TRANSIENT report indicates a unit involved with the error. Replace the unit. If this unit is an active duplex-essential unit, switch the mate active first.
- 2) Next step is to replace the units one at a time on the same IFB bus on which the transient error occurred, following the same guidelines on the duplex-essential unit. IFB bus member number equals error unit member number.
- 3) If the error persists after all the units have been replaced, remove the bus.
- 4) If the IFB passed diagnostics and the error persists, request technical assistance.

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[1] Are any GCP reply register bits 4-5, 8-11, 13-15, or 17-21 set to one [Figure 1, Page 2]

No

[2] Contact Technical Assistance Center

Yes

[3] See NOTES 1, 2, and 3. Identify suspect pack vertical location [TABLE A] and horizontal location [TABLE B] associated with GCP reply register bits set to one. Use TOP 234-351-021 or 234-351-022 to replace IOP circuit packs

TABLE A			
IOUS	IOMP	FRAME VERTICAL LOCATION	
		SD5A052-01 SD5A052-02	
		SD5A052-01	SD5A052-02
0	0	62	62
	1	54	54
1	0	38	32
	1	30	24
2	0	62	62
	1	54	54
3	0	38	32
	1	30	24
4	0	62	62
	1	54	54
5	0	38	32
	1	30	24
6	0	62	62
	1	54	54
7	0	38	32
	1	30	24

TABLE B			
GCP REPLY REGISTER			
GCP BIT	SUSPECT EQUIPMENT		
	TYPE	HORIZONTAL LOCATION	COMMENTS
4,5	FG23	35	—
	FG41	24	—
	FG25	39	—
	136H	08	Power unit*
8,9	235A	02	Power unit
	FG41	24	—
10,11	FG44	28	May be FG87
	FG20	22	—
13,14	FG43	31	May be FG86
	FG44	28	May be FG87
15	FG22	26	—
	FG20	22	—
17	FG22	26	—
	FG44	28	May be FG87
18,19	FG22	26	—
	FG43	31	May be FG86
	FG44	28	May be FG87
20	FG42	33	May be FG85
	FG22	26	—
21	FG22	26	—
	FG42	33	May be FG85

* Even IOUS - Vert 68
Odd IOUS - Vert 44

NOTES

1. If IOUS only is indicated, assume IOMP 0 for TABLE A use
2. IOUS number on printout is same as IOP number on power switch
3. Notify users that channels are to be removed from service

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ANALYZE PFLR F-LEVEL INTERRUPT, IOP FRAME (SD-5A052-01/02)
EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)

DATA: F-LEVEL (FLEV)

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASF(H)	AC1ASF(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	AC1LIT	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1LR	ST1INS
AC1PSQ	AC1ULR	AC1PES	ST1RP1	ST1ER	ST1PRM
ST1PRL	ST1PSC	AC1RP0	AC1RP1	ST1RP0	ST1RP1
ST1CSC	ST1INH	PU1RFLC00	PU1RFLC01	PU1RFLC02	PU1RFLC03
PUQRFLC04	PUQRFLC05	PUQRFLC06	PUQRFLC07		

POSITION OF WORD
FOR 1B F-LEVEL LAYOUT



Figure 1 - F-Level Layout

ANALYZE PFLR F-LEVEL INTERRUPT, IOP FRAME (SD-5A052-01/02)
EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)

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TABLE A		
I O U S	I O M P	VERTICAL LOCATION
0	0	62
	1	50
1	0	32
	1	20
2	0	62
	1	54
3	0	32
	1	24
4	0	62
	1	50
5	0	32
	1	20
6	0	62
	1	50
7	0	32
	1	20

TABLE B			
IOMP 1			
GCP BIT	SUSPECT PACK		
	TYPE	HORIZONTAL LOCATION	COMMENTS
10	UN60	056	—
	*(PC20)	108	These RC packs are not listed in order of fault probability
	*(PC21)	100	
	*(PC22)	092	
	*(PC23)	084	
	*(PC30)	048	
	*(PC31)	040	
	*(PC32)	032	
*(PC33)	024		
14	FG87	28	At IOMP 0 vertical location
	FG22	26	
15	FG20	22	
	FG22	26	
17	FG87	28	
	FG22	26	
18,19	FG86	31	
	FG87	28	
	FG85	33	
20	FG22	26	
21	FG22	26	
	FG85	33	
* TN75, TN75B, TN75C, or TN82B (office dependent)			

TABLE C		
IOMP 0		
GCP BIT	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
8,9	FG41	24
	FG87	28
10,11	FG20	22
	FG86	31
13,14	FG87	28
	FG22	26
15	FG20	22
	FG22	26
17	FG87	28
	FG22	26
18,19	FG86	31
	FG87	28
	FG85	33
20	FG22	26
21	FG22	26
	FG85	33

**ANALYZE F-LEVEL PFLR INTERRUPT, IOP FRAME (SD-5A052-02)
EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)**

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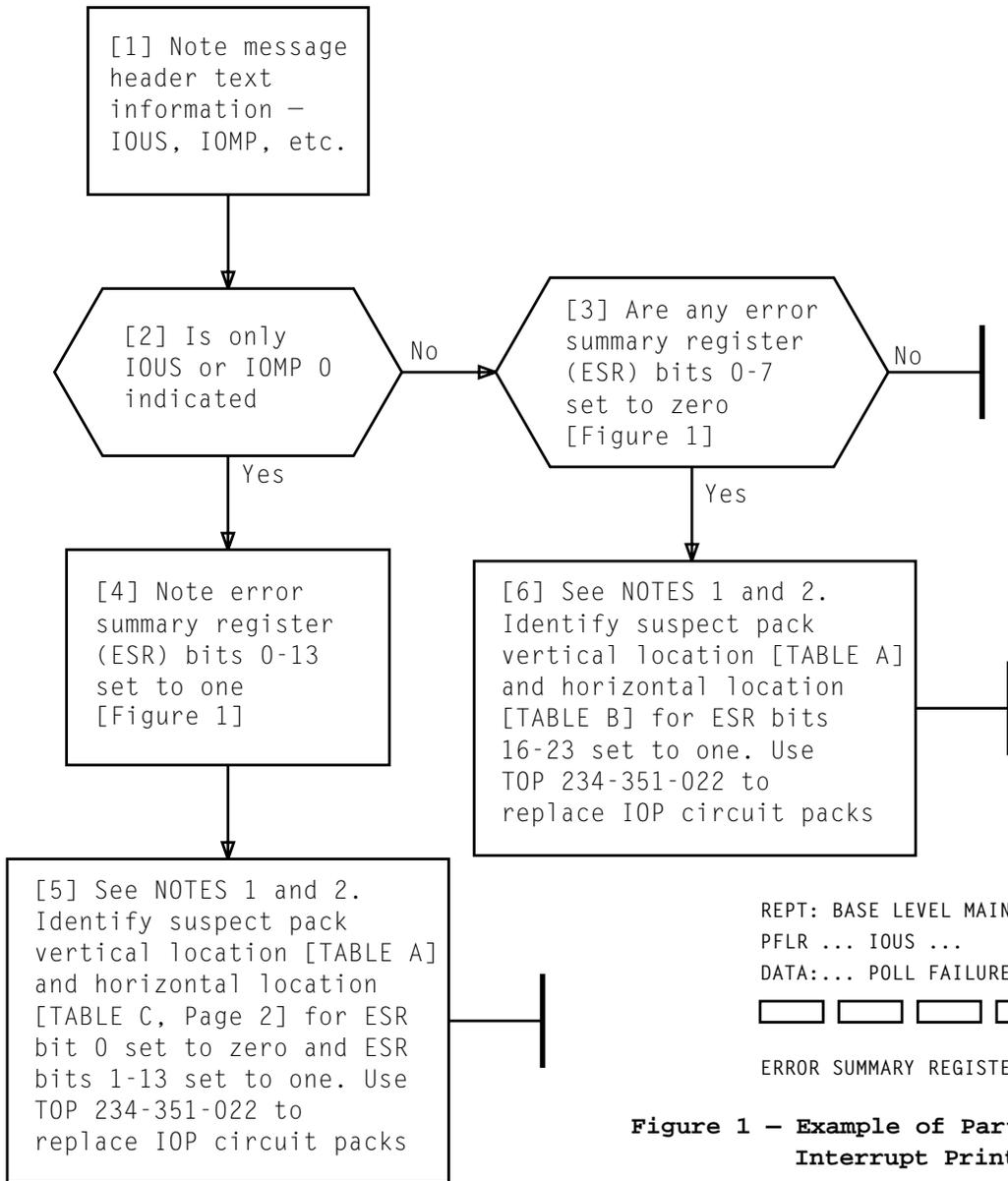


Figure 1 - Example of Partial Base Level Interrupt Printout

TABLE A		
IOUS	IOMP	VERTICAL LOCATION
0	0	62
	1	50
1	0	32
	1	20
2	0	62
	1	50
3	0	32
	1	20
4	0	62
	1	50
5	0	32
	1	20
6	0	62
	1	50
7	0	32
	1	20

TABLE B		
IOMP 1		
ESR BIT	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
16	*(PC20)	108
	UN60	056
17	*(PC21)	100
	UN60	056
18	*(PC22)	092
	UN60	056
19	*(PC23)	084
	UN60	056
20	*(PC30)	048
	UN60	056
21	*(PC31)	040
	UN60	056
22	*(PC32)	032
	UN60	056
23	*(PC33)	024
	UN60	056
* TN75, TN75B, TN75C or TN82B (office dependent)		

NOTES
 1. IOUS number on printout is same same as IOP number on power switch
 2. Users should be notified that channels are to be removed from service

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TABLE C					
IOMP 0					
ESR BIT		SUSPECT PACK			
POSITION	SET	TYPE	HORIZONTAL LOCATION	COMMENTS	
0	No	FG41	24	—	
1	Yes	FG41	24	Pin 5,6 bottom 400-ns square wave	
2	Yes	FG41	24	—	
3	Yes	FG21	18		
		FG41	24		
4	Yes	FG20	22		
		FG41	24		
		FG22	26		
5,6	Yes	FG41	24		
7	Yes	*	14		Line unit packs not listed in order of fault probability
		*	12P		
		*	11		
		*	09P		
		*	08		
		*	06P		
		*	05		
		*	03P		
8-13	Yes	FG86	31	—	
		FG87	28		
		FG22	26		
		FG23	35		
		FG85	33		

* FG19, FG26, or FG27

**ANALYZE BASE LEVEL PFLR POLL FAILURE, IOP FRAME
(SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)**

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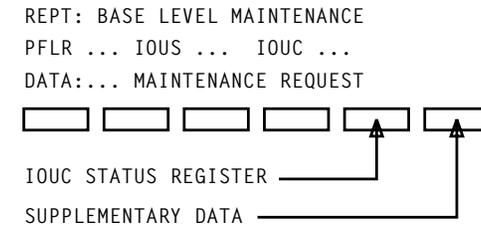
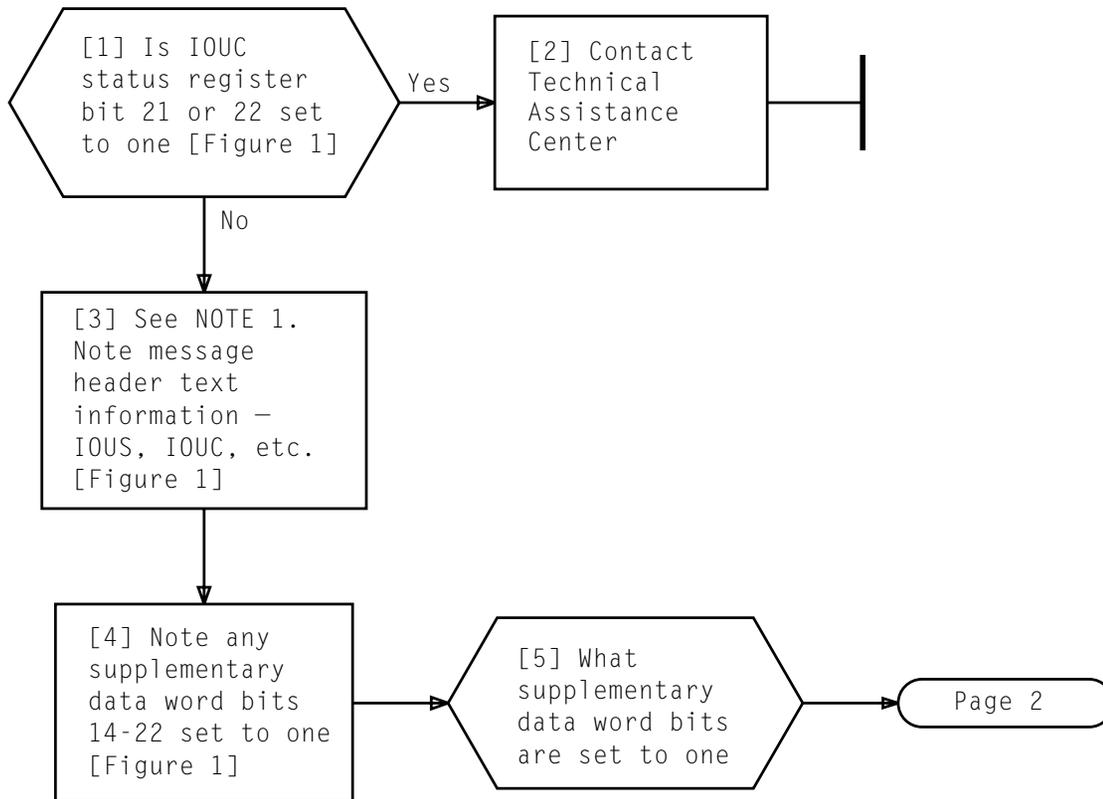
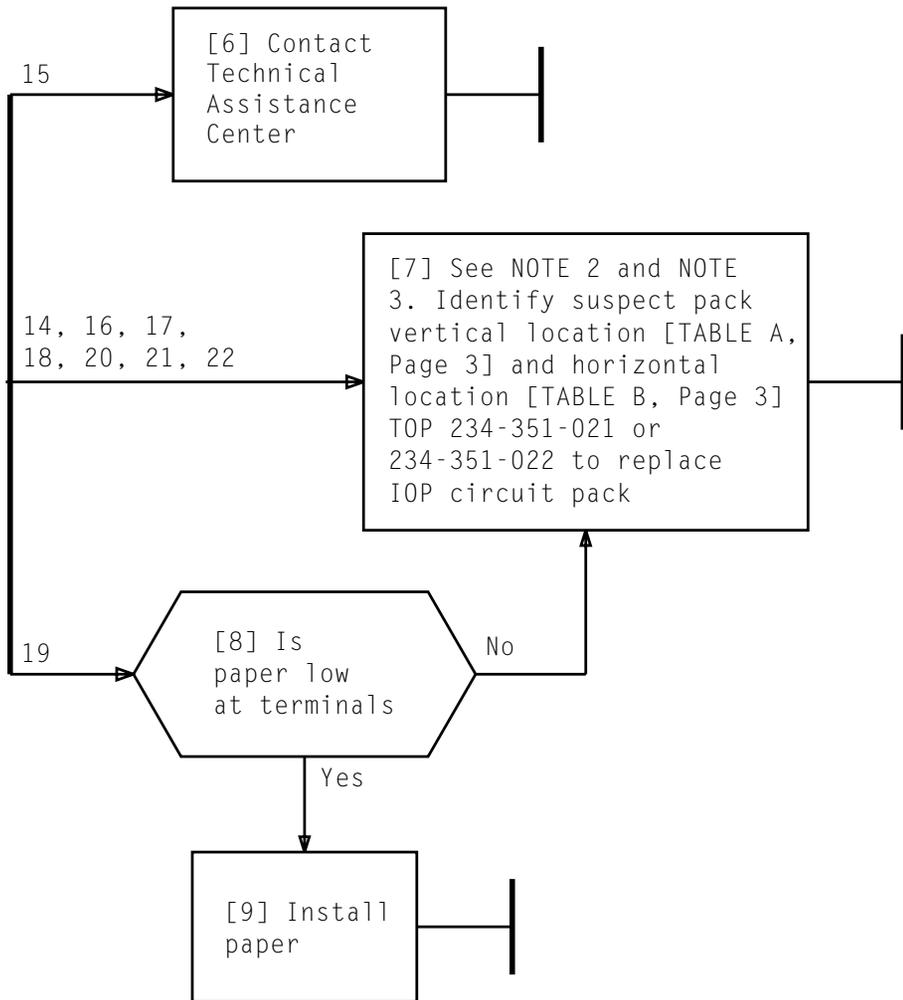


Figure 1 - Example of Partial Base Level Interrupt Printout

NOTE	
IOUS number on printout is same as IOP number on power switch	
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NOTES	
2. Users should be notified that channels are to be removed from service	
3. If interrupt recurs after replacing most suspect pack and the supplementary data word bit 17 and 18 are zero, suspect IOUC terminal equipment or terminal cabling. If 17 or 18 set to one, suspect packs using TABLES A and C, Page 3	
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**ANALYZE BASE LEVEL PFLR MTCE REQUEST, IOP FRAME
(SD-5A052-01/02) EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)**

TABLE A			
IOUS	IOUC	FRAME VERTICAL LOCATION	
		SD5A052-01	SD5A052-02
0	0-7	62	62
	8-15	50	50
1	0-7	38	32
	8-15	30	20
2	0-7	62	62
	8-15	54	54
3	0-7	38	32
	8-15	30	24
4	0-7	62	62
	8-15	54	54
5	0-7	38	32
	8-15	30	24
6	0-7	62	62
	8-15	54	54
7	0-7	38	32
	8-15	30	24

TABLE B		
IOUC	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
0, 8	*	14
1, 9	*	12P
2, 10	*	11
3, 11	*	09P
4, 12	*	08
5, 13	*	06P
6, 14	*	05
7, 15	*	03P
* FG19, FG26, or FG27		

TABLE C	
SUSPECT PACKS	
TYPE	HORIZONTAL LOCATION
FG20	22
FG41	24

**ANALYZE BASE LEVEL PFLR MTCE REQUEST, IOP FRAME
(SD-5A052-01/02) EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)**

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[1] Identify error summary register (ESR) bits 0-13 set to one [Figure 1]

[2] See NOTES 1 and 2. Identify suspect pack vertical location [TABLE A, Page 2] and horizontal location [TABLE B, Page 2] for ESR bit 0 set to zero and ESR bits 1-13 set to one. Use TOP 234-351-021 or 234-351-022 to replace IOP circuit packs.

```

REPT: BASE LEVEL MAINTENANCE
PFLR ... IOUS ...
DATA:... POLL FAILURE
[ ] [ ] [ ] [ ] [ ]
ERROR SUMMARY REGISTER ↑
  
```

Figure 1 - Example of Partial Base Level Interrupt Printout

NOTES

1. If IOUS only is indicated on printout, assume IOMP 0 for TABLE A use. IOUS number on printout is same as IOP number on power switch
2. Users should be notified that channels are to be removed from service

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**ANALYZE BASE LEVEL PFLR POLL FAILURE IOP FRAME
(SD-5A052-01/02) EQUIPPED WITH 1B GROWTH UNIT (SD-4C049-01)**

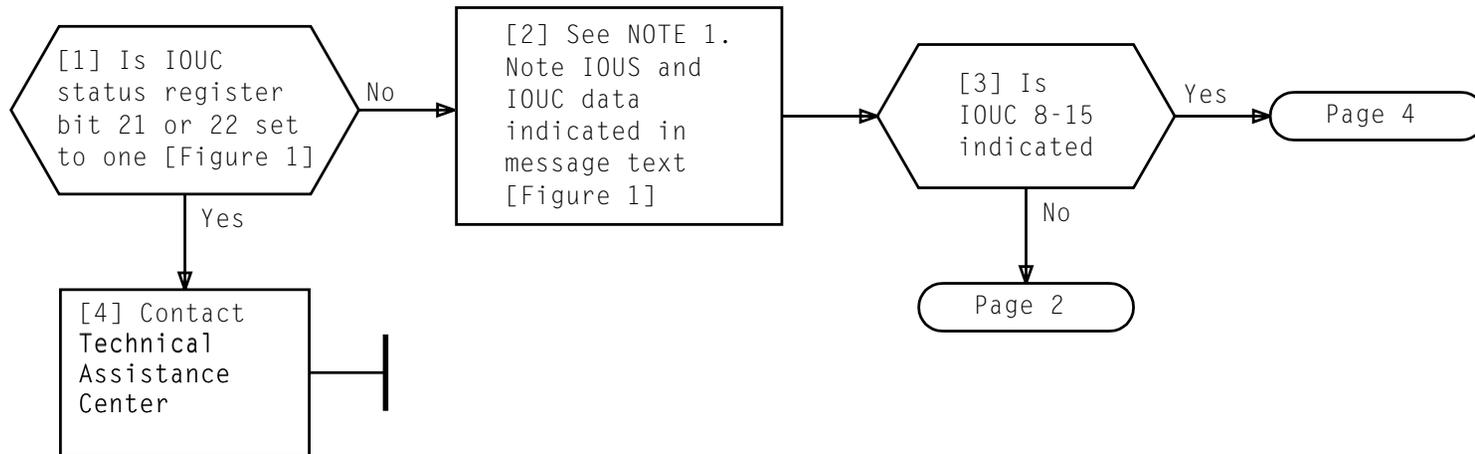
TABLE A			
I O U S	I O M P	FRAME VERTICAL LOCATION	
		SD5A052-01	SD5A052-02
0	0	62	62
	1	54	54
1	0	38	32
	1	30	24
2	0	62	62
	1	54	54
3	0	38	32
	1	30	24
4	0	62	62
	1	54	54
5	0	38	32
	1	30	24
6	0	62	62
	1	54	54
7	0	38	32
	1	30	24

TABLE B					
ESR BIT		SUSPECT PACK			
POSITION	SET	TYPE	HORIZONTAL LOCATION	COMMENTS	
0	No	FG41	24	-	
1	Yes	FG41	24	Pin 5, 6 bottom 400NS square wave	
2	Yes	FG41	24	-	
3	Yes	FG21	18		
		FG41	24		
4	Yes	FG20	22		
		FG41	24		
		FG22	26		
5,6	Yes	FG41	24		
7	Yes	*	14		Line unit packs not listed in order of fault probability
		*	12P		
		*	11		
		*	09P		
		*	08		
		*	06P		
		*	05		
8-13	Yes	FG43	31	May be FG86	
		FG44	28	May be FG87	
		FG22	26	May be FG85	
		FG23	35		
FG42	33				

* FG19, FG26, or FG27

**ANALYZE BASE LEVEL PFLR POLL FAILURE, IOP FRAME
(SD-5A052-01/02) EQUIPPED WITH 1B GROWTH UNIT (SD-4C049-01)**

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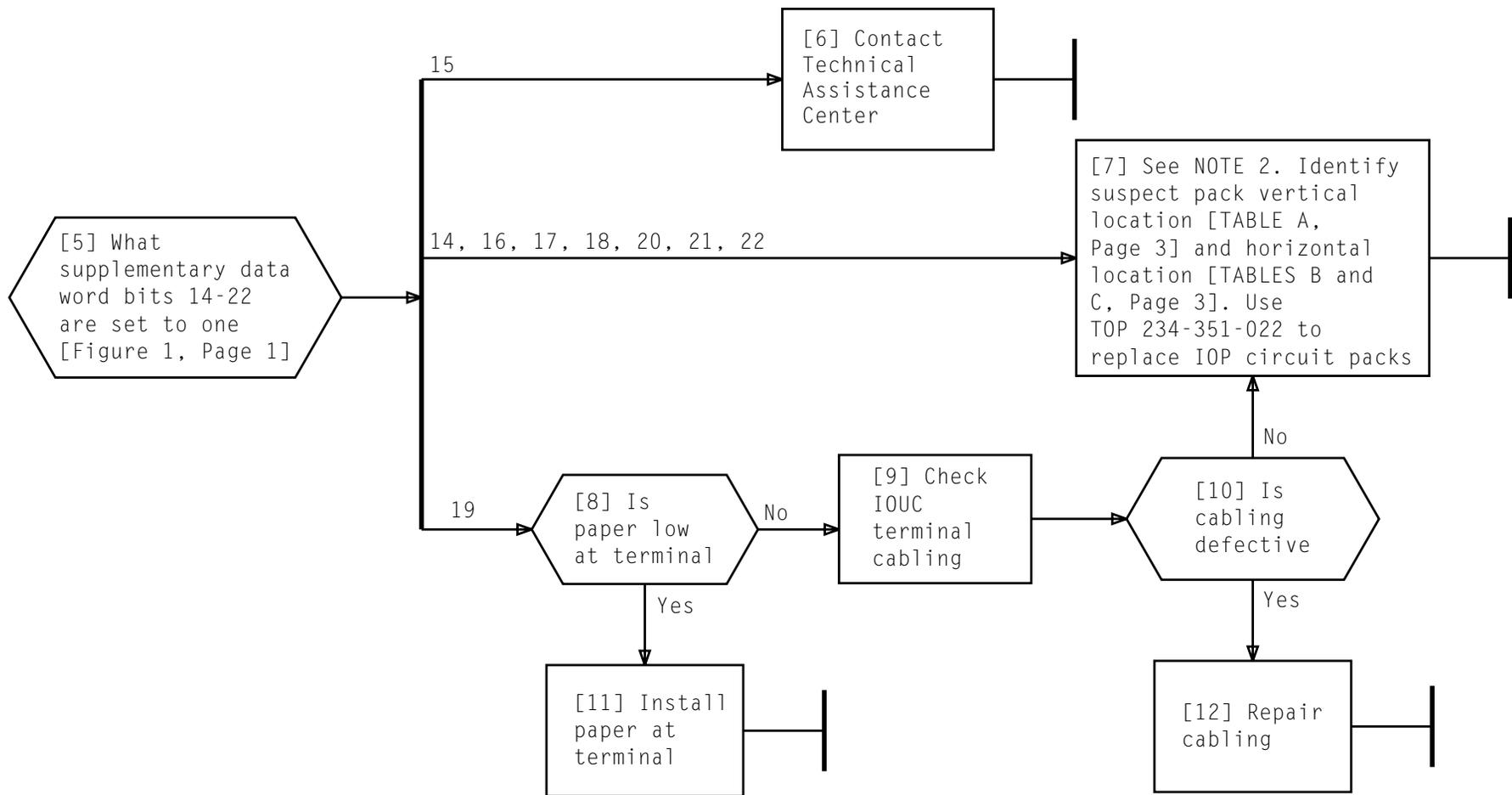
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REPT: BASE LEVEL MAINTENANCE
PFLR ... IOUS ... IOUC ...
DATA:... MAINTENANCE REQUEST
[ ] [ ] [ ] [ ] [ ] [ ]
IOUC STATUS REGISTER --> [ ]
SUPPLEMENTARY DATA --> [ ]
  
```

Figure 1 - Example of Partial Base Level Interrupt Printout

NOTE 1	
IOUS number on printout is same as IOP number on power switch	
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ANALYZE BASE LEVEL PFLR INTERRUPT MTCE REQUEST, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)



NOTE 2	
Notify users that channels are to be removed from service	
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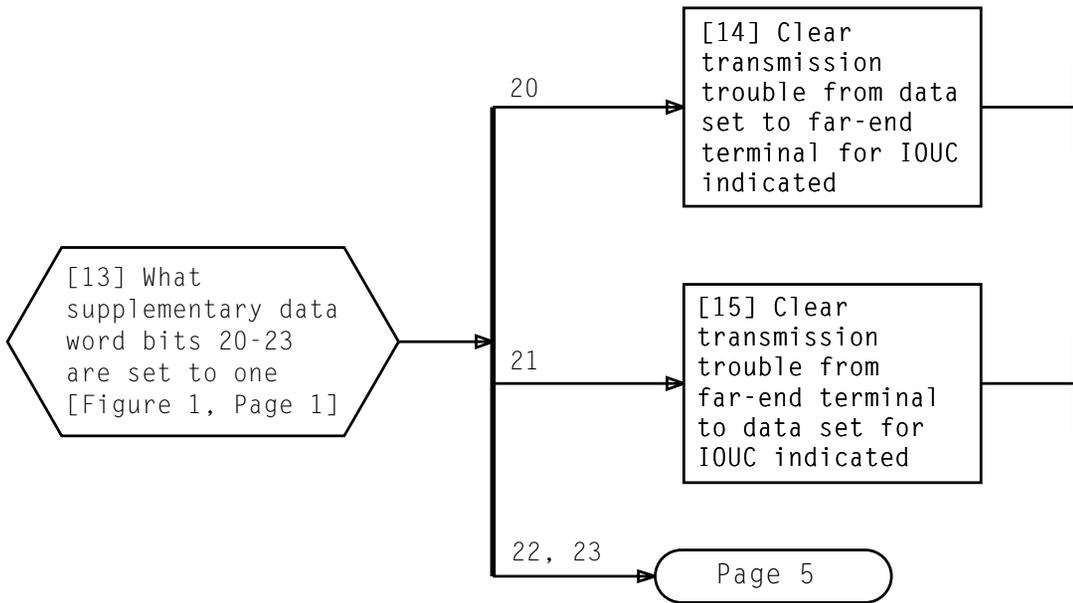
TABLE A		
I O U S	I O M P	VERTICAL LOCATION
0	0	62
	1	50
1	0	32
	1	20
2	0	62
	1	50
3	0	32
	1	20
4	0	62
	1	50
5	0	32
	1	20
6	0	62
	1	50
7	0	32
	1	20

TABLE B		
I O U C	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
0	*	14
1	*	12P
2	*	11
3	*	09P
4	*	08
5	*	06P
6	*	05
7	*	03P
* FG19, FG26, or FG27		

TABLE C	
SUSPECT PACKS	
TYPE	HORIZONTAL LOCATION
FG20	22
FG41	24

**ANALYZE BASE LEVEL PFLR INTERRUPT MTCE REQUEST, IOP FRAME
(SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)**

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ANALYZE BASE LEVEL PFLR INTERRUPT MTCE REQUEST, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)

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[16] See Note 2, Page 2 and Note 3. Identify suspect pack vertical location [TABLE D] and horizontal location [TABLE E]. Use Top 234-351-022 to replace IOP circuit packs.

TABLE D		
I O U S	I O M P	VERTICAL LOCATION
0	0	62
	1	50
1	0	32
	1	20
2	0	62
	1	50
3	0	32
	1	20
4	0	62
	1	50
5	0	32
	1	20
6	0	62
	1	50
7	0	32
	1	20

TABLE E		
I O U C	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
8	PC20	108
9	PC21	100
10	PC22	092
11	PC23	084
12	PC24	048
13	PC25	040
14	PC26	032
15	PC27	024

NOTE 3

If interrupt recurs after replacing most suspect pack and the supplementary data word bit 2 is set to one, Automatic calling unit (ACU) trouble should be cleared in data set frame of IOUC indicated. If bit 2 is not set to one, Data set associated with indicated IOUC should be checked. If data set is OK, transmission trouble between data set and frame far end should be cleared

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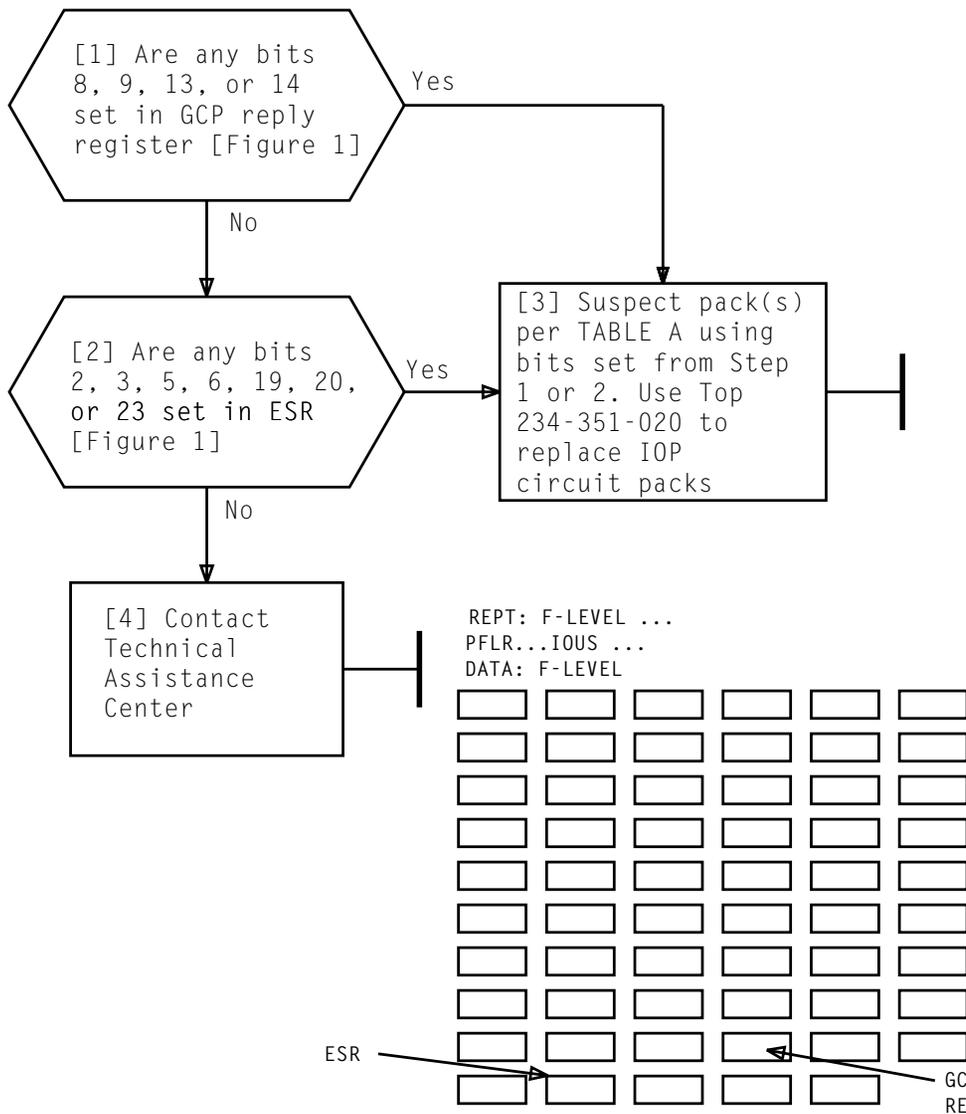


Figure 1 - Part of Interrupt Printout

TABLE A				
GCP BIT	ESR BIT	SUSPECT PACK	UNIT LOC. *	COMMENT
8	2	FA440	06-29	PARITY FAIL EVEN BITS
		FA444	06-22	
9	3	FA440	06-29	PARITY FAIL ODD BITS
		FA444	06-22	
13	5	FA440	06-29	MULTI K-CODE MATCH
		FA444	06-22	
14	6	FA441	06-19	INVALID INSTRUCTION
		FA444	06-22	
-	19	See TABLE B	See TABLE B	CHANNEL RESPONSE FAIL
-	20	FA448	06-27	CHANNEL BUFFER PARITY FAIL
		FA447	06-31	
		FA447	06-14	
-	23	FA444	06-22	CLOCK FAILURE

* ODD unit location starts at vertical 18.
Even unit locations starts at vertical 46.
Add unit vertical location given to suspect unit starting location to get frame vertical.

TABLE B		
CHANNEL MEMN*	SUSPECT PACK	UNIT LOC.
0	FA453	10-10
1	FA453	06-07
2	FA453	02-10
3	FA453	10-21
4	FA453	02-21
5	FA456	10-35
6	FA453	06-38
7	FA456	02-35

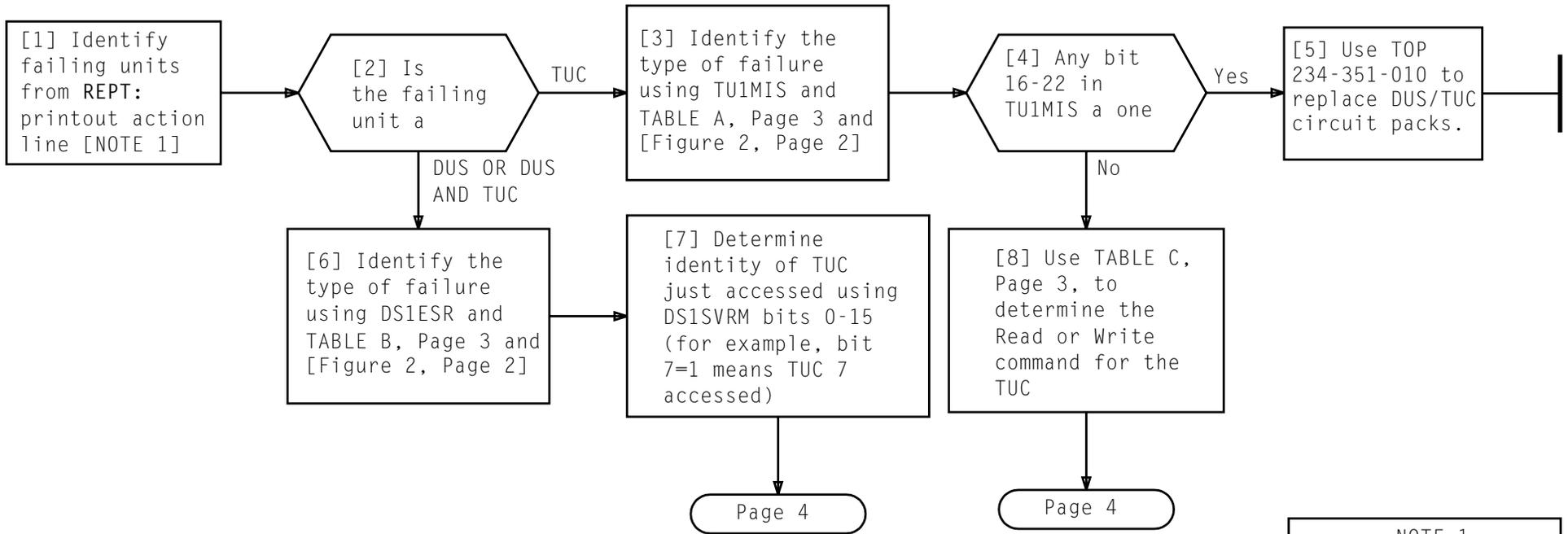
* See REPT: text phrase

ANALYZE PFLR F-LEVEL INTERRUPT OR BASE LEVEL POLL FAILURE, IOP FRAME (SD-5A021)

SUMMARY

This type of failure is due to either a CC read or write of an internal DUS location or a write of an internal TUC register location. When CC writes into an internal TUC location, the write data is looped back to the DUSOBR. When CC reads an internal TUC location, the TUC read data (for that read operation) is gated into the DUSOBR. In

order to verify data written into a TUC or to obtain data read from a TUC, CC must perform a read of the DUSOBR. Most often, the DUS-TUC communication portion of the CC-TUC read/write operation fails, causing the DUS to freeze. When this happens, the CC read of the DUSOBR to obtain TUC read or write data also fails because the DUS is frozen. This produces the D-Level interrupt.



DATA: D-LEVEL

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASD(H)	AC1ASD(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR

Figure 1 - Part of D-Level Printout

NOTE 1
ADDRESS where interrupt occurred is in AC1ASD. DUS/TUC address, being read or written, that caused the interrupt is in AC1SDA (STACK) [Figure 1]

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DATA: INTERNAL DUS REGISTERS AND TEST RESULTS

DS1OBR	DS1IBR	DS1OAR	DS1IRA	DS1SELREG	DS1SVRM
DS1OIRA	DS1MCR	DS1PCR	DS1ESR	GCPA	GCPR
DS1R_TFWRD	DS1R_TADDR	DS1R_TVCTR	DS1R_TRSLT	DS1R_XFRWD0	DS1R_SVR1
DS1R_TFWRDB	DS1R_TADDRB	DS1R_TVCTRB	DS1R_TRSLTB	DS1R_XFRWD1	DS1R_SVR2
DS1ROVSTAT+0	DS1RSTAT0+0	DS1RSTAT0+1	DS1RSTAT1+0	DS1RSTAT1+1	DS1R_SVR3
DC1RSTAT0+0	DC1RSTAT0+1	DC1RSTAT0+2	DC1RSTAT0+3	DC1RSTAT0+4	DC1RSTAT0+5
DC1RSTAT0+6	DC1RSTAT0+7	DC1RSTAT0+8	DC1RSTAT0+9	DC1RSTAT0+10	DC1RSTAT0+11
DC1RSTAT0+12	DC1RSTAT0+13	DC1RSTAT0+14	DC1RSTAT0+15	AU1RSTAT+12	AU1RSTAT+13
DC1RSTAT0+0*	DC1RSTAT0+1*	DC1RSTAT0+2*	DC1RSTAT0+3*	AU1STAT0+4*	AU1STAT0+5*
DC1RSTAT0+6*	DC1RSTAT0+7*	DC1RSTAT0+8*	DC1RSTAT0+9*	DC1RSTAT0+10*	DC1RSTAT0+11*
DC1RSTAT0+12*	DC1RSTAT0+13*	DC1RSTAT0+14*	DC1RSTAT0+15*	AU1RSTAT+12*	AU1RSTAT+13*
aaaaaaaa	bbbbbbbb	cccccccc	dddddddd	eeeeeeee	ffffffff
gggggggg	hhhhhhh	iiiiiiii	jjjjjjjj	kkkkkkkk	mmmmmmm
nnnnnnnn	pppppppp	qqqqqqqq	rrrrrrrr	XR	XR
TU1AREG	TU1DR	TU1CCREG	TU1DBR	TU1COM	TU1PCREG
TU1MR	TU1CBREG	ssssssss	tttttttt	TU1MIS	TU1OIS
TU1TTS	uuuuuuuu	TU1CIBG	TU1HLSB		

WORD	BITS 23-12	BITS 11-0	WORD	BITS 23-12	BITS 11-0
aaaaaaaa	DC1RSTAT2+0	DC1RSTAT1+0	jjjjjjjj	DC1RSTAT2+9	DC1RSTAT1+9
bbbbbbbb	↓ +1	↓ +1	kkkkkkkk	↓ +10	↓ +10
cccccccc	↓ +2	↓ +2	mmmmmmm	↓ +11	↓ +11
ddddddd	↓ +3	↓ +3	nnnnnnnn	↓ +12	↓ +12
eeeeeee	↓ +4	↓ +4	pppppppp	↓ +13	↓ +13
fffffff	↓ +5	↓ +5	qqqqqqqq	↓ +14	↓ +14
ggggggg	↓ +6	↓ +6	rrrrrrrr	↓ +15	↓ +15
hhhhhhh	↓ +7	↓ +7	ssssssss	TU1ECREG	TU1WDREG
iiiiiii	↓ +8	↓ +8	tttttttt	TU1RCRCREG	TU1WCRCREG

* NOT ALWAYS AVAILABLE FOR PRINT				BITS 23-18	BITS 17-0
			uuuuuuuu	TU1SRR	TU1LTCR

Figure 2 - Part of D-Level Printout

TABLE A - TULMIS	
BIT SET TO ONE	TYPE OF FAILURE AS SEEN BY TUC
0	CLOCK SYNC FAILURE
1	ADDRESS PARITY FAILURE
2	R/W REGISTER SELECT FAILURE
3	DATA PARITY FAILURE
8	INCREMENT PARITY FAILURE
9	SELF-CHECK FAILURE
10	DATA XFER PARITY FAILURE
11	BUFFER PARITY FAILURE ON WRITE
12	AUTONOMOUS REGISTER SELECT FAILURE
13	TIME OUT
14	LATE DATA
15	DATA OVERWRITE
16	ERASE-WRITE HEAD CURRENT FAILURE
17	CAPSTAN MOTION ABNORMAL
18	DC POWER FAILURE
19	AC POWER FAILURE
20	TAPE ARMS ABNORMAL
21	SERVO LAMP FAILURE
22	TEMPERATURE ABNORMAL

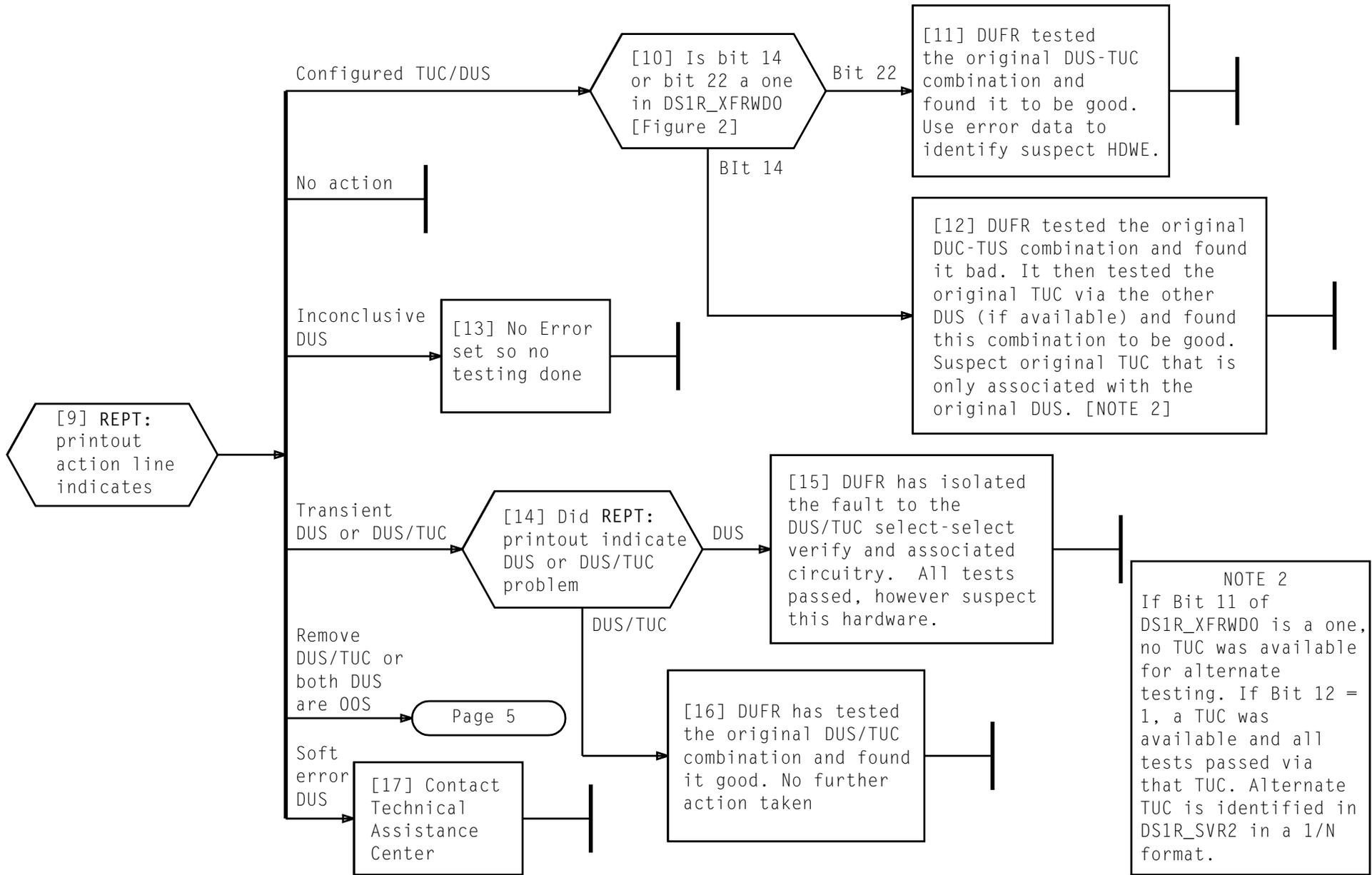
TABLE B - DS1ESR*			
BIT SET TO ONE	TYPE OF FAILURE AS SEEN BY DUS	LEAD NAME	FS†
0	DUC SEQUENCER ERROR	DUCSER	3/1
1	CS/PS SEQUENCER ERROR	SSQER	3/1
6	MODE ERROR READ ONLY	ME0	2/3
9	IBR PARITY FAIL CS/PS	PE0	2/3
10	CS/PS ASW ERROR	SASWE	3/1
12	DUC REPLY BUS PARITY FAILURE	AUCRPER	3/1
13	DUC REPLY BUS ASW FAILURE	AUCBASWO	3/1
14	DUC CONTROL BUS PARITY FAILURE	AUCCPER	3/1
18	DUC SELECT VERIFY FAILURE	AUCSVER	3/1
19	DUC MI REPLY	AUCBMI	3/1

* DS1ESR = 00070000 indicates a complete loss of communication to the TUC. Check TU1HLSB [Figure 1] bits 1 and 2 for possible cause (TBL FF SET or improper bus routing).

† SD5A024

TABLE C		
TULCOM	FUNCTION	REGISTER RESULT
BIT 10 = 1	READ	DUS OUTPUT ADDRESS REGISTER (DS1OAR) SHOULD EQUAL THE TUC ADDRESS REGISTER (TU1AREG) AFTER READING THE TUC ADDRESS REGISTER. ALSO, THE DUS OUTPUT BUFFER REGISTER (DS1OBA) SHOULD EQUAL THE TUC DATA REGISTER (TU1DR) AFTER READING THE TUC DATA REGISTER.
BIT 2 = 1	WRITE	DUS INPUT BUFFER REGISTER (DS1IBR) SHOULD EQUAL THE TUC DATA REGISTER (TU1DR) AFTER WRITING THE TUC DATA REGISTER.

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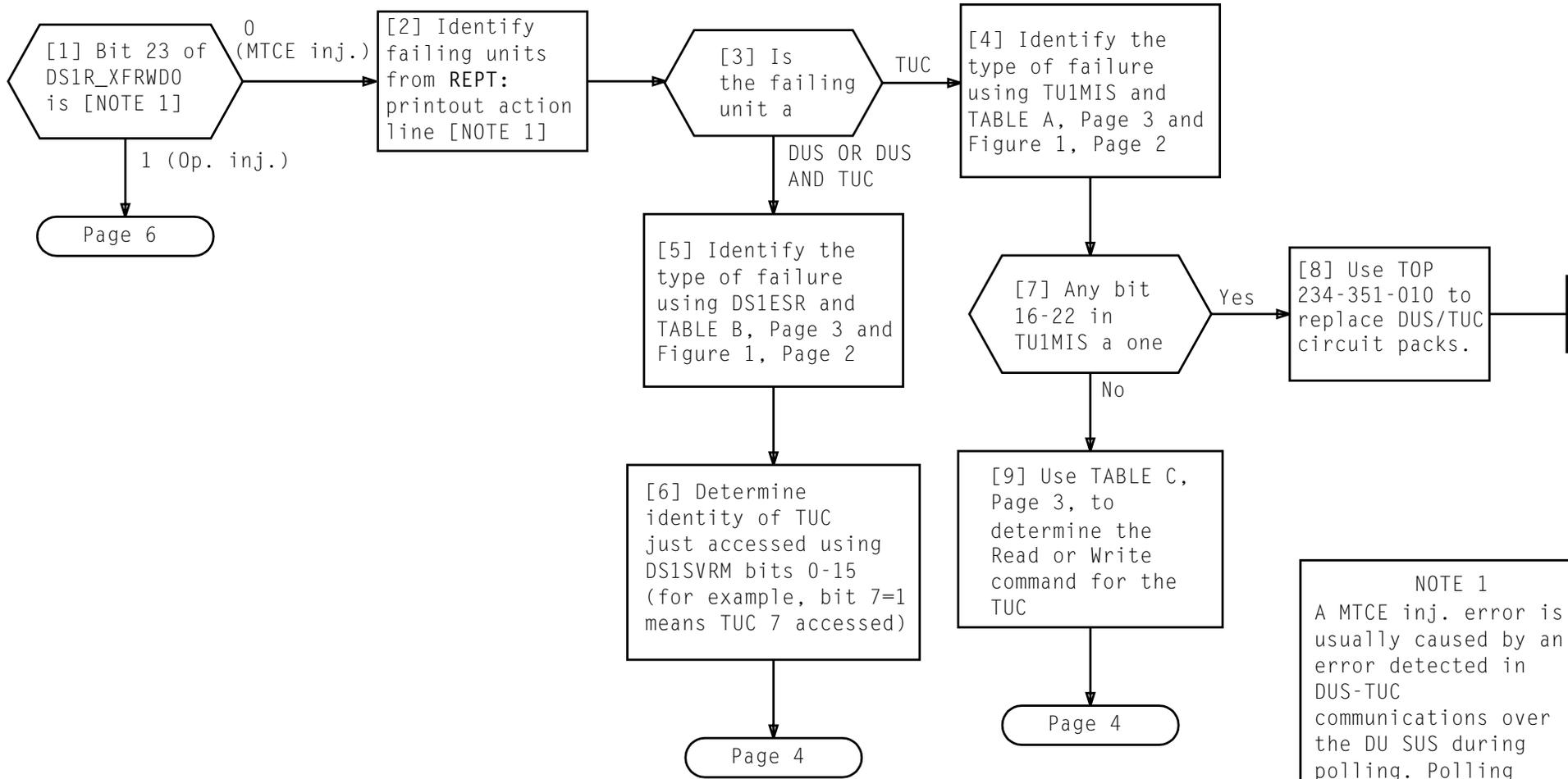


NOTE 2
 If Bit 11 of DS1R_XFRWDO is a one, no TUC was available for alternate testing. If Bit 12 = 1, a TUC was available and all tests passed via that TUC. Alternate TUC is identified in DS1R_SVR2 in a 1/N format.

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[18] Identify suspect unit using DS1R_XFRWDO [Figure 2, Page 2] and TABLE D

TABLE D - DS1R_XFRWDO	
BIT SET TO ONE	SUSPECT UNIT/CONDITION
0	SUSPECT DUS
1	SUSPECT TUC FOR DUS REMOVAL
2	BOTH DUS SUSPECTED FOR TUC REMOVAL
4	ONE DUS THEN THE OTHER DUS FAILED SAME DUFR TEST
5	ONE DUS THEN THE OTHER DUS FAILED A DIFFERENT DUFR TEST
6	TUC CANNOT COMMUNICATE VIA THE OTHER DUS
9	SUSPECT TUC. OTHER DUS IS AVAILABLE BUT TUC FAILS DUFR
10	SUSPECT DUS. FAILED DUFR TEST VIA A TUC
13	SUSPECT DUS. FAILED VIA TWO DIFFERENT DUCs
15	SUSPECT TUC. FAILS DUFR TEST VIA DUS TO TUC
17	SUSPECT DUS. TEST PASS VIA EACH TUC
19	SUSPECT TUC. TEST PASS VIA EACH DUS
20	SUSPECT TUC. CANNOT SWITCH TO OTHER DUS BECAUSE OF PREVIOUS TROUBLE - RECORD
21	SUSPECT TUC. OTHER DUS NOT AVAILABLE



NOTE 1
 A MTCE inj. error is usually caused by an error detected in DUS-TUC communications over the DU SUS during polling. Polling involves reading the TUC address register and/or writing the TUC data register. An operational interject indicates the failure is internal to the TUC.

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DATA: INTERNAL DUS REGISTERS AND TEST RESULTS

DS1OBR	DS1IBR	DS1OAR	DS1IRA	DS1SELREG	DS1SVRM
DS1OIRA	DS1MCR	DS1PCR	DS1ESR	GCPA	GCPR
DS1R_TFWRD	DS1R_TADDR	DS1R_TVCTR	DS1R_TRSLT	DS1R_XFRWD0	DS1R_SVR1
DS1R_TFWRDB	DS1R_TADDRB	DS1R_TVCTRB	DS1R_TRSLTB	DS1R_XFRWD1	DS1R_SVR2
DS1ROVSTAT+0	DS1RSTAT0+0	DS1RSTAT0+1	DS1RSTAT1+0	DS1RSTAT1+1	DS1R_SVR3
DC1RSTAT0+0	DC1RSTAT0+1	DC1RSTAT0+2	DC1RSTAT0+3	DC1RSTAT0+4	DC1RSTAT0+5
DC1RSTAT0+6	DC1RSTAT0+7	DC1RSTAT0+8	DC1RSTAT0+9	DC1RSTAT0+10	DC1RSTAT0+11
DC1RSTAT0+12	DC1RSTAT0+13	DC1RSTAT0+14	DC1RSTAT0+15	AU1RSTAT+12	AU1RSTAT+13
DC1RSTAT0+0*	DC1RSTAT0+1*	DC1RSTAT0+2*	DC1RSTAT0+3*	AU1STAT0+4*	AU1STAT0+5*
DC1RSTAT0+6*	DC1RSTAT0+7*	DC1RSTAT0+8*	DC1RSTAT0+9*	DC1RSTAT0+10*	DC1RSTAT0+11*
DC1RSTAT0+12*	DC1RSTAT0+13*	DC1RSTAT0+14*	DC1RSTAT0+15*	AU1RSTAT+12*	AU1RSTAT+13*
aaaaaaaa	bbbbbbbb	cccccccc	dddddddd	eeeeeeee	ffffffff
gggggggg	hhhhhhh	iiiiiii	jjjjjjj	kkkkkkk	mmmmmmm
nnnnnnnn	ppppppp	qqqqqqq	rrrrrrr	XR	XR
TU1AREG	TU1DR	TU1CCREG	TU1DBR	TU1COM	TU1PCREG
TU1MR	TU1CBREG	sssssss	ttttttt	TU1MIS	TU1OIS
TU1TTS	uuuuuuu	TU1CIBG	TU1HLSB		

WORD	BITS 23-12	BITS 11-0	WORD	BITS 23-12	BITS 11-0
aaaaaaaa	DC1RSTAT2+0	DC1RSTAT1+0	jjjjjjj	DC1RSTAT2+9	DC1RSTAT1+9
bbbbbbb	↓ +1	↓ +1	kkkkkkk	↓ +10	↓ +10
ccccccc	↓ +2	↓ +2	mmmmmmm	↓ +11	↓ +11
ddddddd	↓ +3	↓ +3	nnnnnnn	↓ +12	↓ +12
eeeeeee	↓ +4	↓ +4	ppppppp	↓ +13	↓ +13
fffffff	↓ +5	↓ +5	qqqqqqq	↓ +14	↓ +14
ggggggg	↓ +6	↓ +6	rrrrrrr	↓ +15	↓ +15
hhhhhhh	↓ +7	↓ +7	sssssss	TU1ECREG	TU1WDREG
iiiiiii	↓ +8	↓ +8	ttttttt	TU1RCRCREG	TU1WCRCREG

* NOT ALWAYS AVAILABLE FOR PRINT					
	uuuuuuu			BITS 23-18	BITS 17-0
				TU1SRR	TU1LTCR

Figure 1 - Part of Interject Printout

TABLE A - TULMIS	
BIT SET TO ONE	TYPE OF FAILURE AS SEEN BY TUC
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3	DATA PARITY FAILURE
8	INCREMENT PARITY FAILURE
9	SELF-CHECK FAILURE
10	DATA XFER PARITY FAILURE
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16	ERASE-WRITE HEAD CURRENT FAILURE
17	CAPSTAN MOTION ABNORMAL
18	DC POWER FAILURE
19	AC POWER FAILURE
20	TAPE ARMS ABNORMAL
21	SERVO LAMP FAILURE
22	TEMPERATURE ABNORMAL

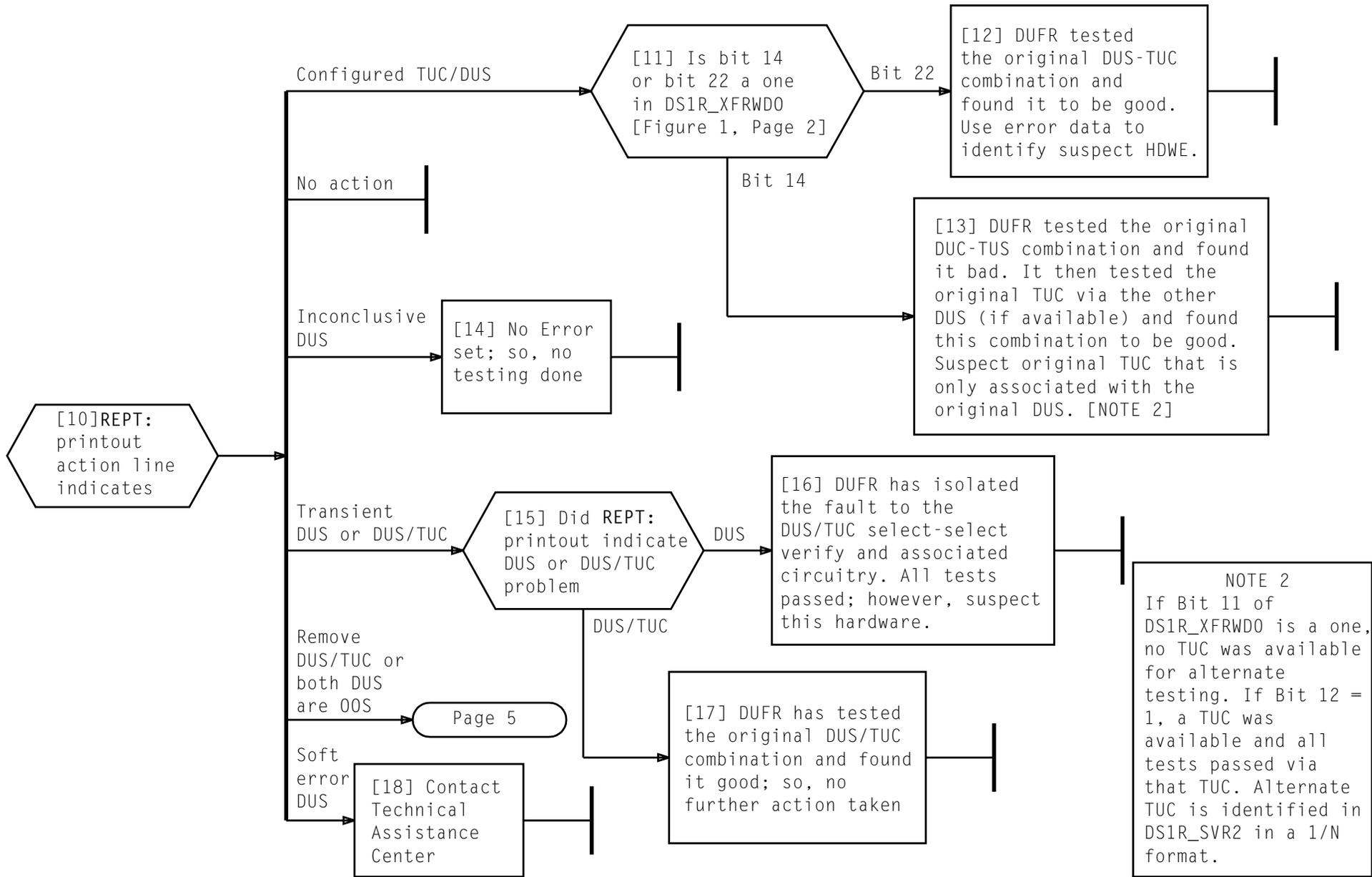
TABLE B - DS1ESR*			
BIT SET TO ONE	TYPE OF FAILURE AS SEEN BY DUS	LEAD NAME	FS†
0	DUC SEQUENCER ERROR	DUCSER	3/1
1	CS/PS SEQUENCER ERROR	SSQER	3/1
6	MODE ERROR READ ONLY	MEO	2/3
9	IBR PARITY FAIL CS/PS	PEO	2/3
10	CS/PS ASW ERROR	SASWE	3/1
12	DUC REPLY BUS PARITY FAILURE	AUCRPER	3/1
13	DUC REPLY BUS ASW FAILURE	AUCBASWO	3/1
14	DUC CONTROL BUS PARITY FAILURE	AUCCPER	3/1
18	DUC SELECT VERIFY FAILURE	AUCSVER	3/1
19	DUC MI REPLY	AUCBMI	3/1

* DS1ESR = 00070000 indicates a complete loss of communication to the TUC. Check TU1HLSB [Figure 1] bits 1 and 2 for possible cause (TBL FF SET or improper bus routing).

† SD5A024

TABLE C		
TULCOM	FUNCTION	REGISTER RESULT
BIT 10 = 1	READ	DUS OUTPUT ADDRESS REGISTER (DS1OAR) SHOULD EQUAL THE TUC ADDRESS REGISTER (TU1AREG) AFTER READING THE TUC ADDRESS REGISTER. ALSO, THE DUS OUTPUT BUFFER REGISTER (DS1OBA) SHOULD EQUAL THE TUC DATA REGISTER (TU1DR) AFTER READING THE TUC DATA REGISTER.
BIT 2 = 1	WRITE	DUS INPUT BUFFER REGISTER (DS1IBR) SHOULD EQUAL THE TUC DATA REGISTER (TU1DR) AFTER WRITING THE TUC DATA REGISTER.

ANALYZE DUS/TUC INTERJECT

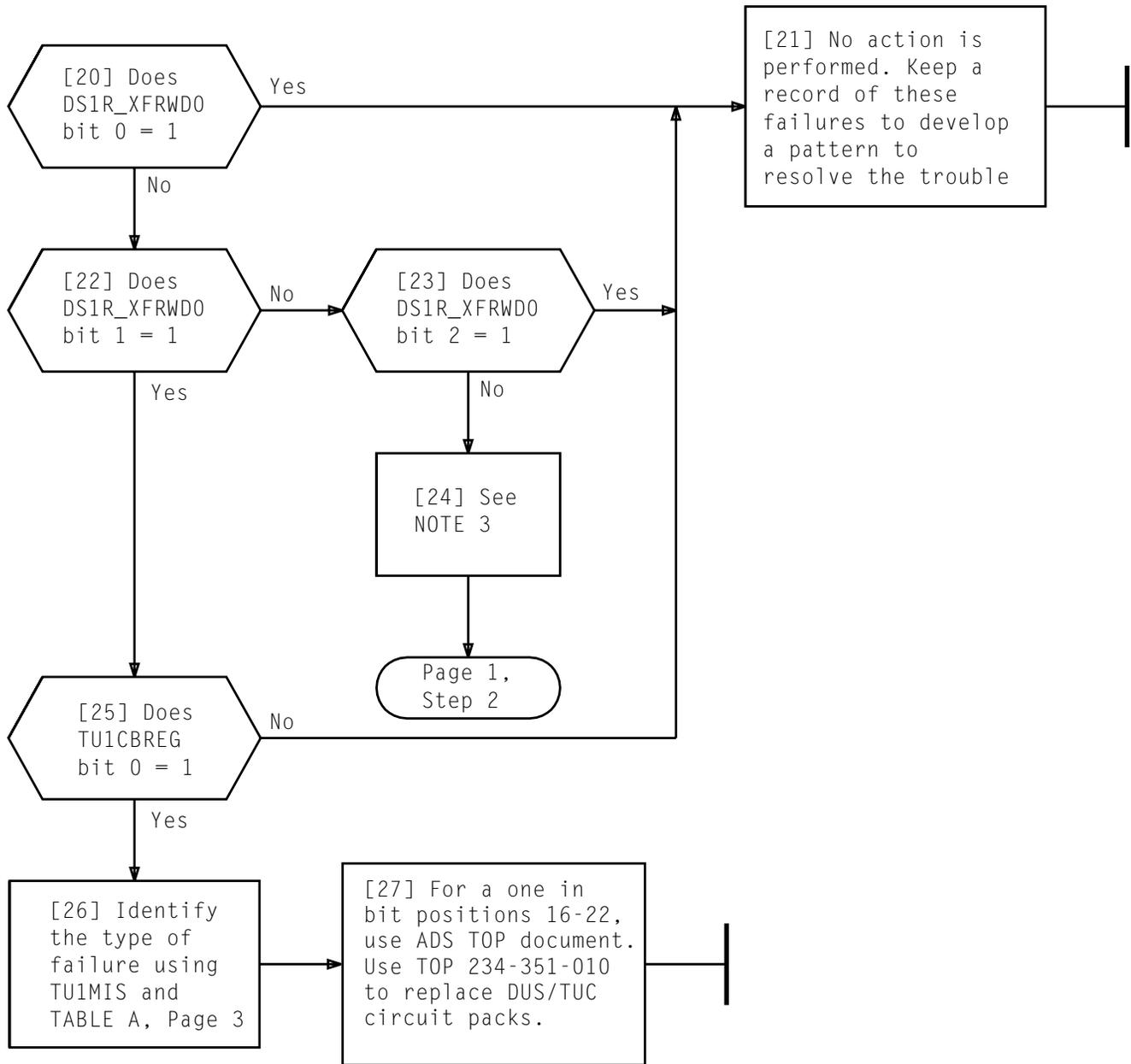


NOTE 2
If Bit 11 of DS1R_XFRWDO is a one, no TUC was available for alternate testing. If Bit 12 = 1, a TUC was available and all tests passed via that TUC. Alternate TUC is identified in DS1R_SVR2 in a 1/N format.

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[19] Identify suspect unit using DS1R_XFRWDO [Figure 2, Page 2] and TABLE D

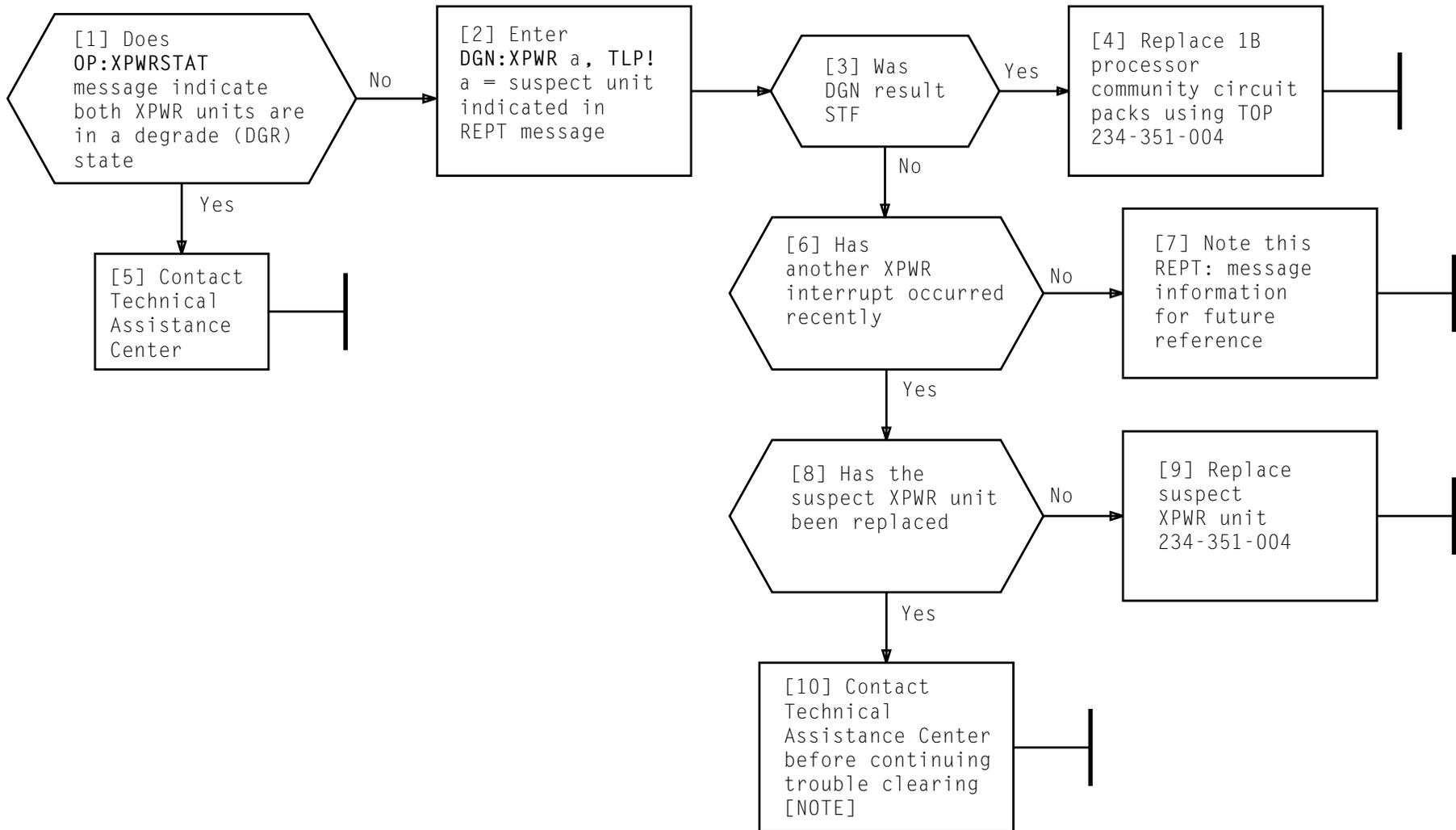
TABLE D - DS1R_XFRWDO	
BIT SET TO ONE	SUSPECT UNIT/CONDITION
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5	ONE DUS THEN THE OTHER DUS FAILED A DIFFERENT DUFR TEST
6	TUC CANNOT COMMUNICATE VIA THE OTHER DUS
9	SUSPECT TUC. OTHER DUS IS AVAILABLE BUT TUC FAILS DUFR
10	SUSPECT DUS. FAILED DUFR TEST VIA A TUC
13	SUSPECT DUS. FAILED VIA TWO DIFFERENT DUCs
15	SUSPECT TUC. FAILS DUFR TEST VIA DUS TO TUC
17	SUSPECT DUS. TEST PASS VIA EACH TUC
19	SUSPECT TUC. TEST PASS VIA EACH DUS
20	SUSPECT TUC. CANNOT SWITCH TO OTHER DUS BECAUSE OF PREVIOUS TROUBLE - RECORD
21	SUSPECT TUC. OTHER DUS NOT AVAILABLE



NOTE 3
 The Data Unit Administration Program has detected:

- a) an unsuccessful job completion
- b) some other non-interruptable operational malfunction
- c) a hardware consistency check failure
- d) a hardware/software consistency check failure

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NOTE	
Interrupt data and test equipment should be used to check voltages.	
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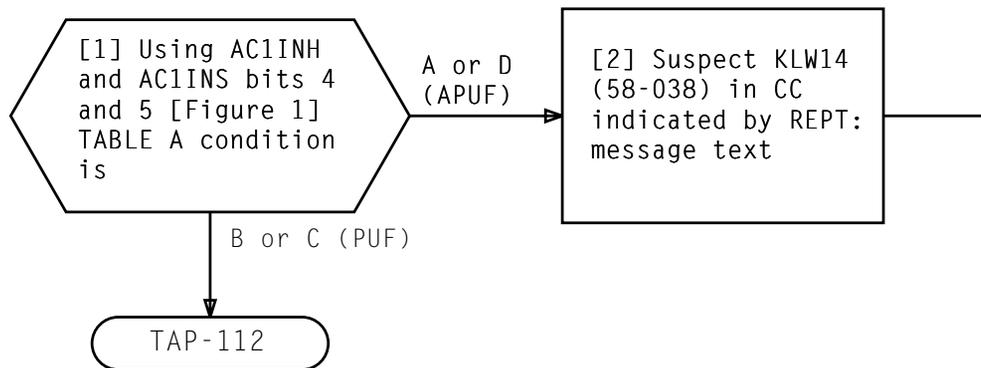
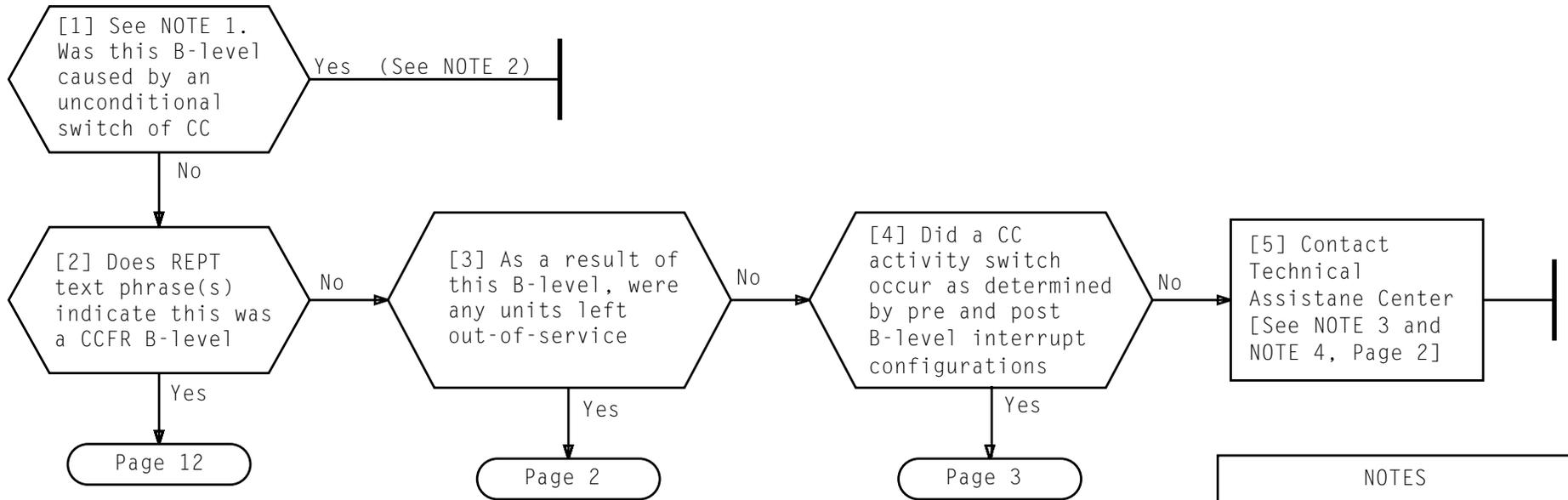


TABLE A				
AC1INH		AC1INS		CONDITION
BIT 5 (IPUFS)	BIT 4 (IAPUFS)	BIT 5 (PUFS)	BIT 4 (APUFS)	
DC	0	0	1	A
0	0	1	DC	B
0	1	1	DC	C
1	0	DC	1	D
DC = Don't Care				

F-LEVEL					
AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASF(H)	AC1ASF(L)
AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES
AC1ILA	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR
AC1SCTR	ST1INS	ELIT	AC1LPI	AC1ER	AC1PRM
AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1LR	ST1PRM
AC1PSQ	AC1ULR	AC1PES	ST1PES	ST1ER	ST1RP1
ST1PRL	ST1PSC	AC1RPO	AC1RP1	ST1RPO	PU1RFLC03
ST1CSC	ST1INH	PU1RFLC00	PU1RFLC01	PU1RFLC02	
PU1RFLC04	PU1RFLC05	PU1RFLC06	PU1RFLC07		

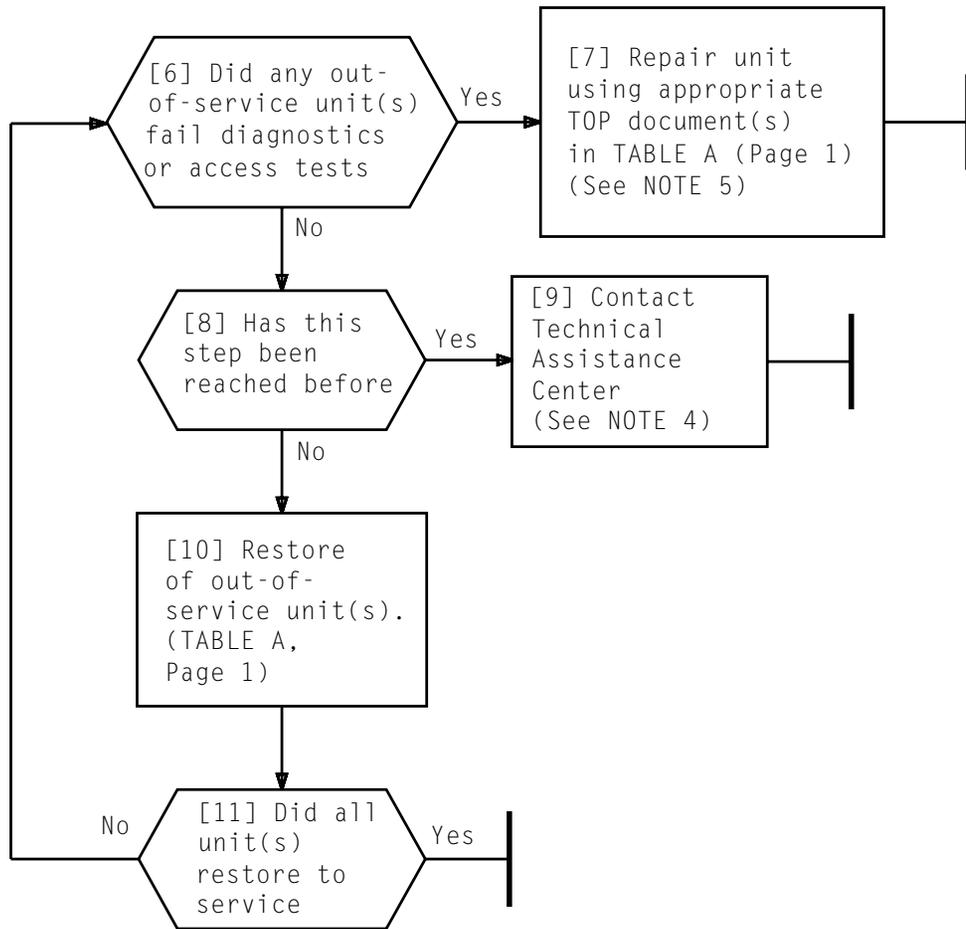
Figure 1 - F-Level Data



NOTES

1. TAD-100 is a good source of general interrupt analysis data.
2. A manual unconditional switch of CC should not be used without good cause.
3. Using any register with an address (J, LPI, stack, etc), the location of the program at the time of the interruption should be determined to determine what process was being done at that time. PCR bits set and PC state should be noted.

TABLE A			
UNIT	DIAGNOSTIC MESSAGE	RESTORE MESSAGE	TOP DOCUMENT
CC	DGN:CC a:TLP!	RST:CC a:TLP!	234-351-004
PS	DGN:PS a:TLP!	RST:PS a:TLP!	234-351-004
PSB	DGN:PSB a:TLP!	RST:PSB a:TLP!	234-351-004
CS	DGN:CS a:TLP!	RST:CS a:TLP!	234-351-004
CSB	DGN:CSB a:TLP!	RST:CSB a:TLP!	234-351-004
AUB	DGN:AUB a!	RST:AUB a!	234-351-010
IFB	DGN:IFB a:TLP!	RST:IFB a:TLP!	234-351-004
AUI	DGN:AUI a:TLP!	RST:AUI a:TLP!	234-351-004
API	DGN:API a:TLP!	RST:API a:TLP!	234-351-016
MUP	DGN:MUP a:TLP!	RST:MUP a:TLP!	234-351-004



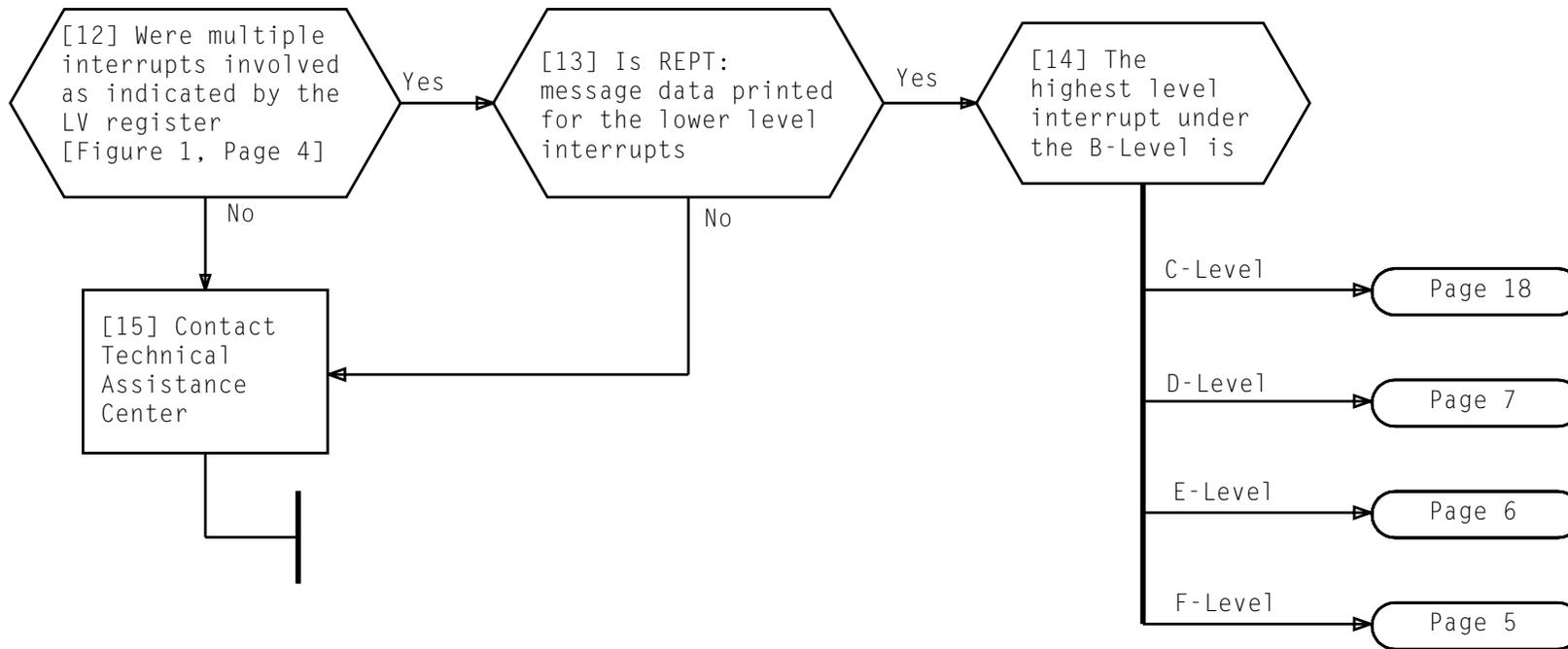
NOTES

4. The following should be done to prepare for technical assistance;

- Determine processor unit status prior to B-level(s), for example, CS status, PS status, etc.
- Ensure message record is logged.
- Output ERLI [Library Program LGXxKG1 (where xx = generic)]. Any processor related interrupt should be output (OP:ERAPDATA:MFNUM).
- Determine out-of-service status after B-Level(s).
- Provide printout data (CS status, etc.) that allows determining pre and post PCRV configuration (M-codes, bus activity, etc.)

5. Whether PCRV should have resulted from failure of unit(s) should be assessed.

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```

A 17 REPT:B-LEVEL @77700040 MFNUM=00000430 MICON=0000023 MSG STARTED
LV REGISTER LV=0012 D0=40001001 D1=00000000 D2=00000000 D3=00001200
PCRIV INCONCLUSIVE
DATA: B-LEVEL          AC1JR          AC1KR
00000000 00240274 00000000 00000000 00000077 00000000
AC1CSC 00240274 00000000 00000077 10062774 00000077 77700040
(B-LEVEL 50063231 54012463 00163537 00060260 77630074 00000000
DATA) 00000002 00000100 16050003 00000000 00000005 10063232
AC1INS 11464510 00000714 00000000 54603531 02402000 00000540
ST1INS 00000000 00000000 00000077 10062774 00100001 00020302
44000000 40000000 00000000 00000000 22120000 00013777
00002460 00000177 77777400 00000000 00000077 77700040
AC1CSC DATA: D-LEVEL
(D AND E) 00000000 00240274 00000000 00000000 00000077 00000000
00240274 00000000 00000077 10062774 00000077 77700040
AC1INS 50063231 54012453 00002433 00000261 37630003 40001000
(D AND E) 00000010 00001000 16000003 04000000 00000005 10063232
76543210 00000000 00000341 54603531 02402000 00000540
ST1INS 00000000 00400000 00000077 10062774 00000261 00000010
(D AND E) 00000715 00000670 01200000 00000000 00000000 77777400
DATA: PCRIV TEST RUN AND HASH SUM RESULTS
00000002 02000000 00400000
DATA: BLEV STANDBY CC REGISTERS
00000000 00000000 14030105 00000004 00000000 77600000
00000213 00000000 00000000 00000000 00000000 00000000
54032410 14410460 20173537 00000000 00000000 00000000
00000002 00000000 76477777 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00100001 00025302
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000
DATA: CONTENTS OF STACK
14020026 56140325 15270474 12356611 15201644 14576202
11464510 52525252 16021026 16030573 13520444 10302720
05/04/93 18:17:27
#935

```

Figure 1 - Example of PCRIV B-Level

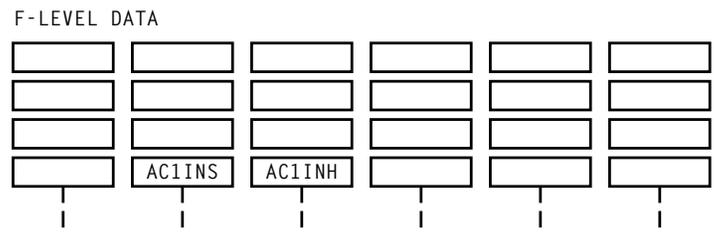
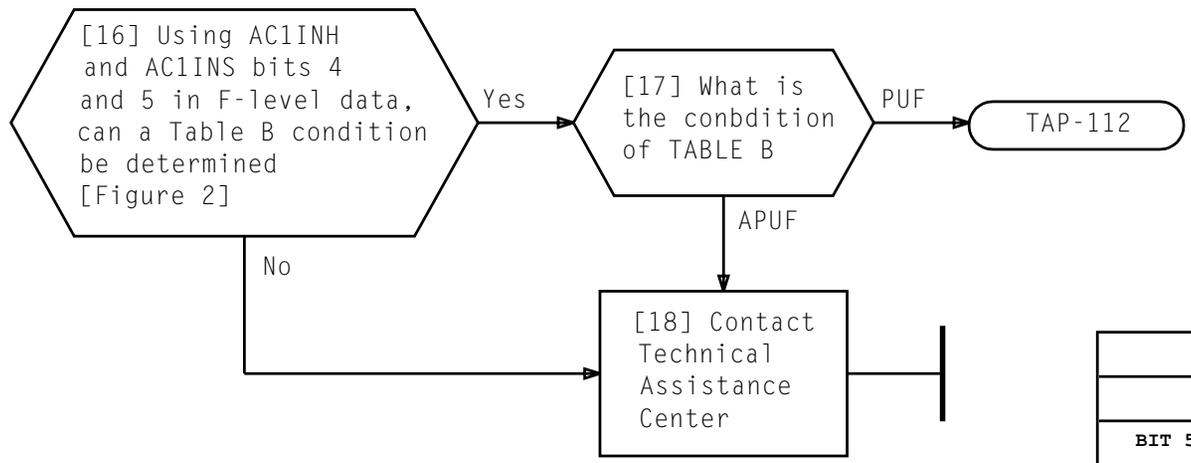
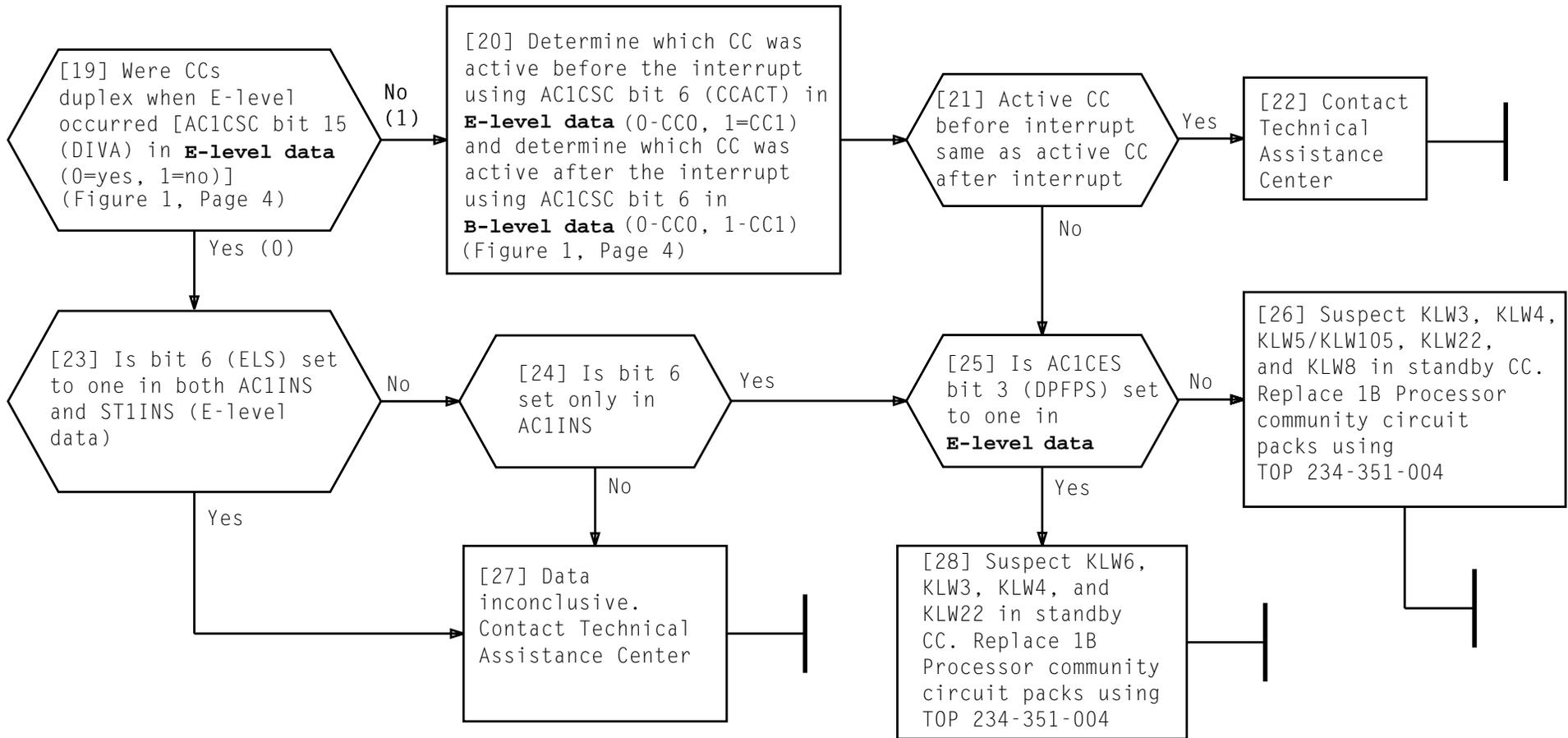
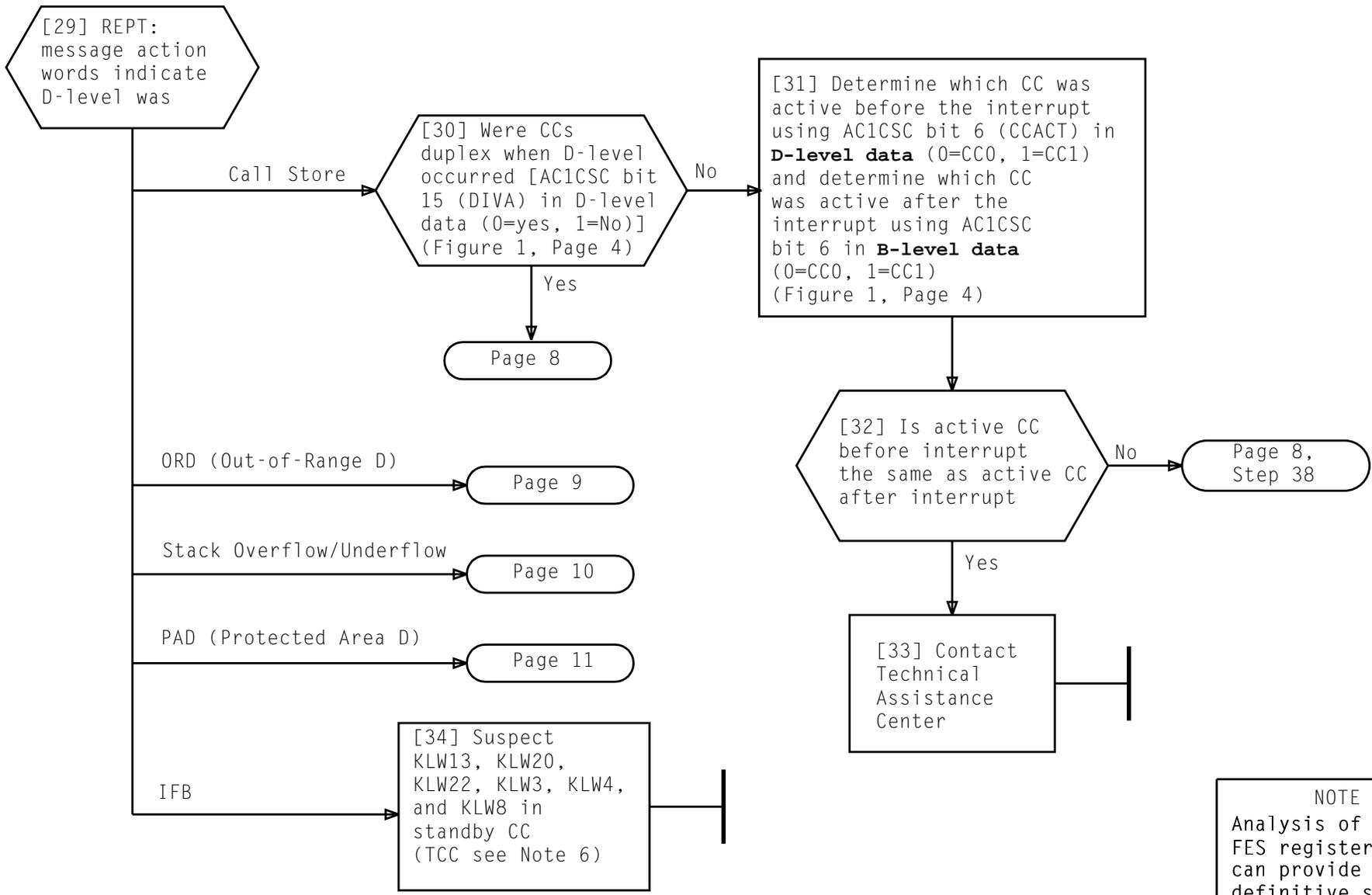


Figure 2 - Part of F-Level Data Layout

TABLE B				
AC1INH		AC1INS		CONDITION
BIT 5 (IPUFS)	BIT 4 (IAPUFS)	BIT 5 (PUFS)	BIT 4 (APUFS)	
DC	0	0	1	APUF
0	0	1	DC	PUF
0	1	1	DC	
1	0	DC	1	APUF

DC = Don't Care

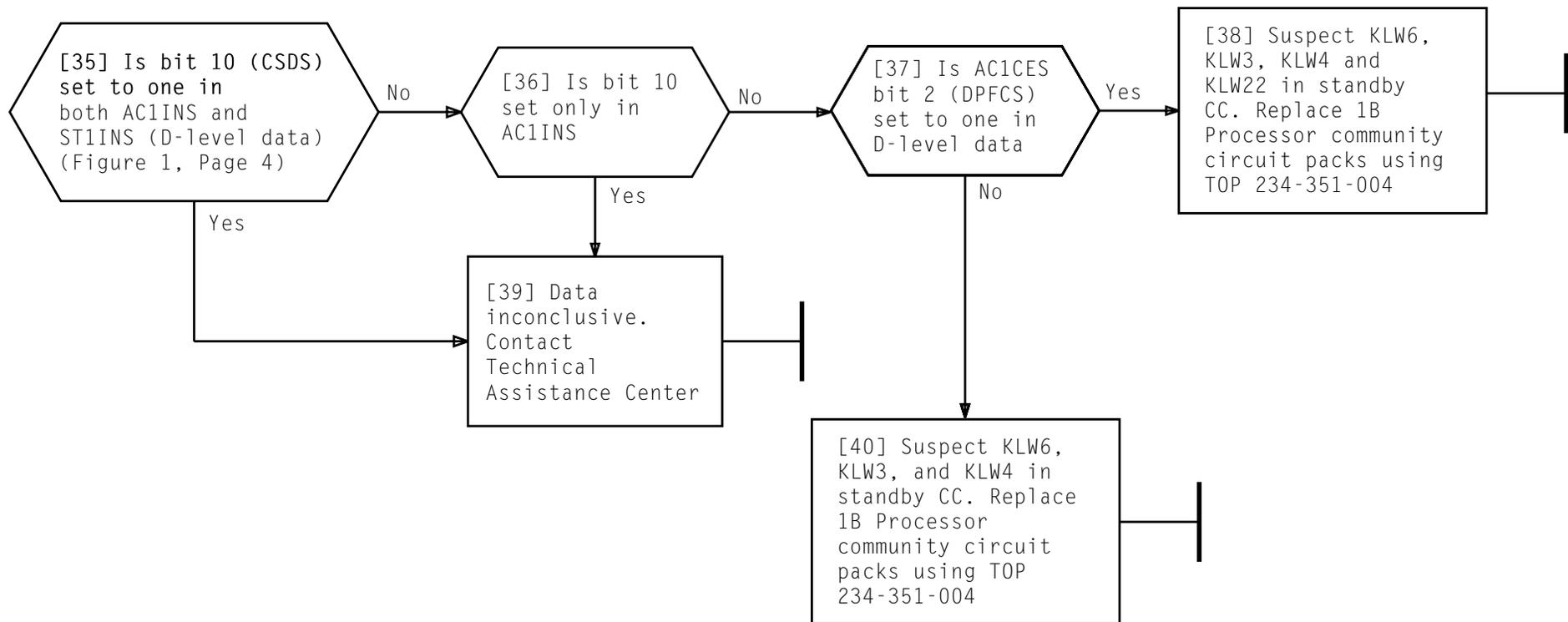


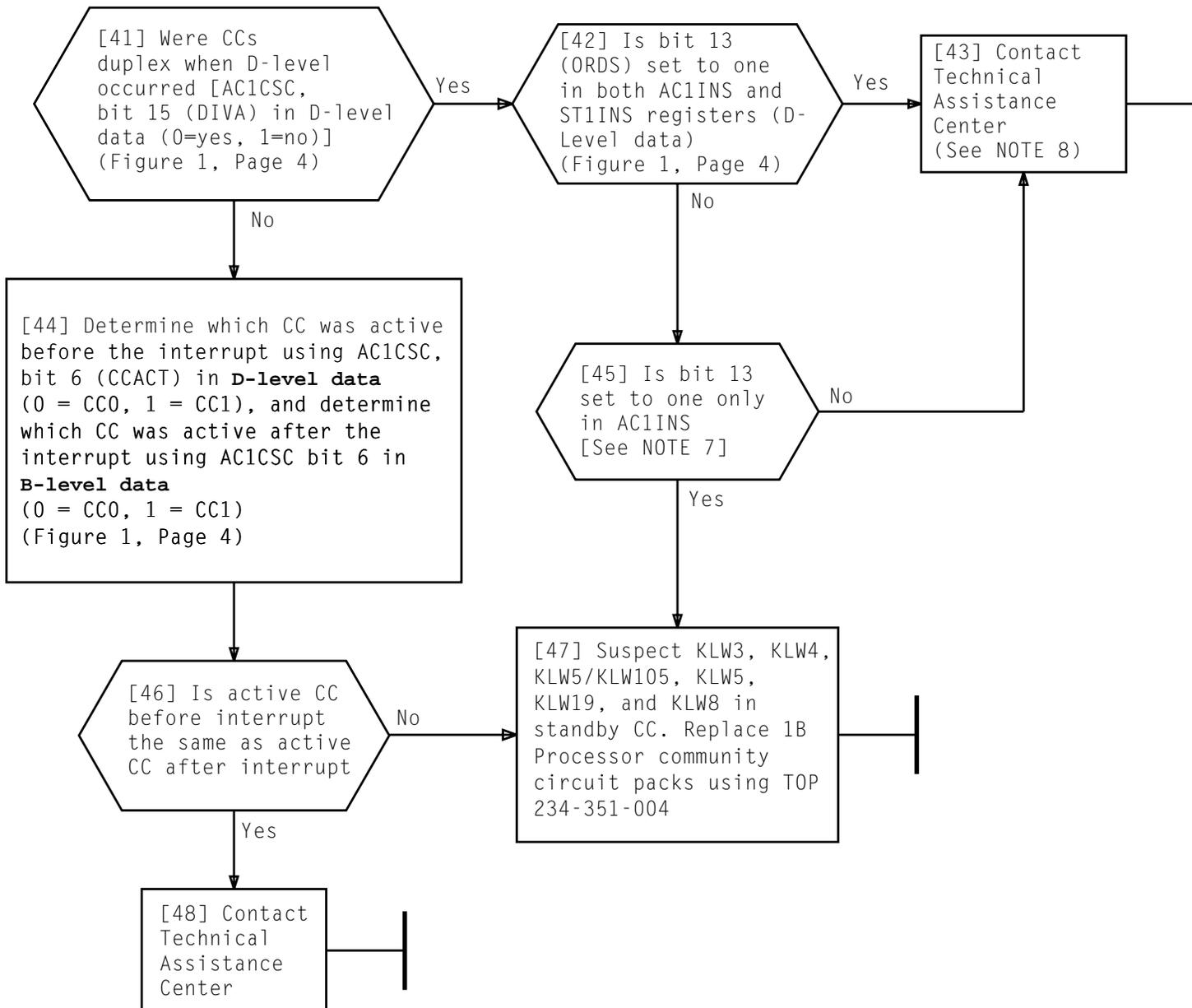


NOTE 6
Analysis of CES and
FES registers can
can provide more
definitive suspect
pack data.

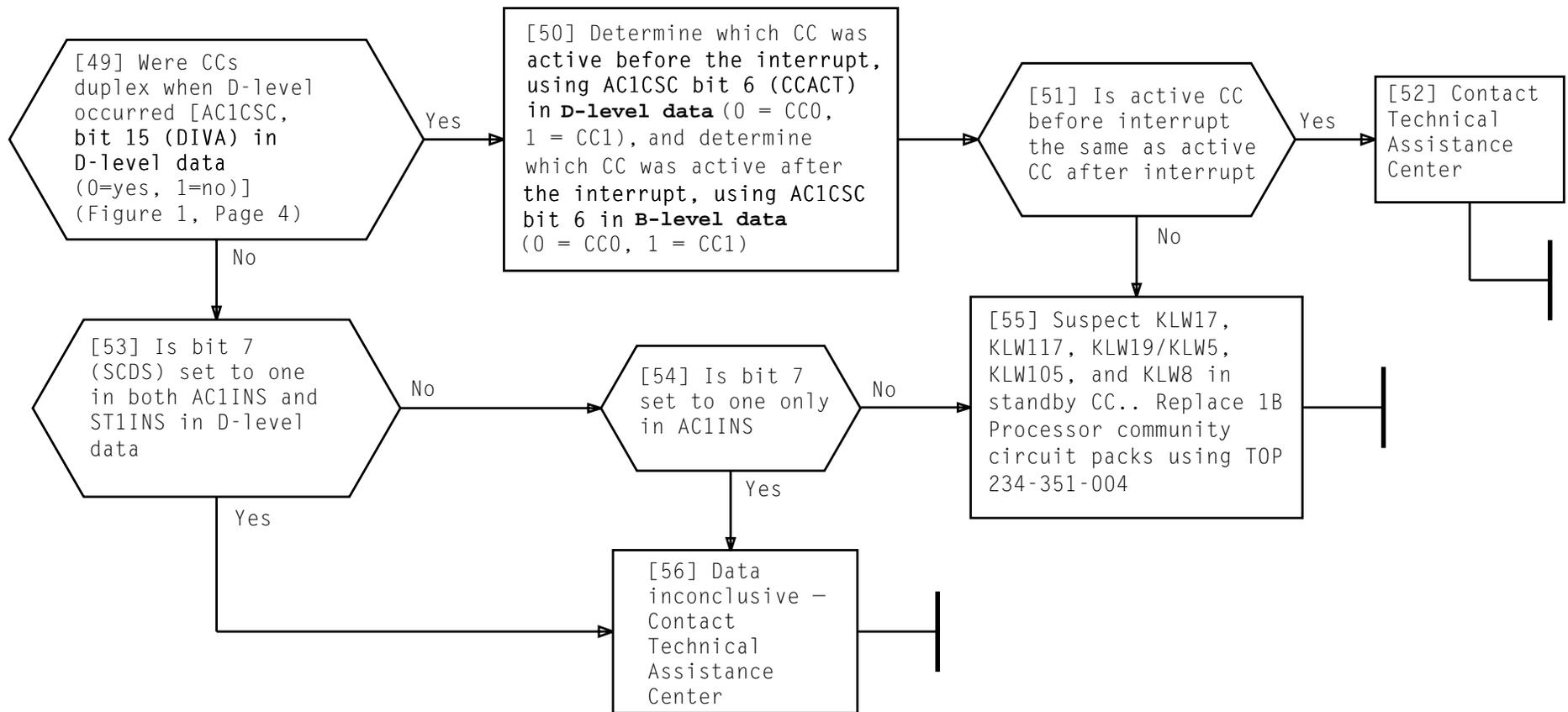
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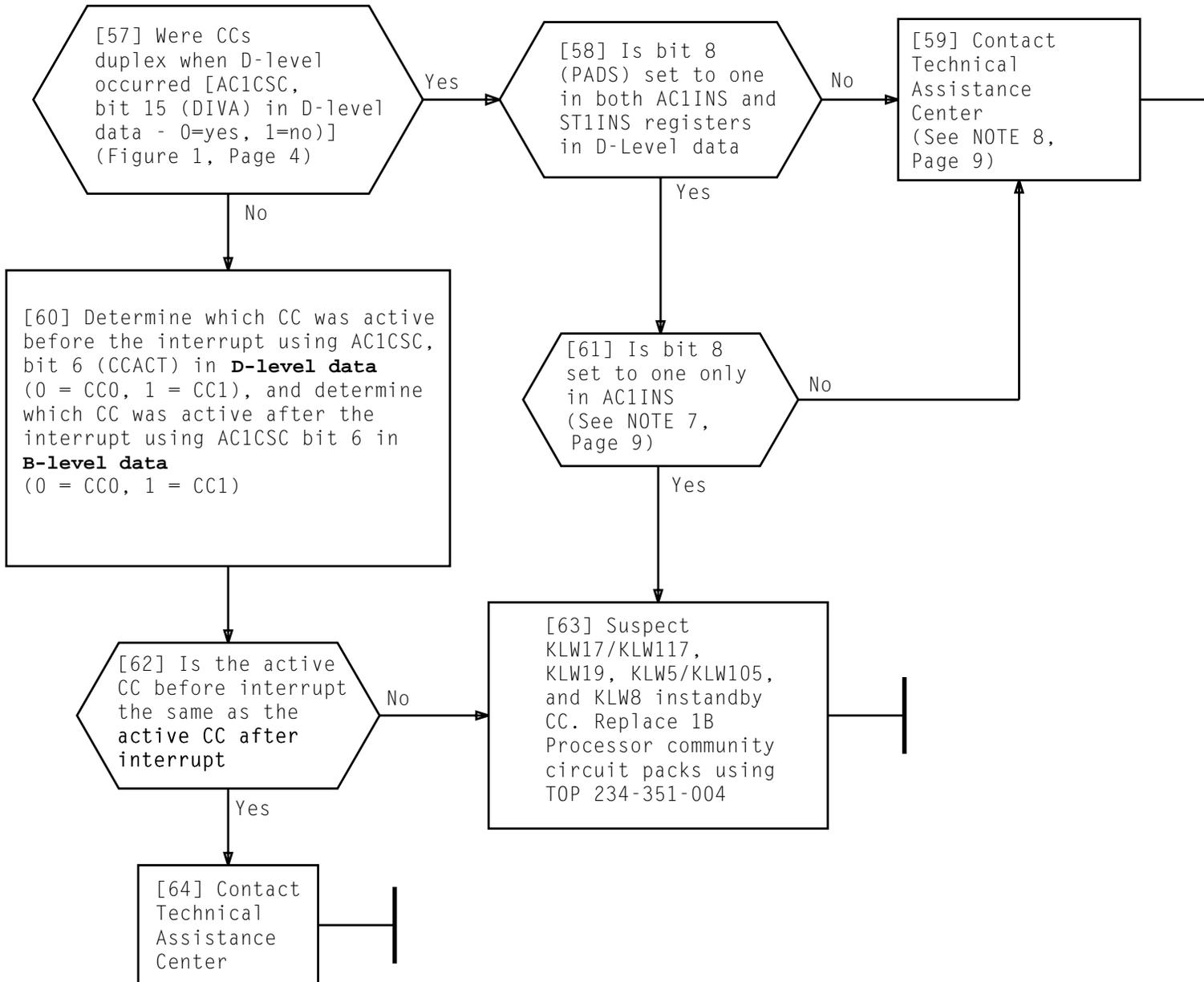
ANALYZE B-LEVEL INTERRUPT





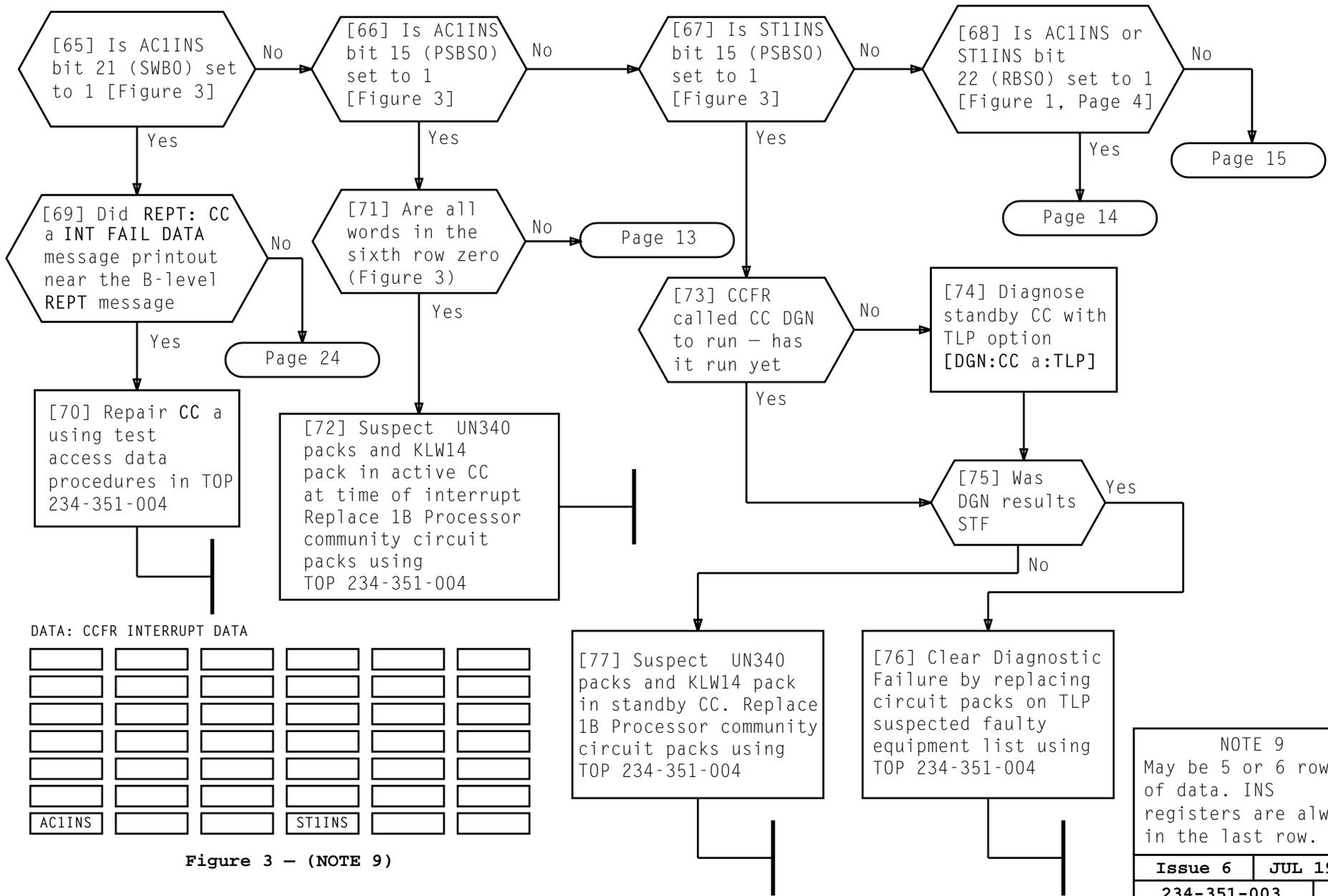
NOTES	
7.	It should be assumed that the active CC is switched out by B-level activity; it is very unlikely CCs could have gotten back duplex during interrupt activity.
8.	The Technical Assistance Center analyzes SCA, ASD, and SDA registers looking for ways the system could have been executing instructions with bad options or executing out of MMIO range.
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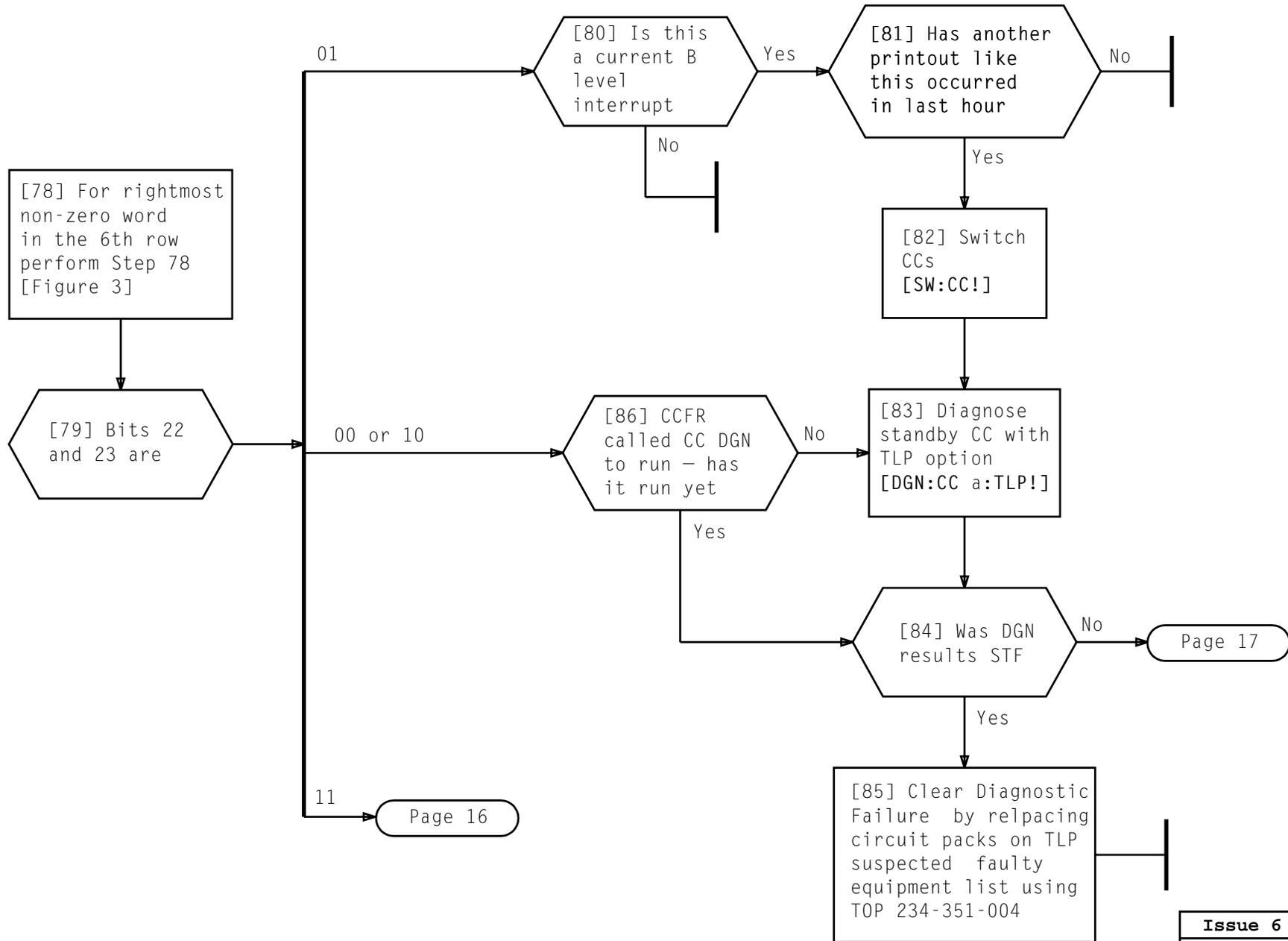
DATA: CCFR INTERRUPT DATA

AC1INS			ST1INS		

Figure 3 - (NOTE 9)

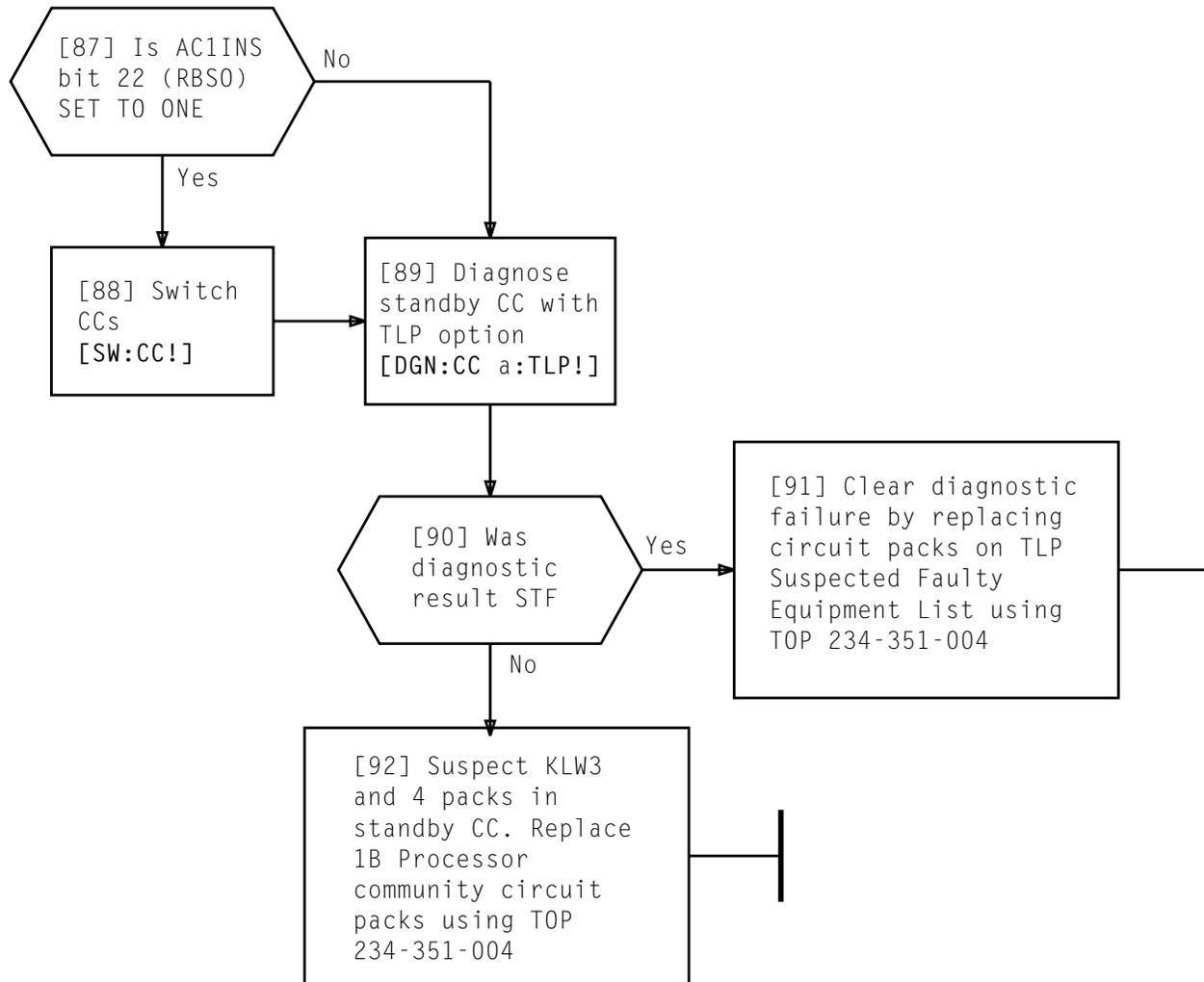
ANALYZE B-LEVEL INTERRUPT

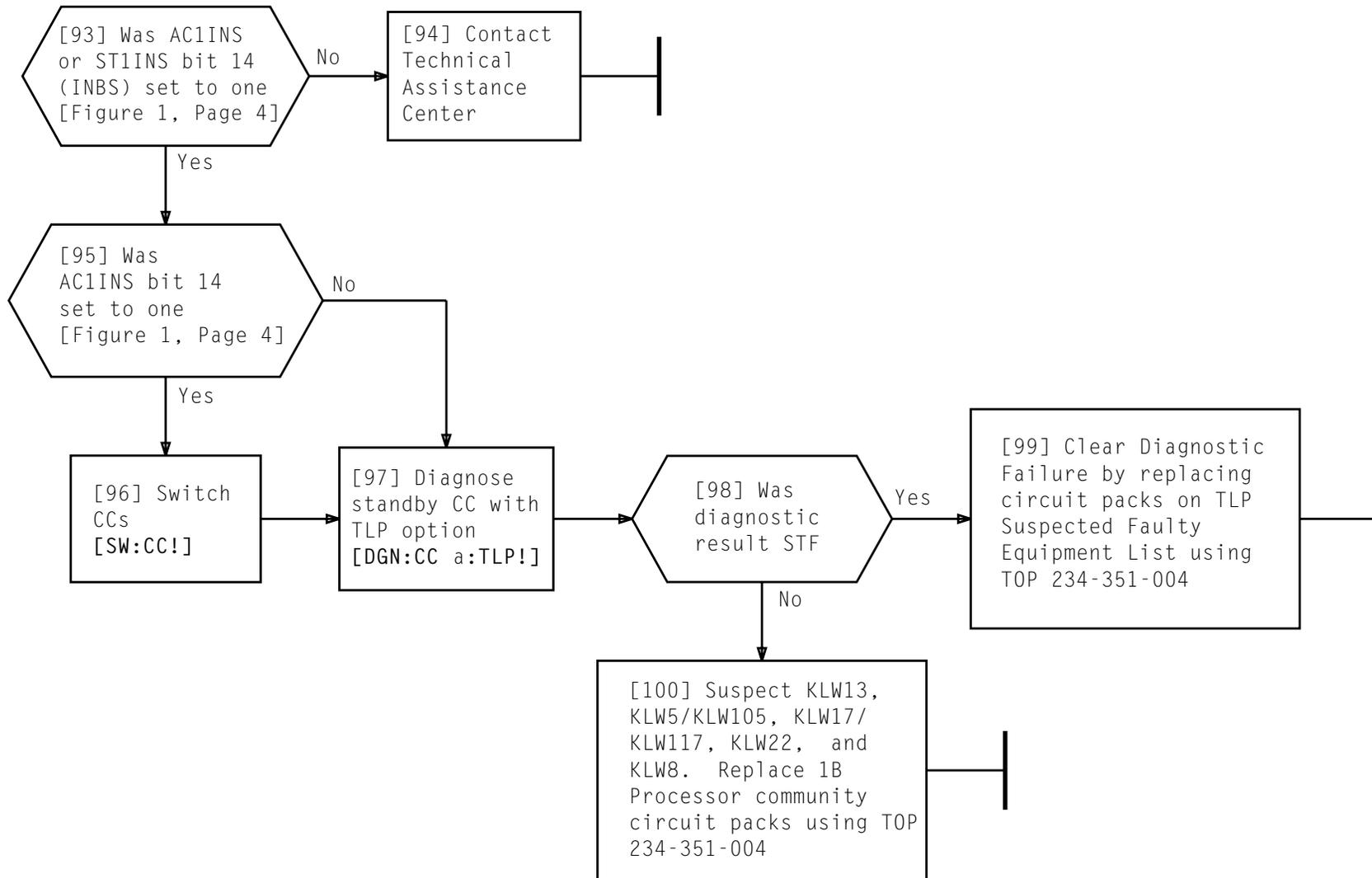
NOTE 9 May be 5 or 6 rows of data. INS registers are always in the last row.	
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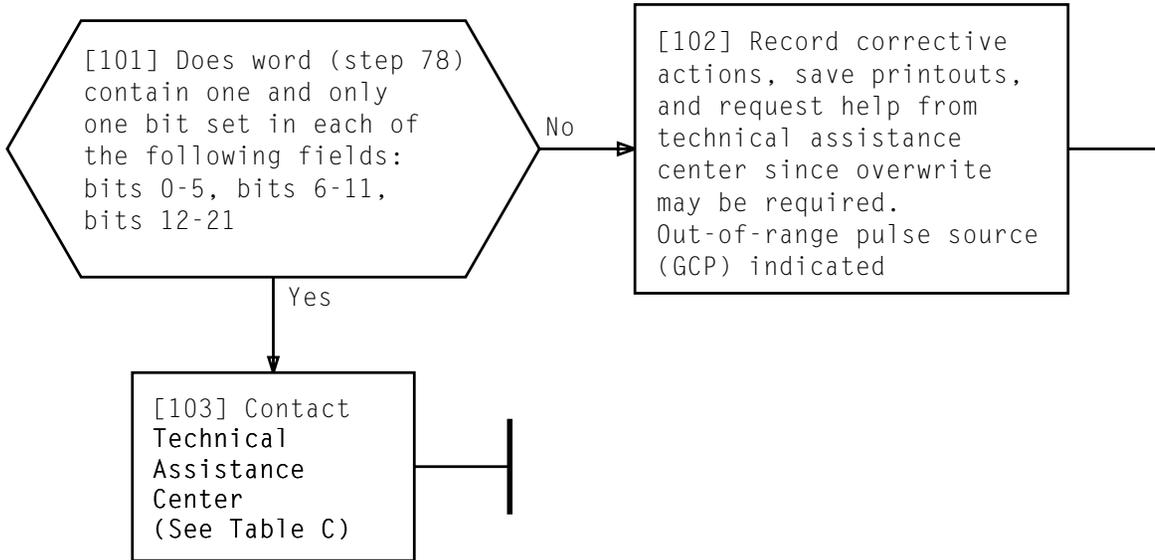
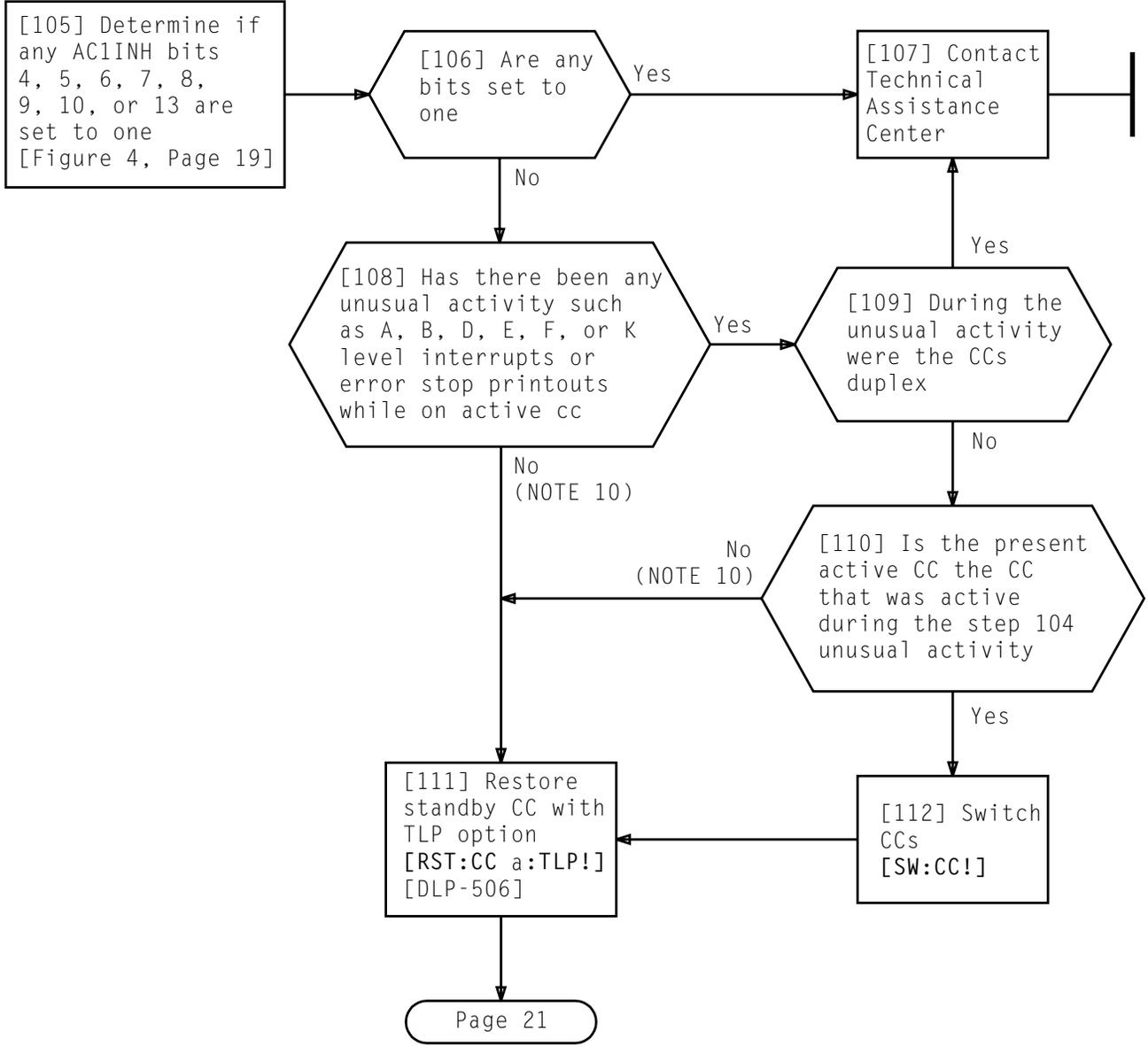


TABLE C INVALID GCP ADDRESSES	
ADDRESS (BITS 0-21)	
00020204-00024040	
00042004-00042040	
00100420-00104040	
00202020-00202040	
02002004-02002020	
04001001-04001040	
04004001-04004040	
10000104	
10000410	
10004002	

[104] Suspect K LW14 and UN340 packs using Table D, Page 17, and lower bits of Step 78 Words for address in standby CC. Replace 1B Processor community circuit packs using TOP 234-351-004



TABLE D PULSE SOURCE ADDRESS TO CP LOCATION CROSS REFERENCE		
PULSE SOURCE ADDRESS	CIRCUIT PACK TYPE	CIRCUIT PACK LOCATION
00010101-00104040	KLW14	058-038
00200101-00200102	UN340	070-062
00200104-00200210	UN340	070-038
00200220-00200240	UN340	070-062
00200401-00200402	UN340	070-038
00200404-00200440	UN340	070-062
00201001-00201010	UN340	070-038
00201020-00202002	UN340	070-062
00202004-00202010	UN340	070-038
00204001-00204010	UN340	070-062
00204020-00204040	UN340	070-038
00400101-01000240	UN340	070-038
01000401-02001040	UN340	070-062
02002001-02002002	UN340	070-038
02002004-02002020	UN340	070-062
02002040-02004040	UN340	070-038
04000101-10004040	KLW14	058-038



NOTE 10	
Because active CC is stable suspect standby CC.	
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DATA: C-LEVEL

	AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR	
	AC1YR	AC1ZR	AC1BR(H)	AC1BR(L)	AC1ASC(H)	AC1ASC(L)	
	AC1SCA	AC1SDA	AC1CSC	AC1CES	AC1FST	AC1FES	
	AC1ILR	AC1INS	AC1INH	AC1INJ	AC1SC	AC1SR	
	<SC+1>	ST1INS	AC1LIT(E)	AC1LPI	AC1ER	AC1PRM	
	AC1PRL	AC1PSC	AC1BRS(H)	AC1BRS(L)	ST1ASC(H)	ST1ASC(L)	
	ST1SCA	ST1SDA	ST1BRS(H)	ST1BRS(L)	AC1MEO(H)	AC1MEO(L)	(ADAN)
	ST1LIT	ST1LPI	AC1MSR	AC1MMR	ST1MIO(H)	ST1MIO(L)	
(AFAN)	AC1MIO(H)	AC1MIO(L)	AC1ME1(H)	AC1ME1(L)	AC1MI1(H)	AC1MI1(L)	(DBR)
	ST1MEO(H)	ST1MEO(L)	ST1MI1(H)	ST1MI1(L)	ST1ME1(H)	ST1ME1(L)	
	AC1SAT	AC1TAR	AC1BNCTL	(DADB)			

DATA: ACTIVE CC REGISTERS

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1SR	AC1SC	AC1CES	AC1IBR
AC1INS	AC1INJ	AC1ILA	AC1ILR	AC1ITR	AC1INH
AC1CSC	AC1SAT	AC1PCR	AC1MCLK	AC1LIT	AC1DLR
AC1LPA	AC1UPA	AC1ACT	AC1ER	AC1PRM	AC1PRL
AC1LPI	AC1PES	AC1PSC	AC1PSQ	AC1RPO	AC1RP1
AC1PMO	AC1PM1	AC1ABC	AC1SAL	AC1SAR	AC1FIS
AC1EPS	AC1IFR	AC1MMR	AC1MSR	AC1MCO(H)	AC1MCO(L)
AC1MCD(H)	AC1MCD(L)	AC1MCP	AC1CCS(H)	AC1CCS(L)	AC1CUI
AC1FCT	AC1FCE	AC1FES	AC1FEE	AC1FER	AC1FST
AC1FLA(H)	AC1FLA(L)	AC1FLD(H)	AC1FLD(L)	AC1FLT(H)	AC1FLT(L)
AC1FRU(H)	AC1FRU(L)	AC1FRL(H)	AC1FRL(L)	AC1FIP	AC1CLE

DATA: STANDBY CC REGISTERS

ST1FR	ST1GR	ST1JR	ST1KR	ST1LR	ST1XR
ST1YR	ST1ZR	ST1SR	ST1SC	ST1CES	ST1IBR
ST1INS	ST1INJ	ST1ILA	ST1ILR	ST1ITR	ST1INH
ST1CSC	ST1SAT	ST1PCR	ST1MCLK	ST1LIT	ST1DLR
ST1LPA	ST1UPA	ST1ACT	ST1ER	ST1PRM	ST1PRL
ST1LPI	ST1PES	ST1PSC	ST1PSQ	ST1RPO	ST1RP1
ST1PMO	ST1PM1	ST1ABC	ST1SAL	ST1SAR	ST1FIS
ST1EPS	ST1IFR	ST1MMR	ST1MSR	ST1MCO(H)	ST1MCO(L)
ST1MCD(H)	ST1MCD(L)	ST1MCP	ST1CCS(H)	ST1CCS(L)	ST1CUI
ST1FCT	ST1FCE	ST1FES	ST1FEE	ST1FER	ST1FST
ST1FLA(H)	ST1FLA(L)	ST1FLD(H)	ST1FLD(L)	ST1FLT(H)	ST1FLT(L)
ST1FRU(H)	ST1FRU(L)	ST1FRL(H)	ST1FRL(L)	ST1FIP	ST1CLE

Figure. 4 - C-Level Portion of B-Level Interrupt

```

A 50 REPT: B-LEVEL 077700000 MFNUM=00000134 MICON=40000063 MSG STARTED
LV=0006 DO=41140000 D1=00000000 D2=00000000 D3=00001200
CCFR REMOVED CC 1
DATA: B-LEVEL
00041040 00000000 14134070 14157252 03777777 77600000
77626000 00000006 00000000 01010000 00000077 77700000
54134013 50000210 00175657 00060220 77630074 00000000
00000002 10000100 76473777 00000000 00000020 13530236
11205310 10000000 00000000 54156376 00000000 00000000
76543210 00000000 00000000 01010000 00100001 00020301
40012525 40122000 00000000 00240000 62120000 00003777
00002460 00000177 77777400 63164010 32071003 20030000
DATA: C-LEVEL
00000000 00000314 14115026 00000004 00177777 17600000
77624000 00000314 00000000 00000314 00000077 54115230
54115226 77624012 00000513 00002361 74460003 00000000
00000004 00005000 76000003 04000000 00000003 13530236
14054100 00001000 00000000 50170356 01010000 00001540
00000300 00000006 00000000 00000314 00000177 50124130
54115226 77624012 00000000 00000314 00000077 77624012
25511077 50170356 00202006 00010007 00000077 77624012
00000077 54115232 00000000 00000314 00000000 00000314
00000077 54115234 00000000 00000314 00000000 00000314
00000241 00000177 77777400
07/09/93 14:49:55
#149

```

Figure. 5 - Example of AFAN mismatch

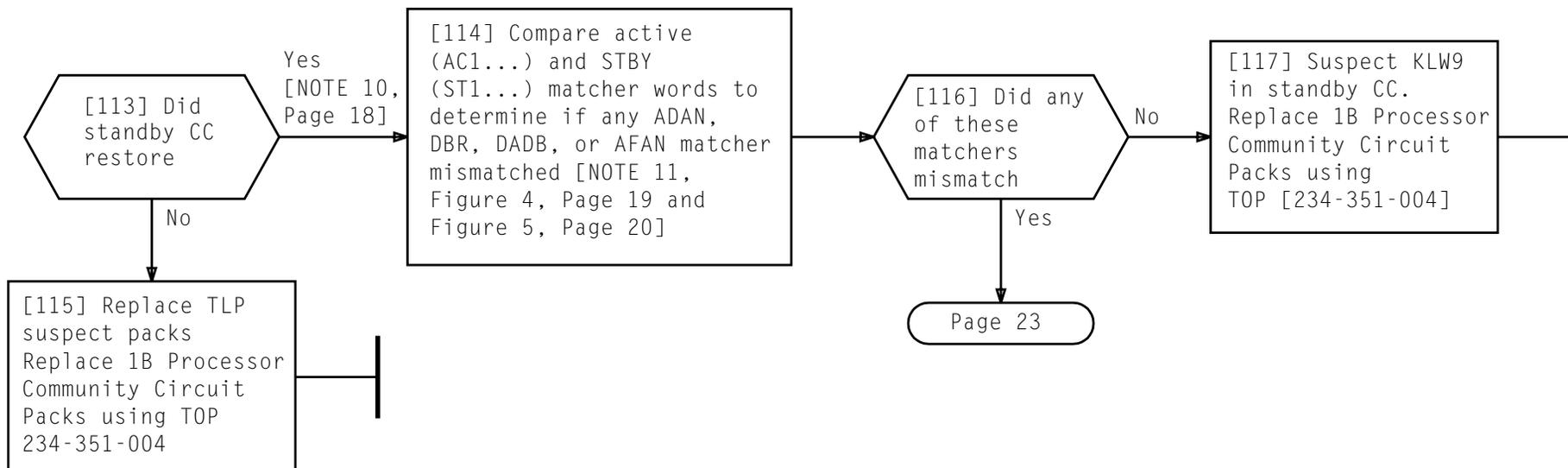
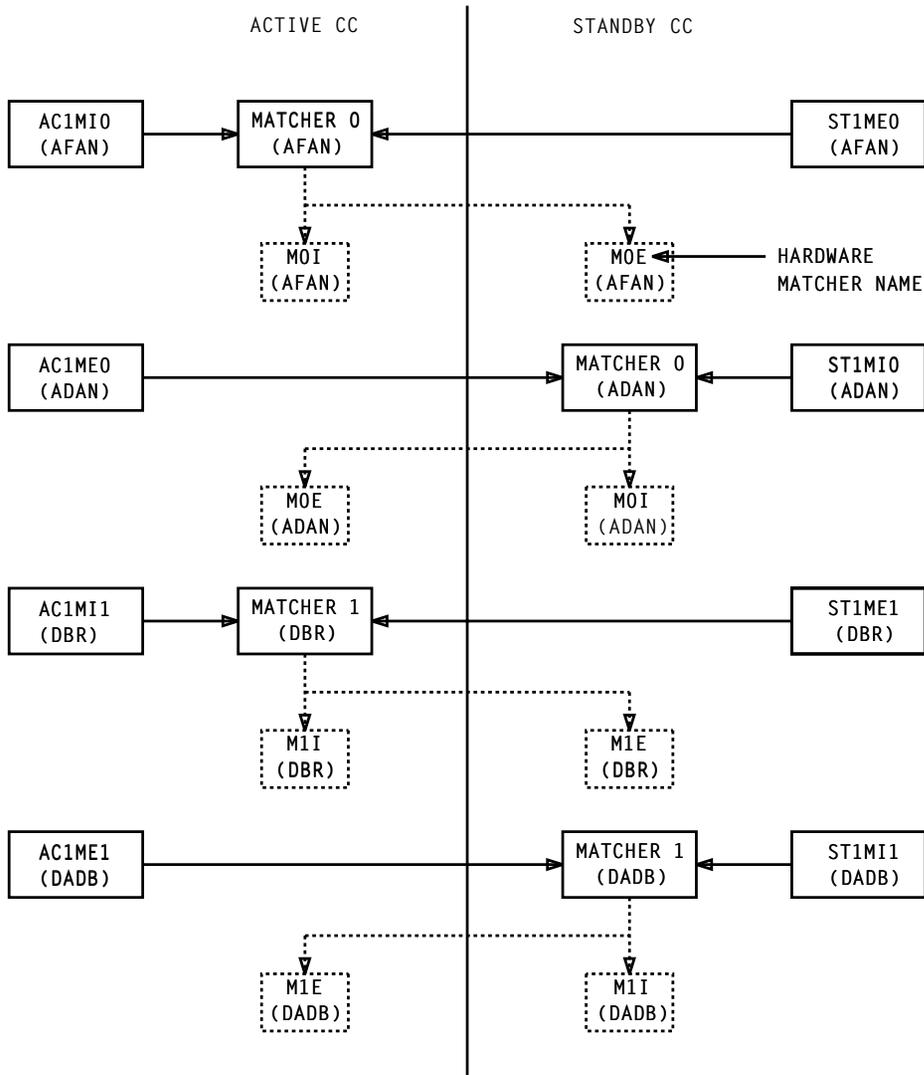


TABLE E - MATCH SUMMARY REGISTER (MSR) LAYOUT			
BIT	HARDWARE NAME	DESCRIPTION	ACCESS
0	MACT	Matcher Active	R
1	MLIERR	Matcher Latched Internal Error	R
2	MLEERR	Matcher Latched External Error	R
10	MOI	Internal Matcher 0 Error Latched Output	R/W
11	MOE	External Matcher 0 Error Latched Output	R/W
12	M1I	Internal Matcher 1 Error Latched Output	R/W
13	M1E	External Matcher 1 Error Latched Output	R/W
16	MAOI	Direct Output Internal Matcher 0 Error	R
17	MINO	Direct Output External Matcher 0 Error	R
18	MA1I	Direct Output Internal Matcher 1 Error	R
19	MIN1	Direct Output External Matcher 1 Error	R

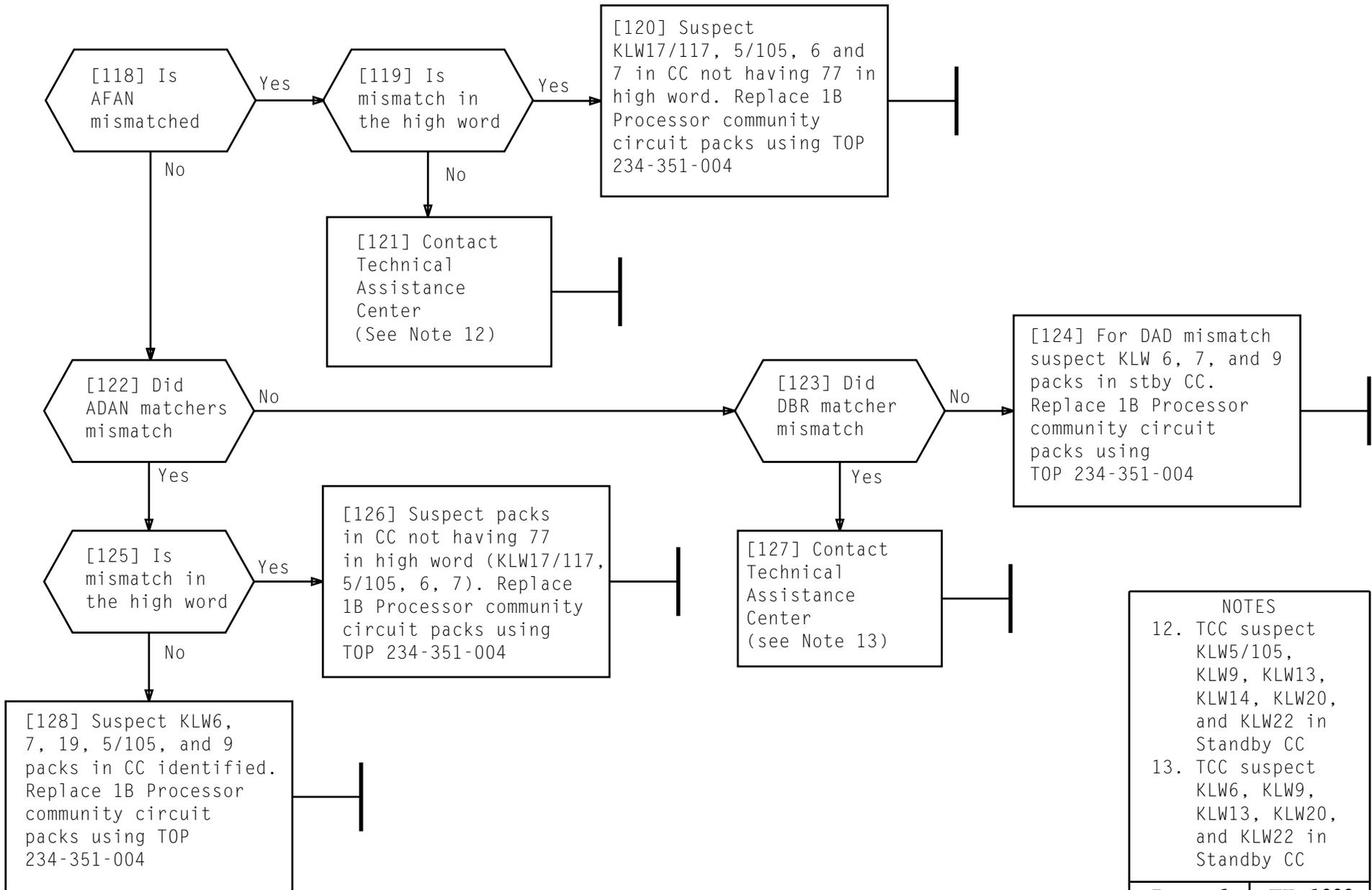
NOTE 11 Figure 6 and TABLE A, Page 1, and TABLE E provide additional matcher information	
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NAME	BITS	SIGNAL	MATCHER	CC WHERE MATCHED
AFAN	32	FETCH ADDRESS BUS	0	ACTIVE
ADAN	30	DATA ADDRESS BUS	1	STANDBY
DBR	32	BUFFER REGISTER	1	ACTIVE
DADB	32	ALU OUTPUT BUS	1	STANDBY

NOTE: DASHED LINES INDICATE MATCHER ERROR SOURCES

Figure 6 - CC Matchers



NOTES

12. TCC suspect KWL5/105, KWL9, KWL13, KWL14, KWL20, and KWL22 in Standby CC

13. TCC suspect KWL6, KWL9, KWL13, KWL20, and KWL22 in Standby CC

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[129] Using the addresses in the AC1JR and AC1KR find the pident they are in [Figure 1, Page 4, DLP-509]



[130] Use TABLE F to identify suspect packs based upon the pident names. Replace 1B Processor community circuit packs using TOP 234-351-004



TABLE F	
PIDENT	SUSPECT PACK(S)
PSFRXXXX OR CSFRXXXX	KLW22, KLW3, KLW4, KLW6, KLW5/KLW105, KLW8
BBFRXXXX OR PLFRXXXX	KLW14, UN338, KLW24
IFFRXXXX	KLW13, KLW20, KLW22, KLW3, KLW4
DIFFRXXXX	UN340, NOTE 14

NOTE 14	
DIF DGN should be run on any DIF member 24 and above to check extended polling	
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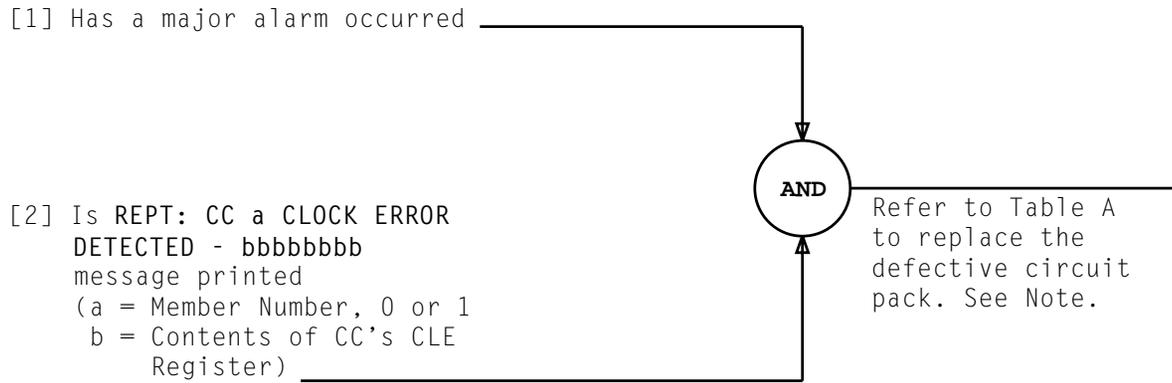


TABLE A	
CLE Register bit set	Actions
0	Unlatch CLK ES for clock generator -n/a (Summary bit)
1	ACT generator clock error bit (KLW24 in CC a)
2	CC distribuion clock error (KLW24 in CC a)
3	Interface bus 0T4 clock error (KLW20 in CC a)
4	Interface bus 2T6 clock error (KLW13 in CC a)
5	STBY CC TRC or cable fail error (KLW24 in STBY CC)
6	STBY CC TRC or cable fail set (KLW24 in STBY CC)

NOTE	
It is very important to attach a copy of the audit failure to the defective pack, or it is impossible for the factory to repair it.	
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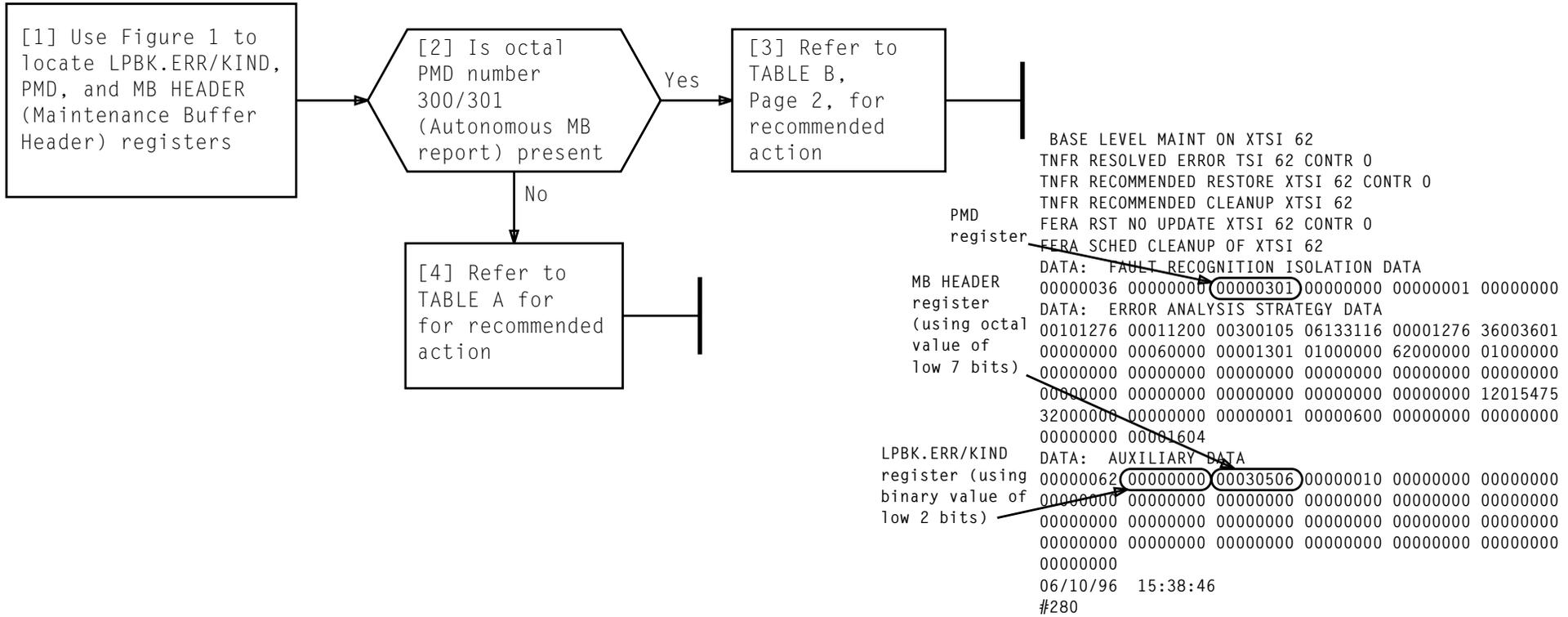


Figure 1. LPBK.ERR/KIND, PMD, and MB HEADER Registers

TABLE A			
XTSI BLM PRINTOUT			
LPBK.ERR/ KIND BITS	OCTAL PMD NUMBER	DESCRIPTION	RECOMMENDED ACTIONS
01	307	Illegitimate MB Report	No action required by craft-persons, unexpected non-autonomous MB response or out of range subunit autonomous MB response
10	302	Loopback BLM	No action required by craft-persons, invalid DS1/DS3 loopback state
11	Not used	Not used	Not used

TABLE B		
XTSI AUTONOMOUS BLM		
OCTAL MB HEADER*	MEANING	RECOMMENDED ACTIONS
6	XTSI autonomous report sent by D3U firmware	No action required by craft-persons
102	Flash memory file audit error	Copy XTSI file (COPY:XTSI file-number) (See Figure 2 for file-number) and refer to DLP-533
103	Busy idle audit error for TSM	No action required by craft-persons
106	Flash memory or USEC audit disable	If FERA REQ NO ACTION, then restore XTSI. Else, no action required by craft-persons (RST:XTSI a,CONTR b)
107	Protection switch table mismatch detected	No action required by craft-persons
110	XTC scheduler has been stopped for 30 minutes	If FERA REQ NO ACTION, then restore XTSI. Else, no action required by craft-persons (RST:XTSI a,CONTR b)
* See Figure 1, Page 1		

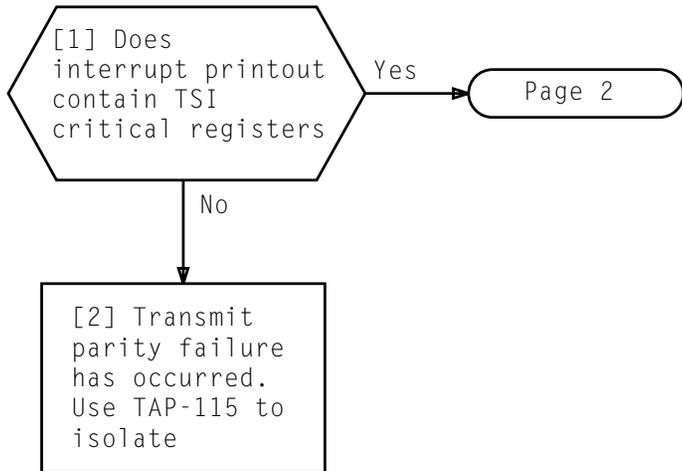
```

BASE LEVEL MAINT ON XTSI 62
TNFR RESOLVED ERROR TSI 62 CONTR 0
TNFR RECOMMENDED RESTORE XTSI 62 CONTR 0
TNFR RECOMMENDED CLEANUP XTSI 62
FERA RST NO UPDATE XTSI 62 CONTR 0
FERA SCHED CLEANUP OF XTSI 62
DATA: FAULT RECOGNITION ISOLATION DATA
00000036 00000000 00000301 00000000 00000001 00000000
DATA: ERROR ANALYSIS STRATEGY DATA
00101276 00011200 00300105 06133116 00001276 36003601
00000000 00060000 00001301 01000000 62000000 01000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 12015475
32000000 00000000 00000001 00000600 00000000 00000000
00000000 00001604
DATA: AUXILIARY DATA
00000062 00000000 00030506 00000010 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000
06/10/96 15:38:46
#280

```

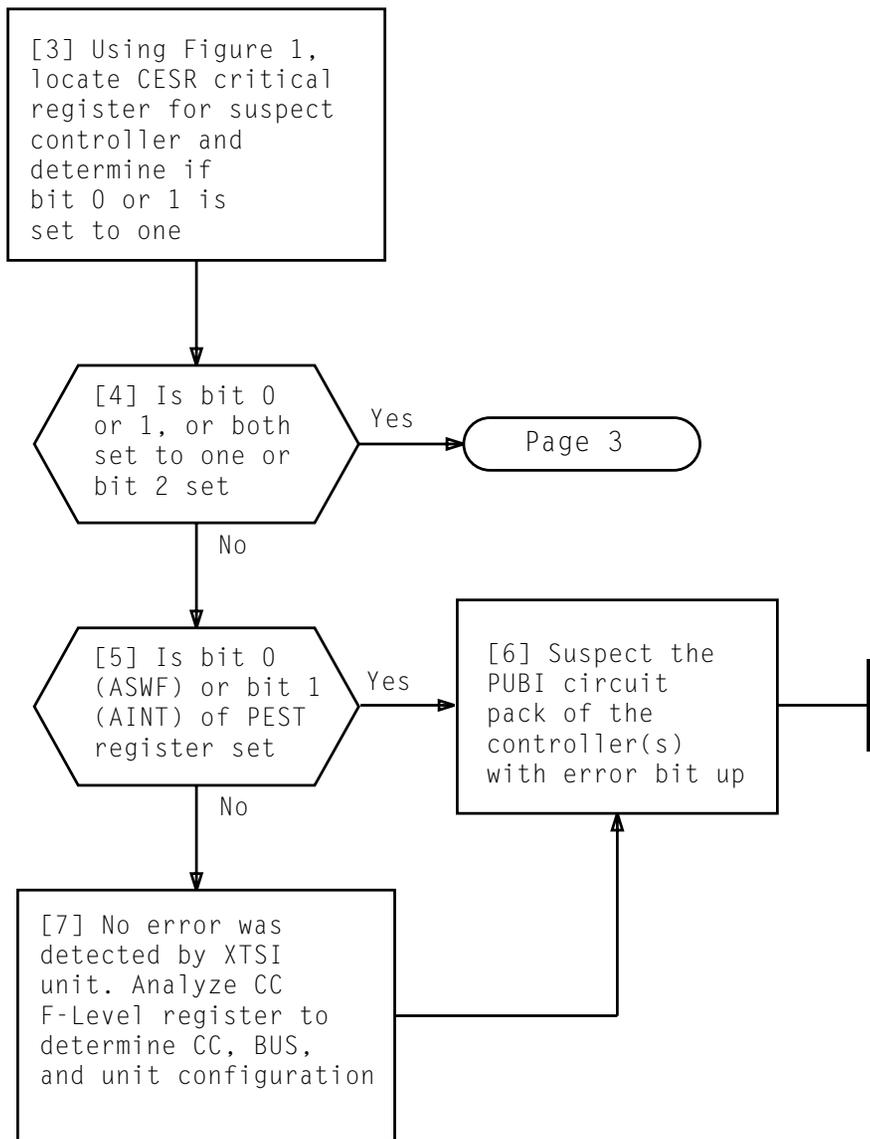
File-number register (Using octal value of low 7 bits)

Figure 2. File-Number Register



ANALYZE TNFR F-LEVEL INTERRUPT, EXPANDED TIME-SLOT INTERCHANGE (XTSI)

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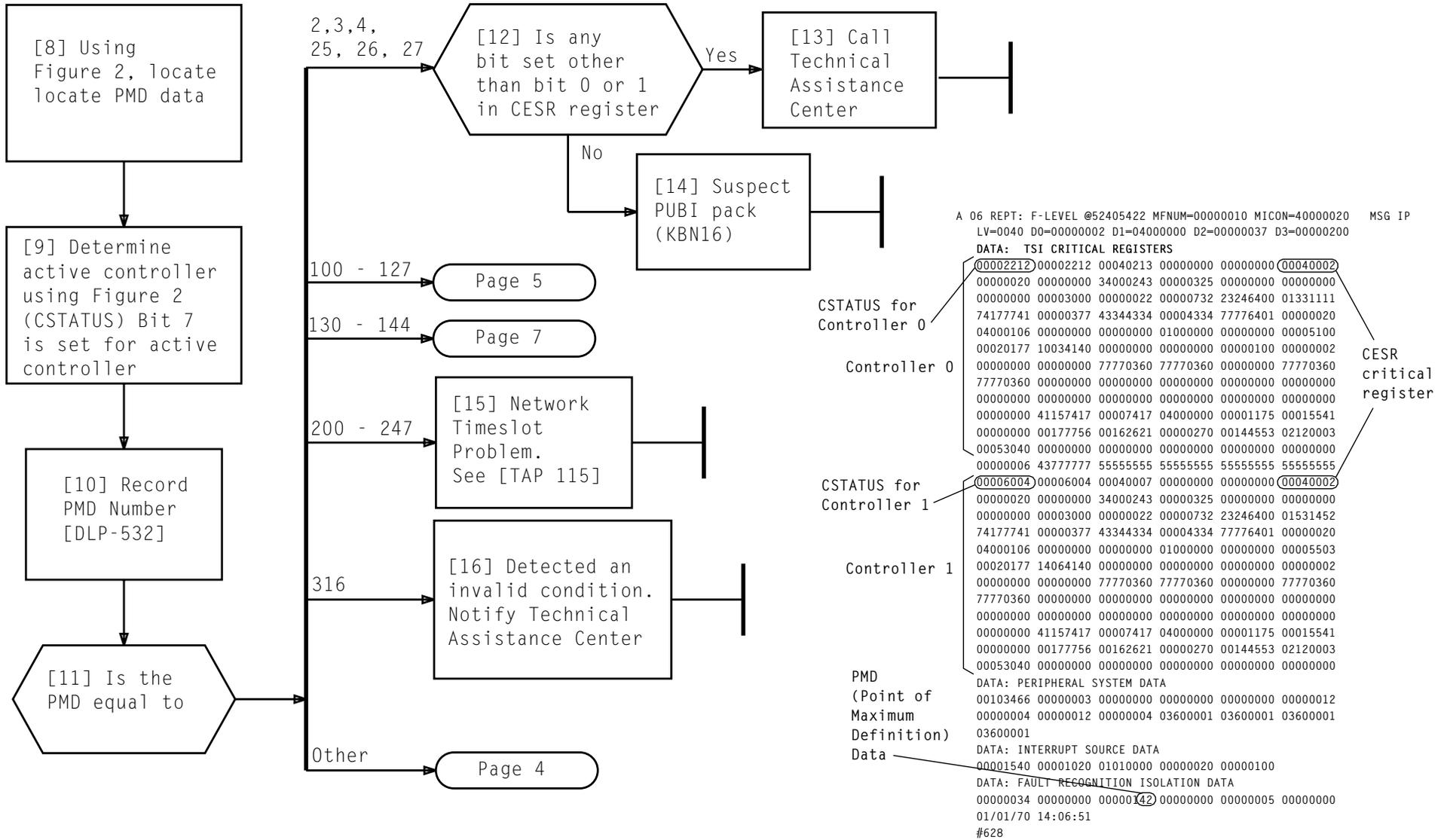
```

A 06 REPT: F-LEVEL @52405422 MFNUM=00000010 MICON=40000020 MSG IP
LV=0040 D0=00000002 D1=04000000 D2=00000037 D3=000000200
DATA: TSI CRITICAL REGISTERS
00002212 00002212 00040213 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000
00000000 00003000 00000022 00000732 23246400 01331111
74177741 00000377 43344334 00004334 77776401 00000020
04000106 00000000 00000000 01000000 00000000 00005100
00020177 10034140 00000000 00000000 00000100 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
00000006 43777777 55555555 55555555 55555555 55555555
00006004 00006004 00040007 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000
00000000 00003000 00000022 00000732 23246400 01531452
74177741 00000377 43344334 00004334 77776401 00000020
04000106 00000000 00000000 01000000 00000000 00005503
00020177 14064140 00000000 00000000 00000000 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
DATA: PERIPHERAL SYSTEM DATA
00103466 00000003 00000000 00000000 00000000 00000012
00000004 00000012 00000004 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00001540 00001020 01010000 00000020 00000100
DATA: FAULT RECOGNITION ISOLATION DATA
00000034 00000000 00000142 00000000 00000005 00000000
01/01/70 14:06:51
#628
  
```

Figure 1 - XTSI Critical Registers

ANALYZE TNFR F-LEVEL INTERRUPT, EXPANDED TIME-SLOT INTERCHANGE (XTSI)

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```

A 06 REPT: F-LEVEL @52405422 MFNUM=00000010 MICON=40000020 MSG IP
LV=0040 D0=00000002 D1=04000000 D2=00000037 D3=00000200
DATA: TSI CRITICAL REGISTERS
00002212 00002212 00040213 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000
00000000 00003000 00000022 00000732 23246400 01331111
74177741 00000377 43344334 00004334 77776401 00000020
04000106 00000000 00000000 01000000 00000000 00005100
00020177 10034140 00000000 00000000 00000100 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
00000006 43777777 55555555 55555555 55555555 55555555
CSTATUS for Controller 0
00006004 00006004 00040007 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000
00000000 00003000 00000022 00000732 23246400 01531452
74177741 00000377 43344334 00004334 77776401 00000020
04000106 00000000 00000000 01000000 00000000 00005503
00020177 14064140 00000000 00000000 00000000 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
PMD (Point of Maximum Definition) Data
DATA: PERIPHERAL SYSTEM DATA
00103466 00000003 00000000 00000000 00000000 00000012
00000004 00000012 00000004 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00001540 00001020 01010000 00000020 00000100
DATA: FAULT RECOGNITION ISOLATION DATA
00000034 00000000 00000142 00000000 00000005 00000000
01/01/70 14:06:51
#628

```

Figure 2 - XTSI Critical Registers

ANALYZE TNFR F-LEVEL INTERRUPT, EXPANDED TIME-SLOT INTERCHANGE (XTSI)

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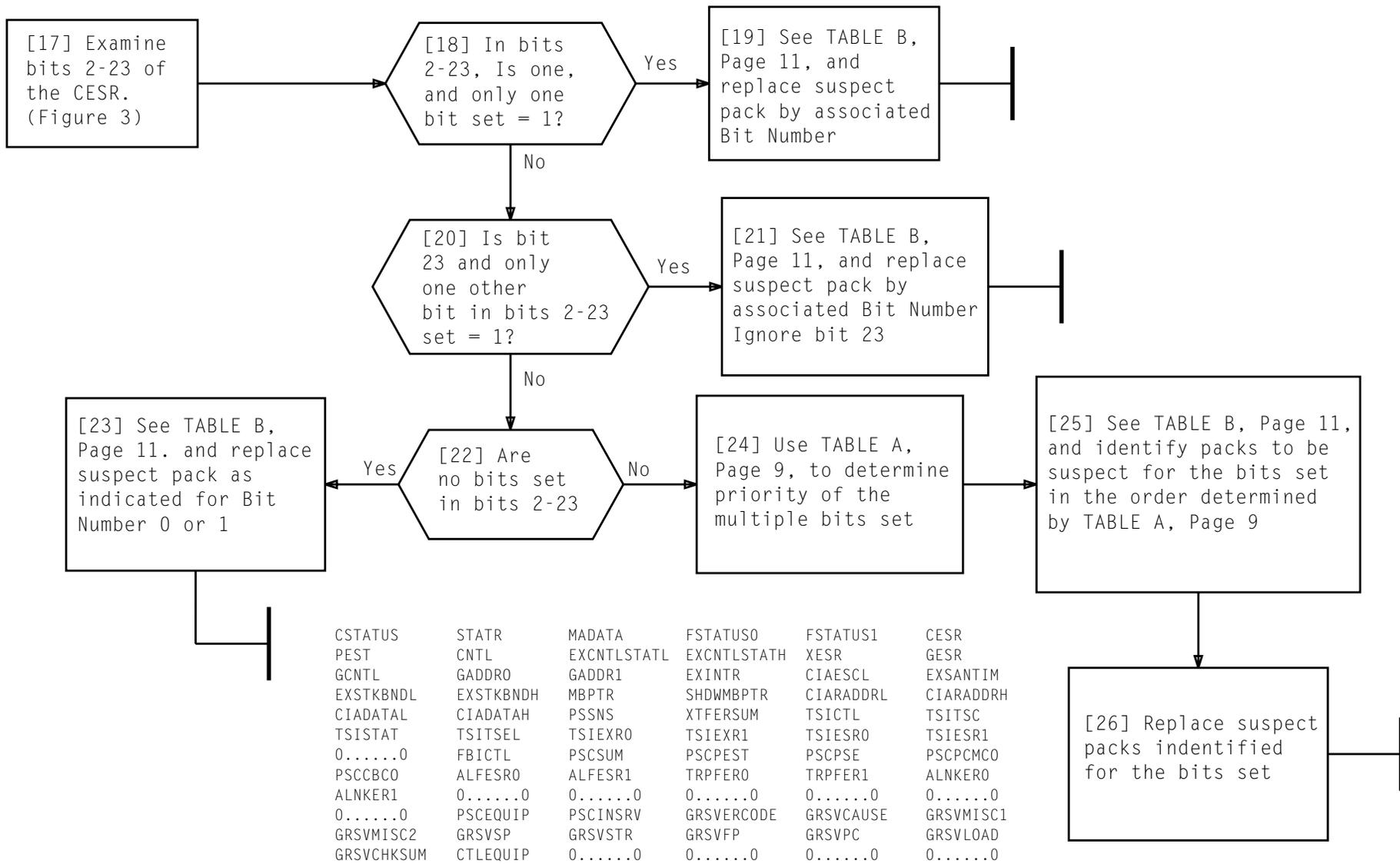
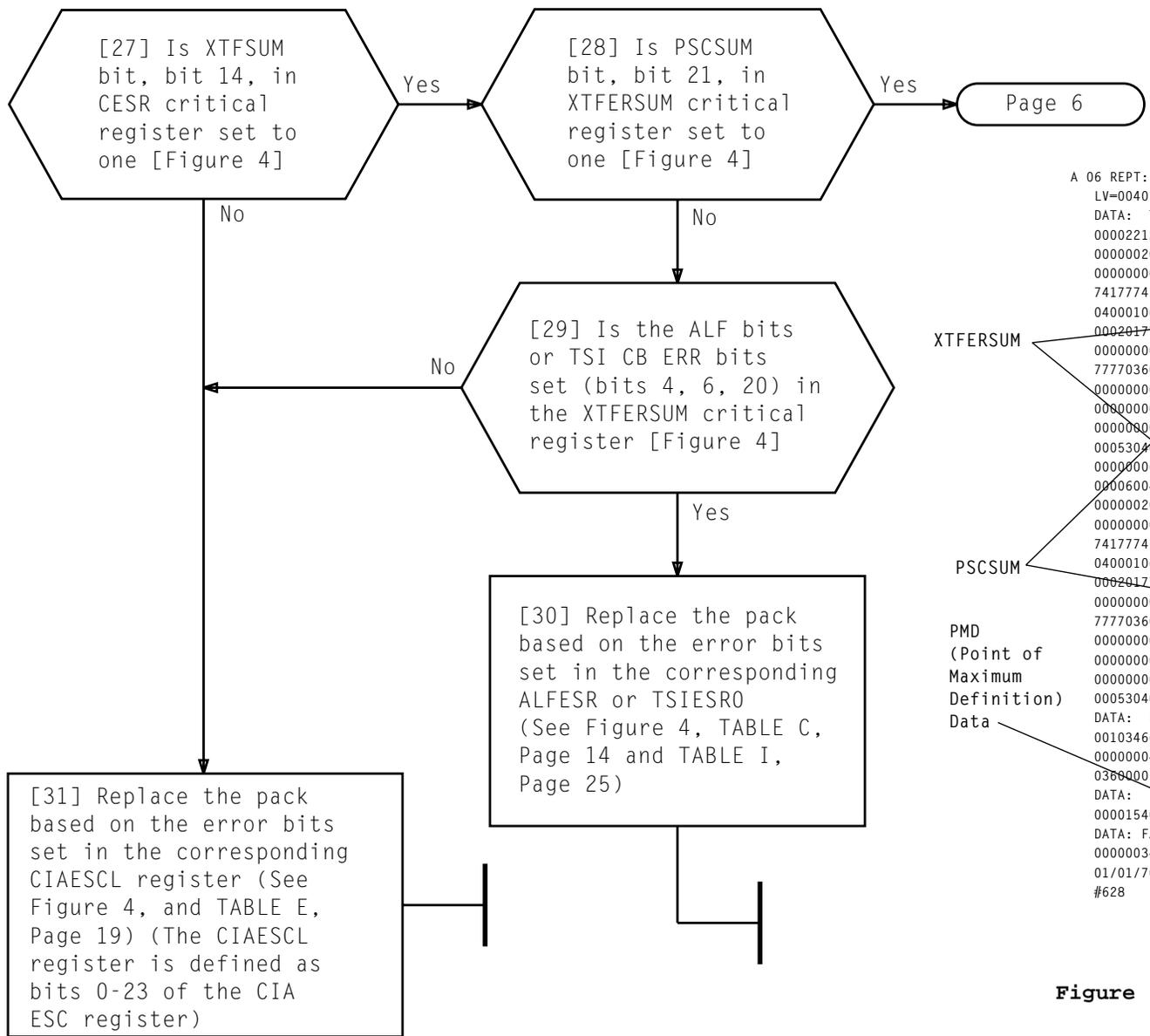


Figure 3 - XTSI Internal Register Layout
(same as Critical Registrar layout on F-level)



```

A 06 REPT: F-LEVEL @52405422 MFNUM=00000010 MICON=40000020 MSG IP
LV=0040 D0=00000002 D1=04000000 D2=00000037 D3=00000200
DATA: TSI CRITICAL REGISTERS
00002212 00002212 00040213 00000000 00000000 00040002 TSIESRO
00000020 00000000 34000243 00000325 00000000 00000000 TSIESR1
00000000 00003000 00000022 00000732 23246400 01331111 CESR
74177741 00000377 43344334 00004334 77776401 00000020 critical
04000106 00000000 00000000 01000000 00000000 00005100 register
00020177 10034140 00000000 00000000 00000100 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
00000006 43777777 55555555 55555555 55555555 55555555
00006004 00006004 00040007 00000000 00000000 00040002
00000020 00000000 34000243 00000325 00000000 00000000 TSIESRO
00000000 00003000 00000022 00000732 23246400 01531452
74177741 00000377 43344334 00004334 77776401 00000020 TSIESR1
04000106 00000000 00000000 01000000 00000000 00005503
00020177 14064140 00000000 00000000 00000000 00000002
00000000 00000000 77770360 77770360 00000000 77770360
77770360 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 41157417 00007417 04000000 00001175 00015541
00000000 00177756 00162621 00000270 00144553 02120003
00053040 00000000 00000000 00000000 00000000 00000000
DATA: PERIPHERAL SYSTEM DATA
00103466 00000003 00000000 00000000 00000000 00000012
00000004 00000012 00000004 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00001540 00001020 01010000 00000020 00000100
DATA: FAULT RECOGNITION ISOLATION DATA
00000034 00000000 00000142 00000000 00000005 00000000
01/01/70 14:06:51
#628
  
```

Figure 4 - XTSI Critical Registers

ANALYZE TNFR F-LEVEL INTERRUPT, EXPANDED TIME-SLOT INTERCHANGE (XTSI)

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[32] Perform an EXCLUSIVE OR (or compare) between Critical Registers PSCSUM and PSCPEST. Any resultant "1s" should indicate a suspect PSC. Replace the pack based on the error bits in the corresponding D3UESR. [See the DUMP that accompanied the interrupt. (See Figure 5 and TABLE H, Page 23).]

```

DUMP
SIZE          PUFR_INT    ER_CODE_H    ER_CODE_L    RTN_ADR_H    RTN_ADR_L
D3UX          D3UX_CSTAT  D3UX_STAT   D3UX_ESR     D3UX_CTL     D3UX_EXR
WTT WD1      WTT WD2      WTT WD3     WTT WD4     WTT WD5     WTT WD6
WTT WD7      WTT WD8     WTT WD9     WTT WD10    WTT WD11    WTT WD12
WTT WD13     WTT WD14    WTT WD15    WTT WD16    WTT WD17    WTT WD18
WTT WD19     WTT WD20    WTT WD21    WTT WD22    WTT WD23    WTT WD24
WTT WD25     WTT WD26    WTT WD27    WTT WD28    WTT WD29    WTT WD30
WTT WD31     WTT WD32    WTT WD33    WTT WD34    WTT WD35    WTT WD36
WTT WD37     WTT WD38    WTT WD39    WTT WD40    WTT WD41    WTT WD42
WTT WD43     WTT WD44    WTT WD45    WTT WD46    WTT WD47    WTT WD48
WTT WD49     WTT WD50    WTT WD51    WTT WD52    WTT WD53    WTT WD54
WTT WD55     WTT WD56    WTT WD57    WTT WD58    WTT WD59    WTT WD60
WTT WD61     WTT WD62    WTT WD63    WTT WD64    WTT WD65    WTT WD66
WTT WD67     WTT WD68    TASK_ID     ERR_DATA1    ERR_DATA2    ERR_DATA3
ERR_DATA4    ERR_DATA5    ERR_DATA6    ERR_DATA7    ERR_DATA8    ERR_DATA9
ERR_DATA10   ERR_DATA11   ERR_DATA12   ERR_DATA13   ERR_DATA14   ERR_DATA15
STACK WD1    STACK WD2    STACK WD3    STACK WD4    STACK WD5    STACK WD6
STACK WD7    STACK WD8    STACK WD9    STACK WD10   STACK WD11   STACK WD12
STACK WD13   STACK WD14   STACK WD15   STACK WD16   STACK WD17   STACK WD18

```

Analysis:

Dump Size-Report Type and Block Size

Octal 00010344

PUFR_INT-Development Only.

ER_CODE_H-High 8-bit of a 32-bits Error Code

Bit 0-7 = Contains the software issue number

ER_CODE_L-Low 24-bit of a 32-bits Error Code

Bit 0-11 = Contains the code (See Codes and Class Layout for values.)

12-15 = Contains the error class (See Error Codes and Class Layout for values.)

16-23 = Number of 32 bit error words reported/found in Auxiliary Data Dump.

The remainder is stack information (up to maximum number of error words).

RTN_ADR_H-Pack Type

Bit 0-8 = D3U Pack type = 1

RTN_ADR_L-Low 24-Bits of Failing Address

Bit 0-23 = Failing Address

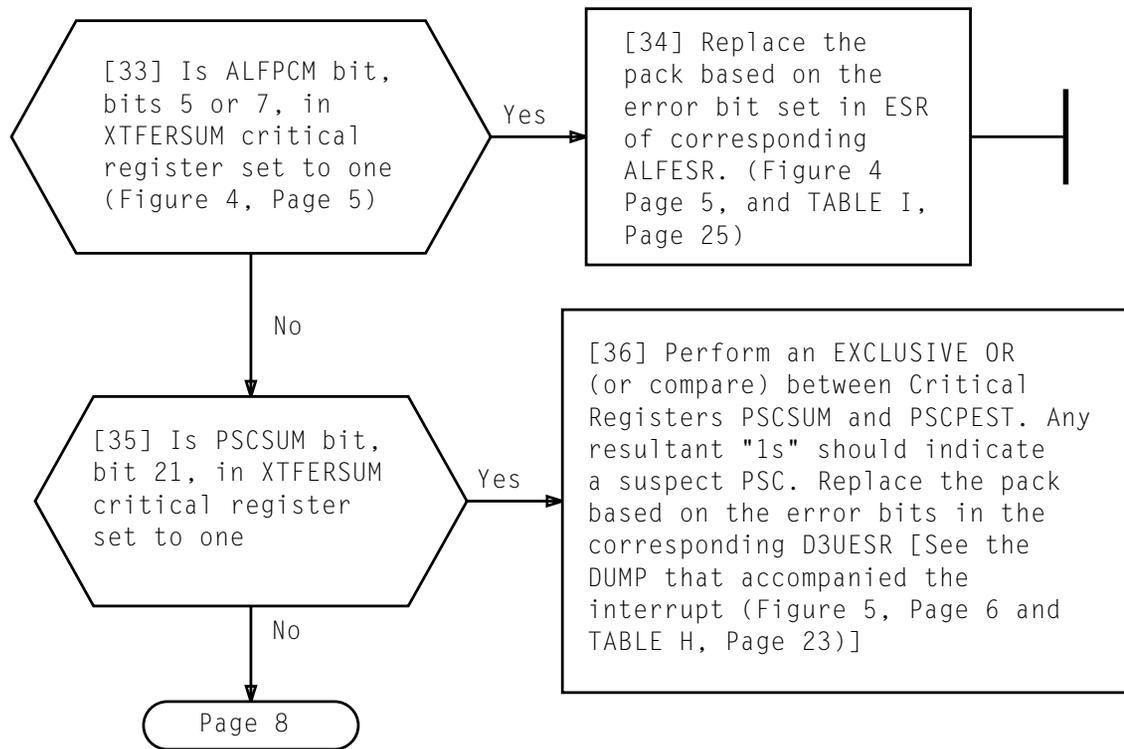
D3UX Subunit-D3U subunit Data

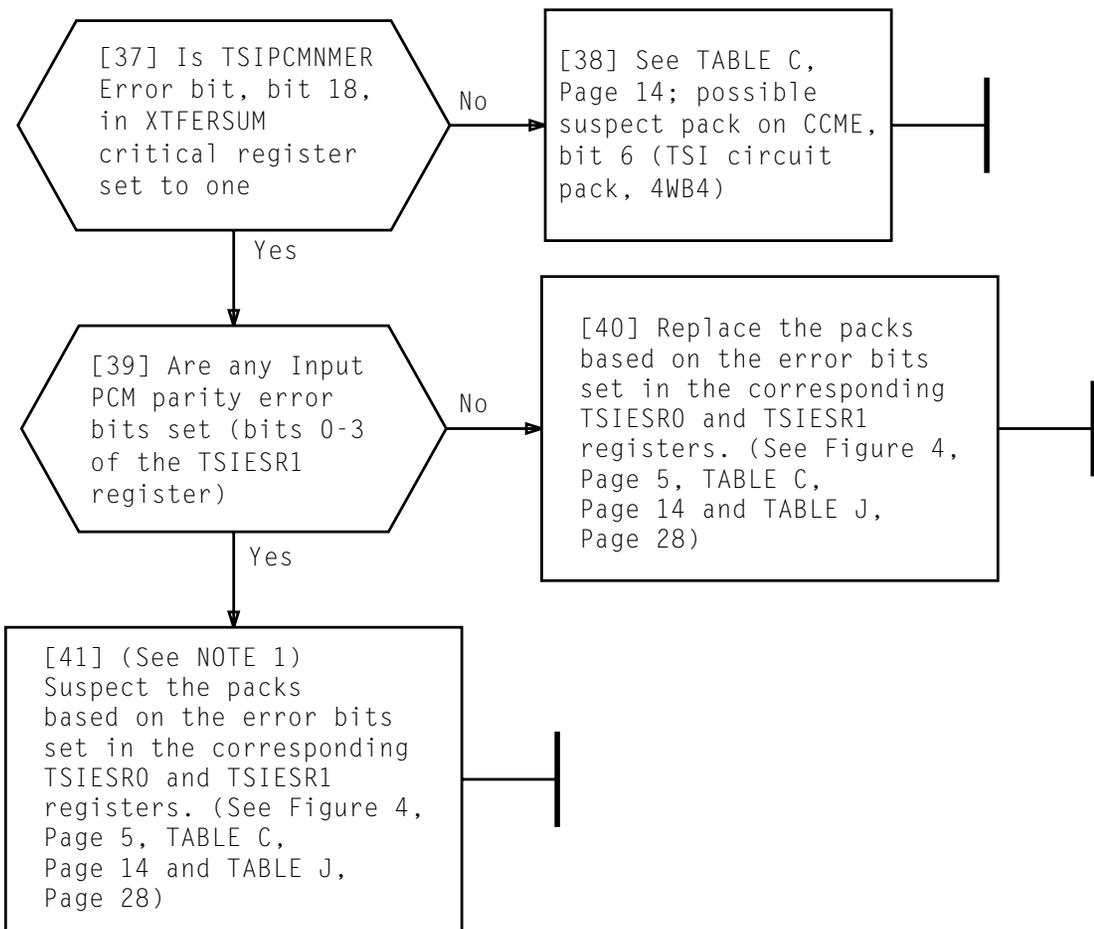
Bit 0-8 = D3U member number (between 0 and 7) (UTMEM)

9-11 = D3U Unit type = 0

12-23 = Unused

Figure 5 - Examples of D3U Shared Memory Auxiliary Data Dump





NOTE 1	
If the error occurs more than once on the same sub-branch (the subunit is the same in the AUX DUMP for all errors), all the circuit packs on the sub-branch should be replaced until the fault disappears	
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TABLE A SUSPECT PRIORITY TABLE AND SUSPECT PACK TABLES				
PRIORITY LEVEL	TYPE OF ERROR	ASSOCIATED ERROR SOURCE REGISTER	SUSPECT BIT(S)	SUSPECT PACK TABLE WITH BIT SET
1	CLOCK ERROR	CESR	15,22	B
		TSIESRO	4,7,8,9	C
2	ACT/STBY ERROR IN HARDWARE	TSIESRO	18	C
		XTFERSUM	22	D
		CESR	10*	B
3	UNRECOVERABLE ERROR	CESR	9	B
4	STACK BOUNDARY ERROR	EXESR	0	E
5	HARD-INIT ERROR	CESR	8	B
6	HARDWARE ERROR	CESR	2,3,6,12,13,19,20,21	B
		CIAESC	1,2,3,4,5,6	F
		GESR	0-3,4-7,8-11,12,13,14	G
		EXESR	2,3,5-12,15	F
7	CONTROL BUS ERROR	CIAESC	7	E
		XTFERSUM	0,1,2,3,4,6,8,16,17	D
8	AUDIT ERROR	CESR	11	B
9	PSC ERROR	CESR	10*	B
		D3UESR	10,11,12,13,14,15,16,17,19	H
* Bit 10 of CESR and GRSVERCODE (Figure 3, Page 4) value of 30, 31, or 32 results in ACT/STBY error in hardware. For other values of GRSVERCODE register, the type of error is PSC error.				

ANALYZE TNFR F-LEVEL INTERRUPT, EXPANDED TIME-SLOT INTERCHANGE (XTSI)

TABLE A (CONTD)				
SUSPECT PRIORITY TABLE AND SUSPECT PACK TABLES				
PRIORITY LEVEL	TYPE OF ERROR	ASSOCIATED ERROR SOURCE REGISTER	SUSPECT BIT(S)	SUSPECT PACK TABLE WITH BIT SET
10	OUTPUT PCM PARITY ERROR	ALFESR	8,9,10,11,12,13	I
		D3UESR	4,5,6,7,8,9	H
11	TSI INPUT PCM PARITY ERROR	TSIESR1	0-3	J
12	TSI PACK ERROR	TSIESR0	10-17,19	C
		TSIESR1	4-23	J
13	ALNK ERROR	ALFESR	16	I
14	ALF LOCAL PCM PARITY ERROR	ALFESR	14,15	I
15	ALF BUSY/IDLE & INTERNAL PARITY ERROR	ALFESR	4,18,19,20,21,22	I
16	TRPF ERROR	ALFESR	17	I
17	PSM BUS MISMATCH ERROR	TSIESR0	6	C
18	SOFTWARE ERROR	CESR	7	B
19	SANITY TIMER	EXESR	1	E
20	CONTROLLER MISMATCH ERROR	CESR	23	B

ANALYZE TNFR F-LEVEL INTERRUPT, EXPANDED TIME-SLOT INTERCHANGE (XTSI)

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TABLE B CONTROLLER ERROR SOURCE REGISTER (CESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	ASWF	All Seems Well Failure	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
1	AINT	Autonomous Interrupt	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
2	PUPFE	Peripheral Unit Bus Even Parity Failure	KBN16 UN559 UN559	052-137 052-164 052-180	061-137 061-164 061-180
3	PUPFO	Peripheral Unit Bus Odd Parity Failure	KBN16 UN559 UN559	052-137 052-172 052-156	061-137 061-172 061-156
4	APUT	Autonomous Peripheral Unit Trouble	KBN16 UN547	052-137 052-082	061-137 061-082
5	SEQERR	Error Detected by PUB Sequencers	KBN16 UN548	052-137 052-114	061-137 061-114
6	UNASOP	Invalid/Unassigned OP-Code	KBN16 UN559 UN548	052-137 052-164 052-114	061-137 061-164 061-114
7	SWERRO	Firmware Error Bit 0, Forces Soft Initialization (Restart at point of error)	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082

TABLE B (CONTD)					
CONTROLLER ERROR SOURCE REGISTER (CESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
8	SWERR1	Firmware Error Bit 1, Forces Hard Initialization (does not clear stable calls)	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
9	SWERR2	Firmware Error Bit 2, Forces Zero Start (clears stable calls)	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
10	SWERR3	Firmware Error Bit 3, PSC Software Detection Error	KBN16 UN548 UN557 UN547 PSCs	052-137 052-114 052-106 052-082 *	061-137 061-114 061-106 061-082 *
11	AUDSUM	Audit Error Source Summary	KBN16 UN548 UN557 UN547 4WB4	052-137 052-114 052-106 052-082 014-098	061-137 061-114 061-106 061-082 031-098
12	MODFL	Mode Failure	KBN16 UN559 UN559	052-137 052-156 052-164	061-137 061-156 061-164
13	PPE	PUB1 Parity Error	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
* See TABLE K for all PSC (D3U) locations.					

TABLE B (CONTD)					
CONTROLLER ERROR SOURCE REGISTER (CESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
14	XTFSUM	XTSI Fabric Error Source Summary	See TABLE D		
15	LCLKF	Local Clock Failure	KBN16 UN548	052-137 052-114	061-137 061-114
16	LASUM	LAN Access Error Source Summary	KBN16 UN548	052-137 052-114	061-137 061-114
17	SPARESUM	Spare Pack Error Source Summary (Future Expansion)	KBN16 UN548	052-137 052-114	061-137 061-114
18	CIASUM	Control Bus and Image Administration Error Source Summary	See TABLE E		
19	GRAMSUM	Global Ram Local Error Source Summary	UN557 KBN16	052-106 052-137	061-106 061-137
20	EXECSUM	EXEC Local Error Source Summary	UN548 KBN16	052-114 052-137	061-114 061-137
21	BPSUM	Backplane Error Source Summary	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082
22	CLKSUM	Clock Error Source Summary	UN548 KBN16 4WB4	052-114 052-137 014-098	061-114 061-137 031-098
23	CCMM	GRAM, EXEC Complex Cross Controller Mismatch	KBN16 UN548 UN557 UN547	052-137 052-114 052-106 052-082	061-137 061-114 061-106 061-082

TABLE C					
TSI ERROR SOURCE REGISTER 0 (TSIESR0)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	CBDPE0	Control Bus Data Write Parity Error for Byte 0	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 031-090 061-082
1	CBDPE1	Control Bus Data Write Parity Error for Byte 1	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 031-090 061-082
2	CBDPE2	Control Bus Data Write Parity Error for Byte 2	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 031-090 061-082
3	CBDPE3	Control Bus Data Write Parity Error for Byte 3	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 031-090 061-082
4	TSCERR	Time-Slot Counter Error. Does Not Match Frame Bit from Network Clock	4WB4	014-098	031-098
5	UNUSED				
6	CCME	Cross-Controller Mismatch Error	4WB4	014-098	031-098
7	NSE	Network Sync Error	4WB4	014-098	031-098
8	PLE	32.768 MHz Phase Lock Error	4WB4	014-098	031-098
9	CSE	32.768 MHz Clock Source Error. 32 MHz Distribution Stuck Low or High	4WB4	014-098	031-098

TABLE C (CONTD)
TSI ERROR SOURCE REGISTER 0 (TSIESR0)

BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
10-13	TSXRMM	Mismatch Error	4WB4	014-098	031-098
14	PCE0	TSXR0 PCM Enable Parity Error	4WB4	014-098	031-098
15	PCE1	TSXR1 PCM Enable Parity Error	4WB4	014-098	031-098
16	PCE2	TSXR2 PCM Enable Parity Error	4WB4	014-098	031-098
17	PCE3	TSXR3 PCM Enable Parity Error	4WB4	014-098	031-098
18	ACTMME	Active/Standby Signal Mismatch Error	4WB4	014-098	031-098
19	BMIMSE	Buffer Memory Input MUX Select Error	4WB4	014-098	031-098
20-23	UNUSED				

TABLE D XTF FABRIC ERROR SUMMARY REGISTER (XTFERSUM)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	WTPERB0	When Set, Indicates a Byte 0 Parity Error Occurred on an FBI Local CB Write	4WB2 UN547	014-090 052-082	031-090 061-082
1	WTPERB1	When Set, Indicates a Byte 1 Parity Error Occurred on an FBI Local CB Write	4WB2 UN547	014-090 052-082	031-090 061-082
2	WTPERB2	When Set, Indicates a Byte 2 Parity Error Occurred on an FBI Local CB Write	4WB2 UN547	014-090 052-082	031-090 061-082
3	WTPERB3	When Set, Indicates a Byte 3 Parity Error Occurred on an FBI Local CB Write	4WB2 UN547	014-090 052-082	031-090 061-082
4	ALFOCBER	When Set, Indicates Any CB Related Error on ALF0	4WB6 4WB2 UN547	014-082 014-090 052-082	- 031-090 061-082
5	ALFOPCMER	When Set, Indicates PCM Related Error on ALF0. Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB6 4WB4	014-082 014-098	- 031-098
6	ALF1CBER	When Set, Indicates any CB related Error on ALF1	4WB6 4WB2 UN547	014-106 014-090 052-082	- 031-090 061-082
7	ALF1PCMER	When Set, Indicates and PCM Related Error on ALF1. Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB6 4WB4	014-106 014-098	- 031-098
8	ALF2CBER	When Set, Indicates any CB related Error on ALF2	4WB6 4WB2 UN547	- 014-090 052-082	031-082 031-090 061-082
9	ALF2PCMER	When Set, Indicates and PCM Related Error on ALF2. Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB6 4WB4	- 014-098	031-082 031-098

TABLE D (CONTD)					
XTF FABRIC ERROR SUMMARY REGISTER (XTFERSUM)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
10	ALF3CBER	When Set, Indicates any CB related Error on ALF3	4WB6 4WB2 UN547	- 014-090 052-082	031-106 031-090 061-082
11	ALF3PCMER	When Set, Indicates and PCM Related Error on ALF3. Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB4 4WB6	- 014-098	031-106 031-098
12	SPARECBER	When Set, Indicates any CB Related Error on the SPARE Controller Client	4WB2 UN547	014-090 052-082	031-090 061-082
13	SPAREPCMER	When Set, Indicates any PCM Related Error on the SPARE Controller Client.	4WB4 4WB6 4WB6	014-098 014-082 014-106	031-098 031-082 031-106
14	TERMOCBER	When Set, Indicates any CB Related Error on the TERMO Controller Client	4WB7 4WB2 4WB6 UN547	014-008 014-090 052-082 052-082	031-008 061-090 061-082 061-082
15	TERMOPCMER	When Set, Indicates any PCM Bus Related Error on the TERMO Controller Client	4WB7 4WB4 4WB6	014-008 014-098 014-082	031-008 031-098 031-082
16	TERM1CBER	When Set, Indicates any CB Related Error on the TERM1 Controller Client	PSCs 4WB2 UN547	* 014-090 052-082	* 061-090 061-082
* See TABLE K for all PSC (D3U) locations.					

TABLE D (CONTD)					
XTF FABRIC ERROR SUMMARY REGISTER (XTFERSUM)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
17	TERM1PCMER	When Set, Indicates Any PCM Bus Related Error on the TERM1 Controller Client	PSCs 4WB4 4WB6 4WB6	* 014-098 014-082 014-106	* 031-098 031-082 031-106
18	TSIPCMNER	When Set, Indicates Any TSI Detected PCM, Error, Can Cause Autonomous Reconfiguration of the A-Link. Latches the Time-Slot Counter on the TSI Board	4WB4 4WB6 4WB6 PSCs	014-098 014-082 014-106 *	031-098 031-082 031-106 *
19	TSIPCMER	When Set, Indicates Any TSI Detected Cross-Controller Mismatch PCM Error	4WB4 4WB6 4WB6	014-098 014-082 014-106	031-098 031-082 031-106
20	TSICBER	When Set, Indicates Any TSI Detected CB Related Error	4WB4 4WB2 UN547	014-098 014-090 052-082	031-098 061-090 061-082
21	PSCSUM	When Set, Indicates That a PSC Error Summary Bit is Set in the PSCERSUM Register	PSCs 4WB4 4WB6 4WB6	* 014-098 014-082 014-106	* 031-098 031-082 031-106
22	ASMMER	When Set, Indicates a Mismatch Between the Duplicated Act./Sty. Signals Within the Local Controller or a Mismatch Between the Act./Sty. State of Controller 0 and The Act./Sty. State of Controller 1 (Act./Act. or Sty./Sty.).	4WB2 KBN16	014-090 052-137	031-090 061-137
23	UNUSED	Can not be Written and is Read as 0			
* See TABLE K for all PSC (D3U) locations.					

TABLE E
CIA ERROR, STATUS AND CONTROL REGISTER (CIAESC)

BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	FLASHPE	FLASH Write Parity Error (Writing Clears Bit 0-7)	UN547	052-082	061-082
1	SDATPE	Source A Data Parity Error	UN547 UN548 UN557 KBN16 4WB6 4WB6 4WB4 PSCs	052-082 052-114 052-106 052-137 014-082 014-106 014-098 *	061-082 061-114 061-106 061-137 031-082 031-106 031-098 *
2	DDATPE	Destination Data Parity Error	UN547	052-082	061-082
3	SMOPE	Source Mode & Offset Parity Error	UN547	052-082	061-082
4	DMOPE	Destination Mode & Offset Parity Error	UN547	052-082	061-082
5	XTFWPE	XTF Client Write Parity Error	UN547 4WB2 4WB6 4WB6 4WB4 PSCs	052-082 014-090 014-082 014-106 014-098 *	061-082 031-090 031-082 031-106 031-098 *
6	XTFRPE	XTF Client Read Parity Error	UN547 4WB2 4WB6 4WB6 4WB4 PSCs	052-082 014-090 014-082 014-106 014-098 *	061-082 031-090 031-082 031-106 031-098 *
7	ESACK	Client SACK Error	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
* See TABLE K for all PSC (D3U) locations.					

TABLE E (CONTD)
CIA ERROR, STATUS AND CONTROL REGISTER (CIAESC)

BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
8-15	LSACK	Last SACK Received. Gives Value of SACK Received During Last CB Transfer	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
16-23	LSACKEXP	Last SACK Expected. Gives Value of SACK Expected During Last CB Transfer	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
24	FLPTR24	Overflow Bit for Left Shifting of CIA Address Register	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
25	FLPTR25	Overflow Bit for Left Shifting of CIA Address Register	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
26	FLSHRST	Toggle this Bit for Hard Reset of the Flash Card	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
27	NRFLR	Near Flash ready. The FLASH Card on this CIA Circuit Pack is ready for Another Access	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
28	SNCFLR	Sync Flash Ready. The FLASH Card on this CIA Circuit Pack is Ready For Another Access	4WB6 4WB6 4WB4 PSCs	014-082 014-106 014-098 *	031-082 031-016 031-098 *
29-31	UNUSED				

* See TABLE K for all PSC (D3U) locations.

TABLE F EXEC ERROR SOURCE REGISTER (EXESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	STKBND	Stack Bounds Error	UN548	052-114	061-114
1	SANTIMEX	Sanity Timer Expiration	UN548	052-114	061-114
2	ILLOC	Illegal Opcode	UN548	052-114	061-114
3	SRCPERR	Source Parity Error	UN548 UN557 KBN16 UN547 4WB6 4WB6 4WB4 PSCs	052-114 052-106 052-137 052-082 014-082 014-106 014-098 *	061-114 061-106 061-137 061-082 031-082 031-106 031-098 *
4	UNUSED				
5-12	MRPE	MicroRAM Parity Error	UN548	052-114	061-114
13-14	UNUSED				
15	SOFTERR	Software Error (causes EXEC ESR bit to be set in PUBI)	UN548	052-114	061-114
16-23	FPEMW	Force Parity Error in Microword			
* See TABLE K for all PSC (D3U) locations.					

TABLE G GRAM ERROR SOURCE REGISTER (GESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0-3	ERAP	RAM Bank A Parity Error	UN557	052-106	061-106
4-7	ERBP	RAM Bank B Parity Error	UN557	052-106	061-106
8-11	EDDP	Destination Bus Address Parity Error	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
12	EDAP	Destination Bus Address Parity Error	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
13	ESAAP	Source Bus A Address Parity Error	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
14	ESBAP	Source Bus B Address Parity Error	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
15	EXUMM	Update Bus Mismatch	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
16	EXSMM	Syndrome Mismatch	UN557 UN548 KBN16 UN547	052-106 052-114 052-137 052-082	061-106 061-114 061-137 061-082
17-23	UNUSED	All zero			

TABLE H
D3U ERROR SOURCE REGISTER (D3UESR)

BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	CBDPE0	Control Bus Data Parity Error, Byte 0	PSCs 4WB2 UN547	* 014-090 052-082	* 031-090 061-082
1	CBDPE1	Control Bus Data Parity Error, Byte 1	PSCs 4WB2 UN547	* 014-090 052-082	* 031-090 061-082
2	CBDPE2	Control Bus Data Parity Error, Byte 2	PSCs 4WB2 UN547	* 014-090 052-082	* 031-090 061-082
3	CBDPE3	Control Bus Data Parity Error, Byte 3	PSCs 4WB2 UN547	* 014-090 052-082	* 031-090 061-082
4	TSCPEE	Time-Slot Count Even Bits Parity Error	PSCs 4WB4	* 014-098	* 031-098
5	TSCPEO	Time-Slot Count Odd Bits Parity Error	PSCs 4WB4	* 014-098	* 031-098
6	PCMBIE0	PCM Out Bus 0 (2) Busy/Idle Error. (PCM Bus Busy/Idle Bits Don't Agree)	PSCs 4WB4	* 014-098	* 031-098
7	PCMBIE1	PCM Out Bus 1 (3) Busy/Idle Error. (PCM Bus Busy/Idle Bits Don't Agree)	PSCs 4WB4	* 014-098	* 031-098
8	PCMOPE0	PCM Out Bus 0 (2) Parity Error	PSCs 4WB4	* 014-098	* 031-098
* See TABLE K for all PSC (D3U) locations.					

TABLE H (CONTD)					
D3U ERROR SOURCE REGISTER (D3UESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
9	PCMOPE1	PCM Out Bus 1 (3) Parity Error	PSCs 4WB4	* 014-098	* 031-098
10	PCMOSEQ	PCM Out Sequence Error	PSCs 4WB4	* 014-098	* 031-098
11	PCMISEQ	PCM In Sequence Error	PSCs 4WB4	* 014-098	* 031-098
12	PCMTCLE	PCM Control-Interface Error (TSC State machine Error)	PSCs 4WB4	* 014-098	* 031-098
13	DS1CLKPE	DS1 Clock Phase Error	PSCs 4WB4	* 014-098	* 031-098
14	CLKPE	33 MHz Clock Phase Error	PSCs 4WB4	* 014-098	* 031-098
15	PHALT	D3U Processor Halt	PSCs 4WB4	* 014-098	* 031-098
16	PBUSE	D3U Processor Bus Error	PSCs 4WB4	* 014-098	* 031-098
17	PPARE	D3U Processor Parity Error	PSCs 4WB4	* 014-098	* 031-098
18	D3USWERR	Software Error. D3U Processor has the Ability to Set this Bit	PSCs 4WB4	* 014-098	* 031-098
19-31	UNUSED	—	—	—	—
* See TABLE K for all PSC (D3U) locations.					

TABLE I ALF ERROR REGISTER (ALFESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	CBDPE0	Indicates a Parity Error was Detected on Data From the CB Byte 0	4WB6 4WB6 4WB2 UN547	014-082 014-106 014-090 052-082	031-082 031-106 031-090 061-082
1	CBDPE1	Indicates a Parity Error was Detected on Data From the CB Byte 1	4WB6 4WB6 4WB2 UN547	014-082 014-106 014-090 052-082	031-082 031-106 031-090 061-082
2	CBDPE2	Indicates a Parity Error was Detected on Data From the CB Byte 2	4WB6 4WB6 4WB2 UN547	014-082 014-106 014-090 052-082	031-082 031-106 031-090 061-082
3	CBDPE3	Indicates a Parity Error was Detected on Data From the CB Byte 3	4WB6 4WB6 4WB2 UN547	014-082 014-106 014-090 052-082	031-082 031-106 031-090 061-082
4	ERIDLWR	Wrote ALFIDLE0 or ALFIDLE1 Without Having the Corresponding Enable Bit Set in ALFCTL	4WB6 4WB6	014-082 014-106	031-082 031-106
5-7	UNUSED				
8	ALFTSCPEE	Indicates a Parity Error was Detected on the TSC Even Bits	4WB6 4WB6 4WB4	014-082 014-106 014-098	031-082 031-106 031-098
9	ALFTSCPEO	Indicates a Parity Error was Detected on the TSC Odd Bits	4WB6 4WB6 4WB4	014-082 014-106 014-098	031-082 031-106 031-098
10	ALFPCMBIE0	Indicates a Parity Error was Detected on PCM Bus Busy/Idle 0	4WB6 4WB6 4WB4	014-082 014-106 014-098	031-082 031-106 031-098

TABLE I (CONTD)					
ALF ERROR REGISTER (ALFESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
11	ALFPCMBIE1	Indicates a Parity Error was Detected on PCM Bus Busy/Idle 1	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
12	ALFPCMOPE0	Indicates a Parity Error was Detected on Data from PCM Output Bus 0	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
13	ALFPCMOPE1	Indicates a Parity Error was Detected on Data from PCM Output Bus 1	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
14	ALFPCMIPE0	Indicates a Parity Error was Detected on Data from PCM Input Bus 0	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
15	ALFPCMIPE1	Indicates a Parity Error was Detected on Data from PCM Input Bus 1	4WB6	014-082	031-082
			4WB6	014-106	031-106
			4WB4	014-098	031-098
16	ALNKSUM	Indicates a Parity Error was Detected in One or More of the 16 A'Link Circuits. ALF Register ALNKPER indicates Which Circuit Detected the Error	4WB6	014-082	031-082
			4WB6	014-106	031-106
			UN546	052-026	061-026
			UN545	052-014	061-014

TABLE I (CONTD)					
ALF ERROR REGISTER (ALFESR)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
17	TRPFSUM	Indicates that a Transmission parity Error (TRPF) was Detected in One or More of the 16 A'Link Circuits. ALF Register TRPFPER Indicates Which Circuit Detected the Error	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
18	BITMAPER0	Indicates a Parity Error was Detected on Data from the Busy/Idle Memory Circuit 0	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
19	BITMAPER1	Indicates a Parity Error was Detected on Data from the Busy/Idle Memory Circuit 1	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
20	BUFOPER	Indicates a Parity Error was Detected on Leading-Ones Detector Buffer Memory 0 Read Address	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
21	BUF1PER	Indicates a Parity Error was Detected on Leading-Ones Detector Buffer Memory 1 Read Address	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
22	DBISUM	Indicates that an Internal Matching Error in the LOD Delayed Busy/Idle Circuit Was Detected (Summary Bit for the DBIER Register)	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014
23	NONE	This Bit Always Reads Zero. A Write to the ALFESR with Bit 23 Causes a 60 NS Pulse That Clears BUF (0/1) Per in the ALFESR	4WB6 4WB6 UN546 UN547	014-082 014-106 052-026 052-014	031-082 031-106 061-026 061-014

TABLE J TSI ERROR SOURCE REGISTER 1 (TSIESR1)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
0	OPCMIPER	PCM 0 Input Parity Error (from Clients)	4WB4 4WB6 PSCs	014-098 014-082 *	031-098 031-082 *
1	1PCMIPER	PCM 1 Input Parity Error (from Clients)	4WB4 4WB6 PSCs	014-098 014-082 *	031-098 031-082 *
2	2PCMIPER	PCM 2 Input Parity Error (from Clients)	4WB4 4WB6 PSCs	014-098 014-106 *	031-098 031-106 *
3	3PCMIPER	PCM 3 Input Parity Error (from Clients)	4WB4 4WB6 PSCs	014-098 014-106 *	031-098 031-106 *
4	TSM0MM	Time-Slot Memory 0 Mismatch Error	4WB4	014-098	031-098
5	TSM1MM	Time-Slot Memory 1 Mismatch Error	4WB4	014-098	031-098
6	TSM2MM	Time-Slot Memory 2 Mismatch Error	4WB4	014-098	031-098
7	TSM3MM	Time-Slot Memory 3 Mismatch Error	4WB4	014-098	031-098
8	PCA0	Time-Slot Memory 0 Address Parity Error	4WB4	014-098	031-098
9	PCA1	Time-Slot Memory 1 Address Parity Error	4WB4	014-098	031-098
10	PCA2	Time-Slot Memory 2 Address Parity Error	4WB4	014-098	031-098
11	PCA3	Time-Slot Memory 3 Address Parity Error	4WB4	014-098	031-098
12	PCD0	Time-Slot Memory 0 Data Parity Error	4WB4	014-098	031-098
* See TABLE K for all PSC (D3U) locations.					

TABLE J (CONTD)					
TSI ERROR SOURCE REGISTER 0 (TSIESR0)					
BIT NUMBER	REGISTER BIT NAME	BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
13	PCD1	Time Slot Memory 1 Data Parity Error	4WB4	014-098	031-098
14	PCD2	Time Slot Memory 2 Data Parity Error	4WB4	014-098	031-098
15	PCD3	Time Slot Memory 2 Data Parity Error	4WB4	014-098	031-098
16	PCB0	Time Slot Memory 0 Busy/Idle Parity Error	4WB4	014-098	031-098
17	PCB1	Time Slot Memory 1 Busy/Idle Parity Error	4WB4	014-098	031-098
18	PCB2	Time Slot Memory 2 Busy/Idle Parity Error	4WB4	014-098	031-098
19	PCB3	Time Slot Memory 3 Busy/Idle Parity Error	4WB4	014-098	031-098
20	BM00PE	Buffer Memory 0 Output Parity Error	4WB4	014-098	031-098
21	BM10PE	Buffer Memory 1 Output Parity Error	4WB4	014-098	031-098
22	BM20PE	Buffer Memory 2 Output Parity Error	4WB4	014-098	031-098
23	BM30PE	Buffer Memory 3 Output Parity Error	4WB4	014-098	031-098

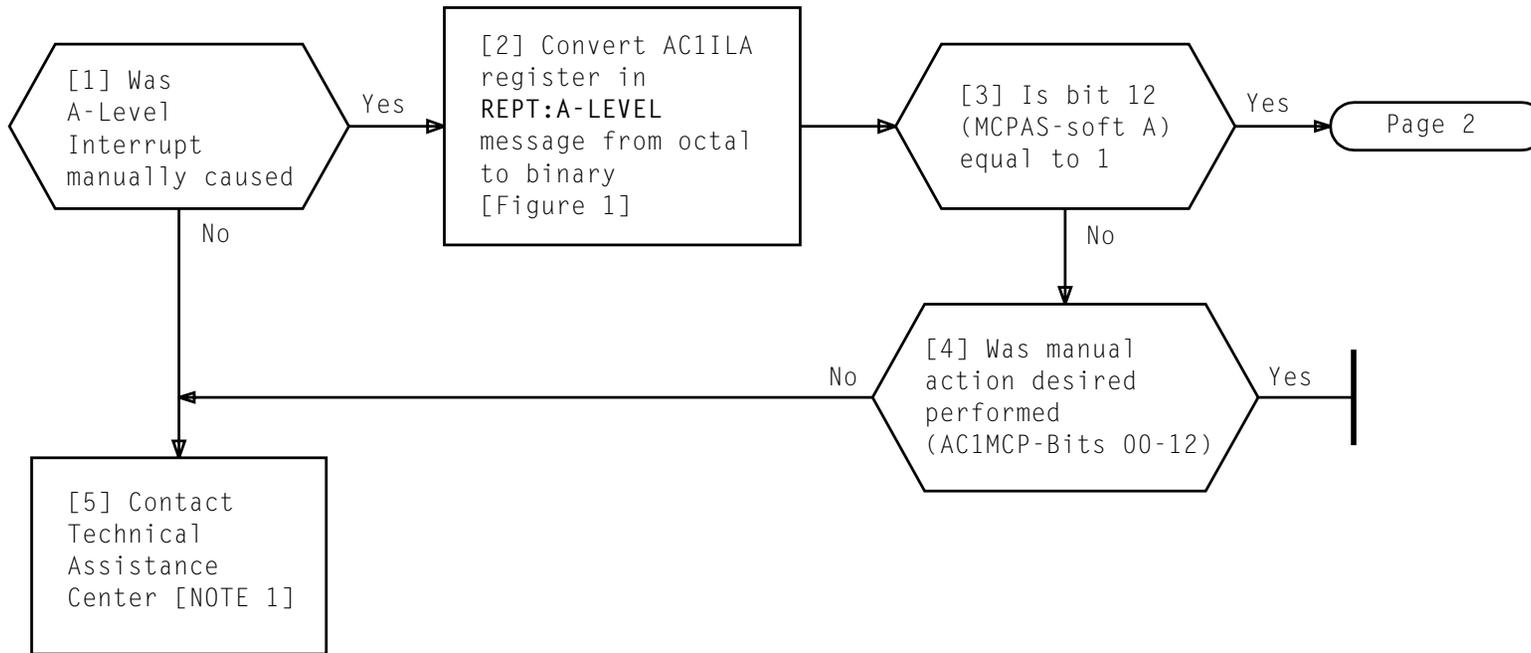
ANALYZE TNFR F-LEVEL INTERRUPT, EXPANDED TIME-SLOT INTERCHANGE (XTSI)

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TABLE K PSC CIRCUIT PACK (D3U) LOCATIONS			
CIRCUIT PACK		LOCATION (Note)	
PSC circuit packs*	D3U Type:	014-016 (PSC Number 00)	014-156 (PSC Number 08)
	4WB3 or	014-024 (PSC Number 01)	014-164 (PSC Number 09)
	4WB11†	014-032 (PSC Number 02)	014-172 (PSC Number 10)
		014-040 (PSC Number 03)	014-180 (PSC Number 11)
Note: Refer to Header Data for appropriate PSC Number * These circuit packs should be replaced one at a time until the trouble is cleared.			

ANALYZE TNFR F-LEVEL INTERRUPT, EXPANDED TIME-SLOT INTERCHANGE (XTSI)

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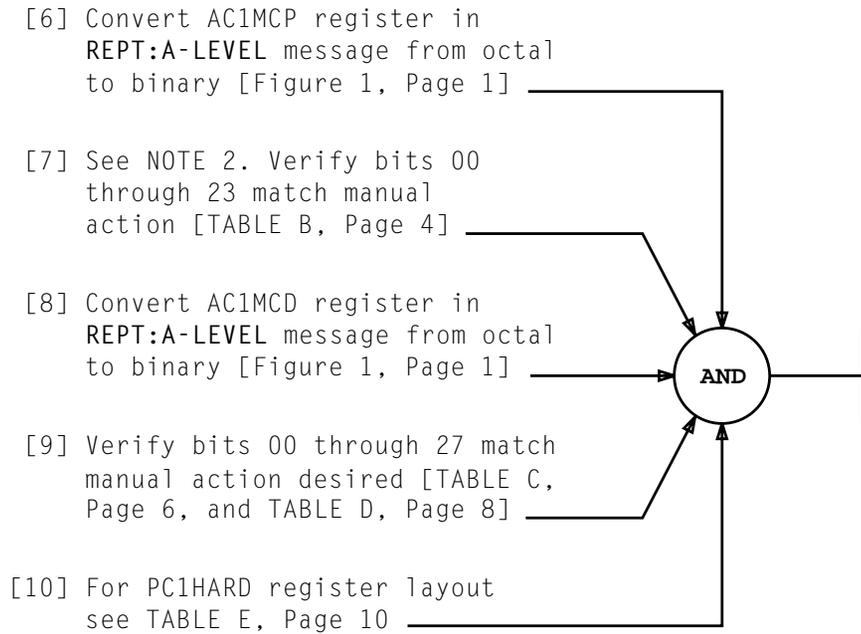
A 18 REPT: A-LEVEL @50124211 MFNUM=00000267 MICON=00000000 MSG STARTED
LV=0401 D0=00001043 D1=00000000 D2=00000000 D3=00000004

DATA: A-LEVEL
00002003 00000004 00000001 00271046 00000177 00030000
41600377 00000002 00000000 00407604 00000077 50124211
50124207 40271051 00100511 00000000 77630074 00000000
00010001 00000100 76010003 00000000 00000000 00000000
00000000 31006251 00000000 00000000 01010000 00001540
00000260 00000000 00000000 00407604 00100600 00000300
00412526 10102000 00000000 00040000 00000177
  
```

AC1ILA AC1MCO AC1MCP AC1MCD(H) AC1MCD(L)

Figure 1 - Sample A-Level Interrupt Message

NOTE 1	
AC1ILA bit 11 (MCCAS) is a hard A and bit 13 (UTAS) is a utility A level.	
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NOTE 2	
When bit 08 equals 1 in MCP register, MCD register specifies DIRECT DATA INSERT used and corresponding bit in INH register is set to one	
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**TABLE A
MCO LAYOUT**

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	MNEMONIC FOR CC REGISTER OR GROUP	OCTAL ADDRESS (7 LEAST SIGNIFICANT BITS)	DESCRIPTION	COMPOOL MNEMONIC
MCO		MC0013		MCC OVERRIDE REGISTER	MCO
MCCCC0		00MC0013		FORCE CC0 ACTIVE	MCCCC0
MCCCC1	01			FORCE CC1 ACTIVE	MCCCC1
MCCPS0	02			LOAD PROGRAM STORE 0	MCCPS0
MCCPS1	03			LOAD PROGRAM STORE 1	MCCPS1
	04				
	05				
MCCPSB0	06			CONFIG ACTIVE CC TO USE PSB 0	MCCPSB0
MCCPSB1	07			CONFIG ACTIVE CC TO USE PSB 1	MCCPSB1
MCCCSB0	08			CONFIG ACTIVE CC TO USE CSB 0	MCCCSB0
MCCCSB1	09			CONFIG ACTIVE CC TO USE CSB 1	MCCCSB1
MCCIFB0	10			CONFIG ACTIVE CC TO USE IFB 0	MCCIFB0
MCCIFB1	11			CONFIG ACTIVE CC TO USE IFB 1	MCCIFB1
MCCFS0	12			CONFIG SYSTEM TO USE FILE SERVER 0	MCCFS0
MCCFS1	13			CONFIG SYSTEM TO USE FILE SERVER 1	MCCFS1
MCLFD	14			LOAD SYSTEM FROM DISK	MCLFD
MCLFTN	15			LOAD SYSTEM FROM TAPE NORMAL MODE	MCLFTN
MCLFTU	16			LOAD SYSTEM FROM TAPE UTILITY MODE	MCLFTU
MCAOVR	17			NOT USED	
MCAUTL	18			NOT USED	
MCAREQ	19			NOT USED	
UTILMAT	20			UTILITY MATCHER GENERATED A-LEVEL	UTILMAT
MCSRDDY	21			SR READY FROM TUC	MCSRDDY
	22				
	23	MC0013			

**TABLE B
MCP LAYOUT**

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	MNEMONIC FOR CC REGISTER OR GROUP	OCTAL ADDRESS (7 LEAST SIGNIFICANT BITS)	DESCRIPTION	COMPOOL MNEMONIC
MCP		MCP012		MCC A-LEVEL PROGRAM REQUEST REG	MCP
MCP R1		00MCP012		MCC PROGRAM REQUEST PHASE 1	MCP R1
MCP R2	01				MCP R2
MCP R3	02				MCP R3
MCP R4	03				MCP R4
MCP R5	04				MCP R5
MCP R6	05				MCP R6
MCINB	06			MCC INHIBIT INTERRUPT SOURCES	MCINB
MCUTL	07			MCC CLEAR UTILITY MATCH CONDITION	MCUTL
MCP A1	08			MCC AUX. PROG. BIT 1	MCP A1
MCP A2	09			MCC AUX. PROG. BIT 2	MCP A2
MCP A3	10			MCC AUX. PROG. BIT 3	MCP A3
MCP A4	11			MCC AUX. PROG. BIT 4	MCP A4
MCP A5	12			MCC AUX. PROG. BIT 5	MCP A5
MCRNORM	13			RESTORE SYSTEM FROM NORMAL PROGRAM FILE	MCRNORM
MCRUPD	14			RESTORE SYSTEM FROM UPDATE PROGRAM FILE	MCRUPD
UTILINF	15			UTILITY INTERFERENCE SWITCH	UTILINF
ACTACT	16			FORCE BOTH MCC/UTILITY PROCESSORS ACTIVE	ACTACT
MUPAA	17			MUP IN ACTIVE-ACTIVE STATUS	MUPAA
MUPAPE	18			MUI ADDRESS PARITY ERROR	MUPAPE
MUPDPE	19			MUI DATA PARITY ERROR	MUPDPE
MUPADD	20			MUI DETECTED BAD ADDRESS	MUPADD
FOREN	21			FORCE ENABLE FLIP-FLOP	FOREN
MC3	22			MC3 RELAY IN NMDCF-READ ONLY	MC3
MUACT	23	012		NEAR MUP ACTIVE	MUACT

TABLE B (Contd)		
MCP LAYOUT		
FMUACT	24MCP012	FAR MUP ACTIVE
SOMNR	25	SET OFFICE MINOR ALARM RESPONSE
SOMJR	26	SET OFFICE MAJOR ALARM RESPONSE
SOCAR	27	SET OFFICE CRITICAL ALARM RESPONSE
RALMS	28	RETIRE ALL ALARMS
SMC	29	SET MACHINE CONGESTION
SDOCT	30	SET DOC TEST
RDOT	31	READ DOC TEST

VERIFY A-LEVEL INTERRUPT REQUEST

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TABLE C
MCD LAYOUT (PCR/PHASE)

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	MNEMONIC FOR CC REGISTER OR GROUP	OCTAL ADDRESS (7 LEAST SIGNIFICANT BITS)	DESCRIPTION
MCD		MCD014		MCC INPUT DATA REGISTER
KEY00		00MCD014		MCC DATA REGISTER 0 - LEAVE ALL PESTS SET AFTER PHASE
KEY01	01			MCC DATA REGISTER 1 - MANUAL ROLLBACK TO TAPE 1
KEY02	02			MCC DATA REGISTER 2 - MANUAL ROLLBACK TO TAPE 2
KEY03	03			MCC DATA REGISTER 3 - MANUAL ROLLBACK OF A NUMBER OF ORDERS
KEY04	04			MCC DATA REGISTER 4 - MANUAL ROLLBACK TO AN ORDER NUMBER
KEY05	05			MCC DATA REGISTER 5 - ZERO ALL SPECIFIED AREAS OF DISK
KEY06	06			MCC DATA REGISTER 6 - CLEAR NTKW MGMT CONTROLS
KEY07	07			MCC DATA REGISTER 7 - INITIALIZE TRK OOS LIST
KEY08	08			MCC DATA REGISTER 8 - RESERVED
KEY09	09			MCC DATA REGISTER 9 - RESERVED
KEY10	10			MCC DATA REGISTER 10 - RESERVED
KEY11	11			MCC DATA REGISTER 11 - RESTORE ALL DUPLEX FAILED CONTROLLERS
KEY12	12			MCC DATA REGISTER 12 - SPARE
KEY13	13			MCC DATA REGISTER 13 - SPARE
KEY14	14			MCC DATA REGISTER 14 - ALLOW DUPLEX FAIL PUBB
KEY15	15			MCC DATA REGISTER 15 - MULTIPLE TAPE SR
KEY16	16			MCC DATA REGISTER 16 - ZERO ALL MEMORY
KEY17	17			MCC DATA REGISTER 17 - SKIP HASHSUM CALCULATION
KEY18	18			MCC DATA REGISTER 18 - BYPASS CC SANITY TESTS
KEY19	19			MCC DATA REGISTER 19 - INHIBIT TAPE ERROR CORRECTION
KEY20	20			MCC DATA REGISTER 20 - INHIBIT MAP AUDITS
KEY21	21			MCC DATA REGISTER 21 - INHIBIT STORE ACCESS TESTS
KEY22	22			MCC DATA REGISTER 22 - READ AND VERIFY DISK DATA IN SR
KEY23		23MCD014		MCC DATA REGISTER 23 - ALW DUPLEX APS FAILURE IN SR

TABLE C (Contd)
MCD LAYOUT (PCR/PHASE)

KEY24	24MCD014	MCC DATA REGISTER 24 – SKIP MUP RESTART DURING PC/SR
KEY25	25	MCC DATA REGISTER 25 – ALLOW MUP SUPERVIORY MODE UTIL SR
KEY26	26	MCC DATA REGISTER 26 – INHIBIT IFB ACCESS TESTS
KEY27	27	MCC DATA REGISTER 27 – INHIBIT AUTOMATIC DIAGNOSTICS
KEY28	28	MCC DATA REGISTER 28 – SPARE
KEY29	29	MCC DATA REGISTER 29 – SPARE
KEY30	30	MCC DATA REGISTER 30 – SPARE
KEY31	31	MCC DATA REGISTER 31 – SPARE

VERIFY A-LEVEL INTERRUPT REQUEST

TABLE D
MCD LAYOUT (INHIBIT INTERRUPT)

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	MNEMONIC FOR CC REGISTER OR GROUP	OCTAL ADDRESS (7 LEAST SIGNIFICANT BITS)	DESCRIPTION
MCD		MCD014		MCC INPUT DATA REGISTER
KEY00		00MCD014		MCC DATA REGISTER 0 – NOT USED
KEY01	01			MCC DATA REGISTER 1 – NOT USED
KEY02	02			MCC DATA REGISTER 2 – NOT USED
KEY03	03			MCC DATA REGISTER 3 – G LEVEL MATCHER
KEY04	04			MCC DATA REGISTER 4 – F LEVEL AUTONOMOUS PERIPHERAL (APUFS)
KEY05	05			MCC DATA REGISTER 5 – F LEVEL PERIPHERAL ORDERS (PUFS)
KEY06	06			MCC DATA REGISTER 6 – E LEVEL PROGRAM STORES
KEY07	07			MCC DATA REGISTER 7 – D LEVEL STACK UNDER/OVERFLOW
KEY08	08			MCC DATA REGISTER 8 – D LEVEL PROTECTED AREA WRITE
KEY09	09			MCC DATA REGISTER 9 – D LEVEL INTERFACE BUS
KEY10	10			MCC DATA REGISTER 10 – D LEVEL CALL STORES
KEY11	11			MCC DATA REGISTER 11 – B LEVEL PULSE POINTS
KEY12	12			MCC DATA REGISTER 12 – A LEVEL UTILITY
KEY13	13			MCC DATA REGISTER 13 – D LEVEL INVALID INSTRUCTION/ADDRESS
KEY14	14			MCC DATA REGISTER 14 – B LEVEL INTERNAL ERROR
KEY15	15			MCC DATA REGISTER 15 – UNUSED
KEY16	16			MCC DATA REGISTER 16 – UNUSED
KEY17	17			MCC DATA REGISTER 17 – K LEVEL SOURCE 0
KEY18	18			MCC DATA REGISTER 18 – UNUSED
KEY19	19			MCC DATA REGISTER 19 – UNUSED
KEY20	20			MCC DATA REGISTER 20 – UNUSED
KEY21	21			MCC DATA REGISTER 21 – UNUSED
KEY22	22			MCC DATA REGISTER 22 – F LEVEL PERIPHERAL ASW ERROR
KEY23	23	23MCD014		MCC DATA REGISTER 23 – F LEVEL PERIPHERAL ANSWER PARITY

VERIFY A-LEVEL INTERRUPT REQUEST

TABLE D (Contd)		
MCD LAYOUT (INHIBIT INTERRUPTS)		
KEY24	24MCD014	MCC DATA REGISTER 24 – UNUSED
KEY25	25	MCC DATA REGISTER 25 – UNUSED
KEY26	26	MCC DATA REGISTER 26 – UNUSED
KEY27	27	MCC DATA REGISTER 27 – UNUSED
KEY28	28	MCC DATA REGISTER 28 – UNUSED
KEY29	29	MCC DATA REGISTER 29 – UNUSED
KEY30	30	MCC DATA REGISTER 30 – UNUSED
KEY31	31	MCC DATA REGISTER 31 – UNUSED

TABLE E
PC1HARD LAYOUT

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	HARDWARE STATUS SELECTION FROM OVERRIDE OR PC STATE
CC0	00	CC0 IS TO BE USED
CC1	01	CC1 IS TO BE USED
PS0	02	PS0 IS TO BE USED
PS1	03	PS1 IS TO BE USED
	04	
	05	
PSB0	06	PSB0 IS TO BE USED
PSB1	07	PSB1 IS TO BE USED
CSB0	08	CSB0 IS TO BE USED
CSB1	09	CSB1 IS TO BE USED
IFB0	10	IFB0 IS TO BE USED
IFB1	11	IFB1 IS TO BE USED
AUB0	12	AUB0 AND API0 IS TO BE USED
AUB1	13	AUB1 AND API1 IS TO BE USED
	14	
	15	
	16	
	17	
	18	
	19	
	20	
RPPC	21	THIS IS A REPEATED PC
PSX	22	USE STORE NOT ACTIVE IN LAST STATE

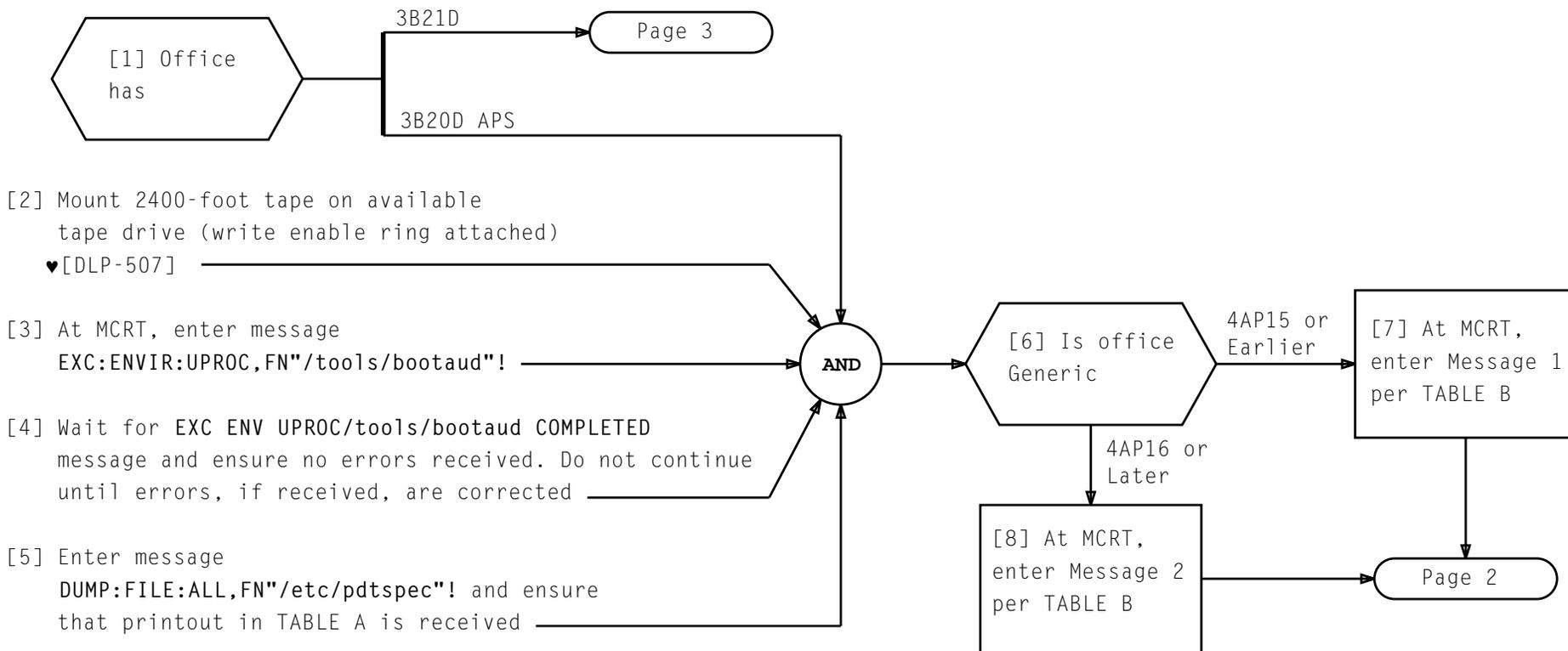


TABLE A	
MESSAGE NUMBER	OUTPUT MESSAGE
1	DUMP FILE ALL COMPLETED /dev/lboot /dev/vtoc /dev/boot /dev/bboot /dev/root /dev/etc /dev/db /dev/amafiles /dev/amabfiles

TABLE B	
MESSAGE NUMBER	INPUT MESSAGES
1	COPY:BKDISK;START:SRC"/dev/vtoc",TD"/dev/mtX8",TPSIZE 2200!
2	COPY:BKDISK;START:SRC"/devv/toc',TD"/dev/mtX8",TPSIZE 2200,COM!
X = tape drive number used in Step 2	

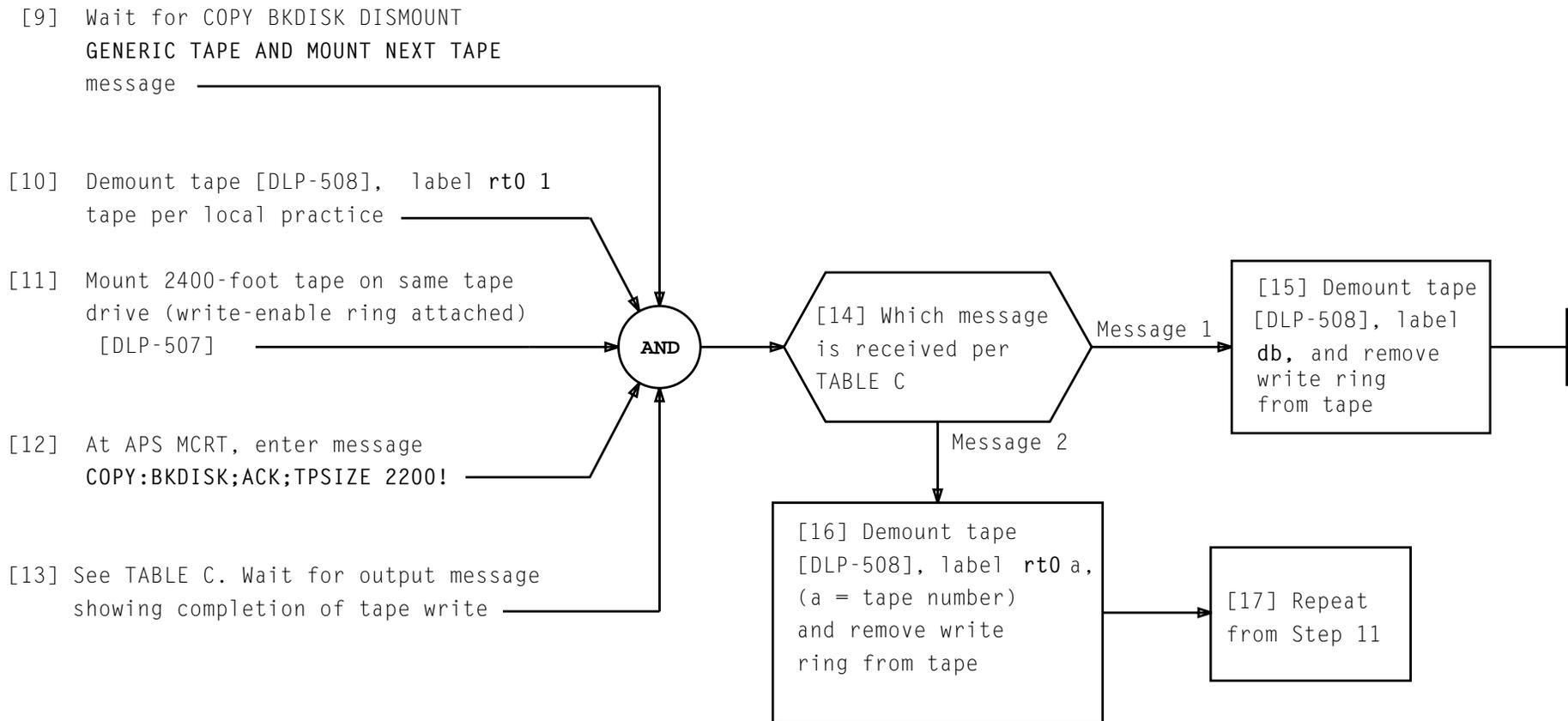


TABLE C	
MESSAGE NUMBER	OUTPUT MESSAGE
1	COPY BKDISK COMPLETED DISMOUNT DATABASE TAPE AND LABEL
2	COPY DISMOUNT GENERIC TAPE LABEL AND MOUNT NEXT TAPE

[18] Insert blank or erasable 4-mm tape with write-protect tab is up (unlocked) position into available 3B21 APS DAT unit [DLP-507]

[19] At 3B21 APS MCRT, enter message `DUMP:FILE:ALL, FN"/etc/pdtspec"` to dump the `/etc/pdtspec` file

[20] Wait for `DUMP FILE ALL COMPLETED` message and ensure that printout in TABLE D is received

[21] At 3B21 APS MCRT, enter message `COPY:DKDISK;START;START;SRC"/dev/vtoc",TD"/dev/mtX0",TPSIZE 90,COM!` [Where X = DAT unit number with backup tape inserted (0 or 1)]

[22] Wait for `COPY DKDISK DISMOUNT GENERIC TAPE LABEL AND MOUNT NEXT TAPE` message

[23] Remove tape from DAT unit [DLP-508], label the tape `rt0 1`, and put write-protect tab in down (locked) position

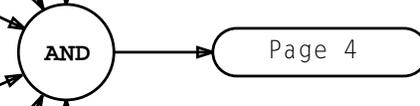
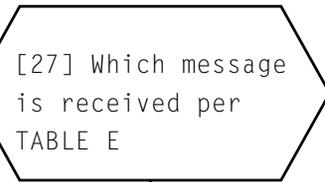
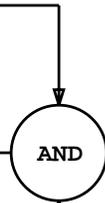


TABLE D	
MESSAGE NUMBER	OUTPUT MESSAGE
1	DUMP FILE ALL COMPLETED /dev/lboot /dev/lboot21 /dev/vtoc /dev/boot /dev/bboot /dev/root /dev/etc /dev/db /dev/amafiles /dev/amabfiles

[24] Insert blank or erasable 4-mm tape, with write-protect tab in up (unlocked) position, into same available 3B21 APS DAT unit [DLP-507]

[25] At APS MCRT, enter message COPY:BKDISK;ACK;TPSIZE 90,COM!

[26] See TABLE E. Wait for output message showing completion of tape write



[28] Demount tape [DLP-508], label db, and remove write ring from tape

[29] Demount tape [DLP-508], label rt0 a, (a = tape number) and remove write ring from tape

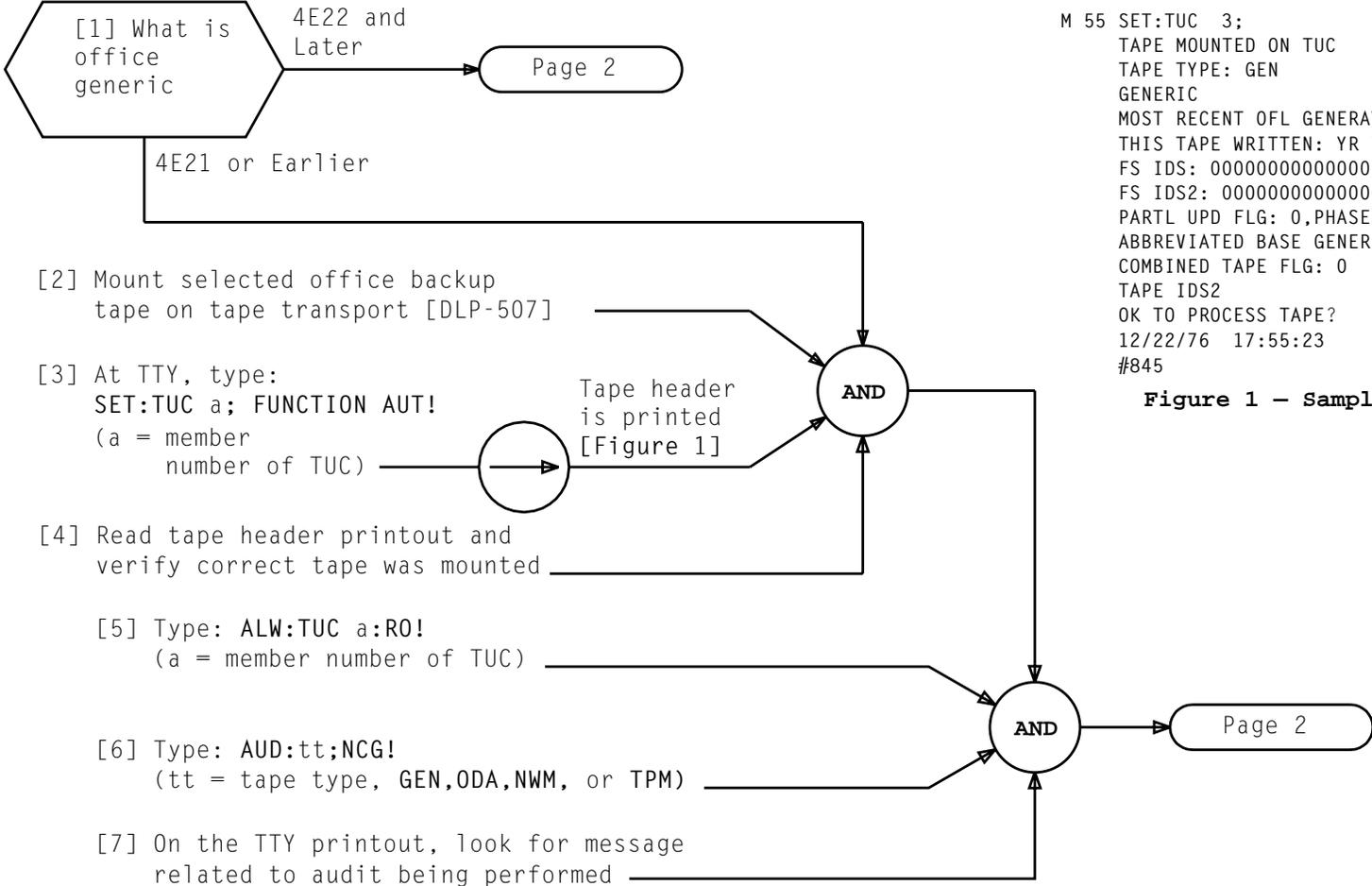
[30] Repeat from Step 24

TABLE E	
MESSAGE NUMBER	OUTPUT MESSAGE
1	COPY BKDISK COMPLETED DISMOUNT DATABASE TAPE AND LABEL
2	COPY DISMOUNT GENERIC TAPE LABEL AND MOUNT NEXT TAPE

SUMMARY

On idle tape transport, select and mount tape containing data to be audited. Input appropriate message to allow tape audit (SAST) to run in noncorrecting mode. Observe TTY for output messages.

When output message indicates **AWAIT INSTRUCTION**, system waits 30 minutes for response before timing out. Analyze output message; and when appropriate, run audit in correction mode; correct errors; or type **STOP:AUD** message to clear tape audit program.



```

M 55 SET:TUC 3;
TAPE MOUNTED ON TUC
TAPE TYPE: GEN
GENERIC
MOST RECENT OFL GENERATION: YR 76,MON 09,DAY 01 AT 19:23
THIS TAPE WRITTEN: YR 76,MON 0/9,DAY 0/1 AT 19:23
FS IDS: 0000000000000010,TAPE IDS 0000000011111111
FS IDS2: 0000000000000010
PARTL UPD FLG: 0,PHASE REQD: 0000100
ABBREVIATED BASE GENERIC:
COMBINED TAPE FLG: 0
TAPE IDS2
OK TO PROCESS TAPE?
12/22/76 17:55:23
#845
  
```

Figure 1 - Sample Tape Audit Header Printout

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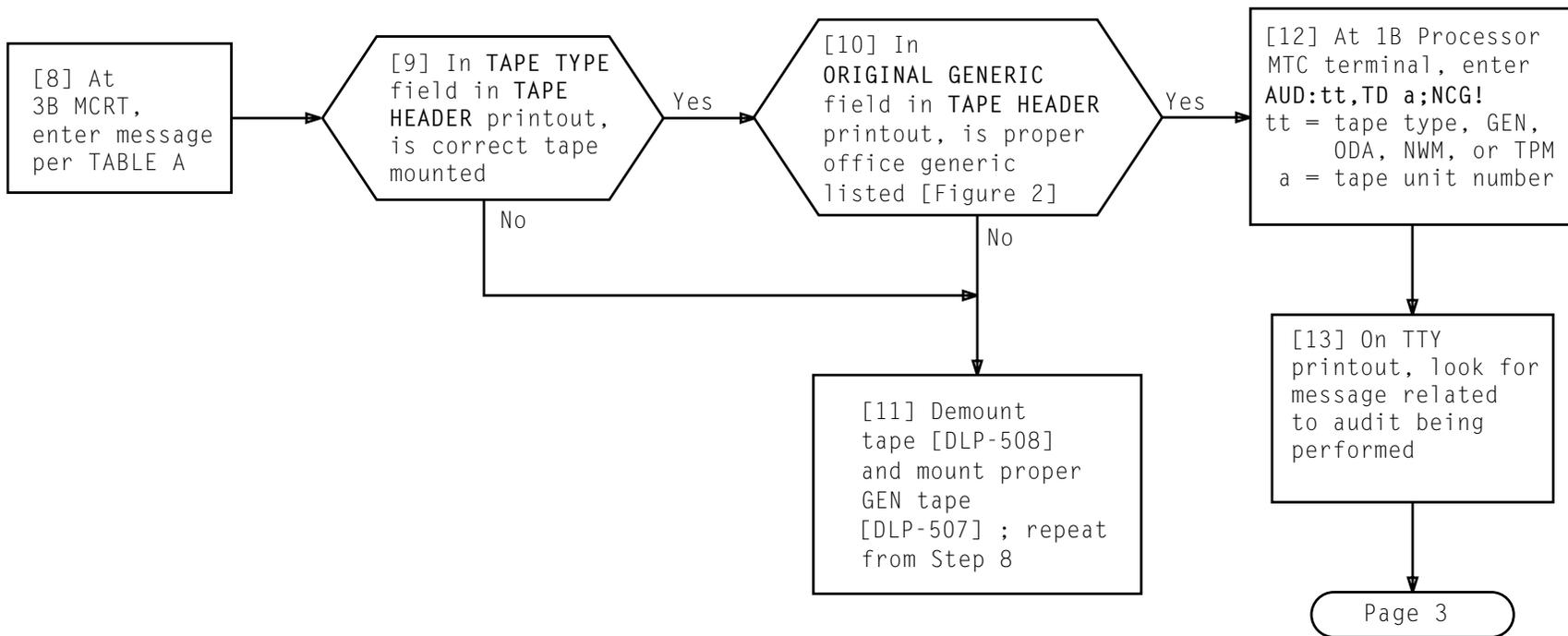


TABLE A	
MESSAGE NUMBER	INPUT MESSAGE
1	VER:UPDATE:TAPE,MT a
a = Tape unit number that GEN tape is mounted	

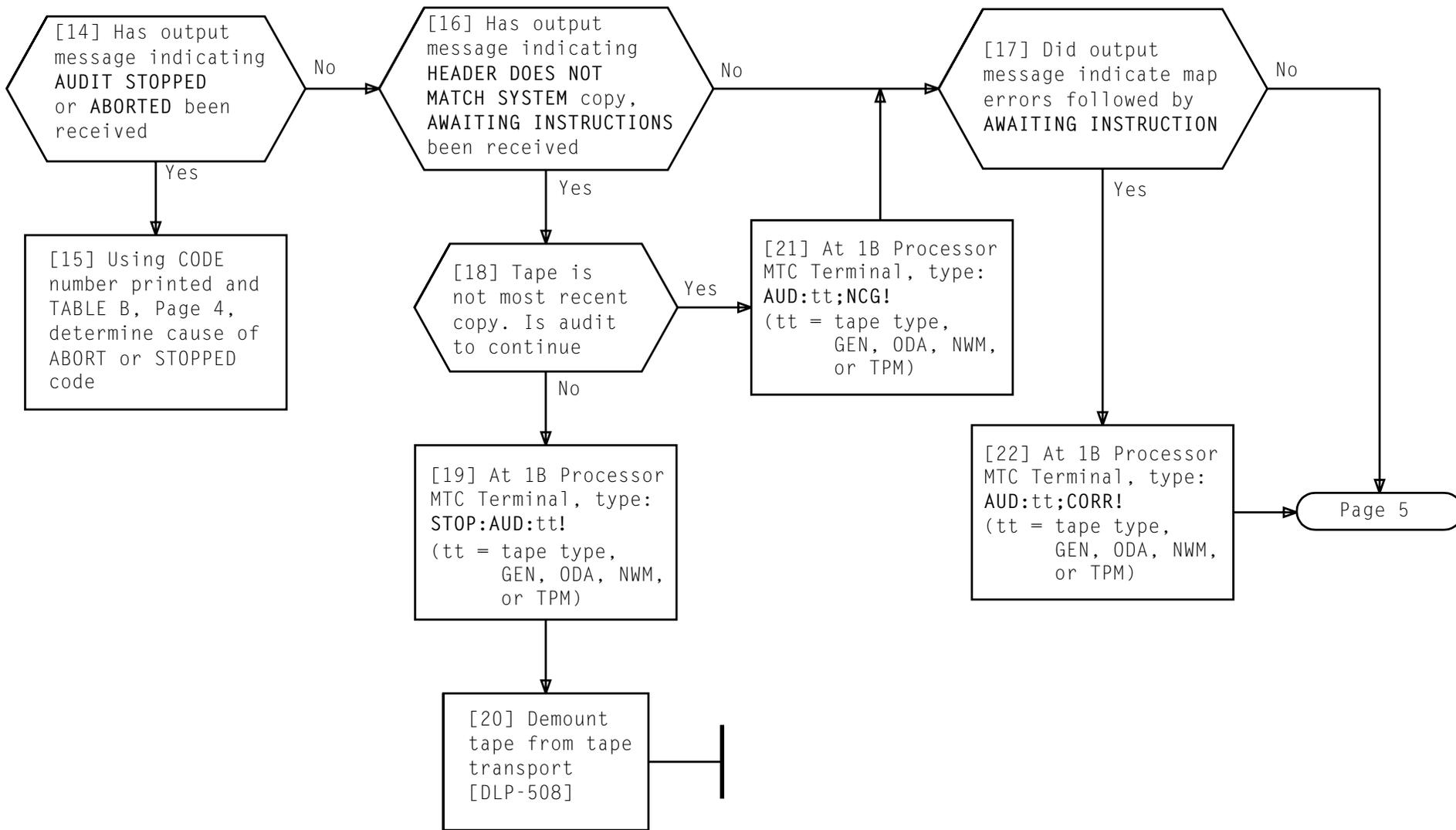
```

TAPe HEADER
TAPe TYPE: GEN
ORIGINAL GENERIC 4E<22>5A.00 R1
MOST RECENT OFL GENERATION: . . . . .
THIS TAPE WRITTEN: . . . . .
FS IDS: . . . . .
PARTL UPD FLG: . . . . .
  
```

THIS VALUE MUST BE SAME AS GENERIC OFFICE IS RUNNING ON

Figure 1 - Example of TAPE HEADER Printout

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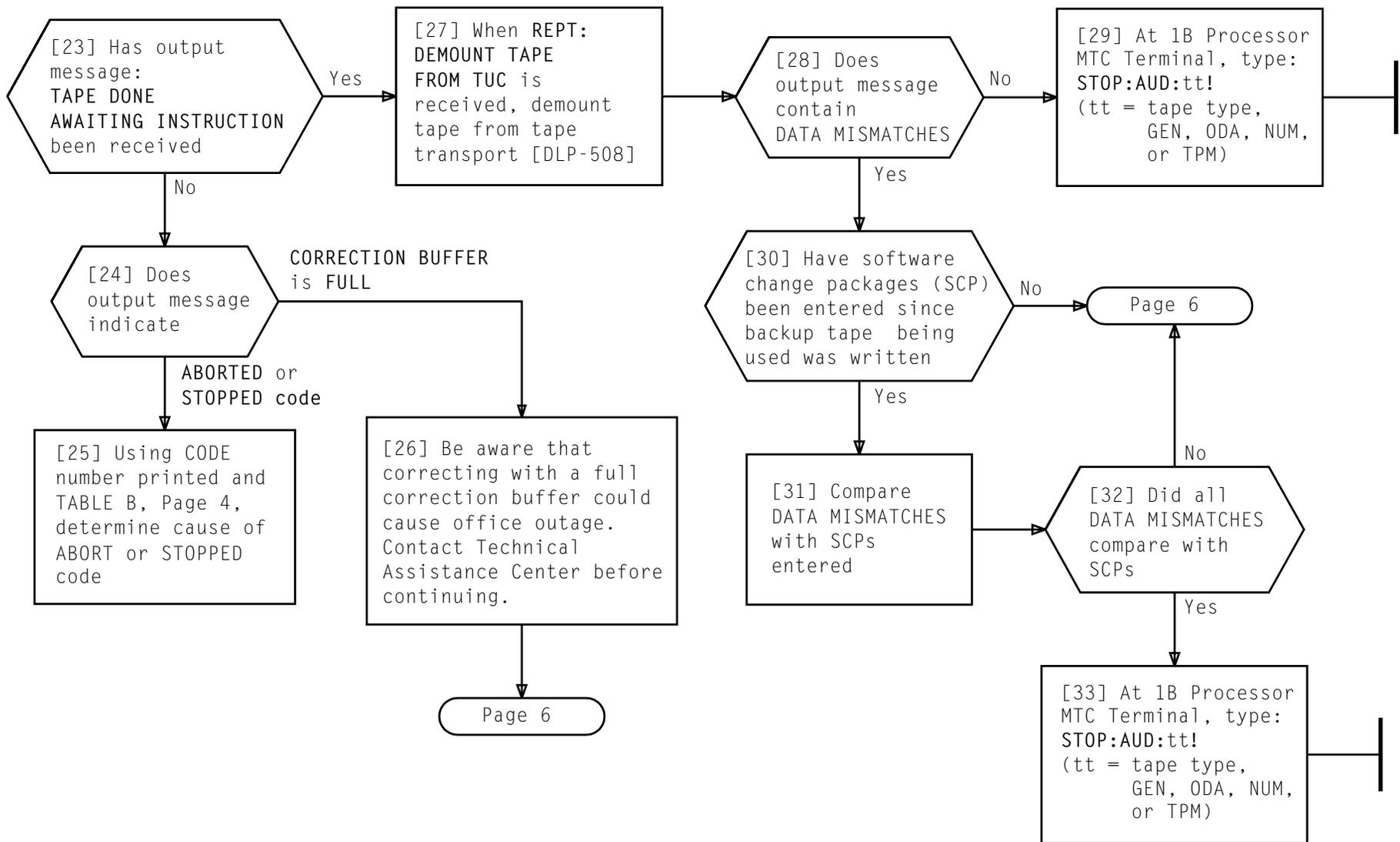


PERFORM TAPE AUDIT OF WRITABLE STORES (SAST)

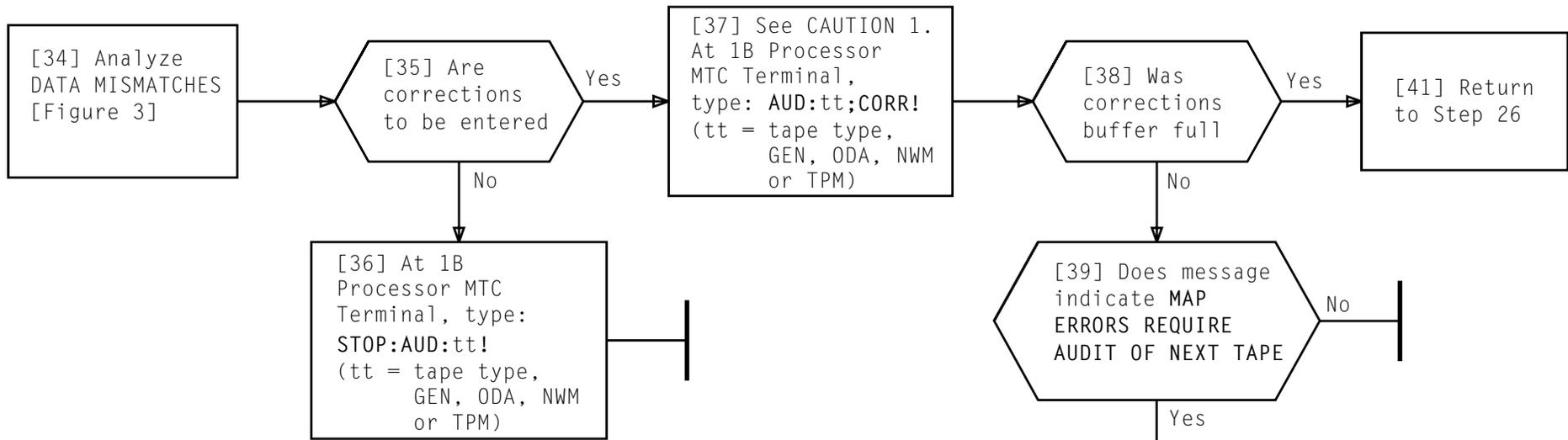
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**TABLE B
STOPPED AND ABORTED CODE DEFINITIONS**

CODE	DEFINITION	CODE	DEFINITION
1.	Tape header expected, EOF read	63.	Invalid load mode for given tape type
3.	Merge data file header expected, EOF read	64.	Invalid hash sum head table index encountered while processing hash sums in load mode
4.	Merge data file header expected, ID mismatch	70.	Tape secure failed
5.	CS2FS map expected, EOF read	71.	Tape unit not in proper mode
6.	CS2FS map expected, ID mismatch	72.	Read tape header request rejected
7.	ID2FS map expected EOF read	73.	Read data record request rejected
8.	Hash head table 1 expected, ID mismatch	74.	Tape operation failed
9.	ID2SEG map expected, EOF read	75.	Unexpected EOT detected
10.	ID2FS map expected, ID mismatch	76.	Open file request rejected
11.	Hash sum head table expected, EOF read	78.	Advance to end-of-file request rejected
12.	Hash sum head table expected, ID mismatch	79.	Request for additional MACP memory failed
13.	ID2SEG map expected, ID mismatch	80.	RC check failed. Personnel must decide if rollback is required
14.	File header expected, ID mismatch	81.	Request for status on the MACP memory request failed
15.	SAST unable to determine hash head cell contents	83.	Failed to find FS backup address for hash table
40.	Print request rejected	85.	Timed out while waiting for additional MACP memory
50.	Disk read request rejected	86.	Failed to convert CORE OFFSET TO CORE 30 bit address
51.	Disk write request rejected	87.	Failed to rebuild XS2FS MAP
52.	Disk queue full	91.	Disk operation failed
53.	Both file systems out of service	93.	MACP holding time exceeded
54.	Core address to file system address conversion failed. No backup	94.	Paging supervisor aborted
60.	SAWS lockout. Other core changing client in progress	96.	Interrupt occurred while SAST was in progress
61.	Unable to determine disk address of hash sum	97.	Termination manually requested
62.	Mismatches found between system maps and maps on nonmemory allocating tape	Other	Unassigned



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```

DATA MISMATCHES
CORE/FILE      TAPE      CORE/ID TAG      FS CPY0      FS CPY1
aaaaaaaaa      bbbbbbb      ccccccc      ddddddd      eeeeeee
.
.
.
aaaaaaaaa      bbbbbbb      ccccccc      ddddddd      eeeeeee
  
```

Mismatches found during audit:

- a = Octal number indicating a 30 bit core address or a file offset
- b = Octal number indicating data found on tape
- c = Octal number indicating data found in core (or ID TAG tag if TYPE = FILE)
- d = Octal number indicating data found in FS copy 0
- e = Octal number indicating data found in FS copy 1

= Text Phase indicating type of address where MISMATCH OCCURRED - FILE OR CORE

Figure 3 - Mismatch Data Layout

NOTE 1
To clear MAP ERRORS may require this procedure to be used with each type of backup tape

CAUTION 1
SCPs entered since last backup tape was written are lost at this point and must be re-entered

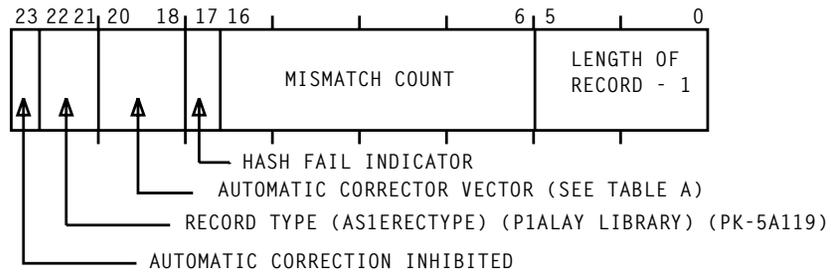
1. Use Figure 1 and TABLES A, B, and C, page 2, to analyze data.

End of procedure

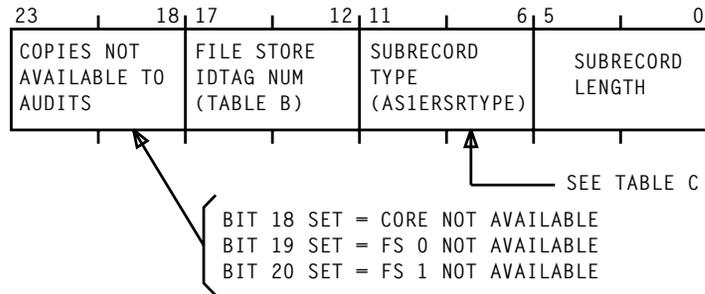
```

aaaaaaaa bbbbbbbb cccccccc cccccccc cccccccc cccccccc cccccccc cccccccc
cccccccc cccccccc dddddddd dddddddd dddddddd eeeeeeee ffffffff gggggggg
gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg
gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg
  
```

WORD a = SAWS Record Header



WORD b = Error Subrecord Header



WORDS c = CC Registers

WORDS d = Stack Entries

WORD e = SAWS Subtask Activity Word

WORD f = SAWS Inhibit, Update Program Activity Word

WORDS g = SAWS Update Client Subroutine Control Block

Figure 1

Reissued

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ANALYZE LOCKOUT INTERFACE FAILURE AND DATA MISMATCH DURING UPDATE WORDS FOR SAWS AUDIT

TABLE A AUTO CORRECTION VECTOR STATES	
STATE	DESCRIPTION
0	Core corrected from either file system
1	Write to file system 0
2	Write to file system 1
3	Core corrected from file system 1
4	Core corrected from file system 0
5	Write to file system 0 and file system 1
6	File system 0 copied to file system 1
7	File system 1 copied to file system 0

TABLE B			
FS ID TAG NUM	FS AREA NAME	FS ID TAG NUM	FS AREA NAME
01	Generic program	14	TR/PLT measurement
02	Library area	21	PAGED Program
03	ODA File Seg. 0	24	ODA File Seg. 1
07	NTWK management	25	ODA File Seg. 2
12	Merge	26	ODA File Seg. 3
13	RC rollback	Other	Invalid for SAWS

TABLE C ERROR SUBRECORD TYPE	
STATE	DESCRIPTION
1	Mismatch subrecord
2	Bink hash failure subrecord
3	Merge structure hash failure
4	Failing range corrected
5	Automatic correction inhibited
6	Excessive failing binks within 1 MEG range
7	Internal error detected
8	Terminal error detected
9	Immediate fail return from DKAD of read into buffer
10	Special hash sums mismatch
11	No good copy of failing range available
12	Good copy of failing range not identifiable
13	Immediate fail return from DKAD during correction
14	Audit-update program interface problem detected
15	Hash structure problem detected
16	DKAD failure return in a SAWS update subroutine
Other	Unassigned

**ANALYZE LOCKOUT INTERFACE FAILURE AND DATA MISMATCH
DURING UPDATE WORDS FOR SAWS AUDIT**

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1. Use Figure 1 and TABLES A, B, and C, page 2, to analyze data

End of procedure

Text phrase or phrases

DATA: aaaaaaaa

DATA:

bbbbbbbb ccccccc ddddddd

HASH CODE FAILURE

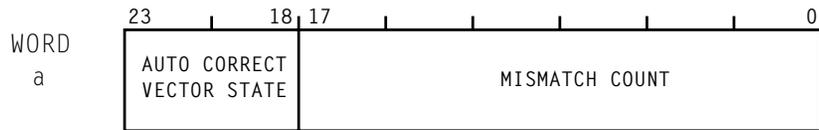
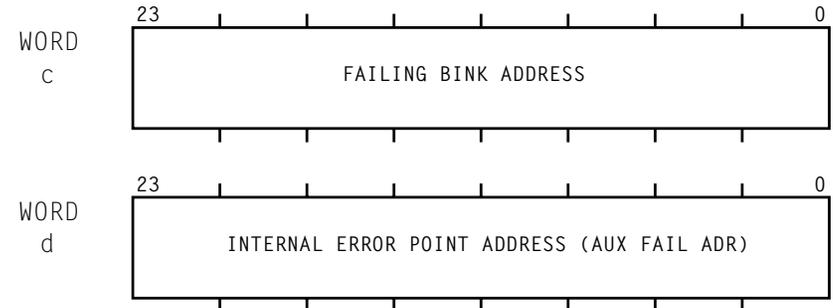
DATA:

eeeeeee ffffffff ffffffff gggggggg hhhhhhhh iiiiiiiii jjjjjjjj

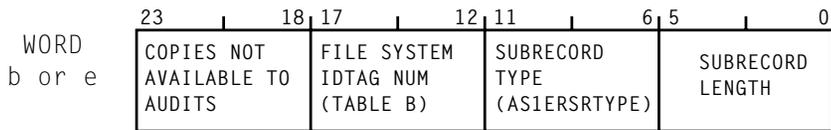
DATA MISMATCH

DATA:

eeeeeee ffffffff ffffffff gggggggg hhhhhhhh iiiiiiiii jjjjjjjj



SEE TABLE A



SEE TABLE C

BIT 18 SET = CORE NOT AVAILABLE
 BIT 19 SET = FS 0 NOT AVAILABLE
 BIT 20 SET = FS 1 NOT AVAILABLE

WORD	FOR HASH CODE FAILURE	FOR DATA MISMATCH
f*	FAILING BINK ADDRESS	MISMATCH ADDRESS
g	CORE-RESIDENT STORE HASH SUM	FILE SYSTEM ADDRESS
h	COMPUTED FS 1 HASH SUM	FS 1 DATA
i	COMPUTED FS 0 HASH SUM	FS 0 DATA
j	COMPUTED CORE HASH SUM	CORE DATA

* Failing Address and Mismatch address are 30 bit address in 4E21. The address is output in 2 parts, ffffffff ffffffff. For example, 00000031 77777773 equates to address 3177777773.

Figure 1

ANALYZE HASH CODE FAILURE AND DATA MISMATCH WORDS FOR SAWS AUDIT

TABLE A AUTO CORRECTION VECTOR STATES	
STATE	DESCRIPTION
0	Core corrected from either file system
1	Write to file system 0
2	Write to file system 1
3	Core corrected from file system 1
4	Core corrected from file system 0
5	Write to file system 0 and file system 1
6	File system 0 copied to file system 1
7	File system 1 copied to file system 0

TABLE B			
FS ID TAG NUM	FS AREA NAME	FS ID TAG NUM	FS AREA NAME
01	Generic program	14	TR/PLT measurement
02	Library area	21	PAGED Program
03	ODA File Seg. 0	24	ODA File Seg. 1
07	NTWK management	25	ODA File Seg. 2
12	Merge	26	ODA File Seg. 3
13	RC rollback	Other	Invalid for SAWS

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10	Special hash sums mismatch
11	No good copy of failing range available
12	Good copy of failing range not identifiable
13	Immediate fail return from DKAD during correction
14	Audit-update program interface problem detected
15	Hash structure problem detected
16	DKAD failure return in a SAWS update subroutine
Other	Unassigned

1. Use Figure 1 and TABLES A and B (Page 2),
to analyze data

End of procedure

EXCESSIVE HASH FAILURE DATA:

aaaaaaaa bbbbbbbb cccccccc dddddddd eeeeeeee

WORD a = ERROR SUBRECORD HEADER

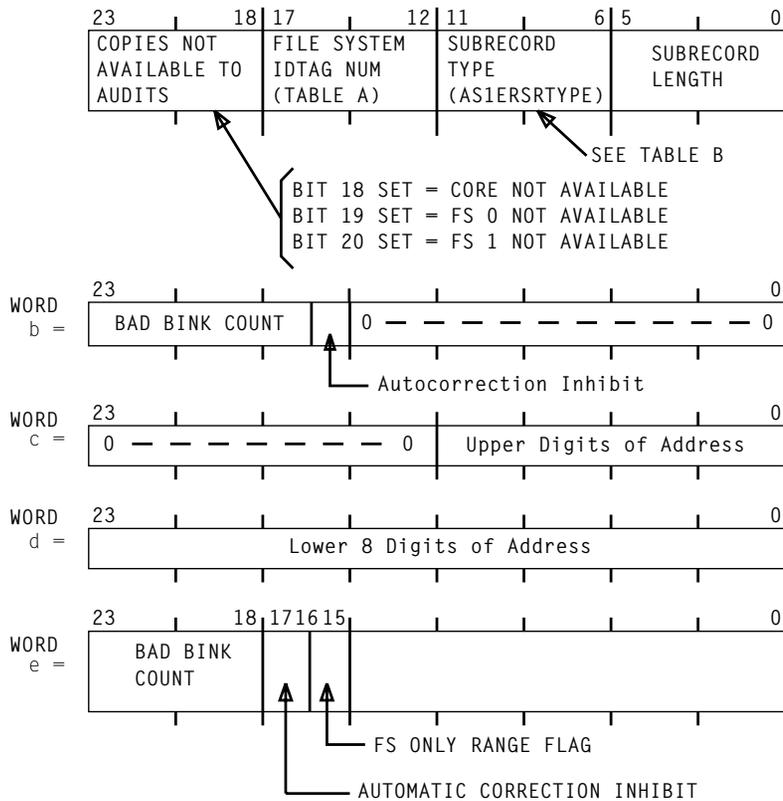


Figure 1

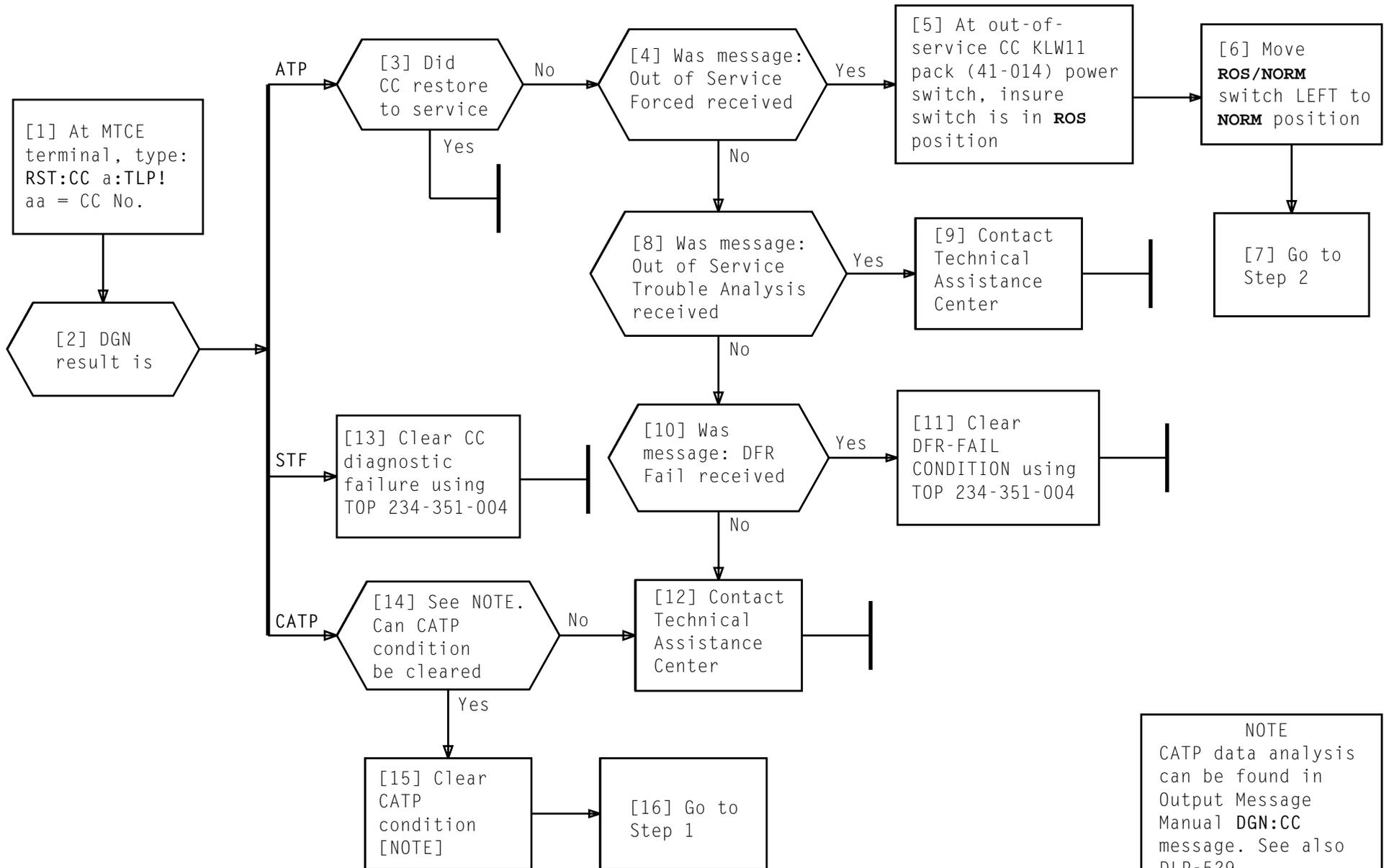
TABLE A			
FS ID TAG NUM	FS AREA NAME	FS ID TAG NUM	FS AREA NAME
01	Generic program	14	TR/PLT measurement
02	Library area	21	PAGED Program
03	ODA File Seg. 0	24	ODA File Seg. 1
07	NTWK management	25	ODA File Seg. 2
12	Merge	26	ODA File Seg. 3
13	RC rollback	Other	Invalid for SAWS

ANALYZE EXCESSIVE HASH CODE FAILURE AND DATA MISMATCH WORDS FOR SAWS AUDIT

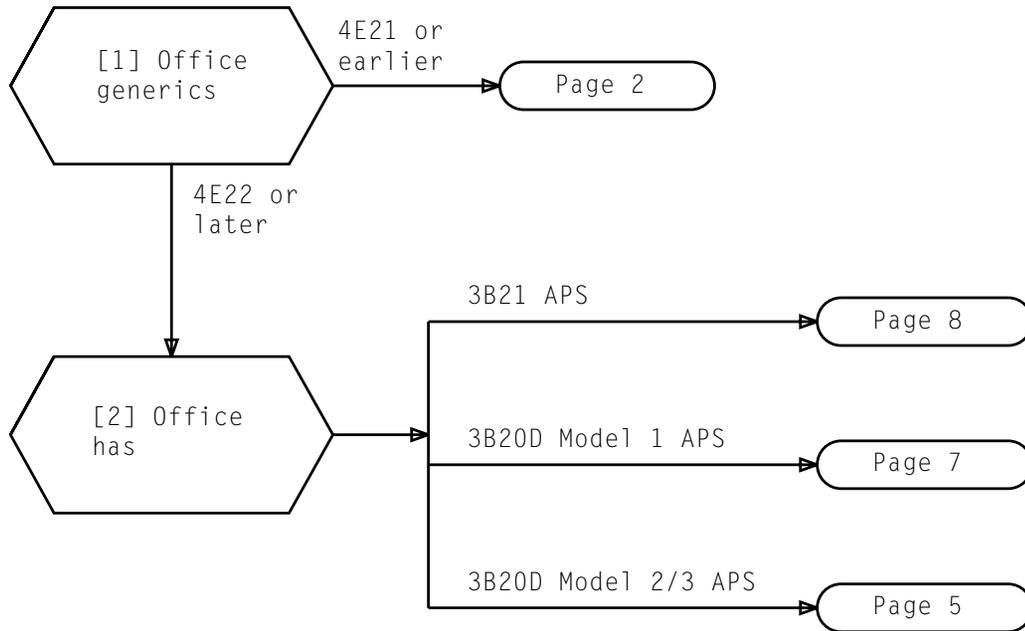
TABLE B ERROR SUBRECORD TYPE	
STATE	DESCRIPTION
1	Mismatch subrecord
2	Bink hash failure subrecord
3	Merge structure hash failure
4	Failing range corrected
5	Automatic correction inhibited
6	Excessive failing binks within 1 MEG range
7	Internal error detected
8	Terminal error detected
9	Immediate fail return from DKAD of read into buffer
10	Special hash sums mismatch
11	No good copy of failing range available
12	Good copy of failing range not identifiable
13	Immediate fail return from DKAD during correction
14	Audit-update program interface problem detected
15	Hash structure problem detected
16	DKAD failure return in a SAWS update subroutine
Other	Unassigned

**ANALYZE EXCESSIVE HASH CODE FAILURE AND DATA MISMATCH WORDS
FOR SAWS AUDIT**

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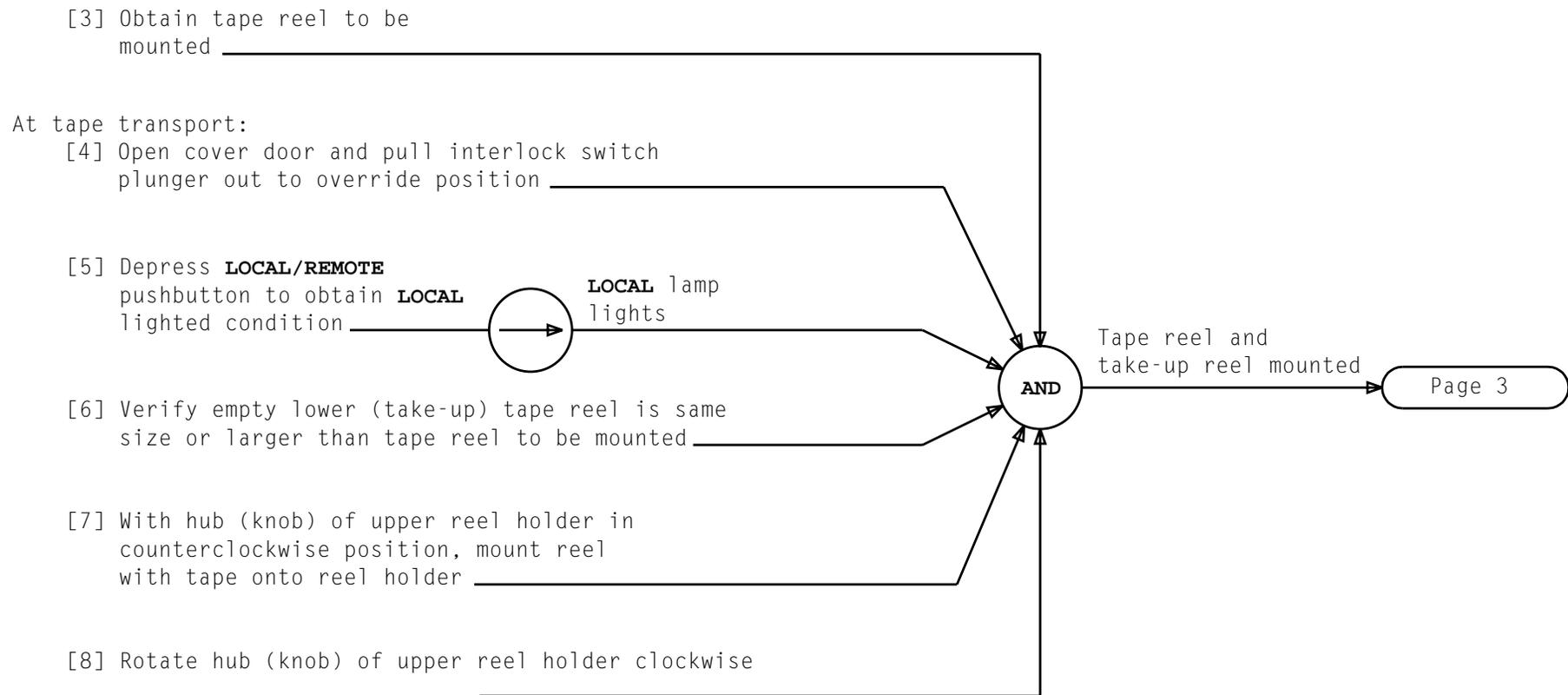


NOTE	
CATP data analysis can be found in Output Message Manual DGN:CC message. See also DLP-529.	
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MOUNT TAPE ON 3B TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

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MOUNT TAPE ON 3B TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

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[9] See WARNING 1. While depressing **BRAKE RELEASE** pushbutton, manually unwind approximately 5 feet of tape and release **BRAKE RELEASE** pushbutton

[10] See WARNING 2. Thread tape through tape path indicated on tape transport

[11] See NOTE 1. Start tape end on lower (take-up) reel making sure tape is not twisted

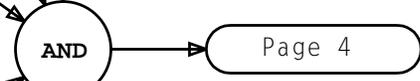
[12] See WARNING 3. While depressing **BRAKE RELEASE** pushbutton, manually wind lower (take-up) reel three or four turns and release **BRAKE RELEASE** pushbutton

[13] Depress **ARMS NORMAL** pushbutton

ARMS NORMAL lamp lights until arms apply tension to tape

[14] Depress **FORWARD** pushbutton

FORWARD lamp lights; tape winds forward to BOT marker and stops

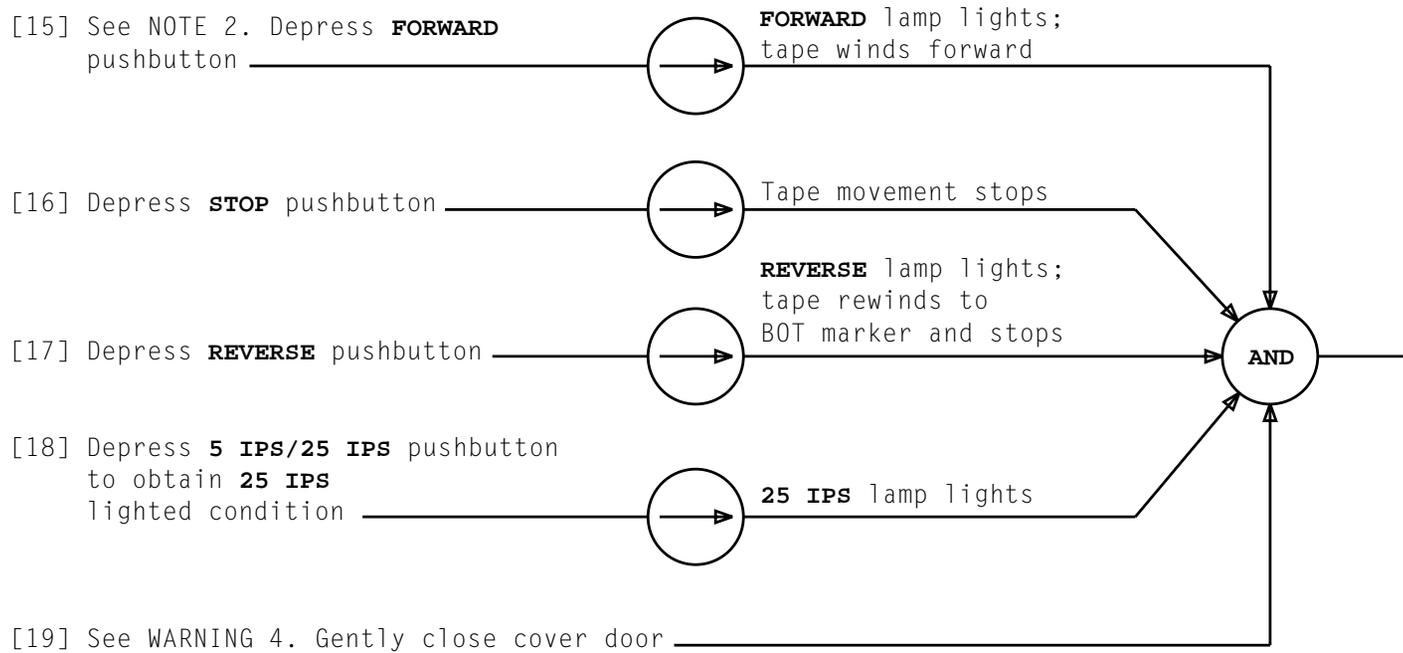


NOTE 1
To start tape on take-up reel, tape end should be moistened (moistened fingers) and tape should be stuck to reel axle

WARNINGS

1. Contamination of tape by contact with floor damages tape heads
2. Tape head surfaces should not be touched; body oil contaminates tape
3. If tape is not properly aligned along rollers and guides or is too loose, tape may be damaged

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NOTE 2	
Steps 13, 14, and 15 cause BOT marker to be approached from recorded area of tape	
<i>WARNING 4</i>	
<i>Closing tape transport cover door in harsh manner may upset alignment</i>	
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MOUNT TAPE ON 3B TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

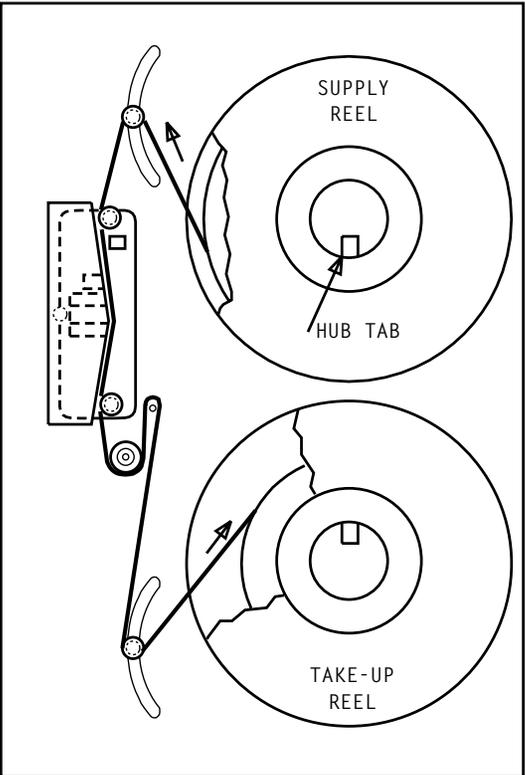
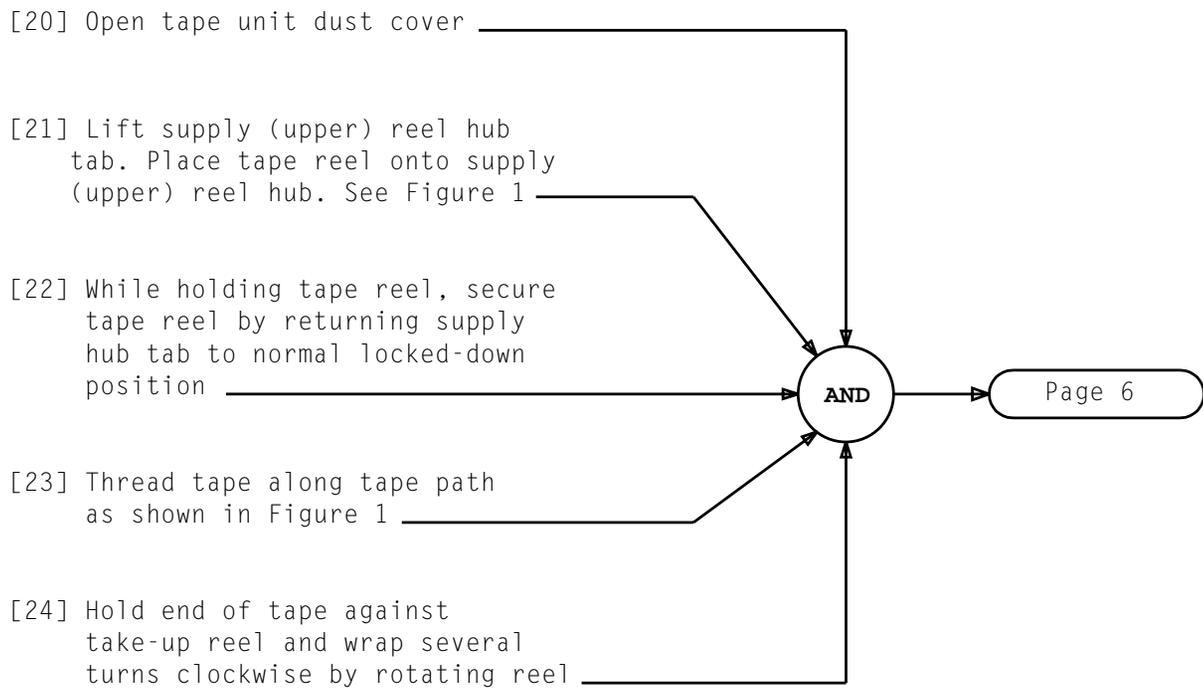
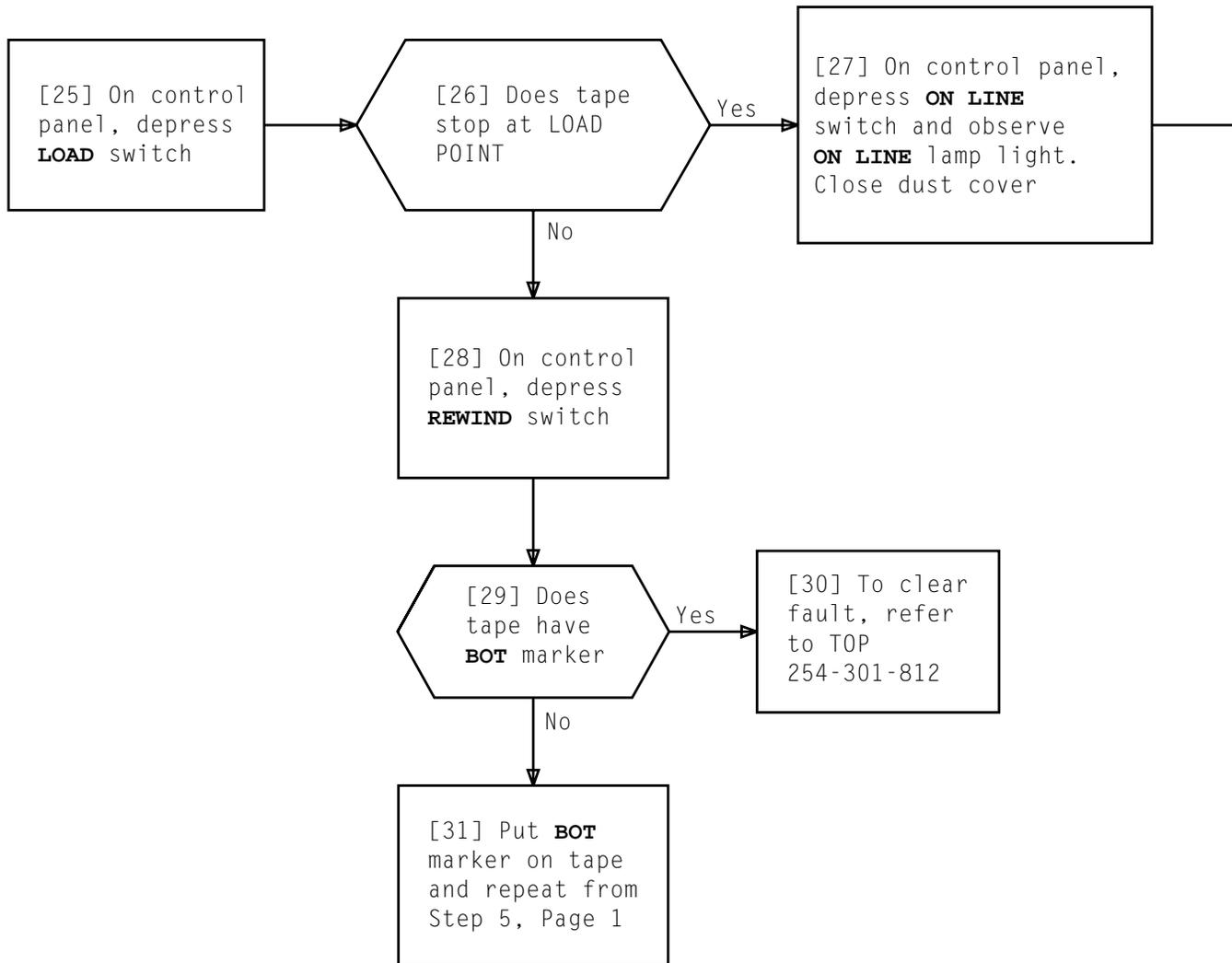


Figure 1



MOUNT TAPE ON 3B TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

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[32] If tape is to be written, attach write-enable ring on supply reel

[33] If **LOGIC OFF** LED lighted, touch **LOGIC ON** switch

[34] Open dust cover and verify circuit breaker at side 1

[35] See Figure 2. Place supply reel on hub and depress hub latch

[36] Thread tape from bottom of supply reel along path as shown in Figure 2

[37] Hold end of tape against take-up reel and wrap several turns clockwise by rotating reel; then close dust cover

[38] At control panel, touch **LOAD/REWIND** switch

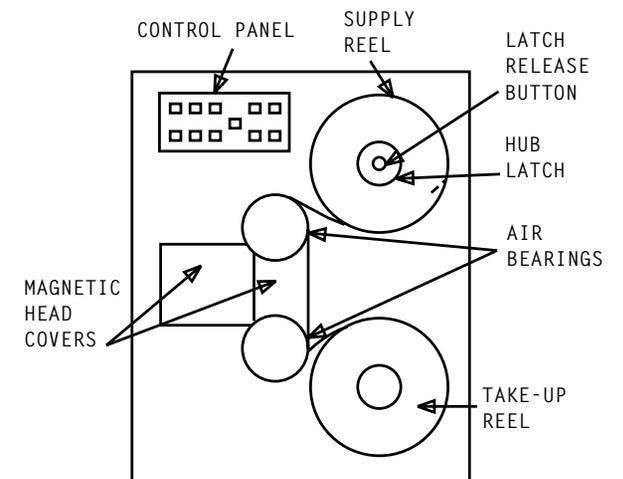
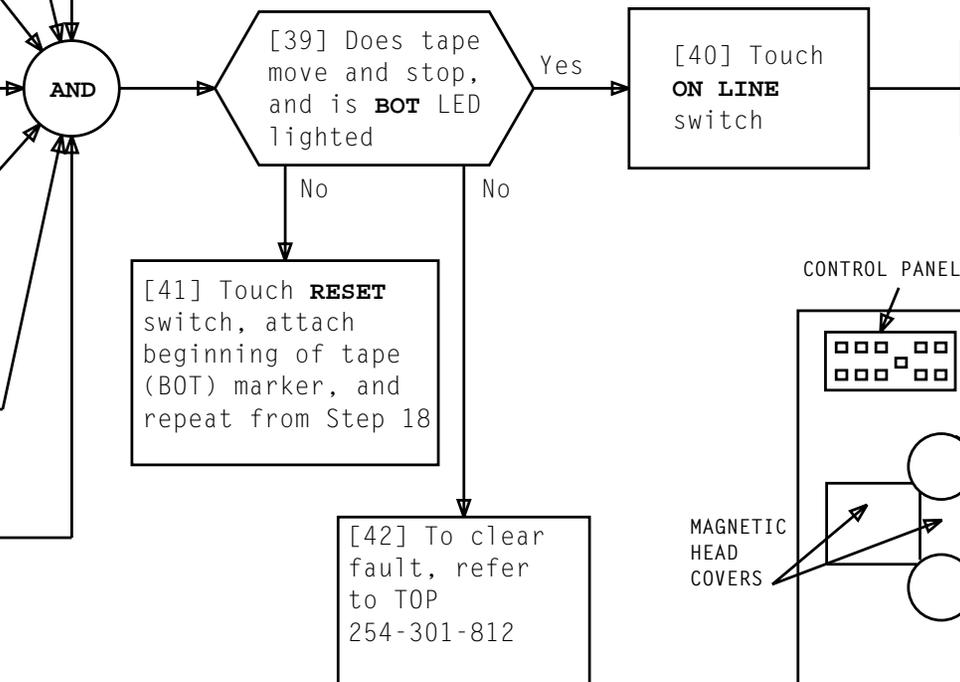


Figure 2

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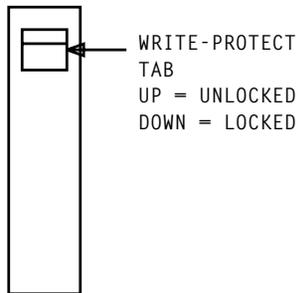
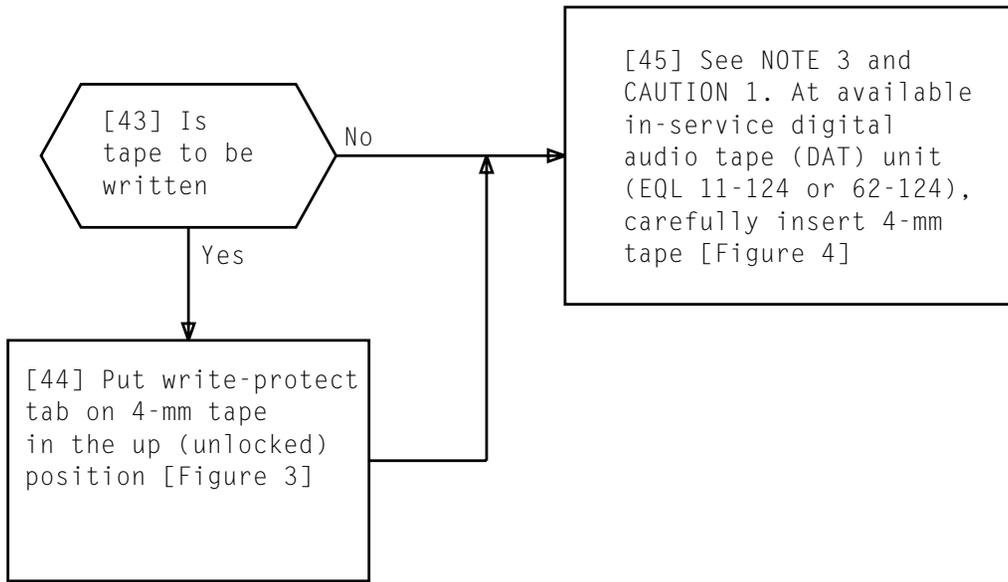


Figure 3 - 4-mm Tape

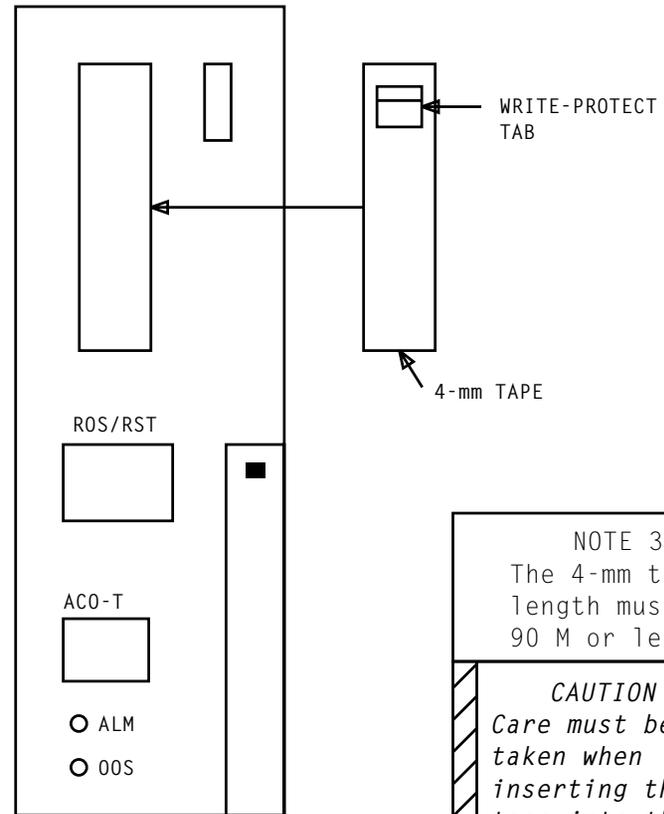
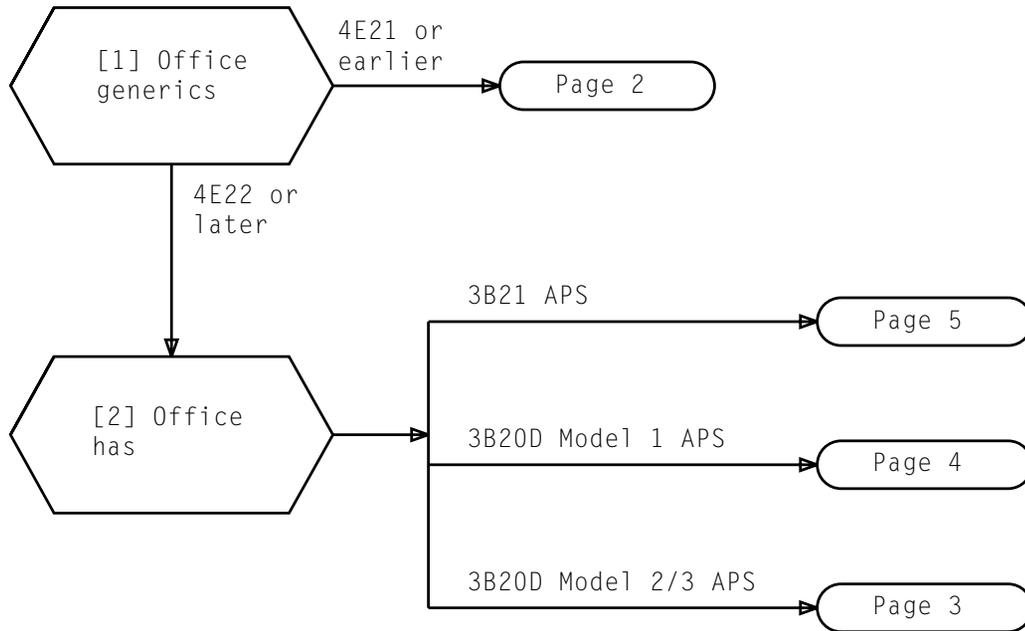


Figure 4 - DAT Unit

NOTE 3
The 4-mm tape length must be 90 M or less

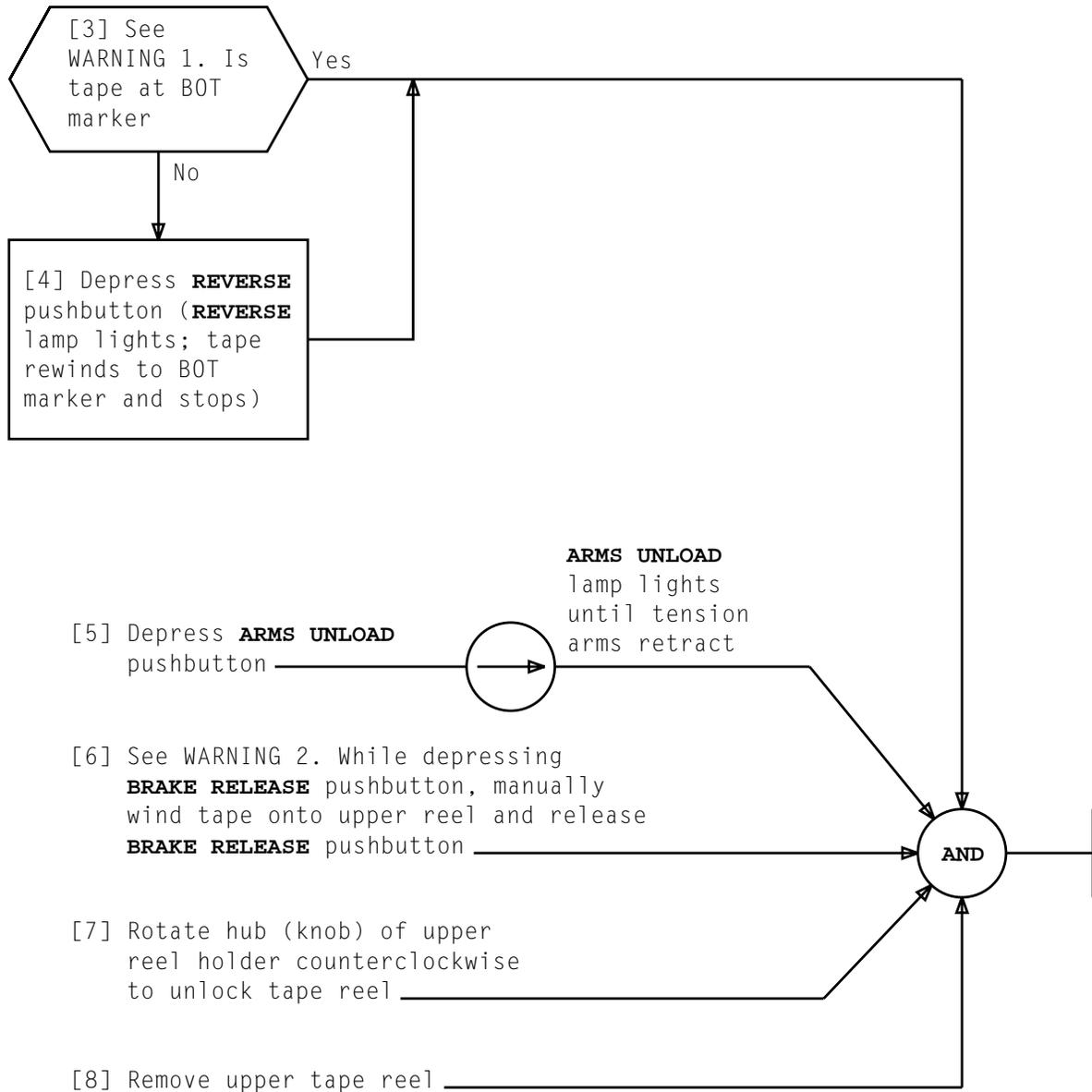
CAUTION 1
Care must be taken when inserting the tape into the DAT unit. Tape must not be forced

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REMOVE TAPE ON 3B TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

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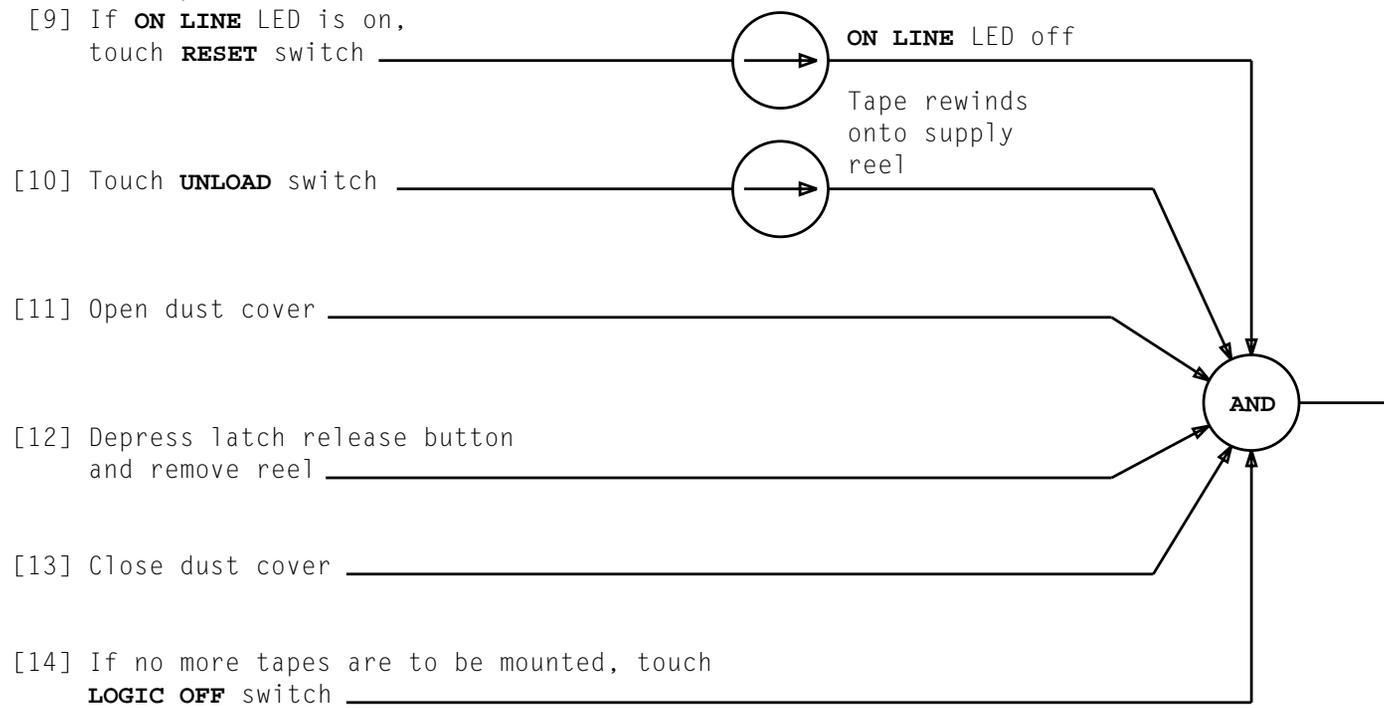
WARNINGS

1. If tape is being demounted due to an obvious faulty tape unit, the proper tape unit maintenance documentation should be referenced
2. Pulling or dragging last 5 feet of tape across heads may contaminate heads

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REMOVE TAPE ON 3B TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

At control panel:



REMOVE TAPE FROM 3B TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

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[15] At control panel, if **ON LINE** lamp is on, depress **ON LINE** switch

[16] If tape is not at BOT, depress **REWIND** switch

LOAD POINT
LED lights

[17] Depress **REWIND** switch

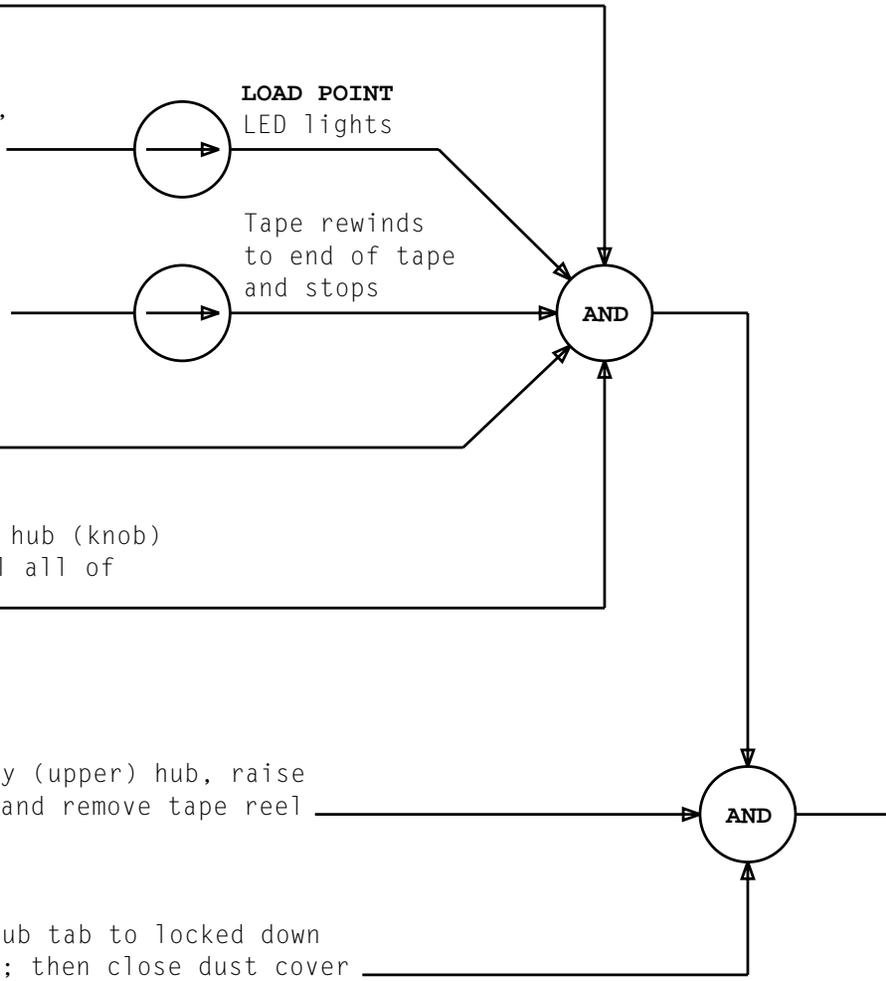
Tape rewinds
to end of tape
and stops

[18] On tape unit,
open dust cover

[19] Rotate supply (upper) hub (knob)
counterclockwise until all of
tape is rewound

[20] On supply (upper) hub, raise
hub tab and remove tape reel

[21] Return hub tab to locked down
position; then close dust cover



REMOVE TAPE FROM 3B TAPE UNIT OR DIGITAL AUDIO TAPE (DAT) UNIT

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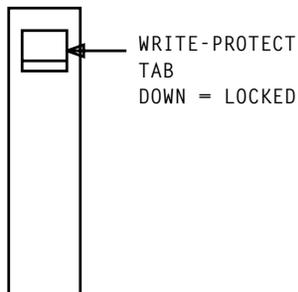
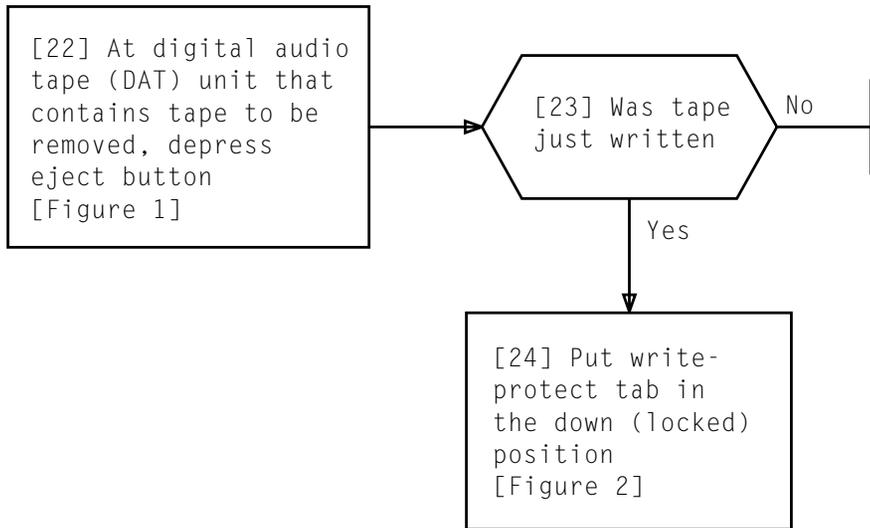


Figure 2 - 4-mm Tape

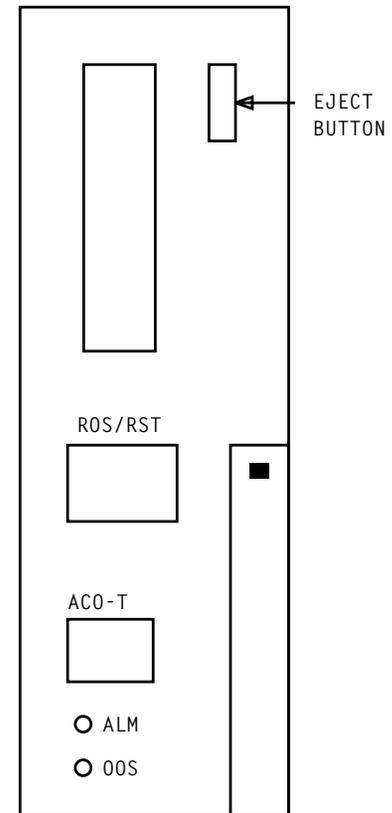


Figure 1 - DAT Unit

1. Note absolute address to be converted

2. [NOTE, Figure 3] Use address space map for applicable generic (PK4A002) and absolute address to identify pident and strip containing this address (for example, if address was 11261737, the pident would be FERACONT and the strip would be AD per Figure 1)

3. Using octal arithmetic, subtract pident and strip starting address from absolute address to be converted [Figure 2]

End of procedure

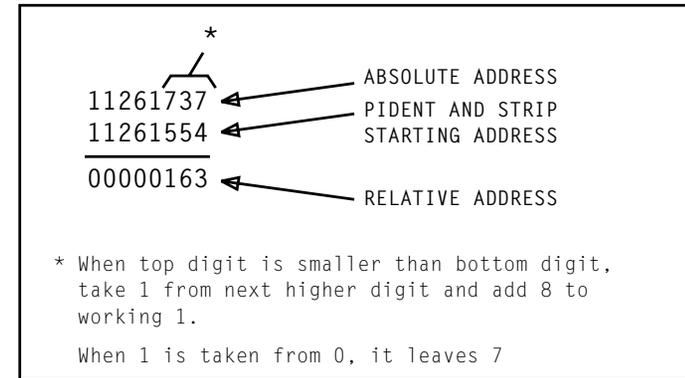


Figure 2 – Sample of Absolute to Relative Address Conversion

000C11254470	12	10	FERACOMM	DF	FERACOMM_AA
000C11254502	105	69	FERACOMM	DG	FERACOMM_AA
000C11254610	316	206	FERACOMM	DH	FERACOMM_AA
000C11255126	1042	546	FERACOMM	EA	FERACOMM_AA
000C11256170	267	183	FERACOMM	GE	FERACOMM_AA
000C11256460	2441	1313	FERACONT	AA	FERACONT_AA
000C11261122	254	172	FERACONT	AB	FERACONT_AA
000C11261376	156	110	FERACONT	AC	FERACONT_AA
000C11261554	401	257	FERACONT	AD	FERACONT_AA
000C11262156	136	94	FERACONT	AE	FERACONT_AA
000C11262314	76	62	FERACONT	AF	FERACONT_AA
000C11262412	66	54	FERACONT	AG	FERACONT_AA

Figure 1 – Excerpt from Address Space Map

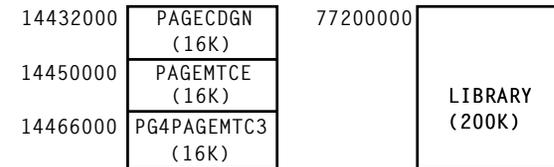


Figure 3 – Memory Areas Not In Space Map

NOTE	
GULP, DGN, and LIBRARY paging areas are not in space map. See Technical Assistance center if address is in these areas.	
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1. Define error using PMDs [TABLE A]

End of procedure

TABLE A	
<p>PMD-006 Fault isolated by TNFRISAD. PMD indicates that one controller of suspect member failed access test. Controller which failed is suspect controller</p> <p>PMD-007 Fault isolated by TNFRISAD. PMD indicates that both controllers failed access test. Each controller is assigned half weight indicating nonunique failure</p> <p>PMD-010 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a unique fault which is up in only one controller; therefore, it is transient unique (AINT)</p> <p>PMD-011 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a unique fault which is up in only one controller; therefore, it is hard unique (AINT)</p> <p>PMD-012 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a unique fault which is up in one controller only; therefore, it is transient unique (AINT)</p> <p>PMD-013 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a unique fault which is up in one controller only; therefore, it is hard unique (AINT)</p> <p>PMD-020 Fault isolated by TNFRTMMN. This is a matched or nonunique type error which occurred in both controllers. Retry was performed and passed; therefore, it is transient nonunique (AINT)</p>	<p>PMD-021 Fault isolated by TNFRTMMN. This is a matched or nonunique type error which occurred in both controllers. Retry was performed and failed; therefore, it is hard nonunique (AINT)</p> <p>PMD-050 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a unique fault which is up in only one controller; therefore, it is transient unique (ASWF)</p> <p>PMD-051 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a unique fault which is up in only one controller; therefore, it is hard unique (ASWF)</p> <p>PMD-052 Fault isolated by TNFRTMMN. This is a software type fault. This PMD indicates that software has caused a problem. Hardware is not suspected (ASWF)</p> <p>PMD-053 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a unique type fault which occurred in both controllers; therefore, it is transient nonunique (ASWF)</p> <p>PMD-054 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a unique type fault which occurred in both controllers</p> <p>PMD-055 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a match type fault which occurred in one controller only; therefore, it is transient unique (ASWF)</p> <p>PMD-056 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a match type fault which occurred in one controller only; therefore, it is is hard unique (ASWF)</p>

TABLE A (Contd)

<p>PMD-100 Fault isolated by TNFRTSMN. Fault type is unique class-1 transient (retry passed). Error is PFE, PFO, MODEF, RTSMPF, TTSMPPF, BIMPPF, or ASWF in only one controller when unit is simplex or duplex; or an RTSMA, TTSMMA, or BIMA in only one controller when unit is duplex (ASWF)</p>	<p>PMD-106 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard (retry failed). Error is PFE, PFO, RTSMPF, TTSMPPF, BIMPPF, or ASWF in both controllers (ASWF)</p>
<p>PMD-101 Fault isolated by TNFRTSMN. Fault type is a unique class-1 hard (retry failed). Error is PFE, PFO, MODEF, RTSMPF, TTSMPPF, BIMPPF, or ASWF in only one controller when unit is simplex or duplex; or RTSMA, TTSMMA, or BIMA in only one controller when unit is duplex (ASWF)</p>	<p>PMD-150 Fault isolated by TNFRTSMN. Fault type is unique class-1 transient (retry passed). Error up in AINT error source register may be AINT only or SSWF or any error which has secondary registers (RTMP, TTMP, BIMP, RSW, or BMAPF) where no errors are up in secondaries</p>
<p>PMD-102 Fault isolated by TNFRTSMN. Fault type is unique soft. Error is MODEF in both controllers or RTSMA, TTSMMA, or BIMA in both controllers if unit is duplex; or up in the in-service controller if unit is simplex (ASWF)</p>	<p>PMD-151 Fault isolated by TNFRTSMN. Fault type is unique class-1 hard (retry failed). Error up in AINT error source register may be AINT only or SSWF or any error which has secondary registers (RTMP, TTMP, BIMP, RSW, or BMAPF) where no errors are up in secondaries</p>
<p>PMD-103 Fault isolated by TNFRTSMN. Fault type is unique transient (retry passed). Error is AMM, DWMM, or BIMWM in only one controller if unit is duplex; or up in the in-service controller if unit is simplex. BIMWM is not checked for CRTSI (ASWF)</p>	<p>PMD-152 Fault isolated by TNFRSTMN. Fault type is unique class-2 transient (retry passed). Error in AINT error source register may be CE or TSSC in only one controller with errors up in secondary registers</p>
<p>PMD-104 Fault isolated by TNFRTSMN. Fault type is unique class-3 hard (retry failed). Error is AMM, DWMM, or BIMWM in only one controller if unit is duplex; or up in the in-service controller if unit is simplex. BIMWM is not checked for CRTS1 (ASWF)</p>	<p>PMD-153 Fault isolated by TNFRTSMN. Fault type is unique class-2 hard (retry failed). Error in AINT error source register may be CE or TSSC in only one controller or RTMP, TTMP, BIMP, RSW, BMAPF, or TSW in only one controller with errors in secondary register</p>
<p>PMD-105 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed). Error is PFE, PFO, RTSMPF, TTSMPPF, BIMPPF, or ASWF in both controllers (ASWF)</p>	<p>PMD-160 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed – both controllers). Error in AINT error source register or sense and and lock register may be AINT only, CE, SSWF, or TSSC in both controllers or RIMP, TIMP, BIMP, or BMBPF in both controllers with errors up in secondaries</p>

TABLE A (Contd)

<p>PMD-161 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard (retry failed – either controller). Error in AINT error source register or sense and lock register may be AINT only, CE, SSWF, or TSSC in both controllers or RTMP,TTMP,BIMP, or BMBPF in both controllers with errors up in secondaries</p>	<p>PMD-173 Fault isolated by TNFRTSMN. A receive or transmit time slot memory parity failure has been detected in the AINT and/or SAL error source registers in both controllers. Both of the controllers have passed the retry. The AUX data block provides the K-code of the suspect unit and the failing level. This is a class-4 transient failure</p>
<p>PMD-170 Fault isolated by TNFRTSMN. Either a receive or transmit time slot memory parity failure has been detected in the AINT and/or SAL error source registers in only one controller. The error is partitionable and a retry of the failing controller has failed. The AUX data block provides the K-code of the suspect unit and the failing level. This is a class-2 hard fault</p>	<p>PMD-207 Fault isolated by TNFRTSMN. Fault is either TRPF, TMM, or TSW. The channel is busy to a time slot. In attempting to trace the call through the network, a mismatch in the TSM data was found in the RTSI. An RTMP error was then found in the RTSI AINT ESR. Suspect frame is changed to RTSI and fault isolation reentered</p>
<p>PMD-171 Fault isolated by TNFRTSMN. Either a receive or transmit time slot memory parity failure has been detected in the AINT and/or SAL error source registers in only one controller. The error is partitionable and a retry of the failing controller has passed. The AUX data block provides the K-code of the suspect unit and the failing level. This is a class-2 transient fault</p>	<p>PMD-210 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. A path was found back to RTSI. RTSI has some error source bits set. Suspect frame is changed to RTSI and fault isolation reentered</p>
<p>PMD-172 Fault isolated by TNFRTSMN. A receive or transmit time slot memory parity failure has been detected in the AINT and/or SAL error source registers in both controllers. One or both of the controllers have failed the retry. The AUX data block provides the K-code of the suspect unit and the failing level. This is a class-4 hard failure</p>	<p>PMD-211 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, the network routine (NTRO) for one controller is incorrect. Fault is treated as unique error. AUX data block has more information</p>
	<p>PMD-212 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, TTSM memory did not have appropriate data. AUX data block has more information. Fault is treated as unique error</p>

TABLE A (Contd)

<p>PMD-213 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, TTSM information from two controllers did not agree. Fault is treated as nonunique error. AUX data block has more information</p>	<p>PMD-220 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, it was found RTSI duplex failed. AUX data block has more information. Fault is treated by letting ERAT attempt to take out RTSI</p>
<p>PMD-214 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, one TMS controller failed to pass access test. AUX data block has information. This TMS controller is treated as unique fault</p>	<p>PMD-221 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, one RTSI controller failed access test. AUX data block has more information. Fault is treated as unique RTSI fault</p>
<p>PMD-215 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, both TMS controllers failed to pass access test. Fault is treated as nonunique TMS fault. AUX data block has more information</p>	<p>PMD-222 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, both RTSI controllers failed access tests. More information in AUX data block. Fault is treated as nonunique RTSI fault</p>
<p>PMD-216 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call though network, mismatch in data stored in TSM memory was found. AUX data block has more information. Fault is treated as TMS nonunique error</p>	<p>PMD-223 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, broken or multiple path found in or multiple path found in RTSI. AUX data block has more information. Fault is treated as RTSI software fault</p>
<p>PMD-217 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, cutoff or multiple path has been found in TMS. AUX data block has more information. Fault is treated as software fault</p>	<p>PMD-224 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to time slot. In attempting to trace call through network, mismatch in TMS routing F/F was found. AUX data has more information. Fault is treated as RTSI nonunique fault</p>

TABLE A (Contd)

<p>PMD-225 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, one TRSI controller has incorrect network routing. AUX data has more information. Fault is treated as TRSI unique fault</p>	<p>PMD-232 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error in both controllers but channel on which error occurred is not involved in network path. Therefore, fault is in this unit and is hard because retry failed. Fault may be in recorrelator or involve BUFC memory but cannot be isolated to unique controller</p>
<p>PMD-226 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, mismatch in TSM data in RTSI was found. AUX data has more information. Fault is treated as RTSI nonunique fault</p>	<p>PMD-233 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of busy idle memory map bits against TS memory was run. Check found that suspect controller has mismatch between time slot memory information and BIMM information. Information not found in other controller. Therefore, BIMM or TTSM in suspect controller may be at fault</p>
<p>PMD-227 Fault isolated by TNFRMIT. Fault is either TRPF, TMM, or TSW. The channel is busy to a time slot. In attempting to trace the call through the network, a broken or multiple path was found in the RTSI. An RTMP error was then found in the RTSI AINT ESR. Suspect frame is changed to the RTSI and fault isolation re-entered</p>	<p>PMD-234 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of busy idle memory map bits against TS memory was run. Check found mismatch in data between two controllers which is attributable to controller fault but cannot be further isolated to unique controller. BIMM or TTSM in one of two controllers is suspect</p>
<p>PMD-230 Fault isolated by TNFRXMIT. Fault type is TRPF, TMM, or TSW with no corresponding secondary ESR bits set. Fault is probably in indicated controller ESRS</p>	<p>PMD-235 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of busy idle memory map bits against TS memory was run. Check has found data between controllers to match but BIMM data and TS data does not correlate. Therefore, error is probably result of software error</p>
<p>PMD-231 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error in both controllers but channel on which error occurred is not involved in network path. Therefore, fault is in this unit but is transient because retry passed. Fault may be in recorrelator or involve BUFC memory but cannot be isolated to controller</p>	

TABLE A (Contd)

<p>PMD-236 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of BIMM and TTSM information passed. Recorrelator tested and both controllers failed. Problem may be in cross controller matchers and is treated as nonunique</p>	<p>PMD-250 Fault isolated by TNFRXMIT. Fault type is hard RSW (retry failed). Fault is probably not in TSI recording error but in transmission subunit connected to interrupting port. AUX data block has details of interrupting ports</p>
<p>PMD-237 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Error of BIMM and TTSM information passed. Recorrelator tested and one controller failed. Fault is in recorrelator or associated circuits and is treated as unique fault</p>	<p>PMD-251 Fault isolated by TNFRXMIT. Fault type is transient RSW (retry passed). Fault is probably not in TSI recording error, but in transmission subunit connected to interrupting ports. AUX data block has details of interrupting ports</p>
<p>PMD-240 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of BIMM and TTSM information passed. Recorrelator tested and both controllers passed. Since failing channel is not involved in network path, no more testing can be done and fault must be in failing frame. Fault is treated as nonunique</p>	<p>PMD-300 Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Attempt to change state of BMA port pest has failed</p>
<p>PMD-241 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Path was found on failing time slot. Attempts made to isolate fault to one of six possible controllers by reconfiguring network routing. AUX data block has more information. Error was not isolated and must be considered nonunique. Final suspect list which is passed on to error analysis is found in AUX data block</p>	<p>PMD-301 Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Attempt to change state of HFIS bit in hardware status register has failed</p>
<p>PMD-242 Fault isolated by TNFRXMIT. Error is unresolvable TRPF. Request controller restore.</p>	<p>PMD-302 Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Attempt to reset FS and FE bits of hardware status register has failed</p>
<p>PMD-243 Fault isolated by TNFRXMIT. Error is a hard unique TRPF. Request controller removed to listen only and request a diagnostic on the controller.</p>	<p>PMD-303 Fault isolated by TNFRMMRT. Fault type is unique software error. Mismatch between controllers of data in critical register dump at time of interrupt. Either HFIS bit of hardware status word (for non-CRTSI only) or port pests do not match or software state and CREG value of port pests do not match</p>
	<p>PMD-304 Fault isolated by TNFRMMRT. Fault type is nonunique class-3 transient. RMM,BMAPF, or BMBPF BMBPF error not detected in SAL registers for either controller after both registers were cleared and unit was allowed to autonomously cycle</p>

TABLE A (Contd)

PMD-305	Fault isolated by TNFRMMRT. Fault type is nonunique class-3 hard. Network connection from failing channel in BMA to maintenance channel in BMD made. Data received in BMD does not match data sent from BMA for both controllers	PMD-361	Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard transient (retry passed). Error is AMM in both controllers
PMD-306	Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Network connection from failing channel in BMA to maintenance channel in BMD made. Data received in BMD does not match data sent from BMA for one controller	PMD-362	Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed). Error is AMM in both controllers
PMD-307	Fault isolated by TNFRMMRT. Fault type is nonunique class-3 hard. Attempt to make connection across the network failed.	PMD-363	Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard (retry failed). Error is AMM in both controllers
PMD-310	Fault isolated by TNFRMMRT. Fault type is nonunique class-3 transient. Loop-around connection of network made. Data received in maintenance channel of BMD matches data sent through failing channel of BMA or both controllers	PMD-364	Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed). Error is DWMM in both controllers
PMD-311	Fault isolated by TNFRMMRT. Fault type is nonunique class-3 transient. Loop-around connection of network made. Data received in maintenance channel of BMD does not match data sent through failing channel of BMA for both controllers	PMD-365	Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard (retry failed). Error is DWMM in both controllers
PMD-312	Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Loop-around connection of network has been made. Data received in maintenance channel of BMD does not match data sent through failing channel of BMA for one controller	PMD-366	Fault isolated by TNFRTMMN. Match type error which occurred in both controllers. (MWM) Retry performed and passed; therefore, it is transient nonunique (ASWF)
PMD-313	Fault isolated by TNFRMMRT. Fault type is nonunique class-3 hard. No test made. Attempt to make loop-around connection of network failed	PMD-367	Fault isolated by TNFRTMMN. Match type error which occurred in both controllers; (MWM) therefore, it is hard unique (ASWF)
PMD-360	Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed). Error is BIMWM up in both controllers	PMD-370	Fault isolated by TNFRTMMN. Match type error which occurred in both controllers. (AMM) Retry performed and passed; therefore, it is transient nonunique (ASWF)
		PMD-371	Fault isolated by TNFRTMMN. Match type error which occurred in both controllers. (AMM) Retry performed and failed; therefore, it is hard nonunique (ASWF)

1. See Figure 1 and EXAMPLE 1. Check contents of CREG 3
2. Convert octal data to binary
3. Regroup bits 7-13 starting at bit 7 and grouping from right to left
4. Convert binary bits back to octal. This is the memory number

TMSP CRITICAL REGISTERS						CREG3 (CONTR 0)
00000034	03011434	00000002	03331420	00076602	00001005	
00000037	55555555	55555555	55555555	55555555	55555555	
00010021	00000000	00000000	<u>00000000</u>	00077177	00000000	
			↑			CREG 3 (CONTR 1)

Figure 1 - TMS ESR+1 Register

ESR+1 DATA	0			3			3			3			1		4		2		0					
BINARY	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	1	1	0	1	1	0	1	1	0	0	1	1	1	0	0	0	0	1	0	0
	REGROUPED										1	1 0 0		1 1 0										
	RECONVERTED OCTAL VALUE										*	4		6										

* INDICATES BAY (0 OR 1) for TMSA Only

EXAMPLE 1 - Determine Memory Number

**IDENTIFY SUSPECT MEMORY AND MEMORY REGISTER CIRCUIT PACKS,
TIME MULTIPLEXED SWITCHING**

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[1] Using bit set in CREG 20/21 (if TSI-B), determine SPC and level from TABLE A

[2] Extract octal time slot from bits 17-19 in CREG 3 [TABLE B]

[3] Use time slot to determine SLIP [TABLE C and Step 2]

[4] Use SLIP and TSWF TMM level [Step 1] to determine BMC level from TABLE D

[5] Use BMC level and SPC [Step 1] to obtain list of primary suspect circuit packs listed in TABLE E, Page 2



Page 3

TABLE B TIME SLOT EXTRACTION									
CREG 3 OCTAL DATA	7			3			0		
BIT POSITION	23	22	21	20	19	18	17	16	15
BINARY EQUIVALENT	1	1	1	0	1	1	0	0	0
OCTAL TIME SLOT							1	1	0 = 6

TABLE C								
OCTAL TIME SLOT (MOD 8)	0	1	2	3	4	5	6	7
SLIP	4	5	6	7	0	1	2	3

TABLE D										
SLIP	0	1	2	3	4	5	6	7	B M C	
T	0	0	1	2	3	4	5	6		7
S	1	1	2	3	4	5	6	7		0
W	2	2	3	4	5	6	7	0		1
F	3	3	4	5	6	7	0	1		2
L	4	4	5	6	7	0	1	2		3
E	5	5	6	7	0	1	2	3		4
V	6	6	7	0	1	2	3	4		5
L	7	7	0	1	2	3	4	5	6	

TABLE A BMB, SPC, AND LEVEL																
CREG	SPC								SPC							
20	1								0							
21	3								2							
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVEL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

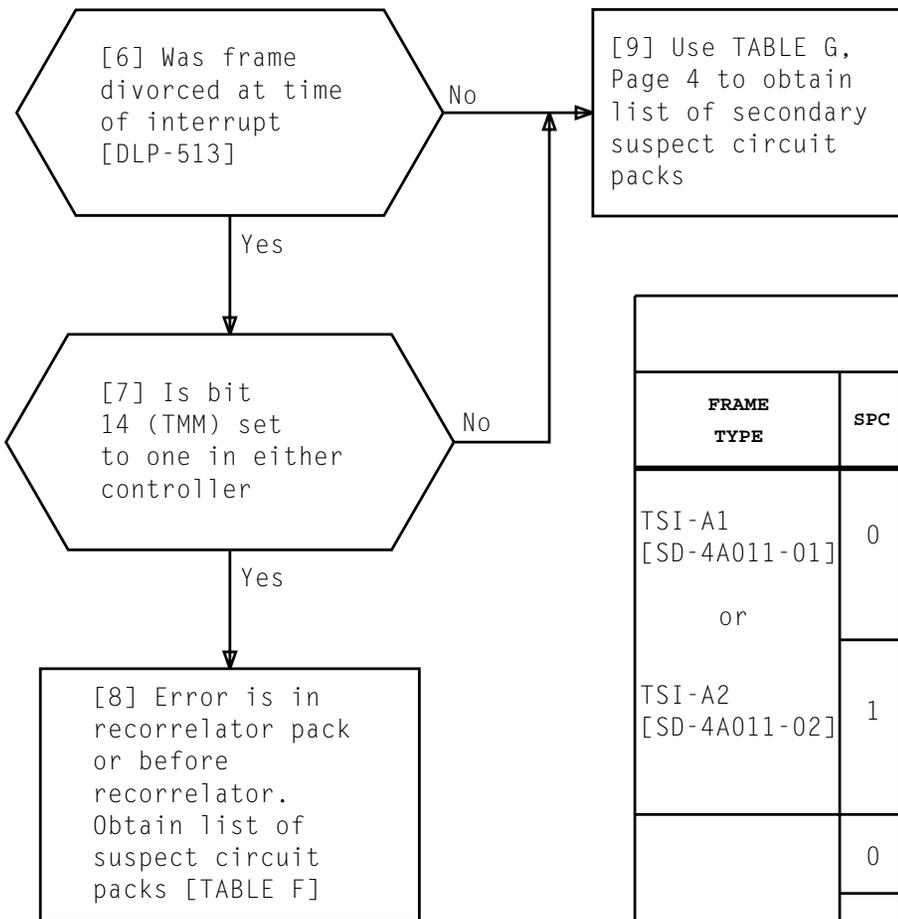
DETERMINE F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE BUFFER MEMORY C (BMC) USING TABLES

TABLE E SUSPECT BMC CIRCUIT PACK LOCATIONS										
FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A011-01] or TSI-A2 [SD-4A011-02]	0	FA633	46-57	46-56	46-55	46-54	46-53	46-52	46-51	46-50
		FA542	42-59	42-59	42-59	42-59	42-56	42-56	42-56	42-56
		FA542	42-58	42-58	42-58	42-58	42-55	42-55	42-55	42-55
		FA542	42-57	42-57	42-57	42-57	42-54	42-54	42-54	42-54
		FA1190	50-57	50-56	50-55	50-54	50-53	50-52	50-51	50-50
	1	FA633	68-57	68-56	68-55	68-54	68-53	68-52	68-51	68-50
		FA542	64-59	64-59	64-59	64-59	64-56	64-56	64-56	64-56
		FA542	64-58	64-58	64-58	64-58	64-55	64-55	64-55	64-55
		FA542	64-57	64-57	64-57	64-57	64-54	64-54	64-54	64-54
		FA1190	72-57	72-56	72-55	72-54	72-53	72-52	72-51	72-50
TSI-B* [SD-4A083-01]	0	FA1781	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
		FA1783	28-28	28-28	28-28	28-28	28-28	28-28	28-28	28-28
		FA1784	28-26	28-26	28-21	28-21	28-12	28-12	28-07	28-07
		FA1785	28-15	28-15	28-15	28-15	28-14	28-14	28-14	28-14
	1	FA1781	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
		FA1783	40-28	40-28	40-28	40-28	40-28	40-28	40-28	40-28
		FA1784	40-26	40-26	40-21	40-21	40-12	40-12	40-07	40-07
		FA1785	40-15	40-15	40-15	40-15	40-14	40-14	40-14	40-14
	2	FA1781	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04
		FA1783	52-28	52-28	52-28	52-28	52-28	52-28	52-28	52-28
		FA1784	52-26	52-26	52-21	52-21	52-12	52-12	52-07	52-07
		FA1785	52-15	52-15	52-15	52-15	52-14	52-14	52-14	52-14
	3	FA1781	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
		FA1783	64-28	64-28	64-28	64-28	64-28	64-28	64-28	64-28
		FA1784	64-26	64-26	64-21	64-21	64-12	64-12	64-07	64-07
		FA1785	64-15	64-15	64-15	64-15	64-14	64-14	64-14	64-14

*FA1781 could be FA1817

**DETERMINE F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE
BUFFER MEMORY C (BMC) USING TABLES**

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**TABLE F
SUSPECT BMC CIRCUIT PACKS (BIT 14)**

FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL								
			0	1	2	3	4	5	6	7	
TSI-A1 [SD-4A011-01] or	0	FA539	38-56	38-55	38-54	38-53	38-52				
		FA633	46-57	46-56	46-55	46-54	46-53	46-52	46-51	46-50	
		FA542	42-59	42-59	42-59	42-59	42-56	42-56	42-56	42-56	
		FA542	42-58	42-58	42-58	42-58	42-55	42-55	42-55	42-55	
		FA542	42-57	42-57	42-57	42-57	42-54	42-54	42-54	42-54	
TSI-A2 [SD-4A011-02]	1	FA539	60-56	60-55	60-54	60-53	60-52				
		FA633	68-57	68-56	68-55	68-54	68-53	68-52	68-51	68-50	
		FA542	64-59	64-59	64-59	64-59	64-56	64-56	64-56	64-56	
		FA542	64-58	64-58	64-58	64-58	64-55	64-55	64-55	64-55	
		FA542	64-57	64-57	64-57	64-57	64-54	64-54	64-54	64-54	
TSI-B* [SD-4A083-01]	0	FA1781	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04	
		FA1787	28-29	28-29	28-29	28-29	28-29	28-29	28-29	28-29	
	1	FA1781	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04	
		FA1787	40-29	40-29	40-29	40-29	40-29	40-29	40-29	40-29	
	2	FA1781	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04	
		FA1787	52-29	52-29	52-29	52-29	52-29	52-29	52-29	52-29	
	3	FA1781	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04	
		FA1787	64-29	64-29	64-29	64-29	64-29	64-29	64-29	64-29	

*FA1781 could be FA1817

**DETERMINE F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE
BUFFER MEMORY C (BMC) USING TABLES**

TABLE G SUSPECT CIRCUIT PACK LOCATIONS FOR ESR BIT 11											
FRAME TYPE	SPC	CIRCUIT PACK TYPE	LEVEL								
			0	1	2	3	4	5	6	7	
TSI-A1 [SD-4A011-01] or TSI-A2 [SD-4A011-02]	0	FA571 FB220	38-50 38-45	38-50 38-45	38-49 38-44	38-49 38-44	38-48 38-43	38-48 38-43	38-46 38-42	NA	
	1	FA571 FB220	60-50 60-45	60-50 60-45	60-49 60-44	60-49 60-44	60-48 60-43	60-48 60-43	60-46 60-42	NA	
TSI-B [SD-4A083-01]	0	FA1790	24-32	24-31	24-29	24-28	24-26	24-24	24-23	24-22	
		FA1789	28-34	28-34	28-34	28-34	28-34	28-34	28-34	28-33	28-33
		FA1787	28-29	28-29	28-29	28-29	28-29	28-29	28-29	28-29	28-29
	1	FA1790	36-32	36-31	36-29	36-28	36-26	36-24	36-23	36-22	
		FA1789	40-34	40-34	40-34	40-34	40-34	40-34	40-34	40-33	40-33
		FA1787	40-29	40-29	40-29	40-29	40-29	40-29	40-29	40-29	40-29
	2	FA1790	48-32	52-31	48-29	48-28	48-26	48-24	48-23	48-22	
		FA1789	52-34	52-34	52-34	52-34	52-34	52-34	52-33	52-33	
		FA1787	52-29	52-29	52-29	52-29	52-29	52-29	52-29	52-29	
	3	FA1790	60-32	60-31	60-29	60-28	60-26	60-24	60-23	NA	
		FA1789	64-34	64-34	64-34	64-34	64-34	64-34	64-33		
		FA1787	64-29	64-29	64-29	64-29	64-29	64-29	64-29		

**DETERMINE F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE
BUFFER MEMORY C (BMC) USING TABLES**

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Using printout and TABLE A, examine registers [Figure 1, Page 2] for both controllers to determine the following:

NOTE: If frame is divorced, ignore error bits in OOS controller. Use Error Source Registers for in-service controller only

1. Determine if frame is operating in DUPLEX (not divorced) or SIMPLEX (divorced) mode

2. Determine OOS controller (if any)

NOTE: A TRPF may occur where the TRPF traces back to receive TSI and, in this case, CREG 2 could contain all zeros

3. Determine type of error (APUF or PUF)

4. If APUF, check for TRPF (AUX. DATA Reg 0 contains octal 220, 221 for all XTSI frames or if bit 10 is set for TSI frames)

End of procedure

TABLE A			
STEP NUMBER	REGISTER AND BIT POSITION	BIT VALUE	INDICATION
* [1]	CREG 0, BIT 4	0	Frame is not divorced (in DUPLEX operating mode)
		1	Frame is divorced (in SIMPLEX operating mode)
[2]	CREG 0, BIT 0	0	Controller is in service
		1	Controller is OOS
† [3]	CREG 2, BIT 0	1	Error type is PUF
	CREG 2, BIT 1	1	Error type is APUF
[4]	AUX. DATA REG. 0	octal 220, 221	Transmit parity failure (TRPF)
	CREG 3, BIT 10	1	
	CREG 4, BIT 10	1	
* If bit 4 is not set to same value in both controllers, suspect a software error and notify PECC			
† If bits 0 and 1 are set to one, treat as PUF			

**DETERMINE TYPE OF ERROR AND MODE OF FRAME OPERATION,
F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE**

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```

                                CREG 2  CREG 3  CREG 4
A 41 REPT: F-LEVEL 054175146 MENUM=00000044 MICON=00000020 MSG IP
LV=0040 D0=00000000 D1=04000000 D2=00000037 D3=00000200
DATA: TSI CRITICAL REGISTERS
00000034 42000034 00000002 63400200 00000200 00000060
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00001000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000200 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000171 00000000 00036200
00000016 20637777 55555555 55555555 55555555 55555555
(20016020) 42004423 (00000002) (77400200) (00020000) 00000360
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00074400 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00001000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00020000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00036200
DATA: PERIPHERAL SYSTEM DATA
00141454 00000001 00000001 00000000 00000000 00000004
00000012 00000004 00000012 03600001 03600001 03600001
03600001
DATA: INTERRUPT SOURCE DATA
00000200 00000000 01330000 00000020 00040000
DATA: FAULT RECOGNITION ISOLATION DATA
00000031 00000003 00000250 00000000 00000003 00000000
DATA: ERROR ANALYSIS STRATEGY DATA
03025431 00000013 00000000 00000031 00000013 00000000
00000001
DATA: AUXILIARY DATA
(00001044) 00000034 20016020 02000034 02004423 00000000
20637777 00000002 00000002 63400200 77400200 00000000
00001237 00000001 00000000 00000000 00000000 00000000
10/27/98 18:39:52
#929

```

CREG 0 points to the first column of the TSI CRITICAL REGISTERS section.
 AUX DATA REG 0 points to the first column of the AUXILIARY DATA section.
 CONTR 0 REGS and CONTR 1 REGS are indicated by vertical arrows on the right side of the dump.

Figure 1 - Part of F-Level Register Dump

**DETERMINE TYPE OF ERROR AND MODE OF FRAME OPERATION,
F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE**

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[1] Using bit set in CREG 20/21
(if TSI-B), determine SPC and
level from TABLE A

[2] Extract octal time slot from
bits 17-19 in CREG 3 [TABLE B]

[3] Add 4 to octal
time slot

[4] Add result to level
obtained in Step 1

[5] Use rightmost digit as BMC
level and SPC obtained in
Step 1 to obtain primary list of
suspect circuit packs listed
in TABLE C, Page 2

AND

Page 3

TABLE A SPC AND LEVEL																
CREG	SPC								SPC							
20	1								0							
21	3								2							
BIT	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LEVEL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

TABLE B TIME SLOT EXTRACTION										
CREG 3 OCTAL DATA	7			3			0			
BIT POSITION	23	22	21	20	19	18	17	16	15	
BINARY EQUIVALENT	1	1	1	0	1	1	0	0	0	
OCTAL TIME SLOT							1	1	0	= 6

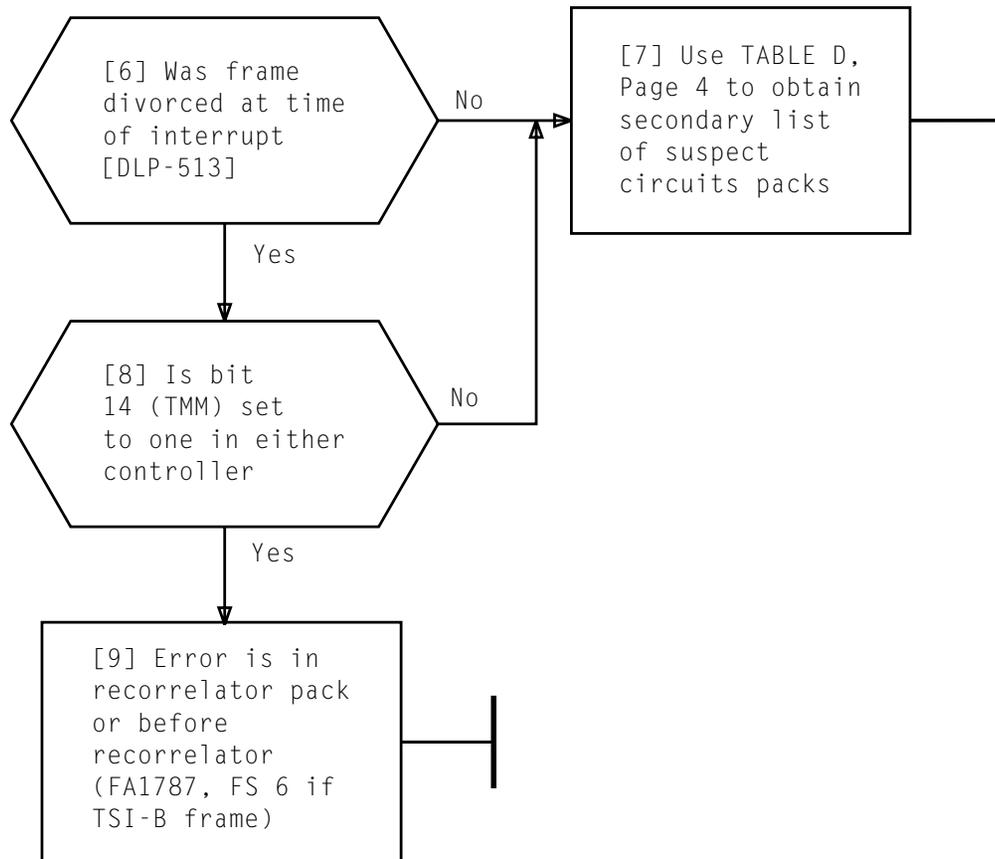
**DETERMINE F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE
BUFFER MEMORY C (BMC) USING FORMULA**

TABLE C SUSPECT BMC CIRCUIT PACK LOCATIONS										
FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A011-01] or TSI-A2 [SD-4A011-02]	0	FA633	46-57	46-56	46-55	46-54	46-53	46-52	46-51	46-50
		FA542	42-59	42-59	42-59	42-59	42-56	42-56	42-56	42-56
		FA542	42-58	42-58	42-58	42-58	42-55	42-55	42-55	42-55
		FA542	42-57	42-57	42-57	42-57	42-54	42-54	42-54	42-54
		FA1190	50-57	50-56	50-55	50-54	50-53	50-52	50-51	50-50
	1	FA633	68-57	68-56	68-55	68-54	68-53	68-52	68-51	68-50
		FA542	64-59	64-59	64-59	64-59	64-56	64-56	64-56	64-56
		FA542	64-58	64-58	64-58	64-58	64-55	64-55	64-55	64-55
		FA542	64-57	64-57	64-57	64-57	64-54	64-54	64-54	64-54
		FA1190	72-57	72-56	72-55	72-54	72-53	72-52	72-51	72-50
TSI-B* [SD-4A083-01]	0	FA1781	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
		FA1783	28-28	28-28	28-28	28-28	28-28	28-28	28-28	28-28
		FA1784	28-26	28-26	28-21	28-21	28-12	28-12	28-07	28-07
		FA1785	28-15	28-15	28-15	28-15	28-14	28-14	28-14	28-14
	1	FA1781	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
		FA1783	40-28	40-28	40-28	40-28	40-28	40-28	40-28	40-28
		FA1784	40-26	40-26	40-21	40-21	40-12	40-12	40-07	40-07
		FA1785	40-15	40-15	40-15	40-15	40-14	40-14	40-14	40-14
	2	FA1781	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04
		FA1783	52-28	52-28	52-28	52-28	52-28	52-28	52-28	52-28
		FA1784	52-26	52-26	52-21	52-21	52-12	52-12	52-07	52-07
		FA1785	52-15	52-15	52-15	52-15	52-14	52-14	52-14	52-14
	3	FA1781	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
		FA1783	64-28	64-28	64-28	64-28	64-28	64-28	64-28	64-28
		FA1784	64-26	64-26	64-21	64-21	64-12	64-12	64-07	64-07
		FA1785	64-15	64-15	64-15	64-15	64-14	64-14	64-14	64-14

*FA1781 could be FA1817

**DETERMINE F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE
BUFFER MEMORY C (BMC) USING FORMULA**

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DETERMINE F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE BUFFER MEMORY C (BMC) USING FORMULA

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TABLE D SUSPECT CIRCUIT PACK LOCATIONS FOR ESR BITS 11										
FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A011-01]	0	FA571	38-50	38-50	38-49	38-49	38-48	38-48	38-46	NA
		FB220	38-45	38-45	38-44	38-44	38-43	38-43	38-42	
TSI-A2 [SD-4A011-02]	1	FA571	60-50	60-50	60-49	60-49	60-48	60-48	60-46	NA
		FB220 FB639	60-45	60-45	60-44	60-44	60-43	60-43	60-42	
TSI-B [SD-4A083-01]	0	FA1790	24-32	24-31	24-29	24-28	24-26	24-24	24-23	24-22
		FA1789	28-34	28-34	28-34	28-34	28-34	28-34	28-33	28-33
		FA1787	28-29	28-29	28-29	28-29	28-29	28-29	28-29	28-29
	1	FA1790	36-32	36-31	36-29	36-28	36-26	36-24	36-23	36-22
		FA1789	40-34	40-34	40-34	40-34	40-34	40-34	40-33	40-33
		FA1787	40-29	40-29	40-29	40-29	40-29	40-29	40-29	40-29
	2	FA1790	48-32	48-31	48-29	48-28	48-26	48-24	48-23	48-22
		FA1789	52-34	52-34	52-34	52-34	52-34	52-34	52-33	52-33
		FA1787	52-29	52-29	52-29	52-29	52-29	52-29	52-29	52-29
	3	FA1790	60-32	60-31	60-29	60-28	60-26	60-24	60-23	NA
		FA1789	64-34	64-34	64-34	64-34	64-34	64-34	64-33	
		FA1787	64-29	64-29	64-29	64-29	64-29	64-29	64-29	

**DETERMINE F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE
BUFFER MEMORY C (BMC) USING FORMULA**

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1. Define error using PMDs [TABLE A]

End of procedure

TABLE A			
PMD-1	Growth unit	PMD-21	Bus at unit fault configuration was simplex controllers; duplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-2	Soft error configuration was duplex controllers	PMD-22	Bus at unit fault configuration was simplex controllers; duplex bus controller 1 and minor bus (IPUB) 0 suspect
PMD-3	Soft error configuration was simplex controller 0	PMD-23	Bus at unit fault configuration was simplex controllers; duplex bus controller 1 and minor bus (IPUB) 1 suspect
PMD-4	Soft error configuration was simplex controller 1	PMD-24	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 0 and minor bus (IPUB) 0 suspect
PMD-5	Transient error configuration was duplex controllers	PMD-25	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 0 and minor bus (IPUB) 1 suspect
PMD-6	Transient error configuration was simplex controller 0	PMD-26	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 1 and minor bus (IPUB) 0 suspect
PMD-7	Transient error configuration was simplex controller 1	PMD-27	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 1 and minor bus (IPUB) 1 suspect
PMD-10	Bus at unit fault configuration was duplex controllers; duplex bus controller 0 and minor bus (IPUB) 0 suspect	PMD-30	PUB fault configuration was duplex; bus major bus 0 suspect
PMD-11	Bus at unit fault configuration was duplex controllers; duplex bus controller 0 and minor bus (IPUB) 1 suspect	PMD-31	PUB fault configuration was duplex; bus major bus 1 suspect
PMD-12	Bus at unit fault configuration was duplex controllers; duplex bus controller 1 and minor bus (IPUB) 0 suspect	PMD-32	PUB fault configuration was simplex; bus major bus 0 suspect
PMD-13	Bus at unit fault configuration was duplex controllers; duplex bus controller 1 and minor bus (IPUB) 1 suspect		
PMD-14	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 0 suspect		
PMD-15	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 1 suspect		
PMD-16	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 1 suspect		
PMD-17	Bus at unit fault configuration was duplex controllers; simplex bus controller 1 and minor bus (IPUB) 0 suspect		
PMD-20	Bus at unit fault configuration was simplex controllers; duplex bus controller 0 and minor bus (IPUB) 0 suspect		

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TABLE A (Contd)

PMD-33	PUB fault configuration was simplex; bus major bus 1 suspect	PMD-47	CC fault suspect stand-by CC 1
PMD-34	Controller fault configuration was duplex controllers; controller 0 suspect	PMD-50	Interrupt from duplex failed unit
PMD-35	Controller fault configuration was duplex controllers; controller 1 suspect	PMD-51	No unit found; PBFR could not identify a unit that was responsible for the interrupt or interject
PMD-36	Controller fault configuration was simplex controllers; controller 0 suspect	PMD-52	System clock controller fault configuration was simplex system clock controllers; controller 0 suspect
PMD-37	Controller fault configuration was simplex controllers; controller 1 suspect	PMD-53	System clock controller fault configuration was simplex system clock controllers; controller 1 suspect
PMD-40	Controller fault configuration was simplex controller; bus suspect undetermined	PMD-54	System clock controller fault configuration was simplex system clock controller; and bus suspect undetermined
PMD-41	Controller fault configuration was simplex controller; bus suspect undetermined	PMD-55	System clock controller fault configuration was simplex system clock controller; and bus suspect undetermined
PMD-42	Controller fault configuration was duplex controllers; controller 0 suspect, but not conclusively. Sequence table will try to remove and diagnose mate controller on subsequent interrupts if they occur	PMD-56	System clock soft error configuration was simplex system clock controllers; controller 0 suspect
PMD-43	Controller fault configuration was duplex controllers; controller 1 suspect, but not conclusively. Sequence table will try to remove and diagnose mate controller on subsequent interrupts if they occur	PMD-57	System clock soft error configuration was simplex system clock controllers; controller 1 suspect
PMD-44	CC fault suspect active CC 0	PMD-60	System clock transient error configuration was simplex system clock controllers; controller 0 suspect
PMD-45	CC fault suspect active CC 1	PMD-61	System clock transient error configuration was simplex system clock controllers; controller 1 suspect
PMD-46	CC fault suspect stand-by CC 0		

[1] See NOTE 1. Identify failing test type and failing test number (in octal)
[Figure 1 and 2]

[2] Identify failing data bit positions (binary)

[3] Identify PBFR relative address that initiated test

[4] On TABLE A, Page 2 identify failing test function

SUBMEMBER AND DECISION REACHED	UNIT TYPE AND MEMBER NUMBER	PMD	FR PROGRAM ADDRESS WHERE DECISION WAS REACHED	STARTING ADDRESS OF PBFR
DATA: PERIPHERAL FAULT RECOGNITION RESULTS				
00040100	00000001	00004217	16242751	16234546
00401002	00000001	00004717	00000000	00000000
00401002	00000001	00006107		00005165

Figure 1 - Part of PBFR Printout With Trace Data Words 6 Through 14

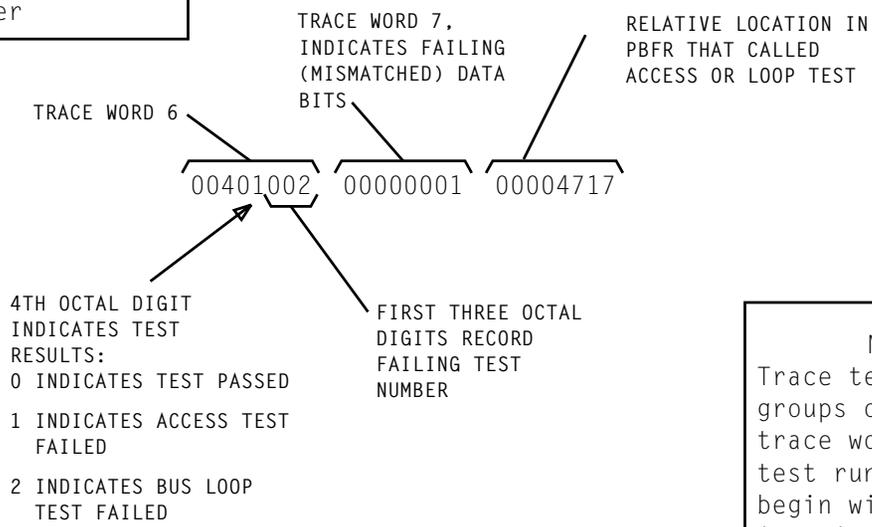
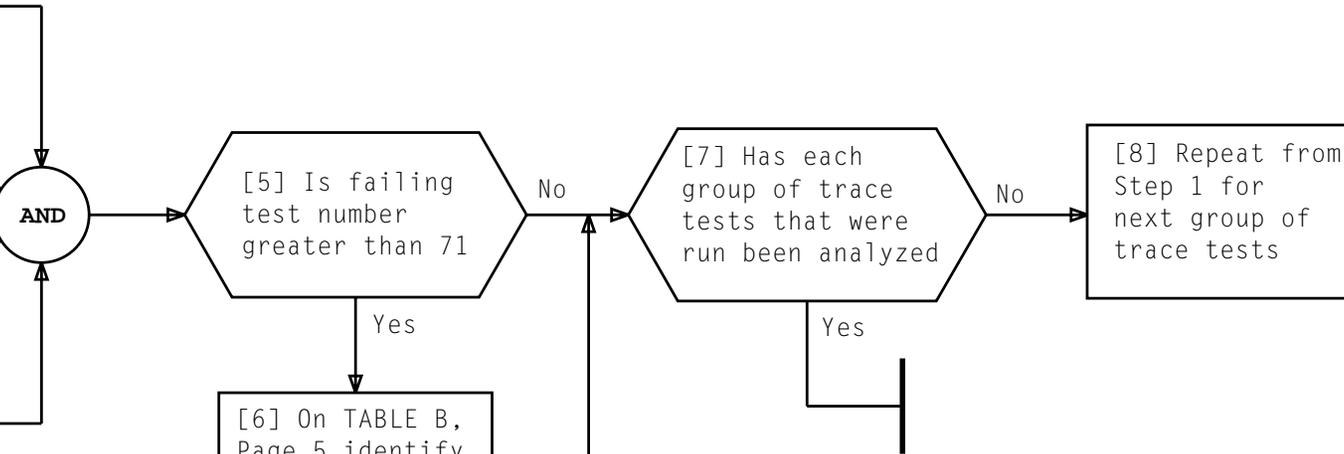


Figure 2 - Trace Word Layout

NOTE 1
Trace tests are in groups of three trace words for each test run and always begin with word 6 in printout

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TABLE A			
ACCESS TEST	PBFR TABLE OF ACCESS TESTS	ACCESS TEST	PBFR TABLE OF ACCESS TESTS
1	Reset MA, read SR to verify MA=0	30	Looparound pattern 20202020
2	Set MA, read SR to verify MA=1	31	Read reply register, verify 20202020
3	Verify ASWEPU=0 due to above orders	32	Looparound 57575757
4	Looparound pattern 00000000	33	Read reply register, verify 57575757
5	Read reply register, verify 00000000	34	Looparound pattern 40404040
6	Looparound pattern 77777777	35	Read reply register, verify 40404040
7	Read reply register, verify 77777777	36	Looparound 37373737
10	Looparound pattern 01010101	37	Read reply register, verify 37373737
11	Read reply register, verify 01010101	40	Looparound 07007007
12	Looparound 76767676	41	Read reply register, verify 07007007
13	Read reply register, verify 76767676	42	Looparound 70770770
14	Looparound pattern 02020202	43	Read reply register, verify 70770770
15	Read reply register, verify 02020202	44	Looparound 700700700
16	Looparound 75757575	45	Read reply register, verify 700700700
17	Read reply register, verify 75757575	46	Looparound 077077077
20	Looparound pattern 04040404	47	Read reply register, verify 077077077
21	Read reply register, verify 04040404	50	Looparound 00700707
22	Looparound 73737373	51	Read reply register, verify 00700707
23	Read reply register, verify 73737373	52	Looparound 77077070
24	Looparound pattern 10101010	53	Read reply register, verify 77077070
25	Read reply register, verify 10101010	54	Verify APEPU = 0 & non-TMS, TSI ASWEPU=0
26	Looparound 67676767	55	Clear ESR, read ESR, verify PFE=0 & PFO=0
27	Read reply register, verify 67676767		

TABLE A (Contd)

ACCESS TEST	PBFR TABLE OF ACCESS TESTS	ACCESS TEST	PBFR TABLE OF ACCESS TESTS
56	Looparound with EDATA (bit 10) inverted, verify PFE,PF0=0	75	Set IP1,IP2=1, send bit pattern D, verify PFE,PF0=1 MTCPU=1 BIT 35 =0
57	Looparound with EDATA (bit 11) inverted, verify PFE,PF0=0	76	Set IP1,IP2=1, send bit pattern E, verify PFE,PF0=1 MTCPU=1 BIT 35 =0
60	Looparound with EDATA (bit 12) inverted, verify PFE,PF0=0	77	Set IP1,IP2=1, send bit pattern F, verify PFE,PF0=1 MTCPU=1 BIT 35 =0
61	Looparound with EDATA (bit 13) inverted, verify PFE,PF0=0	100	Set IP1,IP2=1, send bit pattern G, verify PFE,PF0=1 MTCPU=1 BIT 35 =0
62	Looparound with EDATA (bit 14) inverted, verify PFE,PF0=0	101	Set IP1,IP2=1, send bit pattern H, verify PFE,PF0=1 MTCPU=1 BIT 35 =0
63	Looparound with EDATA (bit 15) inverted, verify PFE,PF0=0	102	Set IP1,IP2=1, send bit pattern I, verify PFE,PF0=1 MTCPU=1 BIT 35 =0
64	Looparound with EDATA (bit 16) inverted, verify PFE,PF0=0	103	Set IP1,IP2=1, send bit pattern J, verify PFE,PF0=1 MTCPU=0 BIT 35 =0
65	Looparound with EDATA (bit 17) inverted, verify PFE,PF0=0	104	Set IP1,IP2=1, send bit pattern K, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
66	Looparound with EDATA (bit 18) inverted, verify PFE,PF0=0	105	Set IP1,IP2=1, send bit pattern U, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
67	Looparound with EDATA (bit 19) inverted, verify PFE,PF0=0	106	Set IP1,IP2=1, send bit pattern L, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
70	Looparound with EDATA (bit 20) inverted, verify PFE,PF0=0	107	Set IP1,IP2=1, send bit pattern V, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
71	Looparound with EDATA (bit 21) inverted, verify PFE,PF0=0 MTCPU=1 BIT 35 =0		
72	Set IP1,IP2=1, send bit pattern A, verify PFE,PF0=1 MTCPU=1 BIT 35 =0		
73	Set IP1,IP2=1, send bit pattern B, verify PFE,PF0=1 MTCPU=1 BIT 35 =0		
74	Set IP1,IP2=1, send bit pattern C, verify PFE,PF0=1 MTCPU=1 BIT 35 =0		

TABLE A (Contd)

ACCESS TEST	PBFR TABLE OF ACCESS TESTS	ACCESS TEST	PBFR TABLE OF ACCESS TESTS
110	Set IP1,IP2=1, send bit pattern M, verify PFE,PF0=1 MTCPU=0 BIT 35 =1	120	Set IP1,IP2=1, send bit pattern Q, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
111	Set IP1,IP2=1, send bit pattern W, verify PFE,PF0=1 MTCPU=0 BIT 35 =1	121	Set IP1,IP2=1, send bit pattern 1, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
112	Set IP1,IP2=1, send bit pattern N, verify PFE,PF0=1 MTCPU=0 BIT 35 =1	122	Set IP1,IP2=1, send bit pattern R, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
113	Set IP1,IP2=1, send bit pattern X, verify PFE,PF0=1 MTCPU=0 BIT 35 =1	123	Set IP1,IP2=1, send bit pattern 2, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
114	Set IP1,IP2=1, send bit pattern O, verify PFE,PF0=1 MTCPU=0 BIT 35 =1	124	Set IP1,IP2=1, send bit pattern S, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
115	Set IP1,IP2=1, send bit pattern Y, verify PFE,PF0=1 MTCPU=0 BIT 35 =1	125	Set IP1,IP2=1, send bit pattern 3, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
116	Set IP1,IP2=1, send bit pattern P, verify PFE,PF0=1 MTCPU=0 BIT 35 =1	126	Set IP1,IP2=1, send bit pattern T, verify PFE,PF0=1 MTCPU=0 BIT 35 =1
117	Set IP1,IP2=1, send bit pattern Z, verify PFE,PF0=1 MTCPU=0 BIT 35 =1	127	Set IP1,IP2=1, send bit pattern 4, verify PFE,PF0=1

TABLE B PBFR TABLE OF ACCESS TESTS					
BIT PATTERN	PRM	PRL	BIT PATTERN	PRM	PRL
A	0000	00000000	0	7410	10101010
B	0001	01010101	P	7420	20202020
C	0002	02020202	Q	7440	40404040
D	0004	04040404	R	7507	07007007
E	0010	10101010	S	7570	70070070
F	0020	20202020	T	7577	00700707
G	0011	40404040	U	7577	77777777
H	0022	07007007	V	7576	76767676
I	0037	70070070	W	7575	75757575
J	0007	00700707	X	7573	73737373
TESTS 72-103 Skip for EST, TMS, and TSI 72-127 Skip for DIF and SCS 104-127 Skip for TAC, SYSCLK			Y	7567	67676767
			Z	7557	57575757
			1	7537	37373737
			2	7470	70770770
			3	7407	07707707
K	7400	00000000	4	7400	77077070
L	7401	01010101			
M	7402	02020202			
N	7404	04040404			

1. Define error using PMDs [TABLE A]

End of procedure

TABLE A	
PMD-001	VCFR00 allowed error analysis to resolve the error. VIC 1 failed the access test. The VIF was simplexed
PMD-002	VCFR00 allowed error analysis to resolve the error. VIC 0 failed the access test. The VIF was simplexed
PMD-003	VCFR00 decided to remove and diagnose controller 1. VIC 1 failed the access test. The VIF was duplexed
PMD-004	VCFR00 decided to remove and diagnose controller 1. VIC 0 failed the access test. The VIF was duplexed
PMD-005	VCFR00 decided to remove and diagnose controller 1. A unique failure in controller 1 has been detected. VCFR main flow leg
PMD-006	VCFR00 decided to remove and diagnose controller 0. A unique failure in controller 0 has been detected. VCFR main flow leg
PMD-007	VCFR00 allowed error analysis to resolve the error. A nonunique failure in controller 1 has been detected. VCFR main flow leg
PMD-010	VCFR00 allowed error analysis to resolve the error. A nonunique failure in controller 0 has been detected. VCFR main flow leg
PMD-011	VCFR00 allowed error analysis to resolve the error. This is the VIF DUPLEX failure for controller 0. VCFR main flow leg
PMD-012	VCFR00 allowed error analysis to resolve the error. This is the VIF DUPLEX failure for controller 1. VCFR main flow leg
PMD-013	VCFR00 took no action because of transient error. Select mode circuitry appears functional. ESM mismatch leg
PMD-014	VCFR00 decided to remove and diagnose controller 1. The ESM flip-flop in controller 0 is stuck at 0. ESM mismatch leg
PMD-015	VCFR00 decided to remove and diagnose controller 0. The ESM flip-flop in controller 0 is stuck at 0. ESM mismatch leg
PMD-016	VCFR00 decided to remove and diagnose controller 1. The ESM flip-flop in controller 1 is stuck at 1. ESM mismatch leg
PMD-017	VCFR00 decided to remove and diagnose controller 0. The ESM flip-flop in controller 0 is stuck at 1. ESM mismatch leg
PMD-020	VCFR00 took no action because of a transient error. Register test gives ATP results. Reply register mismatch routine
PMD-021	VCFR00 decided to remove and diagnose controller 0. A fault in a register in controller 0 was detected. Reply register mismatch – general purpose register test

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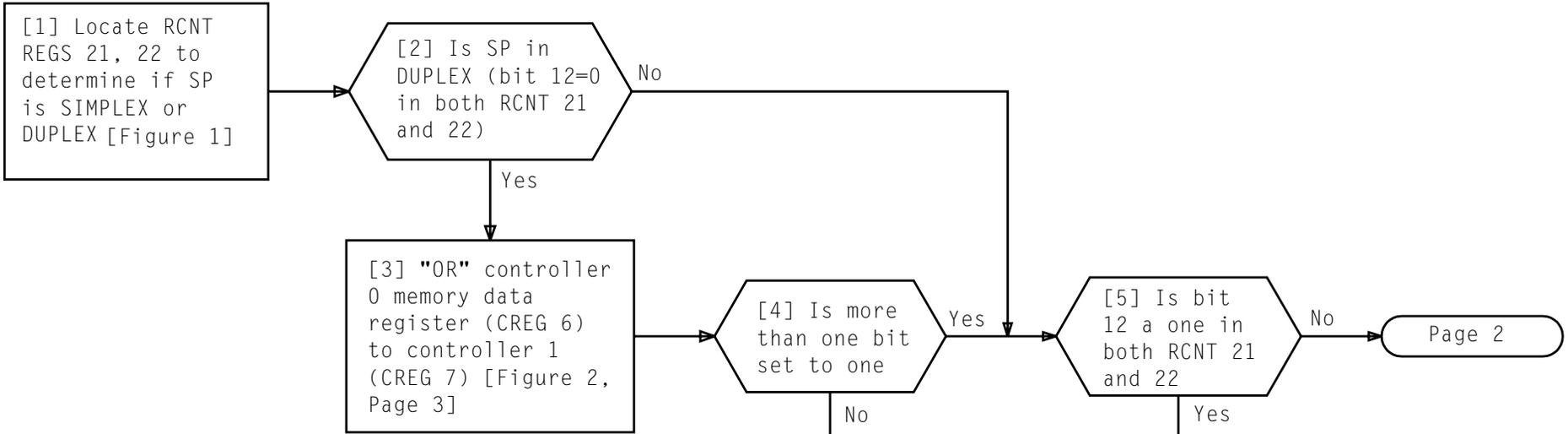
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TABLE A (Contd)

PMD-023	VCFR00 allowed error analysis to resolve the error. A single VIU 1 failed in a frame which had a protection switch up. VIC 1 was active. This VIU will be restored on the first interrupt. Multiple VIU failure leg	PMD-032	VCFR00 allowed error analysis to resolve the error. VIU's 0-3 errors implicate VIC 0. Multiple VIU failure leg
PMD-024	VCFR00 allowed error analysis to resolve the error. A single VIU failed in a frame which had a protection switch up. VIC 0 was active. This VIU will be restored on the first interrupt. Multiple VIU failure leg	PMD-033	VCFR00 allowed error analysis to resolve the error. VIU's 4-7 errors implicate VIC 1. Multiple VIU failure leg
PMD-025	VCFR00 allowed error analysis to resolve the error. VIC 1 recorded failing VIUs. Multiple VIU failure leg	PMD-034	VCFR00 decided to remove and diagnose controller 0. Controller 0 failed register state proof test. Multiple VIU leg - special register test
PMD-026	VCFR00 allowed error analysis to resolve the error. VIC 0 recorded failing VIUs. Multiple VIU failure leg	PMD-035	VCFR00 decided to remove and diagnose controller 1. Controller 1 failed register state proof test. Multiple VIU leg - special register test
PMD-027	VCFR00 allowed error analysis to resolve the error. Allow error analysis to resolve possible TSI-VIU data stream problem. Controller 0 was in service. VCFR00 passed control to error analysis	PMD-036	VCFR00 decided to remove and diagnose controller 0. Error resolved to controller 0. Input parity failure leg
PMD-030	VCFR00 allowed error analysis to resolve the error. Allow error analysis to resolve possible TSI-VIU data stream problem. Controller 1 was in service. VCFR00 passed control to error analysis	PMD-037	VCFR00 decided to remove and diagnose controller 1. Error resolved to controller 1. Input parity failure leg
PMD-031	VCFR00 allowed error analysis to resolve the error. CS0 recorded in multiple VIUs; possible controller problem. Multiple VIU failure leg	PMD-040	VCFR00 decided to remove and diagnose controller 0. Error resolved to controller 0. Clock error subroutine
		PMD-041	VCFR00 decided to remove and diagnose controller 1. Error resolved to controller 1. Clock error subroutine
		PMD-042	VCFR00 allowed error analysis to resolve the error. Restore VIU on first interject

TABLE A (Contd)

PMD-043	VCFR00 decided to remove and diagnose controller 0. A controller problem has been found. VIU interject leg
---------	--



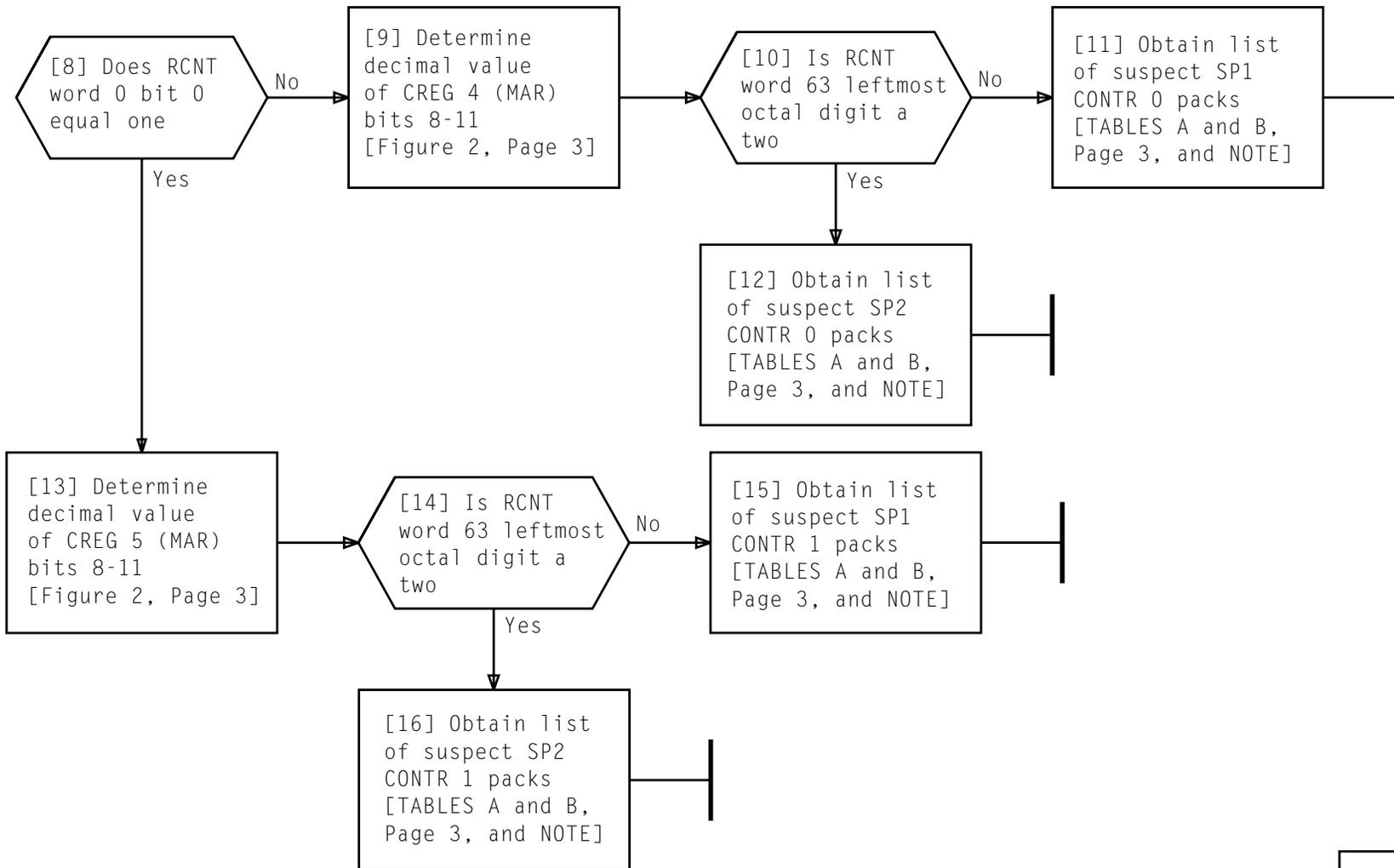
BIT 0 (DETERMINES WHICH CONTR. 0/1 IS SUSPECT)

ERROR ANALYSIS RECENT HISTORY TABLE							
00241030	10401630	00000000	00000000	00000000	00000000	00000000	00000000
00000003	00000001	00010000	77777776	00000000	00000000	00000001	
30602040	00000000	40001604	00000002	00000003	00000000		
00000000	00000044	00000052	00000004	00000012	00241030		
00402040	00000000	00000000	00000000	00070010	20000201		
00025673	00025673	00000000	00000000	00000000	00000000	00000000	
00000000	00000000	00000000	00000000	00000000	00000000	00000000	
00100001	00011702	00000101	00000000	00000000	00000000	00000000	
00000000	00000000	03471371	00000000	00000001	00000000		
04000151	00000000	10000252	00000000	00000000	00000000		
00000000	00000000	00000000	00000000	40600000			
12/30/88	02:02:33						
#247							

RCNT 21, SUSPECT CONTROLLER SOFTWARE STATUS

RCNT 22, MATE CONTROLLED SOFTWARE STATUS

Figure 1 - RCNT Register Printout



NOTE	
If this step was reached use "OR'D" bit position to select a suspect memory (column)	
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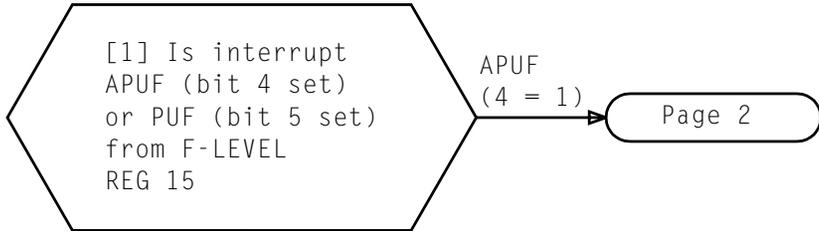
TABLE A FA634 AND FA580 PACKS						
CREG 4 BITS 8-11 DECIMAL VALUE	FA634/FA634B PACK LOCATIONS					
	SP-2/COMBINED MATRIX			SP-1/COMBINED MATRIX		
	BITS 0-8	BITS 9-17	18-23/ No bits set	BITS 0-8	BITS 9-17	18-23/ No bits set
0	62-51	62-56	62-64	60-31	60-35	60-39
1	62-52	62-57	62-65	60-32	60-36	60-40
2	62-54	62-58	62-66	60-33	60-37	60-41
3	62-55	62-59	62-67	60-34	60-38	60-42
4	70-51	70-56	70-64	68-31	68-35	68-39
5	70-52	70-57	70-65	68-32	68-36	68-40
6	70-54	70-58	70-66	68-33	68-37	68-41
7	70-55	70-59	70-67	68-34	68-38	68-42
	BITS 0-7	BITS 8-16	17-23/ No bits set	<div style="border: 1px solid black; width: 100%; height: 100%; display: flex; align-items: center; justify-content: center;"> X </div>		
8		62-60	70-60			
9		62-61	70-61			
10		62-62	70-62			
11		62-63	70-63			
FA580	Pack Locations 66-54, 66-55, 66-58, 66-59, 66-63, 66-64			64-35, 64-36, 64-37, 64-39, 64-41, 64-42		

TABLE B MEMORY REGISTER PACKS		
PACK TYPE	SP-1/COMBINED MATRIX	SP-2/COMBINED MATRIX
FA582	64-38	66-57
FA580	64-40	66-58
FA578	64-26, 27, 28	66-43, 44, 45
FA578	64-31, 32, 33	66-46, 47, 48

CREG 4

SP INTERNAL REGISTERS					
CREG 6	00000000	00000000	00000000	00000000	00002640
	00000000	05620243	00000000	00002377	00000000
	00000000	00000000	00000000	00000000	00000000
CREG 7	00000000	77777777	00000000	77770000	00000000
	00000000	00000000	00000000	50027704	00000000
	00000000	60406000	00000000	00000000	60406000
	00000000	46200000	00000000	46200000	00054406
	00000000	00070007	00000000	00002525	00000000
	37403740	37403740	37133703	37133703	34003400
	00000000	37473747	00000000	32443244	00000000
	00000000	00000000	00000000	25252525	00000000
	00000000	00000000	00000000	00000000	00000000
	00000000	77777777	00000000	77777777	00000001
	00000000	00006067	00000000	00007740	00000000
	00000000	01246033	00000000	00200000	00000000
	00000000	35160400	00000000	00000000	00000000
	00000000	13600000			

Figure 2 - SP Critical Register (CREG) Printout



PUF
(5 = 1)

BITS	K-BLOCK			CREG BITS (ROW DATA)								F-LEVEL BITS				
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STEP 3							1	1	0	1	1	1	0	0	0	0
STEP 4					0	0	1	1	0	1	1	1	0	0	0	0
STEP 6	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0
STEP 7 Octal MSN	0			1			5			6			0			

STEP 5 SP = 0

STEP 2 K = 4
STEP 4 - 4
(FROM NOTE) ———
 K = 0

[2] See EXAMPLE 1. Obtain SP column (from F-LEVEL REG 30, bits 0-3), SP row (from CREG 10, 11; bits 0-5) and SP K-block (CREG 10, 11; bits 6-8)

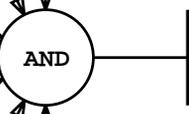
[3] Combine data from both registers with SP column being bits 0-3; SP row becomes bits 4-9

[4] See NOTE 1. Insert K-block in bit positions 10 and 11

[5] Obtain SP member number from text header [Figure 1, Page 2]

[6] Convert SP member number to binary and place result in bit positions 12-15

[7] Convert bit positions 0-16 to octal. This is MSN, MDN, TSN



EXAMPLE 1

NOTE 1
Only two data bits (10 and 11) are reserved for K-Block data; therefore, if K is 4 or 5, then subtract 4 from the K

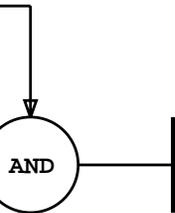
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DETERMINE MSN, MDN, OR TSN

[8] Obtain SP member number
from text of interrupt
printout [Figure 1]

[9] Locate CREG 8/9 and obtain
octal value of bits 0-11
[Figure 2]

[10] Obtain MSN, MDN, TSN by placing
SP member number (octal) in
front of value contained in
CREG 8/9 [EXAMPLE 2]



```

REPT F-LEVEL 014242534 MENU=00043101 MICON=000000222 MSG STARTED
LV=0040 D0=00000002 D1=70000000 D2=00000000 D3=00000000
SPER REMOVED AND REQUESTED DIAGNOSTICS SP 0 CONTR 0
SPER MATRIX INHIBIT SP 0 CONTR 1
DATA: E-IEVFL
  
```

SP MEMBER NUMBER

Figure 1 - Text Header

```

                CREG 8  CREG 9
SP INTERNAL REGISTERS
00000000 00000000 00000000 00000000 00000000 00002640
00000000 05620243 0001560 0001560 00000467 00000467
00000000 00000000 00000000 00000000 00000000 00000000
00000000 77777777 00000000 77770000 00000000 42424242
00000000 00000000 00000000 50027704 00000000 50027704
00000000 60406000 00000000 00000000 00000000 60406000
00000000 46200000 00000000 46200000 00000000 00054406
00000000 00070007 00000000 00002525 00000000 37523752
37403740 37403740 37133703 37133703 34003400 34003400
00000000 37473747 00000000 32443244 00000000 77777777
00000000 00000000 00000000 25252525 00000000 52525252
00000000 00000000 00000000 00000000 00000000 00000000
00000000 77777777 00000000 77777777 00000000 00000001
00000000 00006067 00000000 00007740 00000000 02500200
00000000 01246033 00000000 00200000 00000000 01404043
00000000 35160400 00000000 00000000 00000000 34200252
00000000 13600000
  
```

Figure 2 - P/O F-Level Printout

SP MEMBER NUMBER = 0
CREG 8/9 = 1560
MSN, MDN, TSN = 01560

EXAMPLE 2

DETERMINE MSN, MDN, OR TSN

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1. Define error using PMDs [TABLE A]

End of procedure

TABLE A	
PMD-001	Millisecond clock values stored at time of interrupt were unequal. Testing proved to show clock in CONTR 0 was at fault
PMD-002	Millisecond clock values stored at time of interrupt were unequal. Testing proved to show clock in CONTR 1 was at fault
PMD-003	Millisecond clock values stored at time of interrupt were unequal. Further testing was unable to find problem. Error exits to error analysis preparation when one controller is out of service
PMD-004	CONTR 0 was only controller in service at time of interrupt. Its clock activity does not set to 0
PMD-005	CONTR 1 is only controller in service at time of interrupt. Its clock activity does not set to 1
PMD-006	CONTR 0 is only controller in service at time of interrupt. R0 does not set to active bus
PMD-007	CONTR 1 is only controller in service at time of interrupt. R0 does not set to active bus
PMD-010	Only CONTR 0 was in service at time of interrupt. Its memory parameters indicate internal bus failure
PMD-011	Only CONTR 1 was in service at time of interrupt. Its memory parameters indicate internal bus failure
PMD-012	Only CONTR 0 was in service at time of interrupt. It has unique error
PMD-013	Only CONTR 1 was in service at time of interrupt. It has unique error
PMD-014	CONTR 0 is in service at time of interrupt and analog timer has timed out; ie, on-line controller is assumed to have stopped longer than 100 ms but stop flop of controller is assumed at fault
PMD-015	CONTR 1 is in service at time of interrupt and analog timer has timed out; ie, on-line controller is assumed to have stopped longer than 100 ms but stop flop of controller is assumed to be at fault
PMD-016	Memory mismatch caused AINT interrupt. Memory access REG MAR and MDR were found equal. CONTR 0 matcher detector is in error
PMD-017	Memory mismatch caused AINT interrupt. Memory access REG MAR and MDR were found equal. CONTR 1 matcher detector is in error
PMD-020	CONTR 0 has bad clock circuit
PMD-021	CONTR 1 has bad clock circuit
PMD-022	CONTR 1 has bad error source register
PMD-023	CONTR 0 has bad error source register
PMD-024	CONTR 0 has failed memory parameter check of fixed memory words. Suspect internal busing system or memory access circuit
PMD-025	CONTR 1 failed memory parameter check of fixed memory words. Suspect internal busing system or memory access circuit

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TABLE A (Contd)

PMD-026	Both controllers AINT and ASWF are reset. Suspect transient or ESR	PMD-044	CONTR 0 received on F/F, R0, failed
PMD-027	Unique error in CONTR 0 has AINT unique error involving an SR	PMD-045	CONTR 0 has error in matrix interface or matrix sequencing logic
PMD-030	Unique error in CONTR 1 has AINT unique error involving SR	PMD-046	CONTR 1 has error in matrix interface or matrix sequencing logic
PMD-031	No controller is on-line according to status. Force CONTR 0 on-line by assuming CONTR 0 simplex failure	PMD-047	Duplexed SP interrupt. Fault isolated to SP simplex matrix
PMD-032	CONT 0 failed. Suspect analog timer circuitry	PMD-050	Matrix interrupt occurred; testing failed to find cause
PMD-033	CONTR 1 failed. Suspect analog timer circuitry	PMD-051	Matrix error in CONTR 0 of simplex SP detected, retired, and failed again
PMD-034	One or both controllers had analog timer timed out. Call store status said it was not stopped. Thus, it was left stopped by unknown program for excessive amount of time	PMD-052	Matrix error in CONTR 1 of simplex SP detected, retired, and failed again
PMD-035	CONTR 1 has unique error. Found after ASWF interrupt involving SP	PMD-053	Simplex SP had matrix error which could not be found
PMD-036	CONTR 0 has unique error. Found after ASWF interrupt involving SP	PMD-054	Simplex SP had matrix error which could not be found
PMD-037	CONTR 0 has peripheral sequencer time-out failure	PMD-055	Universal row accessed by duplexed controller but row was out of range. Multilication detection number already loaded in recent history table for error analysis
PMD-040	CONTR 1 has peripheral sequencer time-out failure	PMD-056	Unequipped portion of matrix accessed in simplex SP with CONTR 0 active
PMD-041	SP was duplexed. Only CONTR 0 recorded software error such as invalid OPCODE. Both would have recorded error if it existed; CONTR 0 recorded it incorrectly	PMD-057	Unequipped portion of matrix accessed in simplex SP with CONTR 1 active
PMD-042	SP was duplexed. Only CONTR 1 recorded software error such as invalid OPCODE. Both would have recorded error if it existed; CONTR 1 recorded it incorrectly	PMD-060	Miscellaneous row accessed by duplexed controller but row was out of range. Multilication detection number already loaded in recent history table for error analysis
PMD-043	CONTR 1 received on F/F, R0, failed		

TABLE A (Contd)

PMD-061	Unequipped portion of matrix accessed in simplex SP with CONTR 0 active	PMD-100	DPOWL full, bit set in both controllers. MDNs loaded in RCNT history table. SP was duplexed.
PMD-062	Unequipped portion of matrix accessed in simplex SP with CONTR 1 active	PMD-101	DPOWL full, in CONTR 0 while simplexed. Audit MDN loaded into RCNT history table
PMD-063	Matrix error found in duplex SP	PMD-102	DPOWL full, in CONTR 1 while simplexed. Audit MDN loaded into RCNT history table
PMD-064	Matrix error found in simplex SP with CONTR 1 on line	PMD-103	CONTR 0 has invalid INVOP ESR bit stuck or failing pest bit
PMD-065	Transient matrix failure found in duplexed SP	PMD-104	CONTR 1 has invalid INVOP ESR bit stuck or failing pest bit
PMD-066	CONTR 0 has memory access mismatch. Controllers were duplexed. Error occurred during a peripheral order access	PMD-105	CONTR 0 simplexed. Invalid ESR bit set
PMD-067	CONTR 1 has memory access mismatch. Controllers were duplexed. Error occurred during peripheral order access	PMD-106	CONTR 1 simplexed. Invalid ESR bit set
PMD-070	Memory access mismatch detected while controllers were duplexed. Further testing unable to find error. Error occurred during CC order access	PMD-107	CONTR 0 has analog timer timed out. SP stopped
PMD-071	CONTR 0 failed PU reply bus register test	PMD-110	CONTR 1 has analog timer timed out. SP stopped
PMD-072	CONTR 1 failed PU reply bus register test	PMD-111	ASWF recorded in ESR of duplexed SP. PUF not recorded in CC
PMD-073	CONTR 0 failed and caused PU reply bus register mismatch	PMD-112	ASWF recorded in ESR of simplexed SP. PUF not recorded in CC
PMD-074	CONTR 1 failed and caused PU reply bus register mismatch	PMD-113	ASWF recorded in ESR of simplexed SP. PUF not recorded in CC
PMD-075	SP detected invalid OPCODE. Audit MDN number loaded in RCNT history table	PMD-114	Ring counters mismatched between controllers
PMD-076	SP detected invalid OPCODE. Audit MDN number loaded in RCNT history table	PMD-115	Ring counters mismatched between controllers
PMD-077	SP detected invalid OPCODE. Audit MDN number loaded in RCNT history table	PMD-116	CONTR 0 has matrix error in simplex SP
		PMD-117	SP recorded ASWF interrupt; CC recorded APUF in (INS) register and matrix errors were set. No error processing could be done. Remove and DGN a controller. Pest the matrix so DGN can complete

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TABLE A (Contd)

PMD-120	SP recorded ASWF interrupt, CC recorded APUF in (INS) register and matrix errors were set. No error processing could be done. Remove and DGN controller 0 and pest the matrix so DGN could complete.	PMD-201	Error in DT interface found. CONTR 0 implicated by fault recognition
PMD-121	SP recorded ASWF interrupt, CC recorded APUF in (INS) register and matrix errors were set. No error processing could be done. Remove and DGN controller 1 and pest the matrix so DGN could complete.	PMD-202	Error in DT interface found. CONTR 1 implicated by fault recognition
PMD-122	SP recorded ASWF. CC did not remove and diagnose controller 0 because it has errors set	PMD-203	Mismatch in DT interface found. Fault recognition determined SP CONTR 0 faulty
PMD-123	SP recorded ASWF. CC did not remove and diagnose controller 1 because it has errors set	PMD-204	Mismatch in DT interface found. Fault recognition determined SP CONTR 1 faulty
PMD-124	Simplex controller 0 digit buffer not full but ESR had INTJ set	PMD-205	Unique error found in simplex SP, CONTR 0
PMD-125	Simplex controller 1 digit buffer not full but ESR had INTJ set	PMD-206	Unique error found in DT interface. SP CONTR 1 simplex
PMD-126	SP duplexed. Digit buffer not full. ESR INTJ bit set in CONTR 0 only	PMD-207	Transient DT interface error detected by CONTR 0. All link tests passed
PMD-127	SP duplexed. Digit buffer not full. ESR INTJ bit set in CONTR 1 only	PMD-210	Transient DT interface error detected by CONTR 1. All link tests passed
PMD-130	CONT 0 simplex. Digit buffer full. Suspect software error and unload buffer	PMD-310	AINT memory mismatch occurred. CONT 0 accessed out-of-range address. Incompatible with state of active sequencer
PMD-131	CONTR 1 simplex. Digit buffer full. Suspect software error and unload buffer	PMD-311	AINT memory mismatch occurred. CONT 1 accessed out-of-range address. Incompatible with state of active sequencer
PMD-132	SP duplexed. Digit buffer full. Suspect software error and unload buffer	PMD-312	AINT memory mismatch occurred. Tests run on memory address and data registers were ATP
		PMD-313	ASW interrupt caused by sequencer mismatch when CONTR 0 failed to stop in valid stopping state for peripheral access of SP
		PMD-314	ASW interrupt caused by sequencer mismatch when CONTR 1 failed to stop in valid stopping state for peripheral access of SP

TABLE A (Contd)

PMD-315	Client sequencer found active in CONTR 0. Incorrect client	PMD-326	SPRF suspected MF out. Sequencer in error. Retry ATP
PMD-316	Client sequencer found active in CONTR 1. Incorrect client	PMD-327	DPO sequencer in CONTR 0 mismatched and is not faulty
PMD-317	CONTR 0 incorrectly sensed a sequencer mismatch	PMD-330	DPO sequencer in CONTR 1 mismatched and is faulty
PMD-320	CONTR 1 incorrectly sensed a sequencer mismatch	PMD-331	SDR sequencer in CONTR 0 mismatched and is faulty
PMD-321	Executive sequencer mismatched. No apparent reason for mismatch found.	PMD-332	SDR sequencer in CONTR 1 mismatched and is faulty
PMD-322	Executive sequencer mismatched. CONTR 0 faulty	PMD-333	CONTR 0 failed a general register check. SPFR ran a memory mismatch test but did not find a suspect controller. Address of register checked is in the J register
PMD-323	Executive sequencer mismatched. CONTR 1 faulty	PMD-334	CONTR 1 failed a general register check. SPFR ran a memory mismatch test but did not find a suspect controller. Address of register checked is in the J register
PMD-324	MF out; sequencer active. Mismatch occurred. CONTR 0 faulty		
PMD-325	MF out; sequencer active. Mismatch occurred. CONTR 1 faulty		

1. Define error using PMDs [TABLE A]

End of procedure

TABLE A			
PMD-001	APUF (Duplex) no error found	PMD-033	Unique error in active only; pested mismatch and hit-timed; then error is gone
PMD-002	PUF (Duplex) no error found; ASWF set in active only	PMD-034	Unique error in mate only; pested mismatch and hit-timed; then error in active only
PMD-003	PUF (Duplex) no error found; ASWF set in mate only	PMD-035	Unique error in mate only; pested mismatch and hit-timed; then error in mate only
PMD-004	PUF (Duplex) no error found	PMD-036	Unique error in mate only; pested mismatch and hit-timed; then error in both controllers
PMD-005	(Duplex) no CC PUF or APUF error source found	PMD-037	Unique error in mate only; pested mismatch and hit-timed; then error was gone
PMD-011	Clock error in active only; hit-timed and clock error still present	PMD-040	Unique error in both controllers; pested mismatch and hit-timed; then error was inactive only
PMD-012	Clock error in active only; hit-timed and clock error is gone	PMD-041	Unique error in both controllers; pested mismatch and hit-timed; then error in standby only
PMD-014	Clock error in mate only; hit-timed and clock error is still present	PMD-042	Unique error in both controllers; pested mismatch and hit-timed; then error in both controllers
PMD-015	Clock error in mate only; hit-timed and clock error is gone	PMD-043	Unique error in both controllers; pested mismatch and hit-timed; then error is gone
PMD-017	Clock error in both controllers; hit-timed and clock error in active only	PMD-044	Mismatch found in active only
PMD-021	Clock error in both controllers; hit-timed and clock error in mate only	PMD-045	Mismatch found in mate only
PMD-025	Clock error in both controllers; hit-timed and clock error in both controllers	PMD-046	Mismatch found in both controllers
PMD-026	Clock error in both controllers; hit-timed and error is gone in both	PMD-047	Firmware detected errors found in both controllers
PMD-030	Unique error in active only; pested mismatch and hit-timed; then error in active only	PMD-050	Firmware detected errors in active controller
PMD-031	Unique error in active only; pested mismatch and hit-timed; then error in mate only	PMD-051	Firmware detected errors in standby controller
PMD-032	Unique error in active only; pested mismatch and hit-timed; then error in both controllers	PMD-054	Microprocessor in both controllers has detected a normal buffer overflow

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TABLE A (Contd)

PMD-056	Microprocessor in both controllers has detected a normal maintenance buffer overflow	PMD-103	Highest priority mismatch found in active only; reset divorce in mate and retry order; order fails in active only
PMD-060	Microprocessor in both controllers has detected an invalid macro	PMD-104	Highest priority mismatch found in active only; reset divorce in mate and retry order; order fails in mate only
PMD-061	Microprocessor in both controllers has detected a task table overflow	PMD-105	Highest priority mismatch found in active only; reset divorce in mate and retry order; order fails in both controllers
PMD-062	Microprocessor in both controllers has detected an error condition	PMD-106	Highest priority mismatch found in active only; reset divorce in mate and retry order; order passes in both controllers
PMD-064	Microprocessor in both controllers has detected an invalid macro	PMD-107	Highest priority mismatch found in standby only; reset divorce in active and retry order; order fails in active only
PMD-065	Microprocessor in both controllers has detected a task table overflow	PMD-110	Highest priority mismatch found in mate only; reset divorce in active and retry order; order fails in mate only
PMD-066	Microprocessor in both controllers has detected an error condition	PMD-111	Highest priority mismatch found in standby only; reset divorce in active and retry order; order fails in both controllers
PMD-070	The peripheral order was no good	PMD-112	Highest priority mismatch found in standby only; reset divorce in active and retry order; order passes in both controllers
PMD-071	Unique error in active controller; retry the order and active still has unique error	PMD-113	Highest priority mismatch found in both controllers; retry order; order fails in active only
PMD-072	Unique error in active controller; retry the order and active has no error	PMD-114	Highest priority mismatch found in both controllers; retry order; order fails in mate only
PMD-073	Unique error in mate controller; retry the order and mate still has unique error	PMD-115	Highest priority mismatch found in both controllers; retry order; order fails in both controllers
PMD-074	Unique error in mate controller; retry the order and mate has no error		
PMD-075	T1 line mismatch in active only		
PMD-076	T1 line mismatch in standby only		
PMD-077	T1 line mismatch in both controllers		
PMD-100	Low frequency clock mismatch in active only		
PMD-101	Low frequency clock mismatch in standby only		
PMD-102	Low frequency clock mismatch in both controllers		

TABLE A (Contd)

PMD-116	Highest priority mismatch found in both controllers; retry order; order passes in both controllers	PMD-154	Microprocessor has detected a normal maintenance buffer overflow
PMD-117	Firmware detected errors in active controller	PMD-156	Microprocessor has detected a normal maintenance buffer overflow
PMD-120	Unique error in active controller during a "buffer read" order	PMD-160	Microprocessor has detected an invalid macro
PMD-121	Unique error in mate controller during a "buffer read" order	PMD-161	Microprocessor has detected a task table overflow
PMD-122	Highest priority mismatch found only in active controller during a "buffer read" order	PMD-162	Microprocessor has detected an error condition
PMD-123	Highest priority mismatch found only in mate controller during a "buffer read" order	PMD-164	Microprocessor has detected an invalid macro
PMD-124	Highest priority mismatch found in both controllers during a "buffer read" order	PMD-165	Microprocessor has detected a task table overflow
PMD-125	Firmware detected errors in standby controller	PMD-166	Microprocessor has detected an error condition
PMD-130	APUF (simplex); no error found	PMD-170	Peripheral order was no good
PMD-131	PUF (simplex); no error found	PMD-171	Unique error found; retry the order; unique error was still present
PMD-132	(Simplex); no CC PUF or APUF error source found	PMD-172	Unique error found; retry the order; unique error was gone
PMD-141	Clock error found; hit-timed and clock error was still present	PMD-173	T1 line mismatch found
PMD-142	Clock error found; hit-timed and clock error was gone	PMD-174	Low frequency clock mismatch found
PMD-150	Unique error found; pested mismatch and hit-timed; error was still present	PMD-175	"Sequencer", "internal bus", "reply register", or "LUSP M-bit" (DIF-E1) mismatch found
PMD-151	Unique error found; pested mismatch and hit-timed; error was gone	PMD-176	Firmware detected errors
PMD-152	Mismatch found in T1 line, low frequency clock, internal reply register or LUSP M-bit (DIF-E1 only)	PMD-177	Unique error found during a "buffer read" order
PMD-153	Firmware detected errors	PMD-200	CONSISTENCY CHECK – HARD LOM STB – DGN INAPUT set in ACT and STB, IAS zero in STB
		PMD-201	CONSISTENCY CHECK – HARD LOM ACT – DGN INAPUT set in ACT, reset in STB, IAS zero in STB
		PMD-202	CONSISTENCY CHECK – HARD LOM STB – DGN INAPUT set in ACT, reset in STB, IAS nonzero in STB

TABLE A (Contd)

PMD-203	CONSISTENCY CHECK – TRANSIENT LOM STB – DGN INAPUT reset in ACT and STB	PMD-222	HARDCORE PARITY ERROR
PMD-204	CONSISTENCY CHECK – HARD LOM STB – DGN INAPUT reset in ACT, set in STB, IAS zero in STB	PMD-240	INTERJECT FILTER – DIU Restore DIU – Cleanup Consistency check passes, common alarm, DS120 line error
PMD-205	CONSISTENCY CHECK – HARD LOM ACT – DGN INAPUT reset in ACT, set in STB, IAS nonzero in STB	PMD-241	INTERJECT FILTER – DIU Force DIU – DGN – Cleanup Consistency check passes, common alarm
PMD-206	CONSISTENCY CHECK – TRPF TRANSIENT Force STB INAPUT reset in ACT, simplex frame, INTJ from O/S contr	PMD-242	INTERJECT FILTER – HARD LOM ACT – DGN Multiple DIU's alarming
PMD-207	INTERJECT FILTER – SOFTWARE No Action Consistency check passes, normal DB overflow	PMD-301	BASE FILTER – DIU Force Digroup – DGN DIU BLM, Digroup failure
PMD-210	INTERJECT FILTER – HARD LOM ACT – DGN Consistency check passes, duplex frame, DB overflow, but pointers are inconsistent	PMD-302	BASE FILTER – DIU Force DIU – DGN BLM, routine diagnostic failure, implicates DIU
PMD-211	INTERJECT FILTER – HARD Restore ACT Consistency check passes, simplex frame, DB overflow, but pointers are inconsistent	PMD-303	INVALID
PMD-215	INTERJECT FILTER – HARD LOM ACT – DGN Force DIU if I/S else Restore SUBJ Consistency check passes, duplex frame, PSW audit failure	PMD-304	BASE FILTER – DIU Force Digroup – DGN DIU BLM, routine diagnostic failure, implicates digroup
PMD-216	INTERJECT FILTER – HARD Restore ACT Force DIU if I/S else Restore SUBJ Consistency check passes, simplex frame, PSW audit failure	PMD-305	BASE FILTER – HARD Hit Time BLM, illegitimate report, duplex frame
PMD-217	INTERJECT FILTER – TRANSIENT LOM ACT – DGN Consistency check passes, duplex frame, but no sources found	PMD-306	BASE FILTER – HARD Hit Time BLM, illegitimate report, simplex frame
PMD-220	INTERJECT FILTER – TRANSIENT Restore ACT – Force STB Consistency check passes, simplex frame, but no sources found	PMD-307	BASE FILTER – DIU Force DIU – DGN BLM, illegitimate report from spare DIU – not PSW
PMD-221	INTERJECT FILTER – TRANSIENT Restore ACT – Audit 27 DB overflow from DIF out of polling range	PMD-330	RAM errors found in standby only or in both controllers (DIF-E1 only)
		PMD-331	RAM errors found in active controller only and standby may have F/W errors (DIF-E1 only)
		PMD-340	Firmware detected errors in active controller with RAM errors (DIF-E1 only)
		PMD-341	Firmware detected errors in standby controller with RAM errors (DIF-E1 only)

TABLE A (Contd)

PMD-350	Firmware detected errors found and RAM errors (DIF-E1 only – APUF)
PMD-360	Firmware detected errors found and RAM errors (DIF-E1 only – PUF)
PMD-373	Hardware access test failure
PMD-374	Interrupt from a growth frame
PMD-375	Interrupt from an unequipped frame
PMD-377	Interrupt from a duplex failed frame

1. Enter **RMV:SCLK 0,NCSU 0!**

NOTE: Bit 12 of word A indicates controller status. If 0, use word C in CONTR 0. If 1, use word C in CONTR 1

2. Identify oscillator using bits 0, 1, and 2 of word C and TABLE A [Figure 1]

3. At oscillator, disable oscillator using **ENABLE/DISABLE** switch

4. Locate cable connectors at NCSU [TABLE A]

5. Remove cable connectors and inspect for broken connectors, broken leads, etc.

6. Reseat cable connectors

7. At oscillator identified in Step 2, remove and reseat cable connector (labeled **D/A INPUT/OUTPUT**)

8. Enable oscillator using **ENABLE/DISABLE** switch on oscillator

9. Enter **RST:SCLK 0,NCSU 0!**

End of procedure

DATA:SCLK CRITICAL REGISTERS

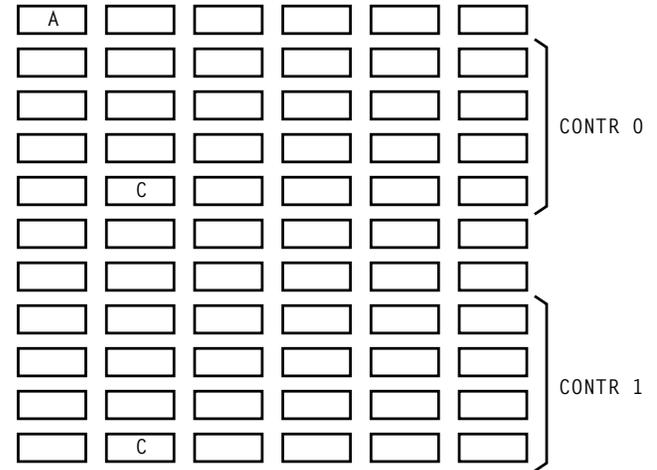
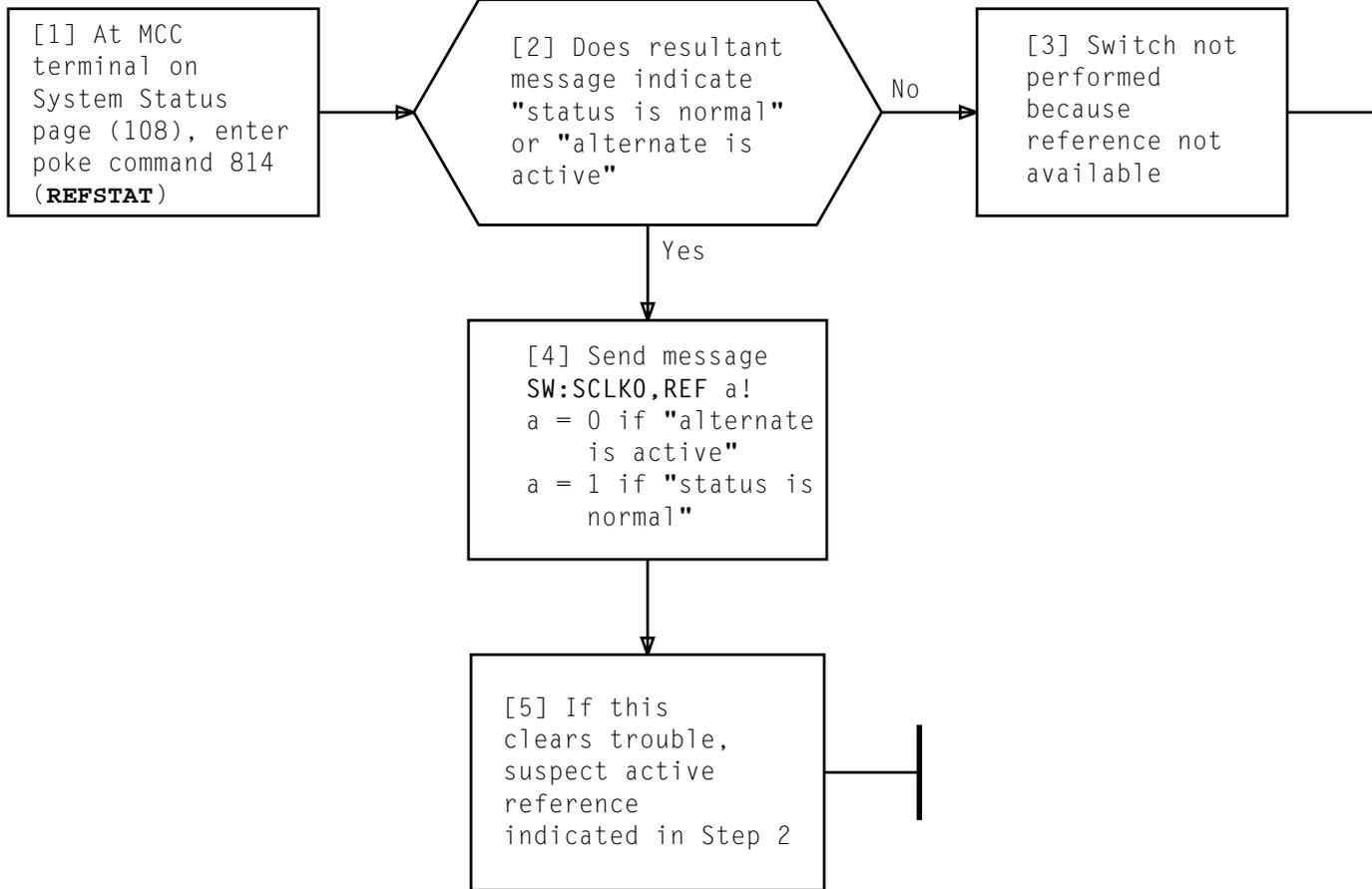
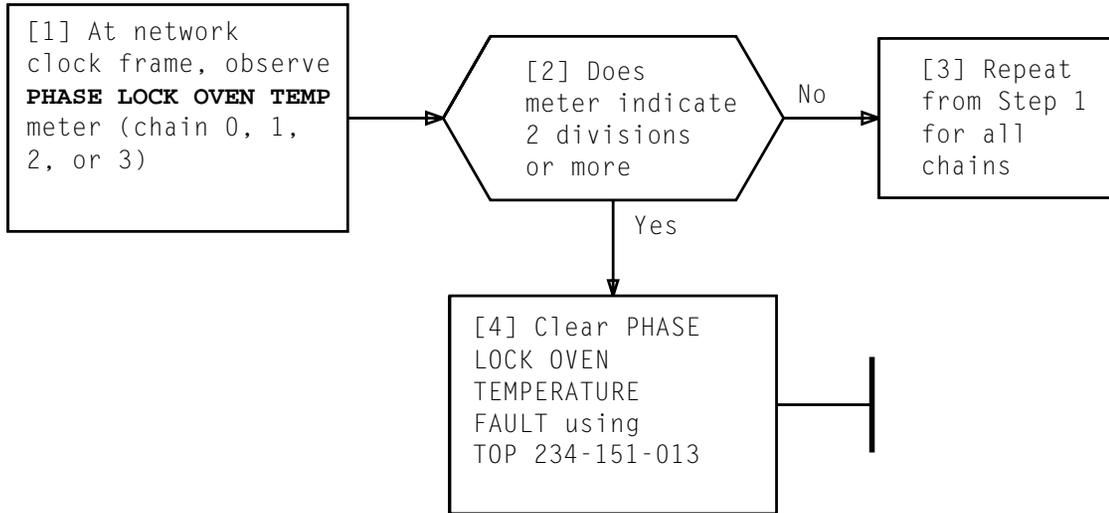


Figure 1 – SCLK Critical Registers

TABLE A				
BIT			OSC	NCSU CONNECTORS
2	1	0		
0	0	0	0	0-48-56
0	0	1	1	0-52-56
0	1	0	2	0-52-58
0	1	1	3	0-48-58
1	0	0	0	0-48-56
1	0	1	1	0-52-56
1	1	0	2	0-52-58
1	1	1	3	0-48-58





CHECK PHASE LOCK OVEN TEMP METER

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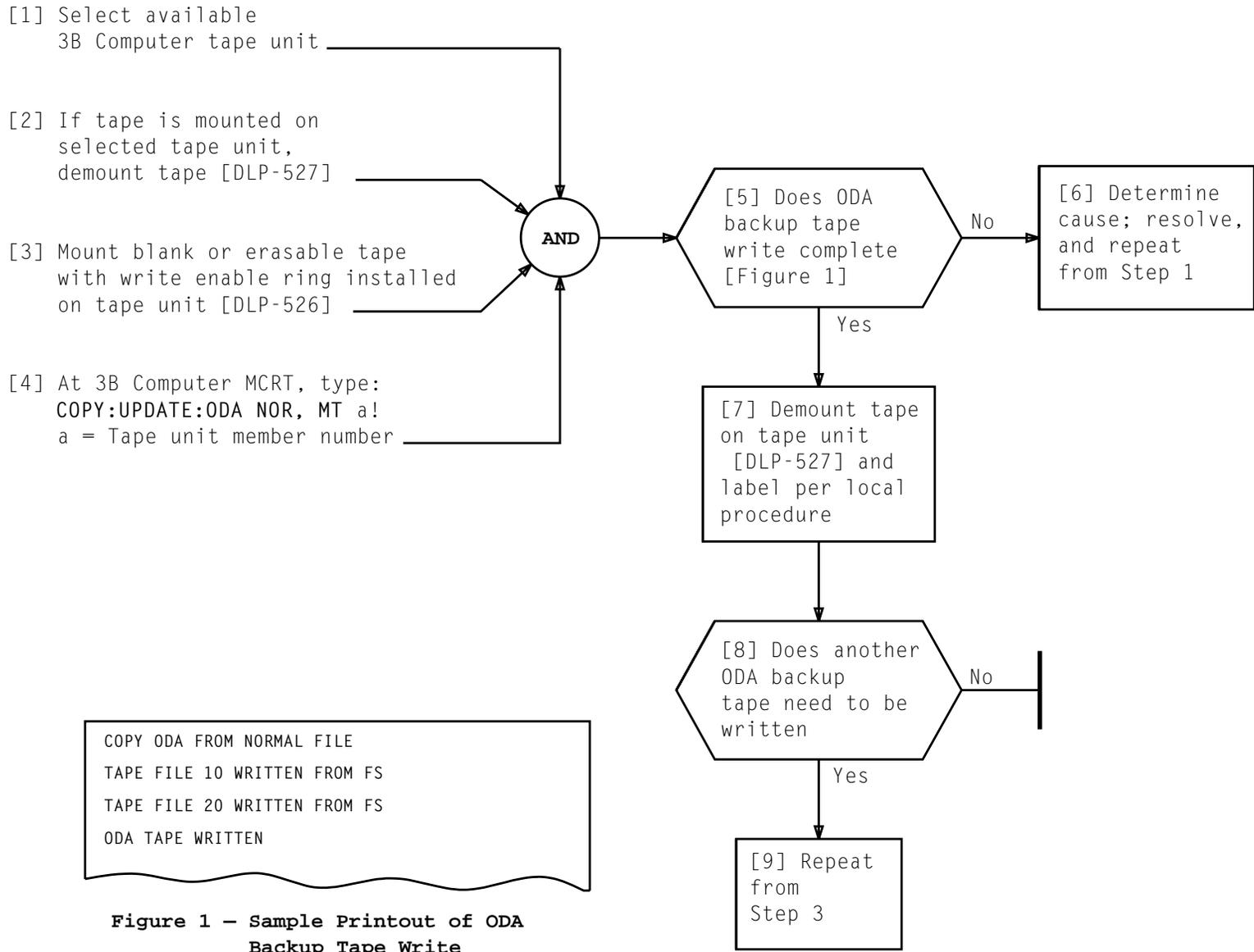


Figure 1 - Sample Printout of ODA Backup Tape Write

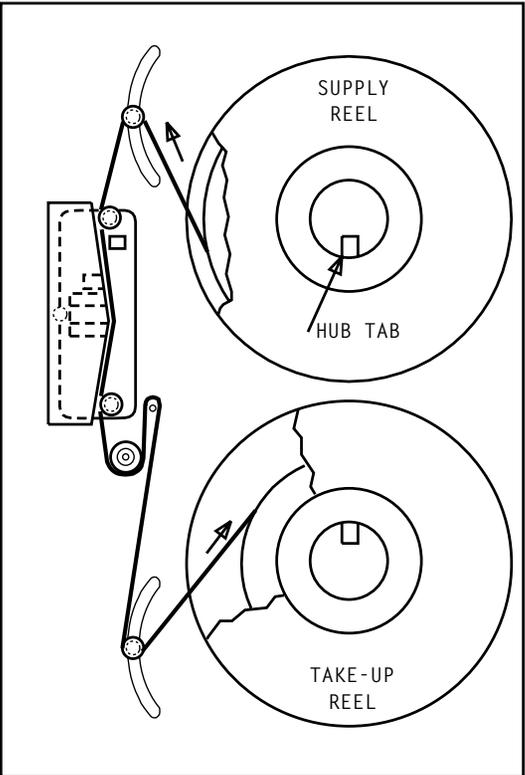
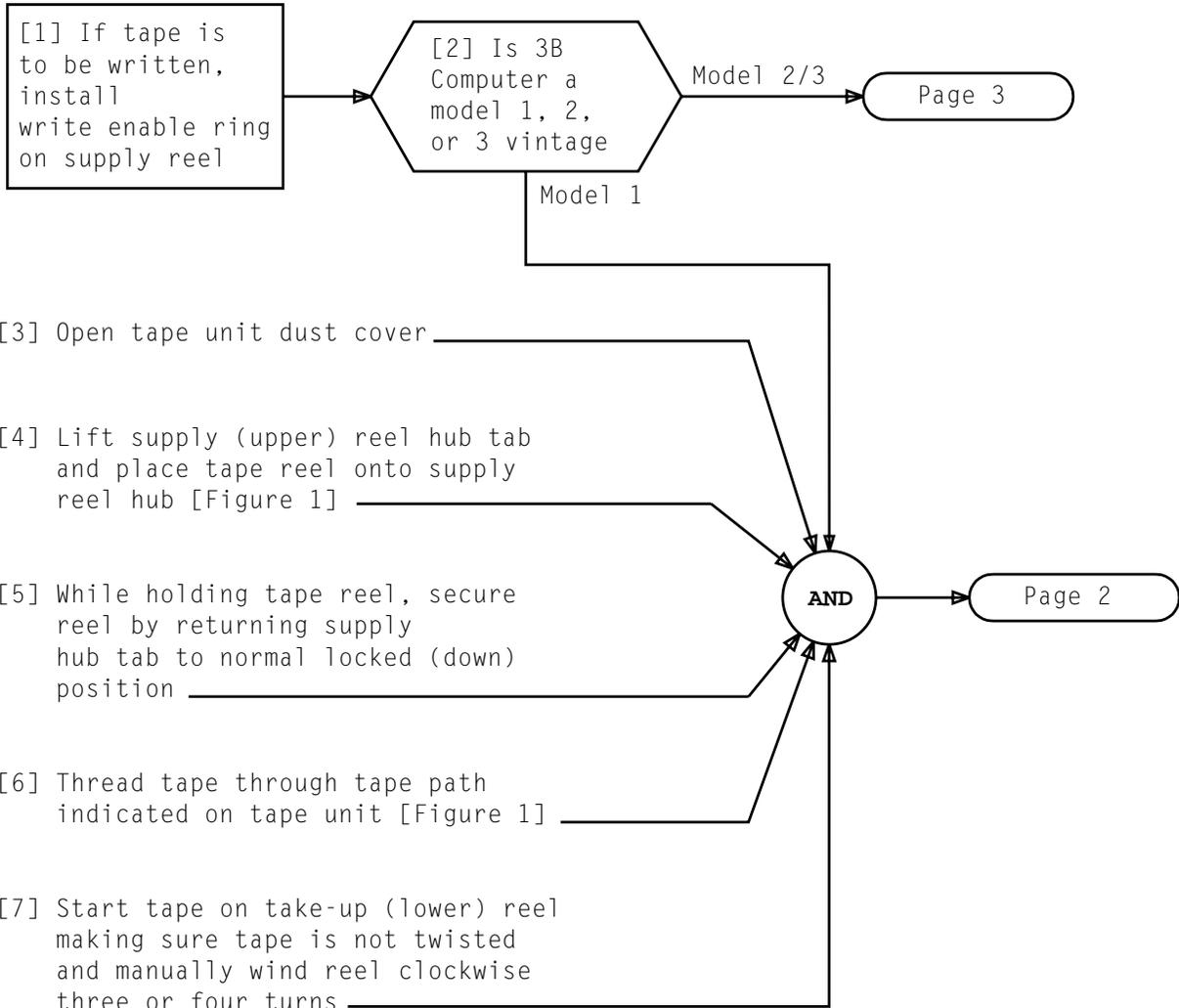
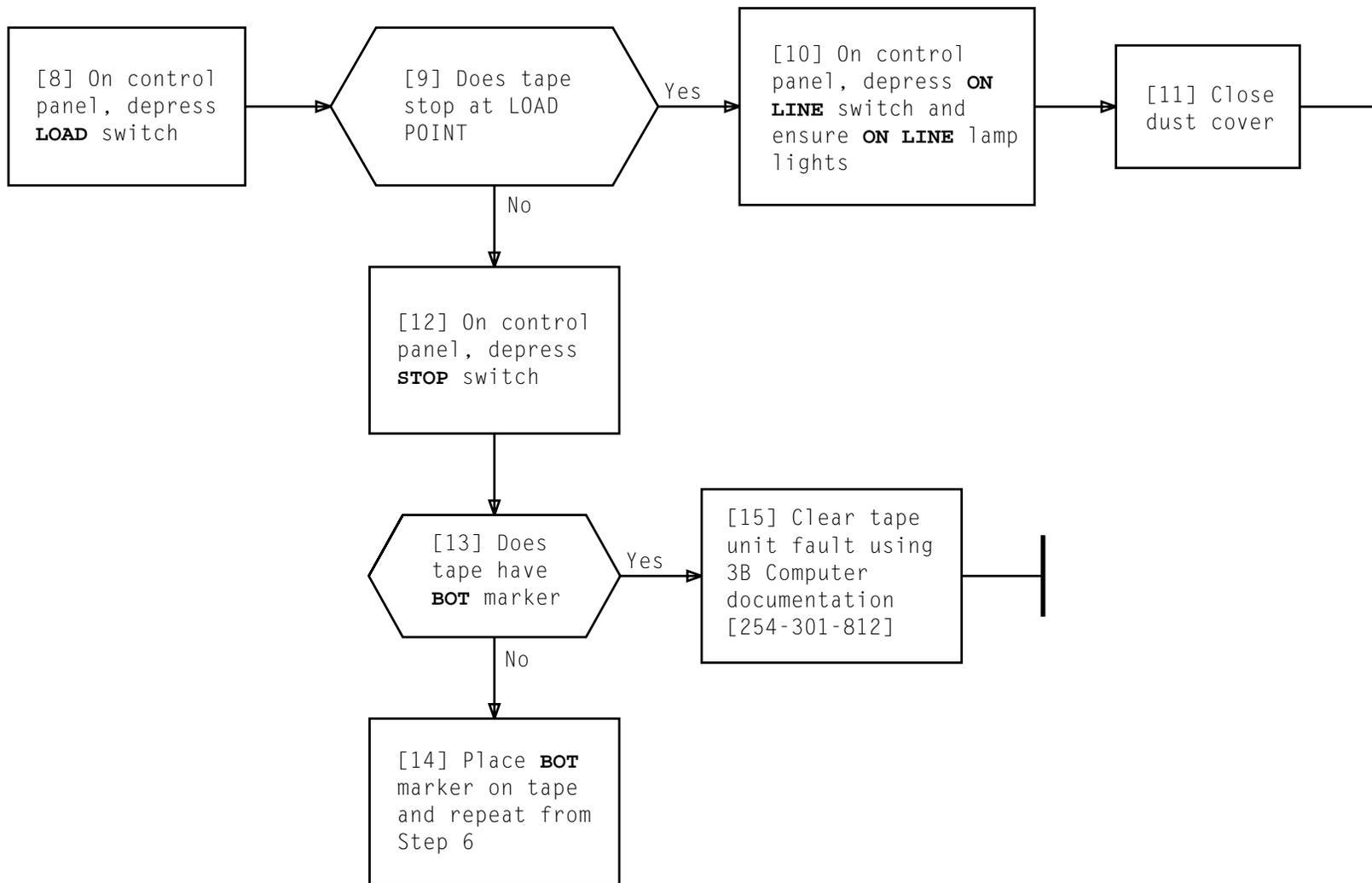


Figure 1 - 3B Computer Tape Unit



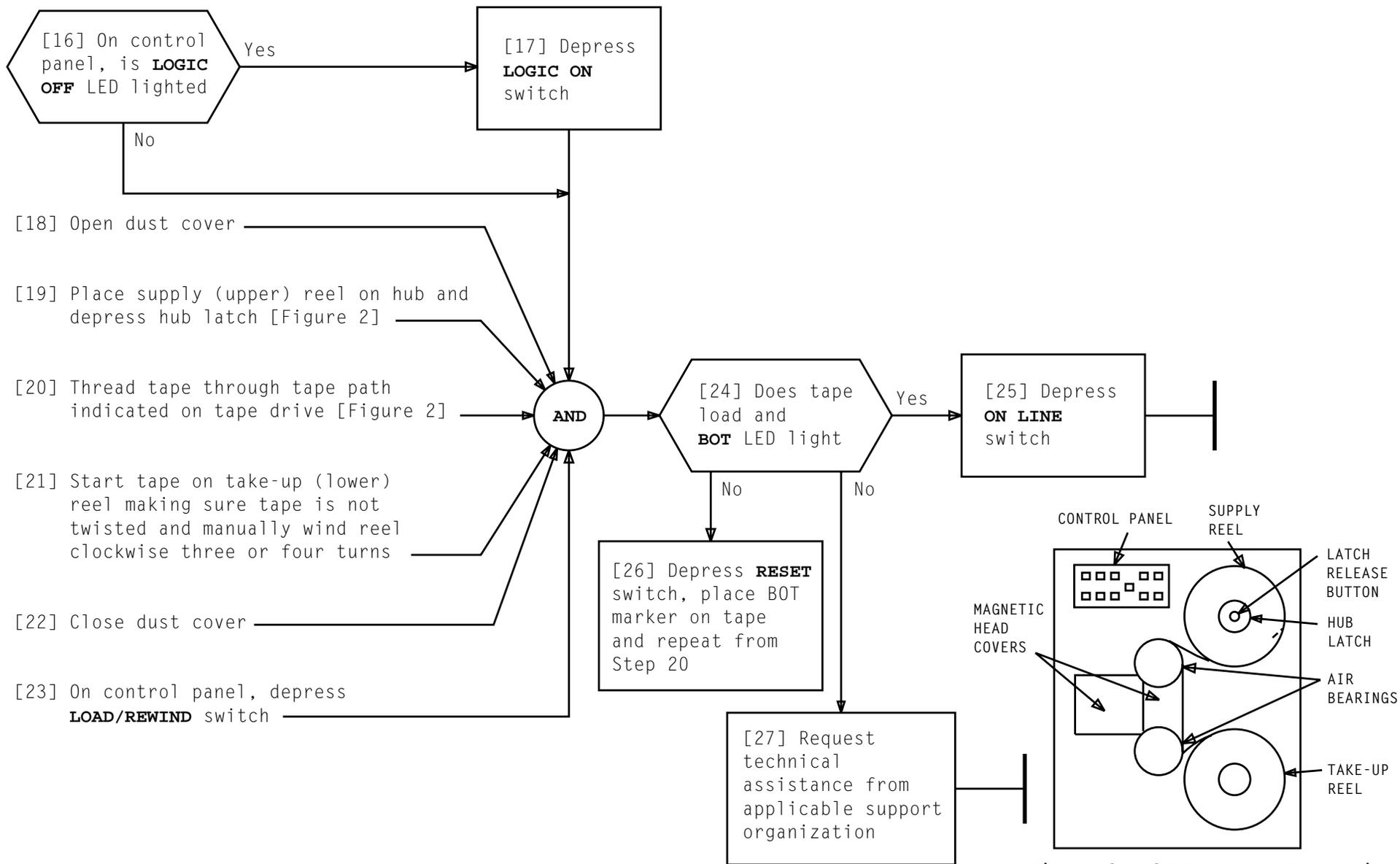
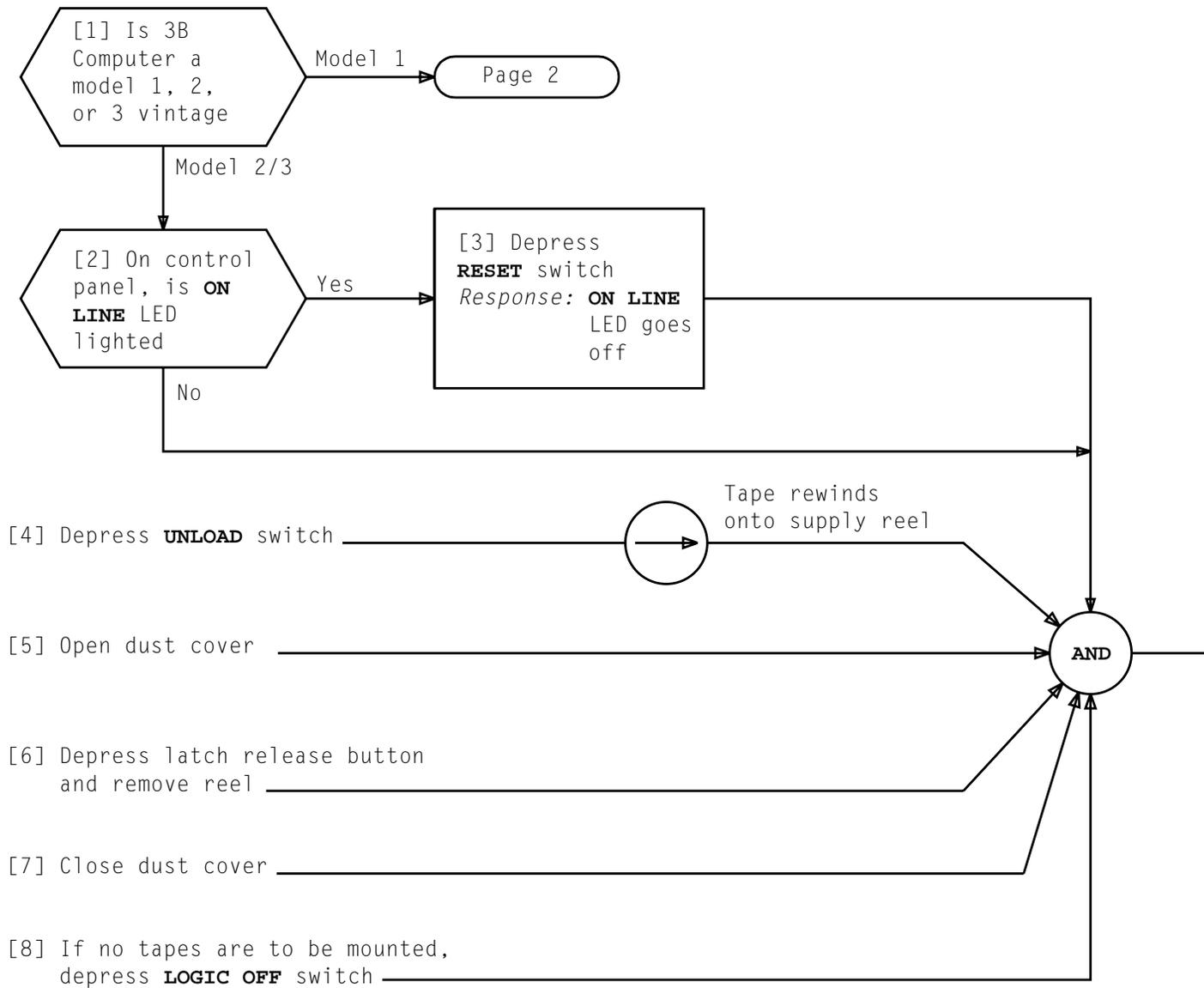


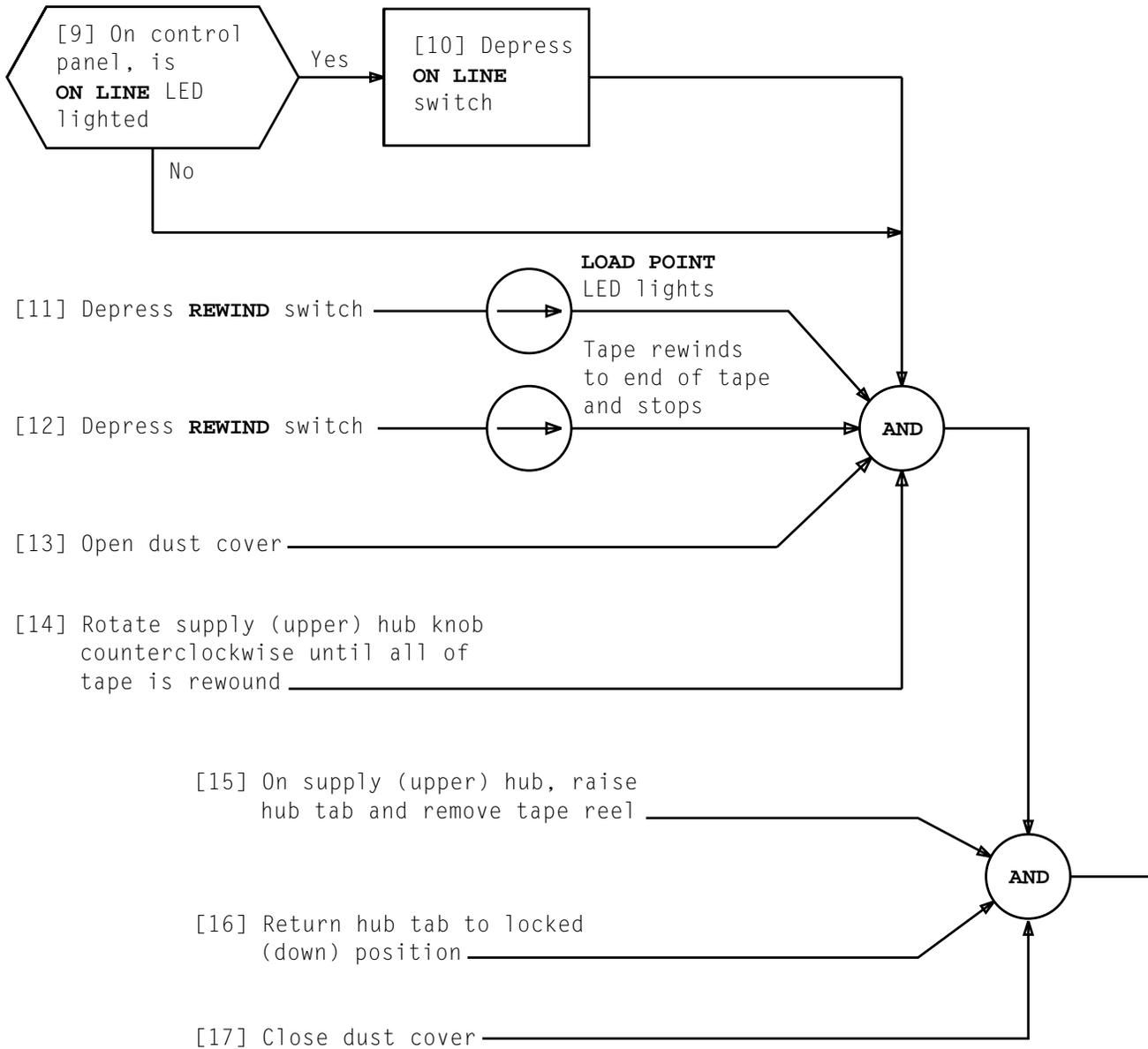
Figure 2 - 3B Computer Tape Unit

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DEMOUNT 1600 BPI TAPE ON 3B COMPUTER TAPE UNIT

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1. Define error using PMDs [TABLE A]

End of procedure

TABLE A	
PMD-001 apuf (duplex) – no error found	PMD-042 Unique error in both contrs, after hit-timing, then error in both contrs
PMD-002 puf (duplex) – no error found – aswf set in act only	PMD-043 Unique error in both contrs, after hit-timing, then error is gone
PMD-003 puf (duplex) – no error found – aswf set in stby only	PMD-044 Clock phase mismatch found in act only
PMD-004 puf (duplex) – no error found	PMD-045 Clock phase mismatch found in stby only
PMD-005 Duplex – no cc puf or apuf error source found	PMD-046 Clock phase mismatch found in both contrs
PMD-030 Unique error in act only, after hit-timing, then error in act only	PMD-047 Firmware detected errors found in both controllers, no PPE (no ram errors)
PMD-031 Unique error in act only, after hit-timing, then error in stby only	PMD-050 Firmware detected errors found in active contr only, no PPE (no ram errors)
PMD-032 Unique error in act only, after hit-timing, then error in both contrs	PMD-051 Firmware detected errors found in stby contr only, no PPE (no ram errors)
PMD-033 Unique error in act only, after hit-timing, then error is gone	PMD-052 Firmware detected errors found in both controllers with PPE (no ram errors)
PMD-034 Unique error in stby only, after hit-timing, then error in act only	PMD-053 Firmware detected errors found in active contr only with PPE (no ram errors)
PMD-035 Unique error in stby only, after hit-timing, then error in stby only	PMD-054 Firmware detected errors found in stby contr only with PPE (no ram errors)
PMD-036 Unique error in stby only, after hit-timing, then error in both contrs	PMD-055 Stack boundary or sanity timer error found in both or stby contr EXEC pack
PMD-037 Unique error in stby only, after hit-timing, then error is gone	PMD-056 Stack boundary or sanity timer error found in active contr EXEC pack only
PMD-040 Unique error in both contrs, after hit-timing, then error in act only	PMD-057 Stack boundary or sanity timer error found in both contr EXEC pack
PMD-041 Unique error in both contrs, after hit-timing, then error in stby only	PMD-060 Cross controller mismatch in act contr only, no EB intj source found

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TABLE A (Contd)

PMD-061	Cross controller mismatch in stby contr only, no EB intj source found	PMD-111	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby only, retry order, fails in both contrs
PMD-062	Cross controller mismatch in both contr only, no EB intj source found	PMD-112	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby only, retry order, passes in both contrs
PMD-070	The peripheral order is no good	PMD-113	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs, retry order, order fails in act only
PMD-071	Unique error in act contr, retry the order and act still has unique error	PMD-114	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs, retry order, order fails in stby only
PMD-072	Unique error in act contr, retry the order and act has no error	PMD-115	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs, retry order, order fails in both contrs
PMD-073	Unique error in stby contr, retry the order and stby still has unique error	PMD-116	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs, retry order, order passes in both contrs
PMD-074	Unique error in stby contr, retry the order and stby has no error	PMD-117	Firmware detected errors in active contr, no PPE (no ram errors)
PMD-075	puf – stack boundary or sanity timer error found in act contr EXEC pack	PMD-120	Unique errors in act contr during a "no retry allowed" order
PMD-076	puf – stack boundary or sanity timer error found in stby contr EXEC pack	PMD-121	Unique errors in stby contr during a "no retry allowed" order
PMD-103	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act only, retry order, fails in act only	PMD-122	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act contr during a "no retry allowed" order
PMD-104	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act only, retry order, fails in stby only	PMD-123	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby during a "no retry allowed" order
PMD-105	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act only, retry order, fails in both contrs	PMD-124	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs during a "no retry allowed" order
PMD-106	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act only, retry order, passes in both contrs	PMD-125	Firmware detected errors in stby contr, no PPE (no ram errors)
PMD-107	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby only, retry order, fails in act only	PMD-126	Firmware detected errors in act contr with PPE (no ram errors)
PMD-110	cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby only, retry order, fails in stby only	PMD-127	Firmware detected errors in stby contr with PPE (no ram errors)

TABLE A (Contd)

PMD-130 apuf (simplex) – no error found	PMD-201 CONSISTENCY CHECK – inaput set in act, reset in stby, ias zero in stby (duplex)
PMD-131 puf (simplex) – no error found	PMD-202 CONSISTENCY CHECK – inaput set in act, reset in stby, ias nonzero in stby (duplex)
PMD-132 simplex – no cc puf or apuf error source found	PMD-203 CONSISTENCY CHECK – inaput reset in act and stby (duplex)
PMD-150 Unique error found, after hit-timing, error still present	PMD-204 CONSISTENCY CHECK – inaput reset in act, set in stby, ias zero in stby (duplex)
PMD-151 Unique error found, after hit-timing, error is gone	PMD-205 CONSISTENCY CHECK – inaput reset in act, set in stby, ias nonzero in stby (duplex)
PMD-152 Mismatch found (cpmm, ccmm)	PMD-206 CONSISTENCY CHECK – inaput reset in act, frame simplex interject from o/s contr (simplex)
PMD-153 Firmware detected errors found, no PPE (no ram errors)	PMD-207 INTERJECT FILTER – consistency check passes, normal digit buffer overflow (entry_configuration)
PMD-154 Firmware detected errors found with PPE (no ram errors)	PMD-217 INTERJECT FILTER – consistency check passes, but no sources found, frame duplex
PMD-155 Stack boundary or sanity timer error found in contr EXEC pack	PMD-220 INTERJECT FILTER – consistency check passes, but no sources found, frame simplex
PMD-170 Peripheral order is no good	PMD-221 INTERJECT CONT – aput set in both contr, but no error source found in neither, frame duplex
PMD-171 Unique error found, retry the order, unique error is still present	PMD-240 INTERJECT FILTER – single ds120 error
PMD-172 Unique error found, retry the order, error is gone	PMD-241 INTERJECT FILTER – single LAN error
PMD-173 Stack boundary or sanity timer error found in contr EXEC pack	PMD-242 INTERJECT FILTER – single invalid state error (active-active or standby-standby)
PMD-174 Firmware detected errors found with PPE (no ram errors)	PMD-243 INTERJECT FILTER – illegal command or data received by scu
PMD-175 cpmm or ccmm found	PMD-244 INTERJECT FILTER – illegal command or data received by controller
PMD-176 Firmware detected errors found, no PPE (no ram errors)	PMD-245 INTERJECT FILTER – receive FIFO full
PMD-177 Unique error found during a "no retry allowed" order	
PMD-200 CONSISTENCY CHECK – inaput set in act and stby, ias zero in stby (duplex)	

TABLE A (Contd)

PMD-246	INTERJECT FILTER – scu hard error, bad scu	PMD-332	fatal firmware detected errors found in both controllers (no ram errors)
PMD-247	INTERJECT FILTER – multiple ds120 errors on the same TSI	PMD-333	fatal firmware detected errors found in active controller (no ram errors)
PMD-250	INTERJECT FILTER – multiple ds120 errors on different TSIs	PMD-334	fatal firmware detected errors found in stby controller (no ram errors)
PMD-251	INTERJECT FILTER – multiple LAN errors	PMD-340	ram errors in active controller
PMD-252	INTERJECT FILTER – multiple invalid link state, hardware status indicates software act contr is active	PMD-341	ram error in stby controller
PMD-253	INTERJECT FILTER – multiple invalid link state, hardware status indicates software act contr is not active	PMD-343	fatal firmware detected errors found in active controller (no ram errors)
PMD-260	ccmm found during apuf, IAS_ACT = 0, IAS_STB = 1	PMD-344	fatal firmware detected errors found in stby controller (no ram errors)
PMD-261	ccmm found during apuf, IAS_ACT = 1, IAS_STB = 0	PMD-350	ram errors
PMD-262	ccmm found during apuf, IAS_ACT = 1, IAS_STB = 1	PMD-353	fatal firmware detected errors found (no ram errors)
PMD-270	ccmm found during puf, IAS_ACT = 0, IAS_STB = 1	PMD-360	ram errors
PMD-271	ccmm found during puf, IAS_ACT = 1, IAS_STB = 0	PMD-363	fatal firmware detected errors found (no ram errors)
PMD-272	ccmm found during puf, IAS_ACT = 1, IAS_STB = 1	PMD-373	hardware access test failure
PMD-301	BASE FILTER – autonomous report	PMD-374	interrupt from a growth frame
PMD-311	BASE FILTER – illegitimate report	PMD-375	interrupt from an unequipped frame
PMD-330	ram errors found in stby only or both controllers	PMD-377	interrupt from a duplex failed frame
PMD-331	ram errors found in act contr (stby may have f/w detected error)		

Using completed diagnostics with
CATP results [Figure 1, Page 2]:

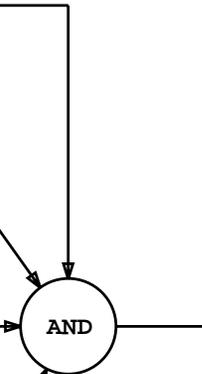
[1] Identify unit being
diagnosed

[2] Identify CATP octal data identifying
conditions causing diagnostics to
complete with CATP results

[3] Convert CATP octal data to binary
and identify failing bits (bits
set to one) [Figure 2, Page 2]

[4] Using failing bits and input/output
message manual or maintenance
reference handbook, identify
conditions causing diagnostics to
complete with CATP results

[5] Contact next higher technical
support group and determine
if CATP results are
explainable and acceptable



IDENTIFY CONDITIONS CAUSING DIAGNOSTICS TO COMPLETE WITH CATP RESULTS

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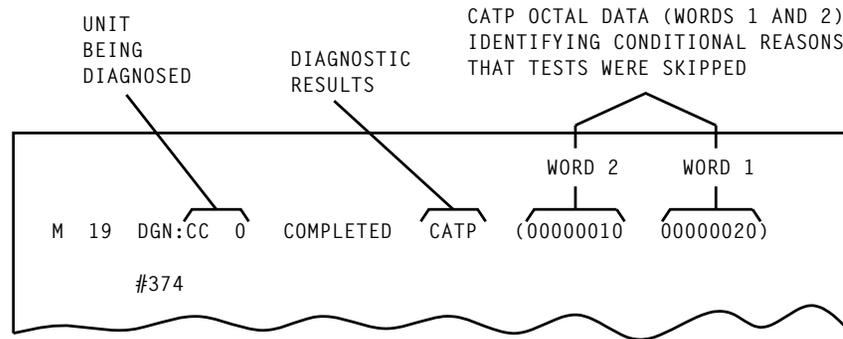


Figure 1 - Sample Printout of Completed Diagnostics With CATP Results

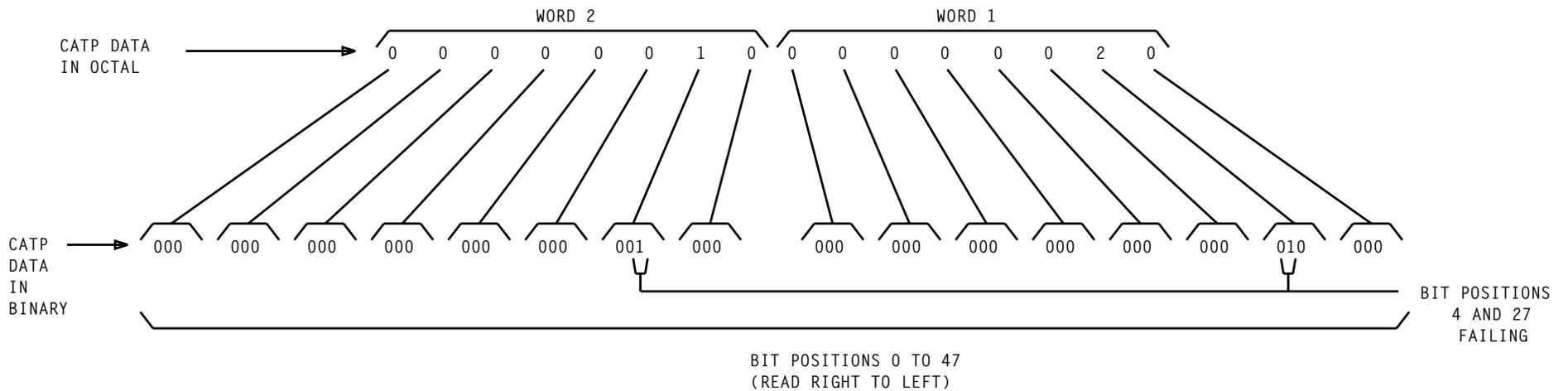


Figure 2 - Example of CATP Data Octal To Binary Conversion

IDENTIFY CONDITIONS CAUSING DIAGNOSTICS TO COMPLETE WITH CATP RESULTS

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DATA: ACTIVE CC BUS NODE DATA - PART 1

BNA_WD0	BNA_WD1	BNA_WD2	BNA_WD0	BNA_WD1	BNA_WD2
BNA_WD0	BNA_WD1	BNA_WD2	BNA_WD0	BNA_WD1	BNA_WD2
BNA_WD0	BNA_WD1	BNA_WD2	BNA_WD0	BNA_WD1	BNA_WD2

DATA: STANDBY CC BUS NODE DATA - PART 1

BNA_WD0	BNA_WD1	BNA_WD1	BNA_WD0	BNA_WD1	BNA_WD2
BNA_WD0	BNA_WD1	BNA_WD1	BNA_WD0	BNA_WD1	BNA_WD2
BNA_WD0	BNA_WD1	BNA_WD1	BNA_WD0	BNA_WD1	BNA_WD2

LAYOUTS FOR BUS NODE DATA

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BNA_WD0	0									v	0	ACCESS TYPE	CCCTL OR IBCTL BITS						P	C	R	UPPER PORT ADDR										

V - VALID ENTRY
ACCESS TYPE

- 0 - NULL ACCESS
- 1 - CALL STORE ACCESS
- 2 - PROGRAM STORE ACCESS
- 3 - PROM ACCESS
- 4 - MMIO
- 5 - BUFFER BUS ACCESS

CCCTL - CC CONTROL BITS

- 00000001 (bit 10) - WRITE CONTROL SIGNAL FROM THE DATA NODE
- 00000010 (bit 11) - MAINTENANCE CONTROL SIGNAL FROM THE DATA NODE
- 00000100 (bit 12) - CONTROL SIGNAL FROM THE DATA NODE
- 00001000 (bit 13) - GCP CONTROL SIGNAL FROM THE DATA NODE
- 00010000 (bit 14) - CONTROL SIGNAL FROM THE INDEX NODE
- 00100000 (bit 15) - WRITE REQUEST FROM THE DATA NODE
- 01000000 (bit 16) - IFB GRANT TO DATA NODE

IBCTL - IFB CONTROL BITS

- 00000001 (bit 10) - WRITE CONTROL SIGNAL FROM THE IFB
- 00000010 (bit 11) - MAINTENANCE CONTROL SIGNAL FROM THE IFB
- 00000100 (bit 12) - CONTROL SIGNAL FROM THE IFB
- 00001000 (bit 13) - WORD DMA REQUEST FROM THE IFB

P - PORT ACCESS

- 0 - DATA NODE
- 1 - INDEX NODE
- 2 - FETCH NODE
- 3 - INTERFACE BUS NODE

CP - CONTROL PARITY BIT

RD - READ BIT

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BNA_WD1	0									LOWER 24 BITS OF PORT ADDRESS																						

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BNA_WD2	0									FAULT RECOVERY RESULTS						RAW BIN ENTRY						BUS NODE RESULTS										

BUS NODE RESULTS

- 000001 - ALL SEEMS WELL
- 000010 - DATA PARITY FAILURE
- 000100 - ALL SEEMS WELL FAILURE
- 001000 - NODE ATTEMPTED ILLEGAL ACCESS
- 010000 - CONTROL PARITY B-SOURCE
- 100000 - CLIENT D-SOURCE

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BREAKDOWN OF BUS NODE DATA

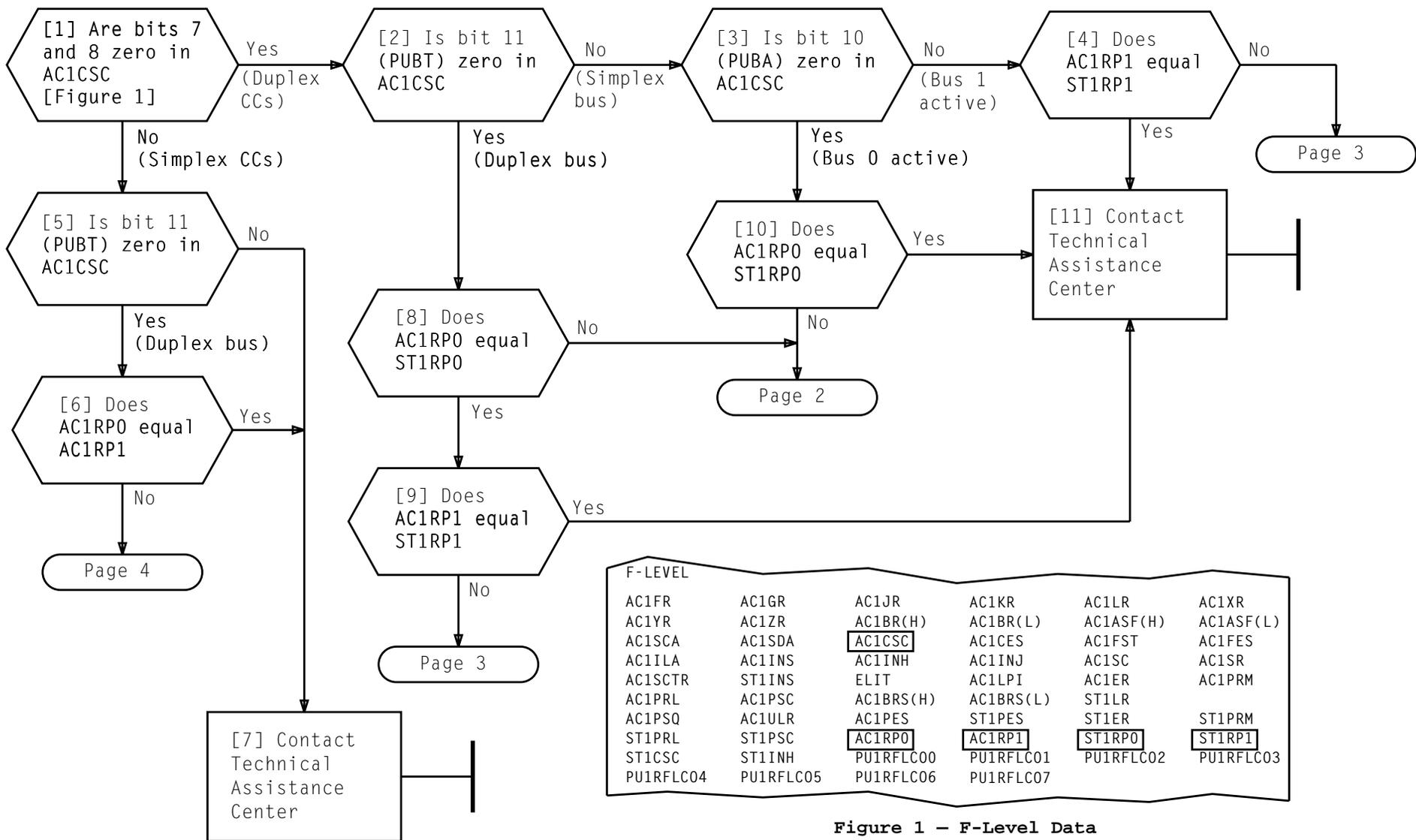
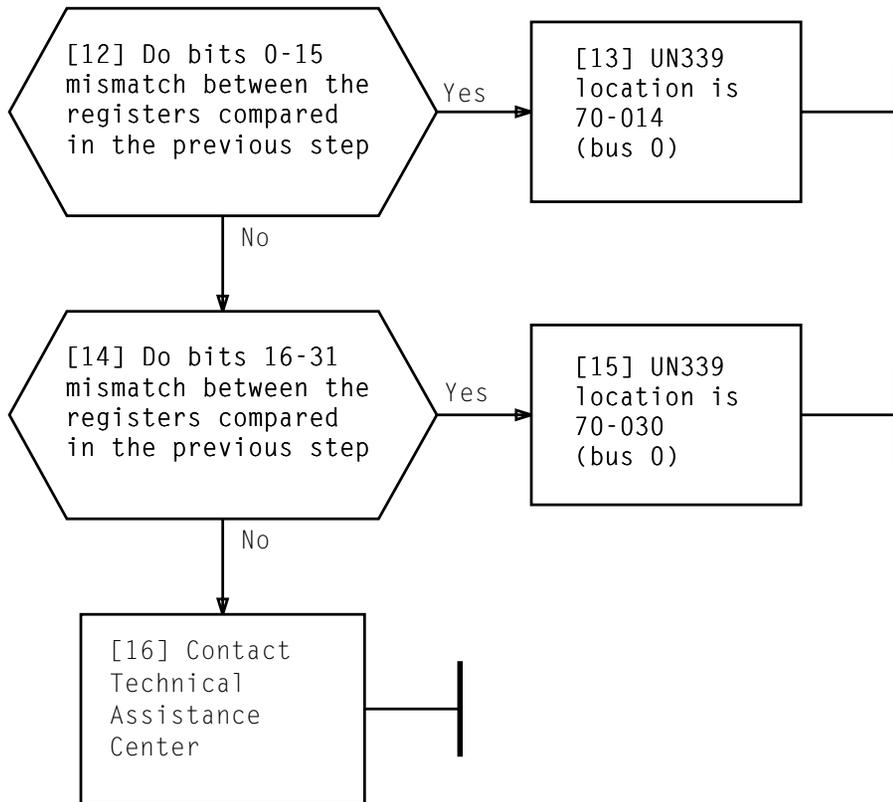
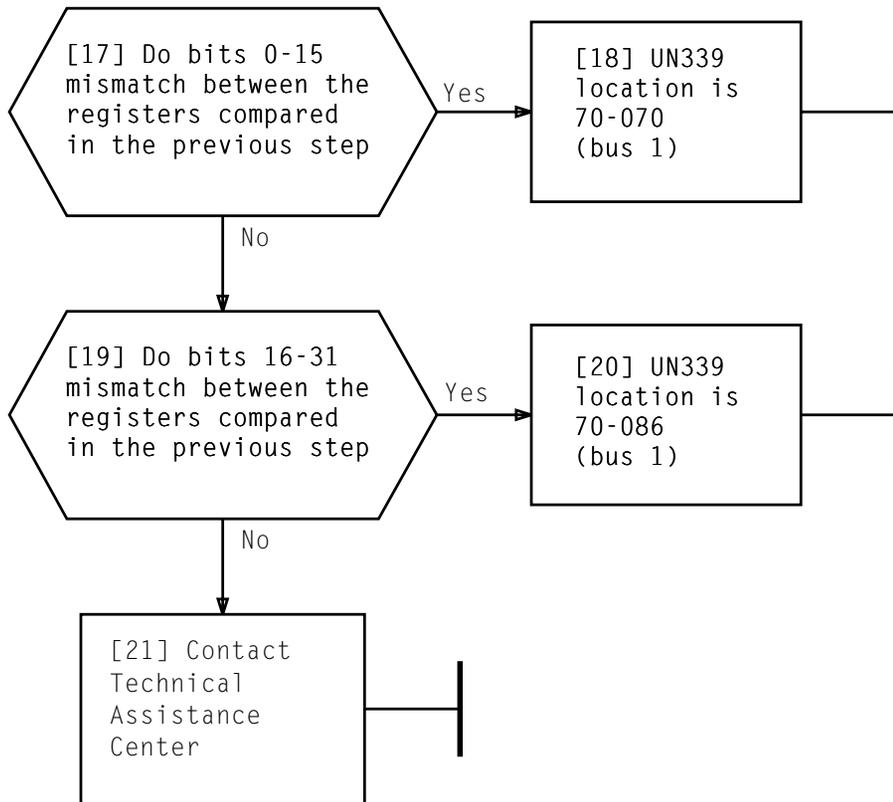


Figure 1 - F-Level Data



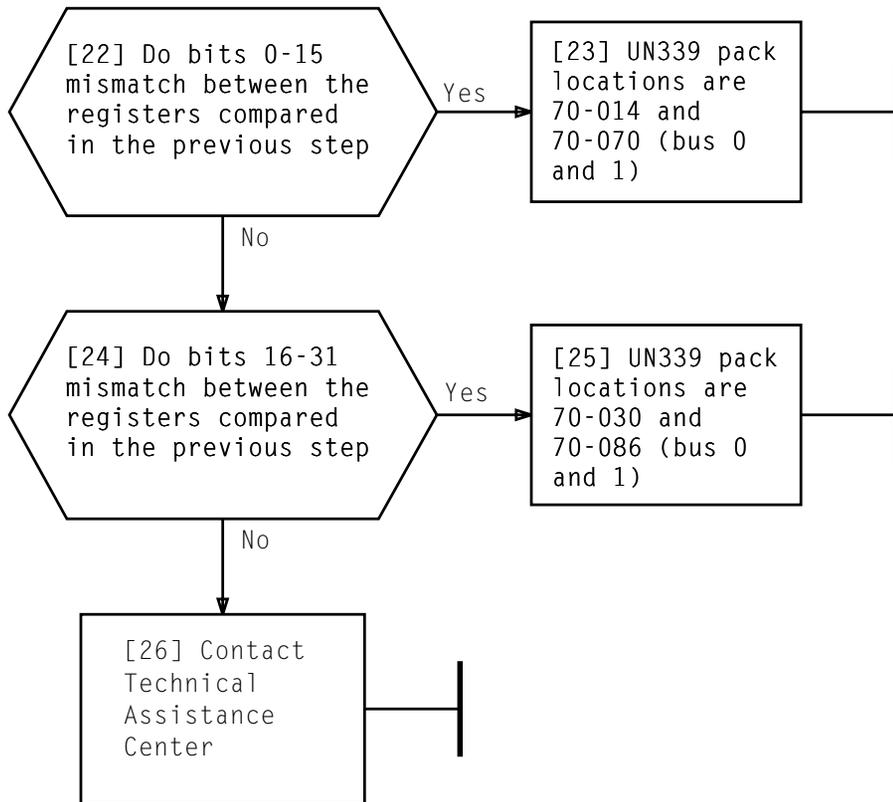
IDENTIFY SUSPECT UN339 PACK LOCATIONS

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IDENTIFY SUSPECT UN339 PACK LOCATIONS

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IDENTIFY SUSPECT UN339 PACK LOCATIONS

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1. Define error using PMDs [TABLE A]
 End of Procedure

TABLE A	
PMD - 001 Invalid PMD	PMD - 030 Transient error in act
PMD - 002 PUF fault, found no error reported in simplex/act	PMD - 031 Transient error in stby
PMD - 003 PUF fault, found no error reported by stby	PMD - 032 Transient error in both
PMD - 004 PUF fault, found no error reported by both controllers	PMD - 033 Hardware error in act
PMD - 005 No CC error source found	PMD - 034 Hardware error in stby
PMD - 006 Access test failure in act	PMD - 035 Hardware error in both
PMD - 007 Access test failure in stby	PMD - 036 ACT/STB mismatch in multiple PSCs
PMD - 010 Reserved (TMS)	PMD - 037 ACT/STB mismatch in multiple PSCs
PMD - 011 Reserved (TMS)	PMD - 040 ACT/STB mismatch in multiple PSCs
PMD - 012 Reserved (TMS)	PMD - 042 XRAM mismatch error in act
PMD - 013 Reserved (TMS)	PMD - 043 XRAM mismatch error in stby
PMD - 014 Reserved (TMS)	PMD - 044 XRAM mismatch in both
PMD - 015 Reserved (TMS)	PMD - 050 Reserved (TMS)
PMD - 016 Reserved (TMS)	PMD - 051 Reserved (TMS)
PMD - 017 Reserved (TMS)	PMD - 052 Reserved (TMS)
PMD - 020 Cross controller mismatch (CCMM) in act only or in both APUF	PMD - 053 Reserved (TMS)
PMD - 021 CCMM or SEQERR in stby only (APUF)	PMD - 054 Reserved (TMS)
PMD - 022 CCMM or SEQERR in act (PUF)	PMD - 055 Reserved (TMS)
PMD - 023 CCMM or SEQERR in stby (PUF)	PMD - 056 Reserved (TMS)
PMD - 024 CCMM or SEQERR error in both (PUF)	PMD - 057 Reserved (TMS)
PMD - 025 APUF fault, found no fault reported in simplex/by act only	PMD - 060 Transient error in act
PMD - 026 APUF fault, found no fault reported by stby	PMD - 061 Transient error in stby
PMD - 027 APUF fault, found no fault reported by both controllers	PMD - 062 Transient error in both
	PMD - 063 Hardware error in act
	PMD - 064 Hardware error in stby
	PMD - 065 Hardware error in both
	PMD - 066 Hardware error in both

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TABLE A (Contd)

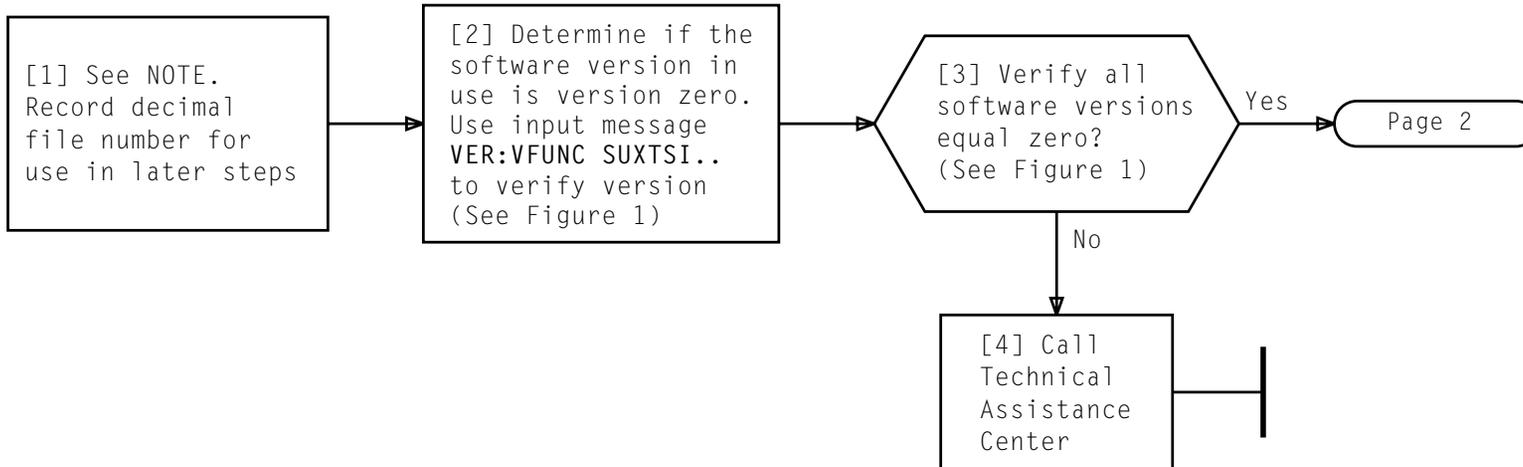
PMD - 067 Flash MEM error in both (APUF)	PMD - 115 Transient CB error on both (APUF)
PMD - 070 Flash MEM error in act (APUF)	PMD - 116 Hard CB error on both/act only (APUF) with SOFTERR
PMD - 071 Flash MEM error in stby (APUF)	PMD - 117 Hard CB error on stby only (APUF) with SOFTERR
PMD - 072 Flash MEM error in both (PUF)	PMD - 120 Hard/Transient CB error on act and PSC (PUF)
PMD - 073 Flash MEM error in act (PUF)	PMD - 121 Hard/Transient CB error on stby and PSC (PUF)
PMD - 074 Flash MEM error in stby (PUF)	PMD - 122 Hard/Transient CB error on both and PSC (PUF)
PMD - 075 Hardware error in act occurs during non-retryable PU order	PMD - 123 Hard CB error on PSC babbling (PUF)
PMD - 076 Hardware error in stby occurs during non-retryable PU order	PMD - 124 Hard/Transient CB error on act and PSC (APUF)
PMD - 077 Hardware error in both controllers during non-retryable PU order	PMD - 125 Hard/Transient CB error on stby and PSC (APUF)
PMD - 100 CB error on act (PUF)	PMD - 126 Hard/Transient CB error on act and PSC (APUF)
PMD - 101 CB error on stby (PUF)	PMD - 127 Hard CB error on PSC babbling (APUF)
PMD - 102 CB error on both (PUF)	PMD - 130 PCM error on act
PMD - 103 Transient CB error on act (PUF)	PMD - 131 Transient PCM error on act
PMD - 104 Transient CB error on stby (PUF)	PMD - 132 PCM error on stby
PMD - 105 Transient CB error on both (PUF)	PMD - 133 Transient PCM error on stby
PMD - 106 Hard CB error on both/act only (PUF) with SOFTERR	PMD - 134 PCM error on both
PMD - 107 Hard CB error on stby only (PUF) with SOFTERR	PMD - 135 Transient PCM error on both
PMD - 110 CB error on act (APUF)	PMD - 140 Hard/Transient PCM error in act and PSCs
PMD - 111 CB error on stby (APUF)	PMD - 141 Hard/Transient PCM error in stby and PSCs
PMD - 112 CB error on both (APUF)	PMD - 142 Hard/Transient PCM error in both and PSCs
PMD - 113 Transient CB error on act (APUF)	PMD - 143 Hard PCM error in PSC
PMD - 114 Transient CB error on stby (APUF)	PMD - 144 Transient PCM error in PSC
	PMD - 145 APUT (Interject) error in CSP
	PMD - 147 Special PSC SOFT-INIT error
	PMD - 150 BM MUX SEL error while in simplex

TABLE A (Contd)

PMD - 151 BM MUX SEL error while in duplex	PMD - 302 BLM loopback report
PMD - 152 Transient hardware or unknown software PSC error	PMD - 307 BLM illegitimate report
PMD - 153 Hard PSC error	PMD - 310 Unrecoverable error in act
PMD - 154 XTC_ERR from PSC	PMD - 311 Unrecoverable error in stby
PMD - 155 PSC SOFT_INIT	PMD - 312 Unrecoverable error in both
PMD - 156 PSC HARD_INIT	PMD - 313 Unrecoverable error in act
PMD - 157 PSC HARD_RESET	PMD - 314 Unrecoverable error in stby
PMD - 200-247 Transmission error handled by TNFRMISC pident	PMD - 315 Unrecoverable error in both
PMD - 260 XMIT error on act without secondary	PMD - 316 Invalid condition
PMD - 261 XMIT error on act with secondary	PMD - 320 SANTIM/STKBND error in act (APUF)
PMD - 262 Transient XMIT error on act without secondary	PMD - 321 SANTIM/STKBND error in stby (APUF)
PMD - 263 Transient XMIT error on act with secondary	PMD - 322 SANTIM/STKBND error in both (APUF)
PMD - 264 XMIT error on stby without secondary	PMD - 323 SANTIM/STKBND error in act (APUF)
PMD - 265 XMIT error on stby with secondary	PMD - 324 SANTIM/STKBND error in stby (APUF)
PMD - 266 Transient XMIT error on stby without secondary	PMD - 325 SANTIM/STKBND error in both (APUF)
PMD - 267 Transient XMIT error on stby with secondary	PMD - 330 HARD_INIT error in act
PMD - 270 XMIT error on both without secondary	PMD - 331 HARD_INIT error in stby
PMD - 271 Transient XMIT error on both without secondary	PMD - 332 HARD_INIT error in both
PMD - 272 XMIT error on both with secondary	PMD - 333 HARD_INIT error in act
PMD - 273 Transient error on both with secondary	PMD - 334 HARD_INIT error in stby
PMD - 274 PSC PCM mismatch	PMD - 335 HARD_INIT error in both
PMD - 300 Receive a BLM	PMD - 336 ACT_STBY signal mismatch in only on PSC
PMD - 301 BLM autonomous	

TABLE A (Contd)

PMD - 340 SOFT_INIT error in active (APUF)
PMD - 341 SOFT_INIT error in standby (APUF)
PMD - 342 SOFT_INIT error in both (APUF)
PMD - 343 SOFT_INIT error in active (PUF)
PMD - 344 SOFT_INIT error in standby (PUF)
PMD - 345 SOFT_INIT error in both (PUF)
PMD - 363 Clock error in both
PMD - 364 Clock error in act
PMD - 365 Clock error in stby
PMD - 366 Reserved
PMD - 367 Reserved
PMD - 370 Reserved
PMD - 371 Reserved
PMD - 372 Invalid PU order in simplex
PMD - 373 Invalid PU order in duplex
PMD - 374 Interrupt from growth frame
PMD - 375 Interrupt from unequipped frame
PMD - 376 AUDSUM error
PMD - 377 Interrupt from duplex failed frame



Input Message: a = XTSI Member Number
 VER:VFUNC SUXTSI:FD1 XTSIMEMN,DT1 a!

Output Message:
 VER:MISC;OPT(SUXTSI): XTSI MEMN a,

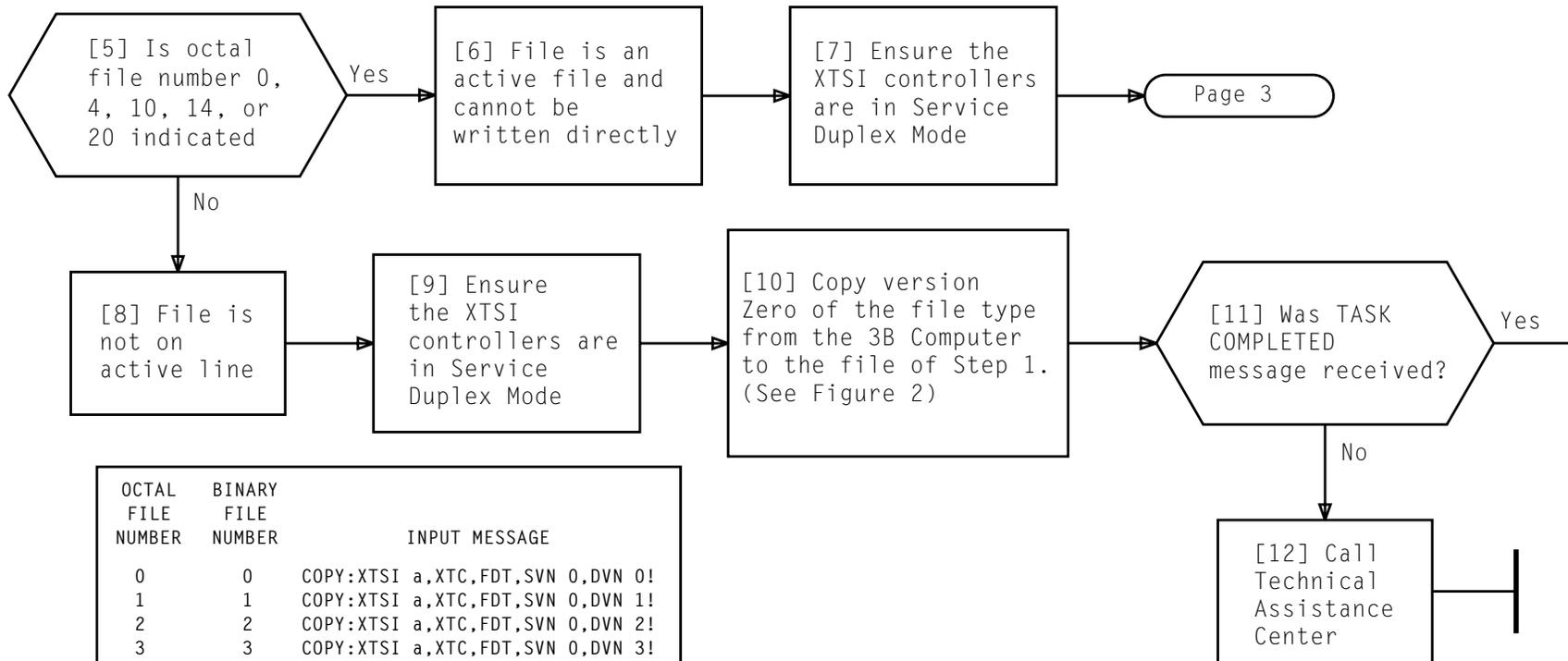
XTCN	0,1	
XTCHV	0,0	
XTCSV	0,0	← Controller Software Version

D3UN	0	1	2	3	4	5	6	7	
D3UEQ	0,	0,	0,	0,	0,	0,	0,	0,	
D3UHV	0,	0,	0,	0,	0,	0,	0,	0,	
D3USV	0,	0,	0,	0,	0,	0,	0,	0,	← D3U Software Version

Figure 1 - Verify Software Version

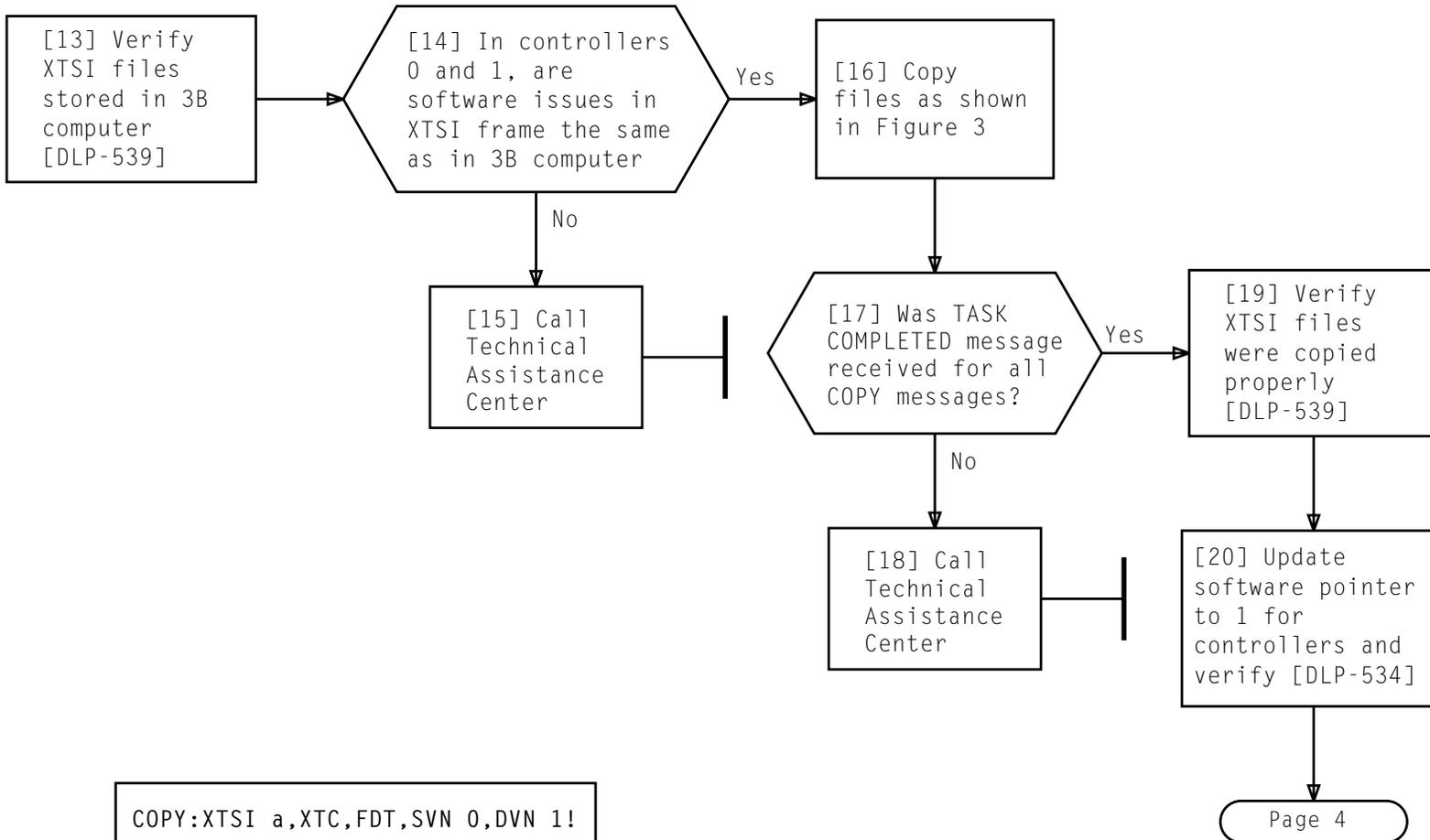
NOTE
 This DLP will overwrite the files that have been suspect with the most recent versions of these files from the 3B Computer. If the suspect files are not active files (not pointed to by the software version pointers) they will be overwritten directly from the 3B Computer. If the suspect files are active files, they cannot be written to directly. In this case, we will overwrite the next higher file numbers, (which should be version 1 files) move the version pointers to point to them, and then overwrite the version 0 (once active) files. Finally, we will move the software version pointers back to the version 0 files

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OCTAL FILE NUMBER	BINARY FILE NUMBER	INPUT MESSAGE
0	0	COPY:XTSI a,XTC,FDT,SVN 0,DVN 0!
1	1	COPY:XTSI a,XTC,FDT,SVN 0,DVN 1!
2	2	COPY:XTSI a,XTC,FDT,SVN 0,DVN 2!
3	3	COPY:XTSI a,XTC,FDT,SVN 0,DVN 3!
4	4	COPY:XTSI a,XTC,OPR,SVN 0,DVN 0!
5	5	COPY:XTSI a,XTC,OPR,SVN 0,DVN 1!
6	6	COPY:XTSI a,XTC,OPR,SVN 0,DVN 2!
7	7	COPY:XTSI a,XTC,OPR,SVN 0,DVN 3!
10	8	COPY:XTSI a,XTC,DGN,SVN 0,DVN 0!
11	9	COPY:XTSI a,XTC,DGN,SVN 0,DVN 1!
12	10	COPY:XTSI a,XTC,DGN,SVN 0,DVN 2!
13	11	COPY:XTSI a,XTC,DGN,SVN 0,DVN 3!
14	12	COPY:XTSI a,D3U,OPR,SVN 0,DVN 0!
15	13	COPY:XTSI a,D3U,OPR,SVN 0,DVN 1!
16	14	COPY:XTSI a,D3U,OPR,SVN 0,DVN 2!
17	15	COPY:XTSI a,D3U,OPR,SVN 0,DVN 3!
20	16	COPY:XTSI a,D3U,DGN,SVN 0,DVN 0!
21	17	COPY:XTSI a,D3U,DGN,SVN 0,DVN 1!
22	18	COPY:XTSI a,D3U,DGN,SVN 0,DVN 2!
23	19	COPY:XTSI a,D3U,DGN,SVN 0,DVN 3!

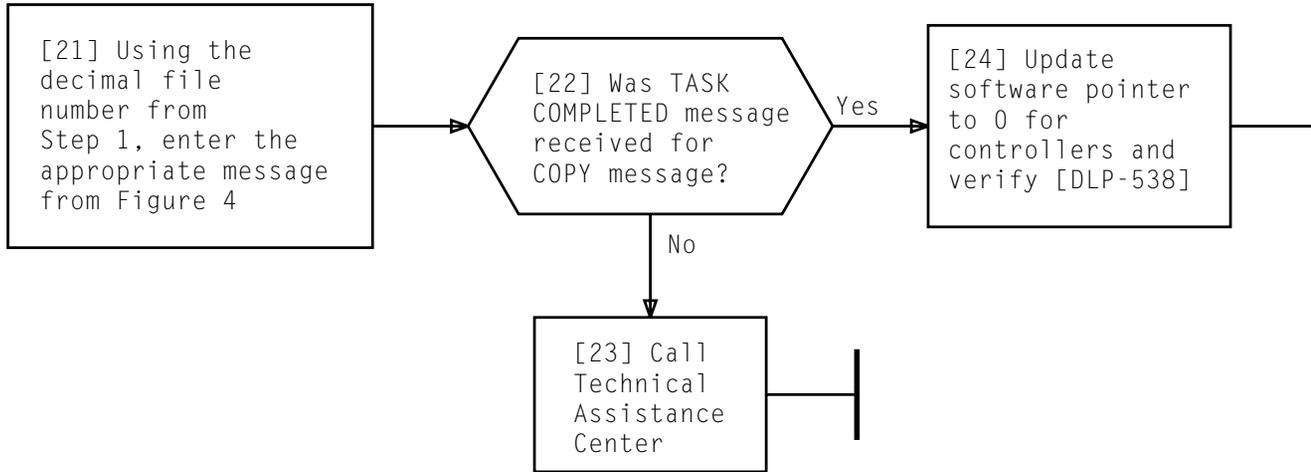
Figure 2 - Overwrite Messages for Non-active files



```

COPY:XTSI a,XTC,FDT,SVN 0,DVN 1!
COPY:XTSI a,XTC,OPR,SVN 0,DVN 1!
COPY:XTSI a,XTC,DGN,SVN 0,DVN 1!
COPY:XTSI a,D3U,OPR,SVN 0,DVN 1!
COPY:XTSI a,D3U,DGN,SVN 0,DVN 1!
  
```

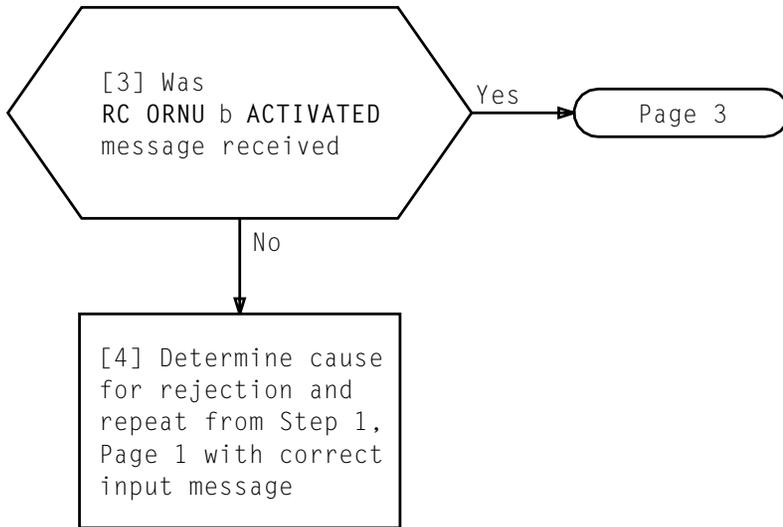
Figure 3 – Copy Files



FILE	INPUT MESSAGE
0	COPY:XTSI a,XTC,FDT,SVN 0,DVN 0! or
4	COPY:XTSI a,XTC,OPR,SVN 0,DVN 0! or
8	COPY:XTSI a,XTC,DGN,SVN 0,DVN 0! or
12	COPY:XTSI a,D3U,OPR,SVN 0,DVN 0! or
16	COPY:XTSI a,D3U,DGN,SVN 0,DVN 0!

Figure 4 – Copy Files

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RECENT CHANGE AND VERIFY SOFTWARE VERSION TO 1 FOR CONTROLLERS, D3Us, AND SPUs, IF EQUIPPED

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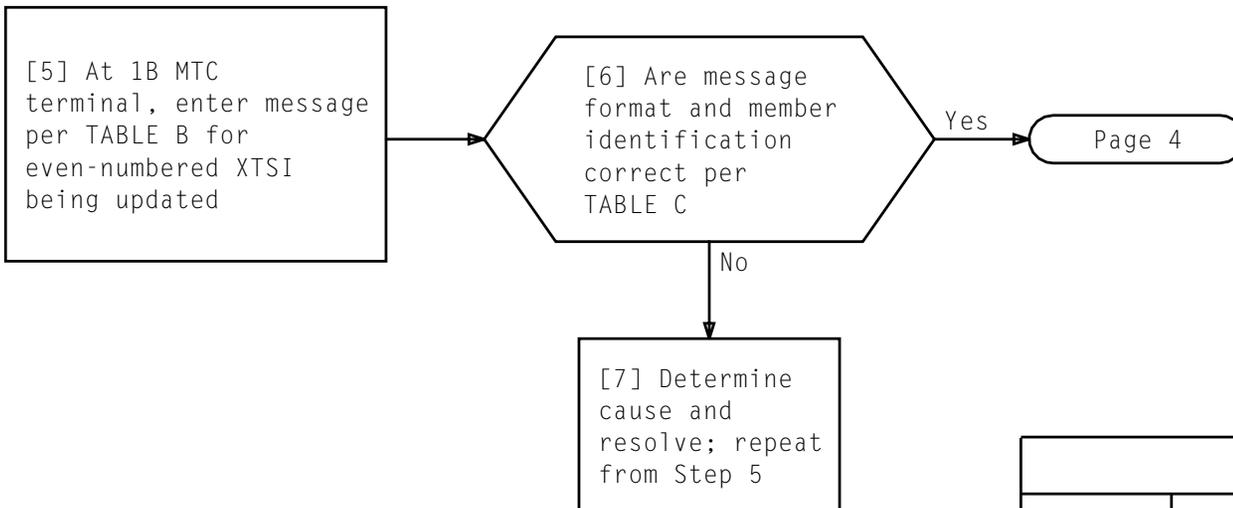
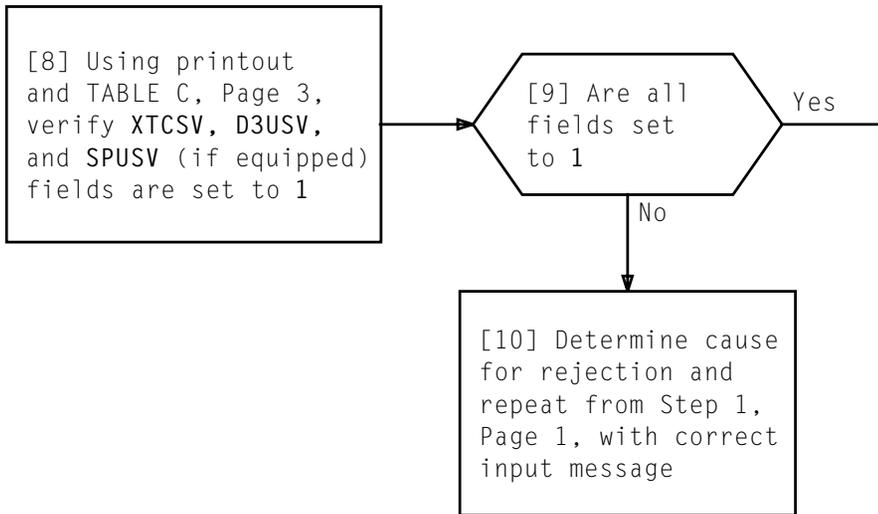


TABLE B	
MESSAGE NUMBER	INPUT MESSAGE
1	VER:VFUNC SUXTSI:FD1 XTSIMEMN,DT1 a!
a = XTSI member number	

TABLE C	
MESSAGE NUMBER	OUTPUT MESSAGE
1	VER:MISC;OPT(SUXTSI): XTSI MEMN a, XTCN 0 1 XTCHV -, XTCSV 1,1, D3UN 0 1 2 3 4 5 6 7 D3UEQ -, -, -, -, -, -, -, - D3UHV -, -, -, -, -, -, -, - D3USV 1,1,1,1,1,1, 1,1, SPUN 0 1 2 3 4 5 6 7 8 9 10 11 SPUEQ -, -, -, -, -, -, -, -, -, - SPUHV -, -, -, -, -, -, -, -, -, - SPUSV 1,1,1,1,1,1,1,1,1,1, 1, 1,
a = XTSI member number	

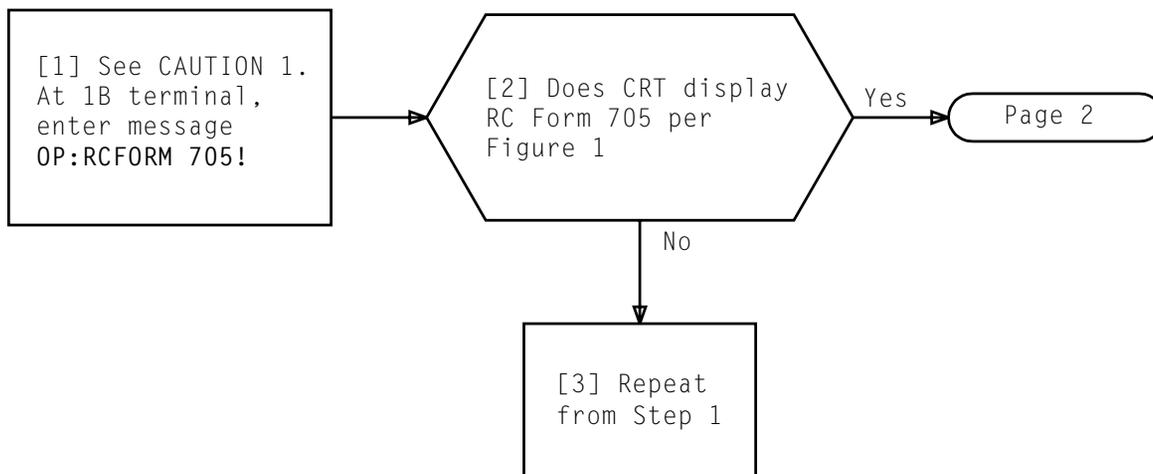
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RECENT CHANGE AND VERIFY SOFTWARE VERSION TO 1 FOR CONTROLLERS, D3Us, AND SPUs, IF EQUIPPED

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```

RC:UTYPE;CHG;OPT(SUXTSI),_ _ _ : TSI MEMN _ ,
ORNU _ _ _ _ ,
D3UN 0 1 2 3 4 5 6 7
D3USV _ , _ , _ , _ , _ , _ , _ , _ ,
REMARKS _ _ _ _ _ _ _ _ _ _ _ _ _ _ !
  
```

Figure 1 - Blank RC Form 705

<i>CAUTION 1</i> <i>Calling up RC form will cause all CRT data to be cleared</i>	
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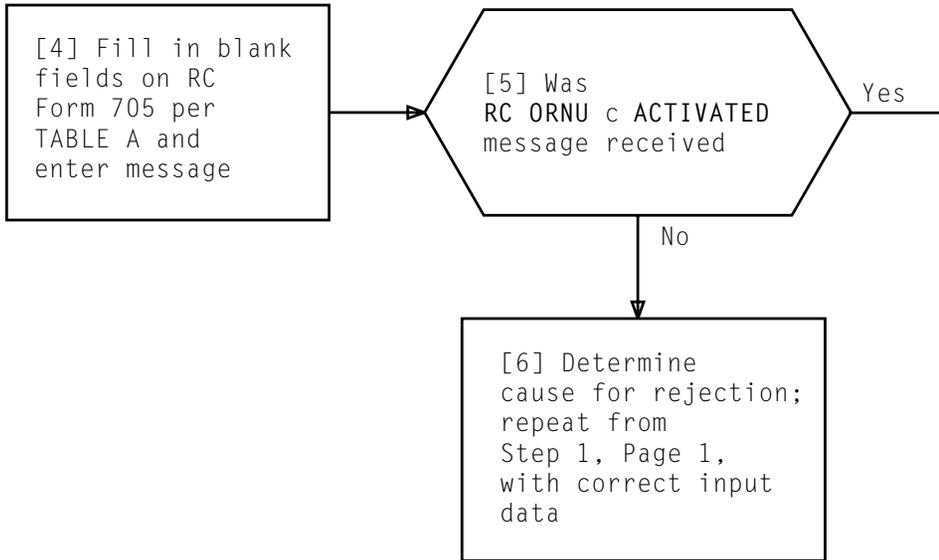
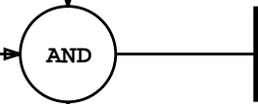


TABLE A	
MESSAGE NUMBER	INPUT MESSAGE
1	RC:UTYPE;CHG;OPT(SUXTSI),a: TSI MEMN b, ORNU c, D3UN 0 1 2 3 4 5 6 7 D3USV d,d,d,d,d,d,d,d, REMARKS _____!
a = FTA b = Even XTSI member number c = RC order number d = 1	

[1] See NOTE 1. At 3B MCRT, enter message
EXC:ENVIR:UPROC, FN "/tools/prxtsihdrs"

[2] Using printout and Figure 1, Page 2,
request next higher technical support
group to verify that latest XTSI
operating and diagnostic files are
3B computer memory

[3] Save printout for later use to verify
that XTSI subunits are running on
latest software



NOTE 1

This command will
take from 5 to 15
minutes to complete,
depending on
system call load

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```

EXC ENVIR UPROC /tools/prxsihdrs STARTED
File(s)      Hash Sums  Size      Header Date      Issue
xtsi/fdt/xfdtver0  0000 xxxx  0000 nnnn  CAnn/nn/nn nn:nn:nnC<nn>d.efg
xtsi/fdt/xfdtver1  0000 xxxx  0000 nnnn  CAnn/nn/nn nn:nn:nnC<nn>d.efg
xtsi/xtc/xoprver0  0000 xxxx  0000 nnnn  OAnn/nn/nn nn:nn:nnC<nn>d.efg
xtsi/xtc/xoprver1  0000 xxxx  0000 nnnn  OAnn/nn/nn nn:nn:nnC<nn>d.efg
xtsi/xtc/xdgnver0  0000 xxxx  0000 nnnn  DAnn/nn/nn nn:nn:nnC<nn>d.efg
xtsi/xtc/xdgnver1  0000 xxxx  0000 nnnn  DAnn/nn/nn nn:nn:nnC<nn>d.efg
xtsi/d3u/doprver0  0000 xxxx  0000 nnnn  OAnn/nn/nn nn:nn:nnU<nn>d.efg
xtsi/d3u/doprver1  0000 xxxx  0000 nnnn  OAnn/nn/nn nn:nn:nnU<nn>d.efg
xtsi/d3u/ddgnver0  0000 xxxx  0000 nnnn  DAnn/nn/nn nn:nn:nnU<nn>d.efg
xtsi/d3u/ddgnver1  0000 xxxx  0000 nnnn  DAnn/nn/nn nn:nn:nnU<nn>d.efg
xtsi/spu/soprver0  0000 xxxx  0000 nnnn  OAnn/nn/nn nn:nn:nns<nn>d.efg
xtsi/spu/soprver1  0000 xxxx  0000 nnnn  OAnn/nn/nn nn:nn:nns<nn>d.efg
xtsi/spu/sdgnver0  0000 xxxx  0000 nnnn  DAnn/nn/nn nn:nn:nns<nn>d.efg
xtsi/spu/sdgnver1  0000 xxxx  0000 nnnn  DAnn/nn/nn nn:nn:nns<nn>d.efg

```

EXC ENVIR UPROC /tools/prxsihdrs COMPLETED SEGMENT 2

xxxx = Checksum/Hashsum value for file in hex

In Header Date Column:

C means FDT file

D means DGN file

O means OPR file

In Issue Column:

C means XTC subunit

U means D3U subunit

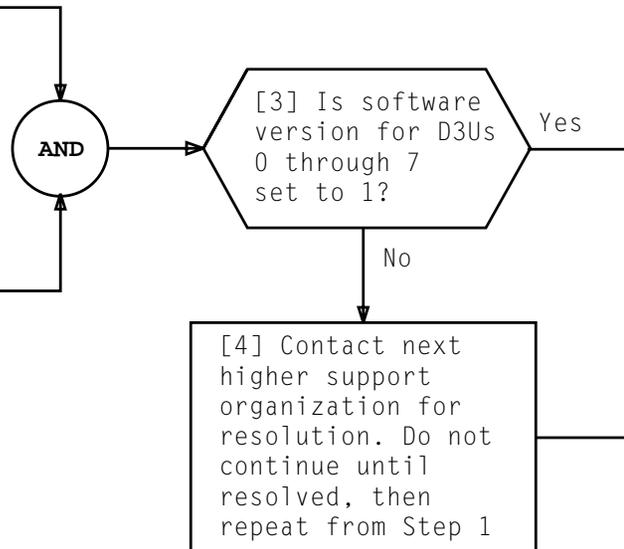
S means SPU

d.efg is file issue number

Figure 1 – EXC:ENVIR:UPROC Sample Printout

[1] At 1B MTC terminal, enter message
 VER:VFUNC SUXTSI:FD1 TSIMEMN,DT1 a!
 a = Even XTSI member number

[2] Using printout and Figure 1, determine
 if software version for D3Us
 0 through 7 are set to 1



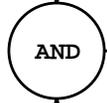
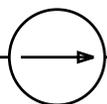
<u>Input Message:</u>		a = XTSI Member Number	
VER:VFUNC SUXTSI:FD1 XTSIMEMN,DT1 a!			
<u>Output Message:</u>			
VER:MISC;OPT(SUXTSI):		XTSI MEMN a,	
XTCN	0,1		
XTCHV	0,0		
XTCSV	0,0	← Controller Software Version	
D3UN	0 1 2 3 4 5 6 7		
D3UEQ	0, 0, 0, 0, 0, 0, 0, 0,		
D3UHV	0, 0, 0, 0, 0, 0, 0, 0,		
D3USV	1, 1, 1, 1, 1, 1, 1, 1,	← D3U Software Version	

Figure 1 - Verify Software Version

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[1] See CAUTION 1. At 1B terminal, enter message
OP:RCFORM 705!

CRT displays RC Form 705



Page 2

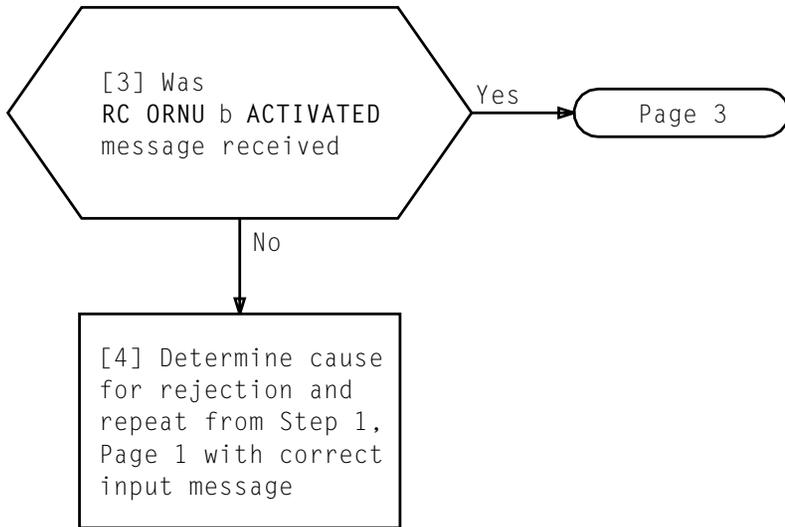
[2] Fill in blanks on RC Form 705 per TABLE A and enter message _____

TABLE A	
MESSAGE NUMBER	OUTPUT MESSAGE
1	RC:UTYPE;CHG;OPT(SUXTSI),a: XTSI MEMN b, ORNU c, XTCN 0 1 XTCHV -, -, XTCSV d,d, D3UN 0 1 2 3 4 5 6 7 D3UEQ -, -, -, -, -, -, -, -, D3UHV -, -, -, -, -, -, -, -, D3USV d,d,d,d,d,d, d,d, REMARKS -----!
a = FTA b = XTSI member number c = RC order number d = 1 for fields in XTCSV, and D3USV	

CAUTION 1
Calling up RC form will cause all CRT data to be cleared

RECENT CHANGE AND VERIFY SOFTWARE VERSION TO 0 FOR CONTROLLERS, AND D3Us, IF EQUIPPED

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RECENT CHANGE AND VERIFY SOFTWARE VERSION TO 0 FOR CONTROLLERS, AND D3Us, IF EQUIPPED

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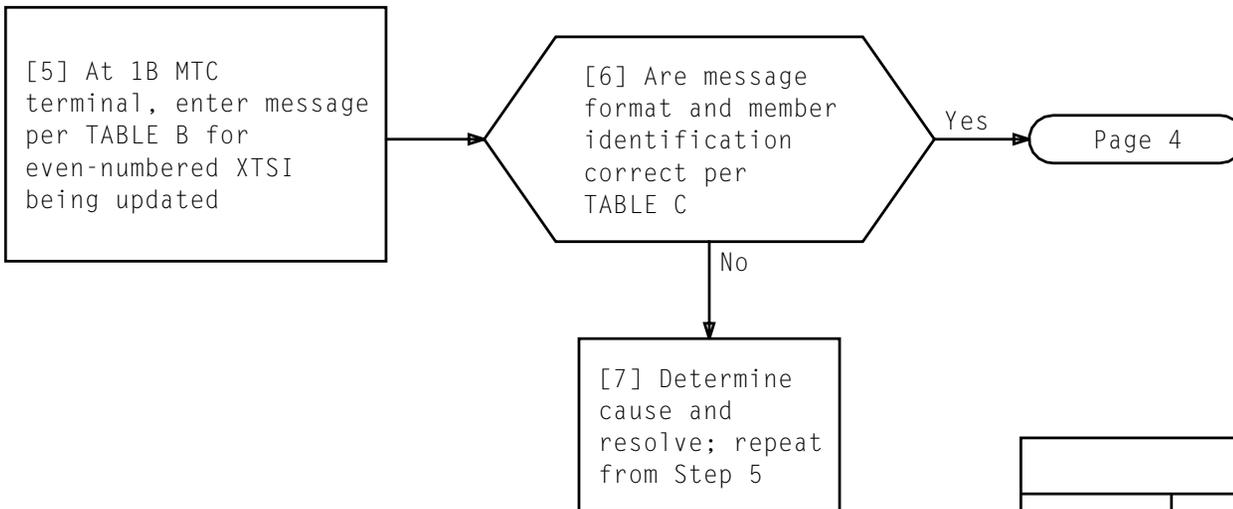
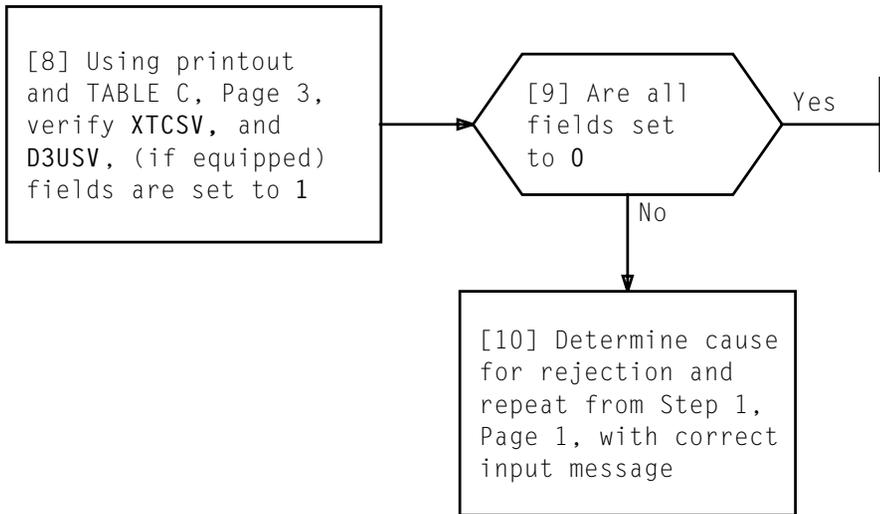


TABLE B	
MESSAGE NUMBER	INPUT MESSAGE
1	VER:VFUNC SUXTSI:FD1 XTSIMEMN,DT1 a!
a = XTISI member number	

TABLE C	
MESSAGE NUMBER	OUTPUT MESSAGE
1	VER:MISC;OPT(SUXTSI): XTISI MEMN a, XTCN 0 1 XTCHV -, -, XTCSV 1,1, D3UN 0 1 2 3 4 5 6 7 D3UEQ -, -, -, -, -, -, -, -, D3UHV -, -, -, -, -, -, -, -, D3USV 1,1,1,1,1,1, 1,1,
a = XTISI member number	

RECENT CHANGE AND VERIFY SOFTWARE VERSION TO 0 FOR CONTROLLERS, AND D3Us, IF EQUIPPED



RECENT CHANGE AND VERIFY SOFTWARE VERSION TO 0 FOR CONTROLLERS, AND D3Us, IF EQUIPPED

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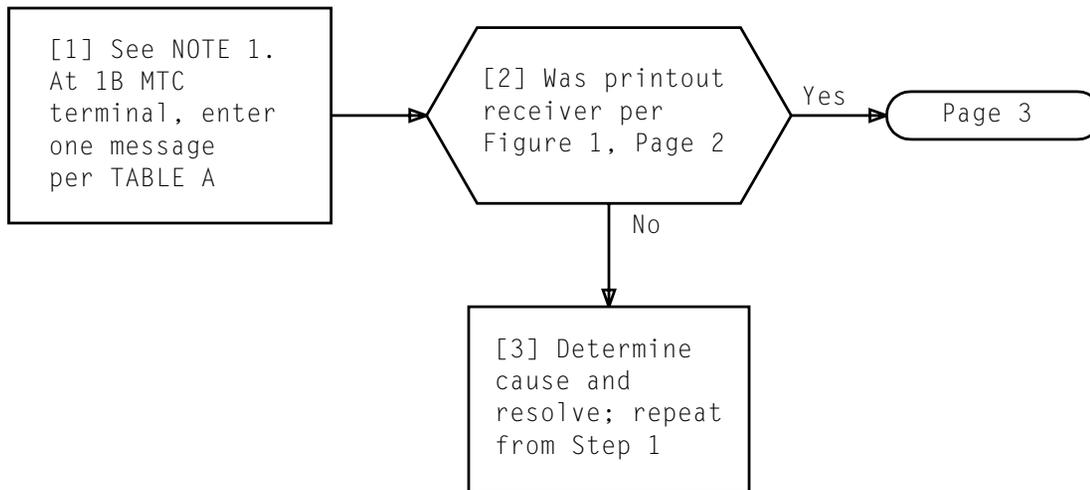


TABLE A		
MESSAGE NUMBER	INPUT MESSAGE	ASSOCIATED FILE DRIVER
1	DUMP:TSIFILE;XTSI a,FILE 1, HADR 0,L 20!	/fdt/fdtver
2	DUMP:TSIFILE;XTSI a,FILE 5, HADR 0,L 20!	/xtc/oprver
3	DUMP:TSIFILE;XTSI a,FILE 9, HADR 0,L 20!	/xtc/dgnver
4	DUMP:TSIFILE;XTSI a,FILE 13, HADR 0,L 20!	/d3u/oprver
5	DUMP:TSIFILE;XTSI a,FILE 17, HADR 0,L 20!	/d3u/dgnver
a = Even XTSI member number		

NOTE 1 Input messages must ben entered one at a time in sequence from 1 through 5	
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VERIFY NEW SYSTEM FILES WERE COPIED TO XTSI

```

DUMP;TSIFILE XTSI A CONTR 0 FILE B HADR 0 L 20;
      COMPLETED
000000  xxxx 0000 ---- 0000 ---- yyyy ---- ----
000008  ---- ---- ---- ---- --zz ---- ---- ----
000010  3e3f 3d-- 0000 3g00

```

```

a = XTSI member number
b = File number (0, 4, 8, 12, or 16)
xxxx = Checksum/Hashsum value for this file in hex
yyyy = Type of file:
      4341 (for fdtver) or
      4441 (for dgnver) or
      4F41 (for oprver)
zz = Type of subunit:
     43 (for xtc or fdt) or
     53 (for SPU)
     55 (for D3U)
e f d g = file issue number d.efg

```

Figure 1 – DUMP:TSIFILE Printout

VERIFY NEW SYSTEM FILES WERE COPIED TO XTSI

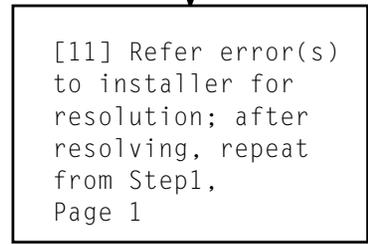
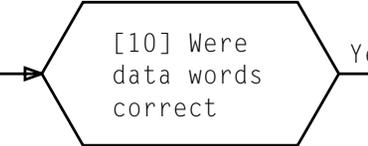
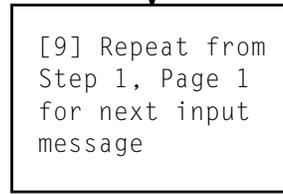
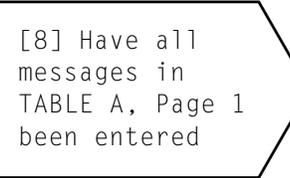
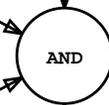
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[4] Using printout, and Figure 1, Page 2, compare checksum value in word 0 with associated checksum value from 3B printout saved earlier (Step 2). Record discrepancy for later use

[5] Using printout, and Figure 1, Page 2, compare software release issue in words 10, 11, and 13 with associated software release issue from 3B printout saved earlier (Step 2). Record discrepancy for later use

[6] Using printout and Figure 1, Page 2, verify type of file data in word 5 for associated message inputted. Record discrepancy for later use

[7] Using printout and Figure 1, Page 2, verify subunit type in word C (hex) for associated message inputted. Record discrepancy for later use



Yes

No

No

Yes

ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE
IXL-001		TAP-133		DLP-515							
NTP-002		TAP-134		DLP-516							
TAD-100		TAP-135		DLP-517							
TAP-101		TAP-136		DLP-518							
TAP-102		TAD-137		DLP-519							
• TAP-103		TAP-138		DLP-520							
TAP-104		TAP-139		DLP-521							
TAP-105		TAP-140		DLP-522							
TAP-106		TAP-141		DLP-523							
TAP-107		TAP-142		DLP-524							
TAP-108		TAP-143		DLP-525							
TAD-109		TAP-144		DLP-526							
TAP-110		TAP-145		DLP-527							
• TAP-111		TAP-146		DLP-528							
• TAP-112		TAP-147		DLP-529							
TAD-113		TAP-148		DLP-530							
TAD-114		TAP-149		DLP-531							
TAP-115		TAP-150		• DLP-532							
TAP-116		• TAP-151		• DLP-533							
TAP-117		• TAP-152		• DLP-534							
TAP-118		• DLP-500		• DLP-535							
TAP-119		DLP-501		• DLP-536							
TAP-120		DLP-502		• DLP-537							
TAP-121		DLP-503		• DLP-538							
TAP-122		DLP-504		• DLP-539							
TAP-123		DLP-505		• CKL-891							
TAP-124		DLP-506		TNG-893							
TAP-125		DLP-507									
TAP-126		DLP-508									
TAP-127		DLP-509									
TAP-128		DLP-510									
TAP-129		DLP-511									
ISD-130		DLP-512									
ISD-131		DLP-513									
TAP-132		DLP-514									

• REVISED OR ADDED ITEM

CANCELED ITEM

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CKL

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CHECKLIST