906A DATA DISTORTION TEST EQUIPMENT

TEST, INSPECTION, AND ALIGNMENT

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1. GENERAL

1.01 The 906A data distortion test equipment is installed in the 20A test board for use in routine testing and maintenance of the narrow-band trunks of the B1 data carrier system. This section covers test procedures for the location of trouble within the 906A.

1.02 Circuitry is provided within the 906A to facilitate testing of its performance. This circuitry is identified as the distortion calibrator circuit and it provides signals of various patterns and distortion for testing purposes.

1.03 The tests are divided into two broad categories, over-all or sectionalizing tests and trouble location tests. The normal testing procedure is to run through the over-all tests and go to appropriate sections in the detailed tests wherever part of the over-all tests fail. Detailed tests are designed to locate the trouble to an individual circuit package, network, or wiring.

2. PURPOSE

2.01 This section is issued to facilitate testing of the 906A data distortion test equipment.

3. APPARATUS

3.01 The following apparatus, or its equivalent, will be required for these tests:

- Simpson 269A VOM
- 908A Logic Circuit Test Set (J79908A)
- Hewlett-Packard type 403A AC Transistor Voltmeter

Note: Do not ground case when making balanced measurements.

- Extender Board of ED-73172

4. OVER-ALL OR SECTIONALIZING TESTS

DISTORTION CALIBRATOR CIRCUIT

4.01 A distortion calibration check is included as part of the 906A. It implements telegraph-type signals of various patterns and with variable amount of distortion for checking the performance of the distortion measuring circuit of the 906A. The distortion calibrator consists of CP8 and the calibrator control panel.

4.02 With the switches on the control calibrator panel in the TST, CONT (continuous hits), and BIAS positions, a dotting signal with marking bias is generated. The amount of BIAS is controlled by the DIST potentiometer.

4.03 With the switches in the TST, CONT, and MULT (multiple hits) positions, every start pulse is delayed, distorting all transitions in all characters.

4.04 With the switches in the TST, INT (intermittent hits), and MULT positions, a burst of 5 distortion hits is registered intermittently.

4.05 With the switches in the TST, INT, or SGL position, a single distortion hit is registered intermittently.

4.06 The MDM-SG switch connects the output of the signal generator of the 906A directly to the distortion measuring circuit, allowing for testing those circuits without the intervening modulator and demodulator.

4.07 Table A gives switch and key settings of the 20A toll testboard and distortion calibration for the over-all tests of this part. The headings at the top of the table are the same as the designations of the appropriate keys and switches of the 20A testboard.

4.08 The tests start with all keys normal, and, when no setting is indicated on a subsequent test, the keys are to remain the same. (---) indicates that where no designation is given to the key position, it is returned to normal.

F1/F2 MODULATOR

4.09 Tests 1 through 6 (Table A) measure the level of the output of the modulator at the terminal test cord.

4.10 Tests 7 through 12 measure the frequency of the output of the modulator.

SIGNAL GENERATOR AND DISTORTION MEASURING CIRCUIT

4.11 Tests 13 through 18 check the operation of the distortion measuring circuit and correlate the distortion meter readings with the thresholds of the hit counter.

4.12 Test 19 tests the distortion meter on isolated hits.

4.13 Test 20 checks the sync logic circuitry.

4.14 Test 21 checks the over-all timing sequence of the signal generator.

4.15 Test 22 checks the register on the hit counter.

F1/F2 DEMODULATOR

4.16 Test 22 is a measurement of data distortion in a looped back path consisting of signal generator, modem, and distortion measuring circuit. The test is a check of the residual distortion introduced by the modem.

4.17 If the demodulator passes the above test, it is sufficient to plug the rear terminal test cord into the GS jack and observe the same indications. This test tests the F2 operation of the demodulator.

4.18 In the case of demodulator malfunctions, it is necessary to make the tests outlined in the demodulator section, 5.06 through 5.13.

CHANNEL SELECTOR

4.19 The channel selector is used in making narrow-band and wide-band sectionalizing tests on a 4-wire facility. Narrow-band sectionalizing tests are those made on the 4-wire side of the B1 data terminals. Transmission, frequency, noise and data distortion tests may be made on each of the B1 data channels. The bridging amplifier and channel selecting circuitry is used in making the transmission, frequency, and noise measurements (4.20 through 4.22). In addition to these circuits, the measurement of disortion of a data channel involves the channel demodulator (4.23 through 4.26) and the F11F2 demodulator. On the supervisory channel, in addition to these tests, demultiplexing tests may be performed to monitor the E lead signals. The supervisory data distortion and demultiplexing tests are discussed in 4.29 through 4.32.

4.20 Wide-band sectionalizing tests are those made on the 4-wire facility of a full voice channel. Transmission, frequency, noise, and data distortion measurements may be made. The 906A is not used in making the transmission, frequency, and noise measurements. In making data distortion tests, the signal is connected directly to the F1/F2 demodulator (4.27 and 4.28).

BRIDGING AMPLIFIER AND CHANNEL SELECTING CIRCUITRY

4.21 This section describes the test for checking the operation of the circuits that permit high impedence monitoring of the signal in each of the six data channels and the supervisory channel of the B1 data carrier system as they appear on the 4-wire facility. Signal power, noise power, or the signal frequency may be measured in any of the channels. The portion of the 906A involved consists of a bridging amplifier (CP52), bandpass filters (included in FL2, 5, 6, and 7), and channel selector relays (CH1 through CH7).

4.22 Each of the seven channels has a bandpass filter; the channel selector relays select the output of the proper channel filter. The gain of the bridging amplifier is adjusted by the channel selector relays to match the loss of channel filter so that the average of the power at the mark and space frequencies, as measured on the transmission measuring set, is within 0.4 db of actual power on the line. However, the channel filter may introduce an additional difference in power between the mark and space frequencies of up to 0.8 db.

TABLE A

	20A Toll Testboard Controls													Distortion Calibrator Panel			
	Keys						Switches										
REAR KEYS	DMS BIAS	TMR	FRR	LEV-OUT HI		TMS	CHAN SEL	GEN SPEED	DIST CTR	GEN MODE				TST	MULT	CONT	SG
	DTA			NOR										OFF	SGL	INT	MDM
	SUPV	SND LEV	FRS CHK	LO	SEND SUPV	TMR									BIAS		
FRONT KEYS	DLY DIST†	TST	TMS														
	DLY DIST†	DMO	SND	SUB AGC	DATA READ	READ											

TEST	SETTINGS															
	All keys initially normal. Where no setting is indicated, key and switch positions remain the same as previous test.															
1. F1, normal level		SND LEV TST	SND	NOR			1	95.5	4	ALL POS	OFF	SG2	INT	MDM	Hold READ key operated.	Read -14.9 ±1 dbm on transmission measuring equipment. (LEV1 and LEV2 relays released)	Perform tests 2 to 6.
2. F1, high level			SND	HI						RDM					Hold READ key operated.	Read -9.9 ±1 dbm on TME. LEV2 relay operated.	If 1 to 6 fail, troubleshoot modulator section.
3. F1, low level				LO											Hold READ key operated.	Read -26.9 ±1 dbm on TME. LEV1 operated.	If 1 to 4 fail, troubleshoot CP31.
4. F1, below AGC level				SUB AGC											Hold READ key operated.	Read -35.9 ±1 dbm on TME. LEV1 and LEV2 relays operated.	If any of 1 to 4 fails, check operation of LEV1 and LEV2 relays.
5. F2, normal level				NOR ---											Hold READ key operated. Plug rear terminal test cord into GS jack.	Read -9.9 ±1 dbm on TME.	If 5 fails, troubleshoot CP31.

TABLE A (Cont)

20A Toll Testboard Controls											Distortion Calibrator Panel				Action	Expected Results	Action If Test Fails
	Keys						Switches										
REAR KEYS	DMS BIAS	TMR	FRR	LEV-OUT HI		TMS	CHAN SEL	GEN SPEED	DIST CTR	GEN MODE	TST	MULT	CONT	SG			
	DTA			NOR							OFF	SGL	INT	MDM			
	SUPV	SND	FRS	LO	SEND	TMR						BIAS					
FRONT KEYS	DLY DIST+	TST	TMS														
	DLY DIST-	DMO	SND	SUB AGC	DATA READ	READ											
TEST	SETTINGS																
All keys initially normal. Where no setting is indicated, key and switch positions remain the same as previous test.																	
6. SUPV, normal level					SEND SUPV	TMR READ	SUPV								Unplug rear terminal test cord. Hold READ key operated. Plug cord into GS jack.	Read -29.2 ±1 dbm on TME.	If 6 fails, troubleshoot CP32.
Normalize all keys; unplug LD test cord.																	
7. F1, mark frequency			FRS CHK			READ	1	95.5	4	MK					Turn on KS-19247, List 1, electronic counter. Set control to 1 sec.	Read frequency of 1270 ±1 cps.	Perform all tests 7 to 12.
8. F1, space frequency										SP						Read 1070 ±1 cps.	If all fail, troubleshoot CP33.
9. F2, space frequency															Plug rear terminal test cord into GS jack.	Read 2025 ±1 cps.	If 7, 8, 9, or 10 fails, troubleshoot CP31.
10. F2, mark frequency										MK						Read 2225 ±1 cps.	

TABLE A (Cont)

TEST	20A Toll Testboard Controls: Keys (REAR KEYS / FRONT KEYS)						20A Toll Testboard Controls: Switches				Distortion Calibrator Panel				Action	Expected Results	Action If Test Fails
	DMS BIAS	TMR	FRR	LEV-OUT HI		TMS	CHAN SEL	GEN SPEED	DIST CTR	GEN MODE	TST	MULT	CONT	SG			
	DTA			NOR							OFF	SGL	INT	MDM			
	SUPV	SND LEV	FRS CHK	LO	SEND SUPV	TMR						BIAS					
	DLY DIST+	TST	TMS														
	DLY DIST-	DMO	SND	SUB AGC	DATA READ	READ											
	SETTINGS Normalize all keys; unplug LD test cord.																
11. SUPV, mark frequency					SEND SUPV		SUPV								Unplug rear terminal test cord.	Read 385 ±1 cps.	If 11 or 12 fails, troubleshoot CP32.
12. SUPV, space										SP						Read 315 ±1 cps.	
	Normalize all keys; calibrate distortion meter (use CAL HI, CAL LO key).																
13. Meter calibration check, overflow lamp check	SUPV							95.5	4	RDM	TST	MULT	CONT	SG	Operate COUNT switch on display panel. Rotate DIST potentiometer slowly to right until message register just begins to count.	Distortion meter reads 4 ±0.5%. When counter counts OVERFLOW lamp comes on and will not stay out when RESET-START button is pushed.	If no distortion is indicated, troubleshoot CP8. If distortion is indicated but tests fail otherwise, troubleshoot distortion measuring set.
14.									8						Repeat test 13.	Meter reads 8 ±0.5%.	
15.		DMO						200	12						Repeat test 13.	Meter reads 12 ±0.5%.	
16.									16						Repeat test 13.	Meter reads 16 ±0.5%	
17.									20						Repeat test 13.	Meter reads 20 ±0.5%.	
18.															Turn COUNT switch off Turn potentiometer switch counterclockwise. Rotate potentiometer smoothly and slowly maximum clockwise.	Meter needle advances without any jumps.	

TABLE A (Cont)

TEST	20A Toll Testboard Controls										Distortion Calibrator Panel				Action	Expected Results	Action If Test Fails
	Keys						Switches										
	REAR KEYS										TST	MULT	CONT	SG			
	DMS BIAS	TMR	FRR	LEV-OUT HI		TMS	CHAN SEL	GEN SPEED	DIST CTR	GEN MODE	OFF	SGL	INT	MDM			
	DTA			NOR								BIAS					
	SUPV	SND LEV	FRS CHK	LO	SEND SUPV	TMR											
	FRONT KEYS																
	DLY DIST+	TST	TMS														
	DLY DIST−	DMO	SND	SUB AGC	DATA READ	READ											
	SETTING																
19. Single hit calibration	SUPV								20	RDM	TST	SGL	INT	SG	Rotate DIST potentiometer clockwise until a single hit is just registered periodically on register.	Meter reads peaks of 19 to 20%. OVERFLOW lamp stays out when RESET-START button is pushed.	Troubleshoot distortion measuring set.
20. Sync Logic	DTA								20	RDM	TST	SGL	INT	SG	Push SYN RESET button.	OUT SYN lamp goes out and stays out.	Troubleshoot distortion measuring set.
21. Signal generator timing check	SUPV							95.5	16							Time between hits = 7.2 to 7.3 seconds.	Troubleshoot signal generator.
22. Hit counter check	SUPV											MULT			Press RESET-START button between bursts. Switch DMS key to DTA and rotate DIST potentiometer counterclockwise until register stops counting.	Register registers 5-10-15-20, etc. When switched to DTA mode, register counts 1-2-3-4, etc. Register should stop counting single hits when meter reads less than 19. 0 to 5%.	Troubleshoot hit counter.
23. Demodulator	DTA	TST		NOR			1	200			OFF			MDM	Push SYN RESET button.	OUT SYN lamp goes out and stays out. Distortion meter reads 0 to 5%	

4.23 To check the operation of this portion of the circuit, perform the following test:

(a) Connect output of 600-ohm balanced oscillator (OSC jack) to LD cord and ground sleeve of cord. This can be done by using the BRIDGE GS jacks if available. Operate key FREQ-NSE to FREQ and block key READ operated. Set oscillator for 640 ±2 cps reading on frequency counter. This is the mark frequency for channel 1.

(b) Restore FREQ-NOISE key and operate key TMR-TMS to TMR. Adjust oscillator for reading of 906 —24.0 ±0.1 dbm.

(c) Disconnect LD cord and connect oscillator to MON cord through circuit of Fig. 1. The OSC IN and MON TEST jacks may be used if they are available. Set switch CHAN SEL to 1. (Relay CH1 operates.) Record to nearest 0.1 db the reading on the transmission measuring set.

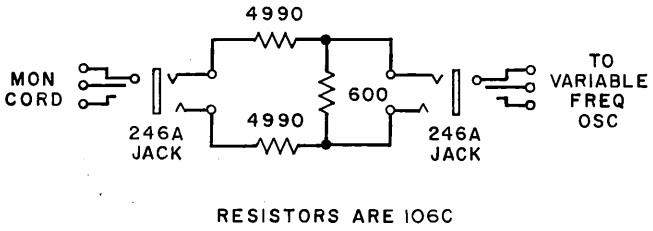

Fig. 1 — Jack Circuit

(d) Repeat (a) through (c) for a frequency of 840 cps, which is the space frequency for channel 1. This reading must be within 0.8 db of that in (c); if not see 5.28.

(e) Average of recorded readings should be within 0.4 db of the reading in (b).

(f) Repeat (a) through (e) for the following settings of the CHAN SEL switch and pairs of frequencies:

CHAN SEL	Mark	Space	Relay Operated
	cps		
2	1118	1318	CH2
3	1595	1795	CH3
4	2073	2273	CH4
5	2550	2750	CH5
6	3028	3228	CH6
SUPV	315	385	CH7

Note: When finished, return all keys to normal.

4.24 If any of the averages of the mark and space power are not within 0.4 db of the input power, see 5.15 through 5.30. The operation of the relays may be checked using SD-73022-01, Sheet B7.

CHANNEL DEMODULATOR

4.25 This section describes the test for checking the circuitry that shifts the frequency band of the data channel, selected as in 4.20 and 4.21 to the F2 band so that the data distortion may be measured. The portion of the circuit that performs this function consists of a channel demodulator on CP51, low-pass filters included in FL5, 6, and 7, a channel amplifier on CP51, the channel selector relays CH1 through CH7, and relays TMC and DDC. The channel demodulator, which shifts the frequency band, is supplied with the necessary carrier frequencies from a B1 data carrier supply unit. The carrier frequency appropriate to the selected channel is connected to the channel demodulator by the channel selector relays.

4.26 The output of the channel amplifier is connected to the F1/F2 demodulator (4.16 through 4.18) and the data distortion is then measured as in the over-all tests. Therefore, it is necessary that the data demodulator and distortion measuring circuit are working properly so that sectionalizing data distortion measurements may be made. Thus, it is assumed that these tests are satisfied before performing the test de-

scribed below, since it checks the signal only as far as the input to the data demodulator.

(a) Adjust the output power of the 600-ohm balanced oscillator (OSC jack) to —24 ±1 dbm.

(b) Connect oscillator to MON cord through circuit of Fig. 1 or use 906 OSC IN and MON TEST jacks. Connect a terminal test cord to the 906 DEMOD INPUT MEAS jack. Operate key SUPV-DATA to DATA and block operated key DATA READ.

(c) Set oscillator frequency to 740 ±20 cps and CHAN SEL switch to 1 and hold operated key TMR-SND LEV to TMR. (Relays DDC, TMC, and CH1 are operated.) On the transmission measuring set, read —19 ±3 db for an oscillator output of —24 dbm.

(d) Release key TMR-SND LEV and hold operated key FRR-FRS CHK to FRR. Read 2125 ±20 cps on the electronic counter. Release key FRR-FRS CHK.

(e) Repeat (c) and (d) for the following frequencies and settings of the CHAN SEL switch:

CHAN SEL	CPS	Relays Operated
2	1218	DDC, TMC, CH2
3	1695	DDC, TMC, CH3
4	2173	DDC, TMC, CH4
5	2650	DDC, TMC, CH5
6	3128	DDC, TMC, CH6

(f) Set switch GEN SPEED to each of its positions. Each time the position is changed, momentarily release the DATA READ key. For each position, the lamps corresponding to the switch setting should light.

(g) When finished, return all keys to normal.

4.27 A detailed discussion of the location of causes for failure of the above test is given in 5.31 through 5.36. If any of the measured frequencies is wrong, there is an error in the carrier frequency being supplied from the B1 data carrier supply unit. (See 4.56.) If any of the measured powers is wrong, make sure that 4.22 is satisfied. If the trouble remains, see 5.32 through 5.35. If no signal gets through at all, see 5.32 through 5.34. The operation of the relays may be checked from SD-73022-01, Sheets B7 and B6.

4.28 If the set fails to measure distortion satisfactorily on B1 system tests even though working on local test (4.15) and the above test, there may be troubles in the channel demodulator. (See 4.35.)

CIRCUIT FOR MEASUREMENT OF DISTORTION ON 4-WIRE WIDE-BAND CIRCUIT

4.29 The signal from the 4-wire facility is connected to the input of the data demodulator by the DMC relay. The output of the demodulator goes to the distortion measuring circuit, and the data distortion is measured as in 4.01 through 4.08. The operation of the F1 relay which controls the frequency of the demodulator is controlled by the F lead. Assuming the tests of 4.15 through 4.17 work, these functions may be checked by the following test.

(a) Connect a front terminal test cord to a line drop (LD) cord and ground the sleeves of the cords. This can be done using the BRIDGE GS jacks in the 20A if they are available.

(b) Operate keys and switches as follows:

(1) DATA-SUPV to DATA

(2) WBF1 to WBF1

(3) SND-TMS to SND and block operated

(4) DATA READ block operated

(5) TST-DMO to TST

(6) GEN MODE to RDM

(7) GEN SPEED to 150

(8) LEV OUT to LO

(Relays A, B, C, GS1, GS3, F, DMC, DDC, and TMC are operated.)

(c) Momentarily operate key SYN RST on display panel. Lamp OUT SYN should go out and stay out. The meter should read approximately 4. Disconnect cords.

(d) Connect a rear terminal test cord to the LD cord and ground the sleeves. This can be done using the BRIDGE GS jacks in the 20A if they are available. Operate key WBF1 to F2. (Relay F1 releases and F2 operates.) Repeat (c).

(e) Restore keys to normal.

(f) If this test fails, see 4.30.

4.30 In making wide-band data distortion measurements, the input from the data test cord circuit is connected directly to the data (FSK) demodulator by the DMC relay. The signal path can be checked, as shown as follows under the conditions of 4.29.

Location	Reading		Trouble
	F1	F2	
	dbm		
TS(B) 44,34	−27 ±4	−22 ±4	Signal not received from 20A or short in wiring* that follows
TS(B) 37,27	Same as above		Relay DMC or wiring

* The wiring can be traced using SD-73022-01, Sheet B6.

SUPERVISORY-DEMODULATOR-DEMULTIPLEXER

4.31 The following sequence of tests may be performed to check the performance of the supervisory-demodulator-demultiplexer.

A. Supervisory Input Signal

4.32 *Verification That a 906A Generated Supervisory Dotting Signal Appears at the Supervisory Input:* Arrange the data signal generator to deliver a 95.5-bps dotting signal at the supervisory frequency (350 ±35 cps) on the GT and GR leads by operating GEN MODE switch to DOT and by operating the SEND SUPV switch. Establish a back-to-back signal path through the 20A toll testboard by operating relays SSV, SV, and RD1. This is accomplished by operating the SUPV key and the DATA READ key. A supervisory dotting signal should be present on leads CT and CR in the 906A. A measurement of level at AMPO will verify this; the level should read between −14 and −22 dbm at test point AMPO on CP52 as read with the high impedance TVM with respect to ground. If this requirement cannot be met, sectionalize the signal generator, modulator, and/or channel selector circuits for the trouble.

B. Supervisory Lamp States—Bias Adjustment

4.33 *Verification of Proper Supervisory Lamp States in Conjunction with a Bias Adjustment if This Adjustment is Required*: Operate relays CH7 and TMC by operating the CHAN SEL switch (20A toll testboard) to position SUPV; relay SMC in the 906A will then operate TMC. A supervisory dotting signal should become available at the demodulator output. This dotting signal is then demultiplexed and directed to the CH lamp circuit through the contacts of relay SMC. The demultiplexed dotting signal should result in a steady on signal for the SYN lamp and alternate frame flashing for each of the six CH lamps. The sequence of flashing is lamps 1, 3, and 5 simultaneously on, followed by lamps 2, 4, and 6 simultaneously on, repeating until this test connection is broken down. If these

lamp states are obtainable, the supervisory bias can be measured, adjusting if necessary, and end the routine maintenance or verification. If these lamp states are not obtainable, adjust the supervisory bias and again attempt to obtain the lamp states. If bias cannot be adjusted, sectionalize trouble to the supervisory demodulator. If the bias can be adjusted but the desired lamp states are unobtainable, sectionalize trouble to the supervisory demultiplexer. The bias adjustment of the supervisory demodulator (screwdriver adjusted potentiometer on CP63) is accomplished as follows. Under the conditions resulting in a demodulated 95.5-bps dotting signal, connect the supervisory demodulator output to the distortion measuring circuit by operating relay SSC. SSC is operated when CRD and SV are operated in the 20A; these were operated when SMC was previously operated. Operated relay BD by operating the DMS BIAS key; this will condition the distortion measuring circuit to measure supervisory bias. Adjust the BIAS potentiometer while operating the BIAS key on the display panel alternately between MK and SPC. Equal minimum readings in both key positions of less than 5 per cent will be the zero bias point.

C. Distortion Check

4.34 *Verification That Distortion is Less Than 8 Per Cent for the 906A Generated Supervisory Dotting Signal*: Operate the DMS SUPV key. This will cause the BD relay to be released and the PS relay to operate, which will condition the distortion measuring circuit to measure the distortion. The distortion as read on the meter should not exceed 8 per cent. If this requirement cannot be met but all previous supervisory requirements are met, trouble should be sectionalized in the supervisory demodulator or in the distortion measuring circuit.

5. TROUBLE LOCATION TESTS

F1/F2 MODULATOR

5.01 If the tests outlined in 4.01 to 4.16 fail to indicate signals of the correct frequency or level at the data test cord, troubleshoot the modulator consisting of circuit packages CP31 to CP34 and associated pads and networks.

5.02 The test procedures outlined here will indicate that where a signal is not present on an output of a circuit package it is not being generated by that unit. However, this condition can also be brought about by an external short circuit on the circuit package output. Therefore, tests must be made to determine whether any short circuits exist; in order to make these tests, it may be necessary to remove the circuit package whose output is being examined. Tests on the modulator are conventional signal tracing tests, as input and output test points are placed on all circuit packages except the input to the binary counter. The test may be made in any order in case there is reason to suspect any particular unit.

5.03 For these tests, it will frequently be necessary to gain access to the electronic counter on the 20A toll testboard for frequency measurements. This is done by plugging the LD cord into the R jack and operating the FRS CHK key. The frequency to be measured is then led from the appropriate test point to the R test point on the CP8.

5.04 *CP34:* With the ACTVM measure level the same as that indicated in Test 2 of Table A with the LEV-OUT key in the HI position and the SUB AGC key normal on the AO test points of CP34. This test should be done with the switch settings that were made when the test described in Test 2 of Table A failed. If no signal is found on the AO test points, measure the level on the AI test point to ground; this should be 23 db below that expected on the AO test points. If a signal is measured on the AI test point, the amplifier on CP34 is out of order or its output is shorted externally. If no signal is found on the AI test point, a signal of -16 ± 2 dbm should be measured on the MO test point. If a signal is found at these test points, the filter or pad circuitry and its associated wiring shown on SD-73022-01, B5 must be checked for open or short circuits. If no signal is found on these test points, connect the 908A to the IN test point on CP34. The 908A should indicate the frequency shown in 5.05.

5.05 Should the signals below not appear, proceed to the BC test point on CP33 and make the tests indicated in 4.23 (f). In case of a specific failure in any one switch setting, CP31 is

suspected if the data supervisory switch is in the data position; CP32 is suspected if it is in the supervisory position. In order to test CP31 and CP32, ground the DM test point on CP31 and the DS test point on CP32. A voltage of 5 to 7 volts dc should be measured on the OSC test point of CP31 and CP 32. If the ground is removed from the DM test point with the data supervisory switch in the data mode, a voltage of 2 to 3 volts should be measured on the OSC test points. Similarly, if ground is removed from the DS test point with the data supervisory switch in the supervisory position, a 2- to 3-volt signal should be measured on the OSC test points. If this voltage is measured, the oscillators are oscillating. With no signal on the BC test point on CP33, the binary counter stages or the wiring between CP31, CP32, and CP33 must be suspected. If the correct voltages are not measured on the OSC test points, remove CP32 and repeat the test, using the voltage measurements above. If the correct voltages are not measured, CP31 is suspected. If the correct voltages are measured, repeat the above for CP32. Card CP33 may also be removed to see if its inputs are shorting the outputs of CP31 and CP32.

GEN MODE	DATA-SUPV	Terminal Test Cord	908A Reading ±10 Per Cent
MK	DATA	OUT	2540
SP	DATA	OUT	2140
SP	SUPV	OUT	630
MK	SUPV	OUT	770
MK	SUPV	IN GS Jack	4450
SP	SUPV	IN GS Jack	4050

DEMODULATOR

5.06 If the demodulator part of the over-all section fails, troubleshoot the demodulator. The tests outlined here will be conventional signal tracing tests. Tests made at F1 will be made with the sleeve of the rear terminal test cord ungrounded, and tests at F2 will be made with the sleeve of the rear terminal test cord grounded. F1 or F2 tests will be made depending on which test failed in the over-all demodulator section. F1 tests only will be described here, as grounding the sleeve of the rear terminal test cord by plugging it into GS jack will be sufficient to make the F2 tests. Where signal levels differ at F2, these levels will be shown in parentheses.

5.07 Normalize all keys on the 20A testboard and the distortion calibrator panel. Set GEN SPEED to 200, CHAN SEL to 1, and GEN MODE to DOT. Lock the TST-DMO keys to DMO. The 906A is now set up to transmit dotting signals from the modulator, back-to-back, to the demodulator.

5.08 By means of the 403A ACTVM, measure a signal of −30.5 ±5 dbm (F2, −25.5 ±5) on terminal points LS1-LS0 of CP43. If this signal is not present, go to terminals 7 and 8 of CP43 and measure a level of −30 ±5 dbm (F2, −25 ±5). If this signal is present, the transformer on CP43 is defective.

5.09 Measure a level of −24 ±5 dbm (F2, −19 ±5) on the AMP test point of CP41. If this signal is not present, the line amplifier of CP41 is defective. Measure a signal of −25.5 dbm (F2, −20.5 ±5) on the LIN test point of CP41. If this signal is not present, the filter associated with the frequency being tested is defective.

5.10 Measure a voltage of 5 ±1 volts on each of the two test points LOUT of CP41 to ground, and measure a voltage of 10 ±1 volts between the two LOUT test points on CP41. If any of these voltages are not correct, the limiter of CP41 is defective.

5.11 Measure a voltage of 1.6 ±0.4 volts between the two test points MFO on CP42 and measure the same voltage between the two test points SFO on CP42. If these voltages are not present, CP42 is defective.

5.12 Measure a voltage of 0.32 ±0.1 volt on test points LP0 and LP1 of CP43. If this voltage is not present, CP43 is defective. Measure a voltage of 5 ±1 volts ac on the SLO1 test point on CP44. Using the same test point, measure a frequency of 100 ±5 cps by means of the 908A logic circuit test set. If either of these tests fails, CP44 is defective.

5.13 If all of the above tests are passed, trouble may be located in the wiring on the output of the demodulator or in the distortion measuring set.

CHANNEL SELECTOR

5.14 The purpose of this section is to aid in locating defective wiring or pieces of equipment such as filters, relays, or circuit boards. No attempt is made to give repair instructions except for the adjustment of the gain of the bridging amplifier (CP52). In most cases, wiring to the relays may be checked by working directly from the SD. In addition to the test equipment built into the 20A testboard, an HP 403A ac transistor voltmeter, a 908A logic circuit test set, and an extender board ED-73172 are needed.

TABLE B

Test	Test Points	Reading dbm	Trouble
1	32, 42 TS (E)	−30 ±3	Trouble not in 906A. See data test cord circuit SD-56528-01.
2	AMPI; CP52	Same as 1	Wiring
3	AMPO, GRD; CP52	−18 ±3	CP52
4	TI, GRD; CP52	−20.7 ±2	FL2, 5, 6, or 7, depending on channel (see SD-73022-01, B7) or wiring
5	PT, PR; CP52	−22 to −26	CP52; replace and repeat 4.22*
6	12, 22 TS (E)	Same as 5†	Wiring

* If the trouble is in CP52, replace it and repeat test of 4.23.

† If reading of test 6 is correct, the trouble is not in the 906A. See the Data Cord Circuit SD-56528-01.

A. Bridging Amplifier and Channel Selecting Circuit

5.15 The bridging amplifier and channel selecting circuit consists of CP52; FL2, 5, 6, and 7; and relays CH1 through CH7.

Signal Path

5.16 Under the conditions of the test of 4.23, the signal can be traced through the circuit at any frequency by checking the points listed in Table B. The measurements are to be made with the ac transistor voltmeter. Although it is not accurate enough for making the gain adjustments described in 5.14 through 5.27, it is sufficiently accurate to locate serious troubles. If a reading is not as indicated, the trouble is given in the trouble column. The entries in the trouble column assume that the lower numbered readings are satisfied. Since the signal path cannot be opened, failure to meet requirements may be caused by trouble in the following stage as well as by the listed trouble.

B. Gain Adjustment

5.17 There are two major contributors to an incorrect reading on the transmission measuring set in the test of 4.23: the bridging amplifier (CP52) and the channel filters (FL2, 5, 6, and 7). Any combination of channels may be bad.

5.18 If the basic gain of the amplifier is off, all channels will be off but a single bad filter can affect all channels. Since the filters are connected in parallel on their input side, a shorted input, for example, on one filter could affect all channels.

5.19 Since the loss will be different for different filters, the gain of the amplifier is matched to the filter loss by changing the input resistor combination through contacts on the channel selector relays (CH1 through CH7). Thus, the gain of the amplifier may be off for some channels but not for others. The filters can affect individual channels.

5.20 If the measurements of 4.23 indicate that the basic gain of the amplifier has drifted, ie, all (or most) of the channels are clustered about some average value other than −24.0 dbm, the basic gain of the amplifier can be adjusted over a limited range by varying potentiometer R21 on CP52. It is accessible only if CP52 is put on the extender board. For example, if the averages of the output power for the mark and space frequencies in each channel clustered about −24.3 dbm rather than −24.0 dbm, R21 would be varied as follows: with the setup of A and either the mark or space frequency of the channel with an average reading closest to the desired setting, vary R21 until the reading is increased by 0.3 db. If the required correction cannot be made, replace CP52 and repeat 4.21. Some adjustments may be necessary on the new board. If the new board fails, examine the wiring and filters.

5.21 If an individual channel still is off after adjusting the gain, the trouble may be in CP52 or the channel filter or in some other channel filter. The following points may be used as a guide.

5.22 If the signal through a channel is off by more than 1 db, the trouble is in a filter. (See 5.28 through 5.30.) If a gain adjusting resistor is bad, it will affect all channels using that resistor; that is, only bad channels and no others would have the same resistor in common. This can be checked by examining contacts 5M, 6M, and 8M on the channel selector relays since each of these contacts is associated with one of the three input resistors. The resistors are wired to the contacts on a given relay according to the gain needed for that channel. Thus, if channels 3 and 5 are bad and contact 8M is wired on relays CH3 and CH5 and no others, it is most likely that the resistor associated with contact 8M is bad. If there are no other channels using a resistor used by a bad channel, temporarily connect that resistor to the relay of a good channel and check that channel. The gain should change according to the following chart which shows the relative gain of the amplifier for each of the input resistor (relay contact) combinations. The change should be equal to the difference in gain for the two resistor combinations. If not, the resistor is bad.

Contacts Used	Relative Gain
	db
None	1.9
8M	1.6
6M	1.3
8M and 6M	1.0
5M	0.7
5M and 8M	0.4
5M and 6M	0.2
5M, 6M, and 8M	0

5.23 As a temporary remedy if a resistor is bad, another resistor combination may be used so that the average is still −24 ±0.02 dbm. Refer to the above chart and select the combination closest to the existing one. Temporarily wire in this combination to the appropriate channel selector relay and recheck the channel according to test in 4.23. Several tries may be necessary.

5.24 If a channel is beyond limits by less than 0.5 db and there is no trouble with an input resistor, the gain of the amplifier can be corrected for that channel by using a different combination of resistors. (See 5.22.) Obtain a new combination by adding or subtracting the error from the gain corresponding to the present combination and then using that combination which gives the closest gain.

C. Channel Bandpass Filters

5.25 Troubles in the channel filters may be shown in many ways. The two most obvious are for the output power in test 4.23 to differ by more than 0.8 db between the mark and space frequencies and for the loss of an individual the channel to be markedly different from that of other channels. In either case, the trouble is most likely in the filter of the channel in trouble.

5.26 Other troubles may arise in the filters on rare occasions and give rise to puzzling trouble conditions. The input impedance of a filter may be low instead of high outside the pass band, thus causing additional loss in some of the other channels, or the filter may inadequately suppress signals from other channels (particularly in the case of crosstalk between the two channel filters contained in a single filter can). This trouble could result in high data distortion readings or high noise measurements.

5.27 Before replacing any filter, disconnect it from the circuit and make an insertion loss test. Check the filter at the center frequency (the average of the mark and space frequencies) and at the mark and space frequencies. All the filters are 600 ohms unbalanced. The loss at the center frequency should be less than 3 db, and the loss at the mark and space frequencies should be within 0.8 db of each other and not more than 1.5 db greater than the loss at the center frequency. See SD-73022-01, Sheet B7 for connections.

D. Channel Demodulator

5.28 The channel demodulator consists of CP51; FL5, 6, and 7; and relays TMC, DDC, and CH1 through CH7.

Signal Path

5.29 The signal can be traced through the circuit by setting up test of B and checking the points listed in Table C with the ac transistor voltmeter. Assume that the frequencies in 4.25 are correct. If a reading is not as indicated, the trouble is given in the trouble column. The entries in the trouble column assume that all the lower number tests are satisfied. Since the signal path cannot be opened, failure to meet requirements may be caused by trouble in the following stage as well as by the listed trouble.

TABLE C

Test	Test Points	Reading for Input of -24.0 dbm dbm	Trouble
1	DEM I, GRD; CP51	−20.7 ±1.5	Wiring
2	DEM O, GRD; CP51	Channel 1 −33 ±3 2 −33 ±3 3 −36.5 ±3 4 −37 ±3 5 −38 ±3 6 −39 ±3	CP51 (or carrier supply, see 4.54)
3	AMP I, GRD; CP51	−40.2 ±2	Low-pass filter, FL5, 6, or 7 depending on channel, see SD-73022-01, B7
4	AMP O; CP51	−18.7 ±2	CP51*
5	16, 26 TS(F)	Same as 4	Wiring
6	35, 45 TS(B)	Same as 5†	Cabling

* If the trouble is in CP51, replace it and repeat test of 4.25.

† If the reading of test 6 is correct, the trouble is in the wiring from TS(B) to the contacts of the DDC relay.

E. Data Distortion (Narrow-Band)

5.30 The preceding table should reveal most troubles; however, there are possible causes of excessive data distortion that would not be detected. If the channel demodulator is not functioning properly, it can cause excessive carrier or signal leak or high harmonic content in the output. A low-pass filter may not have the desired cutoff characteristic, or a channel bandpass filter may not have adequate out of band suppression (5.25 through 5.27). Any of these conditions could result in interfering signals reaching the data demodulator along with the data signal and raising the data distortion.

F. Carrier Supply

5.31 To shift the frequency band of a data signal from the channel frequency to the F2 frequency (2125 cps), the channel demodulator is supplied with carrier frequencies, one for each channel, from a B1 data carrier supply unit. These carriers arrive on leads 1U, 1G through 6U, 6G and are connected through the channel selector relays to the channel demodulator (CP51) where the selected carrier appears on test points CARR. The carrier frequencies correspond to the channels as follows:

Channel	Leads	Punchings on TS (F)	Frequency cps
1	1U, 1G	12, 22	2865
2	2U, 2G	32, 42	3342.5
3	3U, 3G	13, 23	3820
4	4U, 4G	33, 43	4297.5
5	5U, 5G	14, 24	4775
6	6U, 6G	34, 44	5252.5

These frequencies may be measured to an accuracy of ±150 cps using the 908A logic circuit test set. Connect the ground from the 908A to the G lead. Each carrier should measure approximately 0.9 volt rms at the CARR test points when measured with the 403A TVM.

SUPERVISORY-DEMODULATOR-DEMULTIPLEXER

5.32 The supervisory-demodulator-demultiplexer may be internally sectionalized to locate defective cards if any over-all test indicates that a supervisory trouble may exist. The circuits as subdivided for maintenance purposes are as follows:

(a) *Demodulator* (CP61, CP62, CP63) converts a 350 ±35 cps FSK wave to a data train with TRL levels of +5.2 volts and +0.2 volt as the two states.

(b) *Demultiplexer Clock and Steering Memory* (CP64, CP67, CP68) subdivides 3820-cps square wave to 95.5 cps for bit sampling and further subdivides to the framing rate, and provides suitable sequencing inputs for the steering gates (CP70).

(c) *Demultiplexer Sync Recovery* (CP64, CP65, CP66, CP69) examines sync transitions for proper sync or searches for sync as required.

(d) *E Lead Desampling, Steering, and Memory* (CP69, CP70) gates samples of the data train into proper memory registers corresponding to E lead states.

(e) *Sync-Loss Indicator* (CP62) follows the state of K lead by means of SYN lamp and increments counter in a timed period.

5.33 The steps for finding trouble are subsequently tabulated. A 95.5-bps dotting signal should be received by the demodulator in order to apply these tests. While the usual action for an improper test result is to replace a card, the fact that troubles can arise in connectors as well

as wiring should not be ignored. If for any reason the replacement of a card does not clear the trouble, a careful examination of the signal paths, and leads and connectors leading to the card in trouble, should be made to determine if a trouble has developed in these paths. Perform the tabulated tests in the indicated order, unless it is thoroughly understood that such omitted tests would not overlook a possible trouble or necessary circuit preparation.

A. Demodulator—Table D

5.34 This table traces the input signal to the demodulator (TP MO, TP SI), through the limiter (TP LL, TP LO), to the discriminator (TP DO), and to the sliced output (TP BI) which is the regenerated data train. The inverted output (TP $\overline{\text{BID}}$) is verified as well as tracing the 3820-cps clock signal to the squaring circuit (TP CAS) and to the squared output (TP 3820).

B. Demultiplexer Clock and Steering Memory-Table E

5.35 Two inputs to the demultiplexer clock exist: a 3820-cps square wave (TP3820), tested in Table D and the clock inhibit signal (TP G) which prevents countdown when G is in the high state. Test points TP $\overline{\text{C1}}$, TP $\overline{\text{C5}}$ TP $\overline{\text{C6}}$ are intermediate points in the demultiplexer clock counting chain. Test points TP DA, TP DB, and TP DC are in the binary stages referred to as E lead steering sequence. In reality these are stages which continue the countdown sequence of the demultiplexer clock, but are used to sequence the E lead samples into the proper registers.

TABLE D — DEMODULATOR

Test Number	Circuit Package	Test Point	Instrument	Setting	Special Preparation	Test Result	Action for Incorrect Test Result
1	CP61	SI	TVM	—20 dbm	Arrange 20A controls to receive supervisory dotting on test point SI by setting the controls as indicated in 4.31.	>25 dbm	Replace CP61 or CP62
2	CP34	MO	908A	500AF		35 ±2	Troubleshoot modulator (5.01 through 5.05)
3	CP61	LL	908A	500AF		35 ±2	Replace CP61
4	CP61	LO	908A	500AF		35 ±2	Replace CP61
5	CP63	DO	908A	50AF		48 ±2	Replace CP63
6	CP61	BI	908A	50DF		48 ±2	Replace CP61
7	CP62	$\overline{\text{BID}}$	908A	50DF		48 ±2	Replace CP62
8a	CP62	CAS	908A	5000AF		38 ±2	Troubleshoot channel selector (5.14 through 5.31)
8b			TVM	1 volt		>0.5 volt	
9	CP64	3820	908A	5000DF		38 ±2	Replace CP62

TABLE E — DEMULTIPLEXER CLOCK AND STEERING MEMORY

Test Number	Circuit Package	Test Point	Instrument	Setting	Special Preparation	Test Result	Action for Incorrect Test Result
1	P64	G	908A	TRL(+) 50DF	Continue to receive dotting per Table D.	Lamp flashes 10 ±2	Ground test point G; continue and use starred (*) test results where given
2	P64	C1	908A	5000DF		*19 ±2	Replace CP64
						17 ±2	
3	P67	C5	908A	500DF		*19 ±2	Replace CP67
						17 ±2	
4	P68	C6	908A	500DF		*9.5 ±2	Replace CP68
						8.5 ±2	
5	P68	DA	908A	50DF	Ground TP G on CP64 if not previously grounded.	48 ±2	Replace CP68
6	P68	DB	908A	50DF		24 ±2	Replace CP68
7	P68	DC	908A	50DF		12 ±2	Replace CP68

* Requirements if G is grounded.

C. Demultiplexer Sync Recovery — Table F

5.36 Sync recovery logic initially tested under the condition of continuously running clock (TP G grounded) and with the circuit out-of-sync (TP K grounded). This condition is similar to the in sync condition since the sync sampling gates are saturated (65-8, 65-9) with lead $\overline{P}$ changing the state of the H flip-flop, as is the case when the system is running in synchronism. A duty cycle (bias) measurement is made on the P, FP, and T pulses to verify that they are of proper length. With a verification of leads $\overline{T}$ and $\overline{BI}$, enough inputs exist to check the output of the sync transition sampling gates, leads FB and FH, and verify that the outputs on leads FE and FD are blocked for lead G at ground. Lead G is then forced to the high state which stops the demultiplexer clock and opens the sync recovery sampling gates which permits pulses on the FD and FE leads. The grounds on TP FG, FP, and T are removed and lead K is again grounded. The aperture preparation pulse appears, as a result of the running of the demultiplexer clock, and changes the state of the H binary cell at a constant rate. In this condition, either FT or FU as well as FC and FG will have pulses in the output. When test point G in ungrounded and lead KS is grounded, the G flip-flop follows FP and FG. With KS ungrounded, the gate should be blocked if the demultiplexer clock is not running. When the K ground is removed, synchronism should be covered with test point K high and $\overline{K}$ low. If test point H is grounded, $\overline{K}$ should go high indicating loss of sync.

TABLE F — DEMULTIPLEXER SYNC RECOVERY

Test Number	Circuit Package	Test Point	Instrument	Setting	Special Preparation	Test Result	Action for Incorrect Test Result
1	CP65	P	908A	BIAS (—)	Receive dotting per Table D. Ground TPG and TPK on CP64.	41.3 ±2.0	Replace CP65
2	CP64	FP	908A	BIAS (—)		41.3 ±2.0	Replace CP65
3	CP65	T	908A	BIAS (—)		42.5 ±2.0	Replace CP65
4	CP66	T	908A	BIAS (+)		42.5 ±2.0	Replace CP65
5	CP66	$\overline{BI}$	908A	50DF		48 ±2	Replace CP69
6	CP65	FB	908A	50DF		48 ±2	*Replace CP66
7	CP65	FH	908A	50DF		48 ±2	*Replace CP66
8a	CP65	FD	908A	TRL (+)		OFF	Replace CP65
8b				MP (+)		No repetitive flashing	
9a	CP65	FE	908A	TRL (+)		OFF	Replace CP65
9b				MP (+)		No repetitive flashing	
10	CP65	FD	908A	MP (+)	Receive dotting per Table D. Remove ground on TPG, CP64; ground TP FG, TP FP, TP K on CP64 and TP T on CP65.	Lamp flashes	Replace CP65
11	CP65	FE	908A	MP (+)		Lamp flashes	Replace CP65
12	CP65	H	908A	50DF	Receive dotting per Table D. Remove grounds from TP FG, TP FP on CP64, and TP T on CP65; ground TP K and TP G on CP64.	6 ±2	Replace CP65
13	CP66	†FT or FU	908A	50DF		6 ±2	Replace CP66
14	CP64	FC	908A	50DF		6 ±2	Replace CP66
15	CP64	FG	908A	50DF		6 ±2	Replace CP66
16	CP64	G	908A	50DF	Receive dotting per Table D. Ground TP KS on CP64; remove ground on TP G, CP64.	11 ±2	Replace CP64

TABLE F — CONCLUDED

Test Number	Circuit Package	Test Point	Instrument	Setting	Special Preparation	Test Result	Action for Incorrect Test Result
17	CP64	KS	908A	MP(+)	Remove ground on TP KS on CP64.	No repetitive flashing	Replace CP64
18	CP64	K	908A	TRL(+)	Remove ground on TP K on CP64.	ON	Replace CP64
19	CP62	$\overline{K}$	908A	TRL(+)		OFF	Replace CP64
20	CP62	$\overline{K}$	908A	TRL(+)	Ground TP H CP65.	ON	Replace CP64

* Some initial production circuit packages may give incorrect test results even though properly functioning, due to the excessively short period of the monopulsers. Should there be a failure in the tabulated test, the 908A should be set to MP(−) and a very rapid flashing or steady glow should be observed to determine if the monopulser output is present. The timing capacitors (C1 and C2) of monopulsers 66-1, 2 and 66-7, 8 should be more than 2200 uuf to guarantee proper performance under the tabulated test as starred (*).

† May be either.

D. E Lead Desampling, Steering, and Memory-Table G

5.37 The dotting data train BI and its inverse $\overline{BI}$ are verified, followed by a verification of the sample pulse on lead SP. The samples of BI and $\overline{BI}$, termed RESET and SET, respectively, are verified at the sampled data output. The sequential gating of these pulses (steering) is verified at test points SR and RR as the pulses are placed in the registers (memory). The register state changes, due to the dotting signal, are verified at test point E.

TABLE G — E LEAD DESAMPLING,STEERING, AND MEMORY

Test Number	Circuit Package	Test Point	Instrument	Setting	Special Preparation	Test Result	Action for Incorrect Test Result
1	61	BI	908A	50DF	Remove ground on TP H CP65. Receive dotting per Table D.	48 ±2	Troubleshoot demodulator per 5.20
2	66	BI	908A	50DF		48 ±2	Replace CP69
3	69	SP	908A	500 DF	Ground TP G, on CP, CP64; Continue dotting.	9.5 ±2	Replace CP69
4	69	RESET	908A	50DF		48 ±3	Replace CP69
5	69	SET	908A	50DF		48 ±3	Replace CP69
6	70A-70F	SR	908A	50DF	Remove ground on TP G, CP64. Continue dotting.	6 ±2	Replace CP70
7	70A-70F	RR	908A	50DF		6 ±2	Replace CP70
8	70A-70F	E	908A	BUFFER		Lamp flashes	Replace CP70

E. Test of Sync Loss Indicator

5.38 The tests of the sync loss indicator are most readily performed as follows: Ground test point T on CP65 briefly several times while receiving dotting and the 906A is in the sync-loss-counting mode. (Operate relay SL by DIST CTR switch in SUPV SYNC position; also operate DTA-SUPV key to SUPV position and operate and hold DATA READ.) For each grounding, the SYN lamp should go off and the counter should increment one count. If neither lamp nor counter operates, utilize the 908A in the TRL (+) mode in test point K on CP62; the lamp should go off for each grounding of T. If it is continually on or continually off, replace CP64 and CP69. If the 908A lamp flashes as required, replace CP62.

5.39 If the SYN lamp operates but counter does not operate, replace CP62. If trouble still exists, verify that SYG lead is grounded, and trace wiring through CNT relay to the counter. If counter operates but the lamp does not, replace the SYN lamp and verify −24 volts exist in lamp socket.

SIGNAL GENERATOR

A. Circuit Package 1—Oscillator Output Amplitude

5.40 The tests below are made with the transistorized voltmeter (TVM). All voltages are with respect to ground.

5.41 On the 20A testboard, operate the GEN SPEED switch to 95.5. Release and operate DMO switch. The TVM should read at least 2.5 volts ac. Check to see that the GS1 and 3 relays are both unoperated.

5.42 Operate the GEN SPEED switch to 110. Release and operate DMO switch. The meter should read at least 2.5 volts ac. The GS1 meter should read at least 2.5 volts ac. The GS1 relay should be operated, the GS3 relay unoperated.

5.43 Operate the GEN SPEED switch to 150. Release and operate DMO switch. The meter should read at least 2.5 volts ac. The GS1 relay should be unoperated, the GS3 relay operated.

5.44 Operate the GEN SPEED switch to 200. Release and operate DMO switch. The meter should read at least 2.5 volts ac. Both the GS1 and GS3 relays should be operated.

5.45 Under normal conditions, the voltmeter will read about 4 volts ac. If the output is below 2.5 volts ac on any bit rate and the normal +12 volts dc supply voltage is present, CP1 is considered inoperative.

B. Circuit Package 2—Oscillator Countdown Output

5.46 Return the GEN SPEED switch to 110. Release and operate DMO switch.

5.47 Assuming CP1 is working, measure the ac voltage on test points CLK and CHK on CP2. These voltages should measure between 2.5 and 4 volts ac. The nominal voltage is about 3 volts.

5.48 If there is no output, go to terminal 17 on the back of CP2. This is the same point as test point OSC 0 on CP1 and should measure at least 2.5 volts ac.

5.49 Apply +12 volts ac and ground to the appropriate terminals of the 908A logic circuit test set. Put the slide switch in the DF position. Connect the input terminal to test points CLK and CHK in turn. The light on the 908A should come on in both the TRL (−) and TRL (+) positions of the rotary switch.

5.50 All the above tests should be positive for CP2 to be considered good.

C. Circuit Package 2—Clock Frequencies

5.51 This section is used to measure accurately the clock frequencies. It is assumed that tests for 5.40 through 5.49 have been carried out. Unless it is suspected that the oscillator frequencies are off, these tests can be omitted at this point. They should be performed if 5.63 through 5.67 give negative results.

5.52 Place a lead from test point CLK on CP2 to test point R on CP8. Plug the LD cord in the R jack. The balance of the frequency test is carried out at the 20A toll testboard.

5.53 Operate FRR-FRS CHK key to FRS CHK.

5.54 Operate the GEN SPEED switch to 200. Release and operate the DMO switch. Place the TIME SECONDS (T-S) switch on the elect-

ronic counter to 1.0. The count should be between 2411 and 2389. Turn the T-S switch to 10^{-2}. The count should be between 1022 and 1025.

5.55 Operate the GEN SPEED switch to 150. Release and operate the DMO switch. Place the T-S switch to 1.0. The counter should read between 6791 and 6809. Place the T-S switch to 10^{-2}. The counter should read between 7678 and 7681.

5.56 Operate the GEN SPEED switch to 110. Release and operate the DMO switch. Place the T-S switch to 1.0 The counter should read between 6313 and 6327. Place the T-S switch to 10^{-2}. The counter should read between 5630 and 5633.

5.57 Operate the GEN SPEED switch to 95.5. Release and operate the DMO switch. Place the T-S switch to 1.0. The counter should read between 8890 and 8902. Place the T-S switch to 10^{-2}. The counter should read between 4888 and 4891.

D. Circuit Package 3—6-Stage Binary Counter Outputs

5.58 In order to perform these tests, CP1 and CP2 have to be in operating condition.

5.59 Keep the GEN SPEED switch at 110. With the TVM measure the ac voltage on test points C5 and C6. Each should be between 2.5 and 4 volts ac.

5.60 Apply power to the 908A, DF position. Turn the rotary switch to 5000 CPS. Go to test point C2; the meter should read between 34 and 37 (nominal 35.2 corresponds to 3520 cps).

5.61 Go to test point C5. Turn the rotary switch to 500 CPS; the meter should read between 42.5 and 45.5.

5.62 Repeat above for C6. In the 500 CPS position, the meter should read between 20.5 and 23.5.

5.63 All the above conditions must be met.

E. Circuit Package 4—Output Circuits

Dotting Output

5.64 Keep the GEN SPEED switch at 110. Place the GEN MODE switch in the DOT position at the 20A toll testboard.

5.65 Go to test point C1 on CP4. Switch the 908A to the DF position, rotary switch to 500 CPS. The meter should read between 9.5 and 12.5. Switch to BIAS (−); the meter should read 0.

5.66 Go to test point C1 on CP5. Place the 908A on 500 CPS. The meter should read between 4 and 7. Switch to BIAS (+); the meter should read less than 1.5. If it does not, check that the B and C relays are operated and the A relay is unoperated. This portion of CP5 must be operating before the rest of CP4 can be checked.

5.67 Place the 908A in the DF position, rotary switch at 500 CPS. Go to test point G1 on CP4. The meter should read between 4 and 7.

5.68 With the 908A in the DF position, rotary switch at 500 CPS, go to test point G2 on CP4. The meter should read between 9.5 and 12.5. Switch to BIAS (−). The meter should read between 36 and 39.

5.69 Go to test point G3. Put the 908A in the BIAS (−) position. The meter should read between 5 and 8.

5.70 Go to test point G4. Put the 908A in the BIAS (+) position. The meter should read between 5 and 8.

Random Output

5.71 With the GEN SPEED switch at 110, turn the GEN MODE switch to the RDM position on the 20A testboard. On CP7, connect a lead from test point G5 to ground. With the 908A, go to test point G6 on CP4. The light on the 908A should come on in the TRL (−) position and stay dark in TRL (+) position. Leave the 908A connected to G6. Unground test point G5 on CP7 and ground test point G6 on CP7. Switch the 908A to 50 CPS. The meter should read between 8.5 and 11.5

5.72 Go to test point G7 on CP4. Leave the 908A on 50 CPS. The meter should read between 8.5 and 11.5. Switch to BIAS (−). The meter

should read between 30.5 and 33.5. Remove the ground from test point G6 on CP7. Switch the 908A to 50 CPS. The meter should swing between 25 and 30. Check that the A, B, and C relays are all operated.

F. Circuit Package 5—Stop-Start Signals

5.73 With the GEN SPEED switch at 110, place the GEN MODE switch on RDM at the 20A toll testboard.

5.74 Before testing CP5, the binary on CP4 must be checked. Set the 908A on DF, rotary switch to 500 CPS. Go to test point C1 on CP4. The meter should read between 9.5 and 12.5. This test can be deleted if CP4 has been checked.

5.75 Set the 908A on 50 CPS. Go to test point G1 on CP5. The meter should indicate between 8.5 and 11.5. Switch to BIAS (−). The meter should indicate between 39.5 and 42.5.

5.76 Go to test point G2. In the BIAS (−) position, the meter should indicate between 30.5 and 33.5. Switch to 50 CPS. The meter should read between 8.5 and 11.5.

5.77 If the above conditions are not met, make sure the A and B relays have both operated. All tests have to be positive for CP5 to be considered good.

G. Circuit Packages 6 and 7—Quasi-Random Bit Sequence

5.78 On the 20A toll testboard, put the GEN SPEED switch to 110. If this is a change in position, release and operate DMO switch.

5.79 These boards can be tested together as a unit. It is assumed that CP5 is operating properly. Ground test points G1 and G2 on CP5. Set the 908A on DF, MP (+). Connect the 908A to test point G2 on CP7. The light on the 908A should flash on 24 or 25 times in 15 seconds. Connect the 908A to test point G6 on CP7. Set the rotary switch to 50 CPS. The meter reading should fluctuate around 25.

5.80 If either of the above tests fails, there is trouble on either CP6 or CP7.

5.81 Remove ground from test points G1 and G2 on CP5. Connect the 908A to test point G1 on CP7. Set the switch to 500 CPS. The meter should read between 6.5 and 9.5. Set the switch to BIAS (−). The meter should read between 12 and 15. Failure of the above two tests indicates trouble on CP7.

5.82 Ground test points SR1 through SR6 on CP6. With the 908A check test points G2, G3, and G4 on CP7. The light should come on in the TRL (−) position and stay dark in the TRL (+) position. Failure of this test indicates trouble on CP7, unless terminals 17, 6, 16, 5, 4, 15, and 8 on the back of CP6 are not at least +4 volts dc. Check these with a voltmeter. Low voltage indicates trouble on CP6.

5.83 If the previous section tested satisfactorily, check test point G5 on CP7. The light should come on in TRL (+) position. At test point G6 the light should come on in the TRL (−) position. Failure indicates trouble on CP7.

5.84 Remove ground from SR1 through SR5 test points. Ground terminal 15 on the back of CP6 and test point SR6 on CP6. Place the 908A on TRL (+) and check G4 on CP7; the light should come on. Check G5 and G3; the light should come on in the TRL (−) position. If this test fails, check voltages on the back of CP6; terminals 4 and 8 should be at least +4 volts dc. Failure to meet these voltage requirements indicates trouble on CP6; otherwise the trouble is on CP7.

5.85 Remove ground leads. Ground test point SR5 on CP6 and terminal 8 on the back of CP6. Check test point G3 on CP7 with the 908A. The light should come on in the TRL (+) position. If not, there is trouble on CP7. Check G4 and G5 on CP7. The light on the 908A should come on in the TRL (−) position. If not, there is trouble on CP7 unless the voltage on terminals 15 and 14 is less than 4 volts dc. Assuming everything is all right down to this point, with the same setup check G6 on CP7. The light should come on in the TRL (+) position.

5.86 If all these tests except the flashing light test (5.79) give positive results, assume that the trouble is on CP6.

DISTORTION MEASURING CIRCUIT — TABLE H

5.87 The over-all tests for the 906A data distortion test equipment can localize a trouble to the measuring circuit. The test or combination of tests which fail leads one to suspect various parts of the circuit as outlined below. The statement "Replace CP—" means that the trouble may be in the connectors or the wiring behind the bay running to the particplar circuit package in question.

5.88 *Calibration Adjustment Fails*: If the measuring circuit cannot be calibrated, check cards CP11A-B, CP21, CP22, and CP23. Also check the HI CAL and LO CAL relay circuit and the circuitry on the panel. For example, the meter might read backwards regardless of the various settings of the knobs and HI CAL — LO CAL switch. This trouble might be due to the zener diode on the meter circuit which may have opened. In this case, −48 volts would be applied to the meter through approximately 2500 ohms.

5.89 *Bias (+) and/or Bias (−) Readings Fail*: If the circuit can be calibrated, try to get a reading (using either + bias or − bias) with the BIAS-DTA-SUPV key in the SUPV position. If the correct readings are obtained, examine the leads running to the BD relay from the various card. If the circuit does not work, begin performing the tests with CP15.

5.90 *Circuit Does Not Get in Sync with a Random Input and BIAS-DTA-SUPV Key in DTA Position*: If the circuit can be calibrated, and the + bias and − bias work together with the supv mode, check gate Q17 CP12; flip-flop Q1, Q2 CP12; gate Q8 CP15; all of CP13, CP14, and CP16.

5.91 *Smoothness of Reading Test Fails*: Check the four CP11A-D cards as well as CP21, 22, and 23.

5.92 *Single Hit (Peak Reading) Test Fails*: If all the tests up to this point have worked, the trouble should be in the charging path of the capacitor C1 CP22 (41E5). Ground break contact number 2 of the BD relay and repeat the single hit test for hits over 40 per cent. These should be registered on the meter. Note that the meter may not be discharged under these conditions. If this fails, replace CP22; if the test passes, replace CP23.

5.93 *No Correlation Between Meter and Hit Counter*: If the tests to now have checked out, the trouble must be with the relay circuitry (4, A-G, 1), cards CP17, 18, 19, 20, or the panel circuit. Relays D1, D1-1, D2, and D3 must be operated in accordance with the following:

DIST CTR	Relays Operated
4	None
8	D1, D1-1
12	D3
16	D1, D1-1, D3
20	D2

Note: The cards may not be seated properly in their connectors.

5.94 *Burst of Five Test Fails*: The failure of this test indicates that CP19 is bad if the previous tests check out. This is the circuit that holds the number of distortion hits that occurred and and feeds them out slowly to the message register.

5.95 If the burst of five test works but switching to the DTA mode does not produce single hits as called for or the single hits do not cease when the distortion is reduced, check the PS relay and if found to be in order, replace CP18.

5.96 In case of suspected trouble in the signal generator, this section gives the procedure for localizing the fault to a particular board.

5.97 The equipment required to perform the tests are the WECo 908A logic circuit test set and a Simpson 269 VOM. If a 269 is not available and another instrument must be used, place a 0.5-uf capacitor in series with the test lead.

A. Measuring Frequency with the EPUT Meter

5.98 The following examples should clarify the use of the EPUT meter.

Ex: 48.896kc

(a) Set TIME-SECONDS knob on 2. Read 4889 ±1 on meter.

(b) Set TIME-SECONDS knob on 10^{-1}. Read 8896 ±1 on meter.

5.99 Some positive and negative pulses to be checked with the 908A are too narrow (short duration) for it. To overcome this difficulty, these pulses must be widened by the calibrator circuit. When the instructions listed under input to 908A stipulate the use of positive pulse procedure or negative pulse procedure, do the following:

(a) Positive Pulses

(1) Ground TP5 N CP8.

(2) Ground TP4 FF CP8.

(3) Operate FREQ-OFF-TST on calibrator panel to FREQ.

(4) Connect signal to be measured on TP6 MP+ CP8.

(5) Connect input of 908A test circuit to TP5 DI on calibrator panel.

(b) Negative Pulses

(1) Ground TP2 G2 CP8.

(2) Ground TP4 FF CP8.

(3) Operate FREQ-OFF-TST on calibrator panel to FREQ.

(4) Connect signal to be measured on TP7 MP− CP8.

(5) Connect input of 908A test circuit to TP5 DI on calibrator panel.

B. Description of Tests

5.100 *CP*15: The tests in this section detect the required outputs of the various gates and monopulsers in the transition detector due to a known input.

5.101 *CP*11: The first five tests verify the presence of a clock signal and verify the normal operation of those counter stages on CP11. The remaining tests check out the register gates and translators and distortion registers.

5.102 *CP*13: The first, second, and fourth tests check out those binary counters on CP13 (as well as the high fanout gates). The third test checks out the monopulser on CP13.

5.103 *CP*14: The first test verifies operation of the binary counter stages on CP14. The last three tests examine the three AND gates on that board.

5.104 *CP*17: The test insures that the reset pulse for the last eleven stages occurs as it should.

5.105 *CP*12: The first test checks the presence of the gate pulse for the register gates and translators. The second test looks for the reset pulse for the distortion registers. The third test checks the inverter Q17 CP12. The fourth test checks the register which blocks the count feeding the main binary counter.

5.106 *CP*16: This test checks the operation of the sync register and frame sync counter circuit. A random word is fed to the measuring circuit to see if the circuit gets in sync.

5.107 *CP*21: The digital to analog converter is checked by fixing the input and measuring the output voltage.

5.108 *CP*22: The first test checks the out-syn lamp driver circuit as well as the lamp driver. The second test checks the start-stop read out inhibit circuit. The third test checks the meter circuit.

5.109 *CP*23: The test checks the discharge circuit.

5.110 *CP*17: The first five tests check the operation of the threshold circuit and associated relays. Tests six and seven localize the trouble to boards CP17 and CP18. Test eight checks the output gate of the threshold circuit. Test nine checks a pulse stretching monopulser.

5.111 *CP*19 *and* 20: The first three tests check the operation of the buffer counter. The remaining tests work in conjunction with the overall checks to localize the trouble to CP19 or CP20.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
NOTE: Before each step, reset all controls to normal.								
1	*CP15* Set the GEN MODE switch to DOT, the GEN SPEED switch to 200 and the TST DMO key to DMO.	TP2 DI CP15	500 cps	DF	10.0 ±1.0	—	Proceed to the next test.	Either the card is bad or input is not present.
2	Same as above.	TP5 MP1 CP15 Use positive pulse procedure.	500 cps	DF	10.0 ±1.0	—	Proceed to the next test.	Replace CP15.
3	Same as above.	TP6 MP2 CP15 Use positive pulse procedure.	500 cps	DF	10.0 ±1.0	—	Proceed to the next test.	Replace CP15.
4	Same as above.	TP4 G2 CP15 Use negative pulse procedure.	500 cps	DF	10.0 ±1.0	—	Proceed to the next test.	Replace CP15.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
5	CP15 (Cont.) (a) Same as above. (b) Ground TP2 G3 CP14. (c) Set DMS key to BIAS.	TP7 MP3 CP15	500 cps	DF	10.0 ±1.0	—	Proceed to the next test.	Replace CP15
6	(a) Block operated SEND SUPV key. (b) Set CHAN SEL switch to SUPV. (c) Operate DATA SUPV key to SUPV. (d) Block DATA READ key. (e) Set GEN MODE switch to DOT. (f) Set GEN SPEED 200 bits/sec. (g) Release and set TST-DMO to DMO.	TP2 DI CP15	500 cps	DF	10.0 ±1.0	—	Proceed to the next test.	Connect input of 908A to TP $\overline{\text{BID}}$ CP62 and repeat this. If test passes, CP15 is bad. Be sure that the SSC relay is operated.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
7	CP15 (Cont) (a) Set the GEN MODE switch to RDM and the GEN SPEED to 200. (b) Release and Set TST-DMO to DMO.	TP7 MP3 CP15 Use positive pulse procedure.	50	DF	18.2 ±1.0	On each time key goes from BIAS to DTA.	Proceed to the next test.	Connect input of 908A to TP2 G3 CP14 and repeat test. If test passes, CP15 is bad.
8	(a) Set the GEN MODE switch to MK. (b) Ground TP3 R2 CP12. (c) Ground TP5 MP. (d) Operate key BIAS DTA-SUPV from BIAS to DTA and back repeatedly.	TP7 MP3 CP15 Use positive pulse procedure.	MP(+)	DF	—	On each time key goes from BIAS to DTA.	Proceed to the next test.	Connect input of 908A to 10 common of BD relay. If Step 8 again fails, replace CP12. Repeat Step 8 with 908A input connected to TP8 MP1 CP16. If test fails, replace CP16. If above tests pass, replace CP15.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Connections to EPUT Meter	Measure	Upon Failure
1	*CP11* (a) Set GEN SPEED to 95.5. (b) Operate BIAS DTA SUPV key to BIAS. (c) Ground TP7 MP3 CP15. (d) Ground TP8 I2 and TP7 I1 both on CP17. (e) Release and operate TST-DMO to DMO.	Connect TP1 G1 CP17 to TP1 R CP8. Plug LD cord into R jack and operate FRS CHK key.	48.896 KC on EPUT meter	Replace CP17.
2	Same as 1	Connect TP2 C2 CP11A to TP1 R CP8. Plug LD cord into R jack and operate FRS CHK key.	12.224 KC on EPUT meter	Replace CP11A.

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
3	Same as 1	TP2 C2 CP11B	5000 CPS	DF	30.56 ±1.0	—	Continue to next test.	Replace CP11B.
4	Same as 1	TP2 C2 CP11C	2500 CPS	DF	15.3 ±1.0	—	Continue to next test.	Replace CP11C.
5	Same as 1	TP2 C2 CP11D	500 CPS	DF	19.1 ±1.0	—	Continue to next test.	Replace CP11D.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Connections To EPUT Meter	Measure	Upon Failure
6	*CP11 (Cont)* (a) Same as 1 (b) Ground TP3 I1 CP13. (c) Ground TP7 I0 CP12.	Connect TP3 G1 CP11A to TP1 R CP8. Plug LD cord into R jack and operate FRS CHK key.	24.448 KC on EPUT meter	Replace CP11A.
7	Same as Step 6	Connect TP3 G1 CP11B to TP1 R CP8. Plug LD cord into R jack and operate FRS CHK key.	12.224 KC on EPUT meter	Replace CP11A.
8	Same as Step 6	Connect TP5 G3 CP11A to TP1 R CP8. Plug LD cord into R jack and operate FRS CHK key.	6.112 KC on EPUT meter	Replace CP11B.

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
9	Same as above.	TP5 G3 CP11B	5000 CPS	DF	30.56 ±1.0	—	Continue to next test.	Replace CP11B.
10	Same as above.	TP3 G1 CP11C	2500 CPS	DF	30.56 ±1.0	—	Continue to next test.	Replace CP11C.
11	Same as above.	TP5 G3 CP11C	2500 CPS	DF	15.3 ±1.0	—	Continue to next test.	Replace CP11C.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
12	Same as above	TP3 G1 CP11D	500 CPS	DF	38.2 ±1.0	—	Continue to next test.	Replace CP11D.
13	Same as above	TP5 G3 CP11D	500 CPS	DF	19.1 ±1.0	—	Continue to next test.	Replace CP11D.
14	(a) Same as 1 (b) Ground TP 4 I2. (c) Ground TP7 I0 CP12.	Repeat Steps 6 through 13 making the following substitutions: TP4 G2 instead of TP3 G1 and TP6 G4 instead of TP5 G3.						
15	Ground 12 common CAL relay. Ground G2 (TP 6) CP12 and ground momentarily all eight test points (DIG1 - DIG8) on CP21.	DIG1 CP21 and DIG2 CP21	TRL (−)	—	—	ON	Continue to Test 17.	Go to Test 16.
16	Ground TP6 G2 CP12.	TP7 I0 CP12	TRL (+)	—	—	ON	Replace CP11A	Replace CP12 and repeat Test 15.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
17	*CP11 (Cont)* Same as above	DIG3 CP21 and DIG4 CP21	TRL (−)	—	—	ON	Continue to next test.	Replace CP11B.
18	Same as above	DIG5 CP21 and DIG6 CP21	TRL (−)	—	—	ON	Continue to next test.	Replace CP11C.
19	Same as above	DIG7 CP21 and DIG8 CP21	TRL (−)	—	—	ON	Continue to next test.	Replace CP11D.
20	(a) Ground TP6 G2 CP12. (b) Operate and release LO CAL switch on panel.	DIG1 CP21 and DIG2 CP21	TRL (+)	—	—	ON	Continue to next test.	Replace CP11A.
21	Same as above	DIG3 CP21 and DIG4 CP21	TRL (+)	—	—	ON	Continue to next test.	Replace CP11B.
22	Same as above	DIG5 CP21 and DIG6 CP21	TRL (+)	—	—	ON	Continue to next test.	Replace CP11C.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
23	*CP11 (Cont)* Same as above	DIG7 CP21 and DIG8 CP21	TRL (+)	—	—	ON	Continue to next test.	Replace CP11D.
1	*CP13* (a) Set GEN SPEED to 95.5. (b) Operate BIAS-DTA-SUPV to BIAS. (c) Ground TP7 MP3 CP15. (d) Ground TP8 I2 and TP7 I1 both on CP17.	TP3 I1 CP13	500	DF	9.5 ±1.0	—	Continue to next test.	Replace CP13 if CPS 11D has passed.
2	Same as above	TP4 I2 CP13	500	DF	9.5 ±1.0	—	Continue to next test.	Replace CP13 if CPS 11D has passed.
3	Same as above	TP5 MP1 CP13	500	DF	9.5 ±1.0	—	Continue to next test.	Replace CP13 if CPS 11D has passed.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
4	*CP13 (Cont)* Same as above	TP2 C2 CP13	500	DF	4.77 ±1.0	—	Continue to next test.	Replace CP13.
1	(a) Set GEN SPEED to 95.5. (b) Operate BIAS-DTA-SUPV key to BIAS. (c) Ground TP7 MP3 CP15. (d) Ground TP8 I2 and TP7 I1 both on CP17. (e) Release and operate TST-DMO to DMO.	TP5 C5 CP14	50	DF	5.5 ±1.0	—	Continue to next test.	Replace CP14.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
2	*CP14 (Cont)* (a) Same as above. (b) Ground TP8 G3 CP12. (c) Ground TP2 D1 CP15.	TP6 G5 CP14	50	DF	11 ±1.0	—	Continue to next test.	Replace CP14.
3	Same as Step 2	TP4 G4 CP14	50	DF	5.5 ±1.0	—	Continue to next test.	Replace CP14.
4	(a) Ground TP4 G2 CP15. (b) Same as Step 1	G3 TP2	50	DF	5.5 ±1.0	—	Continue to next test.	Replace CP14.
1	*Part of CP17* (a) Operate BIAS-DTA-SUPV key to BIAS. (b) Set GEN SPEED to 200. (c) Set GEN MODE switch to DOT. (d) Release and operate TST-DMO to DMO.	TP7 I1 CP17	500	DF	10.0 ±1.0	—	Continue to next test.	Replace CP17.

TABLE O (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
1	*CP12* (a) Set GEN SPEED to 200. (b) Operate BIAS-DTA-SUPV to BIAS (c) Set GEN MODE switch to DOT. (d) Ground TP1 R1 CP22.	TP7 IO CP12 Use negative pulse procedure.	500	DF	10.0 ±1.0	—	Continue to next test.	Replace CP12.
2	Same as Step 1	2 COMMON LOCAL RELAY Use positive pulse procedure.	500	DF	10.0 ±1.0	—	Continue to next test.	Replace CP12.
3	Same as Step 1	TP 8 G3 CP12 Use negative pulse procedure.	500	DF	20.0 ±1.0	—	Continue to next test.	Replace CP12.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
4	*CP12* (Cont) Set GEN MODE SWITCH on DOT. Set BIAS-DTA-SUPV key on DTA.	TP3 R2 CP12	MP (—)	—	—	Flash on and off.	Continue to next test.	Replace CP12.
1	*CP16* (a) Set GEN MODE on RDM. (b) Set BIAS-DTA-SUPV key on DTA.	TP7 R1 CP16	TRL (+)	—	—	ON	Continue to next test.	Replace CP16.
2	(a) Set GEN MODE on DOT. (b) Set BIAS-DTA-SUPV key on DTA.	TP7 R1 CP16	TRL (—)	—	—	ON	Continue to next test.	Replace CP16.
1	*CP21* Operate LOCAL switch on panel. Measure approximately -12 volts on TP2 ANAL CP22. Ground TP8 DIG8 CP21. Measure -2 volts on TP2 ANAL. Ground also TP7 DIG7 CP21 and measure +3 volts. Ground also TP6 DIG6 CP21 and measure +5.5 volts. Similarly TP5 DIG5 +6.75 volts, TP4 DIG4 +7.38 volts, TP3 DIG3 +7.69 volts, TP2 DIG2 +7.84 volts, TP1 DIG1 +7.91 volts. These measurements need not be exact. If test fails, check LO CAL relay circuit wiring and if it is all right, replace CP21.							

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
	CP22							
1	Ground TP7 R1 CP16 with key BIAS-DTA-SUPV in the DTA position and the GEN MODE on MK. The out of sync lamp on the panel should go on. When the ground on TP7 R1 CP16 is removed and BIAS-DTA-SUPV key moved to SUPV and the SYN RESET button is depressed on the panel, the out of sync lamp should go out and stay out when button is released. If test fails, replace CP22.							
2	(a) Set GEN MODE on RDM (b) Set BIAS-DTA-SUPV key on DTA.	TP5 R1 CP22	50	DF	18.2 ±1.0	—	Continue to next test.	Replace CP22.
3	It should be possible to calibrate the meter. If not, check the HI CAL relay circuit and meter circuit on panel and if all right, pull CP23 from its connector and try calibration. If this should not work, replace CP22.							
	CP23							
1	If meter needle decays very slowly, CP23 is not working and must be replaced. CP23 may also short out the capacitor.							
	CP17							
	(a) Set GEN SPEED to 200.	TP1 R1 CP17	BIAS (−)	—	42 ±1.0	—	Continue to next test.	
1	(b) Operate BIAS-DTA-SUPV key to BIAS.			—		—	Continue to next test.	
	(c) Ground MP3 TP7.			—		—	Continue to next test.	
	(d) Set DIST CTR to 4%.			—		—	Continue to next test.	

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
	CP17 (Cont)							
2	Same as Step 1 except set DIST CTR to 8%.	TP5 R1 CP17	BIAS (−)	—	34 ±1.0	—	Continue to next test.	
3	Same as Step 1 except set DIST CTR to 12%.	TP5 R1 CP17	BIAS (−)	—	26 ±1.0	—	Continue to next test.	
4	Same as Step 1 except set DIST CTR to 16%.	TP5 R1 CP17	BIAS (−)	—	18 ±1.0	—	Continue to next test.	
5	Same as Step 1 except set DIST CTR to 20%.	TP5 R1 CP17	BIAS (−)	—	10 ±1.0	—	Skip steps 6 and 7.	

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Connections To EPUT Meter	Measure	Upon Failure
6	*CP17* (Cont) (a) Ground TP3 I1 CP13. (b) Set DIST CTR at 8%. (c) Ground TP2 C2 CP11A. (d) Set GEN SPEED switch at 200. (e) Ground TP2 C2 CP11B and TP2 C2 CP11C. (f) Set BIAS-DTA-SUPV key to BIAS. (g) Ground TP7 MP3 CP15.	Connect TP3 G3 CP17 to TP1 R CP8. Plug LD cord into R jack and operate FRS-CHK key.	51.200 KC on EPUT meter.	Replace CP17.
7	(a) Set BIAS-DTA-SUPV key to BIAS. (b) Ground I1 TP3 CP13 TP1 and C1 CP11A.			

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
7 (Cont)	*CP17 (Cont)* (c) Set GEN MODE to DOT. (d) Ground TP2 C2 CP11B. (e) Set DIST CTR at 8% (f) Ground repeatedly TP2 C2 CP11C.	TP3 G3 CP17.	TRL (+)	DF	Flash when ground is applied.	—	Check D1, D2, D3, relay circuitry. Replace CP18.	Replace CP17.
8	(a) Ground TP1 R1 CP22 and TP5 R1 CP17. (b) Set GEN MODE on DOT. (c) Set GEN SPEED on 200.	TP4 M1 CP18	500	DF	20 ±1.0	—	Continue.	Replace CP17.
9	(a) Same as above (b) BIAS-DTA-SUPV key must be in DTA POSITION.	ADD TP4 CP19	500	DF	20	—	Continue.	Replace CP18.

TABLE H — OVER-ALL TESTS FOR 906A DATA DISTORTION TEST EQUIPMENT (Cont)

Step	Test Conditions	Input To 908A	908A Settings		908A Requirements		Actions	
			Rotary SW	DPDT SW	Meter Reading	Lamp Condition	Upon Success	Upon Failure
1	*CP19 & 20* (a) Ground TP1 R1 CP22 TP5 and R1 CP17. (b) Set GEN MODE ON DOT. (c) Set GEN SPEED on 200. (d) Ground TP5 SUB CP19.	CNT1 TP3 CP19	500	DF	20	—	Continue.	Replace CP19.
2	Same as above	TP2 CNT2 CP19	500	DF	10	—	Continue.	Replace CP19.
3	Same as above	TP2 CNT3 CP19	500	DF	5	—	Continue.	Replace CP19.
4	(a) Same as Step 1 (b) Ground TP4 ADD CP19.	The OVFL lamp which should be on should go out and stay out when the RST-ST key on the panel is depressed. If not, check key and lamp circuit and replace CP20 if necessary.						
5	Use the test circuit provided with the 906A. If the burst of 5 hits is not counted properly, replace CP19. If no counts at all are registered, check the CNT relay circuit and the message register. Then remove the connections to terminals 8 and 9 of the timer in order to check continuity between these terminals when the timer is on and off. Refer to Sheet B4 location H6-8. If counts are still not registered, replace CP20.							