

# Axxia® Communication Processor AXM5500 Family

## Power-Efficient ARM Multicore for Mobile Networking Applications



### Features

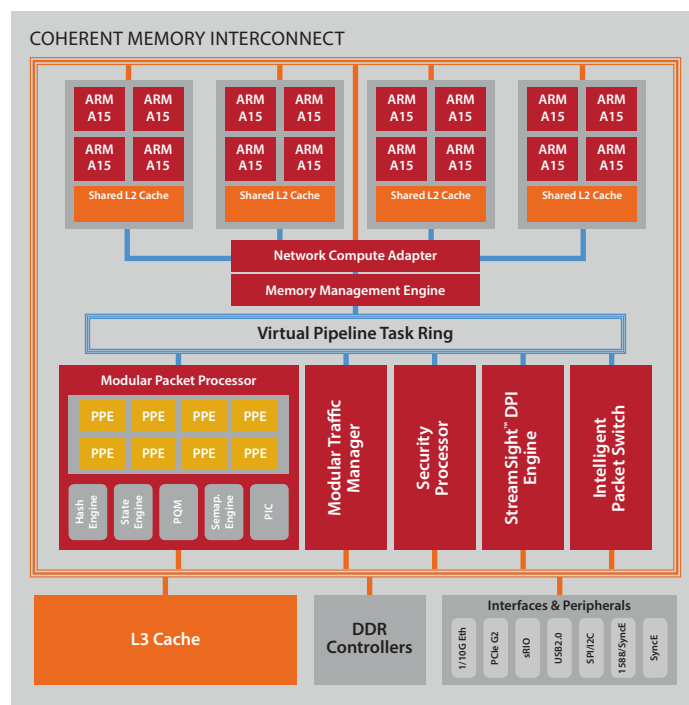
- ARM® Processor Compute Complex
  - Up to 16 ARM® Cortex™-A15 processors
  - CPU clock speed up to 1.6GHz
  - 32KB I / 32KB D L1 cache per core
  - 2MB with ECC shared L2 cache per quad core cluster
- System Communication
  - ARM® CoreLink™ CCN-504 Cache Coherent Network is QoS-aware and optimized for networking workloads
  - Avago Virtual Pipeline™ technology enables efficient autonomous packet processing and deterministic performance
- Memory Subsystem
  - 8MB with ECC non-inclusive L3 cache
  - Dual 72-bit DDR3 system memory controllers
  - Dual 9-bit DDR3 classification memory controllers
- Acceleration Engines
  - Packet Processor (Up to 50Gb/s)
  - Security Protocol Processor (Up to 25Gb/s)
  - StreamSight™ DPI Engine (Up to 7Gb/s)
  - Traffic Manager (7 levels of hierarchy)
- High-Capacity Ethernet Switching
  - Non-blocking L2 switching (Up to 160Gb/s)
- Secure System Complex
  - Including secure boot, secure parameter storage, secure long-term data storage and boundary interface protection features
- Flexible SerDes Interfaces
  - Up to 16x 10GbE interfaces supported by XFI, SFI, and 10GBASE-KR
  - Up to 8x 1GbE interfaces supported by 2x QSGMII
  - Up to 20x 1GbE or 2.5GbE interfaces supported by SGMII or overlocked SGMII
  - 2x PCIe Gen2 controllers supporting x4, x2 or x1 configurations
  - 2x sRIO V2.2 controllers supporting x2 or x1 configurations
  - IEEE 1588 and SyncE support on all Ethernet interfaces
- Software Development Environment
  - Eclipse-based Axxia Software Environment (ASE) provides comprehensive tool-suite for rapid code development
  - Production-quality Axxia Development Kits (ADK) provide protocol acceleration for mobile networking applications
- Technology
  - 28nm process technology
- Package
  - 1680-ball FCBGA, 42.5-mm x 42.5-mm

### Overview

The Axxia® Communication Processor AXM5500 product family is designed to accelerate the performance, power efficiency and integration demands of next-generation mobile networking equipment. Combining Avago's networking expertise, specialized acceleration engines and Virtual Pipeline™ technology with ARM's power-efficient Cortex™-A15 processors and CoreLink™ CCN-504 Cache Coherent Network interconnect on a leading process technology, the AXM5500 solution enables more capable and intelligent mobile networking equipment, including multi-radio base stations, mobile backhaul equipment and gateways.

The AXM5500 product family achieves its performance efficiency by providing a flexible combination of general-purpose processors and specialized packet-processing acceleration engines. These processors and engines use Virtual Pipeline technology, a message-passing control path, to efficiently and autonomously process packets. This approach provides system designers with the ability to define packet processing flows using multiple combinations of acceleration engines and CPUs to meet a wide range of application requirements. In mobile network applications wireless transport processing can be implemented in the Virtual Pipeline and acceleration engines, allowing for greater performance and power efficiencies.

The AXM5500 product family also integrates high-capacity Ethernet switching to drive even greater levels of power, board space and bill of material (BOM) cost savings. Supporting up to 16 10GbE interfaces, the AXM5500 can support a variety of intra-board, intra-chassis and subtending connectivity topologies with a single SoC.



AXM5500 Architecture Diagram

### AXM5500 Configuration Table

Features	AXM5516	AXM5512	AXM5508
CPU Cores	16x ARM® A15 @ up to 1.6GHz	12x ARM® A15 @ up to 1.6GHz	8x ARM® A15 @ up to 1.6GHz
L2 Cache	8MB Total 2MB per Cluster	6MB Total 2MB per Clusterer	4MB Total 2MB per Cluster
L3 Cache	8MB Total	8MB Total	4MB Total
System Memory	2x 72b DDR3 at up to 1866MT/s	2x 72b DDR3 at up to 1866MT/s	1x 72b DDR3 at up to 1866MT/s
Classification Memory	2x 9b DDR3 at up to 1333MT/s	2x 9b DDR3 at up to 1333MT/s	2x 9b DDR3 at up to 1333MT/s
Packet Processing	50Gbps	50Gbps	35Gbps
Security Engine	25Gbps IPSec	25Gbps IPSec	10Gbps IPSec
Traffic Manager	7 levels of hierarchy	7 levels of hierarchy	7 levels of hierarchy
StreamSight™ DPI Engine	7Gbps RegEx	7Gbps RegEx	7Gbps RegEx
Ethernet Switching	160Gb/s	160Gb/s	120Gb/s
Interfaces	Ethernet: - Up to 16x 10GbE (XFI, SFI, KR) - Up to 8x GbE via QSGMII - Up to 20x GbE via SGMII 2x PCIe Gen 2/1, x8 lanes 2x sRIO v2.2 USB2.0	Ethernet: - Up to 16x 10GbE (XFI, SFI, KR) - Up to 8x GbE via QSGMII - Up to 20x GbE via SGMII 2x PCIe Gen 2/1, x8 lanes 2x sRIO v2.2 USB2.0	Ethernet: - Up to 12x 10GbE (XFI, SFI, KR) - Up to 8x GbE via QSGMII - Up to 16x GbE via SGMII 2x PCIe Gen 2/1, x8 lanes 2x sRIO v2.2 USB2.0
SyncE, IEEE-1588	Yes	Yes	Yes
Secure System Complex	Optional	Optional	Optional
Package	1680-Ball FCBGA, 42.5-mm x 42.5-mm		

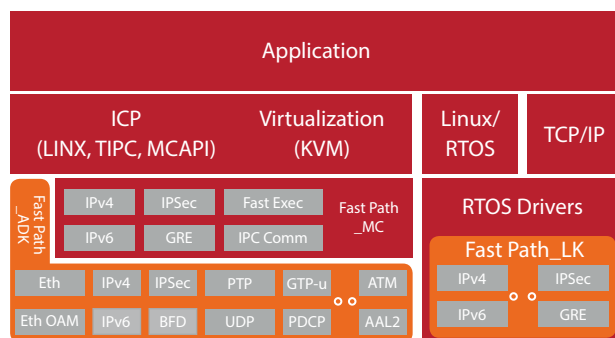
### Accelerating Software Design

The Axxia Software Environment (ASE) and Axxia Development Kit (ADK) enable rapid system development and integration. Avago provides the Axxia Software Environment for end-to-end software development, simulation and debugging. Available on Windows® and Linux® platforms, the Eclipse-based ASE includes efficient tools to seamlessly configure, compile, simulate, debug, optimize and trace an entire application including the dataplane and control planes.

The ADK is a comprehensive suite of production-ready, protocol-processing software modules for wireless infrastructure applications. Optimally balanced for power and performance across the Axxia acceleration engines and the CPU complex, the ADK includes a C-based application programming interface (API) at a functional level of abstraction and high degree of configurability for all underlying functions such as protocol termination and inter-working, traffic processing, traffic management, OA&M and security.

The Run-Time Environment (RTE) software API provides an abstracted model for each hardware accelerator and enables customers to easily add proprietary modules and corresponding functional APIs. Developed in portable, POSIX-compliant C, the RTE is available in versions compatible with Linux, VxWorks® and Enea OSE® software. Open Source Linux compatible Board Support Package (BSP) and bootloader are available for adapting to specific board configurations.

As a founding member of the Linaro Networking Group, Avago works with experts from Networking OEMs, Silicon and Software Vendors to enable virtualization and other high-performance features in Open Source Linux for the Axxia platform. Yocto compliant Open Source Linux compatible Board Support Package (BSP) and boot loader are available for adapting to specific board configurations. Commercial-grade operating systems and BSPs are available from Wind River. JTAG debuggers are available from ARM and Lauterbach.



Axxia Software Architecture Block Diagram



For more information, please visit the website at: [lsi.com](http://lsi.com)

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