82C455 VGA FLAT PANEL/CRT CONTROLLER DATA SHEET

- VGA-Compatible flat panel controller optimized for laptop computer applications.
- Supports CRT, LCD, Plasma and Electro-Luminescent displays of varying resolutions.
- Single chip implementation tightly couples to the CHIPS/250 and CHIPS/280 and interfaces with 8 and 16 bit PC bus and MCA (an interface compatible with the MicroChannel™).
- Up to 40 MHz dot clock speed for graphics and text modes.
- Can utilize an external palette DAC with up to 16 million colors.
- Provides intelligent backward compatibility to the EGA, CGA, Hercules™, and MDA on Flat Panel displays.

The 82C455 Graphics Controller provides a complete solution for implementing a Video Graphics Array-compatible controller. The 82C455 is supplied in a 144-pin PFP package. It can be used in 8 and 16-bit PC bus and in 16-bit MCA bus environments.

Display Types Supported

CGA, EGA, MDA, Multifrequency, IBM PS/2™ and other monitors can be used. The choice of flat panel displays includes EL, plasma, as well as single panel/single drive, dual panel/single drive and dual panel/double drive LCDs. Both gray scale and monochrome panels are supported; a proprietary frame rate control algorithm provides gray scale capability on monochrome panels.

CHIPS/250 and CHIPS/280 Interface

The 82C455 interfaces directly to the CHIPS/250 and CHIPS/280, providing a simple, cost-effective solution for PS/2 compatible systems. When used with one of these CHIPSets®, the 82C455 can execute FAST memory cycles at a speed greater than that normally available on the MCA bus.

Backward Compatibility

The 82C455 is compatible with IBM's EGA, CGA and MDA, in addition to offering a Hercules monochrome-graphics-compatible mode. On-chip compensation registers permit software designed for low resolution displays to utilize the entire screen area on a flat panel with higher resolution.

Hardware Support for Context Switching

Multitasking and windowing environments can be implemented easily since all internal registers of the 82C455 can be read and written.

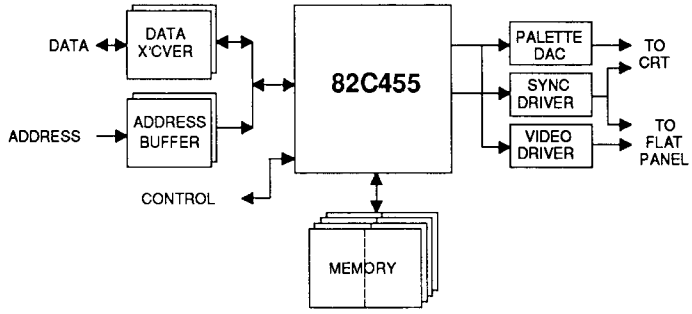


Figure 1: 82C455 System Implementation

82C455 Functional Description

The 82C455 offers a complete solution for implementing a VGA/MCGA/EGA/CGA/MDA/Hercules-compatible display system. By integrating all necessary logic the device ensures that total chip count for a VGA-compatible solution can be as low as 14 chips (includes 82C455, display memory, buffers and drivers).

Any one of a variety of CRT monitors or flat panel displays can be driven. Internal compensation registers ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software. The 256 Kbytes of display memory size is comprised of 8 64K*4 DRAMs. Display memory refresh is controlled by the 82C455; it is transparent to the CPU.

For support of multitasking environments and context switching, the entire state of the 82C455 (internal registers and latches) is readable and writeable. This feature is 100% compatible to IBM's VGA.

The 82C455 directly interfaces to 8-bit PC and PC/XT, 16-bit PC/AT and 8 or 16-bit MCA buses. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations and generation of the necessary control signals.

The 82C455 contains 16 color palette registers. It also interfaces directly to an external Inmos G171 (or compatible) color palette and D/A converter. Like the VGA, it is capable of display resolutions of 640*480 with 16 on-screen colors (internal palette) and 320*200 with 256 on-screen colors from an external palette of 256 thousand (or 16 million) colors. The 82C455 can also be programmed for higher resolutions up to 800*600 in 16 colors.

The 82C455 integrates four different modules as follows:

Graphics Controller

The Graphics Controller interfaces the 8 or 16-bit CPU data bus to the 32-bit data bus used by the four planes (Maps) of display memory. It also latches and supplies to the Attribute Controller display memory data for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and an attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller also performs any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Sequencer

The Sequencer generates all CPU and display memory timing signals. It controls CPU access of display memory by inserting cycles dedicated to CPU access and contains mask registers which can prevent writes of individual display memory planes.

Attribute Controller

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and graphic modes the 4-bit pixel data acts as an index into a set of internal palette registers which generate a 6-bit stream. Two additional bits of color data are added if 256-color mode is enabled. Text blink, underline and cursor are also the responsibility of the Attribute Controller.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

Pin Description Table

Flatpack Pin No.	Name	Type	Active	Description
63	AD0	I/O	Both	SYSTEM ADDRESS and DATA Bits 0-15. These bits are used to address display memory and the I/O mapped 82C455 internal registers. They also transfer data between the CPU bus and display memory and 82C455 registers. Addresses must be valid when output signal DATAEN is low and data must be held until \VGACMD (COMMAND) is low. Addresses are latched internally.
62	AD1	I/O	Both	
61	AD2	I/O	Both	
60	AD3	I/O	Both	
59	AD4	I/O	Both	
58	AD5	I/O	Both	
57	AD6	I/O	Both	
56	AD7	I/O	Both	
53	AD8	I/O	Both	
52	AD9	I/O	Both	
51	AD10	I/O	Both	
50	AD11	I/O	Both	
49	AD12	I/O	Both	
48	AD13	I/O	Both	
47	AD14	I/O	Both	
46	AD15	I/O	Both	
44	A16	I	Both	SYSTEM ADDRESS Bits 16-18 and AUXILIARY DATA Bits 0-2. These bits transfer a high-order address when DATAEN is low. The auxiliary data bits on pins A16, A17, and A18 respectively are read into Bits 0-2, respectively, of the DIP Switch register when that register is accessed by the CPU. The address bits are latched internally and are ignored for I/O cycles.
43	A17	I	Both	
42	A18	I	Both	
72	\BHE	I	Low	BYTE HIGH ENABLE and AUXILIARY DATA Bit. \BHE low indicates that the high order byte at the current word address is being accessed. If active, \BHE must be valid when DATAEN is low. The pin is also an auxiliary data input which is read into Bit 3 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This data bit is latched internally on the falling edge of \VGACMD (\IOR).

Flatpack Pin No.	Name	Type	Active	Description
41	ADDHI	I	High	ADDRESS HI and AUXILIARY DATA Bit. This high order memory address enable input is generated external to the 82C455 by decoding system addresses A19-A23. As an address, it must be valid when DATAEN is low, is latched internally and specifies that the current memory address is valid for the 82C455. This pin is an auxiliary data bit read into Bit 4 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This input pin is ignored during I/O cycles.
67	DATAEN	O	High	DATA ENABLE. The DATAEN output controls external multiplexing of the system address/data bus. DATAEN low selects address and DATAEN high selects data. In an MCA interface, DATAEN is low when \VGACMD is high and DATAEN is high when \VGACMD is low. In a PC or PC/AT bus interface, DATAEN is low when all \MEMR, \MEMW, \IOR, and \IOW are high. DATAEN is high when any one of \MEMR, \MEMW, \IOR or \IOW is low.
65	\RDLO	O	Low	READ LO. This output controls the direction of the external data transceivers on the low order byte (Bits 0-7) of the address/data bus. It is low when data is read from the 82C455 and high when data is written to 82C455. DATAEN can be used to enable the external transceiver.
64	\RDHI	O	Low	READ HI. This output operates in a fashion identically to the \RDLO output except that it controls direction for the high order byte (Bits 8-15) of the address/data bus. RDHI is low when data is read from 82C455 and high when data is written to 82C455.

Flatpack Pin No.	Name	Type	Active	Description
71	M/IO (AEN)	I	Both	MEMORY/IO or ADDRESS ENABLE and AUXILIARY DATA input. In MCA interfaces, the M/IO input pin selects either a memory or an I/O transfer. M/IO high selects a memory cycle and low selects an I/O cycle. When defined as M/IO, it must be valid when the DATAEN input is low. In PC-Bus interfaces, this input is renamed AEN. When low, it indicates a valid I/O address when DATAEN is low. The M/IO (AEN) signal is latched internally. In both MCA and PC-Bus environments this pin serves as an auxiliary data bit input. It is read into Bit 5 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
69	\S0 (\MEMW)	I	Low	S0 or MEMORY WRITE. \S0 is the memory and I/O write input from the MCA bus. In PC-Bus interface applications, this input is named \MEMW. It must be low for CPU writes to display memory.
70	\S1 (\MEMR)	I	Low	S1 or MEMORY READ. \S1 is the memory and I/O read input from the MCA bus. In PC-Bus interface applications, this input is named \MEMR. It must be low to permit the CPU to read display memory.
79	\VGASETUP (\IOW)	I	Low	VGA SETUP or I/O WRITE. In an MCA environment this active low \VGASETUP input allows configuration registers at I/O Addresses 100-104h to be accessed. All other memory and I/O functions are disabled. In PC-BUS interface applications, this input is named \IOW. It must be low to permit the CPU to write to an 82C455 I/O register.
68	\VGACMD (\IOR)	I	Low	VGA COMMAND or I/O READ. In an MCA environment this active low \VGACMD indicates a command bus cycle. \VGACMD must not be asserted during system memory refresh cycles. In a PC-Bus environment this input is named \IOR. It must be low to permit the CPU to read an I/O register.

Flatpack Pin No.	Name	Type	Active	Description
80	VGAENAB (\REFRESH)	I	High/Low	VGA ENABLE or REFRESH and AUXILIARY DATA. In an MCA environment this active high VGAENAB input signal enables memory and I/O accesses. In the PC-Bus interface, REFRESH high indicates a valid memory cycle. This pin also serves as an auxiliary data bit input which is read into Bit 6 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
78	\VGAREQ (\IOCS16)	O	Low	VGA REQUEST or I/O SELECT 16. In an MCA environment this output indicates that a FAST memory cycle can be executed (this feature can be disabled through a register). In a PC-Bus environment this active low \IOCS16 signal indicates a valid 16 bit I/O cycle.
74	VGARDY	O	Low	VGA READY. When low this output indicates that the current CPU read/write cycle must be extended with wait states.
77	\VGADS16 (\MEN16)	O	Low	VGA ADDRESS SELECT 16 or MEMORY ENABLE 16. In an MCA environment this active low \VGADS16 output indicates that a 16-bit memory or I/O transfer cycle is occurring. In a PC-Bus environment this active low \MEN16 signal indicates a 16-bit memory cycle transfer is enabled. This signal should be used in external logic to decode the high order address and generate \MEMCS16 for the PC-AT bus.
75	\VGAACK (\WR46E8)	O	Low	VGA ACKNOWLEDGE or WRITE 46E8h. In an MCA environment this active low \VGAACK output indicates a valid CPU access (memory and I/O) to the 82C455. In a PC-Bus environment this active low \WR46E8 signal indicates a valid I/O write to address 46E8h.
113	VGAINT	O	Either	VGA INTERRUPT. This pin is asserted whenever the vertical sync signal goes active. This pin can be configured to be active high (EGA) or active low (VGA) through the Emulation Mode register (XR14).

Flatpack Pin No.	Name	Type	Active	Description
114	RESET	I	High	RESET. An active high input which resets the 82C455.
38	TEST	I	High	TEST. This input is used for factory testing only. It should be tied low.
40 111	PWRDN2 PWRDN1	I I	Both Both	POWER DOWN 2,1. The POWER DOWN input pins select the Normal, Relax, and Retire modes of operation as follows: PWRDN2 PWRDN1 OPERATION 0 0 Normal Operation 0 1 Relax Mode 1 0 Retire Mode 1 1 Illegal
105 104 103	CLK0 CLK1 CLK2	I I I	Both Both Both	CLOCK 2-0. Video Clock inputs. One of these dot clock inputs is selected by the Miscellaneous Output Register.
101	MCLK	I	Both	MASTER CLOCK. This clock input is used to sequence internal 16-bit I/O cycles.
108	SENSE	I	Both	SENSE. The state of this input pin can be read in Input Status Register 0, Bit 4.
100	\PALRD	O	Low	PALETTE READ. This output is active low during an I/O read to an address in the range 3C6-3C9h and is connected to the Read input of an external Inmos G171 Palette/DAC.
99	\PALWR	O	Low	PALETTE WRITE. This output is active low during an I/O write to an address in the range 3C6-3C9h and is connected to the Write input of an external Inmos G171 Palette/DAC.
142 3 7 12 16 24 28 33	M0D0 M0D1 M0D2 M0D3 M0D4 M0D5 M0D6 M0D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 0 DATA. Display memory data bus for Plane 0 (Map 0).

Flatpack Pin No.	Name	Type	Active	Description
144	M1D0	I/O	Both	MEMORY 1 DATA. Display memory data bus for Plane 1 (Map 1).
5	M1D1	I/O	Both	
10	M1D2	I/O	Both	
14	M1D3	I/O	Both	
22	M1D4	I/O	Both	
26	M1D5	I/O	Both	
31	M1D6	I/O	Both	
35	M1D7	I/O	Both	
115	M2D0	I/O	Both	MEMORY 2 DATA. Display memory data bus for Plane 2 (Map 2).
118	M2D1	I/O	Both	
120	M2D2	I/O	Both	
122	M2D3	I/O	Both	
124	M2D4	I/O	Both	
128	M2D5	I/O	Both	
130	M2D6	I/O	Both	
132	M2D7	I/O	Both	
116	M3D0	I/O	Both	MEMORY 3 DATA. Display memory data bus for Plane 3 (Map 3).
119	M3D1	I/O	Both	
121	M3D2	I/O	Both	
123	M3D3	I/O	Both	
125	M3D4	I/O	Both	
129	M3D5	I/O	Both	
131	M3D6	I/O	Both	
133	M3D7	I/O	Both	
143	AA0	O	Both	ADDRESS PLANES 0,1. Display memory address bus for DRAM planes 0 and 1.
4	AA1	O	Both	
8	AA2	O	Both	
13	AA3	O	Both	
21	AA4	O	Both	
25	AA5	O	Both	
29	AA6	O	Both	
34	AA7	O	Both	

Flatpack Pin No.	Name	Type	Active	Description
141	BA0	O	Both	ADDRESS PLANES 2,3. Display memory address bus for DRAM Planes 2 and 3.
2	BA1	O	Both	
6	BA2	O	Both	
11	BA3	O	Both	
15	BA4	O	Both	
23	BA5	O	Both	
27	BA6	O	Both	
32	BA7	O	Both	
20	\RAS	O	Low	ROW ADDRESS STROBE. Row address strobe for all DRAM memory banks.
134	\CAS0	O	Low	COLUMN ADDRESS STROBE 0. Active low column address strobe for Memory Plane 0.
135	\CAS1	O	Low	COLUMN ADDRESS STROBE 1. Active low column address strobe for Memory Plane 1.
136	\CAS2	O	Low	COLUMN ADDRESS STROBE 2. Active low column address strobe for Memory Plane 2.
137	\CAS3	O	Low	COLUMN ADDRESS STROBE 3. Active low column address strobe for Memory Plane 3.
139	\WE	O	Low	WRITE ENABLE. Active low write enable signal for all display memory banks/planes.
97	HSYNC	O	Both	HORIZONTAL SYNC OUTPUT. HSYNC is active high if the horizontal polarity bit (Bit 6 of the Miscellaneous Output register; I/O address 3C2) is low. It is active low if the horizontal polarity bit is high.
98	VSYNC	O	Both	VERTICAL SYNC OUTPUT. VSYNC is active high if the vertical polarity bit (Bit 7 of the Miscellaneous Output register; I/O address 3C2) is low. It is active low if the vertical polarity bit is high.
96	BLANK	O	Both	BLANK is a programmable output for blanking the CRT or Flat Panel. Its polarity is programmable. It can be redefined as the Display Enable signal.

Flatpack Pin No.	Name	Type	Active	Description
85	VIDEO0	O	Both	VIDEO 0-7. Eight video outputs to drive a color or monochrome display devices. Color values for digital CRT interface are assigned as follows:
86	VIDEO1	O	Both	
87	VIDEO2	O	Both	
88	VIDEO3	O	Both	
89	VIDEO4	O	Both	
93	VIDEO5	O	Both	
94	VIDEO6	O	Both	
95	VIDEO7	O	Both	

Video0	B	Blue
Video1	G	Green
Video2	R	Red
Video3	BS/V	Secondary Blue/ Monochrome
Video4	GS/I	Secondary Green/Intensity
Video5	RS	Secondary Red
Video6		User Defined
Video7		User Defined

92	SHIFTCLK	O	High	SHIFT CLOCK. Output pixel clock to which video output data is synchronized.
83	WGTCLK	O	High	WEIGHT CONTROL CLOCK. Gray scale reference clock for Panels with Pulse Width Modulation support.
17	ACDCLK	O	High	LCD CLOCK. A 50% duty cycle square-wave with programmable period. Used to back bias LCD panels.
140	\ERMEN	O	Low	EARLY MEMORY INDICATOR. This output indicates whether display memory is being accessed by the CPU or by the 82C455 to refresh the display. A high indicates display device access and a low is CPU access. This signal can be redefined as a general purpose output.
112	\TRAP	O	Low	TRAP. This active low output indicates a TRAP condition requiring special CPU assistance. It can be redefined as a general purpose output pin.
82	PTMC	I	Both	PTMC. This input selects the type of CPU interface. PTMC low selects an MCA interface and high selects a PC-Bus interface. This input must always be valid.

Flatpack Pin No.	Name	Type	Active	Description
1	Vcc			POWER
18				
54				
73				
90				
126				
9	Vss			GROUND
19				
30				
45				
55				
66				
81				
91				
102				
117				
127				
138				
36	NC			NO CONNECTS
37				
39				
76				
84				
106				
107				
109				
110				

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	-	7.0	V
Input Voltage	V_i	-0.5	V_{DD}+0.5	V
Output Voltage	V_o	-0.5	V_{DD}+0.5	V
Operating Temperature	T_{op}	-25	85	0°C
Storage Temperature	T_{stg}	-40	125	0°C

82C455 Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	-40	70	0°C

82C455 DC Characteristics

Parameter	Symbol	Min	Max	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage IOL = TBD	V_{OL}		0.45	V
Output High Voltage IOH = TBD	V_{OH}	3.5		V
Input Leakage Current	I_{IL}	-100	+100	uA
Power Supply Current @25 MHz CLK, 0°C	I_{CC}		100	mA
Ouput High Impedance Leakage 0.45 <VPIN <VDD	I_{OZ}	-100	+100	uA

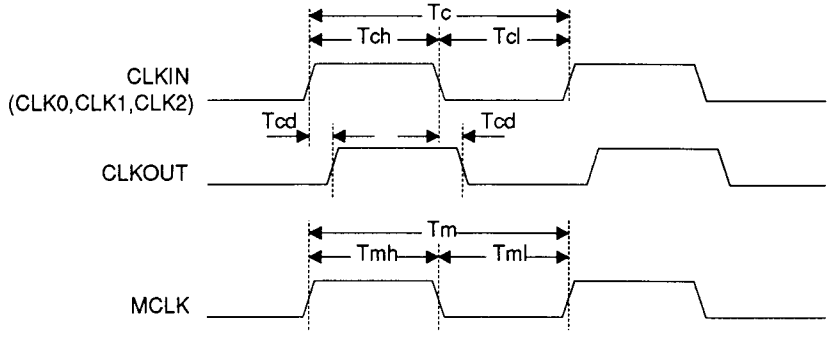
Note: Electrical specifications contained herein are preliminary and subject to change without notice.

82C455 AC Timing Characteristics

(TA = 0°C - 70°C, VDD = 5V±5%)

Clock Timing

Parameter	Symbol	Min(ns)	Max(ns)
CLK Period	T_c	25	
CLK High time	T_{ch}	(Tc/2)-5%	
CLK Low time	T_{cl}	(Tc/2)-5%	
MCLK Period	T_m	25	40
MCLK High time	T_{mh}	(T_m/2)-5%	
MCLK Low time	T_{ml}	(T_m/2)-5%	
CLK to SHIFTCLK delay	T_{cd}		25



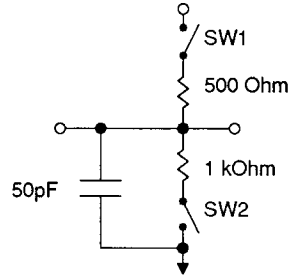
Clock Timing

Video Timing

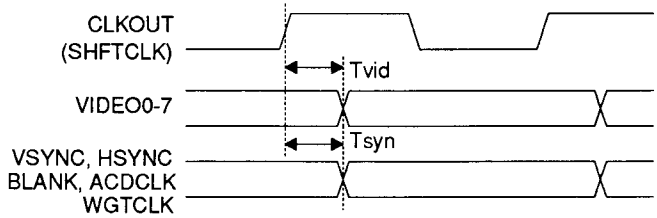
Parameter	Symbol	Min(ns)	Max (ns)
SYNC and VIDEO CONTROL delay from SHIFTCLK	T_{syn}		20
Video delay from SHIFTCLK	T_{vid}	5	20

Other Timing

Parameter	Symbol	Min(ns)	Max (ns)
RESET Pulse Width		64 T_c	



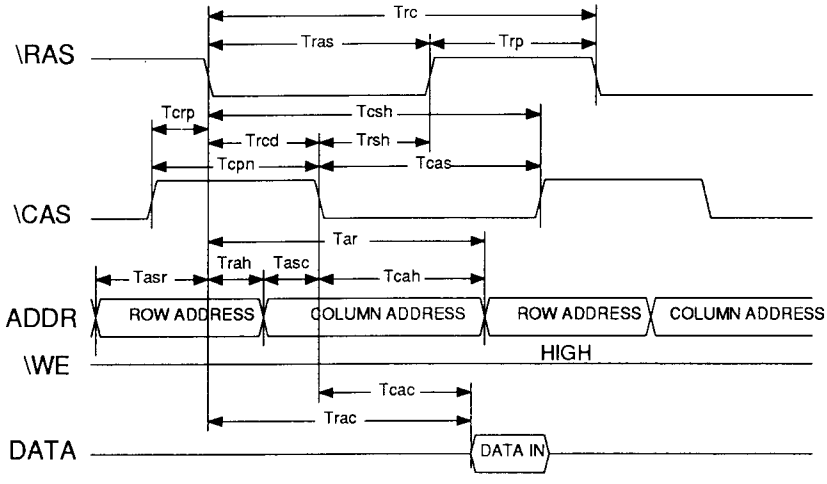
AC Characteristics Load Circuit



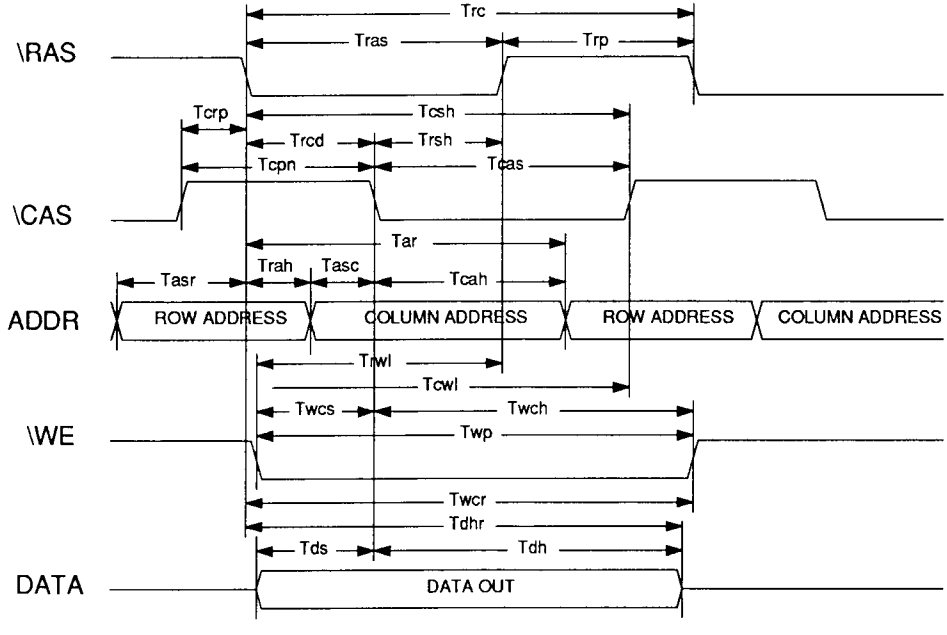
Video Timing

DRAM Timing

Parameter	Symbol	8 dot mode		9 dot mode	
		Min(ns)	Max(ns)	Min(ns)	Max(ns)
Read/Write Cycle time	T_{rc}	$7T_c$	-	$8T_c$	-
\RAS Pulse Width	T_{ras}	$4T_c$	-	$4T_c$	-
Column Address Hold from Ras	T_{ar}	$5T_c$	-	$5T_c$	-
\RAS precharge	T_{rp}	$3T_c$	-	$4T_c$	-
\CAS to \RAS precharge	T_{crp}	$1T_c$	-	$2T_c$	-
\CAS hold from \RAS	T_{csh}	$6T_c$	-	$6T_c$	-
\RAS to \CAS delay	T_{rcd}	$2T_c$	-	$2T_c$	-
\RAS hold from \CAS	T_{rsh}	$2T_c$	-	$2T_c$	-
\CAS Precharge	T_{cpn}	$3T_c$	-	4Tc	-
\CAS Pulse Width	T_{cas}	$4T_c$	-	$4T_c$	-
Row Address Setup to \RAS	T_{asr}	$2T_c$	-	$3T_c$	-
Column Address setup to \CAS	T_{asc}	$1T_c$	-	$1T_c$	-
Row Address hold from \RAS	T_{rah}	$1T_c$	-	$1T_c$	-
Column Address hold from \CAS	T_{cah}	$3T_c$	-	$3T_c$	-
Data Access time from \CAS	T_{cac}	-	$3T_c$	-	$3T_c$
Data Access time from \RAS	T_{rac}	-	$5T_c$	-	$5T_c$
\WE Pulse Width	T_{wp}	$7T_c$	-	$8T_c$	-
Write Data Setup to \CAS	T_{ds}	$2T_c$	-	$2T_c$	-
Write Data Hold from \CAS	T_{dh}	$5T_c$	-	$6T_c$	-
Write Data Hold from \RAS	T_{dhr}	$7T_c$	-	$8T_c$	-
\WE hold from \CAS	T_{wch}	$5T_c$	-	$6T_c$	-
\WE setup to \CAS	T_{wcs}	$2T_c$	-	$2T_c$	-
\WE lead to \RAS	T_{rwl}	$4T_c$	-	$4T_c$	-
\WE lead to \CAS	T_{cwl}	$6T_c$	-	$6T_c$	-
\WE hold from \RAS	T_{wcr}	$7T_c$	-	$8T_c$	-



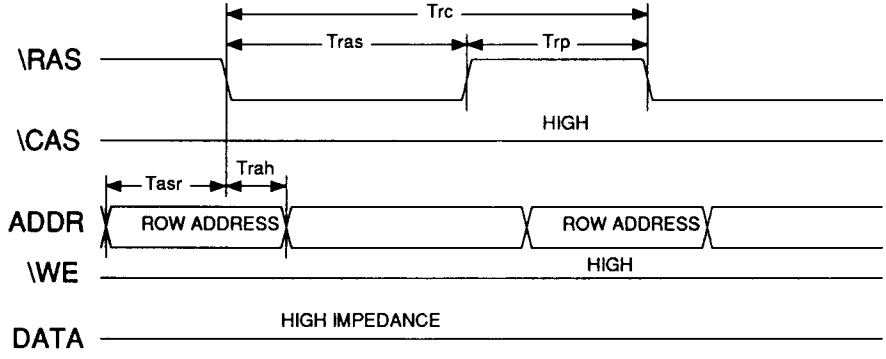
DRAM Read Cycle Timing



DRAM Write Cycle Timing

Compatibility with DRAMs

Parameters	Symbol	Max	Units
CLKIN Frequency for 16 Color Display and 120 ns DRAMS	-	30	MHz
CLKIN Frequency for 16 Color Display and 100 ns DRAMS	-	35-40	MHz
DRAM Refresh interval	-	85000/(V_R*V_L)	ms
Vertical refresh rate	V_R		Hz
Total number of lines per frame (including retrace)	V_L		-

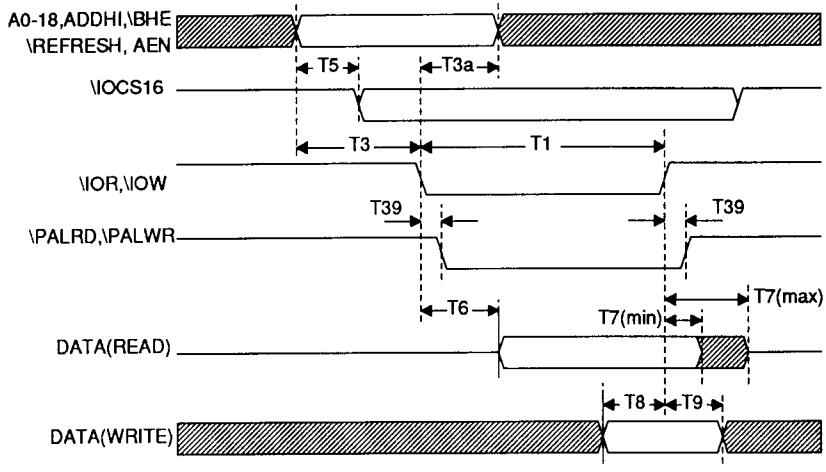


DRAM Refresh Cycle Timing

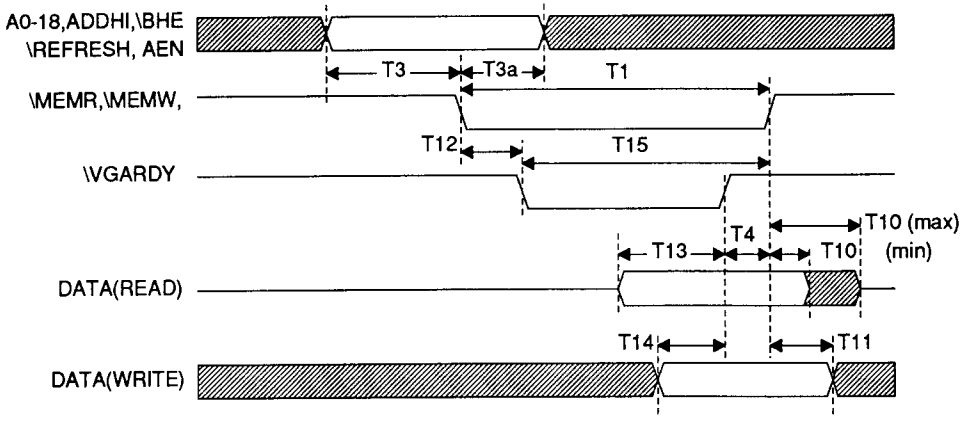
PC & PC/AT BUS Interface

I/O and Memory Bus Timing

Parameter	Symbol	Min(ns)	Max(ns)
\MEMRD, \MEMWR, \IOR, \IOW Pulse Width	T1	175	
Address setup to Read/Write	T3	80	
Address hold from Read/Write Signal	T3a	20	
\IOCS16 Delay from valid address	T5		25
\MEMRD,\MEMWR hold from \VGARDY (Memory)	T4	0	
I/O Read Data delay from \IOR	T6		50
I/O Read Data hold from \IOR	T7	10	40
I/O Write Data setup to \IOW	T8	40	
I/O Write Data hold from \IOW	T9	0	
Memory Read Data hold from \MEMR	T10	10	40
Memory Write Data hold from \MEMW	T11	0	
\MEMRD, \MEMWR to \VGARDY Low delay	T12		25
Memory Read Data setup to \VGARDY	T13	25	
Memory Write Data setup to \VGARDY	T14	40	
\VGARDY width	T15	$7T_c$	128Tc
\PALRD,\PALWR delay from Read/Write	T39		25
\MEN16 delay from Address	T2		25



PC and PC/AT Bus I/O Cycle Timing

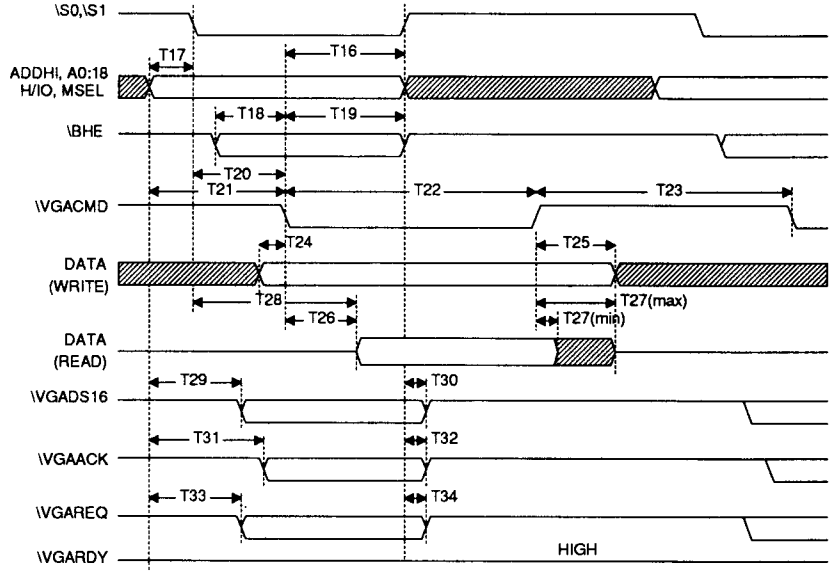


PC and PC/AT Bus Memory Cycle Timing

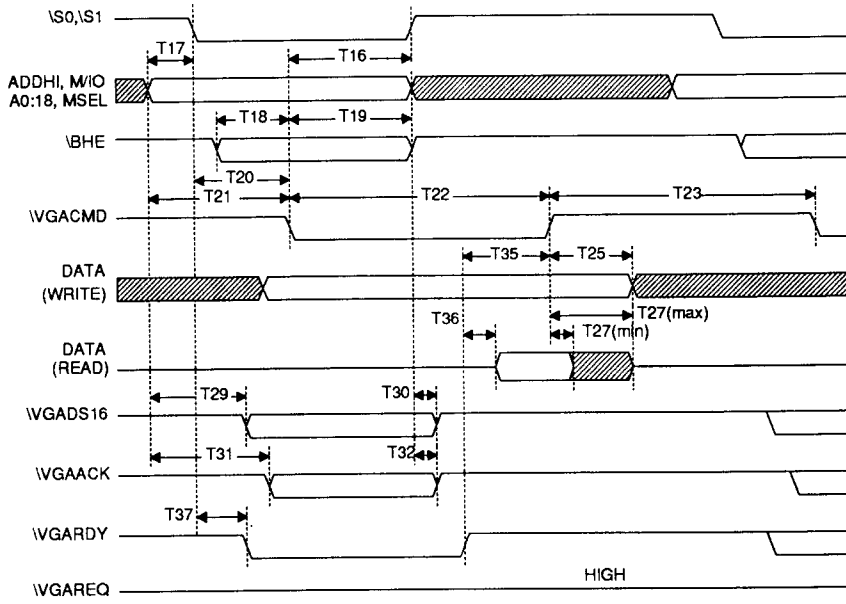
MCA Interface

I/O and Memory Cycle Timing

Parameter	Symbol	Min(ns)	Max(ns)
Status hold from \VGACMD	T16	20	
Status active from address valid	T17	0	
\BHE setup to \VGACMD	T18	30	
Address, \BHE hold from \VGACMD	T19	20	
\VGACMD active from Status	T20	45	
\VGACMD from address valid	T21	80	
\GACMD Pulse Width	T22	80	
\GACMD inactive to next \VGACMD	T23	80	
Write data setup to \VGACMD	T24	0	
Write data hold from \VGACMD	T25	10	
Read data valid from \VGACMD	T26		50
Read data hold from \VGACMD	T27	10	40
Status to Read data valid	T28		125
\VGADS16 active from address valid	T29		25
\VGADS16 inactive from Status	T30	5	25
\VGAACK active from address valid	T31		25
\VGAACK inactive from Status	T32	5	25
\VGAREQ active from address valid	T33		25
\VGAREQ inactive from Status	T34	5	25
\VGARDY active from \VGACMD high	T35	65	
Read data from \VGARDY active (high)	T36		50
\VGARDY inactive (low) from Status	T37		25
Write data setup to \VGARDY active (high)	T38		40
\PALRD, \PALWR delay from Command	T39		25



MCA Bus I/O Cycle Timing

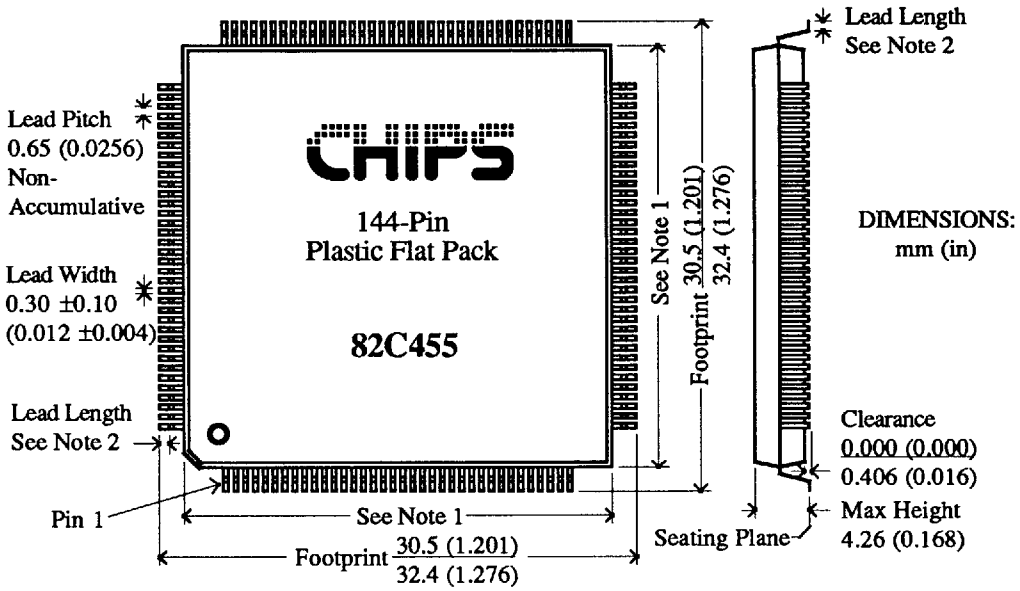


MCA Bus Memory Cycle Timing

Chips and Technologies, Incorporated
3050 Zanker Road, San Jose, CA 95134 408-4340600 Telex 272929 CHIP UR

T-52-33-45

82C455 Mechanical Specifications:



Note 1: Package Body Size = 26 ±0.2 (1.024 ±0.008)
Note 2: Lead Length = 1.2 ±0.2 (0.047 ±0.008)

82C455 Suggested PCB Pad Layout: