ECC-on-SIMM Memory Modules

The ECC-on-SIMM family of memory modules are DRAM SIMMs organized as 2M x 36, 4M x 36 and 8M x 36. In addition to the JEDEC standard pinout, a special option is available which brings out an error indicator signal for each byte of data on the SIMM. The four error lines are brought to the SIMM tabs on pins 29, 46, 66 and 71 for errors on byte 0, 1, 2 and 3, respectively.

Part Number Availability

The error indicator option is available only on X36 70ns ECC-on-SIMM modules. The cross reference table for standard modules and error indicator modules is shown below.

Organization	Standard Part Number	Error Indicator(x36 ONLY)
2M x 36	IBM11E/D2480B-70	IBM11E/D2490B-70
4M x 36	IBM11E/D4480B-70	IBM11E/D4490B-70
8M x 36	IBM11E/D8480B-70	IBM11E/D8490B-70

Error Indicator Line Timings

The error indicator signals are minus-active and are driven by 4mA tristate drivers that come out of tristate whenever $\overline{CAS}$ is activated. Because each error-line driver independently drives either a high or low every cycle, they can not be dotted. The error lines are valid for the same duration as data on a read. That is, 20ns (t_{cac}) after $\overline{CAS}$ is valid during a read cycle, the error lines will be valid. They will remain valid until $\overline{CAS}$ returns high. The drivers will come out of tristate about 5ns after $\overline{CAS}$ falls and return to tristate about 5ns after $\overline{CAS}$ rises, although these timings are not guaranteed. The lines will activate whenever a single-bit error is being corrected or a double bit error is detected. In case of the latter, bad parity will be sent to the system to indicate an uncorrectable error. An active error line could indicate an error in either of the two data-bit DRAMS or the check-bit DRAM associated with that byte.

Error Line Functioning During Write Operations

The ECC-on-SIMM module will detect bad parity on write operations. That is, if the system sends any byte of data with parity different than that of the first byte of data written after power-on, the SIMM will flag that data as being invalid and return a parity error when data is subsequently read. During write operations, the error line comes out of tristate with the same timings as in a read operation, ie: approximately 5ns after $\overline{CAS}$ transitions, however it is valid from a point 15ns after valid $\overline{CAS}$ and remains valid until $\overline{CAS}$ rises. An error during a write operation indicates that a parity error is being detected and that a subsequent read of that data will also reflect that parity error The use of the error line during write operations has not been characterized.