Basic Architecture

Can be used in two, four or eight-byte systems. SIMMs are organized by assignment of data, $\overline{RAS}$ and $\overline{CAS}$. A bank is defined as being one DRAM chip deep by the following data bus width:

Organization	
SIMM Type	Data Bus Width
Non-Parity	32
Parity	36
ECC	36 or 40

If a SIMM has two banks, the corresponding data I/Os from each bank are dotted.

Data bits on non-parity and parity SIMMs are assigned as follows (note that individual bytes are addressable by unique $\overline{CAS}$ signals):

Parity Data Bit Assignment				
SIMM Type	Word 0,2 Data ($\overline{RAS}$ 0,2)		Word 1,3 Data ($\overline{RAS}$ 1,3)	
	Byte 0 ($\overline{CAS}$ 0)	Byte 1 ($\overline{CAS}$1)	Byte 2 ($\overline{CAS}$2)	Byte 3 ($\overline{CAS}$3)
Non-Parity	DQ 0-7	DQ 9-16	DQ 18-25	DQ 27-34
Parity	DQ 0-7, PQ8	DQ 9-16, PQ17	DQ 18-25, PQ26	DQ 27-34, PQ35

ECC SIMMs do not have addressable bytes (a single RAS and CAS select the full word) and are organized as follows:

ECC Data Bit Assignment	
SIMM Type	ECC Word Width
X36	DQ 0-35
X40	DQ 0-39
Note: $\overline{RAS}$ 0, $\overline{CAS}$0 selects first bank and $\overline{RAS}$ 1, $\overline{CAS}$1 select second bank	

Eight-byte ECC systems are implemented with a total of 64 data bits plus 8 check bits, or a total of 72 data bits. Two 36-bit ECC-optimized SIMMs are used in parallel in these applications. Four-byte ECC systems involve 32 data bits plus 7, or 8 check bits and are supported by x40 ECC-optimized SIMMs.

A specific memory subsystem can be designed to support either parity or ECC. This enables a single system to be utilized in multiple ways. The apparent difference in ECC and parity data pins is simply due to their identification numbering and is accommodated by making the proper design provisions in the interfacing memory controller.

DRAM Addressing Effects

(Note that A10 and A11 occur at different pins on ECC and parity and non-parity based SIMMs).

DRAM			Row Addresses	Column Addresses	Cell Retention (ms)
Depth	Organization	Addressing			
1Mb	1M x 4 or 1M x 16	10/10*	A0 - A9	A0 - A9	16
2Mb	2M x 8	11/10	A0 - A10	A0 - A9	32
4Mb	4M x 1 or 4M x 4	11/11* or 12/10	A0 - A10 A0 - A11	A0 - A10 A0 - A9	32 or 64
* Also referred to as symetrical or square addressing.					

Memory refresh problems will occur if all of the required row columns are not refreshed. The memory system designer is advised to ensure the memory refresh generation portion of the memory controller logic correctly accommodates the requirements of all of the SIMMs to be supported.

72 Pin SIMM Pin Assignments

Pin #.	Non-Parity	Parity	ECC Optimized		Pin #	Non-Parity	Parity	ECC Optimized	
	X 32	X 36	X 36	X 40		X 32	X 36	X 36	X 40
1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	*37	-	PQ17	DQ19	DQ19
2	DQ0	DQ0	DQ0	DQ0	*38	-	PQ35	DQ20	DQ20
3	DQ18	DQ18	DQ1	DQ1	39	V_{SS}	V_{SS}	V_{SS}	V_{SS}
4	DQ1	DQ1	DQ2	DQ2	40	$\overline{CAS}$0	$\overline{CAS}$0	$\overline{CAS}$0	$\overline{CAS}$0
5	DQ19	DQ19	DQ3	DQ3	*41	$\overline{CAS}$2	$\overline{CAS}$2	A10	A10
6	DQ2	DQ2	DQ4	DQ4	*42	$\overline{CAS}$3	$\overline{CAS}$3	A11	A11
7	DQ20	DQ20	DQ5	DQ5	43	$\overline{CAS}$1	$\overline{CAS}$1	$\overline{CAS}$1	$\overline{CAS}$1
8	DQ3	DQ3	DQ6	DQ6	44	$\overline{RAS}$0	$\overline{RAS}$0	$\overline{RAS}$0	$\overline{RAS}$0
9	DQ21	DQ21	DQ7	DQ7	45	$\overline{RAS}$1	$\overline{RAS}$1	$\overline{RAS}$1	$\overline{RAS}$1
10	V_{CC}	V_{CC}	V_{CC}	V_{CC}	*46	-	-	DQ21	DQ21
*11	-	-	PD5	PD5	47	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
12	A0	A0	A0	A0	*48	-	-	$\overline{ECC}$	$\overline{ECC}$
13	A1	A1	A1	A1	49	DQ9	DQ9	DQ22	DQ22
14	A2	A2	A2	A2	50	DQ27	DQ27	DQ23	DQ23
15	A3	A3	A3	A3	51	DQ10	DQ10	DQ24	DQ24
16	A4	A4	A4	A4	52	DQ28	DQ28	DQ25	DQ25
17	A5	A5	A5	A5	53	DQ11	DQ11	DQ26	DQ26
18	A6	A6	A6	A6	54	DQ29	DQ29	DQ27	DQ27
*19	A10	A10	$\overline{OE}$	$\overline{OE}$	55	DQ12	DQ12	DQ28	DQ28
20	DQ4	DQ4	DQ8	DQ8	56	DQ30	DQ30	DQ29	DQ29
21	DQ22	DQ22	DQ9	DQ9	57	DQ13	DQ13	DQ30	DQ30
22	DQ5	DQ5	DQ10	DQ10	58	DQ31	DQ31	DQ31	DQ31
23	DQ23	DQ23	DQ11	DQ11	59	V_{CC}	V_{CC}	V_{CC}	V_{CC}
24	DQ6	DQ6	DQ12	DQ12	60	DQ32	DQ32	DQ32	DQ32
25	DQ24	DQ24	DQ13	DQ13	61	DQ14	DQ14	DQ33	DQ33
26	DQ7	DQ7	DQ14	DQ14	62	DQ33	DQ33	DQ34	DQ34
27	DQ25	DQ25	DQ15	DQ15	63	DQ15	DQ15	DQ35	DQ35
28	A7	A7	A7	A7	*64	DQ34	DQ34	-	DQ36
*29	A11	A11	DQ16	DQ16	*65	DQ16	DQ16	-	DQ37
30	V_{CC}	V_{CC}	V_{CC}	V_{CC}	*66	-	-	-	DQ38
*31	A8	A8	A8	A8	67	PD1	PD1	PD1	PD1
32	A9	A9	A9	A9	68	PD2	PD2	PD2	PD2
*33	$\overline{RAS}$3	$\overline{RAS}$3	-	-	69	PD3	PD3	PD3	PD3
*34	$\overline{RAS}$2	$\overline{RAS}$2	-	-	70	PD4	PD4	PD4	PD4
*35	-	PQ26	DQ17	DQ17	*71	-	-	-	DQ39
*36	-	PQ8	DQ18	DQ18	72	V_{SS}	V_{SS}	V_{SS}	V_{SS}

*Indicates differences

Presence Detect Considerations

Presence Detects can provide the following benefits:

- Determine if any SIMM is present.
- Determine module density and generate proper addressing and refresh requirements as appropriate.
- Determine DRAM module speed
- Determine if non-ECC or ECC to provide proper addressing and DQ interpretation.
- Protect against incorrect speed SIMM plugged in.
- Ensure all installed SIMMs are the same type.

The table on below shows the listing for the 72 pin SIMM family. Presence detect ouputs must be

tied to V_{CC} through a pullup resistor to generate a high-logic level when the SIMM PD pin is open or low-voltage when the PD pin is grounded. This produces the required logical signals decodable by the interfacing logic. The Presence Detect circuitry does not permit “dotting” of signals. If a particular system supports multiple SIMM sockets, then MUX methods can be employed to minimize the memory support chip pins used for Presence Detect inputs from multiple SIMM sockets. If Presence Detect signals are employed, then the system user is freed, to some extent, of having to follow complex SIMM installation instructions and limitations spelled out in the operations manual. In addition, a systems power-up test procedure can be employed to perform memory tests to determine the memory present and/or the number of memory banks on an installed SIMM and adjust control and addressing signals as necessary.

Pin #		48	**67**	68	**69**	**70**	**11**
Organization	t_{RAC}	$\overline{ECC}$	PD1	PD2	PD3	PD4	#PD5
256K x32, x36, x40	100ns	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	NC
	80ns	V_{SS}	V_{SS}	NC	NC	V_{SS}	NC
	70ns	V_{SS}	V_{SS}	NC	V_{SS}	NC	NC
	60ns	V_{SS}	V_{SS}	NC	NC	NC	NC
512k x 32, x36, x40	100ns	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	NC
	80ns	V_{SS}	NC	V_{SS}	NC	V_{SS}	NC
	70ns	V_{SS}	NC	V_{SS}	V_{SS}	NC	NC
	60ns	V_{SS}	NC	V_{SS}	NC	NC	NC
1M x 32, x36, x40	100ns	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC
	80ns	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	NC
	70ns	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC
	60ns	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
2M x 32, x36, x40	100ns	V_{SS}	NC	NC	V_{SS}	V_{SS}	NC
	80ns	V_{SS}	NC	NC	NC	V_{SS}	NC
	70ns	V_{SS}	NC	NC	V_{SS}	NC	NC
	60ns	V_{SS}	NC	NC	NC	NC	NC
4M x 32, x36, x40	80ns	V_{SS}	V_{SS}	NC	NC	V_{SS}	V_{SS}
	70ns	V_{SS}	V_{SS}	NC	V_{SS}	NC	V_{SS}
	60ns	V_{SS}	V_{SS}	NC	NC	NC	V_{SS}
	50ns	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}
8M x 32, x36,x40	80ns	V_{SS}	NC	V_{SS}	NC	V_{SS}	V_{SS}
	70ns	V_{SS}	NC	V_{SS}	V_{SS}	NC	V_{SS}
	60ns	V_{SS}	NC	V_{SS}	NC	NC	V_{SS}
	50ns	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}

1. NC=Open circuit (no connections)
2. $\overline{ECC}$ Pin: V_{SS} for.ECC Module, NC for Non ECC Module
3. # PD5 applies only to ECC-Optimized SIMMs. For this PD only, the SIMM PD will be grounded through a 2.6K Ohms resistor

For more information contact your IBM Microelectronics sales representative or
visit us on World Wide Web at http://www.chips.ibm.com