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MICROPROCESSOR REPORT

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The Transformation of Transmeta

Finding New Business in Consulting and IP Licensing

By Kevin Krewell {5/2/05-01}

Depending on your viewpoint, Transmeta is either a high-tech-bubble stock finally gone bad or an earnest but struggling startup that took a whack at the nose of the lion and got mauled. The company has decided to change its business model, deemphasizing its products in the notebook market and backing away from direct competition with Intel. Instead, Transmeta will leverage its extensive intellectual property (IP) portfolio and its experience with microprocessor design to become more of a licensing and services company. The optimal customer is one that licenses Transmeta's IP and then hires the company to help implement the IP. And at the announcement of the restructuring, Transmeta also announced it had found that ideal customer—Sony.

The company has had many hundreds of millions of dollars pumped into it over the past decade and has yet to turn a profit. The latest reinvention of the company is designed to cut the financial bleeding to manageable quantities, but Transmeta has yet to commit to a timeline for profitability. The chances that it can ever generate enough profit to pay for net investment in the company are very slim. Most of the previous investment must be written off, and the company's resources and intellectual property must be freshly assessed.

Lessons Learned

The company started out as a bold upstart startup challenging the king of PC processors, Intel. It had a very different approach to microprocessor design, and it set a public goal to address a new, very low power segment of the notebook market. (See *MPR 1/24/00-05*, "Transmeta Unveils Crusoe," and *MPR 2/14/00-01*, "Transmeta Breaks x86 Low-Power Barrier.") The company underestimated both the speed with which Intel would respond to its challenge and the seriousness with which Intel would take it as a threat. There was a time when Intel was possibly focused more on Transmeta than it was on the much larger and more established competitor AMD. (See *MPR 7/03/00-02*, "Intel Strikes Back at Transmeta.") That attention at Intel led to the Ultra-Low-Voltage (ULV) Pentium III and greater attention to Intel's own Israeli-designed Pentium M processor.

With Intel's full attention on it, Transmeta could not afford to stumble in its execution—but stumble it did. Transmeta's Crusoe processor did not live up to its performance claims, although it did initially offer acceptable performance at reasonable clock speeds and lower power consumption. Back in 2001, Transmeta got the Crusoe processor designed into some of the coolest, most cutting-edge notebook products; then the company stumbled badly.

Transmeta had started fabricating in IBM's 180nm process. For the transition to 130nm, however, the company decided to source 100% of the 130nm product from TSMC, leaving initial partner IBM out in the cold. TSMC was, and still is, a leading foundry that is still popular with many fabless semiconductor manufacturers. Unfortunately for Transmeta, the transition from 180nm aluminum interconnect to 130nm with copper interconnect turned out to be a much longer learning experience for TSMC than the company had planned. TSMC could not build sufficient numbers of processors to meet the market demand in late 2000 and early 2001, just as Transmeta needed to ramp up Crusoe volumes. And Transmeta lacked a backup plan, such as using IBM's 130nm process.

The second major stumble for Transmeta was its taking too long to get the next-generation Efficeon processor to market. In late 2002, Transmeta promised that the TM8000/Efficeon (code-named "Astro") would ship production quantities in 3Q03. (See *MPR 1/06/03-02*, "Transmeta Shows New TM8000 Astro.") Efficeon did sample in late 2003, but shipments of the Sharp notebook with the 130nm Efficeon processor didn't begin until 1Q04. By the time the 130nm Efficeon products launched, Intel had a second-generation, 90nm Pentium M (Dothan). The time lag between Crusoe and Efficeon was too long, and Transmeta lost its design wins at Sony and Fujitsu to Intel, thus losing market momentum. Intel spent well over $100 million on a major worldwide brand campaign for Centrino. Matching Intel's resources and marketing efforts was difficult for a small company like Transmeta.

The Pioneer and the Indians

It is often said that one can tell who the pioneers are: they are the ones with arrows in their backs. As a pioneer of low-power x86, Transmeta has its share of arrows in its back. Although some, as mentioned earlier, were self-inflicted, others came from the original inhabitant of the x86 world—Intel. Transmeta made a point of criticizing Intel for not offering a very low power x86 processor that was suitable for very thin and very small notebooks and tablets PCs, doing everything it could to annoy Intel. Intel responded with the Ultra-Low-Voltage Pentium III and, later, the very capable Pentium M processor family.

Transmeta also found itself in a number of cutting-edge products—some of which were more popular in Japan than in the United States or the rest of the world. Other products never took off (like web tablets); some still have great potential but haven't reached mainstream volumes (like subnotebooks, Tablet PCs, and blade servers); and still others, such as OQO's prototype ultrapersonal PC and Orion Multisystems' DS-96 Deskside Personal Supercomputer, will likely appeal only to a niche market.

New CEO, New Business Model, New Projects

With the company rapidly burning through money, with losses of approximately $25 million per quarter, the company needed some radical restructuring and a new business model, because selling notebook processors was not paying the bills. The company had announced earlier that it was actively pursuing licensing deals for its LongRun2 power-management and leakage-control technology. (See *MPR 10/27/03-01*, "Transmeta Gets More Efficeon.") In January, Transmeta took the unusual step of preannouncing that it would reveal a new business model on March 31. On schedule, on March 31, the company announced a number of significant management, restructuring, and business model changes. The new business model contains a three-part synergistic relationship of engineering design services, IP licensing, and continued Efficeon processor sales.

But in its restructuring conference call, Transmeta delivered a number of surprises, including the announcement of a multiyear engineering services contract with Sony Corporation and Sony Computer Entertainment, Inc., to develop lower-power processors for undisclosed products. More than 100 Transmeta engineers were assigned to the multiyear project to develop processors, including a Cell processor derivative, for Sony.

Part of the announcement included a management reorganization, with Matt Perry leaving his post as president and CEO as well as leaving Transmeta and the company's former VP of marketing, Art Swift, replacing Perry. In the reorganization process, 67 employees lost their jobs, mostly in sales, marketing, and administration. Transmeta went from 310 employees at the end of 2004, to 208 employees after the layoff. (Another 35 employees left voluntarily in 1Q.) Transmeta declared an end of life (EOL) for some older products, such as the Crusoe processor and the 130nm version of the Efficeon processor. Some select customers will continue to receive 90nm Efficeon processors as long as the business remains profitable for Transmeta.

In addition to the services contract with Sony, Transmeta is continuing to look for additional opportunities to license out its IP. The primary IP that Transmeta management has focused on is the LongRun2 power- and leakage-management technology. Transmeta is looking to license the technology to additional fabs. Aside from up-front payments from Sony, Fujitsu, and NEC, the company expects to see royalties from LongRun2 on product to ship in 2006. The company said that LongRun2 has applicability to 90nm and 65nm processes and can complement high-*k* gate dielectric, but that it is not compatible with silicon-on-insulator (SOI) wafers.

Transmeta's short-term goal is to reduce the money bleeding to a manageable size of less than $5 million per quarter.

Why Would Sony Make This Deal?

Many were surprised that Sony would contract with Transmeta for work on Cell. After all, Sony has a significant investment in the STI Design Center with partners Toshiba and IBM. IBM has expressed interest in developing custom Cell derivatives. Why would Sony go to a company like Transmeta that has no Power architecture experience? The first reason is Sony's public statement endorsing Transmeta's LongRun2 power- and leakage-control technology. There are rumors that the IBM Cell processor, even in 90nm SOI, is too power-hungry for Sony's plans. Considering time-to-market factors and the competition with Microsoft's next Xbox360 console, however, Sony may be forced to use the existing first-generation Cell processor in a larger, hotter, and more expensive enclosure; it could then reduce cost and power using a Transmeta design. The Transmeta engineers have spent the better part of the past decade designing low-power processors, whereas IBM is better known for high-powered processors. Transmeta could also apply LongRun2 to other

Sony products, such as the recently introduced PSP, in order to increase battery life.

The less obvious point about LongRun2 is that it has been qualified only on bulk silicon processes, not on the SOI wafers IBM used to fabricate the first-generation Cell processor. In a phone interview, Dave Ditzel, Transmeta founder and chief technology officer (and often chief company evangelist), called LongRun2 a "bridge between SOI and bulk (silicon)." As such, LongRun2 could allow the less expensive bulk silicon to have the same or similar power-saving benefits that IBM and others get from SOI. By eliminating SOI, Sony could lower the cost of the wafers. With the Transmeta technology and expertise, Sony could reduce the cost of a future PlayStation 3.

At this point, we can conjecture even further beyond the public statements. At the Game Developers Conference in March, game programmers were beginning to deal with the complexity of designing code for multicore processors. Many were concerned about the complexity of designing a threaded programming model and debugging it later. If Sony could create a virtual environment wrapper around the Cell architecture to hide some of the complexity, it would greatly improve programmer productivity. Sony, Toshiba, and IBM have also talked of using Cell in other consumer devices beyond Sony's next PlayStation. If game programmers, who have a history of working with odd hardware to make code run fast, are concerned about multicore programming, what will the general embedded programmer think? Abstracting the architectural complexity of Cell under a virtual processor layer could be very helpful. One of the challenges would be to make the virtual wrapper deterministic enough for games and other embedded designs.

Now look at what Transmeta has done with its Crusoe and Efficeon processor families. The company developed an x86 virtual machine using the Code Morphing Software (CMS) layer on top of a VLIW architecture. Although Crusoe performance was not very deterministic, the second-generation CMS on Efficeon made significant improvements in that area. It might be possible for Transmeta to develop a form of CMS that works on top of Cell. At the company launch event for Transmeta, the company demonstrated running Java code on Crusoe, so it can retarget the software if the opportunity is there.

A New Role for Efficeon

Details of the new market for Efficeon were harder to obtain from Transmeta. Transmeta was forced to increase customer charges for processors, which would normally be a way to encourage customers to design a part out. Ditzel said that development work would continue on Efficeon, and that a new processor roadmap will appear in the future. Ditzel hinted that we could also see the release of a LongRun2-enabled Efficeon. Ditzel also said that Transmeta had embarked on a new strategy and a new volume market for Efficeon that would not go head to head with Intel. That information was both enticing and cryptic, implying that Transmeta would back away from the notebook market. Perhaps the company is planning to retarget the CMS and VLIW core at a new instruction-set architecture, such as Power. More likely, the new market will be a volume embedded applications like set-top boxes, PVRs, or media devices, where a low-power, fanless design would be desirable. With most of the R&D expenses written off or applied to the IP business, the company is looking at Efficeon processors as an incremental revenue opportunity.

Transmeta has had to admit defeat in its plans to revolutionize the notebook market, but the company is a scrappy survivor. It has a new mission that can help solve the problems that plague many processors on the cutting edge of process and integration. The company can continue to leverage its unique IP in chip power management and in the combination software and hardware to execute x86 instructions without (apparently) violating AMD and Intel patents. This is IP that may have additional value to the right client. Where else can one go to get a customized x86 processor?

The new word one hears mentioned at Transmeta is "volume," something it didn't have before. The new Transmeta still has some of the baggage of its checkered past, but it also has a wealth of experience, as well as some money and new clients with which to move forward.

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STORAGE PROCESSOR LEVERAGES LEON

Network RAID Controller Based on Free SPARC V8-Compatible Core

By Tom R. Halfhill {5/2/05-02}

How to beat the high cost of living: design a new chip around bits and pieces of LEON, a freely licensable SPARC-compatible processor core from the European Space Agency. The finished RAID controller chip is now solving space problems of a different sort by bringing affordable network-attached storage (NAS) to home and small-business users.

Left on the ground this time are intellectual-property (IP) vendors such as ARC International, ARM, MIPS Technologies, and Tensilica. One of them almost certainly would have scored this design win if a free alternative to their licensable processor cores were not available. However, designing a processor using a free core involves trade-offs that will keep IP vendors from losing significant business for the near future.

The new LEON-derived chip is the IT3107 network storage processor from Infrant Technologies, a four-year-old privately held company in Fremont, California. ("Infrant" stands for "infrastructure new technology.") This is the second RAID controller Infrant has designed using parts of LEON1, a 32-bit processor core adhering to the SPARC V8 instruction-set architecture. The European Space Agency freely distributes a synthesizable VHDL model of LEON1 under a GNU license. (See *MPR 1/16/01-01*, "A GNU SPARC?")

Infrant chose to start with LEON for two reasons. First, it believes the SPARC-compatible architecture is more suitable than other licensable architectures for what amounts to an embedded server. According to Infrant, even the MIPS architecture isn't as good for this application as SPARC is. The company's second reason for choosing LEON was, frankly, to avoid paying a commercial IP vendor hundreds of thousands of dollars in upfront licensing fees and chip royalties.

In addition to offering the IT3107 as a standard part, Infrant also sells complete IT3107-based system boards and RAID software to OEM companies making NAS products. The bundled software includes Infrant's own RAIDiator embedded operating system and an easy management program that runs inside a web browser. Infrant's customers can produce their own RAID subsystems by simply wrapping the system board in a plastic case and adding Serial ATA (SATA) disk drives. This is the kind of turnkey product kit many of today's OEMs demand.

To bring this product concept to market more quickly, Infrant also sells its own RAID boxes at retail. Its newest product is called ExpandaNAS, because users can start with only one disk drive and add more later. Intended for home and small-business users needing large amounts of plug-and-play disk storage with RAID protection, ExpandaNAS has internal connectors for up to four SATA hard drives. Using the largest SATA drives currently available (400GB), users can stuff up to 1.6TB of storage into a box retailing for less than $500 (without drives). Although the ExpandaNAS product would seem to compete with the IT3107-based NAS products from Infrant's own customers, the company says its boxes have limited retail distribution and haven't upset any customers.

Designing a Processor With LEON

To create the IT3107, Infrant started with the LEON1 integer unit, which implements all the SPARC V8 integer instructions and the usual SPARC register windows. Normally, storage controllers don't need floating-point math, so the IT3107 has no FPU. (LEON1 doesn't include an FPU, either, but it has an

interface for the Sun MicroSPARC FPU core, available under a Sun community source license.) As a result, Infrant's core is a basic 32-bit RISC processor with a conventional five-stage uniscalar pipeline. Fabricated in 0.15-micron CMOS, the IT3107 runs at 280MHz.

What distinguishes the IT3107 from other LEON-based chips is the application-specific IP wrapped around the processor core—or rather, the processor cores, because the IT3107 is an asymmetric dual-core chip. One core is the CPU, which runs the RAIDiator operating system and other embedded software, assisted by a hardware RAID engine. The second core powers the DMA controller, which Infrant calls the DataJunction. The DMA controller connects the RAID engine to a 64-bit DDR-1 memory interface running at 140MHz (effectively 280MHz), providing 2.2GB/s of bandwidth to PC2700 DRAM.

In addition, the IT3107 has a four-channel 1.5Gb/s SATA ×4 controller, a Gigabit Ethernet controller with TCP/IP offload hardware, a NAND flash-memory controller for diskless system boots, a 32-bit/33MHz PCI host controller, and a miscellaneous serial controller, which supports a UART, Two-Wire interface, LED interface, and general-purpose I/O (GPIO). There's also a JTAG boundary-scan interface for debugging. The physical link layer (PHY) for SATA is built in, but the Ethernet controller requires an external PHY. The whole chip design fits into a 449-pin PBGA package requiring a 1.5V core supply, 3.3V I/O, and 2.5V DRAM. Figure 1 shows a block diagram of the IT3107.

In a NAS subsystem, disk drives connect to the SATA interfaces and transfer data to and from the host system over a network using the chip's Gigabit Ethernet port. The PCI interface supports additional peripherals—such as external disk drives, printers, and connections to wireless networks—but isn't involved in moving data to the disk array, so it's not a bottleneck. Although the IT3107 has some logic to accelerate Triple-DES (3DES) cryptography, that hardware lies fallow for now, owing to the lack of an industry-standard RAID security protocol.

At $120 in 1,000-unit quantities, the IT3107 seems pricey. It's in the same price range as network storage controllers for much higher end RAID applications, such as AMCC's new PowerPC 440SPe. Announced at Fall Processor Forum 2004, the three-way superscalar PowerPC 440SPe runs at more than twice the clock frequency of the IT3107 and has Gigabit Ethernet, three PCI Express interfaces (eight lanes total), PCI-X, a DDR-2 memory controller, a 256KB L2 cache, and many more features. Yet it costs $110 (533MHz) to $128 (667MHz), virtually the same price as the IT3107, albeit in 10,000-unit quantities. (See *MPR 10/25/04-01*, "Embedded CPUs Zoom at FPF.")

Despite its price, the IT3107 is better suited for the lower-end RAID applications it targets. It integrates the SATA controllers and PHYs (the PowerPC 440SPe requires external chips for those functions), dedicates a second 32-bit processor core to DMA, and includes a license for Infrant's RAIDiator embedded software. The PowerPC 440SPe is clearly designed for RAID subsystems in high-performance servers.

RAIDiator Has User-Level Management Tools

Infrant's RAIDiator software is based on Linux and optimized for RAID applications. It supports RAID levels 0, 1, and 5, plus a proprietary RAID level called xRAID, for which Infrant has applied for a U.S. patent. With xRAID, users can add disks without manually reconfiguring the array. RAIDiator also supports hot swapping and hot spares. The latter feature allows users to designate one drive as a backup that automatically joins the RAID if another drive fails.

RAIDiator is much more than an embedded OS. It also provides a user-level configuration and management tool that runs inside a browser window, with step-by-step wizards for common tasks as well as an advanced-user mode. The management program runs on Windows, Macintosh, Linux, and Unix systems; has multiple levels of security (including separate passwords for user accounts); supports multiple clients; and automatically sends email messages to the user's mailbox if the subsystem detects a disk error.

In the past, OEMs would have written their own software such as RAIDiator. Now, many OEMs expect suppliers to provide near-finished designs with system boards and software. Consequently, Infrant employs more than twice as many software programmers as hardware engineers, despite the extra design effort required to create its custom processor core. The IT3107 and ExpandaNAS board provide a

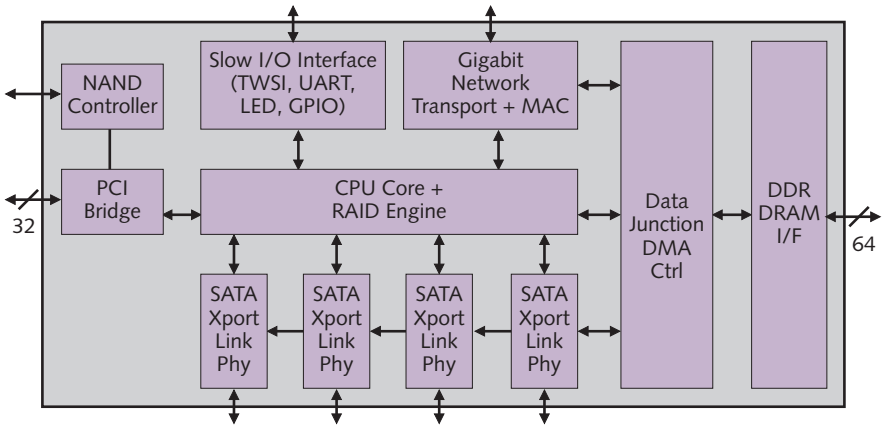

Figure 1. Infrant IT3107 block diagram. This network storage controller has two 32-bit RISC cores derived from the synthesizable LEON1 core freely licensed by the European Space Agency. Additional IP makes it a specialized chip for network-attached storage (NAS) applications. One processor core is the CPU, which runs embedded RAID software, and the other core is in the DataJunction DMA controller.

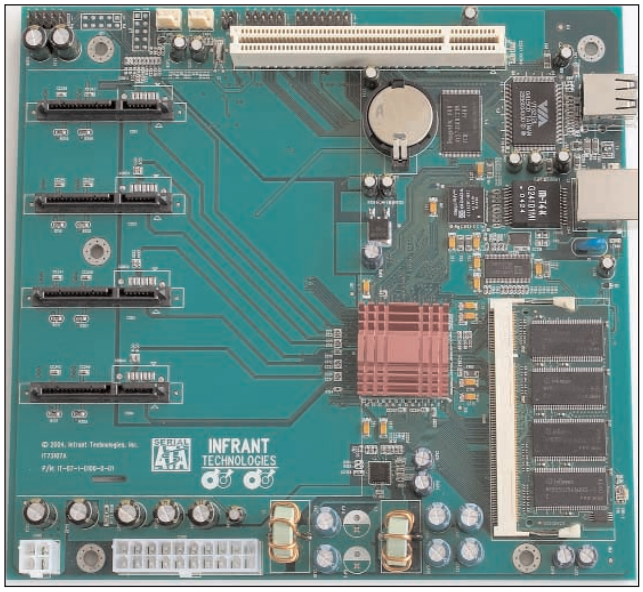

Figure 2. Infrant's ExpandaNAS system board comes populated with an IT3107 processor (beneath a heatsink, slightly lower-right of center), 128MB of SO-DIMM memory (lower right), and the RAIDiator software embedded in on-board flash memory (upper right). A long-life battery (near the PCI slot, at top) powers a real-time clock for RAID event logging and time stamping. Four slots for SATA disk drives are at left. The system board is mostly empty to leave room for hot-swapping the drives. To make a RAID box for NAS, just about all an OEM must add is some industrial design.

turnkey OEM solution. Figure 2 is a photo of Infrant's ExpandaNAS system board as offered to customers.

Weighing the Design Trade-Offs

Licensing a processor core from a commercial IP vendor would have been faster than designing a custom processor core, even after borrowing the LEON1 integer unit. However, because the custom core is a relatively simple RISC design, Infrant believes the time devoted to the project wasn't excessive. Infrant's president and CEO Paul Tien estimates the custom core required about two man-years to design and perhaps ten man-years to debug and verify, with four hardware engineers working full time. (Meanwhile, more than ten programmers were busy writing RAIDiator.)

Had Infrant licensed a suitable processor from a commercial IP vendor, the core would have been ready to use off the shelf. Licensable-IP cores are preverified, so the engineers would have saved time during that part of the project, too, although the whole chip design would still require verification. Infrant says it preferred SPARC to other licensable architectures, but the company could have started with a customizable processor from ARC, MIPS, or Tensilica and added the application-specific features needed. (Tensilica's Xtensa processors even have SPARC-like register windows.) The main trade-off is whether the cost of licensing commercial IP would exceed the revenue lost by reaching the market later.

Ownership is another potential issue. LEON1 is covered by the GNU Lesser General Public License (LPGL), a variation of the GNU General Public License (GPL). Under the terms of the LPGL, users can freely modify the LEON1 source code and combine it with their own code to produce a derivative work. They needn't publish the source code of other IP combined with LEON1, but they are obligated to publish any modifications to the free core. With the IT3107, the demarcation between LEON1 source code and proprietary source code should be clear: LEON1 is in VHDL, and Infrant wrote everything else in Verilog. Infrant is obligated to publicly share only the VHDL of the slightly modified LEON1 integer unit.

Microprocessor Report believes Infrant made a reasonable trade-off by designing a custom processor core—at least on this occasion. The time-to-market disadvantage is less important for a young company trying to establish itself in a new market. Convincing home and small-business users they need a networked RAID subsystem and can manage it themselves will probably take more effort than Infrant's design project did.

However, in a more established market, in which eager customers are lining up at the door of a more established company, licensing a commercial processor core is usually more sensible. Commercial IP cores are expensive, but they are also preverified, have better hardware/software-design tools, run more embedded operating systems, come with expert technical support, and are verified to work with libraries of other IP. If Infrant someday outgrows its homemade processor core, we won't be surprised to see the company open its checkbook and license a processor from a commercial IP vendor. ◇

Price & Availability

Infrant is shipping the IT3107 network storage processor now, as well as the ExpandaNAS system boards and RAIDiator embedded software. In 1,000-unit quantities, the IT3107 costs $120, including a RAIDiator license. A nearly identical chip, the IT3102, supports only two-channel SATA instead of four-channel SATA and costs $80. For more information, visit *www.infrant.com*.

For more information about LEON from the European Space Agency, visit *www.estec.esa.nl/wsmwww/core/soc.html*. For information about LEON2 and LEON3, newer versions of the LEON core, see *www.gaisler.com*. For information about the GNU Lesser General Public License, see *www.gnu.org/copyleft/lesser.html*.