3C87 Numeric Coprocessor

OVERVIEW

The IIT-3C87 is a high performance numeric co-processor that is plug and object-code compatible with the Intel 80387, and operates up to 50% faster in the same socket and at the same clock rates. The unique architecture of the IIT-3C87 requires far fewer co-processor clock cycles to perform the various math operations, resulting in superior performance in the same socket as the Intel 80387, yet maintains full software compatibility with the Intel 80387. Device Icc is 25% less than required by the Intel 80387 when operating under the same conditions, resulting in lower junction temperatures and consequently higher reliability.

- ☐ High performance 80-bit architecture
- ☐ Plug and object-code compatible with the 80387
- ☐ Up to 50% faster than the 80387
- ☐ CMOS implementation requires 25% less power than the 80387
- ☐ Thirty-two registers, three banks of eight available to the user
- ☐ Upward object-code compatible with the 8087 and 80287
- ☐ Implements ANSI/IEEE standard for binary floating point arithmetic
- ☐ Full range transcendental operations for sine, cosine, tangent, arctangent and logarithm
- ☐ Runs all 80387 software
- ☐ Available at 16, 20 and 25 MHz

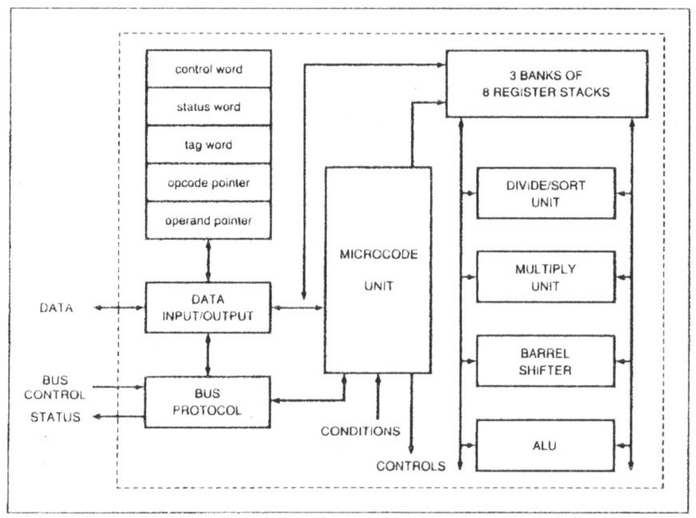

Figure 1. IIT-3C87 Block Diagram

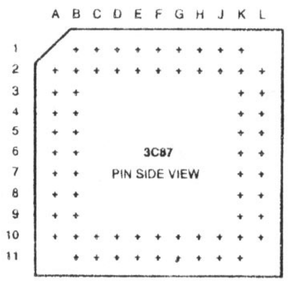

TABLE 1. 3C87 PIN CROSS REFERENCE

A2-D9	B3-D10	C10-D23	F2-V_{SS}	J1-V_{SS}	K9-NoConnect
A3-D11	B4-V_{CC}	C11-V_{SS}	F10-V_{CC}	J2-V_{CC}	K10-CPUCLK2
A4-D12	B5-D13	D1-D5	F11-V_{SS}	J10-V_{SS}	K11-NUMCLK2
A5-D14	B6-D15	D2-D4	G1-D3	J11-CKM	L2-ERROR#
A6-V_{CC}	B7-V_{SS}	D10-D24	G2-D2	K1-PEREQ	L3-READYO#
A7-D16	B8-D17	D11-D25	G10-D28	K2-BUSY#	L4-STEN
A8-D18	B9-D19	E1-V_{CC}	G11-D29	K3-Tie High	L5-V_{SS}
A9-V_{CC}	B10-D20	E2-V_{SS}	H1-D1	K4-W/R#	L6-NPS1#
A10-D21	B11-D22	E10-D26	H2-D0	K5-V_{CC}	L7-V_{CC}
B1-D8	C1-D7	E11-D27	H10-D30	K6-NPS2	L8-CMDO#
B2-V_{SS}	C2-D6	F1-V_{CC}	H11-D31	K7-ADS#	L9-Tie High
				K8-READY#	L10-RESETIN

ENHANCED PERFORMANCE

The IIT-3C87 numeric co-processor is available in speeds of 16, 20, and 25 MHz. The unique architecture of the device requires far fewer co-processor clock cycles for instruction execution. The result is a device which operates up to 50% faster than the 80387 in the same application. Table 2 compares the range of clock cycles required to perform typical floating point instructions.

TABLE 2. CLOCK CYCLES REQUIRED

INSTRUCTION	IIT-3C87	80387
ADD	11	31
MPY	15	57
DIV	44	88
SQRT	45	125
REM	54	155
TAN	192	726

FUNCTIONALITY

The IIT-3C87 is plug and object-code compatible with the Intel 80387 and is capable of running all software designed to support the 80387.

The IIT-3C87 provides extra functions which are not available on the 80387.

There are thirty-two 80-bit registers, 24 of which are available to the user as three stacks of eight registers.

FEATURES:

CMOS IMPLEMENTATION

The IIT-3C87 is implemented in 1.2 micron CMOS (16 and 20 MHz), and 1.0 micron CMOS technology (25 MHz). Device dissipation is typical at 0.6 Watt. The advantage is lower power dissipation than the Intel 80387 with corresponding improvement in reliability.