Preface

Objectives

This document provides an overview and specifications for all orderable VCO/4K network and service circuit cards.

Audience

This guide is designed for personnel assigned to the task of setting up, installing, or maintaining VCO/4K hardware.

Conventions

This document uses the following conventions:

Note Means *reader take note.* Notes contain helpful suggestions or references to material not covered in the manual.

Caution Means *reader be careful.* In this situation, you might do something that could result in equipment damage or loss of data.

Warning **Warning Means *danger.* You are in a situation that could cause bodily injury. Before you work on any equipment, you must be aware of the hazards involved with electrical circuitry and be familiar with standard practices for preventing accidents. To see translated versions of the warning, refer to the *Regulatory Compliance and Safety* document that accompanied the device.**

Tips Means *the following information will help you solve a problem.* The tips information might not be troubleshooting or even an action, but could be useful information.

Related Documentation

Related documentation includes:

- *Cisco VCO/4K System Administrator's Guide*
- *Cisco VCO/4K Extended Programming Reference*
- *Cisco VCO/4K Software Installation Guide*
- *Cisco VCO/4K Hardware Installation Guide*

Obtaining Documentation

The following sections provide sources for obtaining documentation from Cisco Systems.

World Wide Web

You can access the most current Cisco documentation on the World Wide Web at the following sites:

- http://www.cisco.com
- http://www-china.cisco.com
- http://www-europe.cisco.com

Documentation CD-ROM

Cisco documentation and additional literature are available in a CD-ROM package, which ships with your product. The Documentation CD-ROM is updated monthly and may be more current than printed documentation. The CD-ROM package is available as a single unit or as an annual subscription.

Ordering Documentation

Cisco documentation is available in the following ways:

- Registered Cisco Direct Customers can order Cisco Product documentation from the Networking Products MarketPlace:

  http://www.cisco.com/cgi-bin/order/order_root.pl

- Registered Cisco.com users can order the Documentation CD-ROM through the online Subscription Store:

  http://www.cisco.com/go/subscription

- Nonregistered Cisco.com users can order documentation through a local account representative by calling Cisco corporate headquarters (California, USA) at 408 526-7208 or, in North America, by calling 800 553-NETS(6387).

Documentation Feedback

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You can e-mail your comments to bug-doc@cisco.com.

To submit your comments by mail, for your convenience many documents contain a response card behind the front cover. Otherwise, you can mail your comments to the following address:

Cisco Systems, Inc.
Document Resource Connection
170 West Tasman Drive
San Jose, CA 95134-9883

We appreciate your comments.

Obtaining Technical Assistance

Cisco provides Cisco.com as a starting point for all technical assistance. Customers and partners can obtain documentation, troubleshooting tips, and sample configurations from online tools. For Cisco.com registered users, additional troubleshooting tools are available from the TAC website.

Cisco.com

Cisco.com is the foundation of a suite of interactive, networked services that provides immediate, open access to Cisco information and resources at anytime, from anywhere in the world. This highly integrated Internet application is a powerful, easy-to-use tool for doing business with Cisco.

Cisco.com provides a broad range of features and services to help customers and partners streamline business processes and improve productivity. Through Cisco.com, you can find information about Cisco and our networking solutions, services, and programs. In addition, you can resolve technical issues with online technical support, download and test software packages, and order Cisco learning materials and merchandise. Valuable online skill assessment, training, and certification programs are also available.

Customers and partners can self-register on Cisco.com to obtain additional personalized information and services. Registered users can order products, check on the status of an order, access technical support, and view benefits specific to their relationships with Cisco.

To access Cisco.com, go to the following website:

http://www.cisco.com

Technical Assistance Center

The Cisco TAC website is available to all customers who need technical assistance with a Cisco product or technology that is under warranty or covered by a maintenance contract.

Contacting TAC by Using the Cisco TAC Website

If you have a priority level 3 (P3) or priority level 4 (P4) problem, contact TAC by going to the TAC website:

http://www.cisco.com/tac

P3 and P4 level problems are defined as follows:

- P3—Your network performance is degraded. Network functionality is noticeably impaired, but most business operations continue.
- P4—You need information or assistance on Cisco product capabilities, product installation, or basic product configuration.

In each of the above cases, use the Cisco TAC website to quickly find answers to your questions.

To register for Cisco.com, go to the following website:

http://www.cisco.com/register/

If you cannot resolve your technical issue by using the TAC online resources, Cisco.com registered users can open a case online by using the TAC Case Open tool at the following website:

http://www.cisco.com/tac/caseopen

Contacting TAC by Telephone

If you have a priority level 1(P1) or priority level 2 (P2) problem, contact TAC by telephone and immediately open a case. To obtain a directory of toll-free numbers for your country, go to the following website:

http://www.cisco.com/warp/public/687/Directory/DirTAC.shtml

P1 and P2 level problems are defined as follows:

- P1—Your production network is down, causing a critical impact to business operations if service is not restored quickly. No workaround is available.
- P2—Your production network is severely degraded, affecting significant aspects of your business operations. No workaround is available.

CHAPTER 1

VCO/4K Card Overview

The *Cisco VCO/4K Card Technical Descriptions* describe the following types of cards used in a VCO/4K system:

- Control circuit cards are used in system controllers. System controllers provide database management, program load and startup, basic call processing functions, maintenance and administration access, host control and peripheral device interfaces.
- Port interface cards provide incoming and outgoing interfaces between the system and the switched network.
- Service circuit cards provide special facilities that can be accessed by network interface ports.

Each technical description in this series reflects the most current information available about the product. The information contained in a technical description is specific to a single component within a VCO/4K system. Other system documents point to technical descriptions as containing the most detailed information available for a component.

A technical description contains information to service and maintain the component. For system-level servicing, refer to the *Cisco VCO/4K System Maintenance Manual*. The maintenance manual assists in isolating the cause of a system malfunction and serves as a pathfinder to the more detailed information contained in technical descriptions.

Note This document represents the most current information about VCO/4K network and service circuit cards. If you need information pertaining to VCO/4K assemblies, circuit cards, or other components that are not included in this document, see the following URL on Cisco's web site for legacy VCO/4K information:
http://www.cisco.com/univercd/cc/td/doc/product/tel_pswt/index.htm

Card Removal and Replacement Procedures

Caution Read all instructions before attempting to remove or replace a card. To minimize the risk of injury from hazardous voltages, avoid contact with the backplane when removing or replacing system cards. Observe antistatic precautions when handling a card to avoid damaging sensitive CMOS devices. Wear a ground strap connected to the system equipment frame whenever removing or replacing cards or I/O modules.

All port interface, service circuit and international cards can be safely removed and replaced with the system powered up and operating normally.

The card should be in an out-of-service (OOS) status, however, to assure that in-progress calls are not affected when the card is removed from the port subrack.

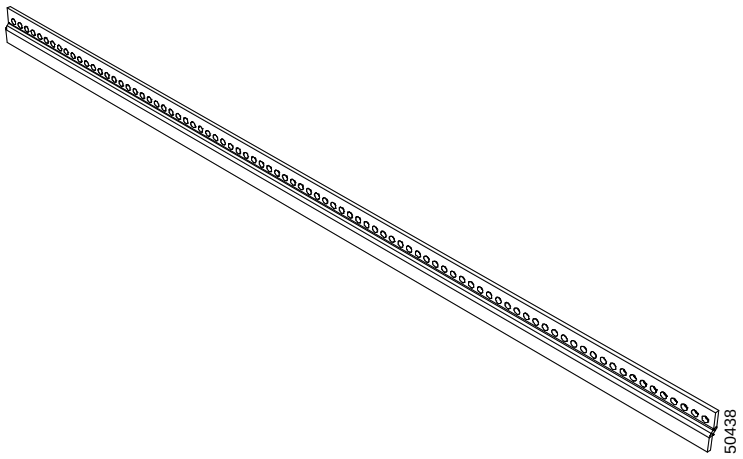
Removing a Card

Perform the following steps to remove a system card from a card slot:

Step 1 Go to the Maintenance menu and then select Card Maintenance to change the status of the card to OOS. Wait for the green LED on the card's front panel to illuminate before removing the card from the card slot.

Step 2 Use a #1 Phillips-head screwdriver to remove the mounting screws/washers from the top and bottom PCB card retainer bars (see Figure 1-1) on the system. Keep the retainers and screws together in a safe place for replacement later.

Figure 1-1 PCB Card Retainer Bar



Step 3 Use your thumbs to push the upper and lower ejectors away from the desired card front panel. This action will pop the card from the backplane connectors.

Note Remove and replace the card using only enough force to disengage or engage the card from or into backplane connectors. Yanking cards from, or jamming cards into, the backplane can seriously damage connectors and result in operating problems which will be very difficult to isolate.

Step 4 With both hands, grasp the card on its top and bottom edges as you remove it from the card slot. Pull the card from the card slot.

Step 5 Place the card on an antistatic mat or envelope.

Caution If your system arrived with blank card assemblies (blank faceplate and blank metal blade) installed, these assemblies must remain in their original locations, unless you replace them with a functional system card. These blank card assemblies are carefully configured to compartmentalize the system for safety reasons and are critical to maintain NEBS GR-63-CORE compliance.

Replacing a Card

Perform the following steps to replace a system card in a card slot:

Step 1 Place the replacement card next to the removed card on the antistatic mat or envelope.

Step 2 Verify that all the switch and jumper settings on the replacement card correspond with those on the removed card.

Note Refer to your release notes and verify that the revision levels of the PROMs match the requirements of the generic software currently loaded in your VCO/4K system.

Step 3 With both hands, grasp the replacement card on its top and bottom edges and align it with the top and bottom card guides of the card slot.

Step 4 Push the card inward until it makes initial contact with the backplane.

Make sure the ejector levers are perpendicular to the front panel. Continue pushing the card inward until it makes firm contact with the backplane. The hooks on the ejectors must be behind the front rail of the card slot. Use your thumbs to push the ejectors inward toward the front panel. The card should be fully seated into the backplane connectors when the levers are flush against the front panel.

Note Most cards are automatically brought into service when you replace them in the port subrack; an appropriate system message is displayed on the master console and logged in the system error log. Cards can take up to 5 minutes, however, to initialize and become active. If a card fails to come into service within an appropriate amount of time, use the Card Maintenance submenu and the Change Status command to place the card in Active status.

Step 5 Reinstall the top and bottom PCB card retainer bars (see Figure 1-1). Use a #1 Phillips-head screwdriver to replace the mounting screws/washers.

Caution The PCB card retainer bars must be installed for the system to meet NEBS Zone 4 Earthquake compliance.

Tips If you are experiencing difficulties with ICC or SPC installation, the following helpful tip may improve installation. When sliding the ICC or SPC into position along the card guide, gently touch the card to the midplane connector. Push lightly on the right side of the card's faceplate and apply slight pressure until you feel the connectors engage. This will ensure a proper fit and midplane interconnection.

Removing an ICC I/O Module

Perform the following steps to remove an I/O Module card from a card slot.

Note Network connections may be disconnected before or after card removal.

Step 1 Take all spans OOS from the Card Maintenance menu.

Step 2 Disconnect the corresponding ICC card from the front of the switch.

Step 3 From the back of the system, unscrew the top and bottom fasteners for the I/O Module.

Note Remove and replace cards using only enough force to disengage or engage the card from or into backplane connectors. Yanking cards from, or jamming cards into, the backplane can seriously damage connectors and result in operating problems which will be very difficult to isolate.

Step 4 Remove the I/O Module and place it on an antistatic mat or envelope.

Replacing an ICC I/O Module

Note The I/O Module must be inserted in the system before the ICC card. The network connections on the I/O Module can be made prior to or following the ICC card insertion.

Perform the following steps to replace an I/O Module in a card slot.

Step 1 Set the replacement card on the antistatic mat or envelope.

Step 2 If there is one in the system, remove the associated ICC card.

Step 3 With both hands, grasp the replacement I/O Module card on its top and bottom edges and (at the back of the system) align it with the top and bottom card guides of the subrack.

Step 4 Push the card inward until it touches the back side of the port subrack backplane. Apply additional pressure to the card to ensure that it is seated. Tighten the mounting screws.

Step 5 Replace the ICC card at the front of the system.

Card Specifications

Part Number	Contact your Cisco Systems sales representative	
Operating Temperature	10 to 40°C (50 to 104°F)	
Relative Humidity	20 to 80% (noncondensing); temperature rise or fall should not exceed 10°C (18°F) per hour	
Physical Dimensions: Port Interface, Service Circuit, and International Cards	**Standard Card**	**ICC I/O Module**
	Height: 15.6 in. (396 mm)	Height: 14.5 in. (368 mm)
	Depth: 12.1 in. (307 mm)	Depth: 5.8125 in. (148 mm)
	Width: 0.79 in. (20 mm)	Width: 0.79 in. (20 mm)
	(9U Eurocard form factor)	

Troubleshooting

This section describes how to detect and correct common problems associated with port interface and service circuit cards.

System Log Error and Status Messages

System and card error messages appear on the System Alarm Display and Card Alarm Display screens, respectively, when a major or minor alarm condition occurs. The message provides the rack-level-slot address of the suspect card.

In addition to illuminating appropriate status LEDs, all system and card alarm conditions are appropriately identified in the log, such as CARD ALRM SET, CARD ALRM CLRD, MIN ALARM SET, MIN ALRM CLRD.

Messages are written to the system error log and output to the system printer. Messages are time stamped by day of week (according to the setting of the system clock/calendar), and identified according to which system controller generated the message. Refer to the *Cisco VCO/4K System Messages* for a list of error messages and their meanings.

Note Refer to the *Cisco VCO/4K System Maintenance Manual* for information on how to use system logs to isolate issues within a system.

Service Circuit Test Utility

The Generic administrative software includes a Service Circuit Test Utility you can use to test individual circuits on service circuit cards. You can test any or all receiver ports on the same card with a single command. Ports are tested in sequential order from the start port specified to the end port specified. You can also set this test to loop repeatedly, testing ports sequentially over and over.

When you test a service circuit card, the SPC presents dial tone, ringback, ringback cessation, busy, and reorder tone events to the card port(s) for detection. Any discrepancy between the presented tone and the reported detection results in the port(s) failing the test. Logfile and system printer error messages specify the port's address and the type of tone it failed to detect.

You can use a port on a line/trunk or receiver port to monitor the test. This port monitors the link between the service circuit being tested and the resource providing test digits or tones. Monitoring the digits and tones being passed allows you to determine the exact point of test failure.

You must place the card on which the receiver ports reside in Diagnostic mode before it can be tested. If any ports are active when the card is placed in Diagnostic mode, the card automatically switches to Camped On mode. The Service Circuit Test function can be run on a service circuit card in Camped On mode; the test skips any nonidle ports on the card.

Refer to the *Cisco VCO/4K System Administrator's Guide* for further information on accessing and using the Service Circuit Test Utility.

Test MF Receivers

From the Diagnostics menu, you can select the DTMF /MF Receiver Tests screen to perform port tests on SPC-MF receivers.

Note Use the Card Maintenance menu under the Maintenance menu to place the desired receiver card(s) in Diagnostic (D) mode. This Test Receiver function will not work unless the card has been placed in Diagnostic mode.

Observe the cautionary note on the screen about specifying start and end ports for the tests. When you have entered the start and end ports, press **Enter** to begin the tests.

A message indicating which port is being tested appears on the bottom of the screen. As testing of each port is completed, a status message indicating the result of the test is displayed on the screen and sent to the system printer.

Detecting and Correcting T1, T1-E, E1, E1-PRI, and PRI/N Problems

Factors which cause major alarm indications include:

- Loss of carrier
- Failure of internal communications bus test (card self-test)
- Card out-of-service (manually via master console or due to a communication bus error)
- T309 expiring (default = 90 seconds) – D-channel failure (E1-PRI or PRI/N)

Factors which cause minor alarm indications include:

- Remote alarm
- Slip maintenance threshold reached
- Out-of-Frame (OOF) condition
- Out-of-Frame (OOF) maintenance threshold reached
- Loss-of-frame (LOF) condition
- LOF maintenance threshold reached

Loss of carrier can be attributed to a fault in the span line or a failure of the digital side of the channel bank. Loss of synchronization can either be related to problems with the T1, T1-E, E1, E1-PRI, or PRI span line providing external sync with the system, an external sync pulse source connected to the NBC3, or NBC3/T1, T1-E, E1, E1-PRI, or PRI phase lock timing.

Verify channel bank operation and the span line connection before removing and replacing any cards. Loss of a channel may be the result of problems on the originating side of the channel bank/digital switch.

Network Card Maintenance States

Network cards may be operating in any of four states—Active, Maintenance, Out-of-Service, or Diagnostic. These maintenance states are described below.

Active State

This is the normal operational state. No alarms are being sent outward on the T1, T1-E, E1, E1-PRI, or PRI stream and no front panel LEDs are illuminated. However, individual ports on the card may be placed in the Out-of-Service state using system Maintenance Menus (refer to the *Cisco VCO/4K System Administrator's Guide* for more information).

Maintenance State

In this state, the system has stopped call processing because of an alarm received from the far end or from internal processing and may be presenting alarms to the far end of the T1, T1-E, E1, E1-PRI, or PRI stream. This state is automatically triggered by the system when an inward T1, T1-E, E1, E1-PRI, or PRI alarm is present.

A card placed into the Maintenance state by alarm processing will continue calls in progress. No new calls will be accepted. All idle channels will be put into the Maintenance Near End state. As channels become idle, they are put into the Maintenance Near End state.

The card is also automatically placed into Maintenance state while the E1-PRI or PRI/N application software is downloaded. Cards can be placed into Maintenance mode manually via the system administration console.

Out-of-Service State (OOS)

In this state, call processing is stopped. E1-CAS sends Blocked signals on all channels. T1, T1-E, E1-PRI, and PRI/N send an unframed, all-ones (1s) signal to the far end, triggering an OOF alarm.

Diagnostic State

In this manually enabled state, the system stops call processing of all ports on the network card to allow the Test Port Card function to be run. The card is set to local loopback (Diagnostic state). E1-CAS sends Blocked signals on all channels. T1, T1-E, E1-PRI, and PRI/N send an unframed, all-ones (1s) signal to the far end, triggering an OOF alarm. These LOF or OOF conditions cause the far end to remove the trunk from service. The cards can also be set to remote loopback (Remote Loopback state). Refer to the *Cisco VCO/4K System Administrator's Guide* for more information on using diagnostics and changing card states.

Note When the NFAS option is used, additional processing states for the Primary/Backup D-channels are supported. These states can be changed using the NFAS Group Configuration screen. Refer to the *Cisco VCO/4K ISDN Supplement* for complete information on NFAS support.

Error Conditions Detected on Incoming Stream

The switch detects several types of error conditions on incoming streams. All cause a major or minor alarm on the Alarm Arbiter Card (AAC).

Yellow Alarm (Remote Alarm Indication)

A Yellow Alarm occurs when zeros appear in the Bit 2 position of all channels in the T1 or T1-E received bit stream, a Remote Alarm Indication (RAI) signal is found in the E1 received bit stream, or 8 ones [1s] are followed by 8 zeros in the E1-PRI or PRI received bit stream. This condition usually indicates a loss of carrier or OOF at the far end. The yellow LED on the card illuminates, a minor alarm is triggered, and the T1, T1-E, E1, E1-PRI, or PRI/N card transitions to the maintenance state. The card automatically returns to Active when the remote carrier alarm clears.

Remote Multiframe Alarm Condition

A Remote Multiframe Alarm condition (also known as a Distant Multiframe Alarm [DMA]) occurs when the Loss of Multiframe Alignment signaling bit in timeslot 16 is set to 1 in the received bit stream. This condition indicates the distant end cannot detect a proper multiframe alignment pattern. The yellow LED on the card illuminates, a minor alarm is triggered, and the card transitions to the maintenance state. The card automatically returns to Active when the DMA clears.

Signaling Bit Alarm

Onhook/offhook information is passed within the T1 stream via “robbed” bit signaling. Every sixth frame, the least significant bit (LSB) of all 24 PCM samples is replaced by a bit representing either the A- or B-signaling bit for that channel. The representation of signaling Bit A and signaling Bit B information alternates every sixth frame. A superframe consists of 12 frames of PCM data containing one Bit A signaling bit and one Bit B signaling bit.

The system monitors the T1 stream looking for repetitive A/B bit patterns. The F_t (terminal framing) and F_s (signaling framing) patterns are defined in *Bell PUB 43801 Digital Channel Bank Requirements And Objectives*. When the F_s pattern is not detected, the system triggers a signaling bit alarm. This is an unusual condition in that an OOF condition and signaling bit alarm will most likely occur together, and an OOF alarm takes precedence over a signaling bit alarm.

The red LED is illuminated, a minor system alarm is triggered, and the card goes into maintenance state. It returns to Active automatically when the condition clears.

Slip

A slip occurs whenever the system clock source frequency differs from the clock recovered from the inward stream. A slip report (either receive or transmit) increments an internal counter which is monitored by the Generic software. When a programmable threshold of slip reports (default=255) are received within a 24-hour period, the system sets a minor alarm. The system automatically places the card in the maintenance state if the MANUAL INTERVENTION FOR SLIP/OOF feature flag is set to Y. The card stays in the maintenance state until you take the card Out-of-Service and then place it back into Active service through the Card Maintenance menu. In either case, the Maintenance Threshold alarm stays on until you manually clear it.

Loss of Carrier

A carrier loss is detected when there are an insufficient number of stream bit transitions from which a clock can be recovered. The error condition automatically places the card in the maintenance state and sends a Yellow Alarm (zeros in Bit 2 of all channels for T1 or T1-E, or 8 ones [1s] followed by 8 zeros for E1-PRI or PRI/N) to the far end of the stream and busies out all trunks. The red LED is illuminated on the front panel of the card and a major system alarm is triggered.

Out-of-Frame (OOF)

An OOF condition is reported when the Frame bit (Bit 193) is lost for a period longer than 2.5 seconds. An OOF report increments an internal counter which is monitored by the system software. The red LED on the card is illuminated (Red Alarm), a minor system alarm is triggered, the card goes to the maintenance state; a Yellow alarm is sent to the far end.

When a programmable threshold of OOF reports are received (T1=4) within a 24-hour period, the system sets an OOF Maintenance Threshold alarm. If the MANUAL INTERVENTION FOR SLIP/OOF feature flag is set to Y, the card stays in the maintenance state until you place the card back into Active service (using the Card Maintenance menu). The red LED remains on until the OOF condition clears. If the MANUAL INTERVENTION FOR SLIP/OOF feature flag is set to N, the card remains in the maintenance state only until the OOF condition clears, then returns to Active automatically. In either case, the Maintenance Threshold alarm stays on until cleared manually.

Loss-of-Frame (LOF)

An LOF condition is reported when an individual frame alignment pattern is not detected within 12 to 14 milliseconds. An LOF report increments an internal counter which is monitored by the system software. The red LED on the card is illuminated, a minor system alarm is triggered, and the card goes to the maintenance state; a Remote Alarm Indication (RAI) is signaled to the far end.

When four LOF reports are received within a 24-hour period, the system sets an LOF Maintenance Threshold alarm. If the MANUAL INTERVENTION FOR SLIP/OOF feature flag is set to Y, the card stays in the maintenance state until you use the Card Maintenance Menu to place the card back into Active service. The red LED remains on until the LOF condition clears. If the MANUAL INTERVENTION FOR SLIP/OOF feature flag is set to N, the card remains in the maintenance state only until the LOF condition clears; then returns to Active automatically. In either case, the Maintenance Threshold alarm stays on until cleared manually.

CHAPTER 2

Control Circuit Cards

Alarm Arbiter Card (AAC) with Alarm Interface Card (AIC)

The Alarm Arbiter Card (AAC) is the central control point for system resets and alarm indication. The AAC is mounted at the top of the VCO/4K as shown in Figure 2-1. Switches on the front panel enable system controller resets and select which system controller is to be master. Status LEDs indicate the currently enabled system controller and major/minor alarms.

The AAC is attached to the Alarm Interface Card (AIC). The AIC accepts fault signals from the VCO/4K Power Subsystem, Fan Unit, and Ring Generator, and generates a single fault signal to the AAC. The AIC also conditions the fault signals for the AAC. Figure 2-2 shows the location of the AAC and AIC.

In VCO/4K applications, the host computer can set any of the alarms by software command. The VCO/4K may also support components which feature programmable alarm severity.

For a complete listing of system alarms supported by Generic software, refer to the *Cisco VCO/4K System Administrator's Guide.*

Figure 2-1 AAC Location

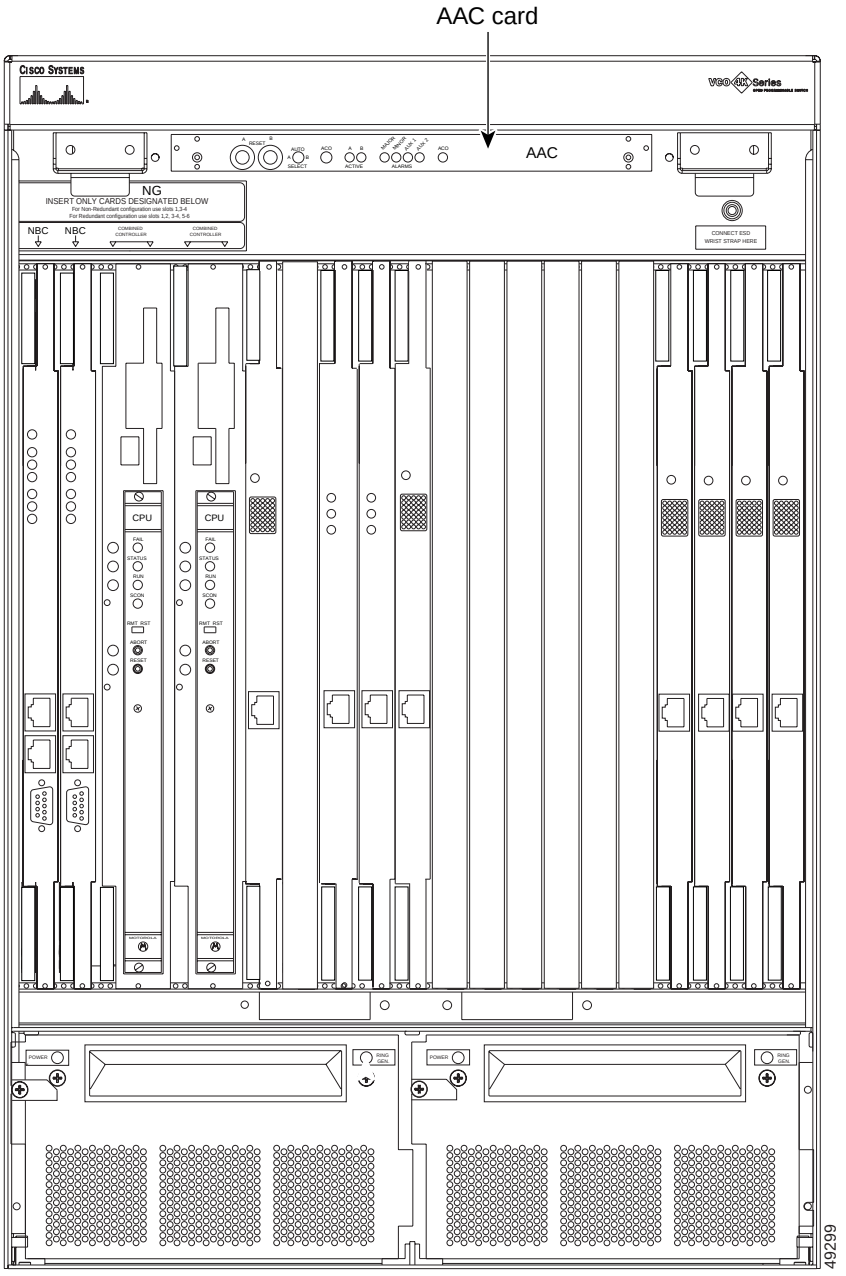
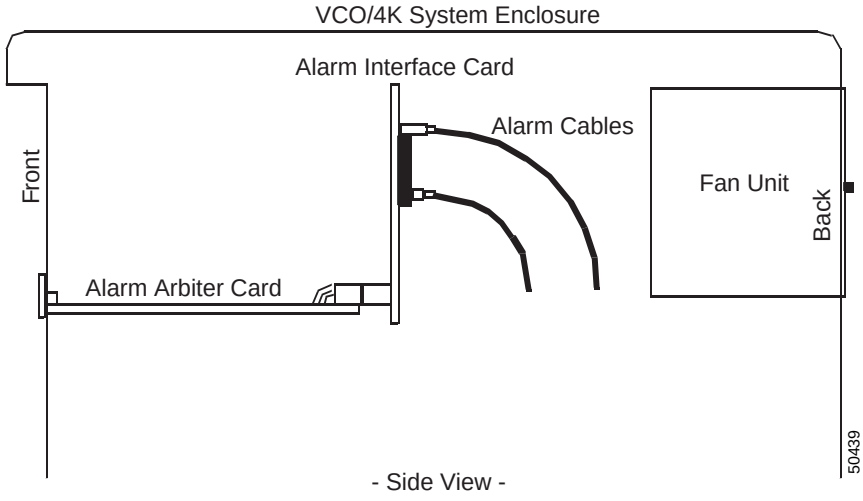


Figure 2-2 Location of the AAC and AIC



Specifications

Alarm Arbiter Card

Watchdog Timer Parameters:

After Reset/Power up: 5 – 7 minutes

Normal operation: 5 – 10 seconds

Alarm Types:

MAJOR, MINOR, AUX 1, AUX 2

Visual indicators on AAC front panel

External NO and NC relay contacts provided for each alarm

External Contacts Type = 2 Form C

Rating = 0.5A @ 24 VDC, 0.25A @ 120VAC (Resistive load only)

Power Requirements: +12 VDC @ 1A

Physical Dimensions	Height:	6.3 in. (160 mm)
	Width:	9.2 in. (234 mm)
	Depth:	0.631 in. (16 mm)

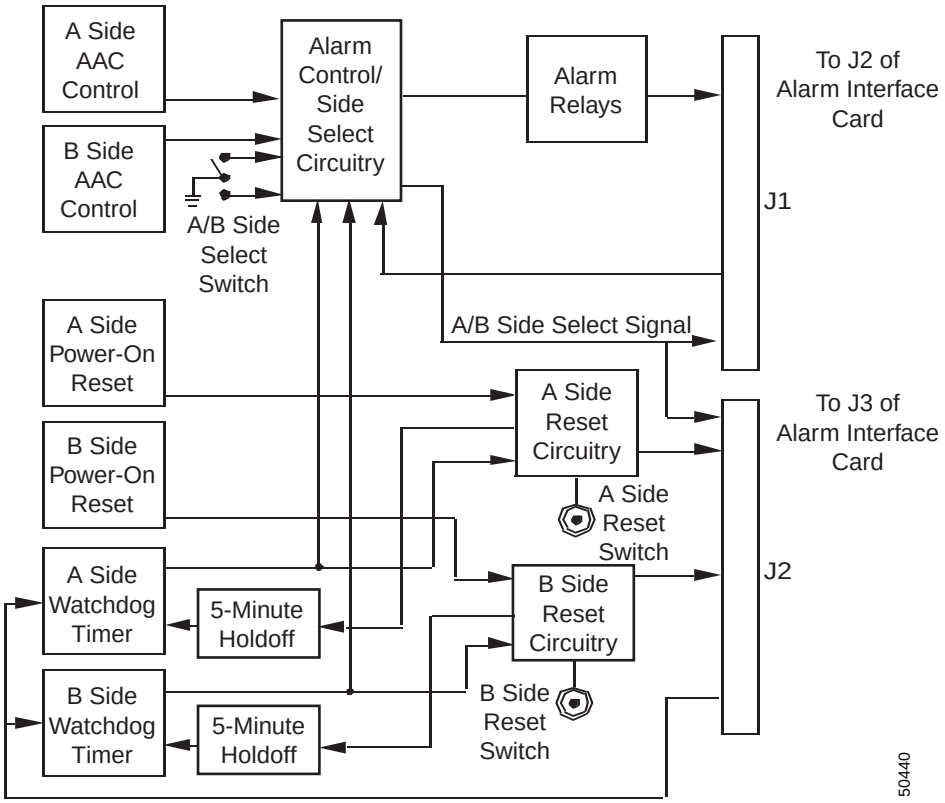
Alarm Interface Card

Power Requirements:	+5 VDC @ 0.2A (redundant)	
Physical Dimensions	Height:	2.75 in. (70 mm)
	Width:	14.75 in. (374 mm)
	Depth	.0631 in. (16 mm)

AAC Circuit Description

The AAC is the hardware interface point for manual and automatic bus resets and alarms. It also functions as a control point for the selection of system controllers in systems equipped with redundant control. Power reset and watchdog timer circuitry is duplicated for A-side and B-side system controllers in VCO/4K systems to minimize possible system effects of AAC failures. Figure 2-3 is a simplified block diagram of the AAC.

Figure 2-3 Block Diagram of the AAC



Watchdog Timer Circuit

The AAC includes independent watchdog timer circuits for both A-side and B-side system controllers. These timers reset a controller's side within 5 seconds if the controller does not provide a tick every 5 seconds.

The watchdog timer for a particular system controller is disabled for approximately 5 minutes after that side is reset with the AAC. The watchdog timer is also disabled for a particular controller side if the other system controller is selected with the SELECT switch on the AAC front panel.

Switching from Active to Standby

The AAC monitors the status of both system controllers and switches active controllers if one of the following conditions occurs:

- Combined Controller Assembly on the Active controller is not available
- Active side watchdog timer expires
- Active side sets an internal AAC signal to indicate that it is offline
- Active controller software requests a switch from Active to Standby

For the switchover to occur, the following conditions must be true:

- Front Panel SELECT switch is in the AUTO position
- NBC3 on the Standby controller is present
- Watchdog timer on the Standby controller has not expired
- Standby controller has set the internal AAC signal to online (file synchronization has successfully completed)

It may take up to one second for the actual switchover to occur. Use the front panel SELECT switch to immediately force a switchover, regardless of the state of the Standby controller. However, make sure you use this type of switchover only in an emergency; database sanity checks are *not* performed.

Note Cisco Systems strongly recommends using the Maintenance Menu to force a switchover. Refer to the *Cisco VCO/4K System Administrator's Guide* for more information.

Front Panel Switches

On the left side of the front panel are two push-button switches labeled RESET A and RESET B (refer to Figure 2-4). Press RESET A to reinitialize the A-side (left) controller; press RESET B to reinitialize the B-side (right) controller.

The SELECT switch is a three-position toggle switch that determines which controller in a redundant control system is currently active. The AUTO setting works for nonredundant and redundant control systems. In nonredundant control systems, the A-side is always active. SELECT A makes the system controller on the left (front view) active; SELECT B makes the right system controller active.

Manually selecting one side disables the watchdog timer of the other side. However, if the manually selected controller should fail, automatic switchover will not be performed. With redundant control systems, always return the SELECT switch to the AUTO position after manually selecting A-side. When a redundant system powers up, the AAC uses Side A as the active controller (if operational) when the switch is set to AUTO.

Note In a redundant system in which the A-side is powered off and the system is to be brought up with the B-side active, the AAC switch must be set to SELECT B. If the AAC switch is in AUTO, the system will come up in Standby.

The Alarm Cut-Off (ACO) switch is disabled. Changing the ACO switch has no effect on the audible alarm.

Status LEDs

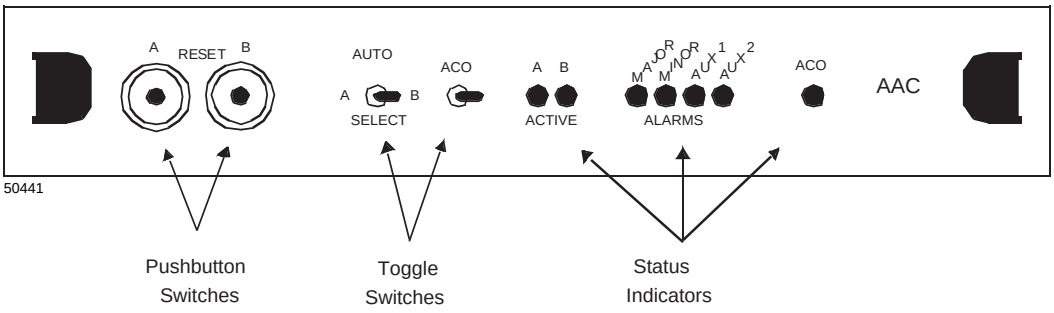
Two green LEDs labeled ACTIVE indicate whether the A-side or B-side system controller is currently the master. Only one of these LEDs is illuminated during normal system operation. The active system controller is also indicated on the bottom message line of the master console display screen.

A red LED illuminates when a MAJOR alarm is signaled by hardware or software. Yellow LEDs indicate MINOR and AUX 1 or AUX 2 alarms. MAJOR and AUX 1 LEDs illuminate when a Power Subsystem or Fan Unit failure occurs. A separate yellow LED illuminates when ACO is enabled.

Note Alarm LEDs on the AAC are disabled when the Audible Cutoff option on the System Alarms Display administration screen is chosen from the Maintenance menu. Refer to the *Cisco VCO/4K System Administrator's Guide* for more information on this option.

Refer to the *Cisco VCO/4K System Maintenance Manual* for more information on alarm LEDs.

Figure 2-4 AAC Front Panel



AAC Alarms

The AAC autonomously sets MAJOR, MINOR, and AUX 1 alarms based on the following criteria:

Major Alarm

- Active side timeout occurs
- Active side is offline
- NBC3 is not installed on Active side
- A power alarm failure occurs

Minor Alarm

- Standby side timeout occurs
- Standby side is offline

AUX 1

- A power alarm failure occurs

Connectors

The J1 connector carries the signals related to one of four peripheral functions to the External Alarms terminal strip, automatic A/B transfer switches, or the Power Subsystem. Table 2-1 lists the pin assignments for the J1 connector.

The J1 connector is attached to connectors JP1, JP3, JP4, and JP5 of the AIC, which provides routing for the signals to and from the AAC.

The J2 connector plugs into the AIC J3 connector. The AAC receives alarm commands from the active system controller, and the watchdog timer “kicks” from both system controllers via the J2 connector. The signals at J2 are proprietary and, therefore, no listing of pin assignments is provided.

The AAC derives power from J2. At least one Combined Controller Assembly must be installed and powered up for the AAC to power up.

Table 2-1 AAC J1 Pinouts

Pin	Signal	Pin	Signal
SLOT 1 – External Alarms			
1	Unused	33	Unused
2	Major Alarm COM	34	Major Alarm CLSD
3	Major Alarm COM	35	Major Alarm OPEN
4	Minor Alarm COM	36	Minor Alarm CLSD
5	Minor Alarm COM	37	Minor Alarm OPEN
6	AUX 1 Alarm CLSD	38	AUX 1 Alarm COM
7	AUX 1 Alarm OPEN	39	AUX 2 Alarm COM
8	AUX 2 Alarm CLSD	40	AUX 2 Alarm OPEN
SLOT 2 – A/B Transfer Switch			
9	Unused	41	Unused
10	Side Select	42	Reserved
11	Reserved	43	DGND
12	Reserved	44	DGND
13	Reserved	45	DGND
14	Reserved	46	DGND
15	Reserved	47	DGND
16	Reserved	48	DGND
SLOT 3 – Power Subsystem			
PROPRIETARY			
SLOT 4 – Backplane			
PROPRIETARY			

AIC Circuit Description

The J1 and J2 connectors of the AAC are mated to the J2 and J3 connectors of the AIC. The AIC cables are locked on to the connectors. The J2 connector is a 64-pin DIN connector.

The J2 connector breaks out the AAC signals into four connectors: JP1, JP3, JP4, and JP5. Table 2-2 lists the AAC signals for these connectors.

Table 2-2 AAC J2 Signals

Connector	Alarm
JP1	Backplane Alarms
JP3	Remote Alarm Output
JP4	A-B Switch for Peripherals
JP5	Selects Active NBC3

The J1 connector is for the Fan Alarm Input. It connects to the Fan Unit through the Fan Unit J4 connector.

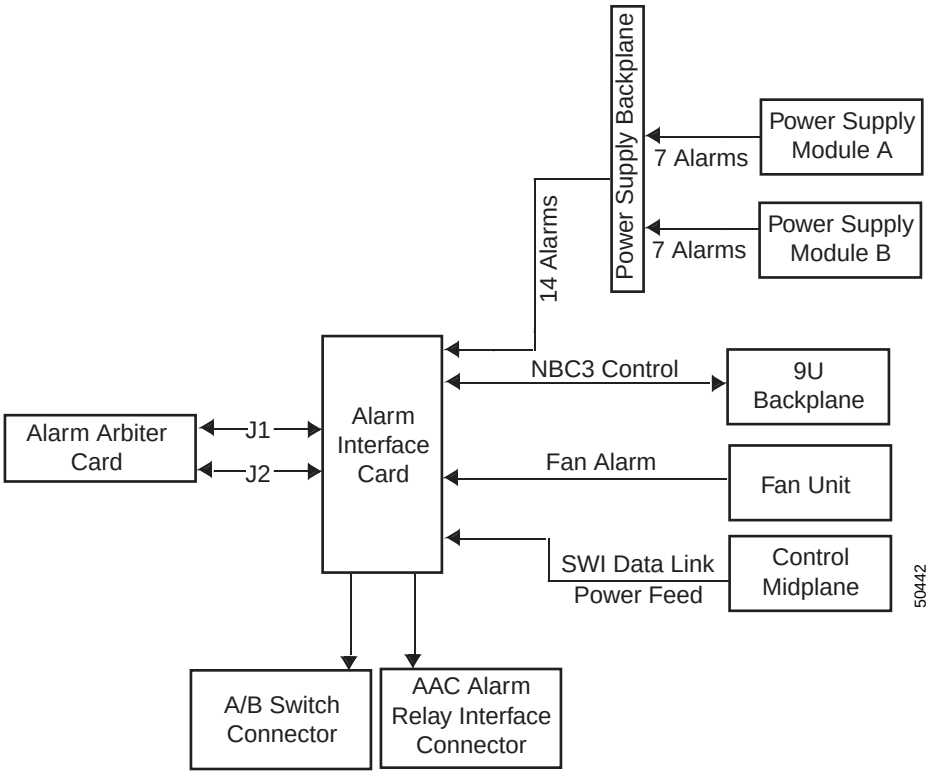
Table 2-3 lists the electrical characteristics of the fault-indicator input to the AIC. The AIC combines and conditions the signals for input to the AAC.

Table 2-3 VCO/4K Fault Indicator Characteristics

Signal	Voltage	Reference Voltage
DC FAIL - Input Power	+0.5 to +5.0V	DC ground
DC FAIL - Power	+0.5 to +5.0V	DC ground
DC OK - Fan	+2.5 to +5.0V	DC ground
DC OK - Ring Generator	100 VAC	–48 VDC
DC OK - Out	+0.5 to +3.0V (200 ohm)	DC ground

Figure 2-5 is a simplified block diagram of the AIC.

Figure 2-5 Block Diagram of the AIC



The output signals from the AAC are used to control remote functions. These signals are not modified by the AIC and are transferred directly from the AAC J1 connector to the AIC JP3 connector.

The DC OK signal on J1-10C is the merged signal of all incoming faults (PWR, FAN, and RING).

Configuration Notes

Alarm Arbiter Card Jumper Locations

Figure 2-6 shows the location and correct installation of jumper plugs on the AAC.

Jumper location J3 allows you to selectively enable the on-board audible alarm device to sound for all alarm conditions or for major alarms only. The Alarm Cut-Off (ACO) switch is disabled. Changing the ACO switch has no effect on the audible alarm.

Position the jumper plug at J4 near R31 for all applications.

Alarm Interface Card

Figure 2-7 shows the location and labeling of the cable connections on the AIC.

Figure 2-6 AAC Jumper Locations

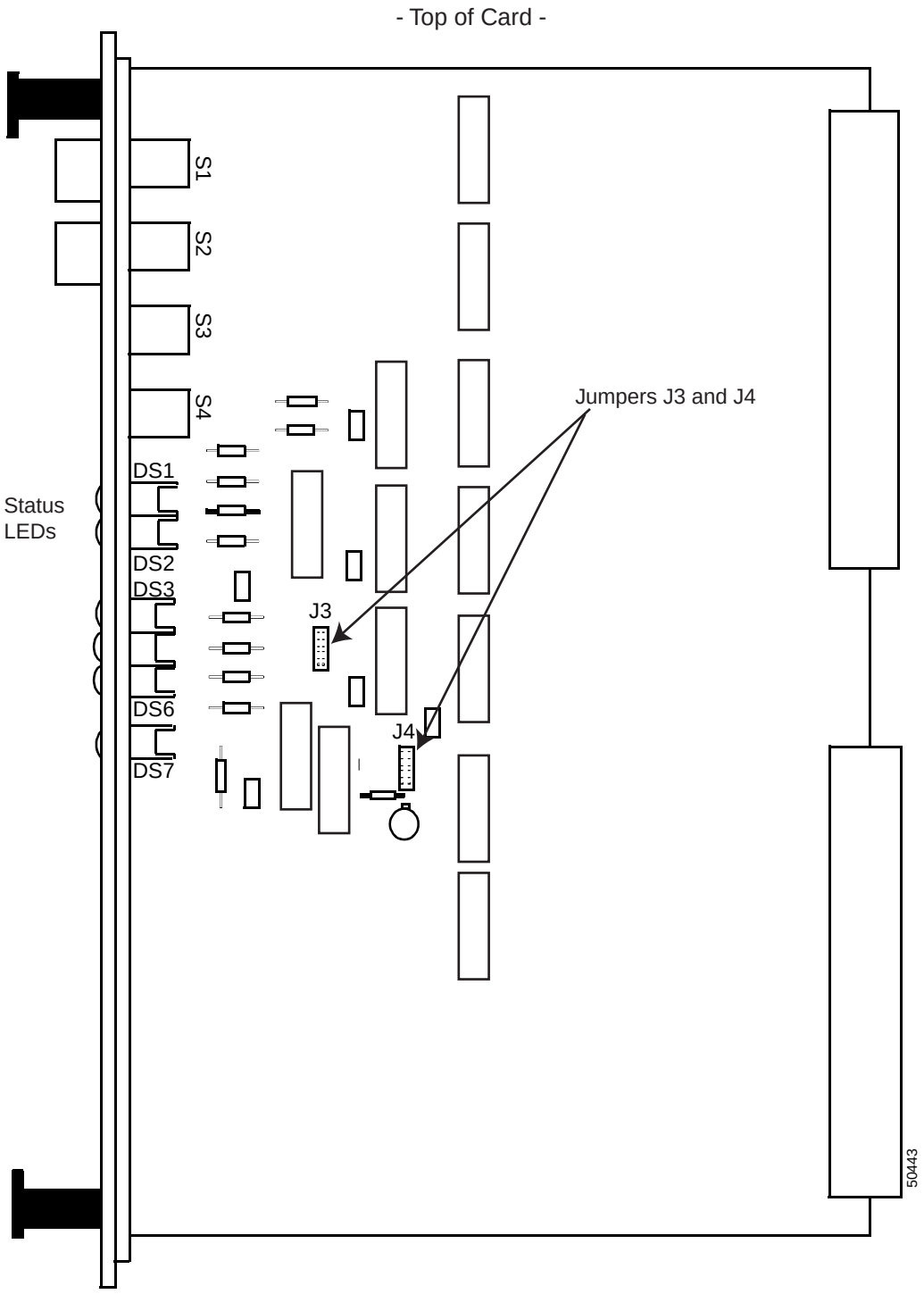
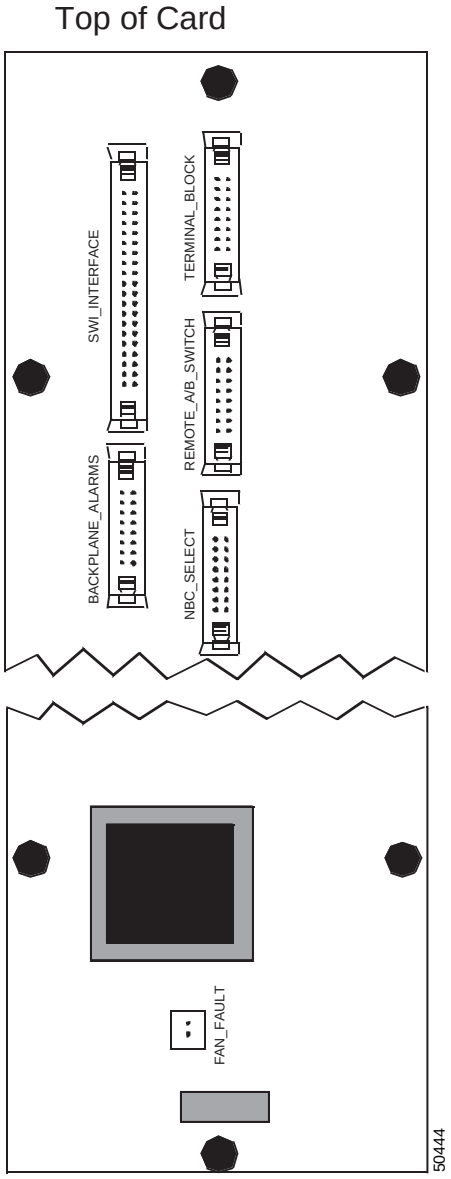


Figure 2-7 AIC Cable Connectors



Removal and Replacement Information

The following subsections provide instructions for removing and replacing alarm arbiter and alarm interface cards.

Caution Removing and replacing the AAC or AIC causes the system controller(s) to reset. Calls in progress will be lost and the system will be out of service for several minutes. To reduce disruptions to service, Cisco Systems recommends replacing these cards when the least amount of traffic is anticipated through the switch.

Caution Power down the system and observe antistatic precautions whenever handling the AAC and AIC to avoid damage to sensitive CMOS devices. Wear a ground strap connected to the VCO/4K equipment frame whenever removing or replacing these control circuit cards.

Removing an AAC

To remove an AAC:

Step 1 Wear a ground strap connected to the VCO/4K equipment frame.

Step 2 Disable the external alarm system.

Step 3 Use a 1/8-inch bladed screwdriver to loosen the captive mounting screws at the top and bottom of the AAC. Do not remove the screws from the card.

Step 4 Set the POWER switch on the Power Entry Module to OFF. The entire system is powered off.

Step 5 Firmly grasp the handles at the sides of the card and pull the card away from the backplane (AIC). The card fits tightly into the AIC connectors and some force is required to pull it.

Note Use only enough force to disengage the AAC. Yanking an AAC card from the AIC can seriously damage connectors and result in operating problems which will be very difficult to isolate.

Step 6 Place the card on an antistatic mat or envelope.

Replacing an AAC

To replace an AAC:

Step 1 Wear a ground strap connected to the VCO/4K equipment frame.

Step 2 Grasp the replacement AAC by the handles and align it with the card guides.

Step 3 Push the AAC inward until it makes contact with the AIC.

Step 4 Firmly grasp the handles of the AAC and push the card toward the AIC. The card fits tightly into the AIC connectors and some force is required to seat the card back firmly into the AIC connectors.

Note Use only enough force to engage the card into the connectors. Jamming an AAC card into the AIC can seriously damage connectors and result in operating problems which will be very difficult to isolate.

Step 5 Place the SELECT switch on the AAC in the A, B, or AUTO position as desired.

Step 6 Set the POWER switch on the Power Entry Module to ON. The system should boot from the hard disk; if it does not, press the Reset A button on the AAC. Normal operation should resume after the system is fully initialized.

Step 7 Use a 1/8-inch bladed screwdriver to tighten the mounting screws at the sides of the card into the tapped holes on the mounting rails.

Step 8 Enable the external alarm system.

Removing and Replacing an AIC

Warning **Only certified Cisco Systems technicians may remove or replace an AIC. Please contact Cisco Systems Technical Support if your AIC needs service.**

Troubleshooting

The AAC will not usually fail during normal operation. However, the AAC interfaces with system controllers and external alarm systems which may cause alarm indications.

Always investigate the operational status of the system controller(s) and the external alarm contacts for faults, and review system logs before suspecting the AAC needs replacement. Remember that Generic software allows the host computer to trigger AUX 1 and AUX 2 alarms.

If the problem is not with the system controllers or external alarm circuits, try rebooting the system (both controllers in a redundant system). If a reset fails, remove and replace the AAC.

In the unlikely event of a software exception (e.g., a bus or address exception) on the active system controller, the AAC may not detect the problem for up to 5 seconds. This delay will cause a loss of the voice path. During the delay, stable calls remain on the Standby controller.

Caution Initiating a reset at the AAC of an active system controller will result in disruption of VCO/4K service. Set the system controller to Standby (redundant control) or be sure that such an interruption is acceptable prior to performing any of the troubleshooting procedures described above.

If replacing the AAC does not correct the problem, the AIC may be at fault and should be removed and replaced by an authorized Cisco Systems technician.

Central Processing Unit (CPU)

The Central Processing Unit (CPU) is a high performance, VMEbus compatible, single board computer that serves as the heart of a system controller. The CPU performs the following system functions:

- Directs read/write data transfers to and from cards on the VMEbus
- Uses TCP/IP for host-to-system communication over an Ethernet interface
- Controls high speed data transfers to and from the hard and floppy disk drives in the system's Storage Subsystem
- Allows transparent access and transfer of system log and trace files between the system and an external device connected via the Ethernet interface
- Provides connections for system peripheral devices (master console, remote maintenance modem, and system printer)

The CPU card incorporates a 68030 type 32-bit microprocessor, 16 MB of dynamic RAM, with 512 KB of ROM. A clock with battery backup supports time-stamped applications.

Specifications

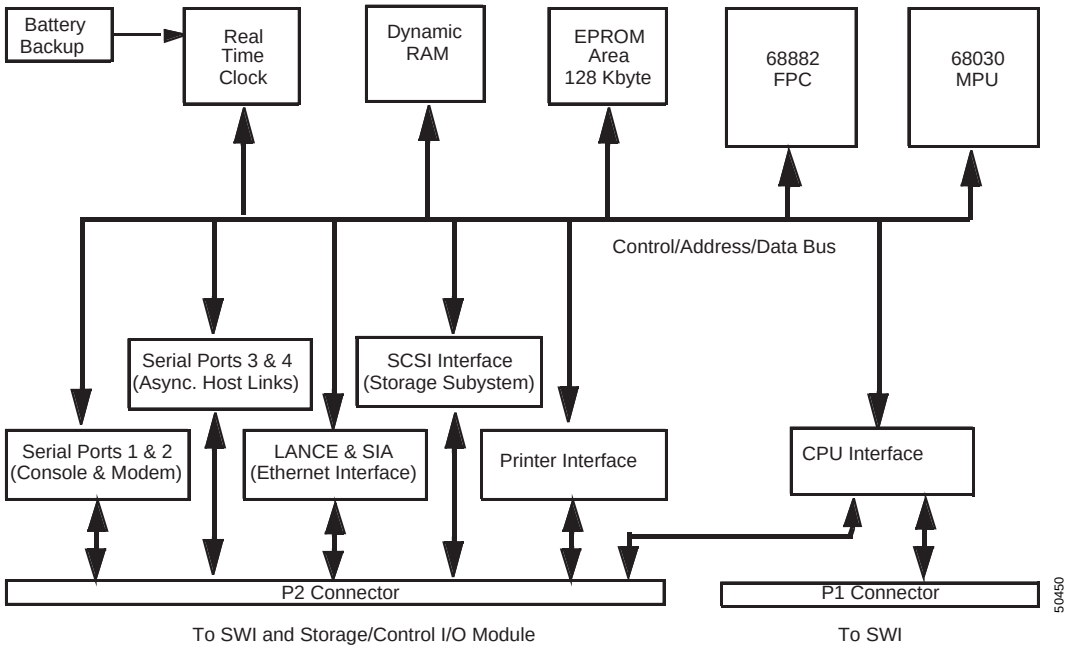
Microprocessor:	MC68030 (33 MHz)		
Real Time Clock:	Programmable real-time clock with battery backup		
Memory:	16 MB of DRAM		
Firmware:	512 MB of PROM		
Power Requirements:		Typical	Maximum
	+5 VDC	3.5 A	4.5 A
	+12 VDC		100 mA
	–12 VDC		100 mA
Physical Dimensions:	Height:	9.2 in. (234 mm)	
	Depth:	6.3 in. (160 mm)	
	Width:	0.8 in. (19.8 mm)	

CPU Card Circuit Description

The 68030 microprocessor supports VMEbus arbitration, memory addressing and refreshing, and multiple I/O ports. The real-time clock is set through a system administration menu (refer to the *Cisco VCO/4K System Administrator's Guide* for more information). Figure 2-8 is a simplified block diagram of the CPU card.

The 68030 microprocessor (MPU) operates at 33 MHz, and includes an asynchronous 32-bit data bus and 32-bit address bus. Memory and I/O devices communicate with the CPU card over its local system bus.

Figure 2-8 Block Diagram of the CPU Card



VMEbus Arbitration

The VMEbus is designed for a multiprocessor application. A CPU card functions as bus master in a system controller with the capability of forcing read or write transfers to and from other cards on the VMEbus. To perform this function, the CPU must be in slot 1 of the upper 9-slot VME backplane. Bus arbitration is daisy-chained to the remaining slots in the backplane.

If the system is equipped with a redundant control subsystem, there are two system controllers. A CPU card is mounted in slot 1 of the redundant upper VME backplanes.

On-Board Dynamic RAM

The on-board RAM (16 MB) is accessible by the 68030 MPU, Local Area Network Controller for Ethernet (LANCE), and VMEbus. Dynamic, RAS-only, RAM refresh is done every 8 ms by performing a memory cycle at each of the 512 row addresses. To accomplish this, once every 15 ms, the refresh timer requests that the RAM sequencer performs a column address strobe.

Firmware

There are four 32-pin EPROM sockets on the CPU cards. Two different PROM memory banks (two PROMs per bank) are used, one for boot up and the other for the system application programs. During power up, the microprocessor reads two vectors from the PROM area: the initial stack pointer and the initial program counter.

Real Time Clock

The real-time clock provides seconds, minutes, hours, day, date, month, and year, in BCD 24-hour format. System administrators can reset the system clock through the Clock/Calendar Configuration screen from the System Configuration menu (refer to the *Cisco VCO/4K System Administrator's Guide* for more information). Automatic corrections are made for 28, 29 (leap year) and 30 day months. The internal backup battery for the clock has a typical life span of from three to five years.

Functional Description of the CPU Card

This section contains a functional description of the major components of the CPU card.

Front Panel Switches and Indicators

Figure 2-9 shows the front panel layout of the CPU card. Two switches, RESET and ABORT, and four LED indicators (FAIL, STATUS, RUN and SCON) are located on the front panel of the card. The RESET switch forces a reset of all on-board devices and the VMEbus, but does not reset the system.

Note To reset the system, use the RESET button on the AAC.

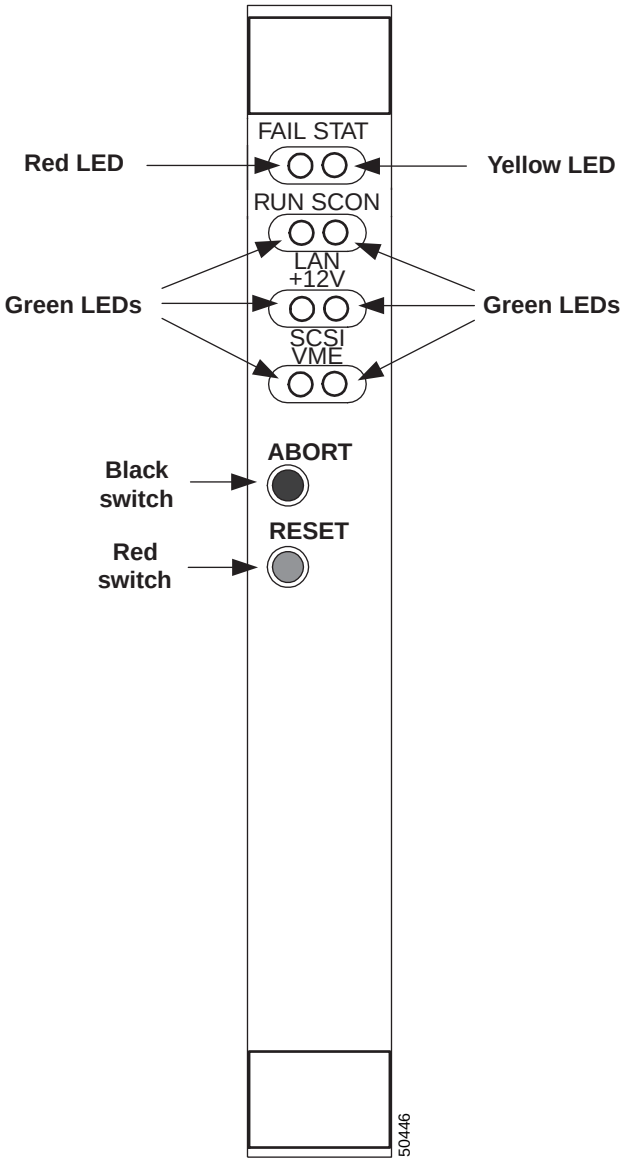
The CPU front panel also contains a connector for a remote reset switch and cable assembly that performs the same function as the RESET switch. Cisco Systems does not provide this switch and cable assembly and does not recommend its use.

The ABORT switch generates a Level 7 interrupt to the 68030 microprocessor. However, the VMEbus is *not* reset.

The red FAIL LED illuminates when the 68030 microprocessor stops processing due to a board failure condition. Users should compare this LED to the yellow STATUS LED to diagnose the failure condition. The STATUS LED indicates a halt condition on the microprocessor. A halt indication following a successful system reset indicates a software problem or a possible DRAM error. A halt on reset may indicate a firmware problem. The PROMs on the CPU card could be improperly installed (wrong location or not in socket), or the firmware may not be at the proper revision level.

Caution A FAIL condition indicates a severe problem that must be dealt with immediately to avoid prolonged loss of service. Reset the system controller from the AAC as a first course of action. If the FAIL condition continues, contact Cisco Systems Technical Support.

Figure 2-9 CPU Card Front Panel



The green RUN and SCON LEDs remain illuminated during normal operation. The RUN LED shows that the 68030 microprocessor is executing a normal bus cycle. The SCON LED shows that the CPU is the system controller. A summary of front panel indicators is provided in Table 2-4.

Table 2-4 CPU Card LED Indicators and Meanings

FAIL Red	STATUS Yellow	RUN Green	CPU STATUS
Off	Off	Off	No power is applied to the CPU or the CPU is not the current local bus master.
Off	Off	On	CPU is waiting for the cycle to complete.
Off	On	Off	CPU is halted.

Table 2-4 CPU Card LED Indicators and Meanings (continued)

FAIL Red	STATUS Yellow	RUN Green	CPU STATUS
Off	On	On	Normal operation.
On	Off	Off	CPU is not the current local bus master and a board failure condition exists.
On	Off	On	Board failure condition exists and the CPU is waiting for cycle to complete.
On	On	Off	CPU is halted and a board failure condition exists.
On	On	On	Complete board failure.

Connectors

The CPU card plugs into the Combined Controller Assembly through two standard DIN 41612 triple-row, 96-pin male connectors.

Configuration Notes

The CPU is a multipurpose OEM-supplied package modified by Cisco Systems for operation in a system. Modifications include the insertion of custom PROM chips in the firmware sockets. Figure 2-10 uses gray scaling to show PROM locations on the CPU card.

PROM Locations

Caution Do not remove or reposition the jumpers on the CPU card. To do so may result in system failures and possible damage to the CPU card or to devices connected to it. Jumpers should remain in the factory-set position on the CPU card.

PROM 1

The 128Kx8 PROM 1 contains firmware with the Low Kernel of the VRTX operating system.

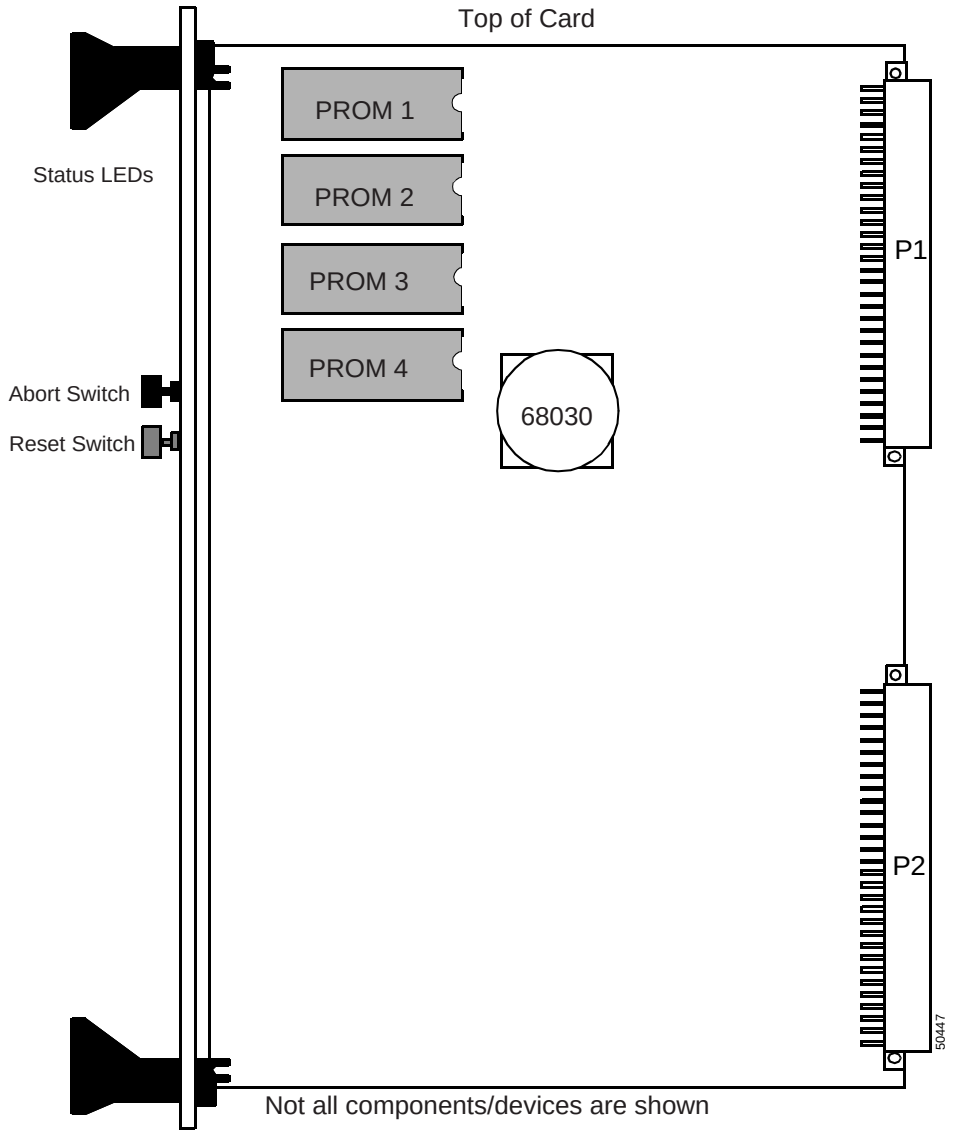
PROM 2

The 128Kx8 PROM 2 contains firmware labeled *High Kernel*.

PROM 3 and PROM 4

PROMs 3 and 4 contain standard EPROM for CPU operation.

Figure 2-10 CPU Card Jumper and PROM Locations



Removal and Replacement Procedures

The CPU card must be the first card plugged into the upper VME backplane of both the primary and redundant system controllers for proper VMEbus control.

Removing and Replacing System Controller Cards

Warning **Read all instructions before attempting to remove or replace a card.**

To minimize the risk of injury from hazardous voltages, avoid contact with the backplane when removing or replacing system cards.

Observe antistatic precautions when handling a card to avoid damaging sensitive CMOS devices. Wear a ground strap connected to the system equipment frame whenever removing or replacing cards or I/O modules.

Control Circuit cards require slightly different procedures for removal and replacement. However, there are some common procedures to be followed before removing and after replacing a circuit card.

All Systems

The CPU card contains the serial number required for the system's timeslot allocation license. This serial number was encoded in the card at the factory and cannot be altered. After the CPU card is replaced, the timeslot allocation license must be updated before the system will operate normally. For information on how to update the license, refer to the *Cisco VCO/4K System Administrator's Guide*.

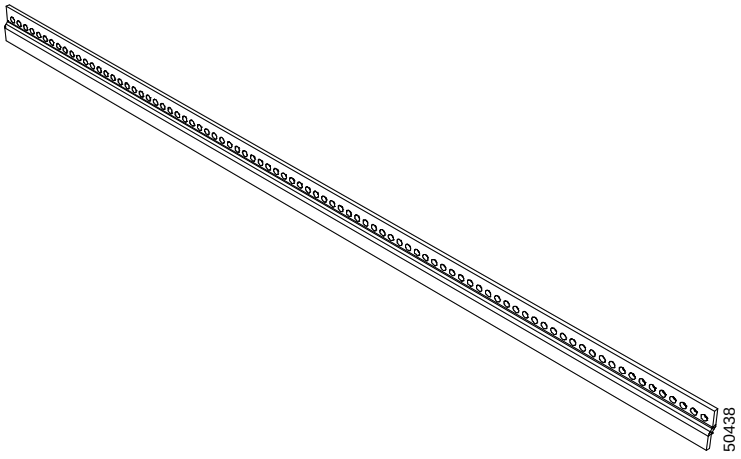
Non-Redundant Control System

A switch with one Combined Controller Assembly will be out of service until the failed Combined Controller Assembly is replaced. To remove and replace a Combined Controller Assembly in a nonredundant switch:

Step 1 Power off the system, following the instructions in your *Cisco VCO/4K System Maintenance Manual*.

Step 2 Use a #1 Phillips-head screwdriver to remove the mounting screws/washers (five per bar) from the top and bottom PCB card retainer bars (see Figure 2-11) on the system. Keep the retainers and screws together in a safe place for replacement later.

Figure 2-11 PCB Card Retainer Bar



Step 3 Remove and replace the failed Combined Controller Assembly(s).

Step 4 Power on the system, following the instructions in your *Cisco VCO/4K System Maintenance Manual*. The system should boot from hard disk; if it does not, press the Reset A button on the AAC. Normal operation should resume after the system has been fully initialized.

Redundant Control System

To remove and replace a CPU card in a switch with redundant control:

Step 1 Use a #1 Phillips-head screwdriver to remove the mounting screws/washers (five per bar) from the top and bottom PCB card retainer bars (see Figure 2-11) on the system. Keep the retainers and screws together in a safe place for replacement later.

Step 2 Place the Combined Controller Assembly to be serviced in Standby mode; use the SELECT switch on the AAC to designate the other Combined Controller Assembly as Active.

Step 3 When the transition to standby is complete, remove the entire Combined Controller Assembly. Calls will be processed through the Active controller.

Step 4 When the service activity has been completed, restore power to the standby side.

Step 5 Press the RESET button of the serviced side on the AAC. The serviced Combined Controller Assembly should boot from hard disk. The update channel will be established and automatic file synchronization will be initiated.

Step 6 When file synchronization is completed, the serviced Combined Controller Assembly should be in standby mode. Return the Side SELECT on the AAC to auto, if desired.

Removing a CPU Card

To remove a CPU card:

Step 1 Use a #1 Phillips-head screwdriver to remove the mounting screws/washers (five per bar) from the top and bottom PCB card retainer bars (see Figure 2-11) on the system. Keep the retainers and screws together in a safe place for replacement later.

Step 2 Remove the entire Combined Controller Assembly from active service (refer to the “Removing and Replacing System Controller Cards” section on page 2-21).

Caution Always remove the Combined Controller Assembly before removing the CPU card. Never remove a CPU card from a Combined Controller Assembly that is mounted in a system.

Step 3 Use your thumbs to push the upper and lower ejectors away from the Combined Controller Assembly front panel. This action will pop the card from the SWI connectors.

Note Remove and replace cards using only enough force to disengage or engage the card from or into backplane connectors. Yanking cards from, or jamming cards into, the backplane can seriously damage connectors and result in operating problems which will be very difficult to isolate.

Step 4 With both hands, grasp the Combined Controller Assembly on its top and bottom edges as you remove it from the card slot. Pull the Combined Controller Assembly from the card slot.

Step 5 Place the card on an antistatic mat or envelope.

Step 6 Use a 1/8-inch bladed screwdriver to loosen the captive mounting screws at the top and bottom of the CPU card. Do not remove the screws from the cards.

Step 7 Use your thumbs to push the upper and lower extractors away from the CPU card front panel. This action disconnects the card from the SWI connectors.

Step 8 Pull the CPU card away from the Combined Controller Assembly.

Step 9 Place the CPU card on an antistatic mat or an antistatic envelope.

Replacing a CPU Card

Caution Always remove the Combined Controller Assembly before replacing the CPU card. Never replace a CPU card in a Combined Controller Assembly that is mounted in a system.

To replace the CPU card:

Step 1 Place the replacement CPU card on the antistatic mat or envelope.

Note Refer to your release notes and verify that the revision levels of the PROMs match the requirements of the generic software currently loaded in your VCO/4K system.

Step 2 Grasp the replacement CPU card by the top handle and the bottom edge and align it with the top and bottom card guides of the Combined Controller Assembly.

Step 3 Push the CPU card in until it makes contact with the SWI connectors. Use your thumbs to push the extractors toward the front panel.

Step 4 Replace the screw at the top of the CPU card front panel.

Step 5 With both hands, grasp the Combined Controller Assembly on its top and bottom edges and align it with the top and bottom card guides of the card slot.

Step 6 Push the Combined Controller Assembly inward until it makes initial contact with the backplane.

Make sure the ejector levers are perpendicular to the front panel. Continue pushing the Combined Controller Assembly inward until it makes firm contact with the backplane. The hooks on the ejectors must be behind the front rail of the card slot. Use your thumbs to push the ejectors inward toward the front panel. The card should be fully seated into the backplane connectors when the levers are flush against the front panel.

Step 7 Grasp the replacement CPU card by the top handle and the bottom edge and align it with the top and bottom card guides of the Combined Controller Assembly.

Step 8 Push the card inward until it makes contact with the backplane.

Step 9 Firmly grasp the handles at the top and bottom of the CPU card and push the card toward the backplane. The card fits tightly into the backplane connectors and some force is required to seat the card back firmly into the backplane connectors.

Step 10 Use a 1/8-inch bladed screwdriver to tighten the mounting screws at the top and bottom of the CPU card.

Step 11 Refer to the "Removing and Replacing System Controller Cards" section on page 2-21 and place the Combined Controller Assembly back in service.

Step 12 Reinstall the top and bottom PCB card retainer bars (see Figure 2-11). Use a #1 Phillips-head screwdriver to replace the mounting screws/washers (five per bar).

Caution The PCB card retainer bars must be installed for the system to meet NEBS Zone 4 Earthquake compliance.

Troubleshooting

Host Communications

The *Cisco VCO/4K System Maintenance Manual* describes corrective maintenance procedures for host communications links. In addition to this manual, you should refer to the *Cisco VCO/4K Standard Programming Reference* or *Cisco VCO/4K Extended Programming Reference* for details relating to command and report formats. *Cisco VCO/4K System Messages* describes the network messages associated with problems detected with the host communications links.

If you are using the optional Ethernet Communications Package, refer to the *Cisco VCO/4K Ethernet Guide* for maintenance procedures.

Other reference materials include the OEM manuals supplied with the host computer I/O package and the modems used for the link (optional), and any documentation related to the communication and application packages to be run on the host computer.

CPU Card Fault Isolation

To isolate and correct CPU card problems, perform the following steps.

Caution Initiating a reset on the CPU card in an Active Combined Controller Assembly will result in disruption of system service. Set the Combined Controller Assembly to Standby (redundant control) or be sure that such an interruption is acceptable prior to performing any of the following troubleshooting procedures.

Step 1 Verify that power is available to the Combined Controller Assembly and comm bus. Check all power cabling to and from the Power Subsystem.

Step 2 Perform a reset by pressing and releasing the RESET switch on the AAC front panel. The LED on the hard disk drive should go ON and OFF intermittently. When the reboot is completed, the RUN, +12V, and SCON indicators should be illuminated.

Step 3 If the Combined Controller Assembly will not reboot, remove and reseat the CPU card into the Combined Controller Assembly. Perform a reset and observe the hard disk drive.

Step 4 Refer to the *Cisco VCO/4K System Maintenance Manual* for additional information on system level troubleshooting techniques. If all else fails, call Cisco Systems Technical Support.

Combined Controller Assembly

The Combined Controller Assembly (CCA) consists of the following components:

- Central Processing Unit (CPU) card (33 MHz)
- Switch Interface (SWI) and floppy disk drive assembly

The CPU is a high-performance, single-board computer that serves as the heart of the system controller.

The SWI provides an interface between the system controller and the following subsystems: Network Bus Controller 3 (NBC3), Alarm Arbiter Card (AAC), and redundant system controller.

The floppy disk drive is a 1.44-MB high-density, 3-1/2 inch, half-height floppy disk drive. The floppy disk drive is used to load software and make backup copies of the system database. You can also choose to store the system database, and log and trace files on floppy disk.

The SWI and floppy disk drive assembly also acts as a carrier for the CPU card.

Figure 2-12 shows the front of a VCO/4K and the location of the Combined Controller Assembly.

Figure 2-12 Combined Controller Assembly (Front Panel)

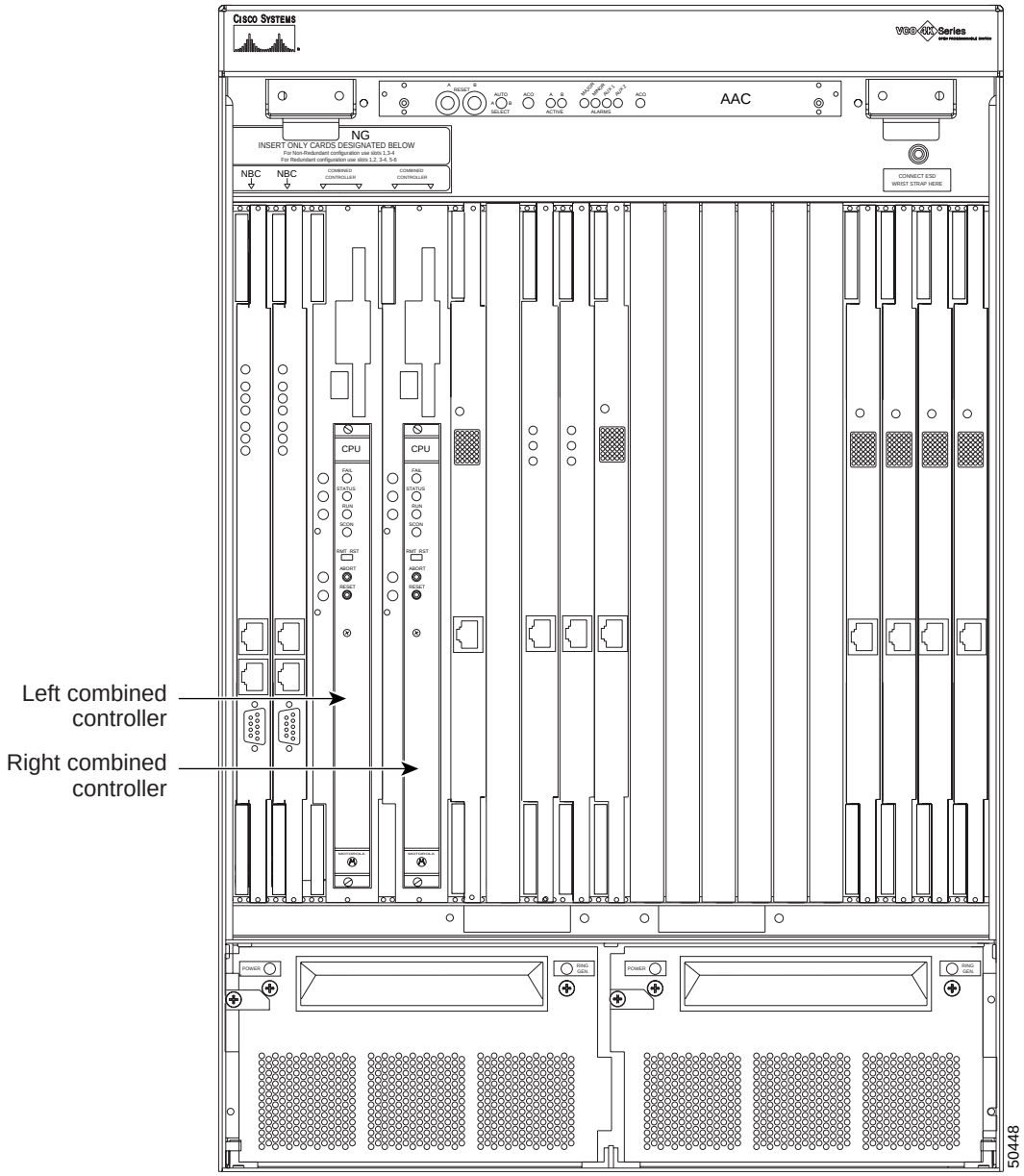
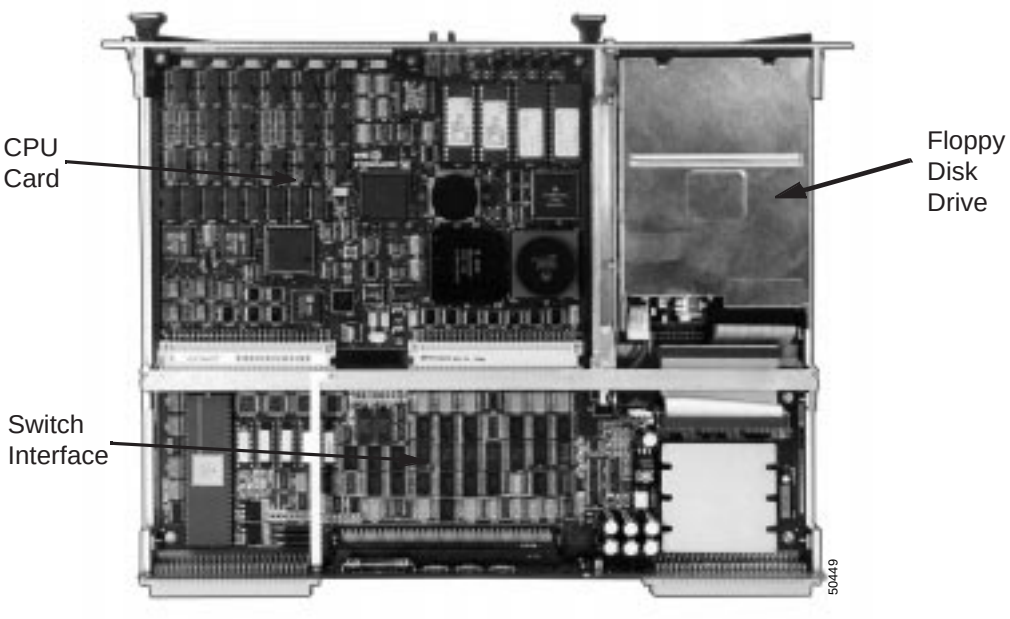


Figure 2-13 is a top view of the Combined Controller Assembly, showing its components.

Figure 2-13 Combined Controller Assembly (Top View)



Specifications

Power Requirements:	+5 VDC	
	–48 VDC	
	–15 VDC	
Physical Dimensions:	Height:	15.6 in. (396 mm)
	Depth:	12.1 in. (307 mm)
	Width:	0.79 in. (20 mm)

CPU Card

The CPU performs the following system functions:

- Directs read/write data transfers to and from the SWI
- Supports host-to-system communication over an Ethernet interface with TCP/IP
- Controls high-speed data transfers to and from the hard and floppy disk drives in the Storage Subsystem
- Allows transparent access and transfer of system log and trace files between the system and an external device connected via the Ethernet interface

- Provides control to peripheral devices (master console, remote maintenance modem, and system printer)

The CPU card incorporates a 68030 type 32-bit microprocessor, 16 MB of dynamic RAM, and 512 KB of ROM. A clock with battery backup supports time-stamped applications.

Specifications

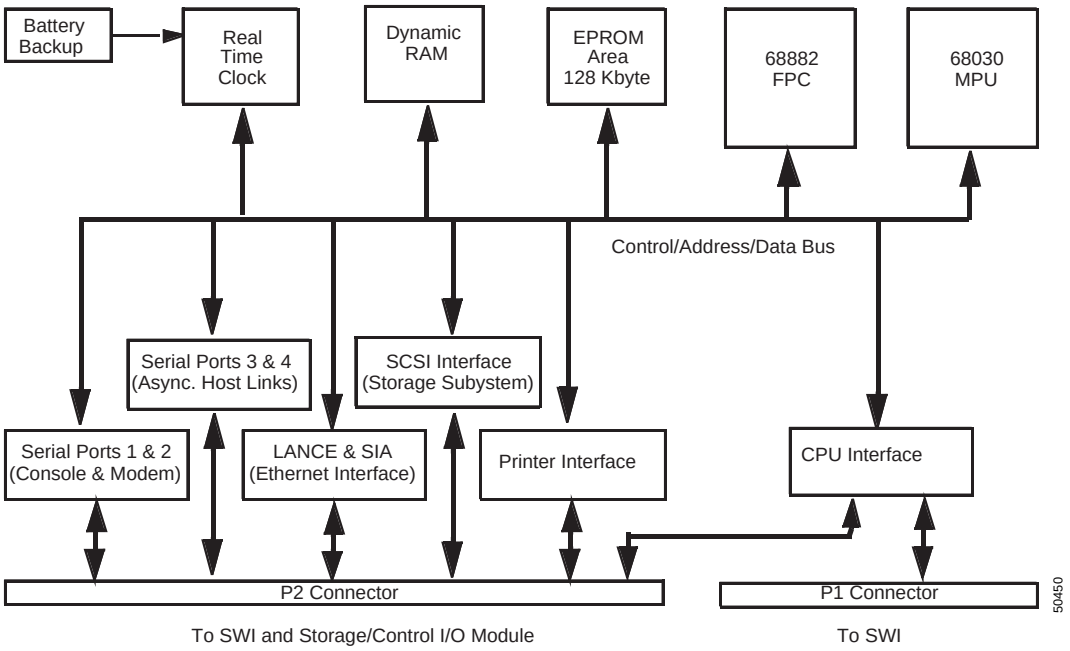
Microprocessor:	MC68030 (33 MHz)	
Real Time Clock:	Programmable real-time clock with battery backup	
Memory:	16 MB of DRAM	
Firmware:	512 KB of EPROM	
Physical Dimensions:	Height:	9.2 in. (234 mm)
	Depth:	6.3 in. (160 mm)
	Width:	0.8 in. (19.8 mm)

CPU Card Circuit Description

The 68030 microprocessor supports memory addressing and refreshing, and multiple I/O ports. The real-time clock is set through a system administration menu (refer to the *Cisco VCO/4K System Administrator's Guide* for more information). Figure 2-14 is a simplified block diagram of the CPU card.

The 68030 microprocessor operates at 33 MHz and includes an asynchronous 32-bit data bus and 32-bit address bus. Memory and I/O devices communicate with the CPU card over its local system bus.

Figure 2-14 Block Diagram of CPU Card



On-Board Dynamic RAM

The on-board RAM (16 MB) is accessible by the 68030 MPU and Local Area Network Controller for Ethernet (LANCE). The CPU refreshes dynamic, RAS-only, and RAM every 8 ms by cycling through the memory at each of the 512 row addresses. To accomplish this, once every 15 ms, the refresh timer requests that the RAM sequencer performs a column address strobe.

Firmware

There are four 32-pin EPROM sockets on the CPU card. Two different EPROM memory banks (2 PROMs per bank) are used—one for bootup and the other for the system application programs. During powerup, the microprocessor reads two vectors from the EPROM area: the initial stack pointer and the initial program counter.

Real-Time Clock

The real-time clock provides seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. The Clock/Calendar Configuration screen from the System Configuration menu allows users to reset the system clock via system administration (refer to the *Cisco VCO/4K System Administrator's Guide* for more information). Automatic corrections are made for 28, 29 (leap year) and 30-day months. The internal backup battery for the clock has a typical life span of three to five years.

Front Panel Switches and Indicators

Two switches, RESET and ABORT, and four LED indicators (FAIL, STATUS, RUN, and SCON) are located on the front panel of the CPU card. The RESET switch forces a reset of all on-board devices, but does not reset the system.

Note To reset the system, use the RESET buttons on the AAC.

The Combined Controller front panel also contains a connector for a remote reset switch and cable assembly that performs the same function as the RESET switch. Cisco Systems does not provide this switch and cable assembly and does not recommend its use.

The ABORT switch generates a Level 7 interrupt to the 68030 microprocessor.

The red FAIL LED illuminates when the 68030 microprocessor stops processing due to a board failure condition. Users should compare this LED to the yellow STATUS LED to diagnose the failure condition. The STATUS LED indicates a halt condition on the microprocessor. A halt indication following a successful system reset indicates a software problem or a possible DRAM error. A halt on reset may indicate a firmware problem. The PROMs on the CPU card could be improperly installed (wrong location or not in socket), or the firmware may not be at proper revision level.

Caution A FAIL condition indicates a severe problem that must be dealt with immediately to avoid prolonged loss of service. Reset the system controller from the AAC as a first course of action. If the FAIL condition remains, contact Cisco Systems Technical Support.

The green RUN and SCON LEDs remain illuminated during normal operation. The RUN LED indicates the 68030 microprocessor is executing a normal bus cycle. The SCON LED indicates the CPU is the system controller. Table 2-5 describes the front panel status LEDs.

Table 2-5 CPU Card LED Indicators and Meanings

FAIL Red	STATUS Yellow	RUN Green	CPU STATUS
Off	Off	Off	No power is applied to the CPU or the CPU is not the current local bus master.
Off	Off	On	CPU is waiting for cycle to complete.
Off	On	Off	CPU is halted.
Off	On	On	Normal operation.
On	Off	Off	CPU is not the current local bus master and a board failure condition exists.
On	Off	On	Board failure condition exists and the CPU is waiting for cycle to complete.
On	On	Off	CPU is halted and a board failure condition exists.
On	On	On	Complete board failure.

Connectors

The CPU card plugs into the SWI and floppy disk drive assembly through two standard DIN 41612 triple-row, 96-pin male connectors.

Configuration Notes

The CPU is a multipurpose, OEM-supplied package modified by Cisco Systems for operation in a system. Modifications include the insertion of custom EPROM chips in the firmware sockets.

CPU Card EPROM Locations

Caution Do not remove or reposition the jumpers on the CPU card, as this may result in system failures and possible damage to the CPU card or to devices connected to it. Jumpers should remain in the factory-set position on the CPU card and should not be removed or changed.

EPROM 1

The 128Kx8 EPROM1 contains firmware with the Low Kernel of the VRTX operating system.

EPROM 2

The 128Kx8 EPROM2 contains firmware labeled *High Kernel*.

EPROM 3 & EPROM 4

EPROMs 3 and 4 contain boot EPROM for CPU operation.

Switch Interface (SWI) and Floppy Disk Drive Assembly

Specifications

DMA Controller:	68450 (4 MHz)	
Memory:	64 KB Static RAM	
Formatted Capacity:	1.44 MB	
Signal Interface:	SCSI	
Recording Method:	MFM	
Media Requirement:	3.5-inch, high-density (2HD) floppy disks	
Rotational Speed:	300 rpm	
Read/Write Heads:	2 heads	
Track Density:	135 tracks per inch (tpi)	
Data Transfer Rate:	500 kbps	
Physical Dimensions:	Height:	15.6 in. (396 mm)
	Depth:	12.1 in. (307 mm)
	Width:	1.58 in. (40 mm)

SWI Circuit Card Description

The SWI is located on the Combined Controller Assembly along with the floppy disk drive and outer backplane. The SWI card generates the specific voltages that are used by the CPU card and the floppy disk drive and Storage/Control I/O Module. It also passes SCSI information to the floppy disk drive and the hard disk drive. The hard disk drive is located on the Storage/Control I/O Module.

The SWI provides a memory-addressable interface from the CPU to the NBC3 and the AAC. The SWI also passes power to the AAC (see Figure 2-15).

The NBC3 interface includes a 16-bit bidirectional data path and handshaking signals. This path carries command data and call setup data loaded into SWI registers by the system controller CPU. Two unidirectional 8-bit data channels allow communication between the A-side and B-side SWI cards in redundant systems.

DMA Controller

All data transfers between the NBC3 and SWI, or between two SWIs, are performed by a 68450 four-channel bidirectional DMA controller. The DMA controller only transfers data to and from the SWI's on-board 64 KB of static RAM. The SWI cannot write data to and from the CPU as a bus master.

The 68450 is a four-channel DMA controller. Channels 0 and 1 are configured for 16-bit data transfers to and from the NBC3. Channels 2 and 3 are configured for 8-bit data transfers to and from the SWI in a redundant system configuration. Channels 0 and 2 are dedicated to incoming data; channels 1 and 3 are used for outgoing (relative to the SWI) data.

Logic on the SWI causes a DMA operation to terminate normally when the last byte/word of data is sent or received. When a data transfer is complete, the DMA controller interrupts the CPU. On the CPU's interrupt acknowledge cycle, the DMA controller returns the appropriate channel's normal interrupt vector.

If a bus error occurs while the DMA controller is in control of the internal SWI bus, the DMA controller terminates the bus cycle, aborts the transfer, sets the channel error register to indicate that a bus error occurred, and interrupts the CPU. On the CPU's interrupt acknowledge cycle, the DMA controller returns the appropriate channel's error interrupt vector.

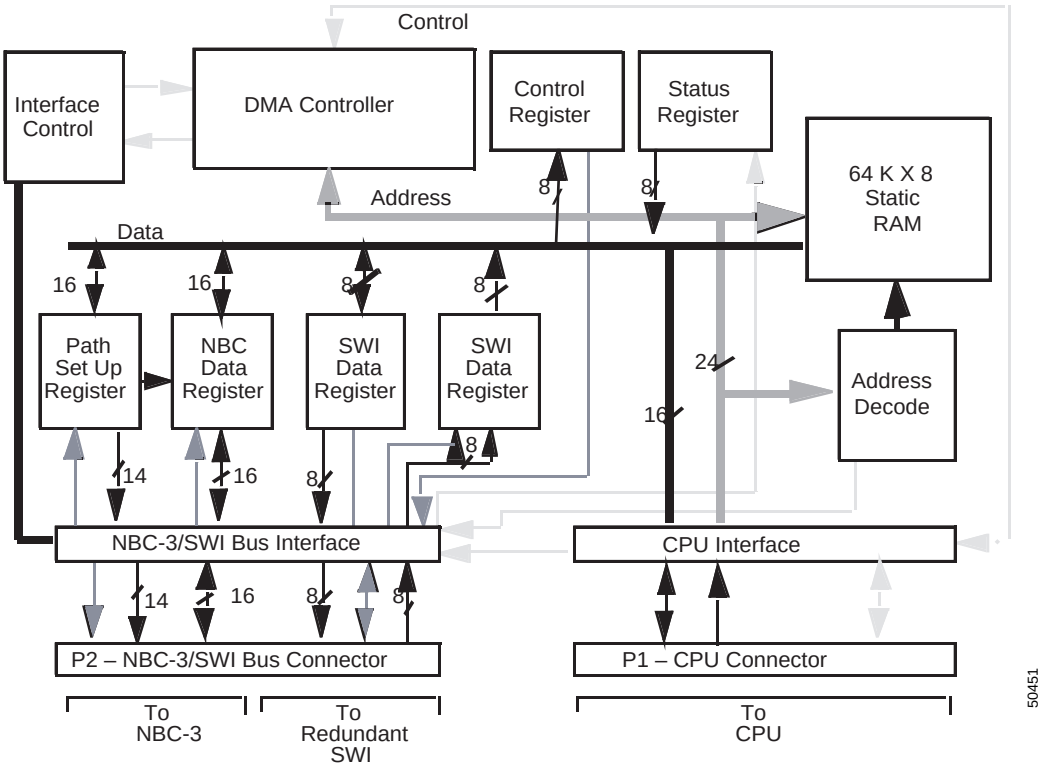
Path Setup

Two sets of bidirectional registers are provided on the SWI. These registers are loaded by the CPU to send path setup information to the NBC3. Verify path setup information by reading the contents of these registers.

Static RAM

Static RAM on the SWI is isolated from the CPU so that DMA transfers to and from memory can occur without interrupting activity on the CPU. When CPU access to any on-board SWI device occurs, the current DMA cycle, if any, is completed before the CPU access takes place.

Figure 2-15 Block Diagram of SWI Card



SWI Interconnections

The signals between SWIs are carried on the control midplane. The signals to the AAC are carried to the control midplane and then through a ribbon cable to the AIC. The AAC then seats directly into the AIC. The connection between the SWI and the NBC3 is made through the control midplane.

Floppy Disk Drive Description

The floppy disk drive is a 1.44-MB high-density, 3-1/2-inch, half-height floppy disk drive. Use the floppy disk to load software and make backup copies of the system database. Disk utilities are accessible from the Maintenance menu during system operation and from the Software Installation Utility diskette when this diskette is used to initialize the system.You can also choose to store the system database, and log and trace files on floppy disk. Refer to the *Cisco VCO/4K System Administrator's Guide* for more information.

The drive reads/writes to 3-1/2-inch double-sided, high density (2HD) floppy disks. Files are stored on the floppy drive in MS-DOS format. The floppy drive has a black ABS plastic front with a disk ejection button and a drive access LED indicator.

Front Panel LEDs

The front panel of the Combined Controller Assembly contains five LEDs.

Three SWI status LEDs are located at the top of the front panel. These LEDs are OFF when the card is operating normally. The red (top) LED is illuminated when either the system controller or the NBC3 fails. All LEDs are illuminated during system initialization.

The red 12VF LED located near the bottom of the panel shows a local 12-volt combined controller power failure.

The red HDD LED located below the 12VF LED shows hard disk drive activity.

Removal and Replacement Procedures

Combined Controller Assembly

System controllers require slightly different procedures for removing and replacing the other cards. Depending on whether you have a redundant or a nonredundant system, there are some common procedures to follow before removing and after replacing the combined controllers. These procedures are discussed in the following sections.

Caution Observe antistatic precautions whenever handling the Combined Controller Assembly to avoid damage to sensitive CMOS devices. Wear a ground strap connected to the system equipment frame whenever removing or replacing control circuit cards.

A system with one Combined Controller (nonredundant systems) remains out of service until a failed Combined Controller Assembly is replaced.

To remove and replace a Combined Controller in a nonredundant system:

Step 1 Power off the system, according to the instructions in the *Cisco VCO/4K System Maintenance Manual*.

Step 2 Remove and replace the Combined Controller Assembly.

Step 3 Power on the system, according the instructions in the *Cisco VCO/4K System Maintenance Manual*. The system should boot from the hard disk. If it does not, press the RESET A button on the AAC. Normal operation should resume after the system is fully initialized.

To remove and replace a Combined Controller Assembly in a redundant system:

Step 1 Use the system administration menus to place the Combined Controller Assembly to be serviced in STANDBY mode. Refer to the *Cisco VCO/4K System Administrator's Guide* for more information.

Step 2 Remove and replace the STANDBY Combined Controller Assembly. Calls will continue to be processed through the ACTIVE system.

Step 3 When the service activity is complete, use the system administration menus to place the STANDBY Combined Controller Assembly in ACTIVE mode. Refer to the *Cisco VCO/4K System Administrator's Guide* for more information. The update channel is established and automatic file synchronization is initiated.

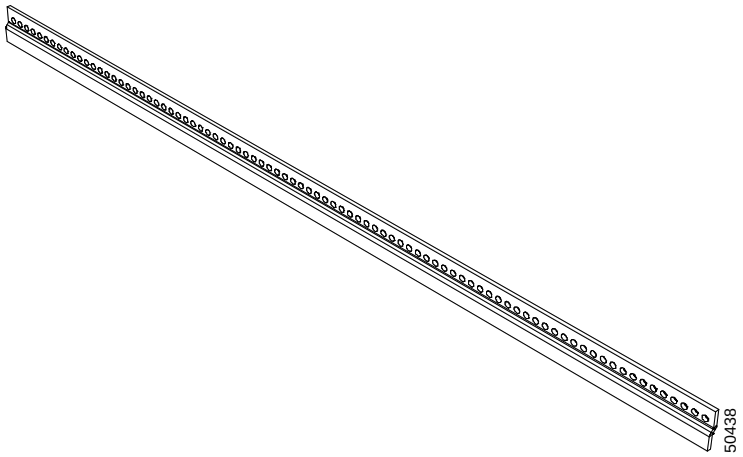
Removing a Combined Controller Assembly

To remove a Combined Controller Assembly:

Step 1 Wear a ground strap connected to the VCO/4K equipment frame.

Step 2 Use a #1 Phillips-head screwdriver to remove the mounting screws/washers (five per bar) from the top and bottom PCB card retainer bars (see Figure 2-16) on the system. Keep the retainers and screws together in a safe place for replacement later.

Figure 2-16 PCB Card Retainer Bar



Step 3 Use your thumbs to push the upper and lower extractors away from the card front panel. This action disconnects the assembly from the backplane connectors.

Step 4 Pull the Combined Controller Assembly away from the card slot.

Step 5 Place the card on an antistatic mat or an antistatic envelope.

Replacing a Combined Controller Assembly

To replace a Combined Controller Assembly:

Step 1 Wear a ground strap connected to the VCO/4K equipment frame.

Step 2 Grasp the replacement Combined Controller Assembly by the top handle and the bottom edge and align it with the top and bottom card guides of the rack.

Warning **Be sure to plug the Combined Controller Assembly into the slot marked for the Combined Controller Assembly. Plugging the Combined Controller into the wrong slot may cause serious damage to the controller.**

Step 3 Be sure the extractor levers are perpendicular to the front panel. Push the Combined Controller Assembly into the rack until it makes contact with the backplane. The hooks on the extractors must be behind the front rail of the rack.

Step 4 Reinstall the top and bottom PCB card retainer bars (see Figure 2-16). Use a #1 Phillips-head screwdriver to replace the mounting screws/washers (five per bar).

Caution The PCB card retainer bars must be installed for the system to meet NEBS Zone 4 Earthquake compliance.

CPU Card

The CPU card contains the unique serial number required for the system's timeslot allocation license. This serial number was encoded in the card at the factory and cannot be altered. After the CPU card is replaced, you must update the timeslot allocation license before the system will operate normally. For information on how to update the license, refer to the *Cisco VCO/4K System Administrator's Guide*.

Removing a CPU Card

To remove a CPU card:

Step 1 Wear a ground strap connected to the VCO equipment frame.

Step 2 Remove the Combined Controller Assembly. Refer to the "Removing a Combined Controller Assembly" section on page 2-35 for more information.

Caution Always remove the Combined Controller Assembly before removing the CPU card. Never remove a CPU card from a Combined Controller Assembly that is mounted in a system.

Step 3 Remove the screw at the top of the CPU card front panel.

Step 4 Use your thumbs to push the upper and lower extractors away from the CPU card front panel. This action disconnects the card from the SWI connectors.

Step 5 Pull the CPU card away from the Combined Controller Assembly.

Step 6 Place the CPU card on an antistatic mat or an antistatic envelope.

Replacing the CPU Card

To replace the CPU card:

Step 1 Wear a ground strap connected to the VCO equipment frame.

Caution Always remove the Combined Controller Assembly before replacing the CPU card. Never replace a CPU card in a Combined Controller Assembly that is mounted in a system.

Step 2 Grasp the replacement CPU card by the top handle and the bottom edge and align it with the top and bottom card guides of the Combined Controller Assembly.

Step 3 Push the CPU card in until it makes contact with the SWI connectors. Use your thumbs to push the extractors toward the front panel.

Step 4 Replace the screw at the top of the CPU card front panel.

Step 5 Replace the Combined Controller Assembly. Refer to the "Replacing a Combined Controller Assembly" section on page 2-35 section for more information.

Troubleshooting

Fault Isolation

CPU Card

Use the following steps to isolate and correct programs with the CPU card.

Caution Initiating a reset on the CPU card in an ACTIVE Combined Controller Assembly will result in disruption of system service. Set the Combined Controller to STANDBY (redundant control) or be sure that such an interruption is acceptable prior to performing any of the troubleshooting procedures described below.

Step 1 Verify that power is available to the Combined Controller Assembly. Check all power cabling to and from the Power Subsystem. Also, check the 12V Fail LED on the front panel of the Combined Controller Assembly.

Step 2 Perform a reset by pressing and releasing the appropriate RESET switch on the AAC front panel. The hard disk drive access LED should go ON and OFF intermittently. When the reboot is complete, the RUN and SCON indicators should be illuminated.

Step 3 If the Combined Controller will not reboot, remove it and check that the CPU is properly seated. Perform a reset and observe the hard disk drive.

Step 4 If the Combined Controller resets but the login screen does not appear on the master console screen, the problem may be due to either the VDT or the connecting cable. Check the cable and refer to the OEM manual supplied with the VDT for troubleshooting procedures.

Step 5 Refer to the *Cisco VCO/4K System Maintenance Manual* for additional information on system-level troubleshooting techniques. If all else fails, call Cisco Systems Technical Support.

SWI and Floppy Disk Drive Assembly

Problems with the floppy disk drive are indicated by error messages displayed on the master console and status LEDs on the front of the Combined Controller.

Refer to the *Cisco VCO/4K System Maintenance Manual* for additional information about system level troubleshooting techniques. If all else fails, call Cisco Systems Technical Support.

Error Messages

Problems with the floppy disk drive are shown in error messages generated when the operating system attempts to read or write files to the drive. These messages are displayed on the master console screen and stored in the system error log on the hard disk. A review of the error logs will reveal developing patterns of stored file errors. These errors may indicate impending failure of a floppy disk drive component. Messages associated with floppy disk drive errors begin with a "PRM" prefix. *Cisco VCO/4K System Messages* contains a complete listing of error messages with brief definitions.

Problems with the SWI are shown in error messages generated when the SWI/NBC3 interface fails. If such messages are discovered, refer to the *Cisco VCO/4K System Administrator's Guide* and the "Network Bus Controller 3 Card (NBC3)" section on page 2-39 for additional troubleshooting information.

LEDs

CPU Card

If error messages indicate stored file problems, look to the CPU card LEDs and verify these indicators. If the CPU card appears to be operating normally, use the Disk Utilities menu under the Maintenance menu to call up a directory of the drive (refer to the *Cisco VCO/4K System Administrator's Guide*). Observe the access LEDs on the floppy disk drive and hard disk drive. These LEDs should be illuminated as the operating system reads the directory.

SWI and Floppy Disk Drive Assembly

The red SWI LED located at the top of the panel indicates a major alarm condition when either the system controller or the NBC3 fails.

The red 12VF LED located at the bottom of the panel indicates a local 12V combined controller power failure.

The red HDD LED located above the 12VF LED indicates hard disk drive activity.

The floppy disk drive access LED is illuminated when the drive is accessed for a read/write operation. This LED should illuminate under the following conditions:

- During a reinstall from a floppy
- When saving or loading the database to or from floppy disk
- During initialization of a floppy
- When reading a directory

Network Bus Controller 3 Card (NBC3)

The Network Bus Controller 3 (NBC3) is a special control circuit card that drives the communications bus (comm bus) and timeslot address bus, and generates the system clocks. The NBC3 also provides the data communication path between other control circuit cards and the rest of the system.

The intelligence of the NBC3 comes from an on-board 68360 microprocessor. The 68360 microprocessor memory includes 1 MB of RAM (selectable) and 256 KB of EPROM.

The 68360 microprocessor allows the NBC3 to serve as the comm bus master. The Switch Interface (SWI) functions as a direct memory access (DMA) interface to the NBC3 for communication with the other control circuit cards. Redundant NBC3 cards operate in active or standby mode, depending on which controller is selected as master through the Alarm Arbiter Card (AAC).

Caution Do not pull the active side NBC3 on an operating production switch. Pulling an active NBC3 can generate errors and impact traffic. If you suspect a problem with an NBC3 card and you wish to remove it, first switch sides to make it the standby side.

The NBC3 uses dynamic random access memory (DRAM) for program storage. The program/application is downloaded from the CPU card to the NBC3 through the SWI.

The NBC3 implements special Phase Locked Loop (PLL) circuitry that allows for system synchronization to the network via incoming T1/E1 facilities, or to the central office (CO) composite clock from a Building Integrated Timing Source (BITS) signal, or to the internal clock.

The card is equipped with a Stratum 4 clock.

DTG-2 Mezzanine Card

The NBC3 has connections for a DTG-2 mezzanine card. The DTG-2 mezzanine card functions the same as the full-size DTG card. You can use either DTG card in your system. However, the DTG-2 mezzanine card does not require its own card slot.

Specifications

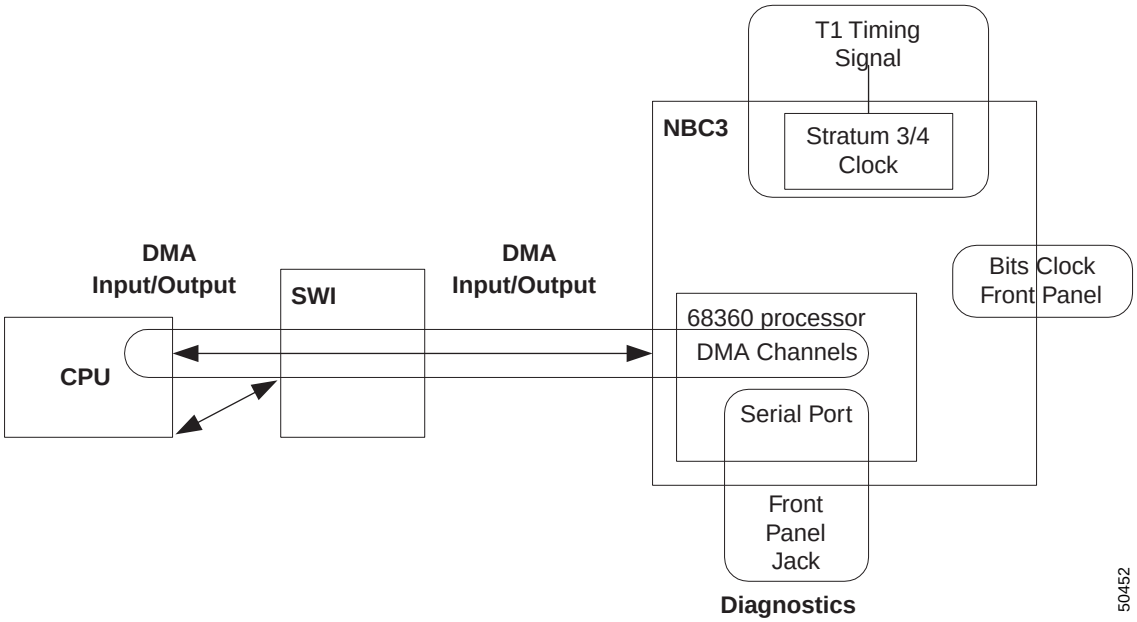
Microprocessor	MCG8EN360-25
Memory	1, 2, 4, or 8 MB DRAM SIMM 256 KB EPROM
Power Requirements (Typical)	5 Volts – 4000 mA +15 Volts – 350 mA –15 Volts – 375 mA

System Synchronization:	
Clock Input	1.544 MHz ±75 Hz (bus) 64 KHz ± 6.4 Hz (external)
Internal Reference Clock	1.544 MHz ± 40 Hz (standard) 1.544 MHz ± 7.1 Hz
Physical Dimensions	Height: 15.6 in. (396 mm) Depth: 12.1 in. (307 mm) Width: 0.79 in. (20 mm)

Circuit Description

Figure 2-17 is a block diagram of the NBC3 card.

Figure 2-17 Block Diagram of NBC3 Card



Communications Bus

As the master of the comm bus, the NBC3 performs the following communication functions:

- Communicates with other boards on the backplane through the comm bus.
- Initiates all data transfers on the comm bus.
- Sends messages to just one card or broadcasts messages to many other cards (except a redundant NBC3) at the same time.

The comm bus is a one-byte-wide half-duplex interface. This interface facilitates the transfer of messages between the port cards and the NBC3.

Clock Synchronization

The NBC3 includes PLL circuitry that lets you synchronize system clocks from an internal or external source. Internally, the NBC3 generates the timeslot reference quadrature (Stratum 4) clock.

Externally, the NBC3 synchronizes the system with a 64-KHz BITS clock input or with any incoming T1 (1.544-MHz clock) stream or E1 (2.048-MHz clock) stream. It can synchronize to an internal 1.544-MHz Stratum 4 clock.

Table 2-6 describes the timing synchronization options on the NBC3.

Table 2-6 System Clock Synchronization Options

Timing Source	Description
A central office 64 KHz bipolar BITS clock.	Signal comes from the BITS. The BITS signal supplies DS1 and/or composite clock timing reference to all the other clocks in the central office. Synchronizes the system to the network. Input is through a DB-9 connector on the NBC3 card front panel. [1]
A 1.544 MHz internal clock reference that synchronizes the pulse code modulation (PCM) bus on T1/E1 data streams. This source does not synchronize the system to the network; it provides a clock source that is Stratum 4 compliant. This clock is normally used for short periods of time (a day or less) when the network timing signal is lost for standalone switch operation.	Stratum-4 Clock Oscillator on card has a 20-year accuracy rating of ±25 ppm (parts per million). Oscillator meets the requirements for Stratum 4.
An incoming T1, E1, or PRI facility that gets its timing from a network timing source.	Timing is sourced from an incoming T1 stream. Input is through a backplane connection.

1. A BITS clock cable kit is available that routes the BITS signals to the rear of the VCO/4K chassis. This allows easy access for external cabling.

The BITS clock signals at the DB-9 (J8) connector on the face of the NBC3 card (and on the optional BITS clock rear conector) are listed in Table 2-7.

If the NBC3 is the last destination of the BITS clock signal, install a jumper at JP3 (Rev E0xR boards) or JP7 (Rev C0xR boards) to terminate the clock signal.

Table 2-7 BITS Clock Connector Pinouts

Signal	Pin
Bipolar, Twisted pair	2
	3

SWI Interface

The NBC3 communicates with the control circuit cards through a 16-bit, DMA-controlled, bi-directional data bus between the NBC3 and the SWI card. The NBC3 translates information from control circuit cards into a serial or 8-bit parallel stream.

The interface is connected internally via one of the serial communications controllers within the CPU, which is controlled by the NBC3 application. The input channel transfers data from the control circuit cards to the NBC3. The output channel transfers data from the NBC3 to the control circuit cards.

Data is transferred to and from the NBC3 memory by the DMA controllers on the SWI that are directionally dedicated.

Control Circuit Cards to NBC3 Messaging

The NBC3 receives command messages from the control circuit cards through the two SWI DMA channels. Received messages are placed into one of the receive buffers on the NBC3. Individual messages are extracted from the receive buffer(s) and placed in the appropriate card output buffer. There is an output buffer for each card in the system.

The NBC3 sends messages to the control circuit cards through the SWI DMA channels. Messages are received from the cards during the card polling cycle, aggregated in one of NBC3 transmit buffers, and when the buffer is full, sends the messages to the control circuit cards.

Control Circuit Cards to NBC3 Timeslot Base Address Information

The timeslot address information stream shares the path on the SWI to the NBC3 with the normal messaging. The NBC3 receives the information from the control circuit cards, after which the information is translated into serial or parallel data. The data is then sent to the cards equipped to receive and interpret translated information through either the high-speed serial interface or the comm bus on the backplane. Other cards receive path setup commands as part of the messages from the control circuit cards through the NBC3.

External Interfaces

Table 2-8 lists the external interfaces for the NBC3 cards.

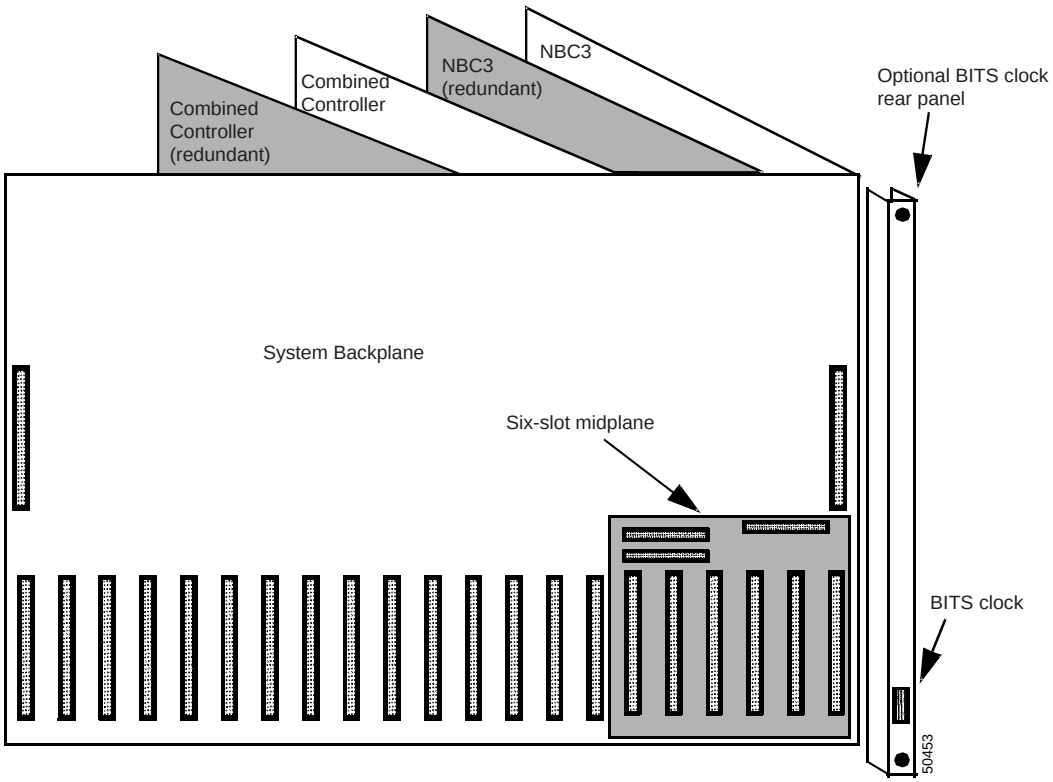
Table 2-8 NBC3 External Interfaces

Connections	VCO/4K
NBC3 to SWI	NBC3 and Combined Controller Assembly are connected to the six-slot midplane on the rear of the system backplane.
BITS Clock	DB-9 connection on NBC3 card front panel.[1]
Debugging	EIA/TIA-232 connection on the NBC3 front panel. This is not for customer use.

1. A BITS clock cable kit is available that routes the BITS signals to the rear of the VCO/4K chassis. This allows easy access for external cabling.

Figure 2-18 shows the NBC3 interconnections for VCO/4K systems.

Figure 2-18 NBC3 Card Interconnections for VCO/4K Systems



NBC3 Status LEDs

The NBC3 card has seven status LEDs on the front panel, as shown in Figure 2-19. (The DTG-2 Presence LED is ON when a DTG-2 mezzanine card is installed on the NBC3 card.)

Figure 2-19 NBC3 Card Front Panel

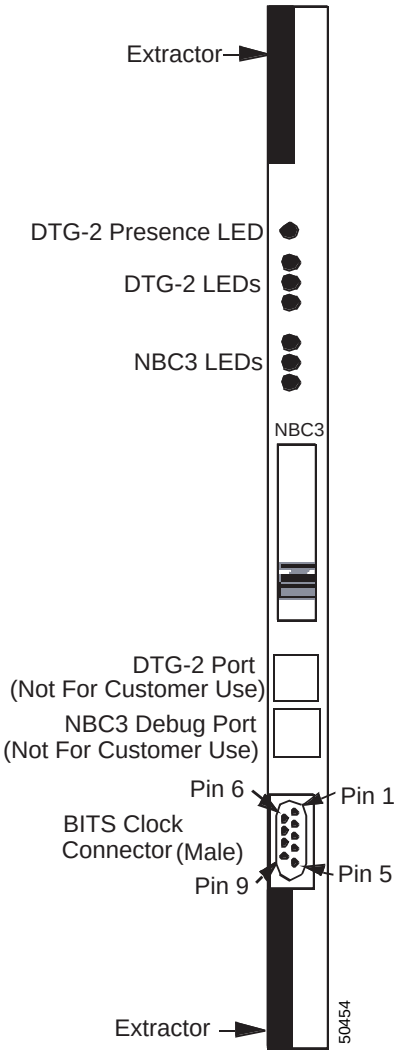


Table 2-9 lists the LED display for the DTG-2 mezzanine card.

Table 2-9 DTG-2 Mezzanine Card LED Display

Card Status	Green	Yellow	Red
Major DTG-2 card failure	Off	Off	On
Minor DTG-2 card failure	Off	On	Off
DTG-2 card is in standby, diagnostic, or out of service mode	On	Off	Off

Table 2-10 lists the LED display for the NBC3 card.

Table 2-10 NBC3 LED Display

Card Status	Green	Yellow	Red
Card plugged in (not initiated)	On	On	On
Card initializing/self testing	On	Blinking	Off
Card receiving download	Blinking	Off	Off
OOS/Admin menu/standby/maintenance/diagnostics/remote	On	Off	Off
Card operational/active	Off	Off	Off
Major alarm (see Table 2-11 for details)	Off	Off	On
Minor alarm (see Table 2-11 for details)	Off	On	Off
Self test failure or stop processing/card failure or register dump	On	Off	On

Table 2-11 lists the conditions that cause a major or minor alarm in the NBC3.

Table 2-11 NBC3 Minor and Major Alarms

Major Alarm	Minor Alarm
Loss of synchronization timing	Unable to communicate due to NBC3 or control circuit cards failure
Communications failure	Cannot obtain 32M lock
Receive buffer overrun encountered	Cannot obtain 3M lock
Transmit buffer overrun encountered	Receive buffer overrun pending
Comm Bus failure	Transmit buffer overrun pending

Connector J1 Pin Assignments

Table 2-12 lists the J1 pin assignments on the NBC3 card. J2 and J3 pin assignments are proprietary and, therefore, are not documented for customer use.

Table 2-12 NBC3 J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused

Table 2-12 NBC3 J1 Pin Assignments (continued)

Pin	Row A	Row B	Row C
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24 V	Unused	+24V
15	Battery (–48V)	Unused	Battery (–48V)
16	Battery (–48V)	Unused	Battery (–48V)
17	Battery (–48V)	Unused	Battery (–48V)
18	Analog (–15V)	Unused	Analog (–15V)
19	Analog (–15V)	Unused	Analog (–15V)
20	Analog (+15V)	Unused	Analog (+15V)
21	Analog (+15V)	Unused	Analog (+15V)
22	Card Address Bit 1	Unused	Card Address Bit 0
23	Card Address Bit 3	Unused	Card Address Bit 2
24	Card Address Bit 5	Unused	Card Address Bit 4
25	Card Address Bit 7	Unused	Card Address Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

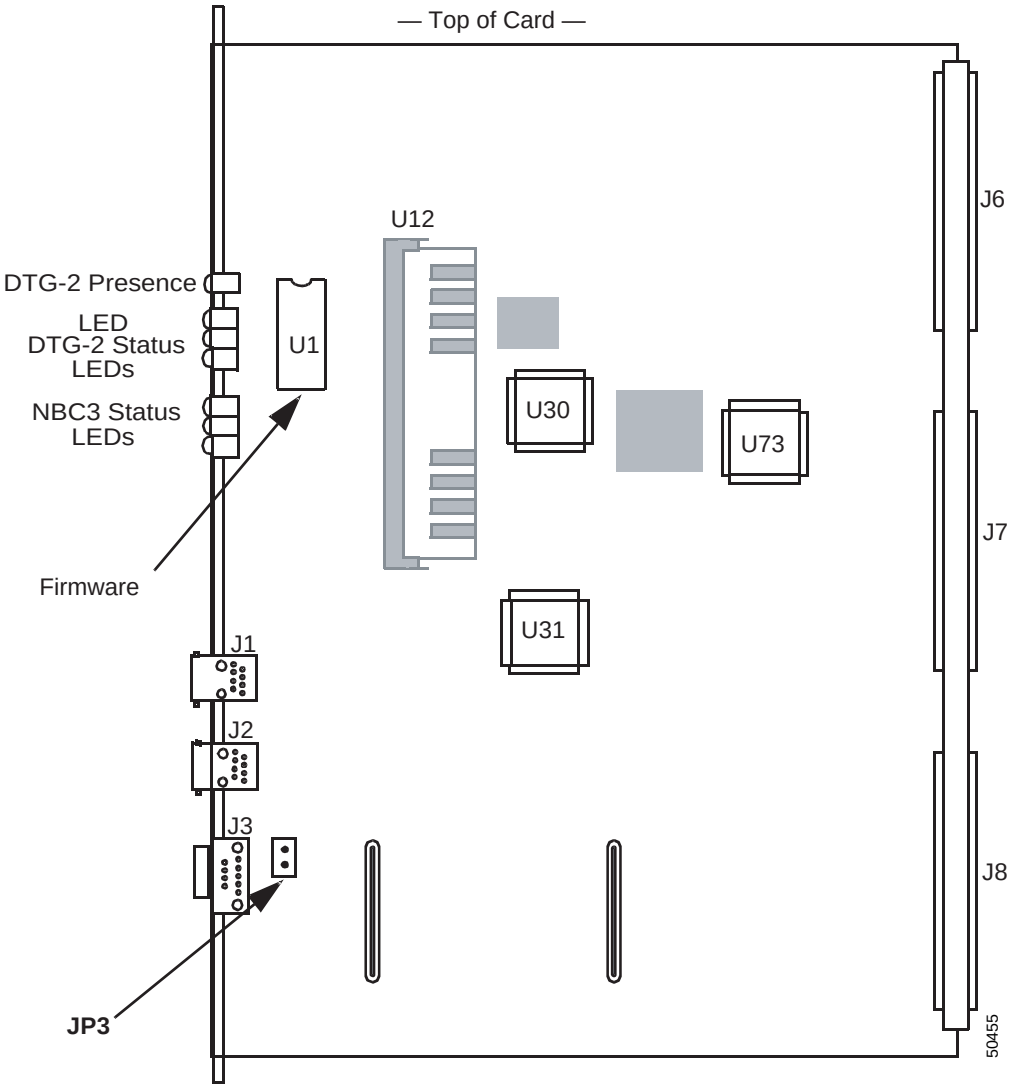
Configuration Notes

The NBC3 card is manufactured by Cisco Systems and includes firmware in the form of a PROM. All NBC3 jumpers except for the JP3 (Rev E) are factory set. If the NBC3 is the last destination of the composite clock signal, install a jumper at the J7/JP3 location to terminate the clock signal.

Figure 2-20 shows the location of the firmware PROM and the JP3 on the NBC3 Rev E card.

Caution Removing or repositioning the jumpers on an NBC3 card may cause system failures and damage to the card. Always verify that the jumpers are in their proper positions before installing or replacing an NBC3 card in the system.

Figure 2-20 NBC3 (Rev E) JP3 and Firmware Location



Note For Rev C cards the jumper is located at JP7, not JP3.

NBC3 Card Population Rules

The following card population rules apply to the NBC3:

- In nonredundant VCO/4K systems, the NBC3 must reside in slot 1 of the card rack.
- In redundant VCO/4K systems, the NBC3 cards must reside in slots 1 and 2 of the card rack.

Removal and Replacement Procedures

This section describes how to remove and replace the NBC3 card. The NBC3 card can be removed and inserted while the system is powered on.

Caution Do not pull the active side NBC3 on an operating production switch. Pulling an active NBC3 can generate errors and impact traffic. If you suspect a problem with an NBC3 card and you wish to remove it, first switch sides to make it the standby side.

Caution Observe antistatic precautions whenever handling the NBC3 to avoid damage to sensitive CMOS devices. Wear a ground strap connected to the system's equipment frame.

Removing an NBC3 Card

Perform the following steps to remove an NBC3:

Step 1 If you have a redundant system, verify that the NBC3 you want to remove is in the standby side. If the card is not in the standby side, run the Switch Active Side to Standby Utility as described in the *Cisco VCO/4K System Administrator's Guide* .

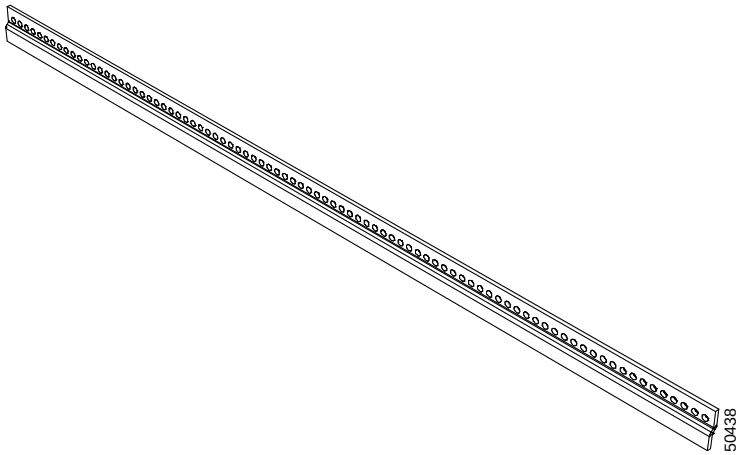
If the utility does not switch the system over, flip the SELECT toggle on the AAC to force the system to switch over. (Refer to the "Alarm Arbiter Card (AAC) with Alarm Interface Card (AIC)" section on page 2-1 for more information.)

Step 2 If you have a redundant system and the NBC3 has a DTG-2 mezzanine card, verify that the DTG-2 is in standby mode and take the DTG-2 card out of service.

Step 3 If you have a nonredundant system, shut down the system. If you have a redundant system, shut down the standby side.

Step 4 Use a #1 Phillips-head screwdriver to remove the mounting screws/washers from the top and bottom PCB card retainer bars (see Figure 2-21) on the system. Keep the retainers and screws together in a safe place for replacement later.

Figure 2-21 PCB Card Retainer Bar



Step 5 Disable the external alarm system to which the AAC might be connected.

Step 6 Disconnect all cables that are attached to the card (for example, BITS clock cable).

Step 7 Use your thumbs to pull the upper and lower extractors away from the card front panel. This action extracts the card from the backplane connectors.

Step 8 Pull the NBC3 free of the card slot.

Step 9 Place the card on an antistatic mat or envelope.

Replacing an NBC3

To replace an NBC3, perform the following steps:

Step 1 Place the replacement NBC3 card next to the removed card on the antistatic mat or antistatic envelope.

Step 2 Refer to your release notes and verify that the revision levels of the PROMs match the requirements of the generic software currently loaded in the system.

Step 3 Verify that the switch and jumper settings on the replacement NBC3 are the same as those on the removed card.

Step 4 Grasp the replacement NBC3 by the top handle and the bottom edge and align it with the top and bottom card guides of the subrack.

Step 5 Make sure the extractor levers are perpendicular to the front panel. Push the NBC3 in until it makes contact with the master port subrack backplane. The hooks on the extractors must be behind the front rail of the subrack. Use your thumbs to push the extractors toward the front panel.

Step 6 If you are using the BITS clock option, reconnect the clock source to the DB-9 connector on the NBC3 front panel.

Step 7 Enable the external alarm system connected to the AAC terminals.

Step 8 If you have a nonredundant system, reboot the system. If you have a redundant system, reboot the standby side. (Refer to the *Cisco VCO/4K System Maintenance Manual* for more information.)

Step 9 If you have a redundant system, flip the SELECT toggle switch on the ACC to the AUTO position.

Step 10 The DTG-2 is automatically brought into service when the NBC3 is downloaded. If the DTG-2 card fails to automatically come into service, change the card status to active from the master console Card Maintenance menu. (Refer to the *Cisco VCO/4K System Administrator's Guide* for more information.)

Step 11 Reinstall the top and bottom PCB card retainer bars (see Figure 2-21). Use a #1 Phillips-head screwdriver to replace the mounting screws/washers (five per bar).

Caution The PCB card retainer bars must be installed for the system to meet NEBS Zone 4 Earthquake compliance.

Troubleshooting

Because problems with the NBC3 critically affect system operation, the generic software provides numerous system error messages describing what type of NBC3 fault is detected. These error messages are fully described in *Cisco VCO/4K System Messages*.

A special set of messages which identify problems with T1 and NBC3 synchronization is also provided in *Cisco VCO/4K System Messages*.

Troubleshooting Procedures for Nonredundant Systems

When an NBC3 major alarm occurs in a nonredundant system, the AAC initiates a system reset. The CPU is cleared of all current data and all calls in progress are dropped. Service disruption lasts until the entire reset process is complete.

If the system reset fails to restore NBC3 operation on VCO/4K systems, replace the NBC3 card. See the "Replacing an NBC3" section on page 2-49 for replacement procedures.

Troubleshooting Procedures for Redundant Systems

Verify that the system switched over so that the malfunctioning NBC3 is on the standby side. If the system did not switch over, flip the SELECT toggle on the AAC to force the system to switch over. (Refer to the "Alarm Arbiter Card (AAC) with Alarm Interface Card (AIC)" section on page 2-1 for more information.)

If the reset fails to restore NBC3 operation, replace the NBC3 card. See the "Replacing an NBC3" section on page 2-49 for replacement procedures.

CHAPTER 3

Network Interface Cards

Drop and Insert Card (D+I)

The Drop and Insert (D+I) card provides DS0 transmission-only access to the VCO/4K system. It supports a maximum of eight interfaces per card, synchronous operation at either 56 KB or 64 KB. The D+I card is configurable as DCE or DTE with normal or reverse bit-packing, and supports both EIA/TIA-449 and V.35 signal specifications for dates and clock leads only. The D+I card can be inserted into the system while the system is active.

Administration of the card is performed through the existing system administration console. Configuration messages are sent to the card from the system software through the NBC/NBC3 interface.

Specifications

Microprocessor:	68360 (25 MHz)
Memory:	4 MB DRAM
	256 KB EPROM
Power Requirements:	+5 Volts 4 amps
	–15 Volts 0.5 amps
I/O Port Specifications:	
Input Level:	EIA/TIA-449 or V.35 (date and clock only)
Output Level:	EIA/TIA-449 or V.35 (date and clock only)

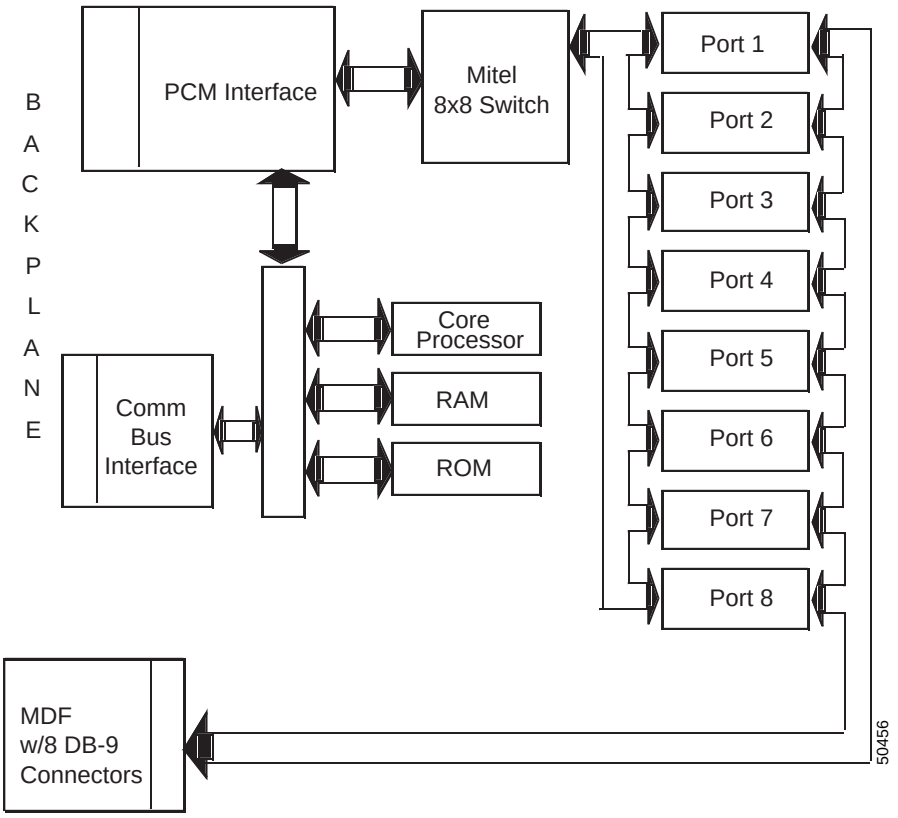
Note The DB-9 to DB-37 cable for DCE operation can be ordered from Cisco Systems.

Circuit Description

Figure 3-1 shows a block diagram of the D+I card. The major elements of the card are:

- Mitel switch
- Core processor
- PCM interface
- Communications bus (comm bus) interface
- Port interface

Figure 3-1 Block Diagram of the D+I Card



The core processor controls the eight synchronous serial links and communicates to the Network Bus Controller (NBC3) via the comm bus. The comm bus interface handshakes all signals with the NBC3, and moves data to and from memory through dedicated DMA channels present on the core CPU.

Mitel Switch

Each D+I port is connected to the Mitel 8985 voice/data switch. The Mitel switch switches data packets between multiple serial PCM highways generated within the PCM interface.

Core Processor

The core processor is a Motorola MC68360, a highly integrated microprocessor that can implement most of the core processor requirements through on-chip peripherals. The 68360 operates at 25 MHz.

The core processor has an EIA/TIA-232 port that is accessible from the face plate via an RJ-45 jack. The electrical signals are +12V and –12V (EIA/TIA-232).

PCM Bus

The VCO/4K uses the PCM bus to move voice and data traffic between port cards. The NBC/NBC3 supplies clocking.

The PCM interface controls the following:

- Independent dynamic timeslot assignment for transmit and receive matrices
- Full utilization of PCM buses A and B for a total of 1776 available timeslots maximum.

Comm Bus Interface

The core processor communicates with the NBC/NBC3 through the comm bus interface, which is implemented with the two DMA channels provided on the MC68360. One channel is dedicated to moving data off the comm bus, and one channel is dedicated to placing data on the comm bus.

Port Interface

The D+I card contains eight synchronous ports that can be individually configured by the system administrator. Because each D+I port interfaces to the VCO/4K, modem control signals are not provided. Only transmit and receive, clock and data signals are provided.

Users may select from the following features and configure the card on a per port basis:

- 56 kbps or 64 kbps
- DCE or DTE
- Bit ordering (normal or reverse)
- Loop back

Clock Rate

Each D+I port is capable of operating at either 64 kbps or 56 kbps. The user selects the operating rate through system administration screens. Refer to the *Cisco VCO/4K System Administrator's Guide* for information on the D+I screens.

Communication Link

Each D+I port communicates over either an EIA/TIA-449 or V.35 link (designed for transmission only). Refer to Figure 3-2 for the appropriate wiring for the link.

On the port side, the cable connects via a 9-pin D-sub connector. On the equipment side, the cable connection is customer supplied and is dependent on the type of link. The cable pinouts for the D+I in DTE or DCE mode are different. Specific cables are required for each type of link.

If you are cabling the D+I card to the VCO/4K integrated SS7 system, note that a DB-9 to DB-37 cable is available from Cisco.

DCE/DTE Operation

Each D+I port is individually capable of operating as either a DCE or DTE, as selected by the system administrator. When configured for DCE operation, the port uses the system clock to create the transmit and receive clocks. In DCE mode, the transmit and receive data path is not subject to data slips. This is the preferred configuration.

When configured for DTE operation, the port uses the received clocks to transmit data as well as receive data. Because receive clocks may not be locked to the VCO/4K system clock, the transmit and receive data paths are subject to data slips. In DTE mode, the port may lose its transmit and receive clocks. (Refer to the *Cisco VCO/4K System Administrator's Guide* for information on selecting DCE or DTE operation.)

Each port has a transmit and receive loss of clock (LOC) detector. When a port is in DTE mode and an LOC occurs, or an LOC condition clears, the core processor is informed via an interrupt. When a port is in DCE mode, no LOC events occur.

Pin Assignments

Each port has the following signals:

- Receive clock—INPUT (DTE)/OUTPUT (DCE)
- Receive data—INPUT
- Transmit clock—INPUT (DTE)/OUTPUT (DCE)
- Transmit data—OUTPUT

Note The D+I card cannot be used as a system clock reference source.

The D+I port only operates in a synchronous mode and as such, only the Data and Clock signals are provided. All I/O signals exit the board through the J3 connector, and an MDF board provides the interface to eight DB-9 female connectors. The eight female DB-9 connectors provide the necessary signals for EIA/TIA-449/V.35 connection.

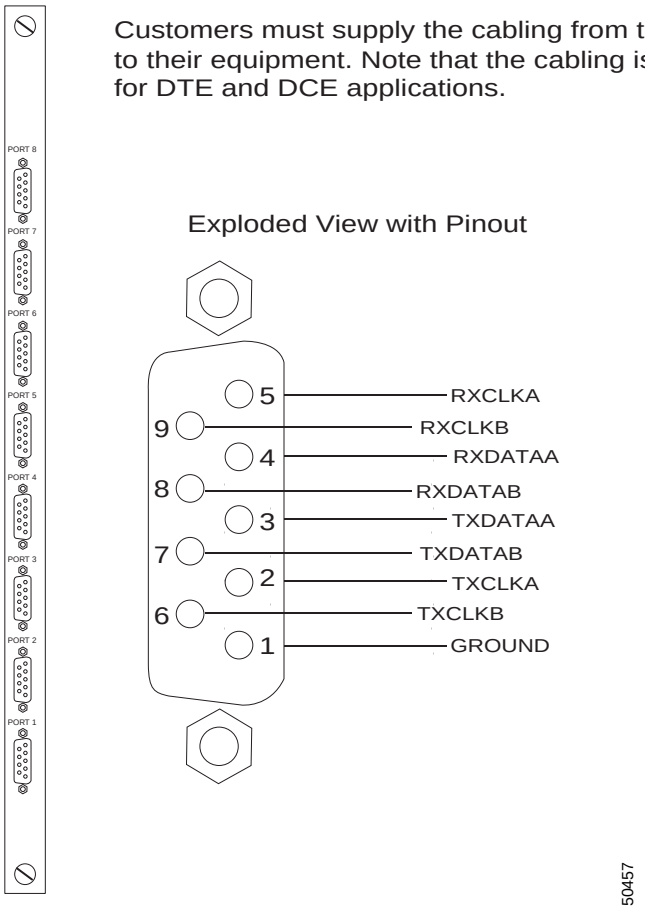
The DB-9 pinout is shown in Table 3-1.

Table 3-1 DB-9 Pinout

Ground	Pin 1	GND
Transmit Clock A	Pin 2	TXCLKA
Transmit Clock B	Pin 6	TXCLKB
Transmit Data A	Pin 3	TXDATAA
Transmit Data B	Pin 7	TXDATAB
Receive Clock A	Pin 5	RXCLKA
Receive Clock B	Pin 9	RXCLKB
Receive Data A	Pin 4	RXDATAA
Receive Data B	Pin 8	RXDATAB

Figure 3-2 illustrates the DB-9 pinout.

Figure 3-2 D+I MDF and DB-9 Pinout



Bit Packing Order

Users may select normal or reverse bit ordering. The bits may be packed into a PCM byte in normal or reverse order as shown in Table 3-2.

Table 3-2 Bit Packing Order

Mode	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
64 kbps Normal	1st bit	2nd bit	3rd bit	4th bit	5th bit	6th bit	7th bit	8th bit
56 kbps Normal	1st bit	2nd bit	3rd bit	4th bit	5th bit	6th bit	7th bit	Fixed at 0

Table 3-2 Bit Packing Order (continued)

Mode	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
64 kbps Reverse	8th bit	7th bit	6th bit	5th bit	4th bit	3rd bit	2nd bit	1st bit
56 kbps Reverse	7th bit	6th bit	5th bit	4th bit	3rd bit	2nd bit	1st bit	Fixed at 0

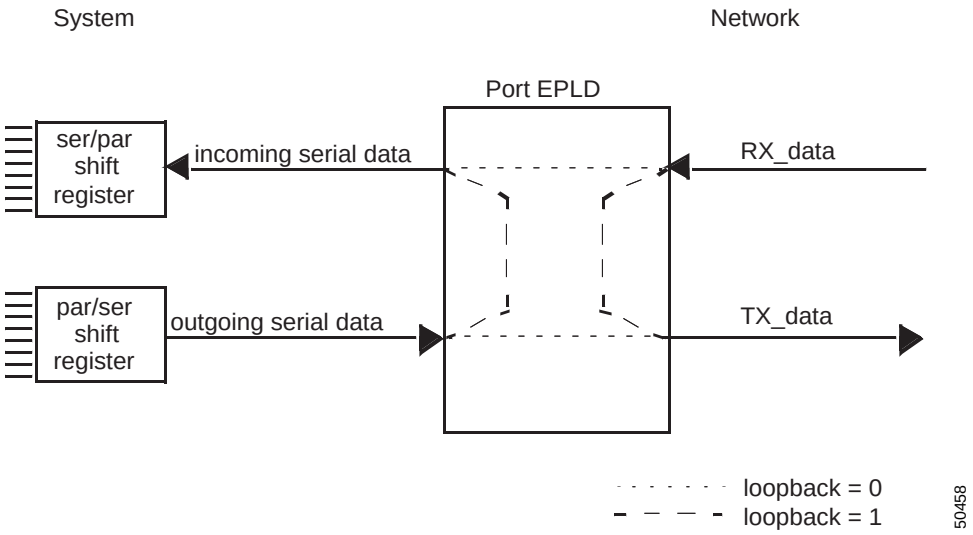
Loopback Mode

Each D+I port is capable of looping back the data presented at each interface. When you place a port in loopback, the data received at the port is looped back to the port transmit path without going through the FIFOs or slip circuits. Loopback also enables transmit data from the transmit PCM bus to go through the (Mitel) voice/data switch to the port controller EPLD, back through the voice/data switch, to the receive PCM bus.

The port EPLD provides all clock selection and synchronization, control of the port side of the FIFOs, error detection, and loopback. All input signals to the EPLD are synchronized with the internal 8 MHz clock so that the state machines are synchronous.

The Rx and Tx data is sent directly from the port interface, and the incoming and outgoing serial data goes to the shift registers prior to the FIFOs.

Figure 3-3 Data Loopback



Interface Controller Card (ICC)

The Interface Controller Card (ICC) is a high-capacity network interface engine. The ICC employs a midplane architecture which enables it to connect with a series of I/O modules specific to different network interface requirements. The midplane isolates the unique physical characteristics of each type of connection leaving the ICC to perform all of the signaling and protocol processing independently. There are six I/O modules supporting 4, 8, or 16 network spans. A C-bus enabled, VCO switching platform (VCO/4K Series) with a full complement of ICCs and 16-span I/O modules will support more than 4000 ports.

For information on the I/O modules, refer to the “Interface Controller Card T1 I/O Module” section on page 3-15, or the “Interface Controller Card E1 I/O Module” section on page 3-23, depending on your network requirements.

The ICC is fully programmable, enabling user control over individual channels.

Other features:

- Contains on-board Flash memory for rapid configuration and boot-up time
- Managed from Cisco’s Administration Console
- Supports SNMP protocol
- Can be installed on both C-bus and non-C-bus systems (lower port capacity)
- Derives all on-board voltages from the +5V system supply
- May use any span as an incoming master timing source
- With 16 spans each, 11 cards will support 4080 T1 timeslots, or 8 cards will support 4064 (clear channel) E1 timeslots.

Restrictions:

- Supported by VCO Series systems only (VCO/4K Series for maximum ports)
- C-bus must be enabled for the increased port capability
- All spans on a card must be of the same network type

Specifications

Compliance with Standards

The ICC is in compliance with all applicable U.S. and international standards. See Table 3-3.

Table 3-3 Standards Compliance

Category	Standard
Safety	UL1459
	CSA C22.2
	EN-60950
	IEC-950
EMI/EMC	FCC Part 15 (US/Canada)
	EN55022 (Europe)
	EN50082-1 (Europe)
	VCCI (Japan)
PCB Manufacture	IPC

ICC Specifications

Microprocessor	MPC860MH-50
Memory	8 MB Flash, 16 MB DRAM SIMM
Power Requirements	5 Volts – 3.5A (Typical)

ICC Architecture

The ICC is a single-slot card. A separate I/O module provides access to the network interfaces. The I/O module includes active circuitry such as T1/E1 framers and is unique to each network configuration. Regardless of the span configuration, the CPU card is common.

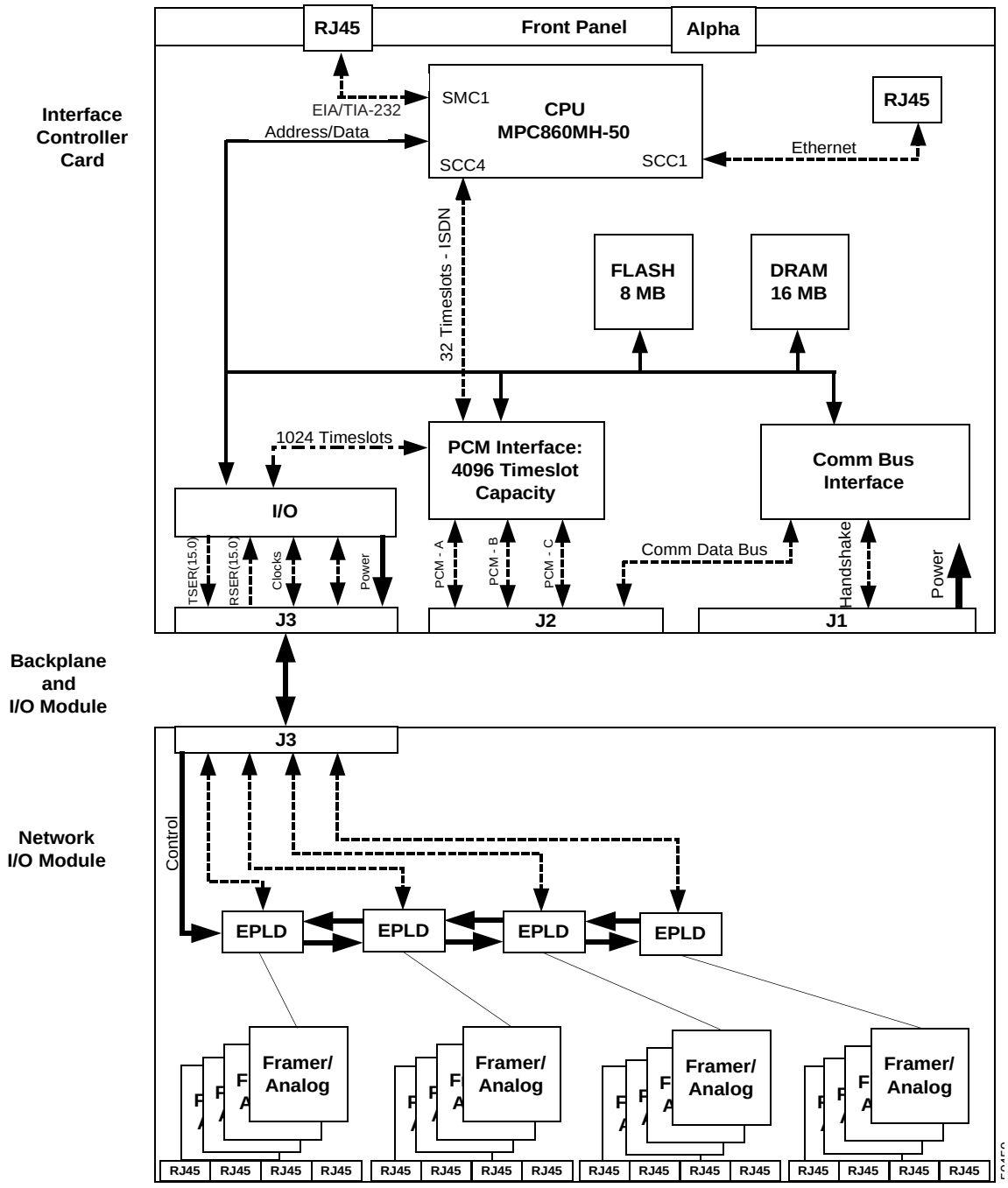
The ICC is inserted in the VCO/4K from the front of the system. An I/O Module, inserted at the rear of the system, aligns with each ICC.

The ICC contains the following functions:

- Core CPU and memory subsystem
- Communications Bus Interface
- PCM Interface
- I/O Interface

The block diagram for the ICC and I/O Module is shown in Figure 3-4.

Figure 3-4 ICC and I/O Module Architecture



CPU and Memory Architecture

The Core Processor coordinates all activities of the ICC including:

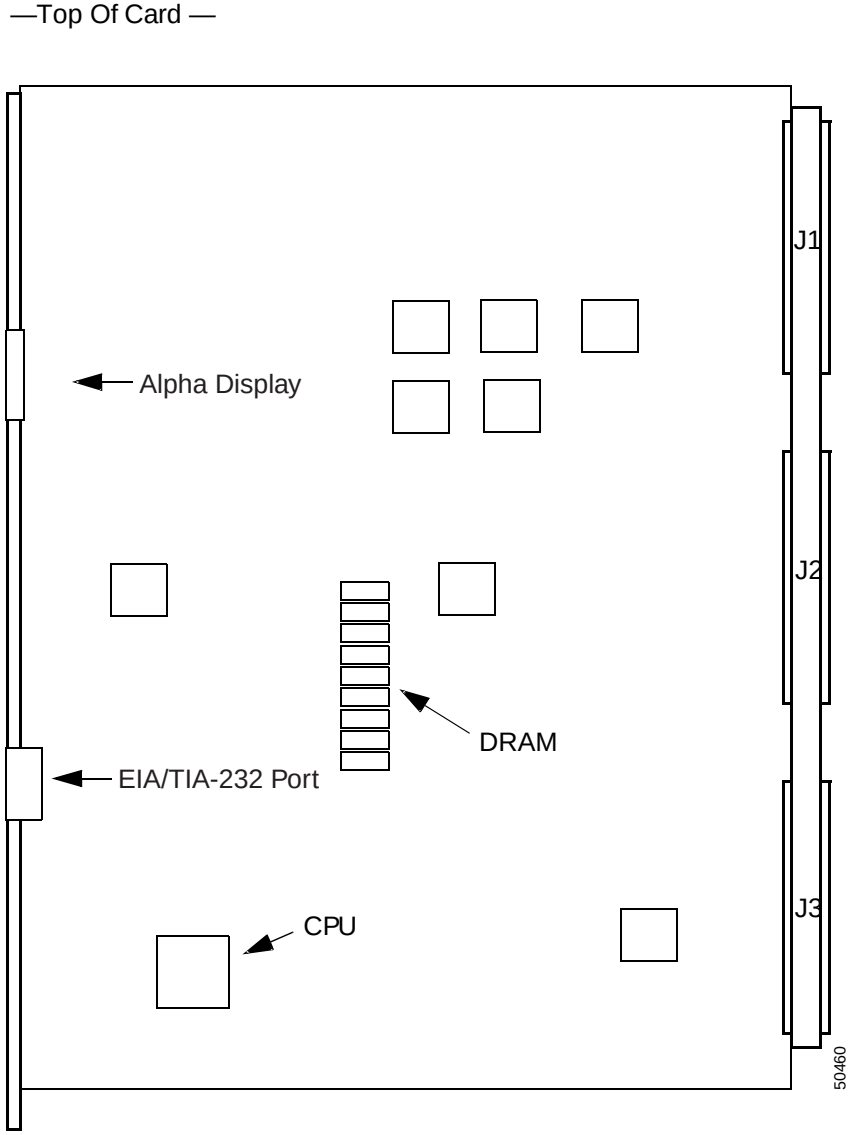
- Controlling timeslot assignments on the PCM buses
- Controlling up to 16 network interfaces

- Communicating with the NBC over the comm bus (Tx/Rx FIFOs)
- Managing the PCM timeslot assignments for voice traffic (Tx/Rx SMXs)
- Managing PCM law conversion and gain control (Tx/Rx lookup table SRAM)
- Managing the telephony components of each network interface (Framers)
- Controlling the Alpha display on the faceplate

The MPC860 processor controls up to 16 network trunks and manages all aspects of the network interface such as framing, call control, mu-law/a-law conversion, gain control, etc.

The MPC860 processor communicates to the Network Bus Controller (NBC) via the comm bus. The comm bus interface is controlled primarily by dedicated hardware. The comm bus interface handshakes all signals with the NBC and retrieves data from, and stores data to memory, by interrupting the MPC860 at the end of a cycle.

Figure 3-5 ICC Layout (Component Side)



SMC1–EIA/TIA-232 Port

The MPC860 Processor has one EIA/TIA-232 port, which is accessible from the face plate. This port utilizes an RJ-45 jack. The electrical signal levels are EIA/TIA-232 compliant.

Note The front panel RJ-45 jack is not intended for customer use.

FLASH Memory

The Flash memory boots the processor so that the application and/or diagnostic software can be downloaded over the comm bus when new revisions are required. The boot Flash is 8 MB.

DRAM Module

The MPC860 processor has an EDO DRAM array of 16 MB on a 72-pin SIMM memory device (similar to a PC memory). The EDO DRAM array is arranged in a 32-bit arrangement, and is controlled by the on-chip DRAM controller provided by the MPC860.

Alpha Display/Power Failure LED

The ICC displays status on a 5x7 Alpha display located on the ICC front panel. Table 3-4 defines the Alpha display states.

Note The ICC has a card failure LED immediately above the Alpha display. This LED indicates a major ICC or I/O card circuit failure. Replace the cards if this is lighted.

Table 3-4 Alpha Display States

Display	Meaning
B	Blue Alarm
D	D-channel failure
E1	Card is E1
F	Framing Error
M	Maintenance
N	No I/O Module
O	Out-of-Service
R	Red Alarm
T1	Card is T1
Y	Yellow Alarm
Download Progress Meter	Rotating line pattern

Only the most severe alarm state is displayed on the LED.

The bottom row of the LED matrix identifies which group of spans is reporting the alarm. The leftmost LED indicates group 1, the next LED indicates group 2, etc. The fifth, right most, LED indicates the state of the core processor. If this fifth LED stops blinking, the card should be removed and reinserted. If the LED still fails to blink, replace the card.

Table 3-5 lists the conditions that cause a major or minor alarm in the ICC.

Table 3-5 ICC Alarm Conditions

Major Alarm	Minor Alarm
Loss of Carrier	Slip Threshold Exceeded
	OOF Threshold Exceeded
	Loss of Remote Carrier
	Signaling Bit Error
	OOF Error
	Out-of-Service (OOS)

Communications Bus Architecture

The MPC860 processor uses the comm bus to communicate with the NBC. The comm bus Interface protocol is managed mostly by hardware, although CPU control is required. An EPLD controls the handshaking and read/write strobes to two FIFOs which store inbound and outbound packets.

The communications bus has the following associated functions:

- Communicates with other boards on the backplane through the comm bus.
- Initiates all data transfers on the comm bus.
- Sends messages to just one card.

The comm bus is a one-byte-wide half-duplex interface. This interface facilitates the transfer of messages between the port cards and the NBC3.

The comm bus architecture of the ICC is responsible for:

- Managing the signal handshaking to/from the NBC (via EPLD)
- Managing packet storage (in and outbound FIFOs)
- Managing packet termination to/from CPU (via EPLD)

The comm bus architecture supports directed downloads.

PCM Interface

Bus Support

There are three PCM buses on the Cisco Systems backplane, known as the A, B, and C Buses. These are 8-bit parallel buses running at 8.192 MHz, with the exception of the C-bus which runs at 16.384 MHz. The C-bus is used with the ICC to achieve 4K ports.

Transmit Gain/Law Conversion

Each inbound and outbound timeslot has the ability to apply mu-law/a-law conversion and gain control. The gain/law conversion occurs between the SMX-controlled Transmit PCM DPRAMs and the Transmit PAC.

The available gains are: 0 dB, -3 dB, -6 dB, -12 dB, +1.5 dB, +3 dB, +6 dB, and +12 dB.

I/O Interface

The J3 connector is the interface between the I/O Module and the ICC. This includes the following: functions:

- Signal buffering
- Transmit clock configuration (per framer)
- Reference clock selection
- Framer host interface and interrupt control

Programmability

You download the application software to each span controller, enabling independent provisioning of each span as well as each channel.

The ICC supports a number of programmable parameters which allow card customization:

- Network programmable protocol
- Line build-out
- Gain control
- Companding law
- Timing for system synchronization
- Transmitted timing source
- Line coding
- Frame control

Cisco can assist in creating your parameters on a floppy disk which you load into the VCO.

Protocol Implementation

Support for network protocols is provided by a state machine (the Protocol State machine) that operates on the ICC. This is a software module that defines how the ICC will behave as a result of specific events.

The state machine performs an action for each predefined event. This state machine is fully programmable, allowing any action to take place as a result of any specific event. This allows predefined configuration of a port or span. Standard network (T1, E1) protocols are preprogrammed. The standard protocols may be modified to meet specific needs and saved as a customized protocol or a new protocol can be developed. All protocols (preprogrammed, modified, or newly developed) are stored with a unique identifier.

To configure the ICC with a new protocol, select one or more ports/spans on which the protocol will be executed. The protocol configuration information is transmitted to the ICC when each span is activated.

Network Considerations

A standard or user-defined protocol is implemented at the port level when the ICC is configured as a T1 card and implemented at the span level when configured as an E1 card. Also, to configure the port (T1) or span (E1) with any protocol, the port or span cannot have active calls. The port or span must be placed in the OOS state when changing protocol configuration.

Configuration Notes

The ICC is software configurable via downloads. There are no jumpers or replaceable PROMs on the ICC.

Interface Controller Card T1 I/O Module

The VCO/4K uses active I/O modules in conjunction with the ICC to connect to the network. Each I/O Module uses one slot on the backplane and supports one ICC. The I/O Module is located at the back of the switch and must be aligned with the ICC. A block diagram for the ICC I/O Module is shown at the bottom of Figure 3-6.

The T1 I/O Module is a specialized backplane card that provides T1 network connection to the ICC. It is available in three configurations supporting 4, 8, or 16 T1 spans. The ICC is inserted in the VCO switch from the front of the system. The I/O Module, inserted at the rear of the system (before ICC insertion), aligns with each ICC.

The T1 I/O module supports a 100-ohm network interface and includes active circuitry such as T1 framers.

For information on the ICC, refer to the “Interface Controller Card (ICC)” section on page 3-7.

Specifications

Compliance with Standards

The ICC I/O Module is in compliance with all applicable U.S. and international standards. See Table 3-6.

Table 3-6 ICC I/O Module Standards Compliance

Category	Standard
Safety	UL1459
	CSA C22.2
Jitter	Pub 62411
EMI/EMC	FCC Part 15 (US/Canada)
	VCCI (Japan)
PCB Manufacture	IPC
Lightning/Power Cross	CSA C22.2
	FCC Part 68
	CS-03
Telecom	FCC Part 68
	CS-03
	JATE
	AT&T Publication 62411
	Bellcore PUB43801
	TR-NPL-000054
	TR-TSY-000510
	TR-TSY-000191
	ANSI T1.403

I/O Module Specifications

Power Requirements (Maximum)	5 Volts (from the ICC) 4 Span T1 – 1.16A 8 Span T1 – 1.42A 16 Span T1 – 1.95A

Figure 3-6 ICC and I/O Module Architecture

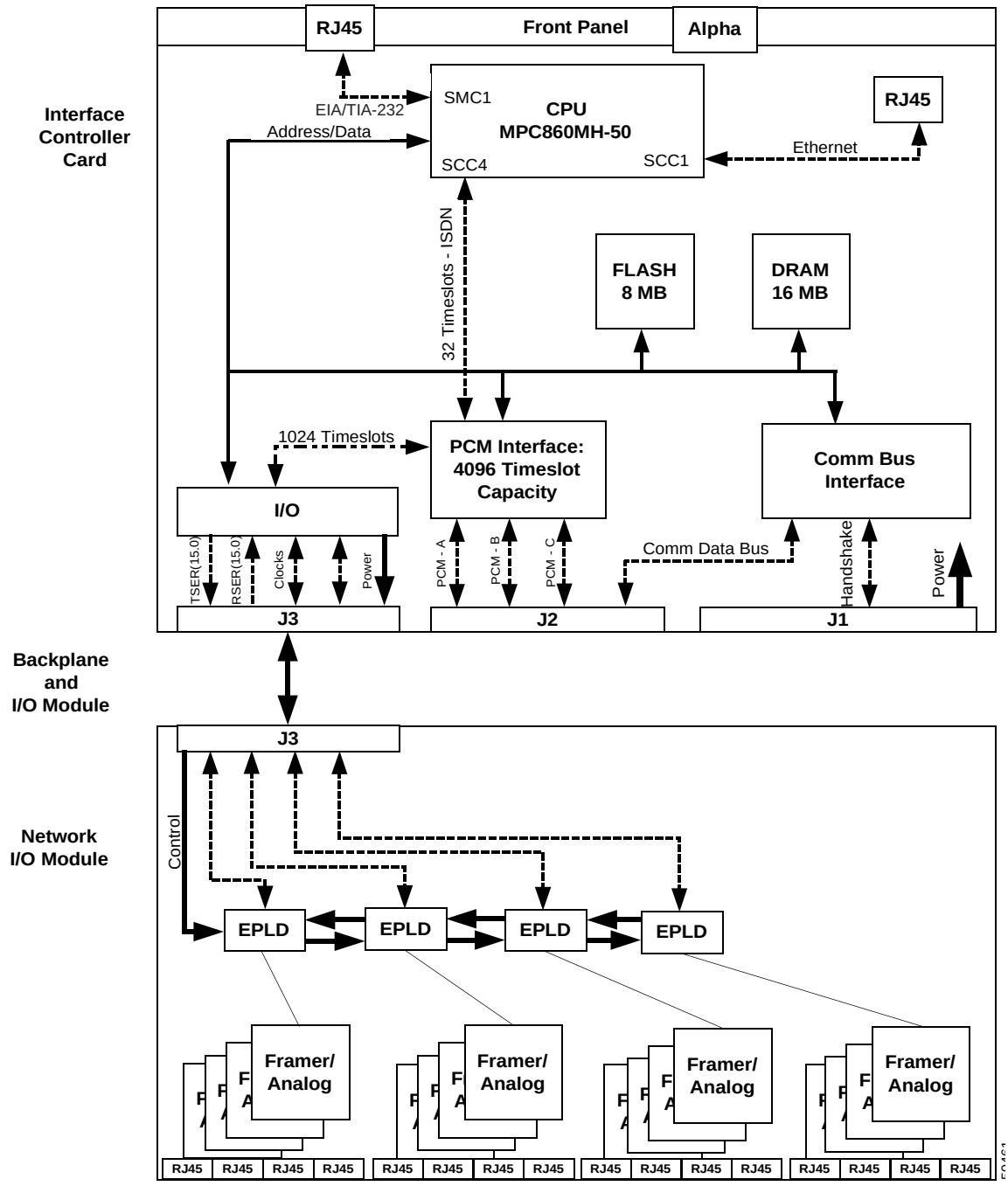
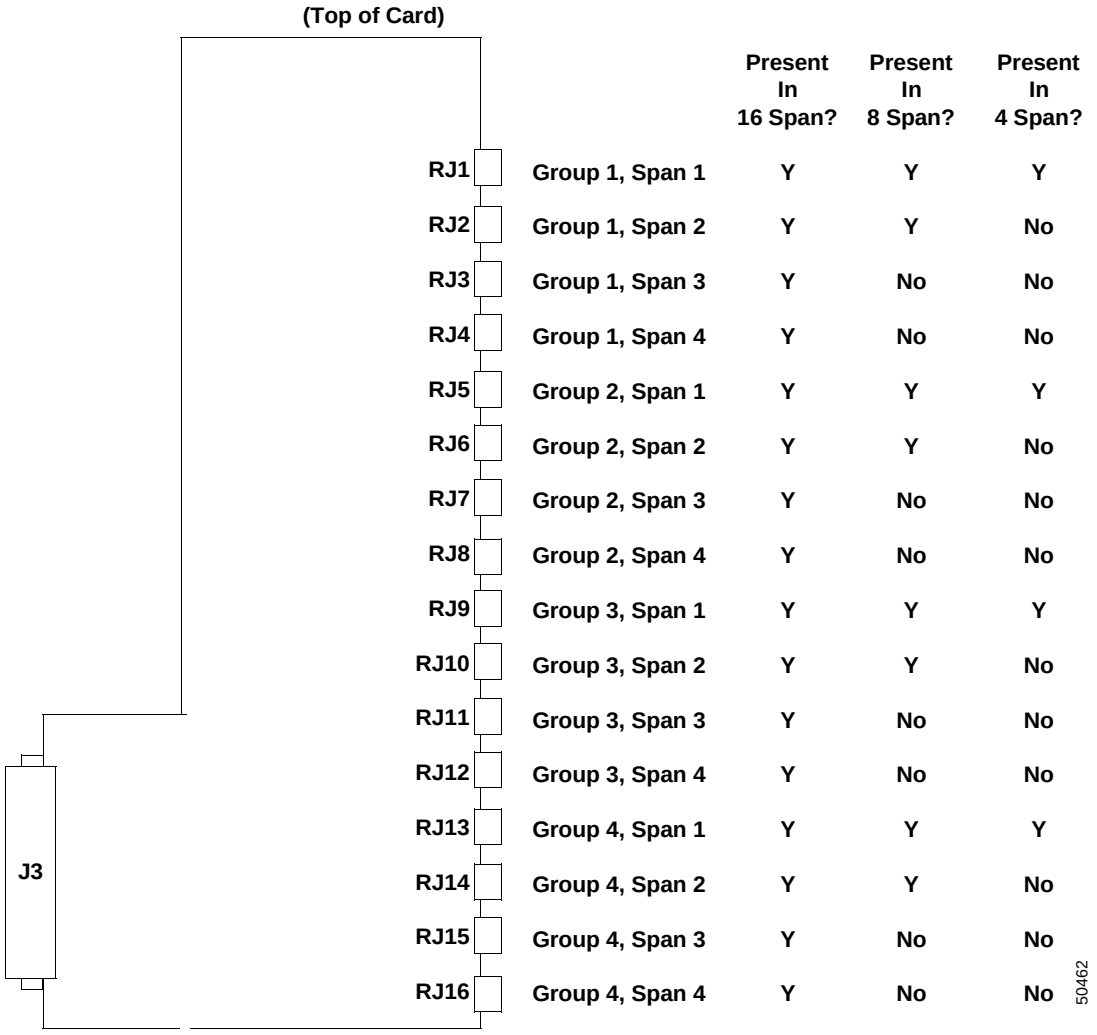


Figure 3-7 I/O Module Card Layout (16-Span, Circuit Side)



Note Not all components are shown.

External Interfaces

Table 3-7 and Table 3-8 list the pinouts for the RJ-45 female receptacles on the I/O module. Use these tables as a reference when you wire RJ-45 male connectors to cables at the installation site.

Table 3-7 lists the external interface for the I/O Module to the network. Table 3-8 lists the external interface for the I/O Module to the Cisco AS5300. Figure 3-8 shows the pin orientation for the RJ-45 connector.

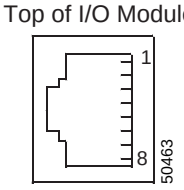
Table 3-7 RJ-45 Pinouts—VCO/Network

VCO Side	Network Side
Pin 1 Tx Ring	Network Rx Ring
Pin 8 Tx Tip	Network Rx Tip
Pin 4 Rx Ring	Network Tx Ring
Pin 5 Rx Tip	Network Tx Tip

Table 3-8 RJ-45 Pinouts—AS5300

VCO Side	AS5300 Side
Pin 1 Tx Ring	Pin 1 Rx Ring
Pin 8 Tx Tip	Pin 2 Rx Tip
Pin 4 Rx Ring	Pin 4 Tx Ring
Pin 5 Rx Tip	Pin 5 Tx Tip

Figure 3-8 RJ-45 Connector



Programmability

You download the application software to each span controller, enabling independent provisioning of each span as well as each channel.

The ICC supports a number of programmable parameters which allow card customization:

- T1 programmable protocol
- Line build-out
- Gain control
- Timing for system synchronization
- Transmitted timing source
- Line coding
- Frame control

Cisco can assist in creating your parameters on a floppy disk which you load into the VCO/4K.

I/O Interface

The J3 connector is the interface between the I/O Module and the ICC. This includes the following functions:

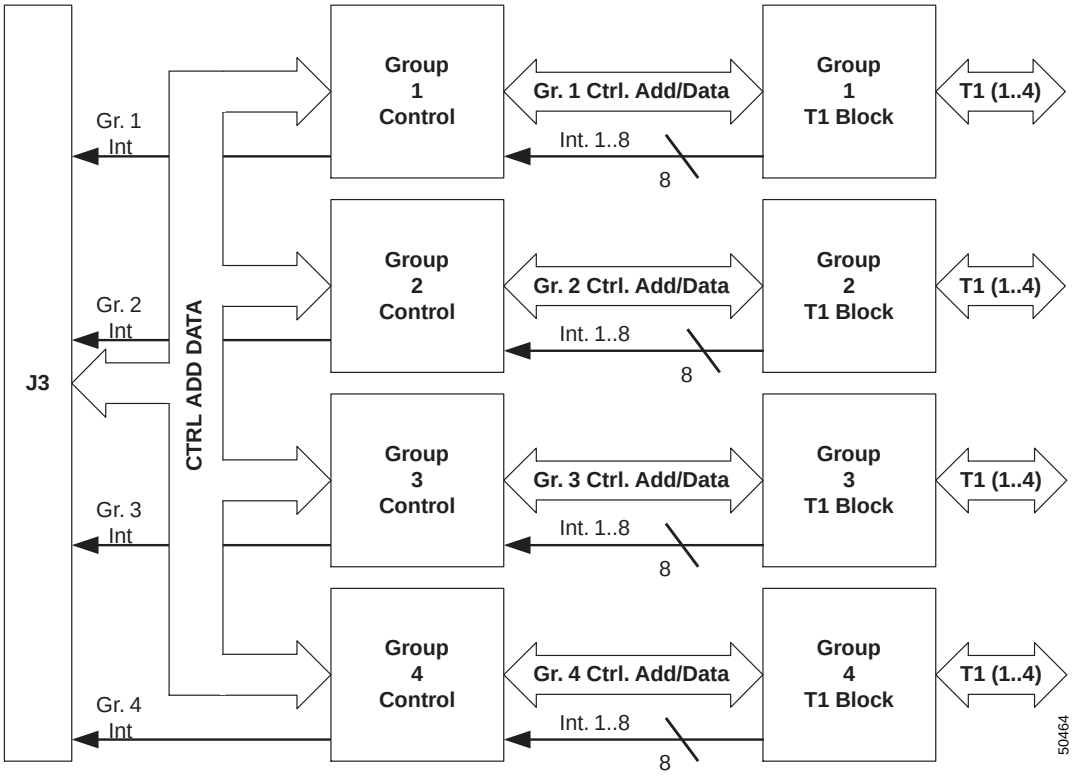
- Signal buffering
- Transmit clock configuration (per framer)
- Reference clock selection
- Framer host interface and interrupt control

I/O Module Description

The I/O Module interfaces the VCO/4K system with 4, 8, or 16 T1 digital data carrier streams. Each stream consists of a 1.544-Mbps, 24-channel, bipolar digital data stream. VCO system synchronization may be set to the receive clock of any T1 span on the I/O Module (the Master Timing Link).

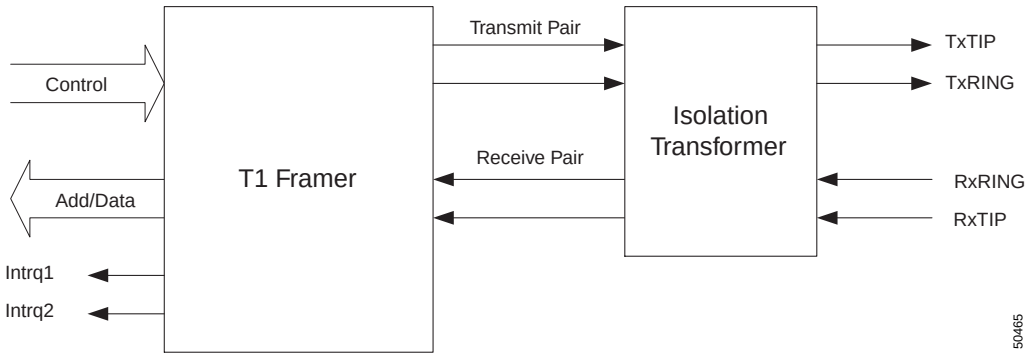
The I/O module's framers are segmented into groups of four called Framer Groups. This design approach reduces the chance of a single point of failure on the card. A hardware failure on the I/O Module normally affects only a group (1, 2 or 4 spans) and not the entire I/O Module. Figure 3-9 illustrates the span grouping architecture of the I/O Module.

Figure 3-9 16-Span I/O Module Span Grouping



The T1 framer (Figure 3-10) contains a Line Interface Unit (LIU). The LIU contains three sections: 1) the receiver which handles clock and data recovery, 2) the transmitter which wave shapes and drives the T1 line, and 3) the jitter attenuator.

Figure 3-10 Framer Block Diagram



The LIU adjusts to the T1 signal being received and can handle T1 transmit line lengths from 0 to 655 feet as configured from the Port Configuration screen (See the *Cisco VCO/4K System Administrator's Guide*).

Circuitry on the I/O card detects loss of carrier errors, framing errors, and remote alarms on its incoming T1 stream. It also detects receive/transmit *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different rate, such as in loop-timed configurations. The ICC contains elastic PCM data buffers to minimize slips caused the T1 stream frequency jitter.

Table 3-9 details the T1 I/O Module's input and output stream specifications.

Table 3-9 T1 Stream Specifications

Input Stream	
Format	D3/D4 or ESF
Data transparency	Alternate Mark Inversion (AMI), Bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, none.
Frequency	1.544 Mbps +/- 76 bps
Impedance	100 ohms
Output Stream	
Format	D3/D4 or ESF
Data transparency	Alternate Mark Inversion (AMI), Bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, none.
Line Equalization (Drive)	0 to 655 ft
Frequency	1.544 Mbps +/- 76 bps
Impedance	100 ohms

The combined framer/LIU performs the following functions:

- Alarm detection (Yellow, Blue, Carrier Lost, Loss of Sync)
- Alarm injection (Yellow and Blue alarms)
- Channel separation

- D4/ESF framing (D4 Superframing and Extended Superframe)
- Robbed bit signaling/channel (A, B, C, and D)
- Data transparency
- AMI, B8ZS data encoding

Note You can use B8ZS for T1 to maintain 1s density (and timing) while providing data transparency.

- Bipolar-to-TTL conversion on the receive side
- Electrical wave shaping on the transmit side
- Clock recovery
- Jitter attenuation, tolerance, and transfer (AT&T 62411 1990)
- Line build-out selection
- Loopback and maintenance functions
- All ones (1s) generation
- Signal monitoring (for loss of signal and quality transmission)

Configuration Notes

There are no jumpers or replaceable PROMs on the I/O Module.

Interface Controller Card E1 I/O Module

The VCO/4K uses active I/O modules in conjunction with the ICC to connect to the network. Each I/O Module uses one slot on the backplane and supports one ICC. The I/O Module is located at the back of the switch and must be aligned with the ICC. A block diagram for the ICC I/O Module is shown at the bottom of Figure 3-11.

The E1 I/O Module is a specialized backplane card that provides E1 network connection to the ICC. It is available in three configurations supporting 4, 8, or 16 E1 spans. The ICC is inserted in the VCO/4K switch from the front of the system. The I/O Module, inserted at the rear of the system (before ICC insertion), aligns with each ICC.

The E1 I/O module supports a 120-ohm network interface for E1 and includes active circuitry such as E1 framers.

Note The E1 I/O Module also supports a 75-ohm network interface when optional Balun impedance matching devices are used.

For information on the ICC, refer to the “Interface Controller Card (ICC)” section on page 3-7.

Specifications

Compliance with Standards

The ICC I/O Module is in compliance with all applicable U.S. and international standards. See Table 3-10.

Table 3-10 ICC E1 I/O Standards Compliance

Category	Standard
Safety	EN-60950
	IEC-950
Jitter	ITU G.823
EMI/EMC	EN55022 (Europe)
	EN50082-1 (Europe)
PCB Manufacture	IPC
Clocking/Framing	ITU G.703
	ITU G.704
Lightning/Power Cross	EN-60950
	IEC-950
Telecom	European country-specific

I/O Module Specifications

Power Requirements (Maximum)	5 Volts (from the ICC) 4 Span E1 – 1.16A 8 Span E1 – 1.42A 16 Span E1 – 1.95A

Figure 3-11 ICC and I/O Module Architecture

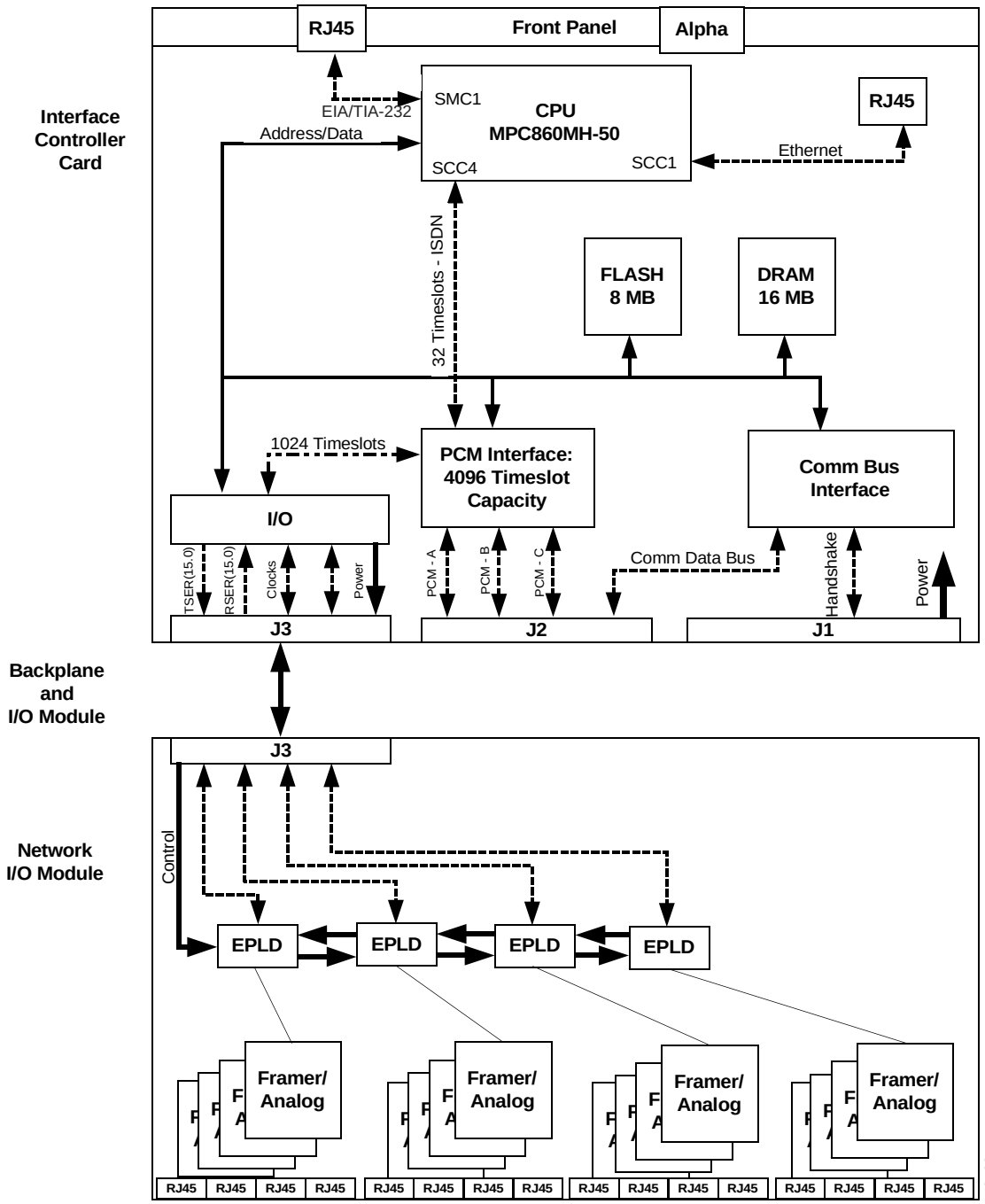
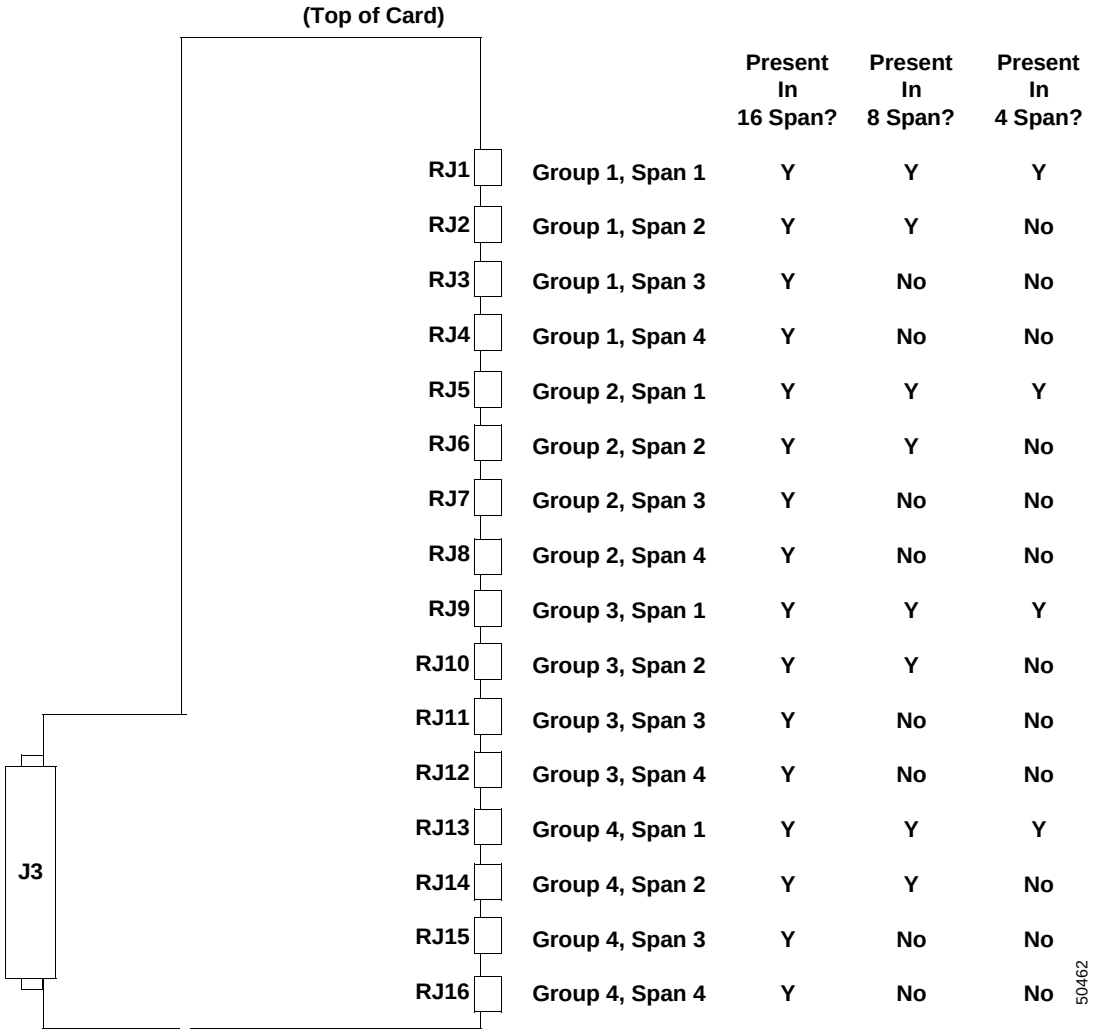


Figure 3-12 I/O Module Card Layout (16-Span, Circuit Side)



Note Not all components are shown.

External Interfaces

Table 3-7 and Table 3-8 list the pinouts for the RJ-45 female receptacles on the I/O module. Use these tables as a reference when you wire RJ-45 male connectors to cables at the installation site.

Table 3-7 lists the external interface for the I/O Module to the network. Table 3-8 lists the external interface for the I/O Module to the Cisco AS5300. Figure 3-13 shows the pin orientation for the RJ-45 connector

Table 3-11 RJ-45 Pinouts—VCO/Network

VCO Side	Network Side
Pin 1 Tx Ring	Network Rx Ring
Pin 8 Tx Tip	Network Rx Tip

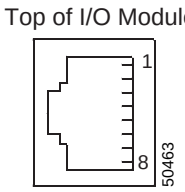
Table 3-11 RJ-45 Pinouts—VCO/Network (continued)

VCO Side	Network Side
Pin 4 Rx Ring	Network Tx Ring
Pin 5 Rx Tip	Network Tx Tip

Table 3-12 RJ-45 Pinouts—AS5300

VCO Side	AS5300 Side
Pin 1 Tx Ring	Pin 1 Rx Ring
Pin 8 Tx Tip	Pin 2 Rx Tip
Pin 4 Rx Ring	Pin 4 Tx Ring
Pin 5 Rx Tip	Pin 5 Tx Tip

Figure 3-13 RJ-45 Connector



Programmability

You download the application software to each span controller, enabling independent provisioning of each span as well as each channel.

The ICC supports a number of programmable parameters which allow card customization:

- E1 programmable protocol
- Line build-out
- Gain control
- Timing for system synchronization
- Transmitted timing source
- Line coding
- Frame control

Cisco can assist in creating your parameters on a floppy disk which you load into the VCO/4K.

I/O Interface

The J3 connector is the interface between the I/O Module and the ICC. This includes the following functions:

- Signal buffering
- Transmit clock configuration (per framer)
- Reference clock selection
- Framer host interface and interrupt control

I/O Module Description

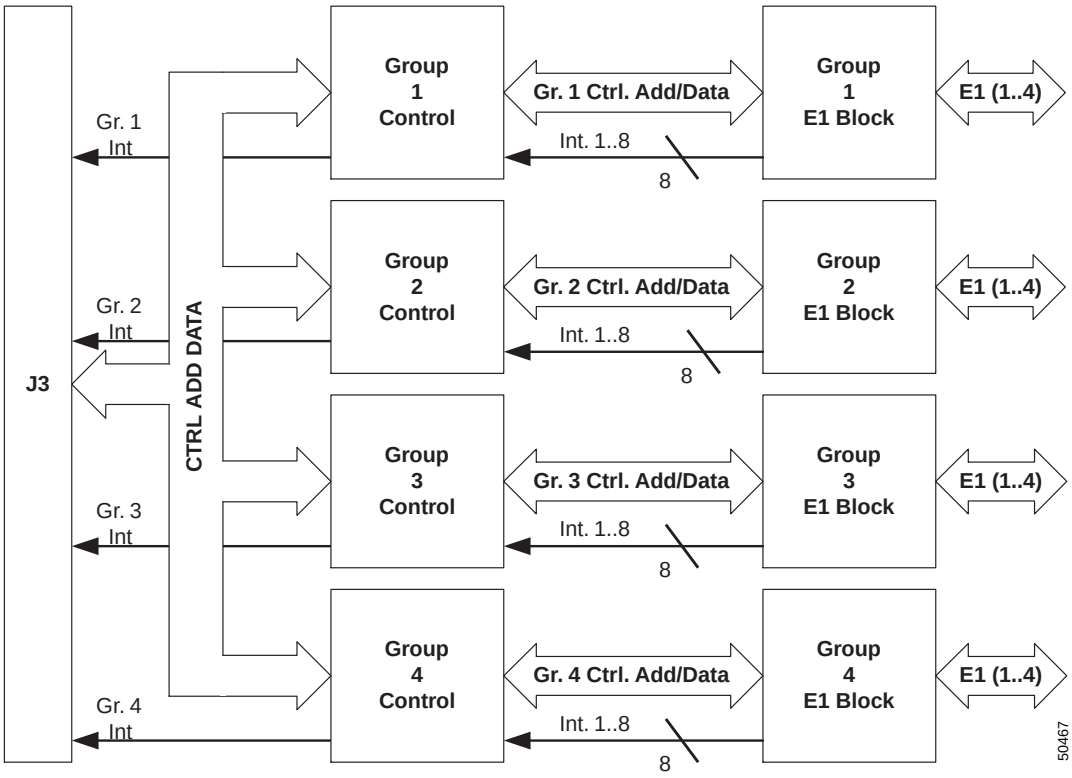
The E1 I/O module supports a 120-ohm network interface for E1.

Note The E1 I/O Module also supports a 75-ohm network interface when optional Balun impedance matching devices are used. (See Technical Bulletin # 63102750100.)

The I/O Module interfaces the VCO/4K system with 4, 8, or 16 E1 digital data carrier streams. Each stream consists of a 2.048-Mbps, 32-channel, bipolar digital data stream (E1). VCO/4K system synchronization may be set to the receive clock of any E1 span on the I/O Module (the Master Timing Link).

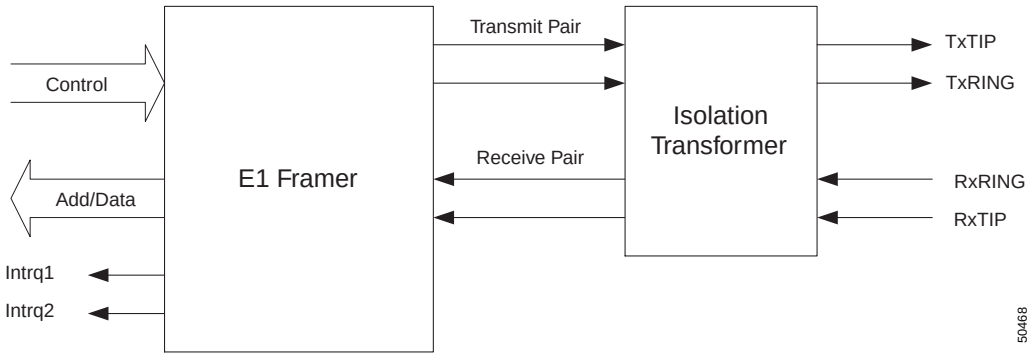
The I/O module framers are segmented into groups of four called Framer Groups. This design approach reduces the chance of a single point of failure on the card. A hardware failure on the I/O Module normally affects only a group (1, 2 or 4 spans) and not the entire I/O Module. Figure 3-14 illustrates the span grouping architecture of the I/O Module.

Figure 3-14 16-Span I/O Module Span Grouping



The E1 framer (Figure 3-15) contains a Line Interface Unit (LIU). The LIU contains three sections: 1) the receiver which handles clock and data recovery, 2) the transmitter which wave shapes and drives the E1 line, and 3) the jitter attenuator.

Figure 3-15 Framer Block Diagram



The LIU adjusts to the E1 signal being received and can handle E1 transmit line lengths to 1.5 km as configured from the Port Configuration screen (see the *Cisco VCO/4K System Administrator's Guide*).

Circuitry on the I/O card detects loss of carrier errors, framing errors, and remote alarms on its incoming E1 stream. It also detects receive/transmit *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different rate, such as in loop-timed configurations. The ICC contains elastic PCM data buffers to minimize slips caused the E1 stream frequency jitter.

Table 3-13 details the E1 I/O Module's input and output stream specifications.

Table 3-13 E1 Stream Specifications

Input Stream	
Format	CAS, Clear Channel, or NET5 ISDN
Data transparency	Alternate Mark Inversion (AMI), Bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, none.
Frequency	2.048 Mbps +/- 50bps
Impedance	120 ohms +/- 10%

Table 3-13 E1 Stream Specifications (continued)

Output Stream	
Format	CAS, Clear Channel, or NET5 ISDN
Data transparency	Alternate Mark Inversion (AMI), Bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, none.
Line Equalization (Drive)	CCITT G.703
Frequency	2.048 Mbps +/- 50bps
Impedance	120 ohms +/- 10%

The combined framer/LIU performs:

- Alarm detection (Remote, All 1s, Carrier Lost, Loss of Sync)
- Alarm injection (Remote and All 1s alarms)
- Error counting (CRC4, frame events)
- Channel separation
- G703 framing and out-of-band channel associated signaling
- Out-of-band CAS signaling (A, B, C & D)
- Data transparency
- AMI, HDB3, data encoding

Note You can use HDB3 for E1 to maintain (1s) density (and timing) while providing data transparency.

- Bipolar-to-TTL conversion on the transmit side
- Electrical wave shaping on the receive side
- Clock recovery
- Jitter attenuation, tolerance, and transfer per G.823
- Loopback and maintenance functions
- Signal monitoring (for loss of signal and quality transmission)

Configuration Notes

There are no jumpers or replaceable PROMs on the I/O Module.

CHAPTER 4

Service Circuit Cards

Integrated Prompt/Record Card (IPRC)

The Integrated Prompt/Record Card (IPRC) is a standard system service circuit card that resides in the Master or any Expansion Port Subrack. It is designed for the system switching product family to play and record digitized voice prompt information. The IPRC is available with the following port configurations:

- 8 playback/4 record ports
- 64 playback/32 record ports
- 128 playback/32 record ports

The IPRC can play voice information on up to 128 channels and record from up to 32 channels. All channels can operate simultaneously. The IPRC supports up to 16 prompt libraries of up to 256 prompts each.

The number and type of IPRCs required by a system is based on anticipated traffic and the call scenario. IPRCs are microprocessor-based and firmware controlled, and are incorporated with the standard system internal control and digital network interfaces.

Specifications

Microprocessor	MC68340 (16 MHz)	
SCSI Interface	NCR53C94 SCSI Controller	
Memory	128 KB EPROM	
	2-16 MB DRAM	
	7 KB Static RAM	
Power Requirements	**Typical**	
	+5 volts	**1.1 amps typical**
Operating Temperature	5 to 50°C	
Relative Humidity	8 to 80% noncondensing	
Physical Dimensions	Height:	15.6 in. (396 mm)
	Depth:	12.1 in. (305 mm)
	Width:	0.79 in. (20 mm)
Voice Playback/Record Channels	8 playback/4 record port	
	64 playback/32 record port	
	128 playback/32 record	
Maximum Prompt Time	35 minutes	
Voice Encoding Method	64 Kb Pulse Code Modulation (PCM)	

Circuit Description

Voice data is stored in DRAM. Upon initialization, announcement data is uploaded and downloaded from the system controller hard disk to the IPRC via a SCSI bus. IPRC ports are allocated and released during a call as specified by the call processing application. The IPRC supports up to 16 prompt libraries, with up to 256 prompts per library and a total duration of 35 minutes. The IPRC plays prompts on up to 128 channels.

Each IPRC port can send prompt messages to any PCM time slot. For a typical call scenario, the application software assigns an IPRC channel to a voice path and then sends available voice prompts. When the IPRC channel is no longer needed, the port is removed from the voice path and the call is allowed to continue. Refer to Figure 4-1 for a functional block diagram.

Note IPRCs are optional in systems, depending on whether the application call scenario requires voice prompting that is not provided by other peripheral equipment.

IPRCs mount in any port card slot and include a microprocessor, speech processing circuitry and requisite firmware.

DRAM Prompt Storage

Prompt data software consists of a series of phrases and scripts which have been converted to digital data. The software is stored on hard disk in the storage subsystem. Prompts are downloaded from the hard disk to an IPRC via the SCSI interface during card initialization.

Prompt data is stored in a 16-MB DRAM controlled by the Packet Processor. The DRAM are 1-Mb x 4 devices. Thirty-five minutes of prompt storage require 32 devices. The IPRC application code and data are also stored in DRAM. The application software controls the output of the prompt data onto the appropriate PCM time slot via a message packet sent over the comm bus.

PCM Time Slot Bus Interface

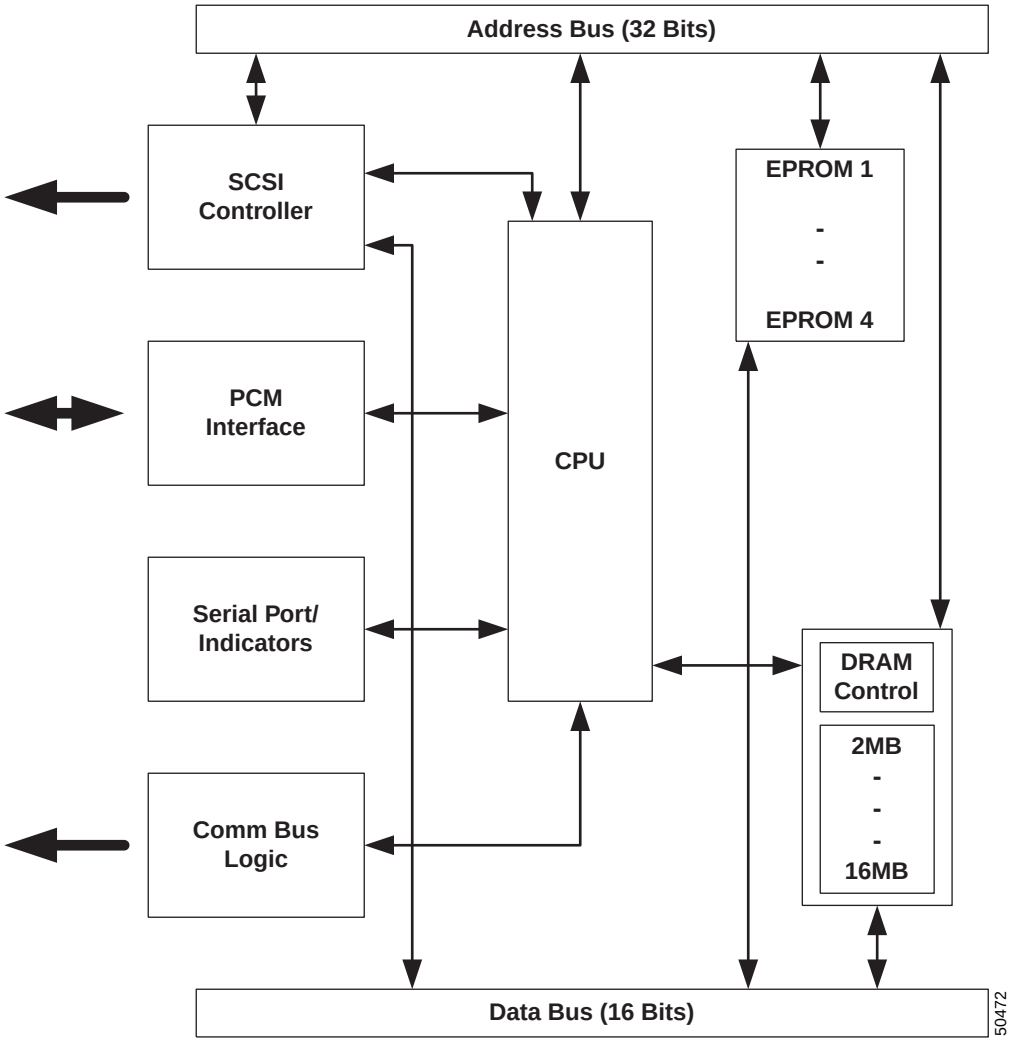
The IPRC PCM Bus Interface consists of dual port RAM to buffer, transmit, and receive PCM data, discrete logic (to control PCM bus access), and one of the internal 68340 timer modules.

The IPRC supports up to 128 channels for prompt playback using two dual port RAM buffers (U22 and U23). Each playback channel requires 32 bytes for PCM buffering, yielding 4KB total dual-port RAM for PCM transmission.

The IPRC supports up to 32 channels for prompt recording using additional dual port RAM buffers.

Each IPRC port interfaces to the PCM bus structure with bus interface circuitry which is common to system port cards. When an IPRC is plugged into the midplane it is automatically assigned a set of a maximum of 128 consecutive port addresses, depending on the IPRC's port configuration. The PCM interfaces control access to the correct PCM time slot on which to send the prompt data.

Figure 4-1 IPRC Functional Block Diagram



Packet Processor

The IPRC contains a 68340-based Packet Processor that interfaces to the comm bus. A packet processor is part of all cards with the exception of the Network Bus Controller (NBC3).

The packet processor consists of the 68340 microcomputer, program and data memory, associated RAM, EPROM, and address decode circuitry, the comm bus interface, an asynchronous serial port, and the LED register. It is via the comm bus that the NBC issues commands to the IPRC in the form of data packets. The IPRC reports the status of its voice channels over the same bus using the data packet protocol. When polled by the NBC, the packet processor reports any status change. The 68340 provides the intelligence for the packet processor and, therefore, for the IPRC.

The packet processor supports a diagnostic serial port connected to a signal line on the backplane and also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

IPRC Status LEDs

The IPRC has three LEDs that are visible through the front panel and two additional internal LEDs that are not visible from the front panel.

Front Panel LEDs

A red, a yellow, and a green LED (DS1, DS2, and DS3, respectively) are visible through the IPRC's front panel to indicate the status of the card. Typically, an illuminated red LED indicates a major card failure, a yellow LED indicates a minor card failure, and a green LED indicates the card is in standby or diagnostic mode. Table 4-1 shows the card status information provided by the illuminated LEDs.

Table 4-1 Front Panel LEDs

Card Status	Green (DS3)	Yellow (DS2)	Red (DS1)
Card Plugged In (not initialized)	On	On	On
Self Test	On	Blinking	Off
Receiving Download	Blinking	Off	Off
Card Out Of Service (OOS)	On	Off	Off
Standby/Diagnostic Mode	On	On	Off
Major Alarm	Off	Off	On
Minor Alarm	Off	On	Off
Card Failure	On	Off	On

Internal LEDs

The red LED inside the front panel (DS5) is tied to the HALT line on the 68340 CPU. DS5 is illuminated when the CPU stops processing.

The green LED inside the front panel (DS4) is the heartbeat indicator for the IPRC. During normal operation, DS4 flashes. Whenever the normal background operation is interrupted (for example, during memory testing), DS4 stops flashing at its last known illumination state.

SCSI Interface

The IPRC uses a SCSI interface to download prompt data to and from the system controller. The SCSI interface is maintained by an NCR 53C94 SCSI Controller, or equivalent, located at U3.

A 16-bit DMA interface is set up between the 68340 and the 53C94 to transfer data between the IPRC DRAM and the SCSI bus. This DMA interface physically exists on the data bus, but program control prevents other devices from using the data bus during DMA operations. The 68340 provides the DMA channel control through the on-chip DMA Module.

IPRC SCSI Cables

The IPRC cards connect to the system controller cards (side A and B) with ribbon cables on the rear of the midplane. One ribbon cable connects from the A-side connector on the small daughter board located on the lower, right side of the midplane as viewed from the rear. Another ribbon cable connects from the B-side connector. These connectors are clearly marked on the daughter board.

The other end of each ribbon cable has connectors for up to four IPRC cards. These are connected to the lower set of pins (J3) on the rear of the midplane for each IPRC installed. Pin 1 on the connector is identified by the red stripe on the ribbon cable. The connectors are installed with Pin 1 facing up.

Note Ensure that each cable connection on the rear of the midplane is aligned with a slot containing an IPRC card.

External Interfaces

This section describes the connectors and jacks on the IPRC.

Note J2 Pin Assignments are proprietary and are therefore not documented for customer use.

J1 Pin Assignments

Table 4-2 lists the pin assignments for J1 on the IPRC.

Table 4-2 IPRC J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5 through 10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14 through 21	Unused	Unused	Unused
22	Card Address Bit 1	Unused	Card Address Bit 0
23	Card Address Bit 3	Unused	Card Address Bit 2
24	Card Address Bit 5	Unused	Card Address Bit 4
25	Card Address Bit 7	Unused	Card Address Bit 6
26	SRV	Unused	Unused
27	DID	Unused	Unused
28	RST	Unused	Unused
29 through 31	Unused	Unused	Unused
32	DGND	Unused	DGND

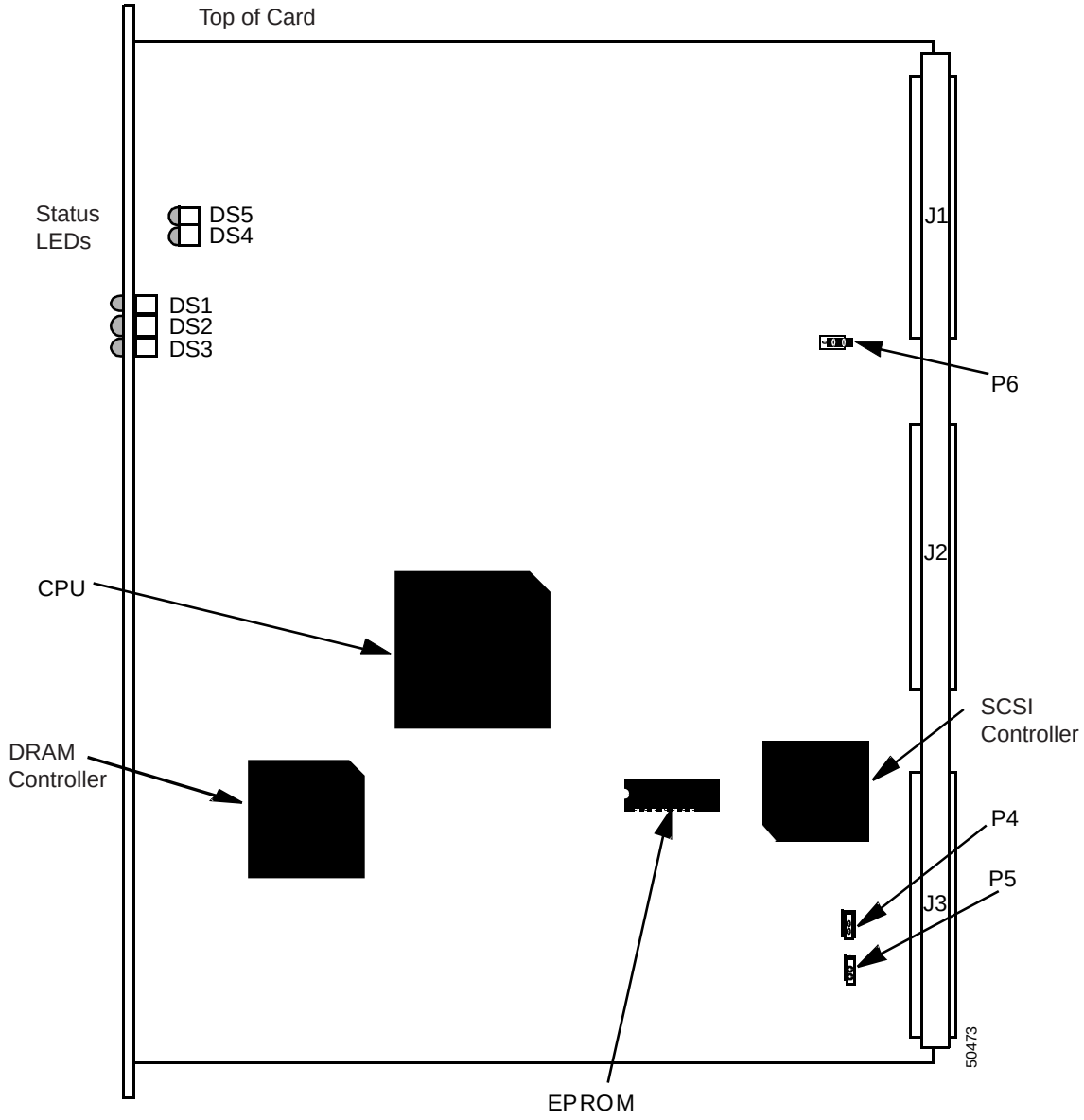
J3 Pin Assignments

The IPRC uses the first 25 pins on J3 rows A and C for SCSI bus signals. Table 4-3 specifies the pin connections.

Table 4-3 J3 Pin Assignments

Pin	Row A	Row B	Row C
1	SD0	Unused	DGND
2	SD1	Unused	DGND
3	SD2	Unused	DGND
4	SD3	Unused	DGND
5	SD4	Unused	DGND
6	SD5	Unused	DGND
7	SD6	Unused	DGND
8	SD7	Unused	DGND
9	SDP	Unused	DGND
10 through 12	DGND	Unused	DGND
13	TPWR	Unused	DGND
14	DGND	Unused	DGND
15	DGND	Unused	DGND
16	ATN	Unused	DGND
17	DGND	Unused	DGND
18	BSY	Unused	DGND
19	ACK	Unused	DGND
20	SRST	Unused	DGND
21	MSG	Unused	DGND
22	SEL	Unused	DGND
23	CD	Unused	DGND
24	REQ	Unused	DGND
25	1O	Unused	DGND
26 through 32	Unused	Unused	Unused

Figure 4-2 IPRC Jumper and EPROM Locations



Front Panel Jack (P2)

The IPRC has a front panel jack used to access internal diagnostics and internal debugger utilities, and to obtain run-time status/error messages. The front panel jack is an asynchronous serial port that is configured at 9600 baud, 8 bits, no parity. The front panel jack accepts the standard phone jack used on all system port cards.

Configuration Notes

The IPRC is manufactured by Cisco Systems, Inc. Jumper plugs are factory set for use in systems. Figure 4-3 and Figure 4-4 show the location of the factory set jumpers. Refer to the jumper settings to verify configuration jumper settings prior to installing the IPRC in a Port Subrack.

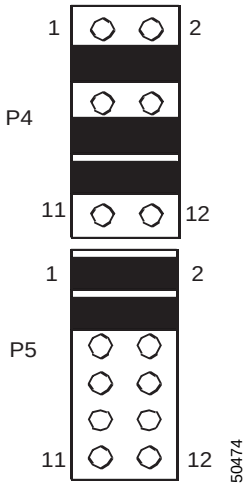
Note Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.

If a card is improperly configured, it may fail to operate. Be certain to verify configuration settings before installing a replacement service circuit card in the system.

EPROM Select Jumpers

The IPRC is provided with an EPROM in socket U2. The default jumper configuration of P4 and P5 for 1 Mb (128k x 8), is shown in Figure 4-3.

Figure 4-3 P4 and P5 Jumper Placement

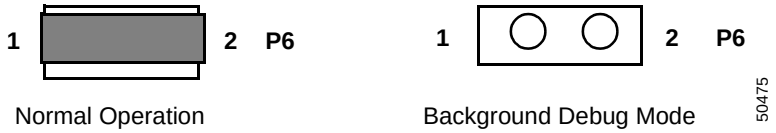


Reset Jumper

Jumper J6 is used to disconnect the Reset signal from the system backplane to the IPRC. Removal of this jumper prevents the NBC from resetting the IPRC. Remove this jumper only when using the background mode debugger on the IPRC on a system environment. During background mode debug operations, normal program execution on the 68340 is interrupted. Failure to remove this jumper during debugging results in the IPRC being reset as soon as the 68340 is placed in debug mode.

Figure 4-4 shows the jumper configuration for normal and background mode operation. The Normal Operation setting is the default.

Figure 4-4 P6 Jumper Placement



Software Configurable Port Limitation

When an IPRC is added to the system, it is defined with the physical number of ports. The 64 and 128 port IPRC configurations may also be configured to support less than the physical port capacity. This feature enables the user to configure the port density in 8-port increments through the IPRC Card Configuration screen. (Refer to the *Cisco VCO/4K System Administrator's Guide* for more information.) The screen processing frees up or reallocates time slots based on the defined port density.

Subrate Switching Card (SSC)

The Subrate Switching Card (SSC) is a service circuit card that occupies a single card slot in the VCO/4K.

The SSC allows the VCO/4K system to switch voice and data calls at N x 8 kbps rates (where N equals the number of channels). With the SSC, service providers can improve trunk efficiency up to eight times by "packing" eight subrate channels within a traditional 64 kbps channel.

The SSC enables VCO/4K switches to be used as Base Station Controllers (BSCs) in wireless telephone networks or other networks that carry compressed audio.

You can remove or replace the SSC without shutting off the system.

The SSC supports a switching matrix of up to 2000 64-kbps time slots, allowing up to 16,000 8-kbps subrate connections.

Specifications

Microprocessor:	(1) MC68360
Memory:	1 MB DRAM
	128 KB EPROM
Power Requirements:	30 Watts @ 5 VDC max
	.5 Watts @ 15 VDC
	.5 Watts @ –15 VDC

Redundancy

Redundant SSC operation requires that two SSC cards be present—an active card and a standby card. The standby card is responsible for verifying the operational status of the active card. When the standby card determines that the active card has failed, the standby card:

- Becomes active
- Informs the generic software of the failure
- Waits for the system to control the switchover to active status

Subrate switching requires that both the active and standby SSCs be located in the same rack and on the same level.

The presence of an SSC does not affect system level redundancy.

Circuit Description

The SSC controls the subrate switching matrix with one Motorola MC68360 QUICC (QUad Integrated Communications Controller).

Circuitry

The SSC includes the following circuitry:

- Clock drivers—Provide clock synchronization for the subrate switching matrix.
- PCM interface—Provides a common interface to the backplane for the subrate switching matrix; provides C-Bus access, which enhances the available time slot count to 4,096 time slots. The PCM interface is hyperchannel compatible (assuring constant delay through the SSC) for any combination of time slots, which allows for subchannels.
- High-speed communications bus—Provides automatic high-speed communications to the system controller when used in conjunction with the NBC3.

Configuration Notes

Hardware Configuration

The following list provides hardware configuration information for the SSC.

- There are no configurable jumpers on the SSC.
- The SSC does not require an MDF Adapter.

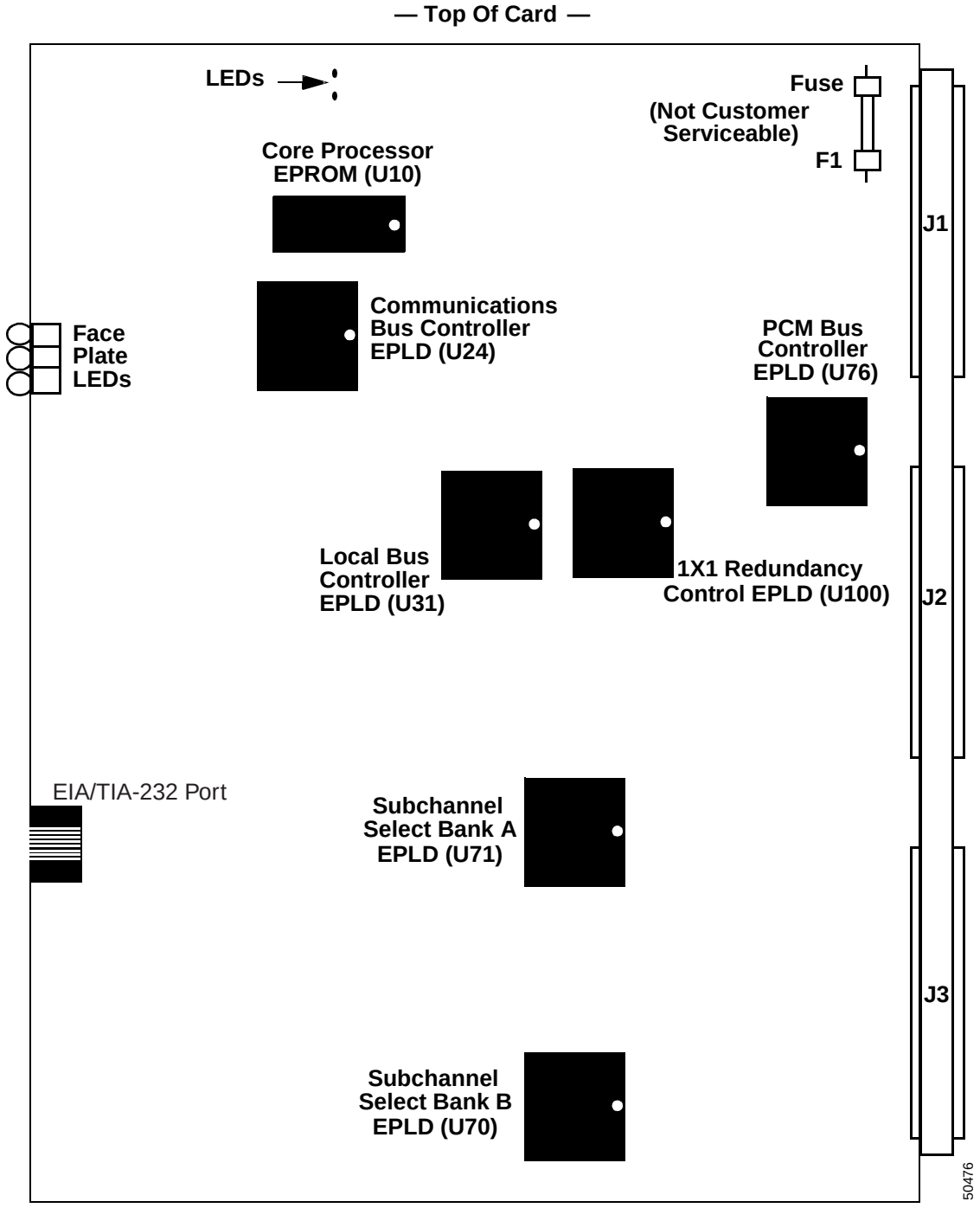
Software Configuration

All configuration parameters for the SSC are configured in software through the administration interfaces. There are no hardware options that you can select on the SSC.

The application software, downloaded to the SSC, enables control and configuration of the card, as well as each subrate channel. For more information about configuring subrate service, refer to the Subrate Configuration screen in the *Cisco VCO/4K System Administrator's Guide*.

Figure 4-5 shows the layout of the SSC.

Figure 4-5 Subrate Switching Card Board Layout



Service Platform Card (SPC)

The Service Platform Card (SPC) provides the service resources element of the three critical system elements of the VCO/4K — system control, port interfaces, and service resources. The SPC allows any service resource function of the VCO/4K to be performed with this card as a base platform, given a minimum of one Service Resource Module (SRM) mezzanine card on the board to perform the service function(s). Mezzanine cards have the capability to perform more than one service function, and to perform these functions simultaneously.

Some other features of the SPC:

- Improved system reliability and error detection capabilities
- Flash memory, which allows faster system boot time, and reduces the amount of communications bus traffic
- FPGA architecture, which supports a soft-configured system boot for easier hardware upgrades
- Ability for users to replaced the card with system power on
- Support for up to 2016 concurrently active service circuits per SPC
- Diagnostics support
- Compatiblity with 2K and 4K port systems
- Programmable service facility software support
- Support for up to 32 DSP engines with four SRM cards populated
- Ability for users to independently define each DSP service engine with a service resource function

Specifications

Compliance with Standards

The SPC Card is in compliance with all applicable U.S. and international standards. Refer to Table 4-4.

Table 4-4 SPC Standards Compliance

Category	Standard
Safety	UL1459
	CSA C22.2
	EN-60950
	IEC-950
EMI/EMC	FCC Part 15 (US/Canada)
	EN55022 (Europe)
	EN50082-1 (Europe)
	VCCI (Japan)
PCB Manufacture	IPC

SPC Card Specifications

Microprocessor	MPC860MHZP-50
Memory	8 MB Flash 16 MB DRAM 3.3V DO-DIMM EDO 60ns
Power Requirements (5V converted to 3.3V on the board)	5 Volts – 1.5A - board only, no SRMs (Max) 5 Volts – 1.0A - each SRM (Max) 5 Volts – 5.5A - board with four SRMs (Max)

SPC Card Architecture

The SPC is a single-slot card. Up to four separate SRMs, mounted as mezzanine cards, provide processing resources.

The SPC is inserted in the VCO/4K switch from the front of the system.

The SPC contains the following elements:

- Core Processor (HDLC-based multiprocessor architecture and command/response data routing)
- Communications Bus Interface
- Up to four SRMs (DSP-based service engine, mezzanine interface architecture, and serial mezzanine boot control), programmable for application requirements
- Memory subsystem (memory controller, DRAM, and Flash memory)
- PCM Interface (bus support)
- Power Subsystem

The block diagram for the SPC and SRM Modules is shown in Figure 4-6.

The SPC hardware layout is shown in Figure 4-7.

Figure 4-6 SPC and SRM Module Block Diagram

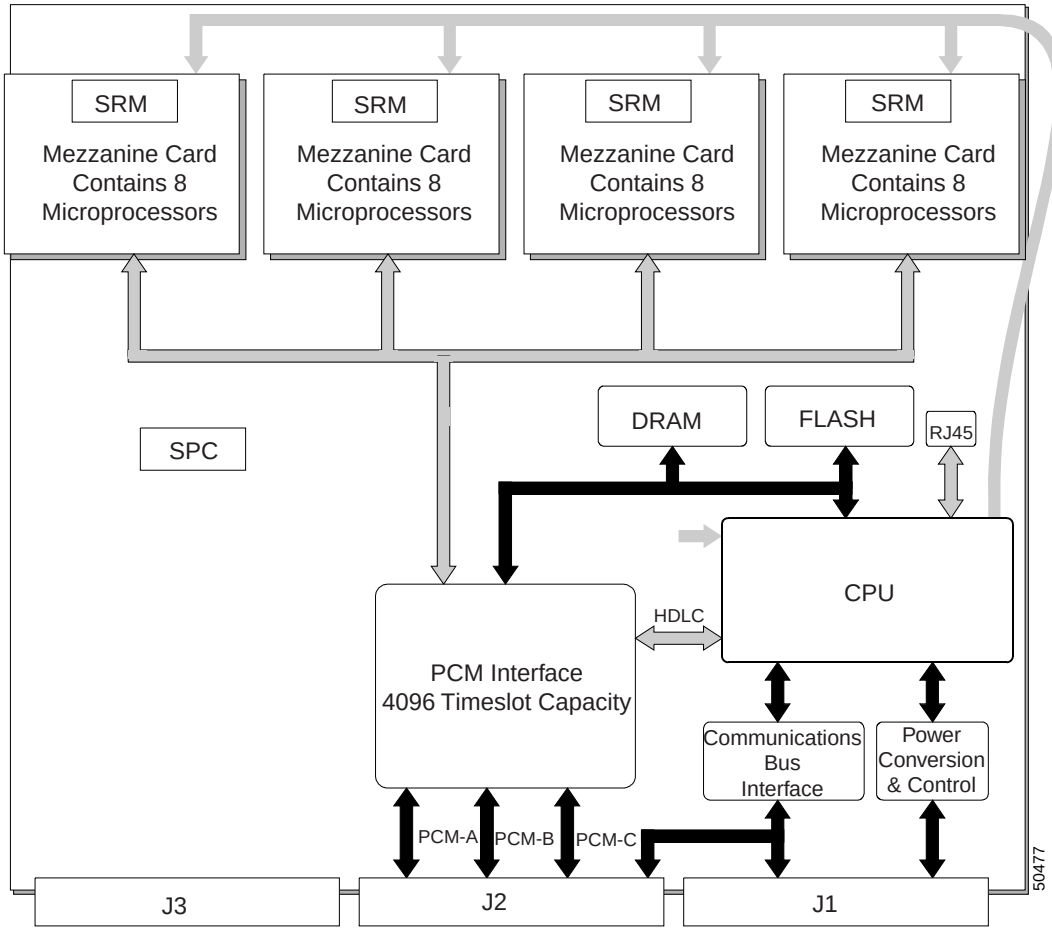
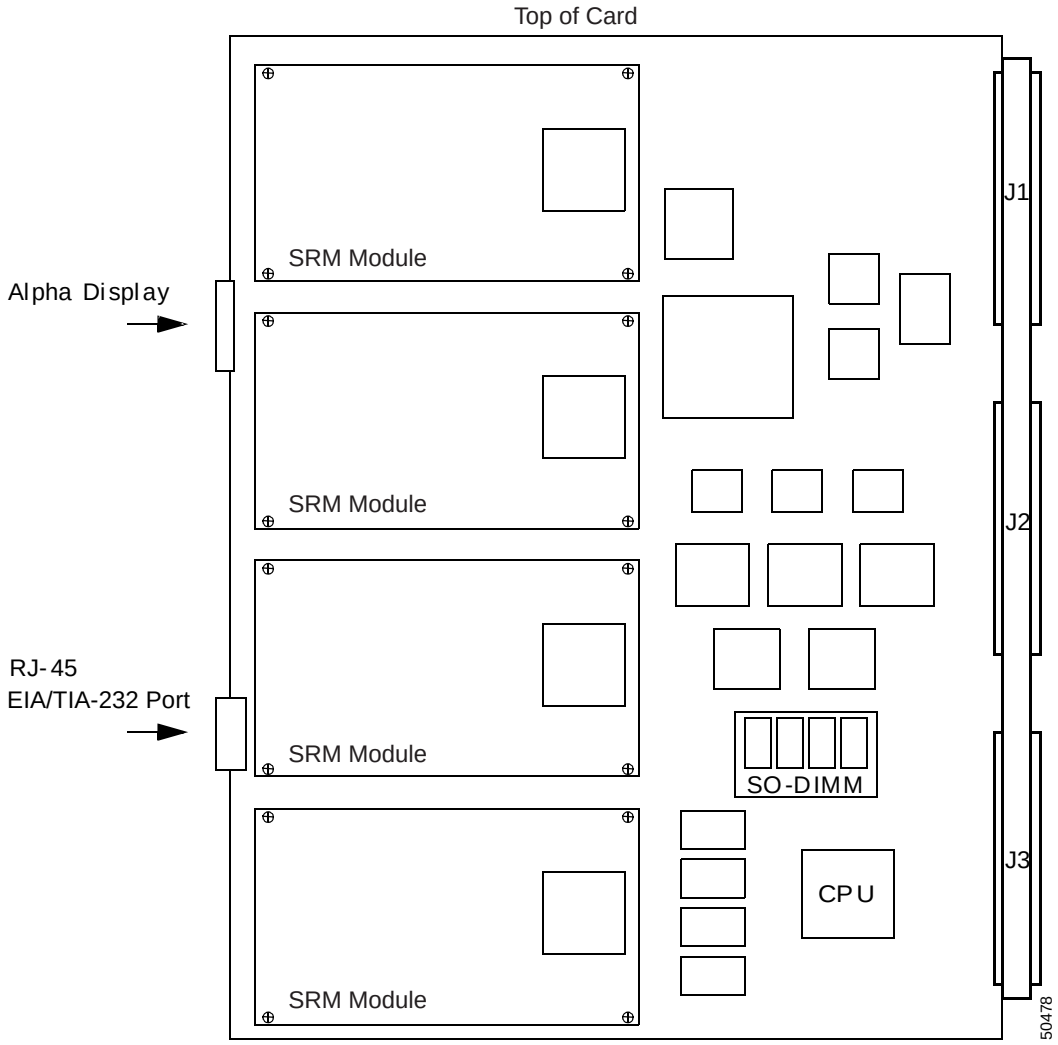


Figure 4-7 SPC Layout (Component Side)



Note Not all components are shown.

Core Processor

The processor and associated peripheral circuitry on the SPC is called the *Core Processor*. The Core Processor runs the card level application and diagnostics and is responsible for managing all SPC-based and mezzanine peripheral devices described in the sections that follow.

Features shown in Figure 4-6 are discussed in this section at a high level.

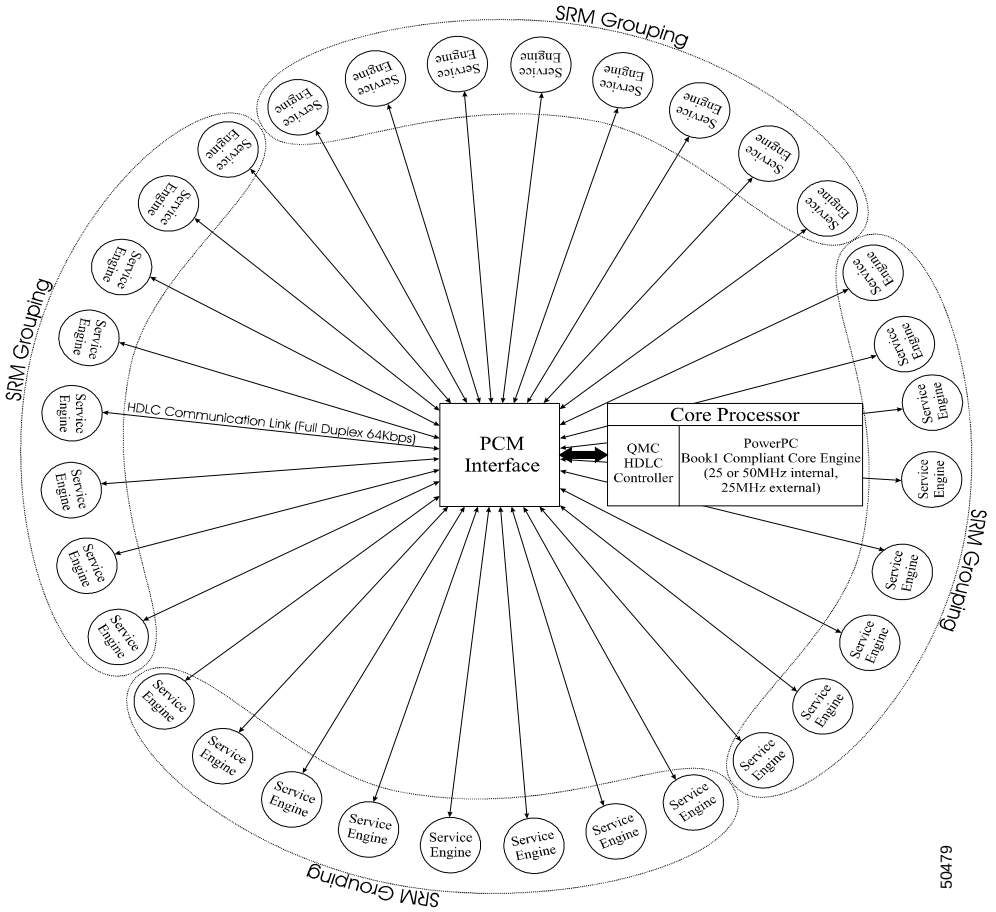
Core Processor Implementation

The Core Processor comprises the Motorola MPC860MHZP-50 CPU and associated peripherals and support circuitry. The main timing reference for the Core Processor is supplied by an on-board 3.3V crystal oscillator.

HDLC-based multiprocessor Architecture

The SPC's architecture is dependent on a centralized (time division multiplexed and switched) HDLC controller connected to service engines (SEs) in a traditional multiprocessor star arrangement. In the SPC's particular implementation of this architecture, the HDLC controller is contained within the Core Processor. The PCM interface acts as the switching device, which spreads the communication time slots across the service engines. Refer to Figure 4-8.

Figure 4-8 HDLC Command/Control Processor Arrangement



The central processor is responsible for command and response message control of any service engine, or any combination of service engines. The use of HDLC in this star manner has several benefits for the SPC:

- The Core Processor uses an on-board RISC engine, called the CPM (Communication Processor Module). The CPM manages all protocol specific actions.

- The CPM handles data in a multichannel mode. This allows up to 64 (32 used in the SPC architecture) separate DMA channels, each one dedicated to a single HDLC full-duplex pipe to a service engine.
- The physical arrangement and PCM interface facilitates the distribution of the 32-channel HDLC command pipes to the service engines on the SRMs.

Command / Response Data Routing

The Communications Processor Module within the MPC860MHZP-50 is internally routed to the time slot assigner. The transmit and receive data is routed through the TDMA interface to devices external to the MPC860MHZP-50. Once the data leaves the Core Processor, it has a time division multiplexed arrangement. This serial data is then routed to the PCM interface, where it is switched under the control of the Core Processor so the time slots are rerouted to the 32 service engine bound serial streams which contain regular PCM traffic. These 32 serial streams connect the service engines with the PCM interface.

The PCM interface routes 32 serial streams running at 4.096 Mbps each to the mezzanine card locations. Eight of the thirty-two streams are used by each mezzanine location. Each mezzanine card contains eight DSP Service Engines, each receiving one 4.096 Mbps, 64-time slot, serial, full duplex stream. One 64-kbps time slot from each stream is dedicated to the HDLC command/response data.

Alpha Display/Power Failure LED

The SPC card displays status on a 5x7 alpha display located on the SPC front panel. Table 4-5 defines the alpha display states.

Note The SPC has a card failure LED immediately above the Alpha display. This LED indicates a major SPC circuit failure. If this is lighted, remove and reinsert the card. If the light illuminates again, replace the card.

Table 4-5 Alpha Display States

Display	Meaning
First Six Rows	
SPC	Card is SPC
Rotating line pattern	Download Progress Meter
Bottom Row	
1st LED (left) through the 4th LED (right)	Indicators for SRMs 1 through 4. A blinking LED indicates the associated SRM is configured. A constantly lighted LED indicates the SRM is populated but not configured. An unlighted LED indicates the SRM is not populated.
5th LED (right)	Heartbeat indicator. Normal operation is one on/off cycle per second. Erratic cycle may indicate a card overload. A stopped cycle may indicate a card failure (reboot or replace).

Communications Bus Interface

The communications bus is used by the Core Processor to communicate with the NBC. The communications bus interface protocol is managed by hardware-based state machines assisted by an interrupt-based CPU support mechanism.

Supported features include high-speed parallel communications to the NBC3 and Flash memory CPU-assisted download capability.

Service Resource Modules

Each Service Resource Module (SRM) contains multiple service engines. Each engine consists of a single digital signal processor (DSP) and associated RAM. The design of the SRM ensures that each service engine is a totally independent entity. Up to four SRMs may be populated per SPC, with eight engines per SRM.

Each service engine is connected to the PCM serial highways (and the PCM interface) through the mezzanine interface. These PCM serial highways contain both PCM data and command/response HDLC traffic from the core processor.

DSP-Based Service Engine

A service engine incorporates a 16-bit, fixed-point, digital signal processor (DSP) and SRAM memory. This signal processing engine contains several interface mechanisms:

- One TI TMS320LC548 (66 MHz) DSP
- Two buffered serial ports
- One time division multiplexed interface serial port
- One host port interface
- 64KB SRAM

Mezzanine Interface Architecture

The mezzanine interface is based upon a TDM traffic switched HDLC command/response architecture (refer to the “HDLC-based multiprocessor Architecture” section on page 4-17), with status and control registers for proper identification and reset control over the mezzanine locations. Additionally, the mezzanine interface uses a serial boot mechanism as its sole core processor master-to-slave boot device.

Serial Mezzanine Boot Control

The SRM core processor provides serial boot control of the mezzanine SRMs. A continuous serial stream of boot code is targeted at a single DSP or to a group of DSP service engines. Any individual DSP or group of DSPs may be booted simultaneously.

Programmability

The SPC supports a variety of service facilities implemented via software. This application software executes on the SRM's DSPs. This allows the SPC to support multiple tone plans and easily updated algorithm changes.

The following services are provided:

- DTMF detection
- Call progress analysis
- MF reception
- MFCR2 reception and transmission
- Tone generation
- DTMF and MF outpulsing
- Call conferencing

The individual SEs operate independently. This results in the ability to:

- Download a service algorithm to one SE while the others are in service
- Download different service algorithms to different SEs
- Set or change the parameters of one SE while the others are in service
- Configure the same service algorithm to multiple SEs

Memory Subsystem

The memory subsystem comprises components that interface to the Core Processor External Bus Interface. The Core Processor external bus consists of a 32-bit address bus, a 32-bit data bus, and several control signals to interface to a wide range of devices. This section discusses the configuration of the SPC's memory subsystem, which includes the FLASH and DRAM components.

Memory Controller

The interface between the Core Processor and external devices uses control signals and a configurable memory controller contained within the MPC860MHZP-50.

DRAM

DRAM is provided by 72-pin standard 32-bit wide Extended Data Out (EDO) 3.3V SO-DIMMs. SO-DIMM support is for multiple-bank 1 to 64-MB modules with a maximum of two banks per module.

FLASH Memory

Flash memory is the boot device. 8 MB of Flash are available for SPC and SE code to minimize boot-up time. The system controller can upgrade Flash memory without users having to remove the card because the Flash is hot-socketed.

PCM Interface

The SPC PCM interface delivers up to 2016 time slots from the system backplane to service resources located on serial streams internal to the SPC. The PCM interface is a full duplex mechanism, capable of time-space-time switching on both the transmit and receive paths. Per time slot loopback is provided for diagnostic mechanisms. Non-bandwidth-impacting loopback is provided to facilitate algorithms.

Bus Support

There are three PCM buses on the VCO/4K backplane, known as the A, B, and C buses. The A and B buses are 8-bit parallel buses running at 8.192 MHz; the C-bus runs at 16.384 MHz. The C-bus is used with the ICC to achieve the extended port capacity of the VCO/4K.

The PCM interface performs the actual switching function. The interface routes 2016 full-duplex time slots to the mezzanine interface and consists of functionally separate transmit, receive, and NBI switch matrixes.

The interface is of the nonblocking *time-space-time* type and is completely controlled by the local core processor.

Power Subsystem

The power subsystem provides power to the on-board and mezzanine-based components on the SPC/SRM board pair, as well as protection from noise, overcurrent, and under and over voltage conditions. Alarming and voltage-monitored reset signals are provided to the core processor.

The power subsystem within the SPC mainboard is based upon two main functional components, the hot swap controller and the switching regulator. These components act together to protect the system from instantaneous current demands on any power rail that the SPC connects to, and additionally, to protect the SPC from dangerous events on the rails it depends upon.

Configuration Notes

The SPC is software configurable via downloads and Flash only. There are no jumpers, sockets, or replaceable PROMs on the SPC.

Note An SRM that is configured in the database but is not physically installed will appear in the M (maintenance) state rather than the O (OOS) state.

Removal and Replacement Procedures

Follow the directions in Chapter 1, "VCO/4K Card Overview" to remove or replace an SPC.

Removing an SRM

To remove an SRM:

Caution Make sure you observe proper ESD procedures when handling this card. Have a wrist strap in place before replacing the card.

Step 1 Remove the SPC card.

Step 2 Using a screwdriver, remove the four screws holding the SRM in place (one at each corner). Ensure all hardware, including washers, is retained.

Step 3 Gently remove the SRM, grasping it by the edges.

Step 4 Replace the screws and washers on the SPC for future use.

Step 5 Replace the SPC card in the system.

Adding an SRM

To add an SRM:

Caution Make sure you observe proper ESD procedures when handling this card. Have a wrist strap in place before replacing the card.

Step 1 Remove the SPC card.

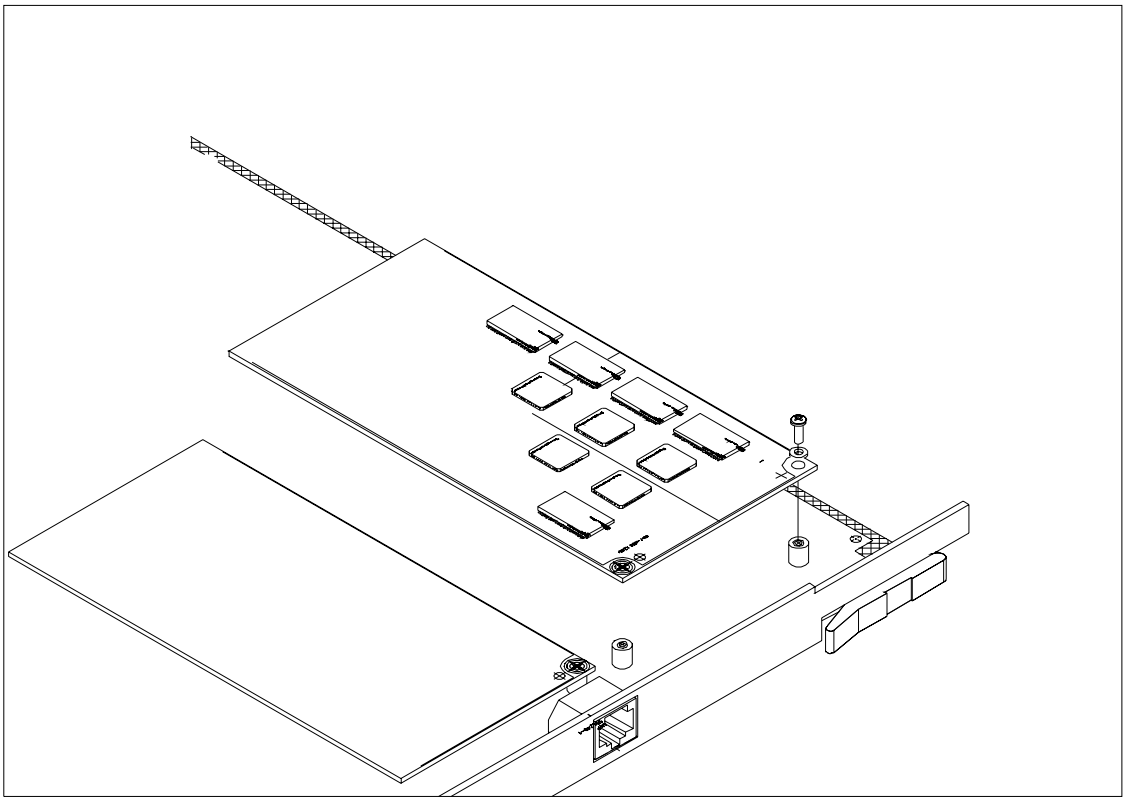
Step 2 Using a screwdriver, remove the four screws and washers in the empty SRM location.

Step 3 Gently insert the SRM on the two connectors. Be careful not to bend the board as you insert it. The large, square Altera component should face the back (connector side) of the SPC (refer to Figure 4-7). (The SRM is keyed to prevent improper insertion.)

Caution Do not press on semiconductor devices. Pressing above connectors, firmly snap in one and then the other connector. Hand tighten with screwdriver.

Step 4 Secure the SRM (refer to Figure 4-9) with the four screws and washers removed in Step 2.

Figure 4-9 Securing the SRM



Step 5 Replace the SPC card in the system.